



**THE DATASHEET OF
IRL1404LPBF**



International IOR Rectifier

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

Description

Seventh Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL1404L) is available for low-

Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|---|-----------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 160 [Ⓓ] | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10\text{V}$ | 110 [Ⓓ] | |
| I_{DM} | Pulsed Drain Current [Ⓛ] | 640 | |
| $P_D @ T_A = 25^\circ\text{C}$ | Power Dissipation | 3.8 | W |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 200 | W |
| | Linear Derating Factor | 1.3 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy [Ⓜ] | 520 | mJ |
| I_{AR} | Avalanche Current [Ⓛ] | 95 | A |
| E_{AR} | Repetitive Avalanche Energy [Ⓛ] | 20 | mJ |
| dv/dt | Peak Diode Recovery dv/dt [Ⓝ] | 5.0 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|--|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 0.75 | °C/W |
| $R_{\theta CS}$ | Case-to-Sink, Flat, Greased Surface | 0.50 | — | |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mounted) [Ⓞ] | — | 40 | |

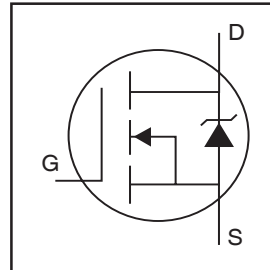
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PD - 95148

IRL1404SPbF

IRL1404LPbF

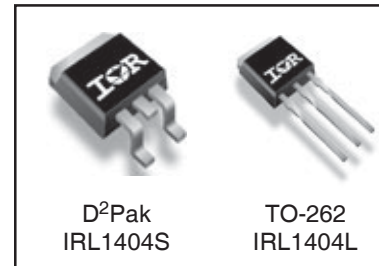
HEXFET® Power MOSFET



$$V_{DSS} = 40\text{V}$$

$$R_{DS(on)} = 0.004\Omega$$

$$I_D = 160\text{A}^{\text{Ⓓ}}$$

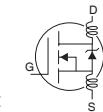


IRL1404S/LPbF

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--|------|-------|-------------|----------|--|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.038 | — | V/°C | Reference to 25°C , $I_D = 1\text{mA}$ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.004 | Ω | $V_{GS} = 10V, I_D = 95A$ ④ |
| | | | | 0.0059 | | $V_{GS} = 4.3V, I_D = 40A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | — | 3.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 93 | — | — | S | $V_{DS} = 25V, I_D = 95A$ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 20 250 | μA | $V_{DS} = 40V, V_{GS} = 0V$ $V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage Gate-to-Source Reverse Leakage | — | — | 200 -200 | nA | $V_{GS} = 20V$ $V_{GS} = -20V$ |
| Q_g | Total Gate Charge | — | — | 140 | | $I_D = 95A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 48 | nC | $V_{DS} = 32V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 60 | | $V_{GS} = 5.0V$, See Fig. 6 ④ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 18 | — | ns | $V_{DD} = 20V$ $I_D = 95A$ $R_G = 2.5\Omega$ $V_{GS} = 4.5V$ $R_D = 0.25\Omega$ ④ |
| t_r | Rise Time | — | 270 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 38 | — | | |
| t_f | Fall Time | — | 130 | — | | |
| L_D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| L_S | Internal Source Inductance | — | 7.5 | — | | |
| C_{iss} | Input Capacitance | — | 6600 | — | pF | $V_{GS} = 0V$ |
| C_{oss} | Output Capacitance | — | 1700 | — | | $V_{DS} = 25V$ |
| C_{rss} | Reverse Transfer Capacitance | — | 350 | — | | $f = 1.0\text{MHz}$, See Fig. 5 |
| C_{oss} | Output Capacitance | — | 6700 | — | | $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ |
| C_{oss} | Output Capacitance | — | 1500 | — | | $V_{GS} = 0V, V_{DS} = 32V, f = 1.0\text{MHz}$ |
| $C_{oss\ eff.}$ | Effective Output Capacitance ⑤ | — | 1500 | — | | $V_{GS} = 0V, V_{DS} = 0V$ to $32V$ |



Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|-------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 160 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 640 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 95A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 63 | 94 | ns | $T_J = 25^\circ\text{C}, I_F = 95A$ |
| Q_{rr} | Reverse Recovery Charge | — | 170 | 250 | nC | $di/dt = 100A/\mu s$ ④ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

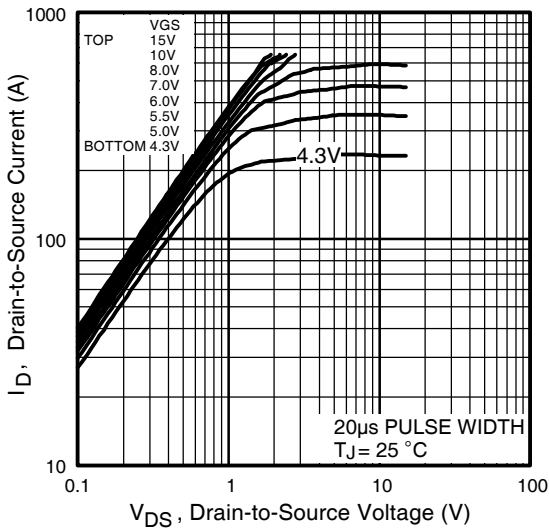


Fig 1. Typical Output Characteristics

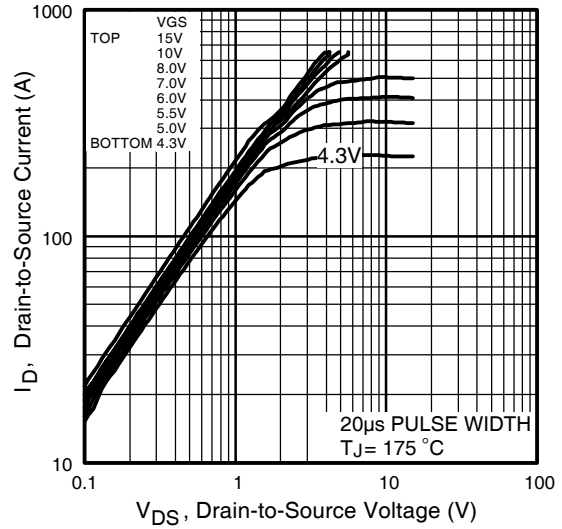


Fig 2. Typical Output Characteristics

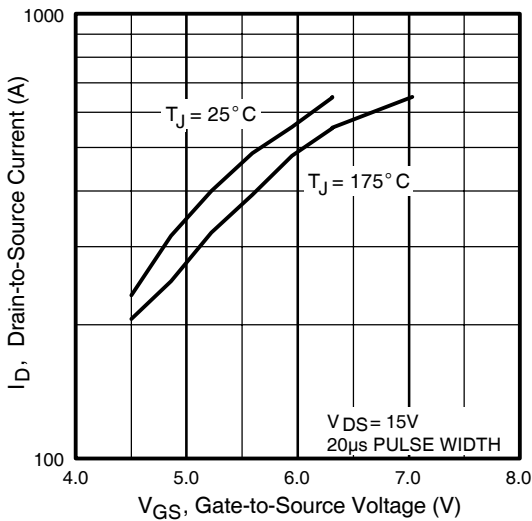


Fig 3. Typical Transfer Characteristics

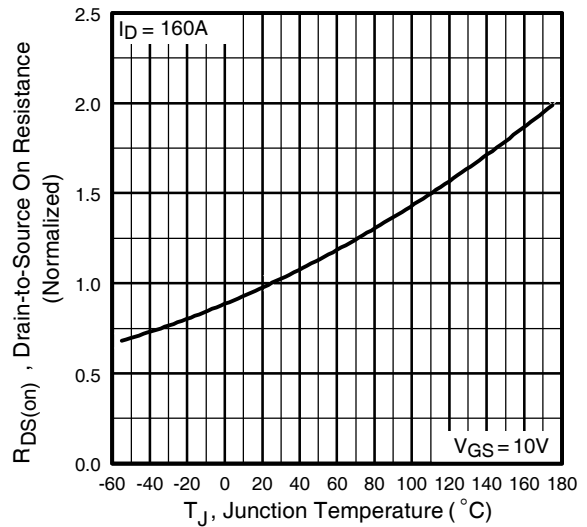


Fig 4. Normalized On-Resistance Vs. Temperature

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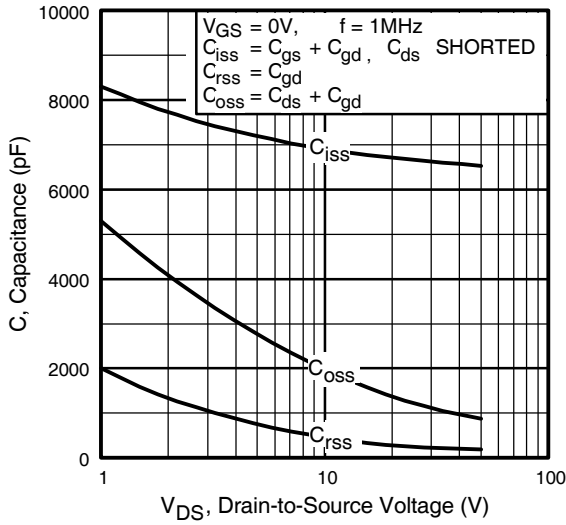


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

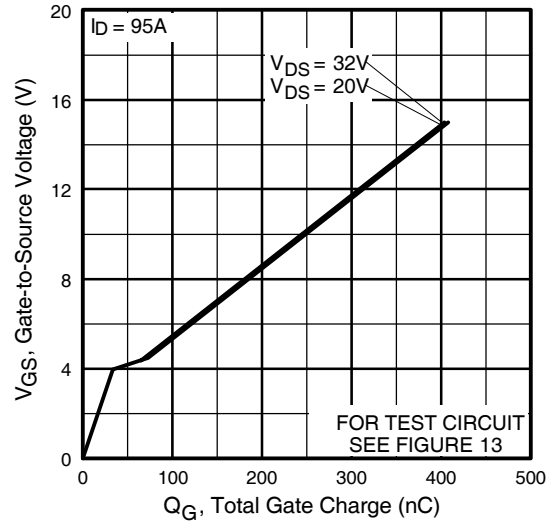


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

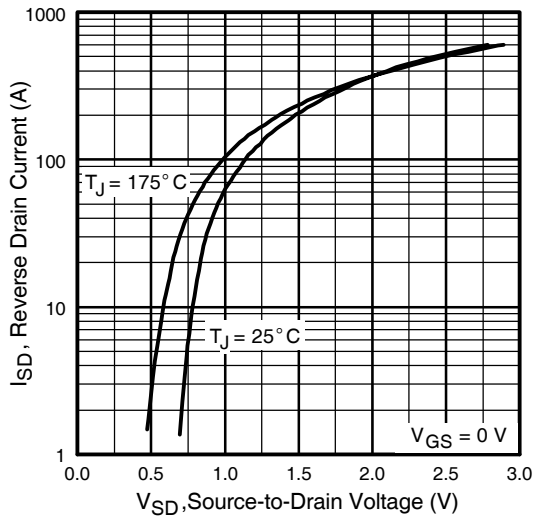


Fig 7. Typical Source-Drain Diode Forward Voltage

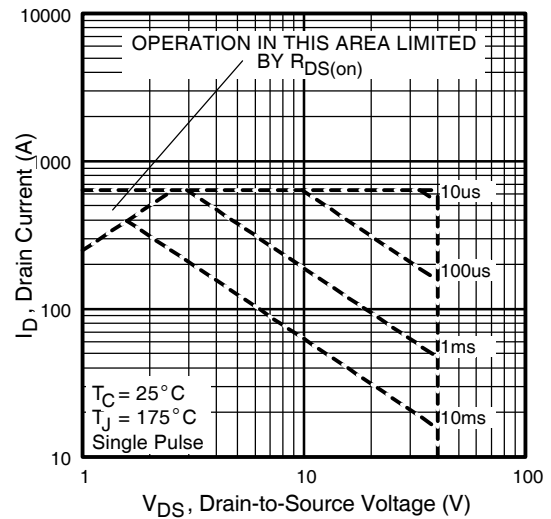


Fig 8. Maximum Safe Operating Area

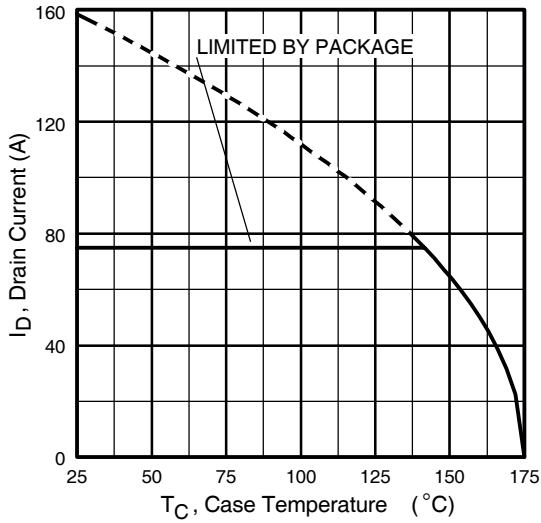


Fig 9. Maximum Drain Current Vs. Case Temperature

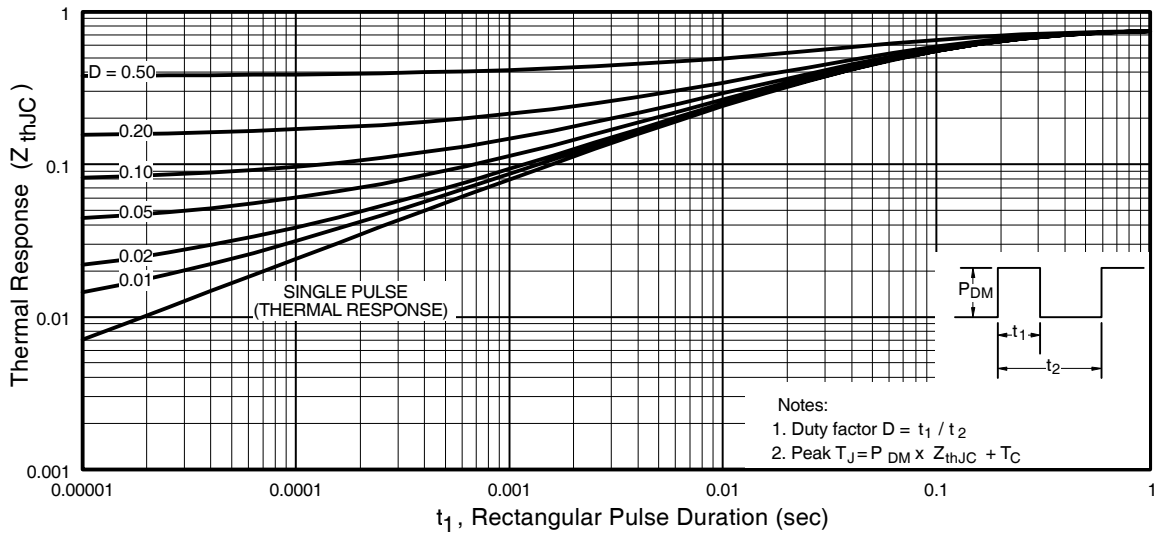
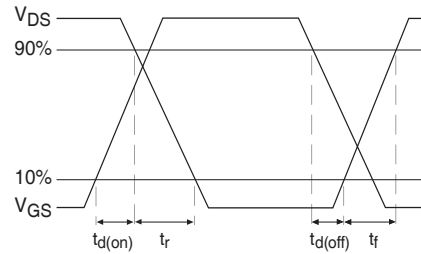
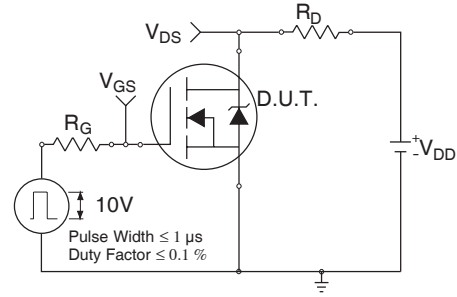


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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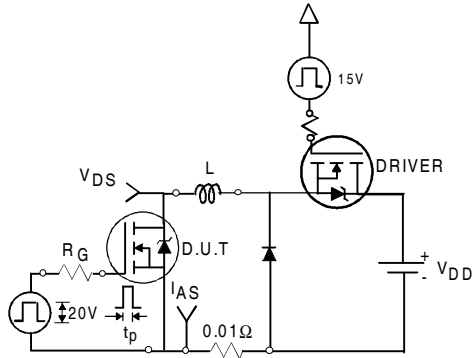


Fig 12a. Unclamped Inductive Test Circuit

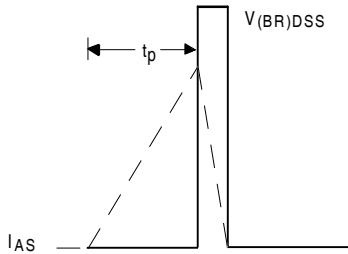


Fig 12b. Unclamped Inductive Waveforms

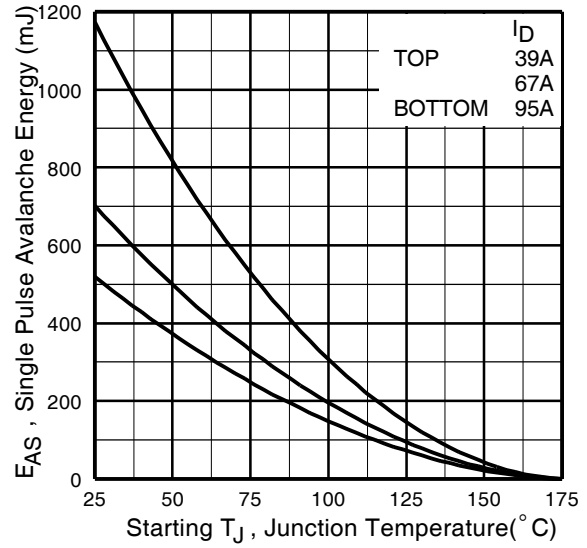


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

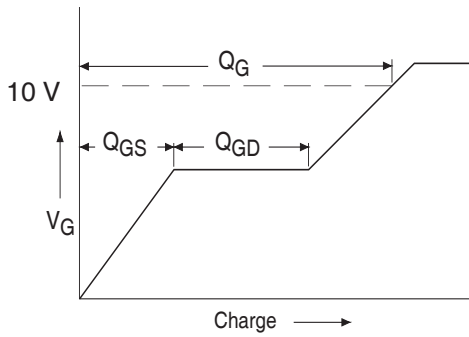


Fig 13a. Basic Gate Charge Waveform

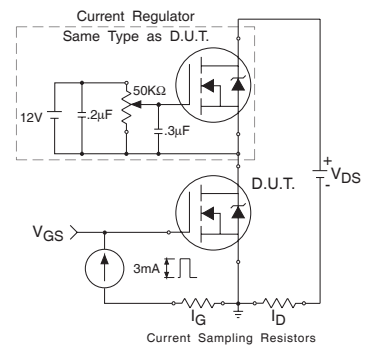
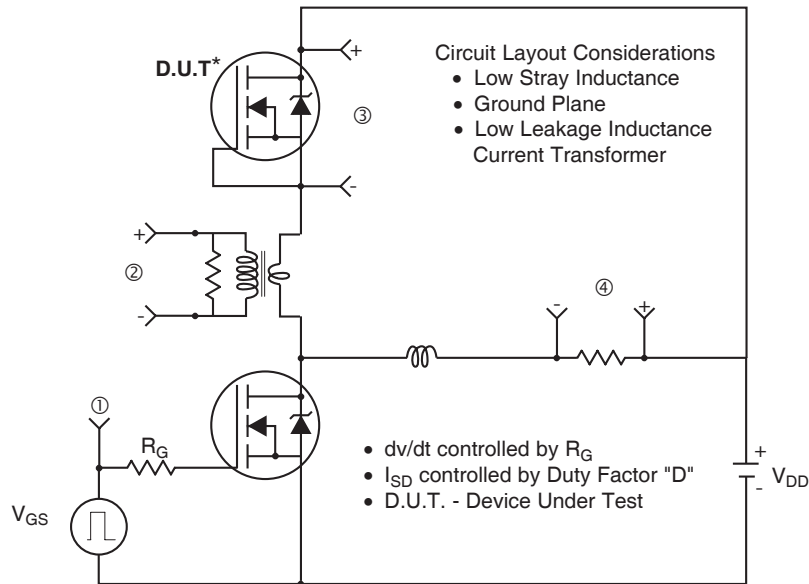
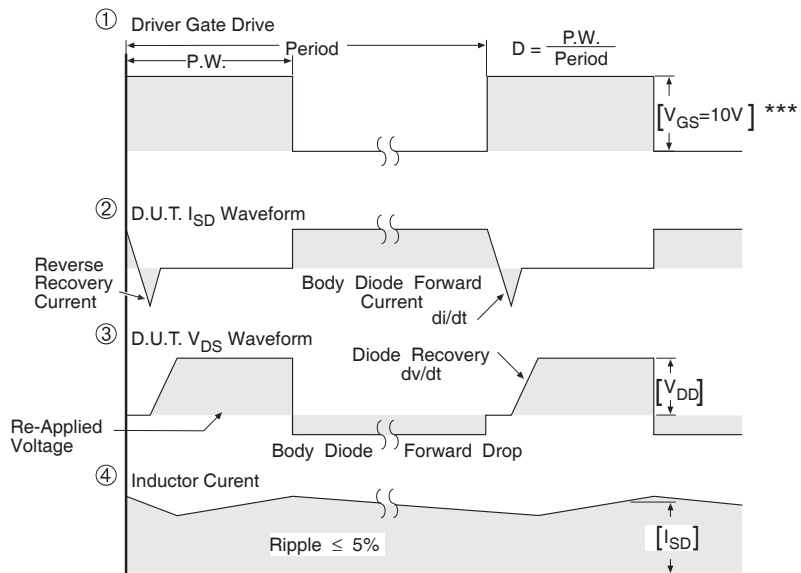


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

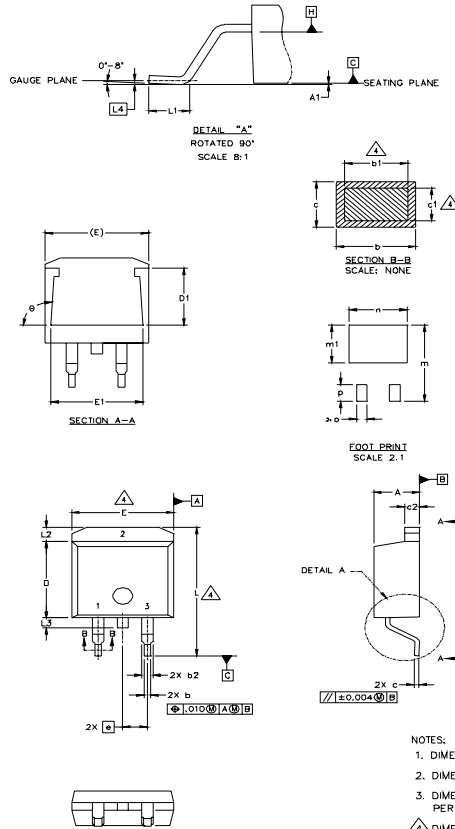
Fig 14. For N-channel HEXFET® power MOSFETs

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D²Pak Package Outline

Dimensions are shown in millimeters (inches)



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|--------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | | 0.127 | | .005 | |
| b | 0.51 | 0.99 | .020 | .039 | 4 |
| b1 | 0.51 | 0.89 | .020 | .035 | |
| b2 | 1.14 | 1.40 | .045 | .055 | 4 |
| c | 0.43 | 0.63 | .017 | .025 | |
| c1 | 0.38 | 0.74 | .015 | .029 | 3 |
| c2 | 1.14 | 1.40 | .045 | .055 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 | BSC | .100 | BSC | |
| L | 14.61 | 15.88 | .575 | .625 | |
| L1 | 1.78 | 2.79 | .070 | .110 | |
| L2 | | | 1.65 | .065 | |
| L3 | 1.27 | 1.78 | .050 | .070 | |
| L4 | 0.25 | BSC | .010 | BSC | |
| m | 17.78 | | .700 | | |
| m1 | 8.89 | | .350 | | |
| n | 11.43 | | .450 | | |
| o | 2.08 | | .082 | | |
| p | 3.81 | | .150 | | |
| θ | 90° | 93° | 90° | 93° | |

LEAD ASSIGNMENTS

| HEXFET | IGBTs, CoPACK | DIODES |
|------------|---------------|-------------|
| 1.- GATE | 1.- GATE | 1.- ANODE * |
| 2.- DRAIN | 2.- COLLECTOR | 2.- CATHODE |
| 3.- SOURCE | 3.- EMITTER | 3.- ANODE |

* PART DEPENDENT.

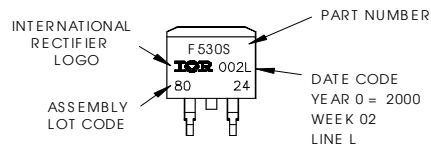
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

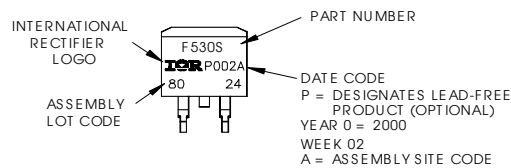
D²Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH
LOT CODE 8024
ASSEMBLED ON WW 02, 2000
IN THE ASSEMBLY LINE "L"

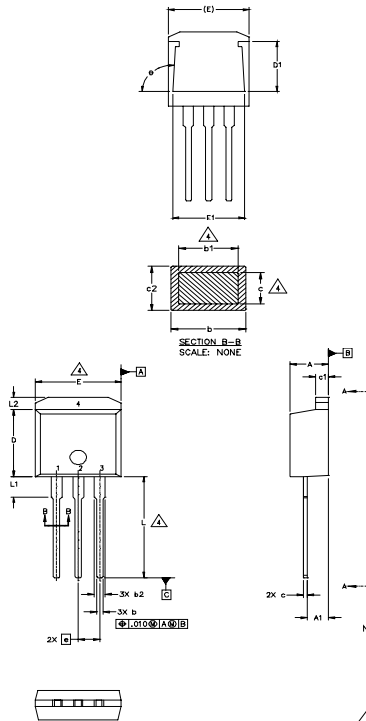
Note: "P" in assembly line
position indicates "Lead-Free"



OR



TO-262 Package Outline



| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|-------|--------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | 2.03 | 2.92 | .080 | .115 | |
| b | 0.51 | 0.99 | .020 | .039 | |
| b1 | 0.51 | 0.89 | .020 | .035 | 4 |
| b2 | 1.14 | 1.40 | .045 | .055 | |
| c | 0.38 | 0.63 | .015 | .025 | 4 |
| c1 | 1.14 | 1.40 | .045 | .055 | |
| c2 | 0.43 | .063 | .017 | .029 | |
| D | 8.51 | 9.65 | .335 | .380 | 3 |
| D1 | 5.33 | | .210 | | |
| E | 9.65 | 10.67 | .380 | .420 | 3 |
| E1 | 6.22 | | .245 | | |
| e | 2.54 | BSC | .100 | BSC | |
| L | 13.46 | 14.09 | .530 | .555 | |
| L1 | 3.56 | 3.71 | .140 | .146 | |
| L2 | | 1.65 | | .065 | |

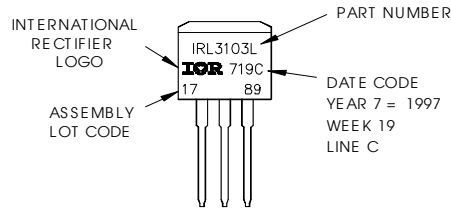
LEAD ASSIGNMENTS

| HEXFET | IGBT |
|------------|---------------|
| 1.- GATE | 1 - GATE |
| 2.- DRAIN | 2 - COLLECTOR |
| 3.- SOURCE | 3 - EMITTER |
| 4.- DRAIN | |

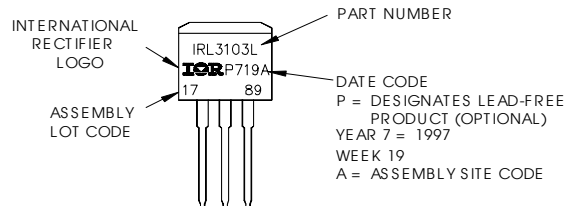
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 2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
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 4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
 5. CONTROLLING DIMENSION: INCH.

TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L
 LOT CODE 1789
 ASSEMBLED ON WW 19, 1997
 IN THE ASSEMBLY LINE "C"
 Note: "P" in assembly line
 position indicates "Lead-Free"



OR

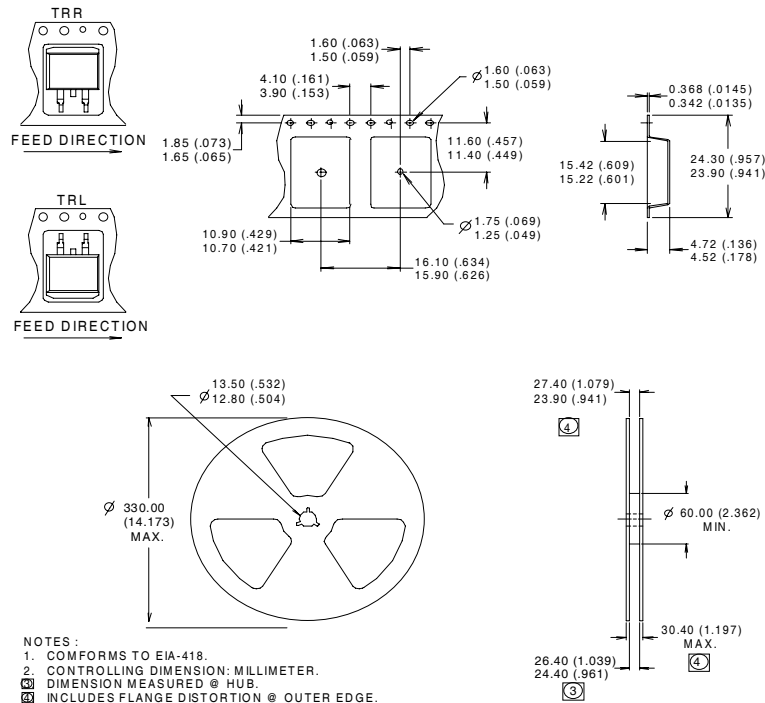


IRL1404S/LPbF

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D²Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.35\text{mH}$
 $R_G = 25\Omega$, $I_{AS} = 95\text{A}$. (See Figure 12)
- ③ $I_{SD} \leq 95\text{A}$, $di/dt \leq 160\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu\text{s}$; duty cycle $\leq 2\%$.
- ⑤ C_{OSS} eff. is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 80% V_{DSS} .
- ⑥ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.
- ⑦ This is applied to D²Pak, When mounted on 1" square PCB (FR-4 or G-10 Material) . For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.04/04

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Note: For the most current drawings please refer to the IR website at:
<http://www.irf.com/package/>

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