THE DATASHEET OF

LTC3861IUHE#TRPBF

Dual, Multiphase Step-Down Voltage Mode DC/DC Controller with Accurate Current Sharing

FEATURES

- **Operates with Power Blocks, DrMOS or External Gate Drivers and MOSFETs**
- **Constant-Frequency Voltage Mode Control with Accurate Current Sharing**
- **±0.75% 0.6V Voltage Reference**
- **Dual Differential Output Voltage Sense Amplifiers**
- **Multiphase Capability—Up to 12-Phase Operation**
- **Programmable Current Limit**
- **Safely Powers a Prebiased Load**
- **Programmable or PLL-Synchronizable Switching Frequency Up to 2.25MHz**
- **Lossless Current Sensing Using Inductor DCR or Precision Current Sensing with Sense Resistor**
- V_{CC} Range: 3V to 5.5V
- V_{IN} Range: 3V to 24V
- Power Good Output Voltage Monitor
- Output Voltage Tracking Capability
- Programmable Soft-Start
- Available in a 36-Pin 5mm × 6mm QFN Package

APPLICATIONS

- High Current Distributed Power Systems
- DSP, FPGA and ASIC Supplies
- Datacom and Telecom Systems
- Industrial Power Supplies

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DESCRIPTION

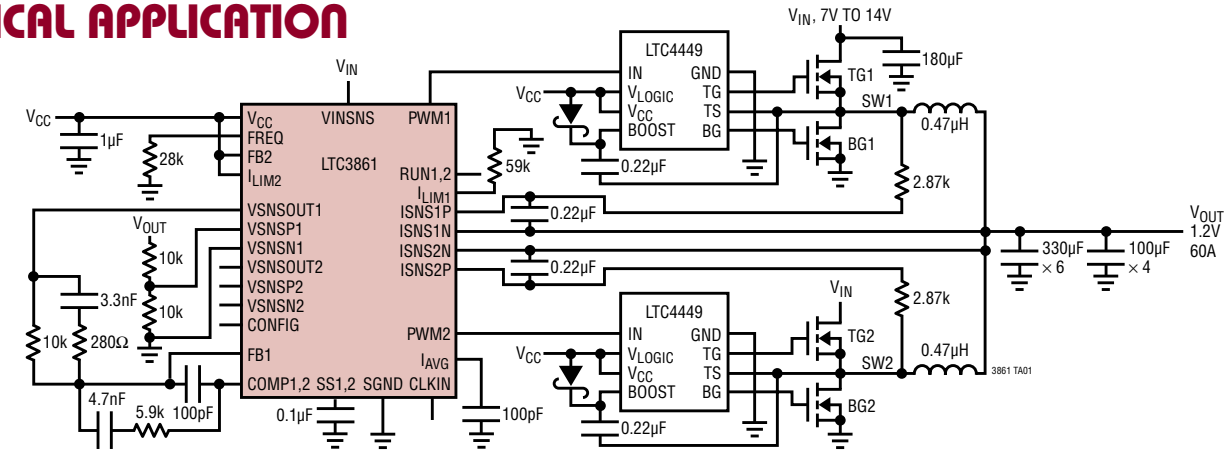
The LTC®3861 is a dual PolyPhase® synchronous step-down switching regulator controller for high current distributed power systems, digital signal processors, and other telecom and industrial DC/DC power supplies. It uses a constant-frequency voltage mode architecture combined with very low offset, high bandwidth error amplifiers and a remote output sense differential amplifier per channel for excellent transient response and output regulation.

The controller incorporates lossless inductor DCR current sensing to maintain current balance between phases and to provide overcurrent protection. The chip operates from a V_{CC} supply between 3V and 5.5V and is designed for step-down conversion from V_{IN} between 3V and 24V to output voltages between 0.6V and V_{CC} – 0.5V.

The TRACK/SS pins provide programmable soft-start or tracking functions. Inductor current reversal is disabled during soft-start to safely power prebiased loads. The constant operating frequency can be synchronized to an external clock or linearly programmed from 250kHz to 2.25MHz. Up to six LTC3861 controllers can operate in parallel for 1-, 2-, 3-, 4-, 6- or 12-phase operation.

The LTC3861 is available in a 36-pin 5mm × 6mm QFN package. LTC3861-1 is a 32-pin QFN version of the LTC3861, which has a single differential remote output voltage sense amplifier.

TYPICAL APPLICATION

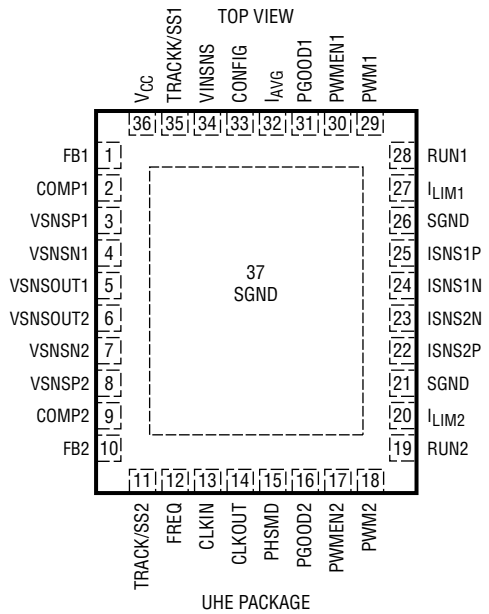


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Voltage ..... –0.3V to 6V
VINSNS Voltage ..... –0.3V to 30V
RUN1, RUN2 Voltage..... –0.3V to V_{CC} + 0.3V
ISNS1P, ISNS1N,
ISNS2P, ISNS2N..... –0.3V to (V_{CC} + 0.1V)
All Other Pins..... –0.3V to (V_{CC} + 0.3V)
Operating Junction Temperature Range
(Notes 2, 3)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UHE PACKAGE
36-LEAD (5mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 37) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3861EUHE#PBF	LTC3861EUHE#TRPBF	3861	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3861IUHE#PBF	LTC3861IUHE#TRPBF	3861	36-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 3). V_{CC} = 5V, $V_{RUN1,2}$ = 5V, V_{FREQ} = V_{CLKIN} = 0V, V_{FB} = 0.6V, f_{OSC} = 0.6MHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Range	V_{CC} = 5V	●	3		24	V
V_{CC}	V_{CC} Voltage Range		●	3		5.5	V
I_Q	Input Voltage Supply Current Normal Operation Shutdown Mode UVLO	 $V_{RUN1,2}$ = 5V $V_{RUN1,2}$ = 0V V_{CC} < V_{UVLO}			 30 8	 50	 mA µA mA
V_{RUN}	RUN Input Threshold	V_{RUN} Rising V_{RUN} Hysteresis		1.95	2.25 250	2.45	V mV
I_{RUN}	RUN Input Pull-Up Current	$V_{RUN1,2}$ = 2.4V			1.5		µA
V_{UVLO}	Undervoltage Lockout Threshold	V_{CC} Rising V_{CC} Hysteresis	●		 100	3.0	V mV
I_{SS}	Soft-Start Pin Output Current	V_{SS} = 0V			2.5		µA
$t_{SS(INTERNAL)}$	Internal Soft-Start Time				1.5		ms
V_{FB}	Regulated Feedback Voltage	–40°C to 85°C –40°C to 125°C	 ●	595.5 594	600 600	604.5 606	mV mV
$\Delta V_{FB}/\Delta V_{CC}$	Regulated Feedback Voltage Line Dependence	3.0V < V_{CC} < 5.5V			0.05	0.2	%/V
I_{LIMIT}	I_{LIM} Pin Output Current	V_{ILIM} = 0.8V		19	20	22	µA
Power Good							
$V_{FB(OV)}$	PGOOD/V_{FB} Overvoltage Threshold	V_{FB} Falling V_{FB} Rising		 650	645 660	 670	mV mV
$V_{FB(UV)}$	PGOOD/V_{FB} Undervoltage Threshold	V_{FB} Falling V_{FB} Rising		530	540 555	550	mV mV
$V_{PGOOD(ON)}$	PGOOD Pull-Down Resistance				15	60	Ω
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 5V				2	µA
t_{PGOOD}	PGOOD Delay	V_{PGOOD} High to Low			30		µs
Error Amplifier							
I_{FB}	FB Pin Input Current	V_{FB} = 600mV		–100		100	nA
I_{OUT}	COMP Pin Output Current	Sourcing Sinking			1 5		mA mA
$A_{V(OL)}$	Open-Loop Voltage Gain				75		dB
SR	Slew Rate				45		V/µs
f_{0dB}	COMP Unity-Gain Bandwidth	(Note 4)			40		MHz
Differential Amplifier							
V_{DA}	V_{SNSP} Accuracy	Measured in a Servo Loop with EA in Loop –40°C to 125°C	 ●	 592	 600	 608	 mV
I_{DIFF^+}	Input Bias Current	V_{SNSP} = 600mV		–100		100	nA
f_{0dB}	DA Unity-Gain Crossover Frequency	(Note 4)			40		MHz
$I_{OUT(SINK)}$	Maximum Sinking Current	DIFFOUT = 600mV			100		µA
$I_{OUT(SOURCE)}$	Maximum Sourcing Current	DIFFOUT = 600mV			500		µA
$V_{SNSOUT(MAX)}$	Maximum Output Voltage				3.3		V
Current Sense Amplifier							
$V_{ISENSE(MAX)}$	Maximum Differential Current Sense Voltage (V_{ISNSP}-V_{ISNSN})				50		mV
$A_{V(ISENSE)}$	Voltage Gain				18.5		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 3). V_{CC} = 5V, $V_{RUN1,2}$ = 5V, V_{FREQ} = V_{CLKIN} = 0V, V_{FB} = 0.6V, f_{OSC} = 0.6MHz, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CM(ISENSE)}$	Input Common Mode Range			–0.3		V_{CC} – 0.5	V
I_{ISENSE}	SENSE Pin Input Current	V_{CM} = 1.5V			100		nA
V_{OS}	Current Sense Input Referred Offset	–40°C to 125°C	●	–1.25		1.25	mV
Oscillator and Phase-Locked Loop							
f_{OSC}	Oscillator Frequency	V_{CLKIN} = 0V V_{FREQ} = 0V V_{FREQ} = 5V	 ● ●	 540 0.9	 600 1	 660 1.15	 kHz MHz
		V_{CLKIN} = 5V R_{FREQ} < 24.9k R_{FREQ} = 36.5k R_{FREQ} = 48.7k R_{FREQ} = 64.9k R_{FREQ} = 88.7k			 200 600 1 1.45 2.1		 kHz kHz MHz MHz MHz
		Maximum Frequency Minimum Frequency		3		 0.25	MHz MHz
I_{FREQ}	FREQ Pin Output Current	V_{FREQ} = 0.8V		18.5	20	21.5	µA
$t_{CLKIN(HI)}$	CLKIN Pulse Width High	V_{CLKIN} = 0V to 5V		100			ns
$t_{CLKIN(LO)}$	CLKIN Pulse Width Low	V_{CLKIN} = 0V to 5V		100			ns
R_{CLKIN}	CLKIN Pull-Up Resistance				13		kΩ
V_{CLKIN}	CLKIN Input Threshold	V_{CLKIN} Falling V_{CLKIN} Rising			1.2 2		V V
V_{FREQ}	FREQ Input Threshold	V_{CLKIN} = 0V V_{FREQ} Falling V_{FREQ} Rising			 1.5 2.5		 V V
$V_{OL(CLKOUT)}$	CLKOUT Low Output Voltage	I_{LOAD} = –500µA			0.2		V
$V_{OH(CLKOUT)}$	CLKOUT High Output Voltage	I_{LOAD} = 500µA			V_{CC} – 0.2		V
θ_2-θ_1	Channel 1-to-Channel 2 Phase Relationship	V_{PHSMD} = 0V V_{PHSMD} = Float V_{PHSMD} = V_{CC}			180 180 120		Deg Deg Deg
θ_{CLKOUT}-θ_1	CLKOUT-to-Channel 1 Phase Relationship	V_{PHSMD} = 0V V_{PHSMD} = Float V_{PHSMD} = V_{CC}			60 90 240		Deg Deg Deg
PWM/PWMEN Outputs							
PWM	PWM Output High Voltage	I_{LOAD} = 500µA	●	4.5			V
	PWM Output Low Voltage	I_{LOAD} = –500µA	●			0.5	V
	PWM Output Current in Hi-Z State					±5	µA
	PWM Maximum Duty Cycle				91.5		%
PWMEN	PWMEN Output High Voltage	I_{LOAD} = 1mA	●	4.5			V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

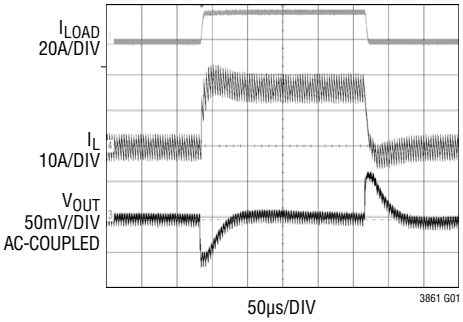
$$T_J = T_A + (P_D \bullet 34°C/W)$$

Note 3: The LTC3861 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3861E is guaranteed to meet performance specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3861I is guaranteed over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistors and other environmental factors.

Note 4: Guaranteed by design.

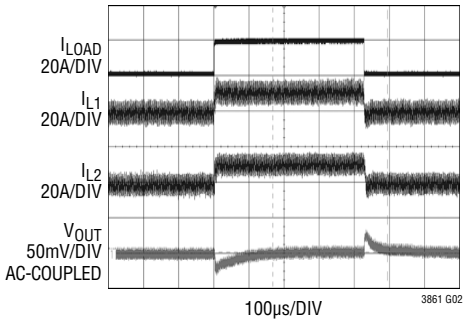
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step Transient Response (Single Phase Using LTC4449)



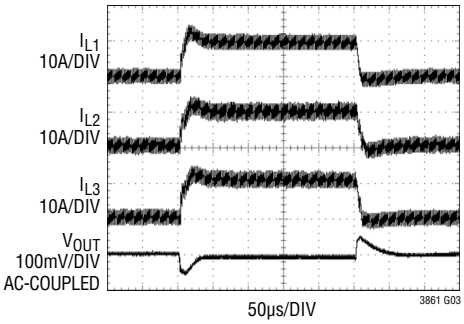
V_{IN} = 12V, V_{OUT} = 1.2V; I_{LOAD} STEP = 0A TO 18A, f_{SW} = 300kHz

Load Step Transient Response (2-Phase Using D12S1R845A Power Block)



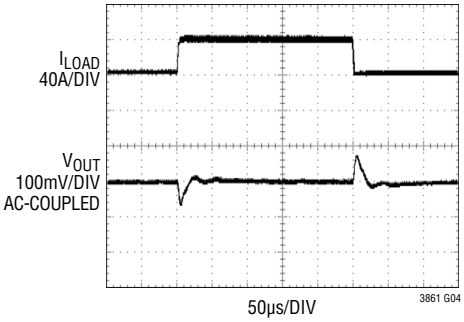
V_{IN} = 12V, V_{OUT} = 1.2V; I_{LOAD} STEP = 0A TO 20A, f_{SW} = 400kHz

Load Step Transient Response (3-Phase Using FDMF6707B DrMOS)



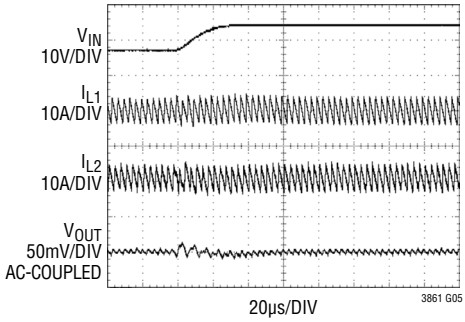
V_{IN} = 12V, V_{OUT} = 1V; I_{LOAD} STEP = 0A TO 30A, f_{SW} = 500kHz EXTERNAL CLOCK

Load Step Transient Response (4-Phase Using TDA21220 DrMOS)



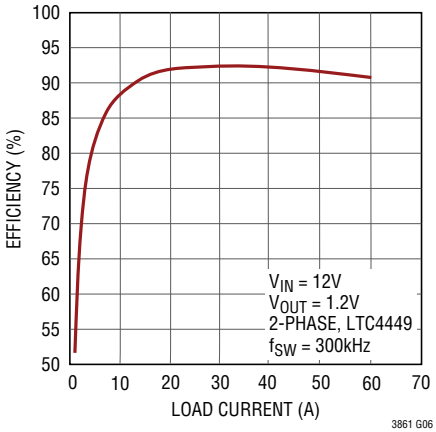
V_{IN} = 12V, V_{OUT} = 1V; I_{LOAD} STEP = 40A TO 80A, f_{SW} = 500kHz EXTERNAL CLOCK

Line Step Transient Response (2-Phase Using LTC4449)

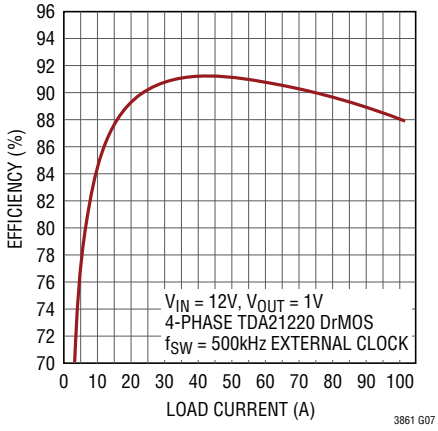


V_{IN} = 7V TO 14V IN 20µs, V_{OUT} = 1.2V; I_{LOAD} = 20A, f_{SW} = 300kHz

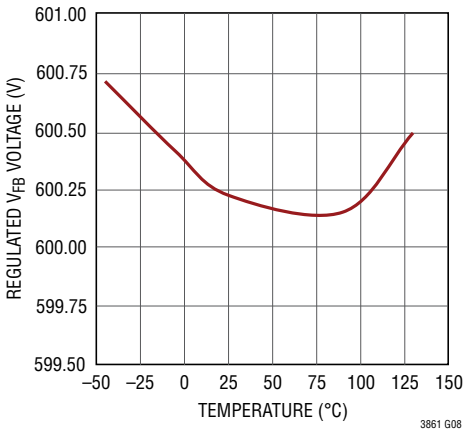
Efficiency vs Load Current



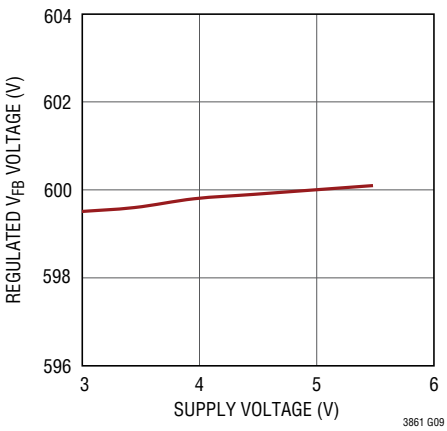
Efficiency vs Load Current



Feedback Voltage V_{FB} vs Temperature

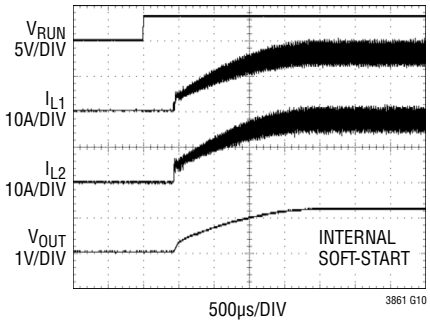


Regulated V_{FB} vs Supply Voltage



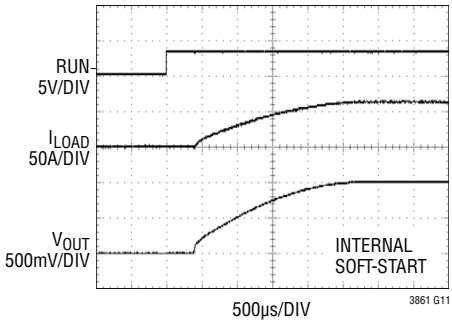
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up Response (2-Phase Using LTC4449)



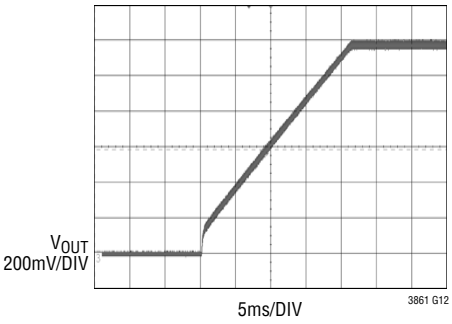
V_{IN} = 12V R_{LOAD} = 70mΩ
V_{OUT} = 1.2V f_{SW} = 300kHz

Start-Up Transient Response (4-Phase Using TDA21220 DrMOS)



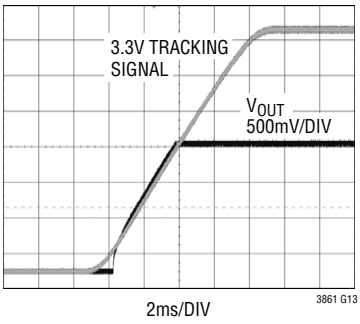
V_{IN} = 12V R_{LOAD} = 0.016Ω
V_{OUT} = 1V f_{SW} = 500kHz EXTERNAL CLOCK

Soft-Start Start-Up Response (2-Phase Using D12S1R845A Power Block)



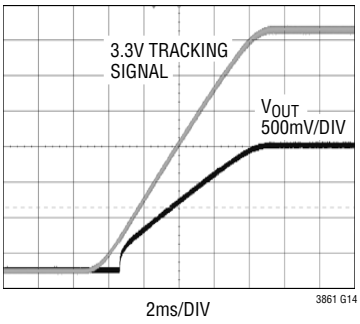
V_{IN} = 12V 0.1µF CAPACITOR ON TRACK/SS1
V_{OUT} = 1.2V f_{SW} = 400kHz

Coincident Tracking (Single Phase Using FDMF6707B DrMOS)



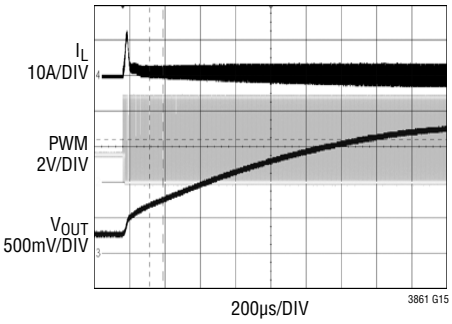
V_{IN} = 12V f_{SW} = 500kHz EXTERNAL CLOCK
V_{OUT} = 1.8V

Ratiometric Tracking (Single Phase Using FDMF6707B DrMOS)



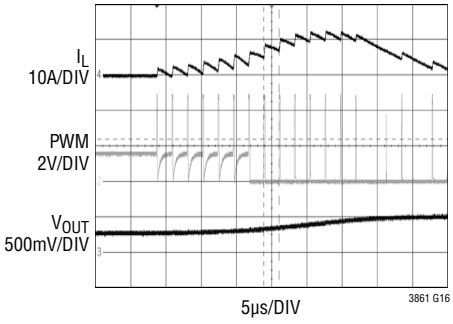
V_{IN} = 12V f_{SW} = 500kHz EXTERNAL CLOCK
V_{OUT} = 1.8V

Start-Up Response Into a 300mV Prebiased Output (Single Phase Using FDMF6707B DrMOS)



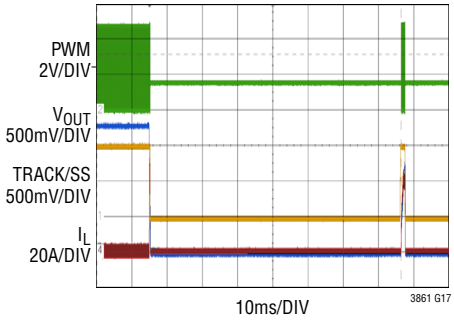
V_{IN} = 12V f_{SW} = 500kHz EXTERNAL CLOCK
V_{OUT} = 1.8V

Initial 7-Cycle Nonsynchronous Start-Up (Single Phase Using FDMF6707B DrMOS)



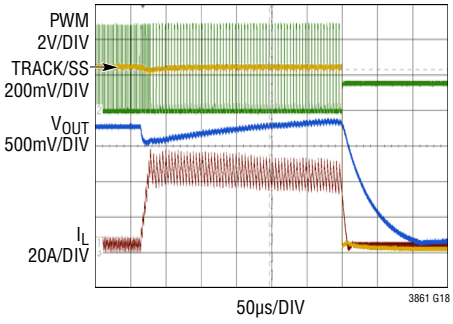
V_{IN} = 12V 300mV PREBIASED OUTPUT
V_{OUT} = 1.8V f_{SW} = 500kHz EXTERNAL CLOCK

Start-Up Into a Short (Single Phase Using FDMF6707B DrMOS)



V_{IN} = 12V f_{SW} = 500kHz EXTERNAL CLOCK
V_{OUT} = 1.8V

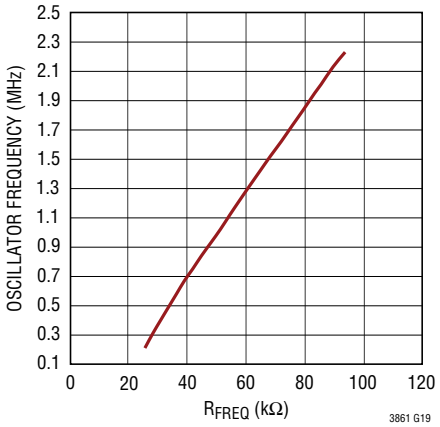
128-Cycle Overcurrent Counter (Single Phase Using FDMF6707B DrMOS)



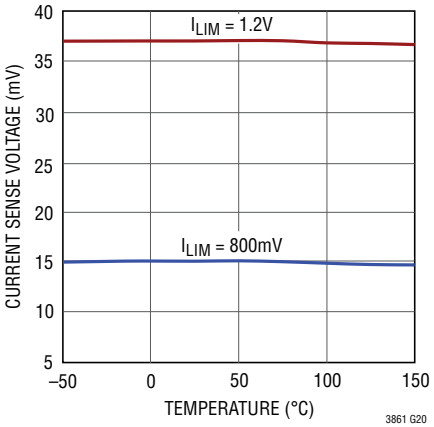
V_{IN} = 12V f_{SW} = 500kHz EXTERNAL CLOCK
V_{OUT} = 1.8V

TYPICAL PERFORMANCE CHARACTERISTICS

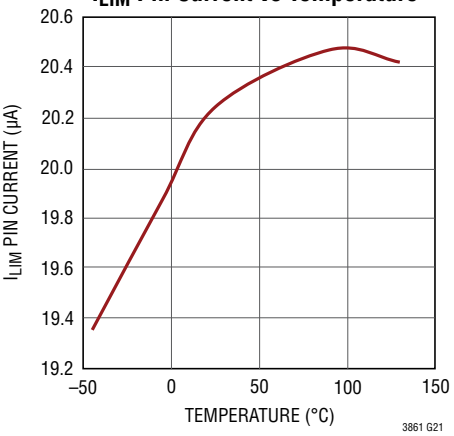
Oscillator Frequency vs R_{FREQ}



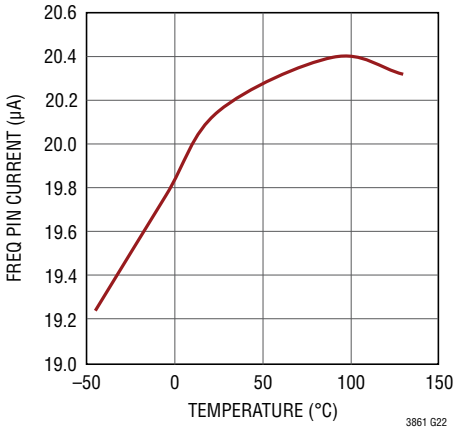
Overcurrent Threshold vs Temperature



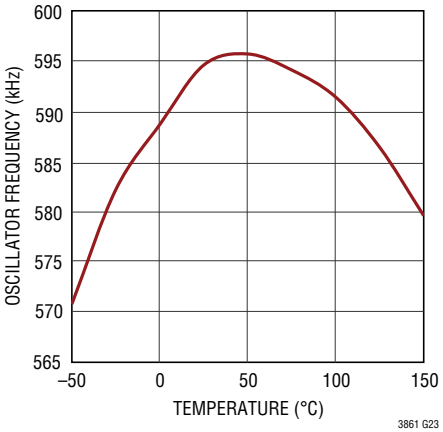
I_{LIM} Pin Current vs Temperature



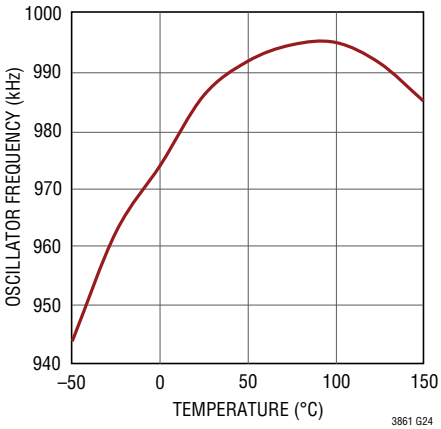
FREQ Pin Current vs Temperature



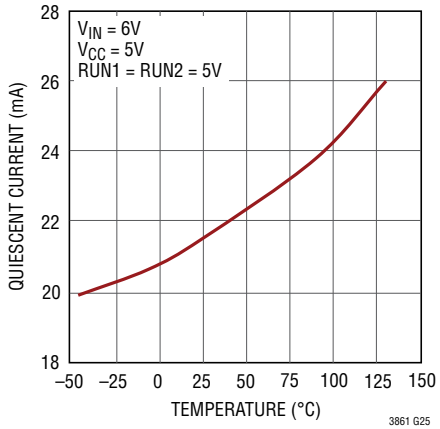
600kHz Preset Frequency vs Temperature



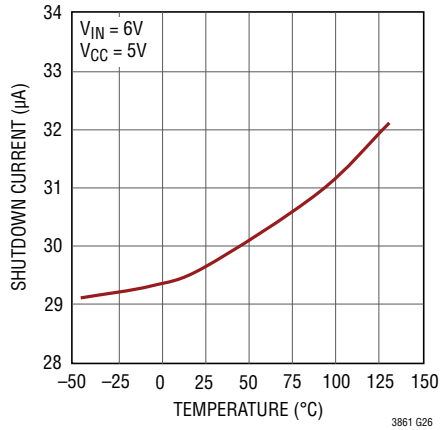
1MHz Preset Frequency vs Temperature



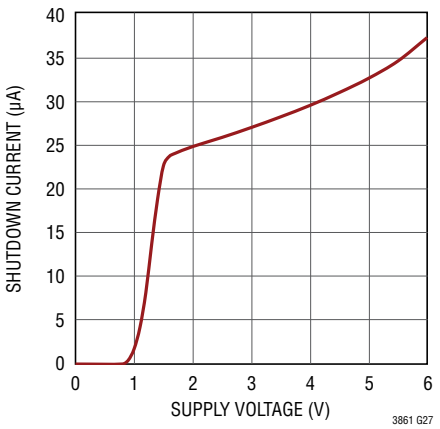
Quiescent Current vs Temperature



Shutdown Quiescent Current vs Temperature

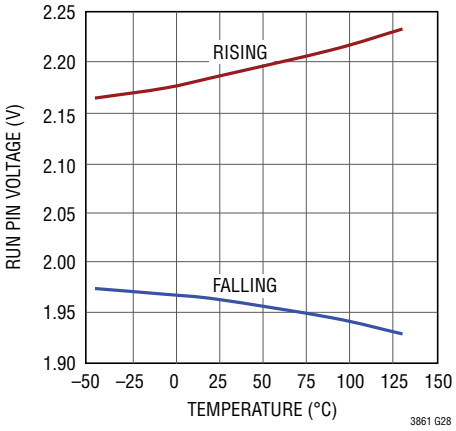


Shutdown Quiescent Current vs Supply Voltage

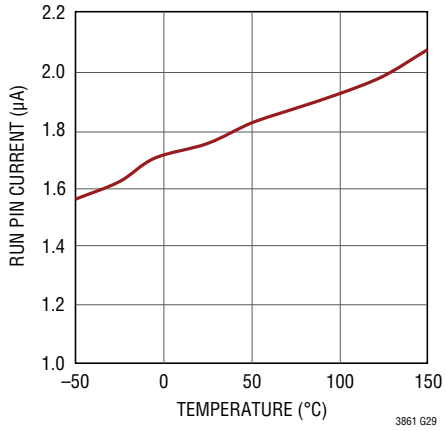


TYPICAL PERFORMANCE CHARACTERISTICS

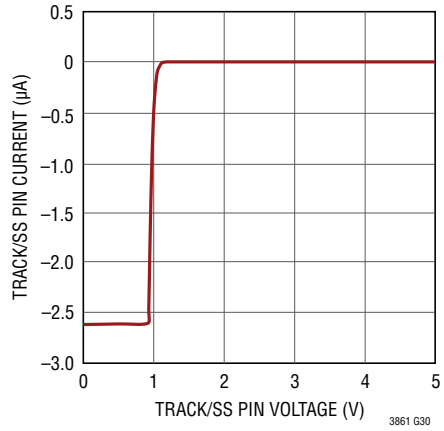
RUN Threshold vs Temperature



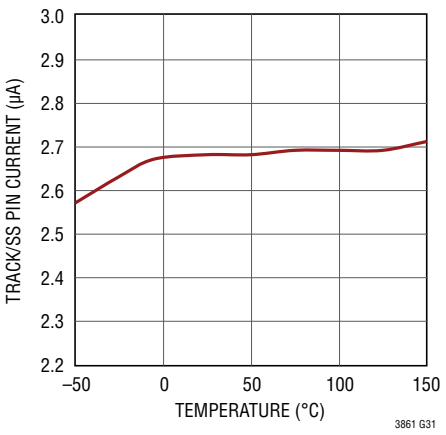
RUN Pull-Up Current vs Temperature



TRACK/SS Current vs TRACK/SS Voltage



TRACK/SS Pull-Up Current vs Temperature



PIN FUNCTIONS

FB1 (Pin 1), FB2 (Pin 10): Error Amplifier Inverting Input. Connect to VSNSOUT1, VNSOUT2 with a compensation network for remote V_{OUT} sensing. Connecting the FB to V_{CC} disables the differential and error amplifiers of the respective channel, and will three-state the amplifier outputs.

COMP1 (Pin 2), COMP2 (Pin 9): Error Amplifier Outputs. PWM duty cycle increases with this control voltage. The error amplifiers in the LTC3861 are true operational amplifiers with low output impedance. As a result, the outputs of two active error amplifiers cannot be directly connected together! For multiphase operation, connecting the FB pin on an error amplifier to V_{CC} will three-state the output of that amplifier. Multiphase operation can then be achieved by connecting all of the COMP pins together and using one channel as the master and all others as slaves. When the RUN pin is low, the respective COMP pin is actively pulled down to ground.

VSNSP1 (Pin 3), VSNSP2 (Pin 8): Differential Sense Amplifier Noninverting Input. Connect this pin to the midpoint of the feedback resistive divider between the positive and negative output capacitor terminals.

VSNSN1 (Pin 4), VSNSN2 (Pin 7): Differential Sense Amplifier Inverting Input. Connect this pin to sense ground at the output load.

PIN FUNCTIONS

VSNSOUT1 (Pin 5), VSNSOUT2 (Pin 6): Differential Amplifier Output. Connect to FB1, FB2 with a compensation network for remote V_{OUT} sensing.

FREQ (Pin 12): Frequency Set/Select Pin. This pin sources 20µA current. If CLKIN is high or floating, then a resistor between this pin and SGND sets the switching frequency. If CLKIN is low, the logic state of this pin selects an internal 600kHz or 1MHz preset frequency.

CLKIN (Pin 13): External Clock Synchronization Input. Applying an external clock between 250kHz to 2.25MHz will cause the switching frequency to synchronize to the clock. CLKIN is pulled high to V_{CC} by a 50k internal resistor. The rising edge of the CLKIN input waveform will align with the rising edge of PWM1 in closed-loop operation. If CLKIN is high or floating, a resistor from the FREQ pin to SGND sets the switching frequency. If CLKIN is low, the FREQ pin logic state selects an internal 600kHz or 1MHz preset frequency.

CLKOUT (Pin 14): Digital Output Used for Daisychaining Multiple LTC3861 ICs in Multiphase Systems. The PHSMD pin voltage controls the relationship between CH1 and CH2 as well as between CH1 and CLKOUT. When both RUN pins are driven low, the CLKOUT pin is actively pulled up to V_{CC}.

PHSMD (Pin 15): Phase Mode Pin. The PHSMD pin voltage programs the phase relationship between CH1 and CH2 rising PWM signals, as well as the phase relationship between CH1 PWM signal and CLKOUT. Floating this pin or connecting it to either V_{CC} or SGND changes the phase relationship between CH1, CH2 and CLKOUT.

SGND (Pins 21, 26, Exposed Pad Pin 37): Signal Ground. Pins 21, 26, and 37 are electrically connected internally. The exposed pad must be soldered to the PCB ground for rated thermal performance. All soft-start, small-signal and compensation components should return to SGND.

ISNS1N (Pin 24), ISNS2N (Pin 23): Current Sense Amplifier (–) Input. The (–) input to the current amplifier is normally connected to the respective V_{OUT} at the inductor.

ISNS1P (Pin 25), ISNS2P (Pin 22): Current Sense Amplifier (+) Input. The (+) input to the current sense amplifier is normally connected to the midpoint of the inductor's parallel RC sense circuit or to the node between the inductor and sense resistor if using a discrete sense resistor.

I_{LIM1} (Pin 27), I_{LIM2} (Pin 20): Current Comparator Sense Voltage Limit Selection Pin. Connect a resistor from this pin to SGND. This pin sources 20µA. The resultant voltage sets the threshold for overcurrent protection.

RUN1 (Pin 28), RUN2 (Pin 19): Run Control Inputs. A voltage above 2.25V on either pin turns on the IC. However, forcing either of these pins below 2V causes the IC to shut down that particular channel. There are 1.5µA pull-up currents for these pins.

PWM1 (Pin 29), PWM2 (Pin 18): (Top) Gate Signal Output. This signal goes to the PWM or top gate input of the external gate driver or integrated driver MOSFET. This is a three-state compatible output.

PWMEN1 (Pin 30), PWMEN2 (Pin 17): Enable Pin for Non-Three-State compatible drivers. This pin has an internal open-drain pull-up to V_{CC}. An external resistor to SGND is required. This pin is low when the corresponding PWM pin is high impedance.

PGOOD1 (Pin 31), PGOOD2 (Pin 16): Power Good Indicator Output for Each Channel. Open-drain logic out that is pulled to SGND when either channel output exceeds a ±10% regulation window, after the internal 30µs power bad mask timer expires.

I_{AVG} (Pin 32): Average Current Output Pin. A capacitor tied to ground from this pin stores a voltage proportional to the instantaneous average current of the master when multiple outputs are paralleled together in a master-slave configuration. Only the master phase contributes information to this average through an internal resistor when in current sharing mode. The I_{AVG} pin ignores channels configured for independent operation, hence the pin should be connected to SGND when the controller drives independent outputs. For single output converters using two or more ICs, tie all of the I_{AVG} pins together. The total capacitance on the I_{AVG} bus should range from 47pF to 220pF, inclusive, with the typical value being 100pF.

PIN FUNCTIONS

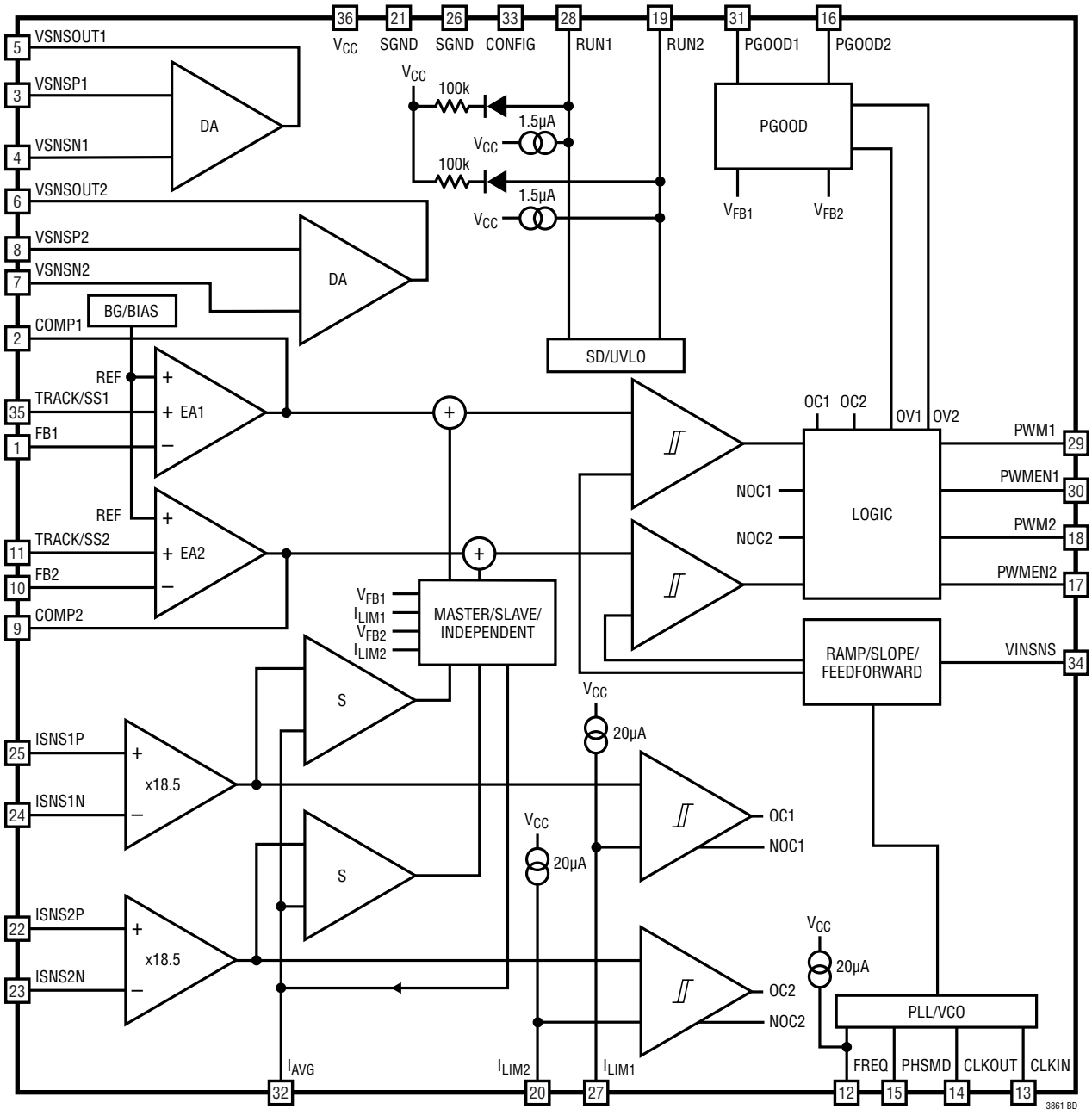
VINSNS (Pin 34): V_{IN} Sense Pin. Connects to the V_{IN} power supply to provide line feedforward compensation. A change in V_{IN} immediately modulates the input to the PWM comparator and changes the pulse width in an inversely proportional manner, thus bypassing the feedback loop and providing excellent transient line regulation. An external lowpass filter can be added to this pin to prevent noisy signals from affecting the loop gain.

CONFIG (Pin 33): Line Feedforward Configuration Pin. This pin allows the user to configure the multiplier to achieve accurate modulator gain over varying V_{IN} and switching frequencies. This pin can be connected to V_{CC} or SGND. An internal resistor will pull this pin to SGND when it is floated.

TRACK/SS1 (Pin 35), TRACK/SS2 (Pin 11): Combined Soft-Start and Tracking Inputs. For soft-start operation, connecting a capacitor from this pin to ground will control the voltage ramp at the output of the power supply. An internal 2.5µA current source will charge the capacitor and thereby control an extra input on the reference side of the error amplifier. For tracking operation, this input allows the start-up of a secondary output to track a primary output according to a ratio established by a resistor divider from the primary output to the secondary error amplifier track pin. For coincident tracking of both outputs at start-up, a resistor divider with values equal to those connected to the secondary VSNSP pin from the secondary output should be used to connect the secondary track input from the primary output. This pin is internally clamped to 1.2V, and is used to communicate over current events in a master-slave configuration.

V_{CC} (Pin 36): Chip Supply Voltage. Bypass this pin to GND with a capacitor (0.1µF to 1µF ceramic) in close proximity to the chip.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Architecture

The LTC3861 is a dual-channel/dual-phase, constant-frequency, voltage mode controller for DC/DC step-down applications. It is designed to be used in a synchronous switching architecture with external integrated-driver MOSFETs or power blocks, or external drivers and N-channel MOSFETs using single wire three-state PWM interfaces. The controller allows the use of sense resistors or lossless inductor DCR current sensing to maintain current balance between phases and to provide overcurrent protection. The operating frequency is selectable from 250kHz to 2.25MHz. To multiply the effective switching frequency, multiphase operation can be extended to 3, 4, 6, or 12 phases by paralleling up to six controllers. In single or 3-phase operation, the 2nd or 4th channel can be used as an independent output.

The output voltage is resistively divided externally to create a feedback voltage for the controller. Connect VSNSP of the unity-gain internal differential amplifier, DA, to the center tap of the feedback divider across the output load, and VSNSN to the load ground. The output of the differential amplifier VSNSOUT produces a signal equal to the differential voltage sensed across VSNSP and VSNSN. This scheme overcomes any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage.

In the main voltage mode control loop, the error amplifier output (COMP) directly controls the converter duty cycle in order to drive the FB pin to 0.6V in steady state. Dynamic changes in output load current can perturb the output voltage. When the output is below regulation, COMP rises, increasing the duty cycle. If the output rises above regulation, COMP will decrease, decreasing the duty cycle. As the output approaches regulation, COMP will settle to the steady-state value representing the step-down conversion ratio.

In normal operation, the PWM latch is set high at the beginning of the clock cycle (assuming COMP > 0.5V). When the (line feedforward compensated) PWM ramp exceeds the COMP voltage, the comparator trips and resets the PWM latch. If COMP is less than 0.5V at the beginning of the clock cycle, as in the case of an overvoltage at the outputs, the PWM pin remains low throughout the entire cycle. When the PWM pin goes high it has a minimum on-time of approximately 20ns and a minimum off-time of approximately one-twelfth the switching period.

Current Sharing

In multiphase operation, the LTC3861 also incorporates an auxiliary current sharing loop. Inductor current is sampled each cycle. The master's current sense amplifier output is averaged at the I_{AVG} pin. A small capacitor connected from I_{AVG} to GND (typically 100pF) stores a voltage corresponding to the instantaneous average current of the master. Each phase integrates the difference between its current and the master's. Within each phase the integrator output is proportionally summed with the system error amplifier voltage (COMP), adjusting that phase's duty cycle to equalize the currents. **When multiple ICs are daisy chained the I_{AVG} pins must be connected together. When the phases are operated independently, the I_{AVG} pin should be tied to ground.** Figure 1 shows a transient load step with current sharing in a 3-phase system.

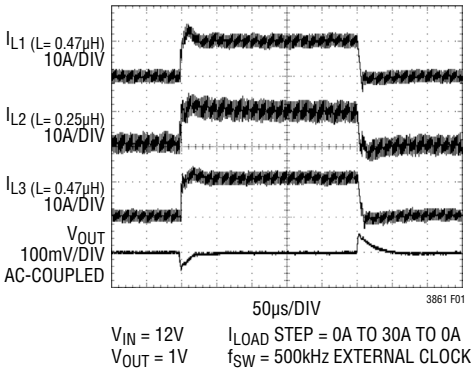


Figure 1. Mismatched Inductor Load Step Transient Response (3-Phase Using FDMF6707B DrMOS)

Overcurrent Protection

The current sense amplifier outputs also connect to overcurrent (OC) comparators that provide fault protection in the case of an output short. When an OC fault is detected for 128 consecutive clock cycles, the controller three-states the PWM output, resets the soft-start capacitor, and waits for 32768 clock cycles before attempting to start up again. The 128 consecutive clock cycle counter has a 7-cycle hysteresis window, after which it will reset. The LTC3861 also provides negative OC (NOC) protection by preventing turn-on of the bottom MOSFET during a negative OC fault condition. In this condition, the bottom MOSFET will be

OPERATION (Refer to Functional Diagram)

turned on for 20ns every eight cycles to allow the driver IC to recharge its topside gate drive capacitor. The negative OC threshold is equal to –3/4 the positive OC threshold. See the Applications Information section for guidelines on setting these thresholds.

Excellent Transient Response

The LTC3861 error amplifiers are true operational amplifiers, meaning that they have high bandwidth, high DC gain, low offset and low output impedance. Their bandwidth, when combined with high switching frequencies and low-value inductors, allows the compensation network to be optimized for very high control loop crossover frequencies and excellent transient response. The 600mV internal reference allows regulated output voltages as low as 600mV without external level-shifting amplifiers.

Line Feedforward Compensation

The LTC3861 achieves outstanding line transient response using a feedforward correction scheme which instantaneously adjusts the duty cycle to compensate for changes in input voltage, significantly reducing output overshoot and undershoot. It has the added advantage of making the DC loop gain independent of input voltage. Figure 2 shows how large transient steps at the input have little effect on the output voltage.

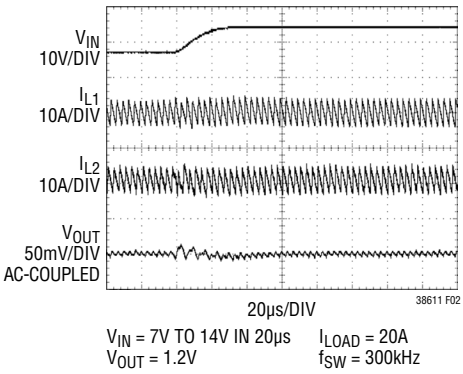


Figure 2

Remote Sense Differential Amplifier

The LTC3861 includes two low offset, unity gain, high bandwidth differential amplifiers for differential output sensing. Output voltage accuracy is significantly improved by removing board interconnection losses from the total error budget.

The noninverting input of the differential amplifier is connected to the midpoint of the feedback resistive divider between the positive and negative output capacitor terminals. The VSNSOUT is connected to the FB pin and the amplifier will attempt to regulate this voltage to 0.6V. The amplifier is configured for unity gain, meaning that the differential voltage between V_{SNSP} and V_{SNSN} is translated to V_{SNSOUT}, relative to SGND.

Shutdown Control Using the RUN Pins

The two channels of the LTC3861 can be independently enabled using the RUN1 and RUN2 pins. When both pins are driven low, all internal circuitry, including the internal reference and oscillator, are completely shut down. When the RUN pin is low, the respective COMP pin is actively pulled down to ground. In a multiphase operation when the COMP pins are tied together, the COMP pin is held low until all the RUN pins are enabled. This ensures a synchronized start-up of all the channels. A 1.5µA pull-up current is provided for each RUN pin internally. The RUN pins remain high impedance up to V_{CC}.

Undervoltage Lockout

To prevent operation of the power supply below safe input voltage levels, both channels are disabled when V_{CC} is below the undervoltage lockout (UVLO) threshold (2.9V falling, 3V rising). If a RUN pin is driven high, the LTC3861 will start up the reference to detect when V_{CC} rises above the UVLO threshold, and enable the appropriate channel.

Overvoltage Protection

If the output voltage rises to more than 10% above the set regulation value, which is reflected as a V_{FB} voltage of 0.66V or above, the LTC3861 will force the PWM output low to turn on the bottom MOSFET and discharge the output. Normal operation resumes once the output is back within the regulation window. However, if the reverse current flowing from V_{OUT} back through the bottom power MOSFET to PGND is greater than 3/4 the positive OC threshold, the NOC comparator trips and shuts off the bottom power MOSFET to protect it from being destroyed. This scenario can happen when the LTC3861 tries to start into a precharged load higher than the OV threshold. As

OPERATION (Refer to Functional Diagram)

a result, the bottom switch turns on until the amount of reverse current trips the NOC comparator threshold.

Nonsynchronous Start-Up and Prebiased Output Load

The LTC3861 will start up with seven cycles of nonsynchronous operation before switching over to a forced continuous mode of operation. The PWM output will be in a three-state condition until start-up. The controller will start the seven nonsynchronous cycles if it is not in an overcurrent or prebiased condition, and if the COMP pin voltage is higher than 500mV, or if the TRACK/SS pin voltage is higher than 580mV. During the seven nonsynchronous cycles the PWM latch is set high at the beginning of the clock cycle, if COMP > 0.5V, causing the PWM output to transition from three-state to V_{CC}. The latch is reset when the PWM ramp exceeds the COMP voltage, causing the PWM output to transition from V_{CC} to three-state followed immediately by a 20ns three-state to ground pulse. The 7-cycle nonsynchronous mode of operation is enabled at initial start-up and also during a restart from a fault condition. In multiphase operation, where all the TRACK/SS should be connected together, an overcurrent event on one channel will discharge the soft-start capacitor. After 32768 cycles, it will synchronize the restart of all channels in to the nonsynchronous mode of operation.

The LTC3861 can safely start-up into a prebiased output without discharging the output capacitors. A prebias is detected when the FB pin voltage is higher than the TRACK/SS or the internal soft-start voltage. A prebiased condition will force the COMP pin to be held low, and will three-state the PWM output. The prebiased condition is cleared when the TRACK/SS or the internal soft-start voltage is higher than the FB pin voltage or 580mV, whichever is lower. If the output prebias is higher than the OV threshold then the PWM output will be low, which will pull the output back in to the regulation window.

Internal Soft-Start

By default, the start-up of each channel's output voltage is normally controlled by an internal soft-start ramp. The internal soft-start ramp represents a noninverting input to the error amplifier. The FB pin is regulated to the lower of the error amplifier's three noninverting inputs (the internal soft-start ramp for that channel, the TRACK/SS pin or the internal 600mV reference). As the ramp voltage rises from 0V to 0.6V over approximately 2ms, the output voltage rises smoothly from its prebiased value to its final set value.

Soft-Start and Tracking Using TRACK/SS Pin

The user can connect an external capacitor greater than 10nF to the TRACK/SS pin for the relevant channel to increase the soft-start ramp time beyond the internally set default. The TRACK/SS pin represents a noninverting input to the error amplifier and behaves identically to the internal ramp described in the previous section. An internal 2.5µA current source charges the capacitor, creating a voltage ramp on the TRACK/SS pin. The TRACK/SS pin is internally clamped to 1.2V. As the TRACK/SS pin voltage rises from 0V to 0.6V, the output voltage rises smoothly from 0V to its final value in:

$$\frac{C_{SS}\mu F \bullet 0.6V}{2.5\mu A} \text{ seconds}$$

Alternatively, the TRACK/SS pin can be used to force the start-up of V_{OUT} to track the voltage of another supply. Typically this requires connecting the TRACK/SS pin to an external divider from the other supply to ground (see the Applications Information section). It is only possible to track another supply that is slower than the internal soft-start ramp. The TRACK/SS pin also has an internal open-drain NMOS pull-down transistor that turns on to reset the TRACK/SS voltage when the channel is shut down (RUN = 0V or V_{CC} < UVLO threshold) or during an OC fault condition.

In multiphase operation, one master error amplifier is used to control all of the PWM comparators. The FB pins for the unused error amplifiers are connected to V_{CC} in order to three-state these amplifier outputs and the COMP pins are connected together. When the FB pin is tied to V_{CC}, the internal 2.5µA current source on the TRACK/SS pin is disabled for that channel. The TRACK/SS pins should also be connected together so that the slave phases can detect when soft-start is complete and to synchronize the nonsynchronous mode of operation.

OPERATION (Refer to Functional Diagram)

Frequency Selection and the Phase-Locked Loop (PLL)

The selection of the switching frequency is a trade-off between efficiency, transient response and component size. High frequency operation reduces the size of the inductor and output capacitor as well as increasing the maximum practical control loop bandwidth. However, efficiency is generally lower due to increased transition and switching losses.

The LTC3861's switching frequency can be set in three ways: using an external resistor to linearly program the frequency, synchronizing to an external clock, or simply selecting one of two fixed frequencies (600kHz and 1MHz). Table 1 highlights these modes.

Table 1. Frequency Selection

CLKIN PIN	FREQ PIN	FREQUENCY
Clocked	R_{FREQ} to GND	250kHz to 2.25MHz
High or Float	R_{FREQ} to GND	250kHz to 2.25MHz
Low	Low	600kHz
Low	High	1MHz

No external PLL filter is required to synchronize the LTC3861 to an external clock. Applying an external clock signal to the CLKIN pin will automatically enable the PLL with internal filter.

Constant-frequency operation brings with it a number of benefits: inductor and capacitor values can be chosen for a precise operating frequency and the feedback loop can be similarly tightly specified. Noise generated by the circuit will always be at known frequencies.

Using the CLKOUT and PHSMD Pins in Multiphase Applications

The LTC3861 features CLKOUT and PHSMD pins that allow multiple LTC3861 ICs to be daisy chained together in multiphase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional ICs in a 3-, 4-, 6- or 12-phase power supply solution feeding a single high current output, or even several outputs from the same input supply.

The PHSMD pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT, as summarized in Table 2. The phases are calculated relative to zero degrees, defined as the rising edge of PWM1. Refer to Applications Information for more details on how to create multiphase applications.

Table 2. Phase Selection

PHSMD PIN	CH-1 to CH-2 PHASE	CH-1 to CLKOUT PHASE
Float	180°	90°
Low	180°	60°
High	120°	240°

Using the LTC3861 Error Amplifiers in Multiphase Applications

Due to the low output impedance of the error amplifiers, multiphase applications using the LTC3861 use one error amplifier as the master with all of the slaves' error amplifiers disabled. The channel 1 error amplifier (phase = 0°) may be used as the master with phases 2 through n (up to 12) serving as slaves. To disable the slave error amplifiers connect the FB pins of the slaves to V_{CC}. This three-states the output stages of the amplifiers. All COMP pins should then be connected together to create PWM outputs for all phases. As noted in the section on soft-start, all TRACK/SS pins should also be shorted together. Refer to the Multiphase Operation section in Applications Information for schematics of various multiphase configurations.

Theory and Benefits of Multiphase Operation

Multiphase operation provides several benefits over traditional single phase power supplies:

- Greater output current capability
- Improved transient response
- Reduction in component size
- Increased real world operating efficiency

Because multiphase operation parallels power stages, the amount of output current available is n times what it would be with a single comparable output stage, where n is equal to the number of phases.

The main advantages of PolyPhase operation are ripple current cancellation in the input and output capacitors, a faster load step response due to a smaller clock delay and

OPERATION (Refer to Functional Diagram)

reduced thermal stress on the inductors and MOSFETs due to current sharing between phases. These advantages allow for the use of a smaller size or a smaller number of components.

Power Good Indicator Pins (PGOOD1, PGOOD2)

Each PGOOD pin is connected to the open drain of an internal pull-down device which pulls the PGOOD pin low when the corresponding FB pin voltage is outside the PGOOD regulation window (±7.5% entering regulation, ±10% leaving regulation). The PGOOD pins are also pulled low when the corresponding RUN pin is low, or during UVLO.

When the FB pin voltage is within the ±10% regulation window, the internal PGOOD MOSFET is turned off and the pin is normally pulled up by an external resistor. When the FB pin is exiting a fault condition (such as during normal output voltage start-up, prior to regulation), the PGOOD pin will remain low for an additional 30µs. This allows the output voltage to reach steady-state regulation and prevents the enabling of a heavy load from retriggering a UVLO condition.

In multiphase applications, one FB pin and error amplifier are used to control all of the phases. Since the FB pins for the unused error amplifiers are connected to V_{CC} (in order to three-state these amplifiers), the PGOOD outputs for these amplifiers will be asserted. In order to prevent falsely reporting a fault condition, the PGOOD outputs for the unused error amplifiers should be left open. Only the PGOOD output for the master control error amplifier should be connected to the fault monitor.

PWM and PWMEN Pins

The PWM pins are three-state compatible outputs, designed to drive MOSFET drivers, DrMOSs, power blocks, etc., which do not represent a heavy capacitive load. An external resistor divider may be used to set the voltage to mid-rail while in the high impedance state.

The PWMEN outputs have an open-drain pull-up to V_{CC} and require an appropriate external pull-down resistor. This pin is intended to drive the enable pins of the MOSFET drivers that do not have three-state compatible PWM inputs. PWMEN is low only when PWM is high impedance, and high at any other PWM state.

Line Feedforward Gain

In a typical LTC3861 circuit, the feedback loop consists of the line feedforward circuit, the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the PWM generator, the external output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearly with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain from the error amplifier output to the inductor input regardless of input voltage. From a feedback loop point of view, the combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the inductor input and has a gain roughly equal to 12V/V.

The LTC3861 has a wide V_{IN} and switching frequency range. The CONFIG pin is used to select the optimum range of operation for the internal multiplier, in order to maintain a constant line feedforward gain across a wide V_{IN} and switching frequency range. The CONFIG is a three-state pin and can be connected to SGND, $V_{CC,}$ or floated. Floating the pin externally is a valid selection as there are internal steering resistors. The selection range based on V_{IN} and switching frequency is summarized in Table 3.

Table 3. Line Feedforward Range Selection

CONFIG PIN	V_{IN}
GND (or) FLOAT	< 14V
V_{CC}	> 14V

APPLICATIONS INFORMATION

Output Voltage Programming and Differential Output Sensing

The LTC3861 integrates differential output sensing with output voltage programming, allowing for a simple and seamless design. As shown in Figure 3, the output voltage is programmed by an external resistor divider from the regulated output point to its ground reference. The resistive divider is tapped by the VSNSP pin, and the ground reference is sensed by VSNSN. An optional feedforward capacitor, C_{FF}, can be used to improve the transient performance. The resulting output voltage is given according to the following equation:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_{FB2}}{R_{FB1}}\right)$$

More precisely, the V_{OUT} value programmed in the previous equation is with respect to the output's ground reference,

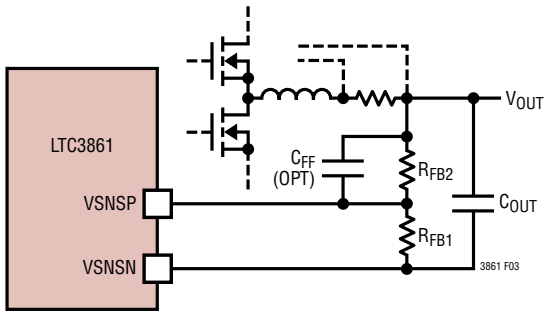


Figure 3. Setting Output Voltage

and thus, is a differential quantity. The minimum differential output voltage is limited to the internal reference, 0.6V, and the maximum differential output voltage is V_{CC} – 0.5V.

The VSNSP pin is high impedance with no input bias current. The VSNSN pin has about 7.5µA of current flowing out of the pin. Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 4 illustrates the potential variations in the power and ground lines due to parasitic elements. These variations are exacerbated in multiapplication systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage.

The LTC3861's differential output sensing scheme is distinct from conventional schemes. In conventional schemes, the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistive divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

The LTC3861 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range from 0.6V to V_{CC} – 0.5V. The difference amplifier of the LTC3861 has a gain bandwidth of 40MHz,

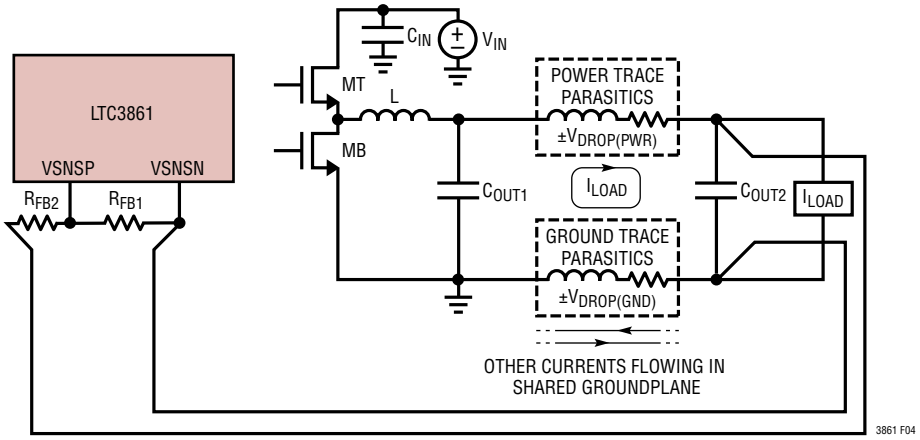


Figure 4: Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane

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high enough not to affect main loop compensation and transient behavior. To avoid noise coupling into VSNSP, the resistor divider should be placed near the VSNSP and VSNSN pins and physically close to the LTC3861. The remote output and ground traces should be routed parallel to each other as a differential pair to the remote output. These traces should be terminated as close as physically possible to the remote output point that is to be accurately regulated through remote differential sensing. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, they should be shielded by a low impedance ground plane to maintain signal integrity.

Programming the Operating Frequency

The LTC3861 can be hard wired to one of two fixed frequencies, linearly programmed to any frequency between 250kHz and 2.25MHz or synchronized to an external clock.

Table 1 in the Operation section shows how to connect the CLKIN and FREQ pins to choose the mode of frequency programming. The frequency of operation is given by the following equation:

$$\text{Frequency} = (R_{FREQ} - 17k\Omega) \bullet 29Hz/\Omega$$

Figure 5 shows operating frequency vs R_{FREQ}.

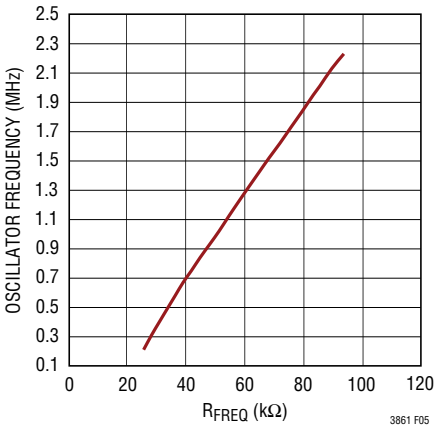

Figure 5. Oscillator Frequency vs R_{FREQ}

Frequency Synchronization

The LTC3861 incorporates an internal phase-locked loop (PLL) which enables synchronization of the internal oscillator (rising edge of PWM1) to an external clock from 250kHz to 2.25MHz.

Since the entire PLL is internal to the LTC3861, simply applying a CMOS level clock signal to the CLKIN pin will enable frequency synchronization. A resistor from FREQ to GND is still required to set the free running frequency close to the sync input frequency.

For cases where the LTC3861s are daisy chained, make sure the clock is applied a minimum of 1ms after the RUN pin is enabled.

Choosing the Inductor and Setting the Current Limit

The inductor value is related to the switching frequency, which is chosen based on the trade-offs discussed in the Operation section. The inductor can be sized using the following equation:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Choosing a larger value of ΔI_L leads to smaller L, but results in greater core loss (and higher output voltage ripple for a given output capacitance and/or ESR). A reasonable starting point for setting the ripple current is 30% of the maximum output current, or:

$$\Delta I_L = 0.3 \bullet I_{OUT}$$

The inductor saturation current rating needs to be higher than the peak inductor current during transient conditions. If I_{OUT} is the maximum rated load current, then the maximum transient current, I_{MAX}, would normally be chosen to be some factor (e.g., 60%) greater than I_{OUT}:

$$I_{MAX} = 1.6 \bullet I_{OUT}$$

The minimum saturation current rating should be set to allow margin due to manufacturing and temperature variation in the sense resistor or inductor DCR. A reasonable value would be:

$$I_{SAT} = 2.2 \bullet I_{OUT}$$

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The programmed current limit must be low enough to ensure that the inductor never saturates and high enough to allow increased current during transient conditions, to account for inductor ripple current and to allow margin for DCR variation.

For example:

$$I_{LIMIT} = 1.6 \bullet I_{OUT} + \frac{\Delta IL}{2}$$

where

$$\Delta IL = \frac{V_{OUT}}{L \bullet f_{SW} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

provided that $I_{LIMIT} < I_{SAT}$.

If the sensed inductor current exceeds current limit for 128 consecutive clock cycles, the IC will three-state the PWM outputs, reset the soft-start timer and wait 32768 switching cycles before attempting to return the output to regulation.

The current limit is programmed using a resistor from the I_{LIM} pin to SGND. The I_{LIM} pin sources 20µA to generate a voltage corresponding to the current limit. The current sense circuit has a voltage gain of 18.5 and a zero current level of 500mV. Therefore, the current limit resistor should be set using the following equation:

$$R_{ILIM} = \frac{18.5 \bullet I_{LIMIT_PHASE} \bullet R_{SENSE} + 0.5V}{20\mu A}$$

In multiphase applications only one current limit resistor should be used per LTC3861. The I_{LIM2} pin should be tied to V_{CC}. Internal logic will then cause channel 2 to use the same current limit levels as channel 1. If an LTC3861 has a slave and an independent, then both I_{LIM} pins must be independently set to the right voltage.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core losses found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Also, core losses decrease as inductance increases. Unfortunately, increased inductance requires more turns of wire, larger inductance and larger copper losses.

Ferrite designs have very low core loss and are preferred at high switching frequencies. However, these core materials exhibit "hard" saturation, causing an abrupt reduction in the inductance when the peak current capability is exceeded. **Do not allow the core to saturate!**

C_{IN} Selection

The input bypass capacitor in an LTC3861 circuit is common to both channels. The input bypass capacitor needs to meet these conditions: its ESR must be low enough to keep the supply drop low as the top MOSFETs turn on, its RMS current capability must be adequate to withstand the ripple current at the input, and the capacitance must be large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor (particularly a non-ceramic type) that meets the first two parameters will have far more capacitance than is required to keep capacitance-based droop under control.

The input capacitor's voltage rating should be at least 1.4 times the maximum input voltage. Power loss due to ESR occurs not only as I^2R dissipation in the capacitor itself, but also in overall battery efficiency. For mobile applications, the input capacitors should store adequate charge to keep the peak battery current within the manufacturer's specifications.

The input capacitor RMS current requirement is simplified by the multiphase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used to determine the maximum RMS current requirement. Increasing the output current

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drawn from the other out-of-phase controller will actually decrease the input RMS ripple current from this maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top N-channel MOSFET is approximately a square wave of duty cycle V_{OUT}/V_{IN}. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN}-V_{OUT}\right)}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. The total RMS current is lower when both controllers are operating due to the interleaving of current pulses through the input capacitors. This is why the input capacitance requirement calculated above for the worst-case controller is adequate for the dual controller design.

Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

Ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited surface mount applicability; and electrolytics' higher ESR and dryout possibility require several to be used. Sanyo OS-CON SVP, SVPD series; Sanyo POSCAP TQC series or aluminum electrolytic capacitors from Panasonic WA series or Cornell Dubilier SPV series, in parallel with a couple of high performance ceramic capacitors, can be used as an effective means of achieving low ESR and high bulk capacitance.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple ΔV_{OUT} is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}} \right)$$

where ΔI_L is the inductor ripple current.

ΔI_L may be calculated using the equation:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Since ΔI_L increases with input voltage, the output ripple voltage is highest at maximum input voltage. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Manufacturers such as Sanyo, Panasonic and Cornell Dubilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or transient current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices include the Sanyo POSCAP TPD, TPE, TPF series, the Kemet T520, T530 and A700 series, NEC/Tokin NeoCapacitors and Panasonic SP series. Other capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

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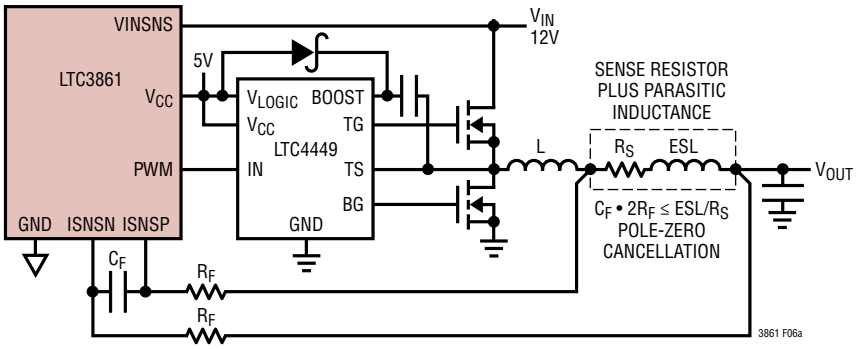
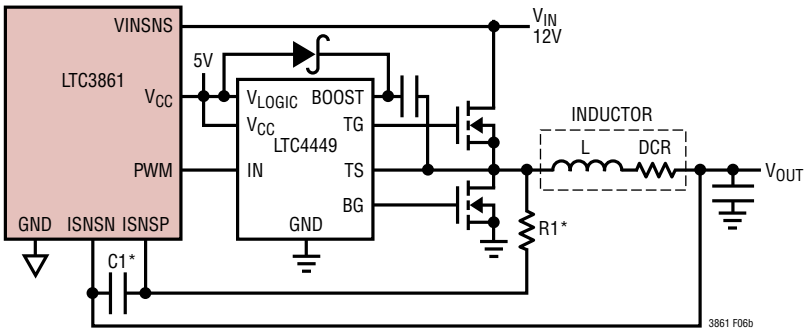
Current Sensing

To maximize efficiency the LTC3861 is designed to sense current through the inductor's DCR, as shown in Figure 6. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which for most inductors applicable to this application, is between 0.3mΩ and 1mΩ. If the filter RC time constant is chosen to be exactly equal to the L/DCR time constant of the inductor, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR. Check the manufacturer's data sheet for specifications regarding the inductor DCR in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a good RLC meter.



FILTER COMPONENTS PLACED NEAR SENSE PINS

(6a) Using a Resistor to Sense Current



$R1 \bullet C1 = \frac{L}{DCR}$ *PLACE R1 NEAR INDUCTOR
PLACE C1 NEAR ISNSP, ISNSN PINS

(6b) Using the Inductor to Sense Current

Figure 6. Two Different Methods of Sensing Current

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Since the temperature coefficient of the inductor's DCR is 3900ppm/°C, first order compensation of the filter time constant is possible by using filter resistors with an equal but opposite (negative) TC, assuming a low TC capacitor is used. That is, as the inductor's DCR rises with increasing temperature, the L/DCR time constant drops. Since we want the filter RC time constant to match the L/DCR time constant, we also want the filter RC time constant to drop with increasing temperature. Typically, the inductance will also have a small negative TC.

The ISNSP and ISNSN pins are the inputs to the current comparators. The common mode range of the current comparators is –0.3V to V_{CC} – 0.5V. Continuous linear operation is provided throughout this range, allowing output voltages between 0.6V (the reference input to the error amplifiers) and V_{CC} – 0.5V. The maximum output voltage is lower than V_{CC} to account for output ripple and output overshoot. The maximum differential current sense input ($V_{ISNSP} – V_{ISNSN}$) is 50mV.

The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Filter components mutual to the sense lines should be placed close to the LTC3861, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 7). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If low value (<5mΩ) sense resistors are used, verify that the signal across C_F resembles the current through the inductor, and reduce R_F to eliminate any large step associated with the turn-on of the primary switch. If DCR sensing is used (Figure 6b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

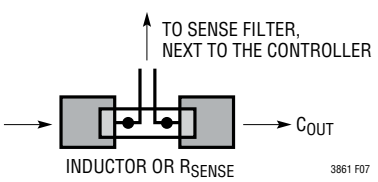

Figure 7. Sense Lines Placement with Inductor or Sense Resistor

Multiphase Operation

When the LTC3861 is used in a single output, multiphase application, the slave error amplifiers must be disabled by connecting their FB pins to V_{CC}. All current limits should be set to the same value using only one resistor to SGND per IC. I_{LIM2} should then be connected to V_{CC}. These connections are shown in Table 4. In a multiphase application all COMP, RUN and TRACK/SS pins must be connected together. For single output converters using two or more ICs, tie all of the I_{AVG} pins together. The total capacitance on the I_{AVG} bus should range from 47pF to 220pF, inclusive, with the typical value being 100pF.

Table 4. Multiphase Configurations

CH1	CH2	FB1	FB2	I_{LIM1}	I_{LIM2}
Master	Slave	On	Off (FB = V_{CC})	Resistor to GND	V_{CC}
Slave	Slave	Off (FB = V_{CC})	Off (FB = V_{CC})	Resistor to GND	V_{CC}
Slave	Additional Output	Off (FB = V_{CC})	On	Resistor to GND	Resistor to GND

For output loads that demand high current, multiple LTC3861s can be daisy chained to run out of phase to provide more output current without increasing input and output voltage ripple. The CLKIN pin allows the LTC3861 to synchronize to the CLKOUT signal of another LTC3861. The CLKOUT signal can be connected to the CLKIN pin of the following LTC3861 stage to line up both the frequency and the phase of the entire system. Tying the PHSMD pin to V_{CC}, SGND or floating it generates a phase difference (between CLKIN and CLKOUT) of 240°, 60° or 90° respectively, and a phase difference (between CH1 and CH2) of 120°, 180° or 180°. Figure 8 shows the PHSMD connections necessary for 3-, 4-, 6- or 12-phase operation. A total of twelve phases can be daisy chained to run simultaneously out of phase with respect to each other.

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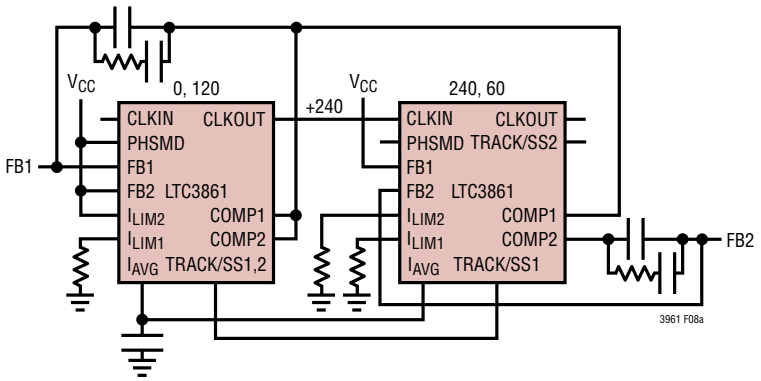

Figure 8a. 3-Phase Operation

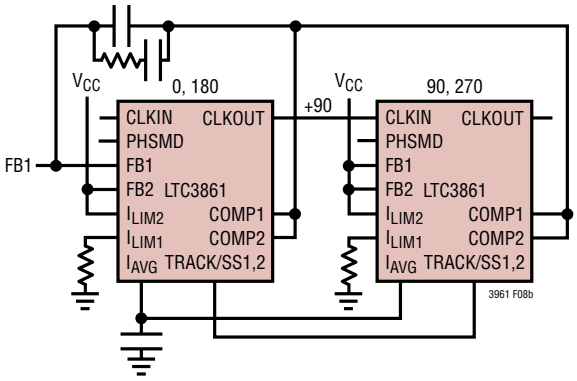

Figure 8b. 4-Phase Operation

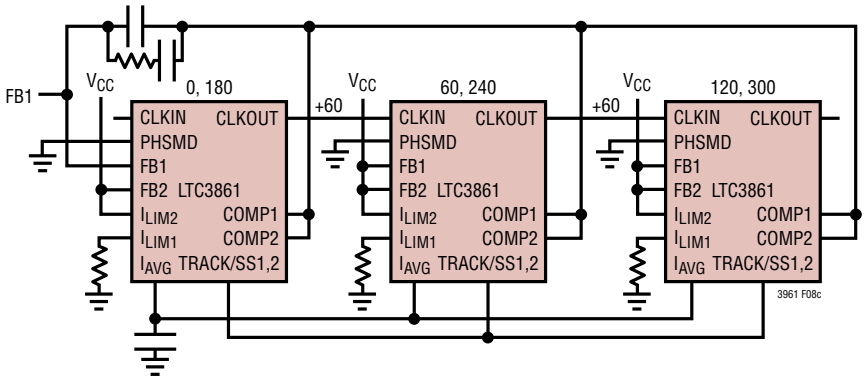

Figure 8c. 6-Phase Operation

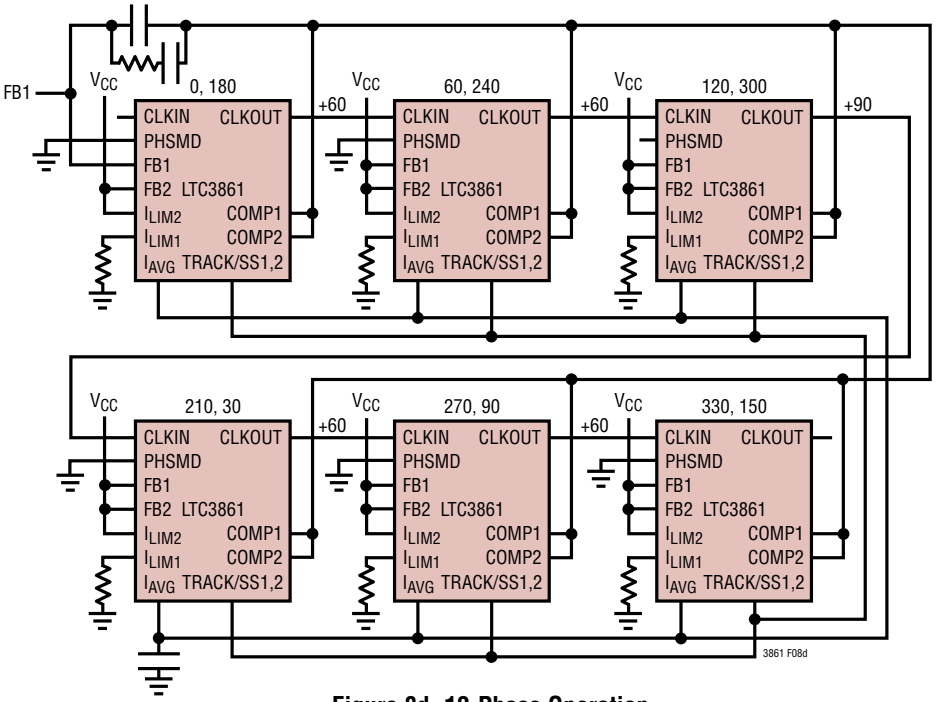

Figure 8d. 12-Phase Operation

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A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used. Figure 9 graphically illustrates the principle.

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst case RMS ripple current for a two stage design results in peak outputs of 1/4 and 3/4 of input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the current in each stage is balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for the single stage switching regulator. Figures 10 and 11 illustrate how the input and output currents are reduced by using an additional phase. For a 2-phase converter, the input current peaks drop in half and the frequency is doubled. The input capacitor requirement is thus reduced theoretically by a factor of four! Just imagine the possibility of capacitor savings with even higher number of phases!

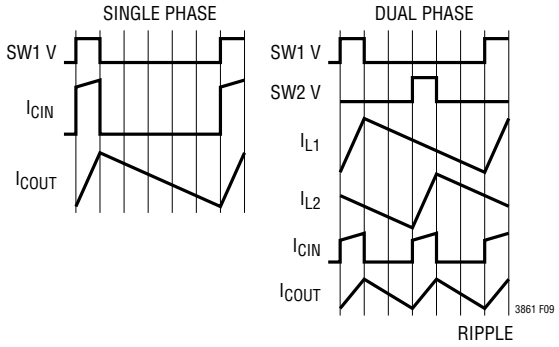

Figure 9. Single and 2-Phase Current Waveforms

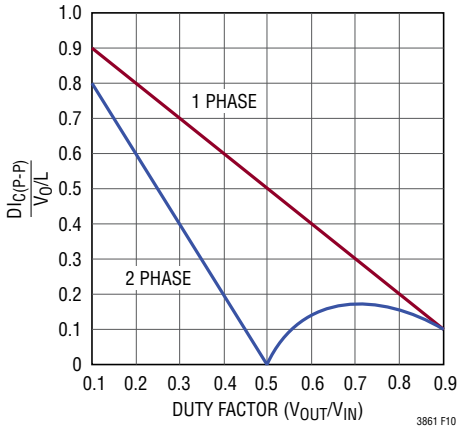

Figure 10. Normalized Output Ripple Current vs Duty Factor [I_{RMS}″ 0.3 ($DI_{C(PP)}$)]

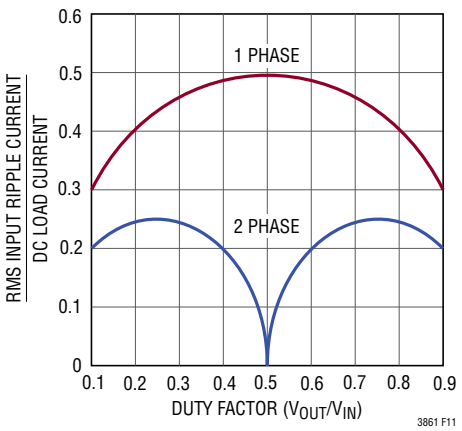

Figure 11. Normalized RMS Input Ripple Current vs Duty Factor for 1 and 2 Output Stages

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Output Current Sharing

When multiple LTC3861s are daisy chained to drive a common load, accurate output current sharing is essential to achieve optimal performance and efficiency. Otherwise, if one stage is delivering more current than another, then the temperature between the two stages will be different, and that could translate into higher switch $R_{DS(ON)}$, lower efficiency, and higher RMS ripple. When the COMP and I_{AVG} pins of multiple LTC3861s are tied together, the amount of output current delivered from each LTC3861 is actively balanced by the I_{AVG} loop. The SGND pins of the multiple LTC3861s must be kelvined to the same point for optimal current sharing.

Dual-Channel Operation

The LTC3861 can control two independent power supply outputs with no channel-to-channel interaction or jitter. The following recommendations will ensure maximum performance in this mode of operation:

- The output of each channel should be sensed using the differential sense amplifier. The SGND pins and exposed pad and all local small-signal GND should then be a Kelvin connection to the negative terminal of each channel output. This will provide the best possible regulation of each channel without adversely affecting the other channel.
- Due to internal logic used to determine the mode of operation, separate current limit resistors should be used for each channel in dual-channel operation, even when the values are the same.

Table 5 shows the I_{LIM} and EA configuration for dual-channel operation.

Table 5. Dual-Channel Configuration

CH1	CH2	EA1	EA2	I_{LIM1}	I_{LIM2}
Independent	Independent	On	On	Resistor to GND	Resistor to GND

Tracking and Soft-Start (TRACK/SS Pins)

The start-up of the supply output is controlled by the voltage on the TRACK/SS pin for that channel. The LTC3861 regulates the FB pin voltage to the lower of the voltage on the TRACK/SS pin and the internal 600mV reference. The TRACK/SS pin can therefore be used to program an external soft-start function or allow the output supply to track another supply during start-up.

External soft-start is enabled by connecting a capacitor from the TRACK/SS pin to SGND. An internal 2.5µA current source charges the capacitor, creating a linear voltage ramp at the TRACK/SS pin, and causing the output supply to rise smoothly from its prebiased value to its final regulated value. The total soft-start time is approximately:

$$t_{SS}(\text{milliseconds}) = C_{SS}\,\mu F \bullet \frac{600mV}{2.5\mu A}$$

Alternatively, the TRACK/SS pin can be used to track another supply during start-up.

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For example, Figure 12a shows the start-up of V_{OUT2} controlled by the voltage on the TRACK/SS2 pin. Normally this pin is used to allow the start-up of V_{OUT2} to track that of V_{OUT1} as shown qualitatively in Figures 12a and 12b. When the voltage on the TRACK/SS2 pin is less than the internal 0.6V reference, the LTC3861 regulates the FB2 voltage to the TRACK/SS2 pin voltage instead of 0.6V. The start-up of V_{OUT2} may ratiometrically track that of V_{OUT1}, according to a ratio set by a resistor divider (Figure 12c):

$$\frac{V_{OUT1}}{V_{OUT2}} = \frac{R2A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R2B + R2A}$$

For coincident tracking (V_{OUT1} = V_{OUT2} during start-up),

$R2A = R_{TRACKA}$

$R2B = R_{TRACKB}$

The ramp time for V_{OUT2} to rise from 0V to its final value is:

$$t_{SS2} = t_{SS1} \bullet \frac{0.6}{V_{OUT1F}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_{TRACKA}}$$

For coincident tracking,

$$t_{SS2} = t_{SS1} \bullet \frac{V_{OUT2F}}{V_{OUT1F}}$$

where V_{OUT1F} and V_{OUT2F} are the final, regulated values of V_{OUT1} and V_{OUT2}. V_{OUT1} should always be greater than V_{OUT2} when using the TRACK/SS2 pin for tracking. If no tracking function is desired, then the TRACK/SS2 pin may be tied to a capacitor to ground, which sets the ramp time to final regulated output voltage. It is only possible to track another supply that is slower than the internal soft-start ramp. **At the completion of tracking, the TRACK/SS pin must be >620mV, so as not to affect regulation accuracy and to ensure the part is in CCM mode.**

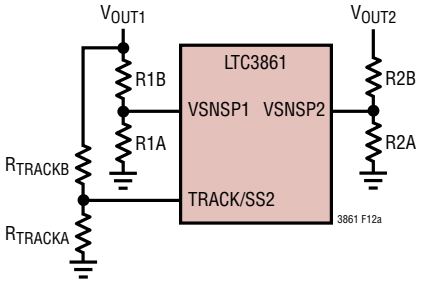
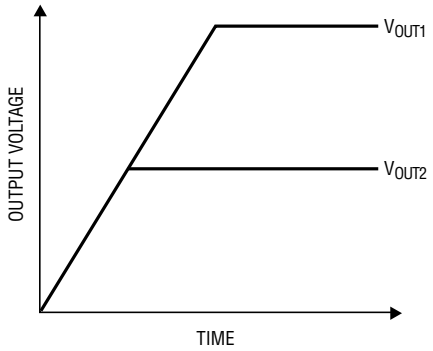
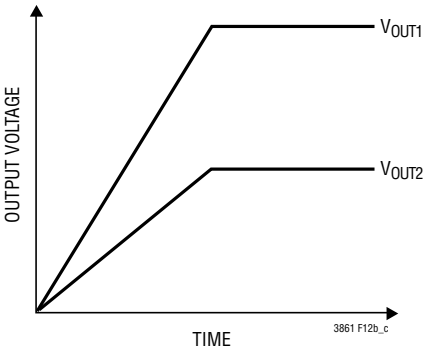


Figure 12a. Using the TRACK/SS Pin



(12b) Coincident Tracking



(12c) Ratiometric Tracking

Figures 12b and 12c. Two Different Modes of Output Voltage Tracking

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Feedback Loop Compensation

The LTC3861 is a voltage mode controller with a second dedicated current sharing loop to provide excellent phase-to-phase current sharing in multiphase applications. The current sharing loop is internally compensated.

While Type 2 compensation for the voltage control loop may be adequate in some applications (such as with the use of high ESR bulk capacitors), Type 3 compensation, along with ceramic capacitors, is recommended for optimum transient response. Referring to Figure 13, the error amplifiers sense the output voltage at V_{OUT}.

The positive input of the error amplifier is connected to an internal 600mV reference, while the negative input is connected to the FB pin. The output is connected to COMP, which is in turn connected to the line feedforward circuit and from there to the PWM generator. To speed up the overshoot recovery time, the maximum potential at the COMP pin is internally clamped.

Unlike many regulators that use a transconductance (g_m) amplifier, the LTC3861 is designed to use an inverting summing amplifier topology with the FB pin configured as a virtual ground. This allows the feedback gain to be tightly controlled by external components, which is not possible with a simple g_m amplifier. In addition, the voltage feedback amplifier allows flexibility in choosing pole and zero locations. In particular, it allows the use of Type 3 compensation, which provides a phase boost at the LC pole frequency and significantly improves the control loop phase margin.

In a typical LTC3861 circuit, the feedback loop consists of the line feedforward circuit, the modulator, the external inductor, the output capacitor and the feedback amplifier with its compensation network. All these components affect loop behavior and need to be accounted for in the loop compensation. The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearly with the input voltage. The line feedforward circuit compensates for this change in gain, and provides a constant gain from the error amplifier output to the inductor input regardless of input voltage. From a feedback loop point of view, the combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the inductor input. It has fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

The external inductor/output capacitor combination makes a more significant contribution to loop behavior. These components cause a second order LC roll-off at the output with 180° phase shift. This roll-off is what filters the PWM waveform, resulting in the desired DC output voltage, but this phase shift causes stability issues in the feedback loop and must be frequency compensated. At higher frequencies, the reactance of the output capacitor will approach its ESR, and the roll-off due to the capacitor will stop, leaving –20dB/decade and 90° of phase shift.

Figure 13 shows a Type 3 amplifier. The transfer function of this amplifier is given by the following equation:

$$\frac{V_{COMP}}{V_{OUT}} = \frac{-(1+sC1R2)[1+s(R1+R3)C3]}{sR1(C1+C2)[1+s(C1//C2)R2](1+sC3R3)}$$

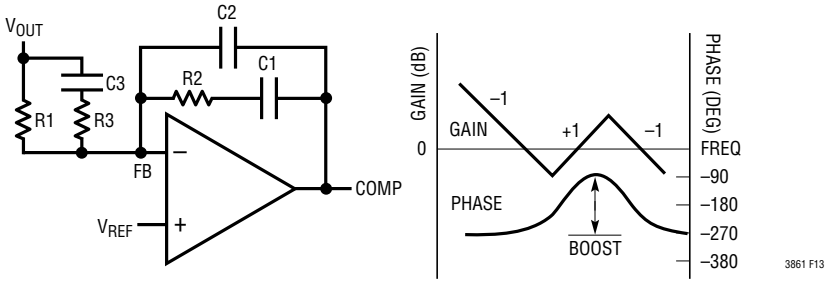


Figure 13. Type 3 Amplifier Compensation

APPLICATIONS INFORMATION

The RC network across the error amplifier and the feedforward components R3 and C3 introduce two pole-zero pairs to obtain a phase boost at the system unity-gain frequency, f_C. In theory, the zeros and poles are placed symmetrically around f_C, and the spread between the zeros and the poles is adjusted to give the desired phase boost at f_C. However, in practice, if the crossover frequency is much higher than the LC double-pole frequency, this method of frequency compensation normally generates a phase dip within the unity bandwidth and creates some concern regarding conditional stability.

If conditional stability is a concern, move the error amplifier's zero to a lower frequency to avoid excessive phase dip. The following equations can be used to compute the feedback compensation components value:

f_{SW} = Switching frequency

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$$

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$$

choose:

f_C = Crossover frequency = $\frac{f_{SW}}{10}$

$$f_{Z1(ERR)} = f_{LC} = \frac{1}{2\pi R2C1}$$

$$f_{Z2(RES)} = \frac{f_C}{5} = \frac{1}{2\pi(R1+R3)C3}$$

$$f_{P1(ERR)} = f_{ESR} = \frac{1}{2\pi R2(C1//C2)}$$

$$f_{P2(RES)} = 5f_C = \frac{1}{2\pi R3C3}$$

Required error amplifier gain at frequency f_C:

$$A \approx 40\log\sqrt{1+\left(\frac{f_C}{f_{LC}}\right)^2} - 20\log\sqrt{1+\left(\frac{f_C}{f_{ESR}}\right)^2} - 20\log(A_{MOD})$$

$$\approx 20\log\frac{R2}{R1}\bullet\frac{\left(1+\frac{f_{LC}}{f_C}\right)\left(1+\frac{f_{P2(RES)}}{f_C}+\frac{f_{P2(RES)}-f_{Z2(RES)}}{f_{Z2(RES)}}\right)}{\left(1+\frac{f_C}{f_{ESR}}+\frac{f_{LC}}{f_{ESR}-f_{LC}}\right)\left(1+\frac{f_{P2(RES)}}{f_C}\right)}$$

where AMOD is the modulator and line feedforward gain and is equal to:

$$A_{MOD} \approx \frac{V_{IN(MAX)}\bullet DC_{MAX}}{V_{RAMP}} \approx 12V/V$$

where DC_{MAX} is the maximum duty cycle and V_{RAMP} is the line feedforward compensated PWM ramp voltage.

Once the value of resistor R1, poles and zeros location have been decided, the value of R2, C1, C2, R3 and C3 can be obtained from the previous equations.

Compensating a switching power supply feedback loop is a complex task. The applications shown in this data sheet show typical values, optimized for the power components shown. Though similar power components should suffice, substantially changing even one major power component may degrade performance significantly. Stability also may depend on circuit board layout. To verify the calculated component values, all new circuit designs should be prototyped and tested for stability.

APPLICATIONS INFORMATION

Inductor

The inductor in a typical LTC3861 circuit is chosen for a specific ripple current and saturation current. Given an input voltage range and an output voltage, the inductor value and operating frequency directly determine the ripple current. The inductor ripple current in the buck mode is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors and output voltage ripple. Thus highest efficiency operation is obtained at low frequency with small ripple current. To achieve this however, requires a large inductor.

A reasonable starting point is to choose a ripple current between 20% and 40% of $I_{O(MAX)}$. Note that the largest ripple current occurs at the highest V_{IN}. To guarantee that ripple current does not exceed a specified maximum, the inductor in buck mode should be chosen according to:

$$L \geq \frac{V_{OUT}}{f\,\Delta I_{L(MAX)}}\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Power MOSFET Selection

The LTC3861 requires at least two external N-channel power MOSFETs per channel, one for the top (main) switch and one or more for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, input capacitance, breakdown voltage and maximum output current.

For maximum efficiency, on-resistance $R_{DS(ON)}$ and input capacitance should be minimized. Low $R_{DS(ON)}$ minimizes conduction losses and low input capacitance minimizes switching and transition losses. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 14).

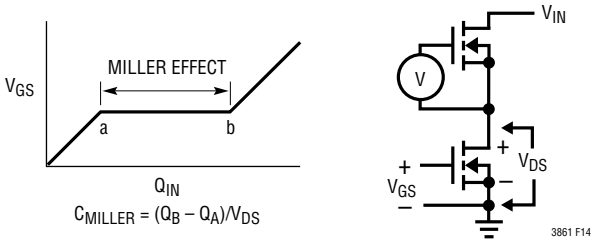


Figure 14. Gate Charge Characteristic

The curve is generated by forcing a constant-input current into the gate of a common source, current source loaded stage and then plotting the gate voltage versus time. The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying by the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturers data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included.

APPLICATIONS INFORMATION

When the controller is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + V_{IN}{}^2\frac{I_{MAX}}{2}(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{CC}-V_{TH(IL)}}+\frac{1}{V_{TH(IL)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(0N)}$$

where δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance, V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique previously described.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve. Typical values for δ range from 0.005/°C to 0.01/°C depending on the particular MOSFET used.

Multiple MOSFETs can be used in parallel to lower $R_{DS(ON)}$ and meet the current and thermal requirements if desired. Suitable drivers such as the LTC4449 are capable of driving large gate capacitances without significantly slowing transition times. In fact, when driving MOSFETs with very low gate charge, it is sometimes helpful to slow down the drivers by adding small gate resistors (5Ω or less) to reduce noise and EMI caused by the fast transitions

MOSFET Driver Selection

Gate driver ICs, DrMOSs and power blocks with an interface compatible with the LTC3861's three-state PWM outputs or the LTC3861's PWM/PWMEN outputs can be used.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% - (L1 + L2 + L3 + …)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the system produce losses, three main sources usually account for most of the losses in LTC3861 applications: 1) I^2R losses, 2) topside MOSFET transition losses, 3) gate drive current.

1. I^2R losses occur mainly in the DC resistances of the MOSFET, inductor, PCB routing, and input and output capacitor ESR. Since each MOSFET is only on for part of the cycle, its on-resistance is effectively multiplied by the percentage of the cycle it is on. Therefore in high step-down ratio applications the bottom MOSFET should have a much lower $R_{DS(ON)}$ than the top MOSFET. It is crucial that careful attention is paid to the layout of the power path on the PCB to minimize its resistance. In a 2-phase, 1.2V output, 60A system, 1mΩ of PCB resistance at the output costs 5% in efficiency.
2. Transition losses apply only to the topside MOSFET but in 12V input applications are a very significant source of loss. They can be minimized by choosing a driver with very low drive resistance and choosing a MOSFET with low Q_G, R_G and C_{RSS}.
3. Gate drive current is equal to the sum of the top and bottom MOSFET gate charges multiplied by the frequency of operation. However, many drivers employ a linear regulator to reduce the input voltage to a lower gate drive voltage. This multiplies the gate loss by that step down ratio. In high frequency applications it may be worth using a secondary user supplied rail for gate drive to avoid the linear regulator.

APPLICATIONS INFORMATION

Other sources of loss include body or Schottky diode conduction during the driver dependent non-overlap time and inductor core losses.

Design Example

As a design example, consider a 2-phase application where V_{IN} = 12V, V_{OUT} = 1.2V, I_{LOAD} = 60A and f_{SWITCH} = 300kHz. Assume that a secondary 5V supply is available for the LTC3861 V_{CC} supply.

The inductance value is chosen based on a 25% ripple assumption. Each channel supplies an average 30A to the load resulting in 7.7A peak-peak ripple:

$$\Delta I_L = \frac{V_{OUT} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f \bullet L}$$

A 470nH inductor per phase will create 7.7A peak-to-peak ripple. A 0.47µH inductor with a DCR of 0.67mΩ typical is selected from the Würth 744355147 series. Float CLKIN and connect 28kΩ from FREQ to SGND for 300kHz operation. Setting I_{LIMIT} = 54A per phase leaves plenty of headroom for transient conditions while still adequately protecting against inductor saturation. This corresponds to:

$$R_{ILIM} = \frac{18.5 \bullet 54A \bullet 0.67m\Omega + 0.53V}{20\mu A} = 58.5k\Omega$$

Choose 59kΩ.

For the DCR sense filter network, we can choose R = 2.87k and C = 220nF to match the L/DCR time constant of the inductor.

A loop crossover frequency of 45kHz provides good transient performance while still being well below the switching frequency of the converter. Six 330µF 9mΩ POSCAPs and four 100µF ceramic capacitors are chosen for the output capacitors to maintain supply regulation during severe transient conditions and to minimize output voltage ripple.

The following compensation values (Figure 13) were determined empirically:

R1 = 10k
R2 = 5.9k
R3 = 280Ω
C1 = 4.7nF
C2 = 100pF
C3 = 3.3nF

To set the output voltage equal to 1.2V:

R_{FB1} = 10k, R_{FB2} = 10k

The LTC4449 gate driver and external MOSFETs are chosen for the power stage. DrMOSs from Fairchild, Infineon, Vishay and others can also be used.

Printed Circuit Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the converter.

1. The connection between the SGND pin on the LTC3861 and all of the small-signal components surrounding the IC should be isolated from the system power ground. Place all decoupling capacitors, such as the ones on V_{CC}, between ISNSP and ISNSN etc., close to the IC. In multiphase operation SGND should be Kelvin-connected to the main ground node near the bottom terminal of the input capacitor. In dual-channel operation, SGND should be Kelvin-connected to the bottom terminal of the output capacitor for channel 2, and channel 1 should be remotely sensed using the remote sense differential amplifier.
2. Place the small-signal components away from high frequency switching nodes on the board. The LTC3861 contains remote sensing of output voltage and inductor current and logic-level PWM outputs enabling the IC to be isolated from the power stage.
3. The PCB traces for remote voltage and current sense should avoid any high frequency switching nodes in the circuit and should ideally be shielded by ground planes. Each pair (V_{SNSP} and V_{SNSN}, I_{SNSP} and I_{SNSN}) should be routed parallel to one another with

APPLICATIONS INFORMATION

minimum spacing between them. If DCR sensing is used, place the top resistor (Figure 6b, R1) close to the switching node.

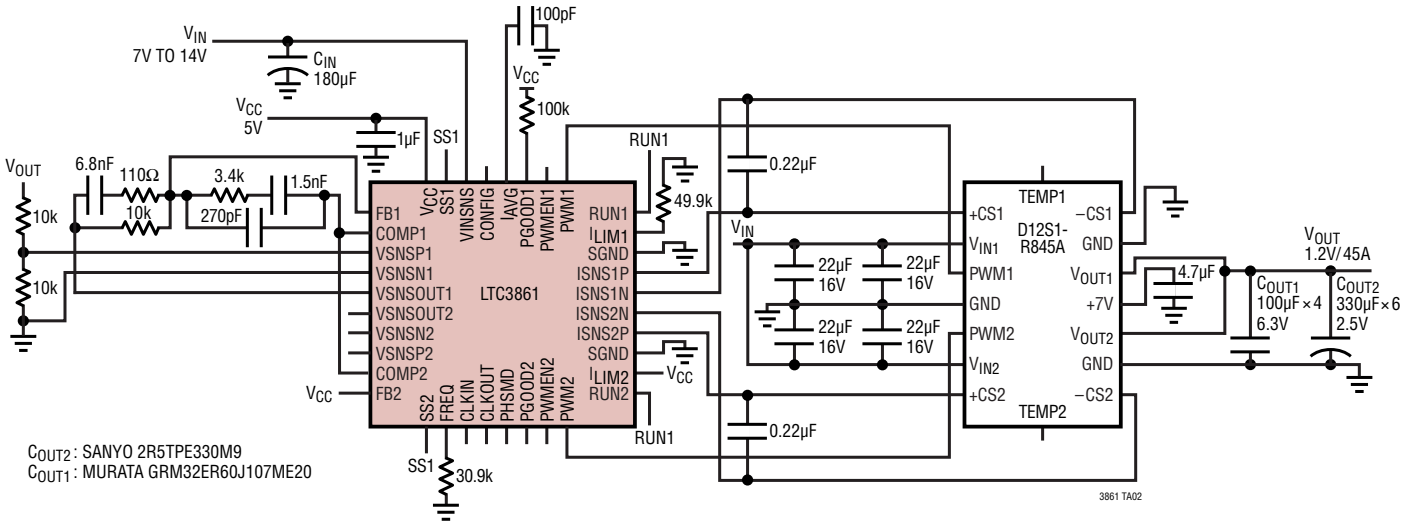
4. The input capacitor should be kept as close as possible to the power MOSFETs. The loop from the input capacitor's positive terminal, through the MOSFETs and back to the input capacitor's negative terminal should also be as small as possible.

5. If using discrete drivers and MOSFETs, check the stress on the MOSFETs by independently measuring the drain-to-source voltages directly across the device terminals. Beware of inductive ringing that could exceed the maximum voltage rating of the MOSFET. If this ringing cannot be avoided and exceeds the maximum rating of the device, choose a higher voltage rated MOSFET.

6. When cascading multiple LTC3861 ICs, minimize the capacitive load on the CLKOUT pin to minimize phase error. Kelvin all the LTC3861 IC grounds to the same point, typically SGND of the IC containing the master.

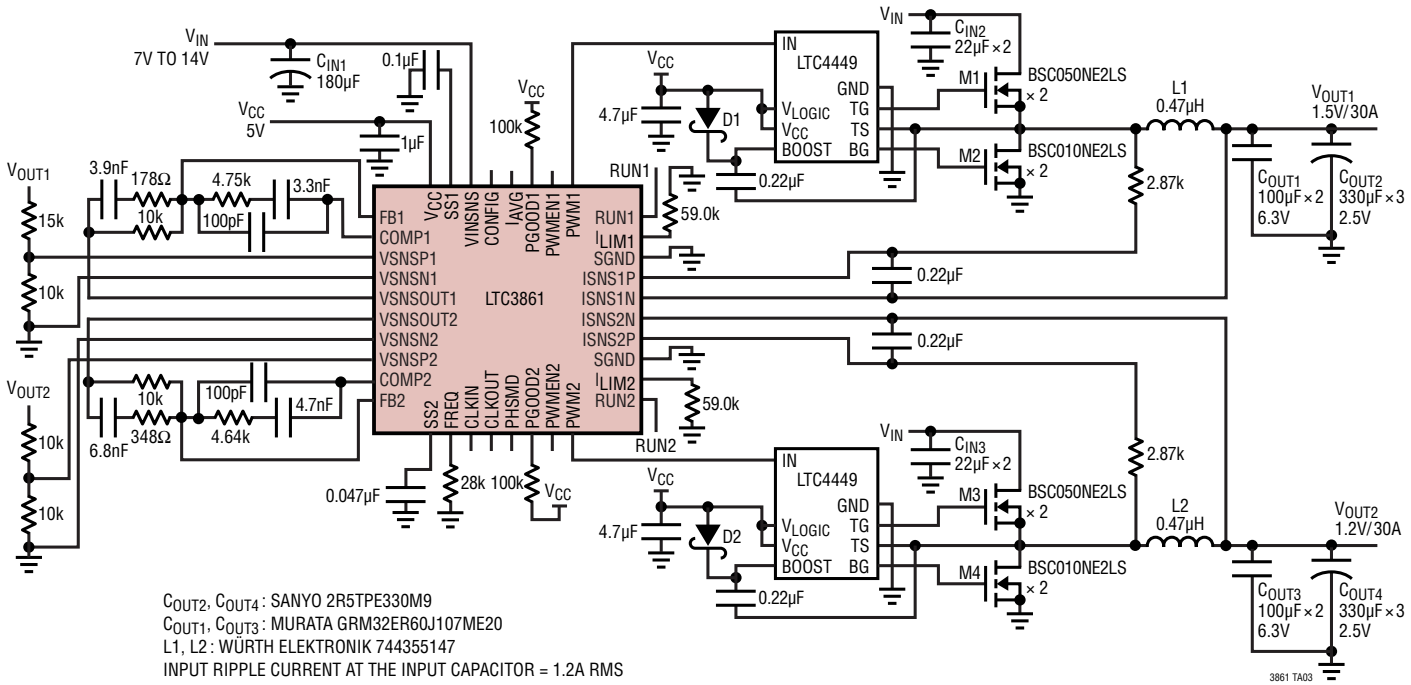
TYPICAL APPLICATIONS

Dual Phase 1.2V/45A Converter with Delta 45A Power Block, f_{SW} = 400kHz



TYPICAL APPLICATIONS

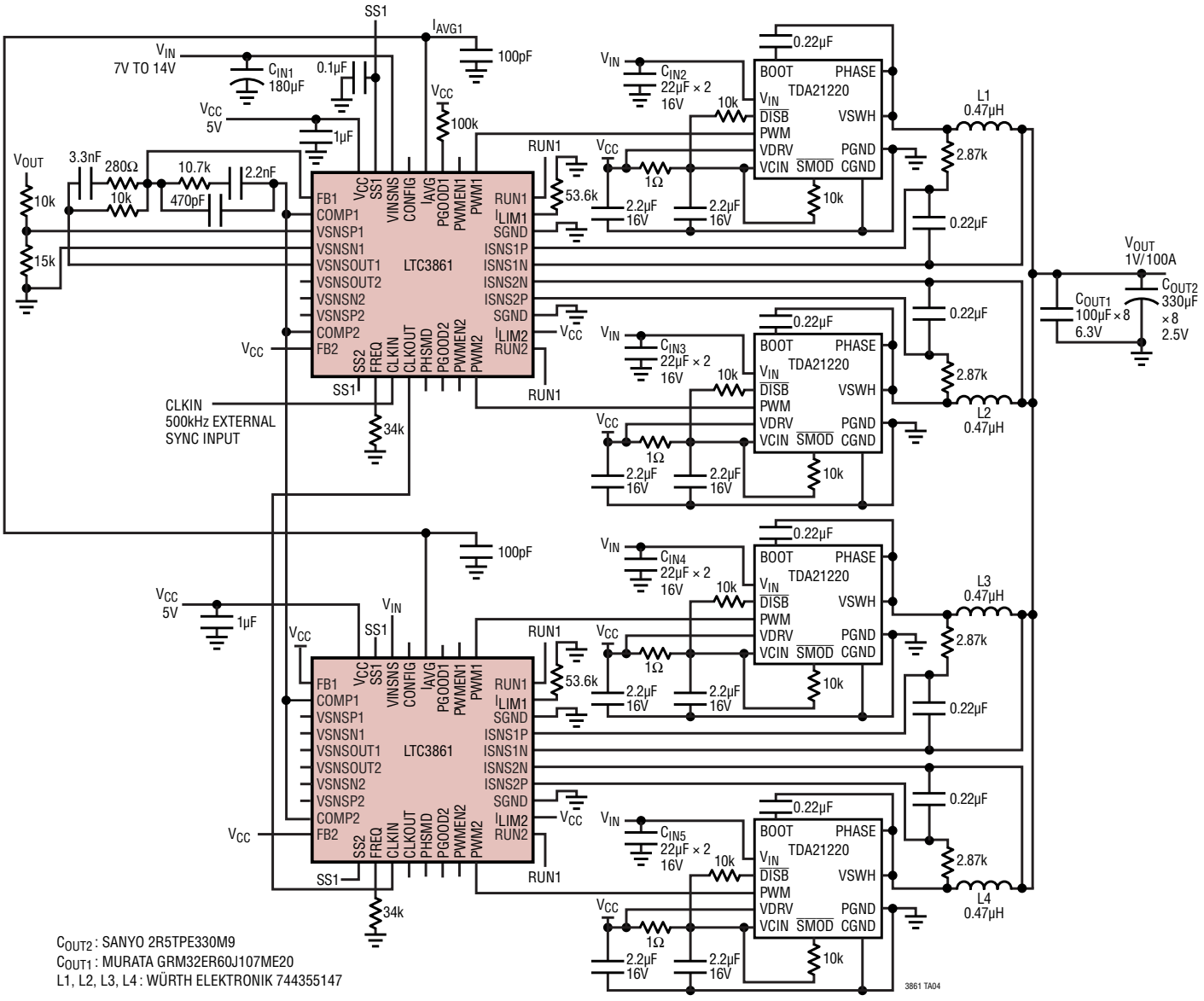
1.5V/30A and 1.2V/30A Converter with Discrete Gate Drivers and MOSFETs, f_{SW} = 300kHz



C_{OUT2}, C_{OUT4} : SANYO 2R5TPE330M9
C_{OUT1}, C_{OUT3} : MURATA GRM32ER60J107ME20
L1, L2 : WÜRTH ELEKTRONIK 744355147
INPUT RIPPLE CURRENT AT THE INPUT CAPACITOR = 1.2A RMS
OUTPUT RIPPLE CURRENT AT THE OUTPUT CAPACITOR = 1.8A RMS

TYPICAL APPLICATIONS

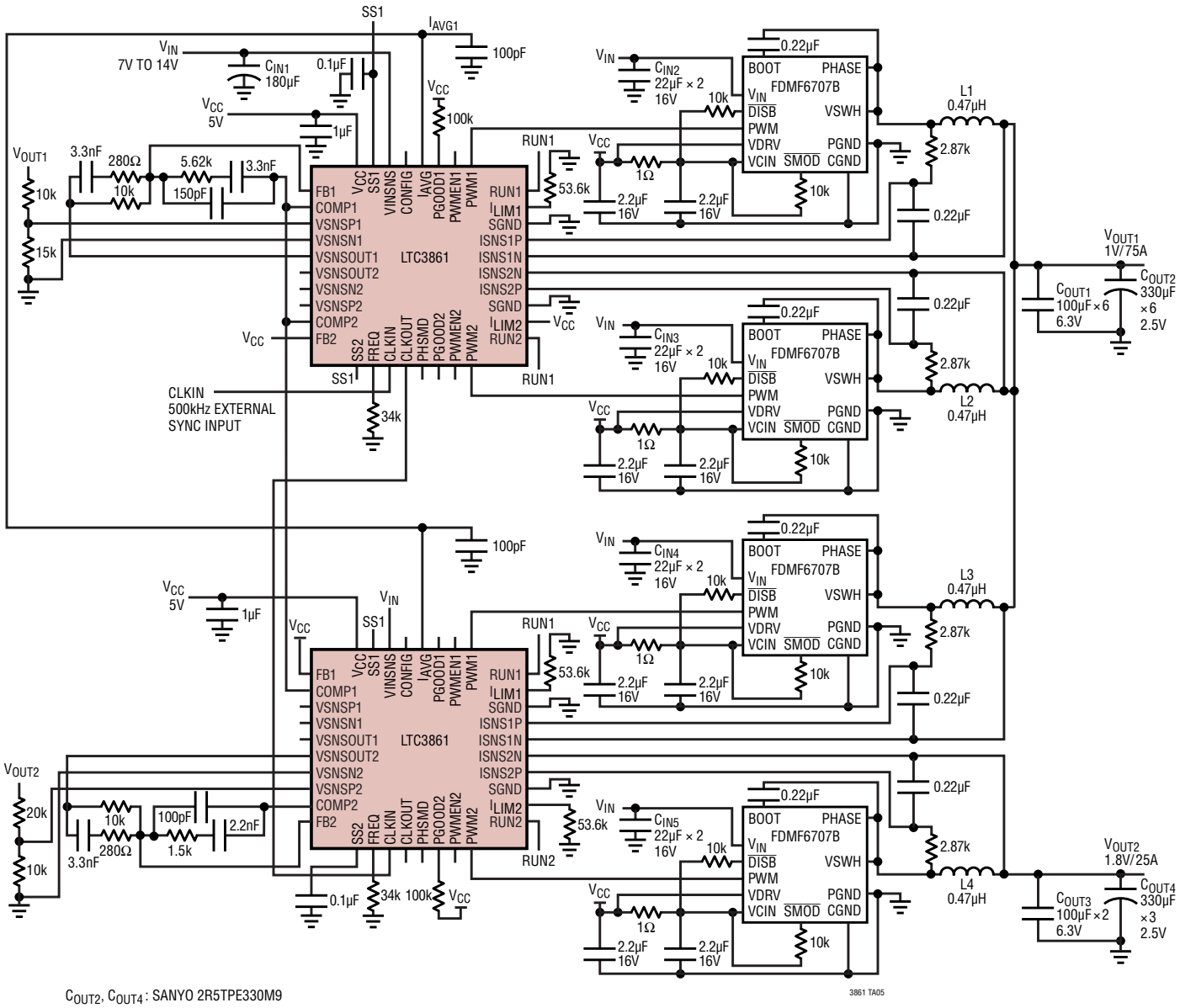
4-Phase 1V/100A Converter with DrMOS, f_{SW} = 500kHz



C_{OUT2} : SANYO 2R5TPE330M9
C_{OUT1} : MURATA GRM32ER60J107ME20
L1, L2, L3, L4 : WÜRTH ELEKTRONIK 744355147

TYPICAL APPLICATIONS

Dual-Output Converter: Triple Phase + Single Phase with DrMOS, Synchronized to an External 500kHz Clock

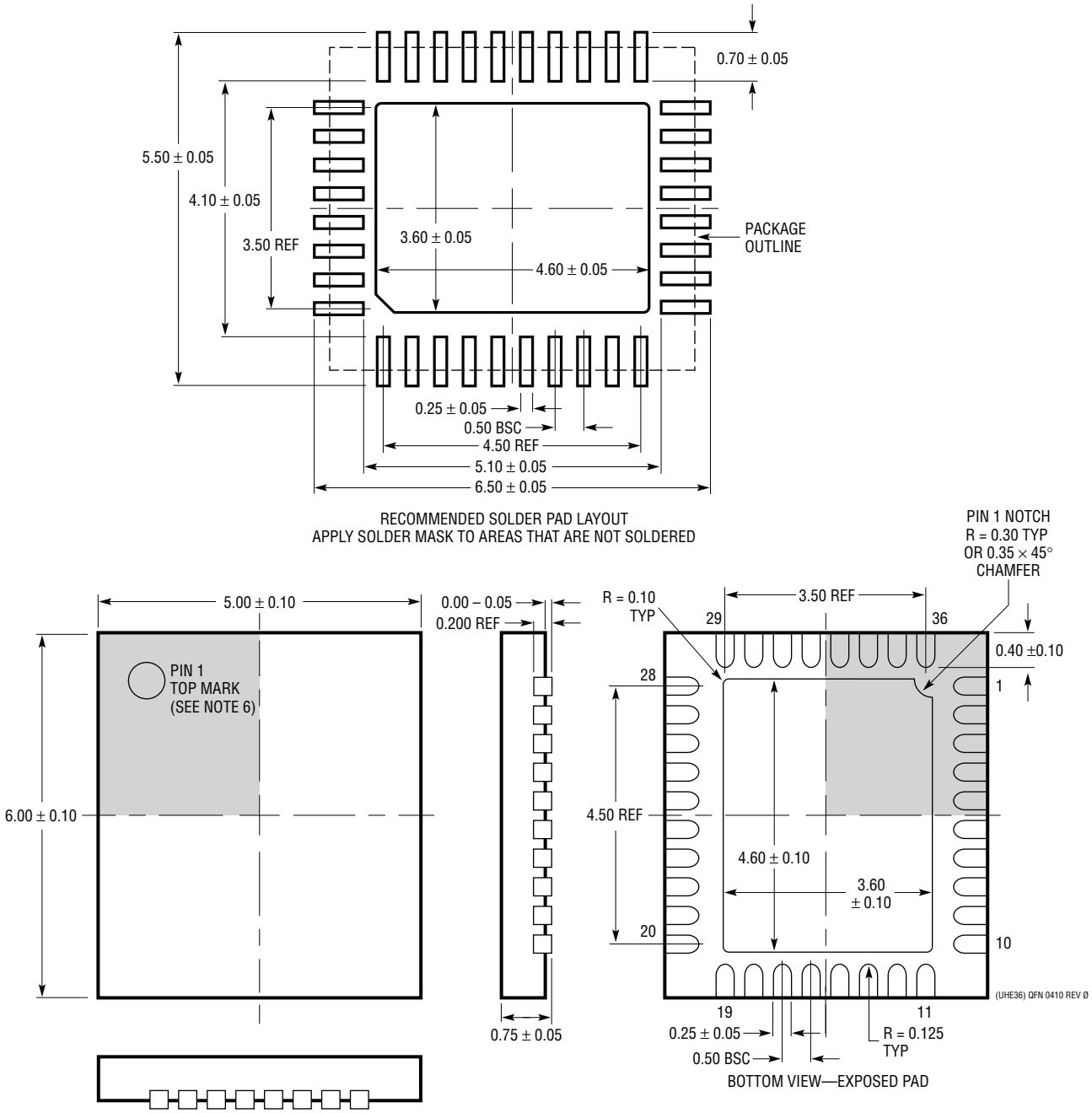


C_{OUT2}, C_{OUT4}: SANYO 2R5TPE330M9
C_{OUT1}, C_{OUT3}: MURATA GRM32ER60J107ME20
L1, L2, L3, L4: WÜRTH ELEKTRONIK 744355147

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UHE Package
36-Lead Plastic QFN (5mm × 6mm)
(Reference LTC DWG # 05-08-1876 Rev Ø)



NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/13	Fixed schematics, graphs, tables, and clarified text	1, 9, 11, 31, 32, 33, 34
B	04/15	Modified I_{AVG} paragraph	9
		Clarified frequency synchronization paragraph	18
		Changed I_{SAT} equation	19
		Clarified multiphase operation paragraph	22

LINEAR TECHNOLOGY

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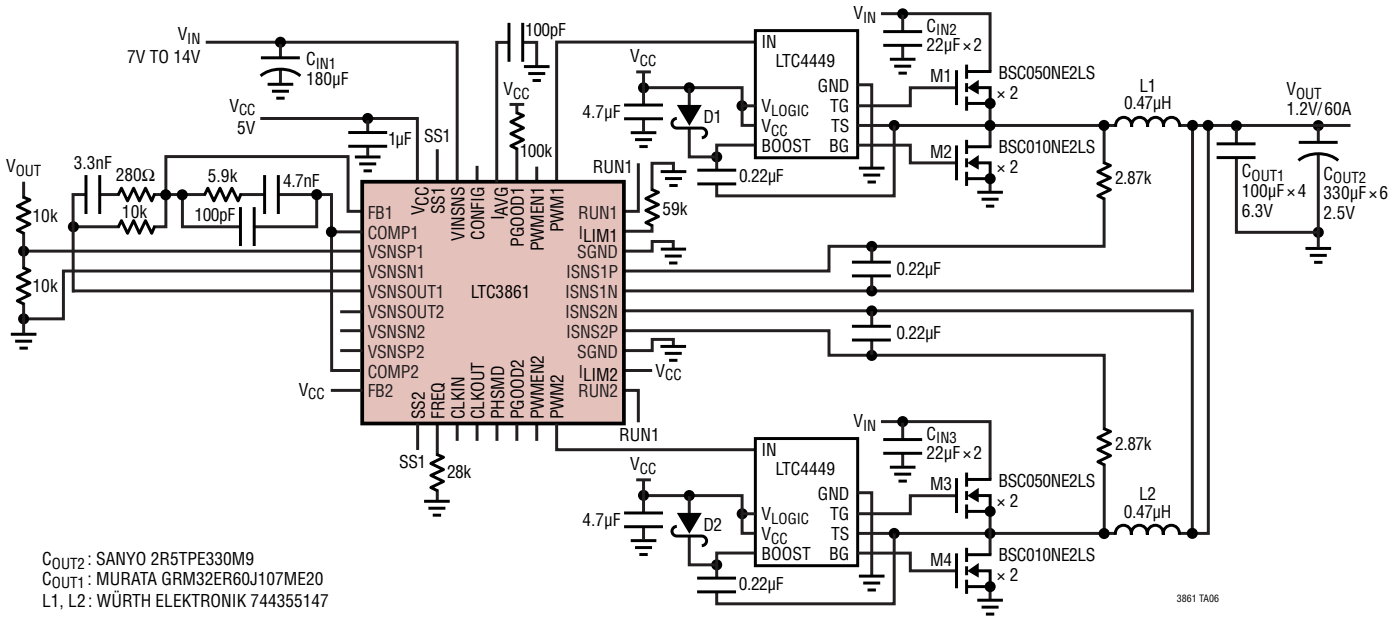
TYPICAL APPLICATION

Dual Phase 1.2V/60A Converter with Discrete Gate Drivers and MOSFETs, f_{SW} = 300kHz



COUT2 : SANYO 2R5TPE330M9
COUT1 : MURATA GRM32ER60J107ME20
L1, L2 : WÜRTH ELEKTRONIK 744355147

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3880/ LTC3880-1	Dual Output PolyPhase Step-Down DC/DC Controller with Digital Power System Management	V_{IN} Up to 24V, 0.5V ≤ V_{OUT} ≤ 5.5V, Analog Control Loop, I^2C/PMBus Interface with EEPROM and 16-Bit ADC
LTC3855	Dual Output, 2-Phase, Synchronous Step-Down DC/DC Controller with Diffamp and DCR Temperature Compensation	4.5V≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 12V, PLL Fixed Frequency 250kHz to 770kHz
LTC3856	Single Output 2-Phase Synchronous Step-Down DC/DC Controller with Diffamp and DCR Temperature Compensation	4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5V, PLL Fixed 250kHz to 770kHz Frequency
LTC3838	Dual Output, 2-Phase, Synchronous Step-Down DC/DC Controller with Diffamp and Controlled On-Time	4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.5V, PLL, Up to 2MHz Switching Frequency
LTC3839	Single Output, 2-Phase, Synchronous Step-Down DC/DC Controller with Diffamp and Controlled On-Time	4.5V ≤ V_{IN} ≤ 38V, 0.8V ≤ V_{OUT} ≤ 5.5V, PLL, Up to 2MHz Switching Frequency
LTC3860	Dual, Multiphase, Synchronous Step-Down DC/DC Controller with Diffamp and Three-State Output Drive	Operates with Power Blocks, DrMOS Devices or External MOSFETs, 3V ≤ V_{IN} ≤ 24V, $t_{ON(MIN)}$ = 20ns
LTC3869/ LTC3869-2	Dual Output, 2-Phase Synchronous Step-Down DC/DC Controller, with Accurate Current Share	4V≤ V_{IN} ≤ 38V, V_{OUT3} Up to 12.5V, PLL Fixed 250kHz to 750kHz Frequency
LTC3866	Single Output, High Power, Current Mode Controller with Sub-milliohm DCR Sensing	4.75V≤ V_{IN} ≤ 38V, 0.6V≤ V_{OUT} ≤ 3.5V, Fixed 250kHz to 770kHz Frequency
LTC4449	High Speed Synchronous N-Channel MOSFET Driver	V_{IN} Up to 38V, 4V ≤ V_{CC} ≤ 6.5V, Adaptive Shoot-Through Protection, 2mm × 3mm DFN-8 Package
LTC4442/ LTC4442-1	High Speed Synchronous N-Channel MOSFET Driver	V_{IN} Up to 38V, 6V ≤ V_{CC} ≤ 9V Adaptive Shoot-Through Protection, MSOP-8 Package

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- Alternative Solution
- Excess Inventory Management