

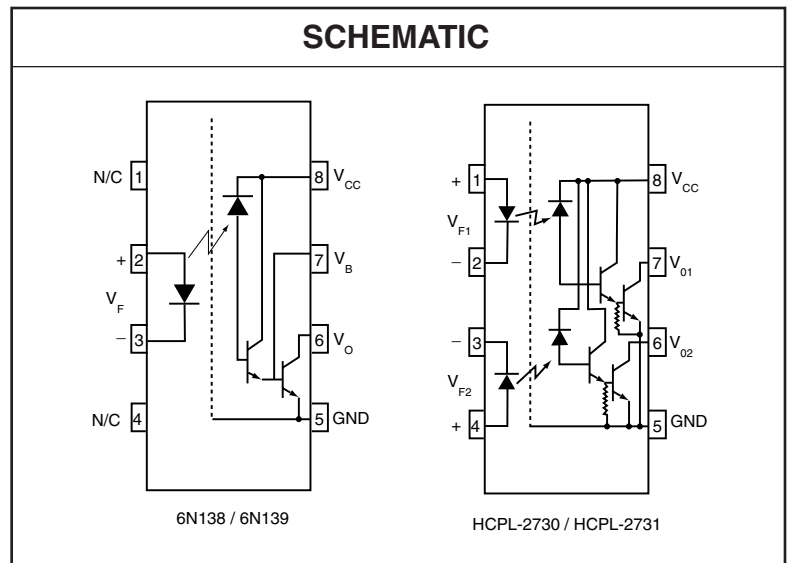
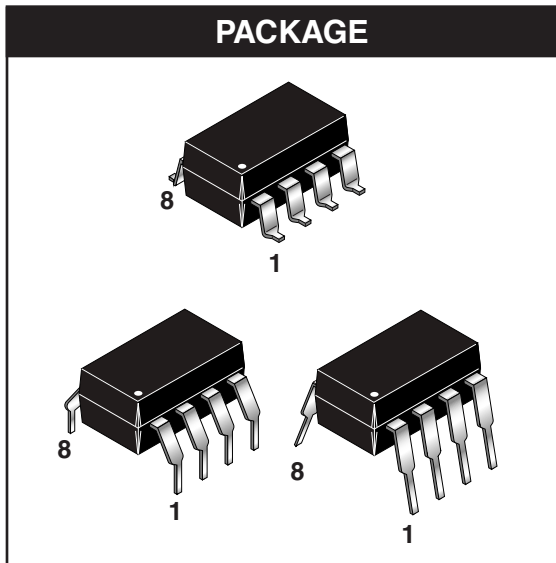


**THE DATASHEET OF  
6N138WV**



**SINGLE-CHANNEL: 6N138**  
**DUAL-CHANNEL: HCPL-2730**

**6N139**  
**HCPL-2731**



## DESCRIPTION

The 6N138/9 and HCPL-2730/HCPL-2731 optocouplers consist of an AlGaAs LED optically coupled to a high gain split darlington photodetector.

The split darlington configuration separating the input photodiode and the first stage gain from the output transistor permits lower output saturation voltage and higher speed operation than possible with conventional darlington phototransistor optocoupler. In the dual channel devices, HCPL-2730/HCPL2731, an integrated emitter - base resistor provides superior stability over temperature.

The combination of a very low input current of 0.5 mA and a high current transfer ratio of 2000% makes this family particularly useful for input interface to MOS, CMOS, LSTTL and EIA RS232C, while output compatibility is ensured to CMOS as well as high fan-out TTL requirements. An internal noise shield provides exceptional common mode rejection of 10 kV/ $\mu$ s.

## FEATURES

- Low current - 0.5 mA
- Superior CTR-2000%
- Superior CMR-10 kV/ $\mu$ s
- CTR guaranteed 0-70°C
- U.L. recognized (File # E90700)
- VDE recognized (File # 120915) Ordering option V, e.g., 6N138V
- Dual Channel - HCPL-2730
- HCPL-2731

## APPLICATIONS

- Digital logic ground isolation
- Telephone ring detector
- EIA-RS-232C line receiver
- High common mode noise line receiver
- $\mu$ P bus isolation
- Current loop receiver

**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

**ABSOLUTE MAXIMUM RATINGS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Value	Units
Storage Temperature	$T_{STG}$	-55 to +125	$^\circ\text{C}$
Operating Temperature	$T_{OPR}$	-40 to +85	$^\circ\text{C}$
Lead Solder Temperature (Wave solder only. See recommended reflow profile graph for convection or infrared reflow soldering process limits)	$T_{SOL}$	260 for 10 sec	$^\circ\text{C}$
<b>EMITTER</b>			
DC/Average Forward Input Current	Each Channel	$I_F$ (avg)	20 mA
Peak Forward Input Current (50% duty cycle, 1 ms P.W.)	Each Channel	$I_F$ (pk)	40 mA
Peak Transient Input Current - ( $\leq 1 \mu\text{s}$ P.W., 300 pps)		$I_F$ (trans)	1.0 A
Reverse Input Voltage	Each Channel	$V_R$	5 V
Input Power Dissipation	Each Channel	$P_D$	35 mW
<b>DETECTOR</b>			
Average Output Current	Each Channel	$I_O$ (avg)	60 mA
Emitter-Base Reverse Voltage	(6N138 and 6N139)	$V_{ER}$	0.5 V
Supply Voltage, Output Voltage	(6N138, HCPL-2730)	$V_{CC}, V_O$	-0.5 to 7
	(6N139, HCPL-2731)		-0.5 to 18
Output Power Dissipation	Each Channel	$P_O$	100 mW

SINGLE-CHANNEL: 6N138

6N139

DUAL-CHANNEL: HCPL-2730

HCPL-2731

**ELECTRICAL CHARACTERISTICS** ( $T_A = 0$  to  $70^\circ\text{C}$  Unless otherwise specified)

**INDIVIDUAL COMPONENT CHARACTERISTICS**

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
<b>EMITTER</b> Input Forward Voltage	$T_A = 25^\circ\text{C}$ Each channel ( $I_F = 1.6$ mA)	$V_F$	All		1.30	1.7	V
					1.75		
Input Reverse Breakdown Voltage	( $T_A = 25^\circ\text{C}$ , $I_R = 10$ $\mu\text{A}$ ) Each Channel	$BV_R$	All	5.0	20		V
Temperature coefficient of forward voltage	( $I_F = 1.6$ mA)	$(\Delta V_F / \Delta T_A)$	All		-1.8		mV/ $^\circ\text{C}$
<b>DETECTOR</b> Logic high output current	( $I_F = 0$ mA, $V_O = V_{CC} = 18$ V) Each Channel	$I_{OH}$	6N139		0.01	100	$\mu\text{A}$
			HCPL-2731				
	( $I_F = 0$ mA, $V_O = V_{CC} = 7$ V) Each Channel		6N138		0.01	250	
			HCPL-2730				
Logic low supply	( $I_F = 1.6$ mA, $V_O = \text{Open}$ ) ( $V_{CC} = 18$ V)	$I_{CCL}$	6N138 6N139		0.4	1.5	mA
	( $I_{F1} = I_{F2} = 1.6$ mA, $V_{CC} = 18$ V)		HCPL-2731		1.3	3	
	( $V_{O1} - V_{O2} = \text{Open}$ , $V_{CC} = 7$ V)		HCPL-2730				
Logic high supply	( $I_F = 0$ mA, $V_O = \text{Open}$ , $V_{CC} = 18$ V)	$I_{CCH}$	6N135 6N136		0.05	10	$\mu\text{A}$
	( $I_{F1} = I_{F2} = 0$ mA, $V_{CC} = 18$ V)		HCPL-2731		0.10	20	
	( $V_{O1} - V_{O2} = \text{Open}$ , $V_{CC} = 7$ V)		HCPL-2730				

\*\* All Typical at  $T_A = 25^\circ\text{C}$

**SINGLE-CHANNEL: 6N138**

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**DUAL-CHANNEL: HCPL-2730**

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**TRANSFER CHARACTERISTICS** ( $T_A = 0$  to  $70^\circ\text{C}$  Unless otherwise specified)

Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit
<b>COUPLED</b>  Current transfer ratio (Note 1, 2)	$(I_F = 0.5 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V})$ Each Channel	CTR	6N139	400	1100		%
			HCPL-2731		3500		
	$(I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N139	500	1300		%
			HCPL-2731		2500		
	$(I_F = 1.6 \text{ mA}, V_O = 0.4 \text{ V}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N138	300	1300		%
			HCPL-2730		2500		
Logic low output voltage output voltage (Note 2)	$(I_F = 0.5 \text{ mA}, I_O = 2 \text{ mA}, V_{CC} = 4.5 \text{ V})$	V <sub>OL</sub>	6N139		0.08	0.4	V
	$(I_F = 1.6 \text{ mA}, I_O = 8 \text{ mA}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N139		0.01	0.4	
			HCPL-2731				
	$(I_F = 0.5 \text{ mA}, I_O = 15 \text{ mA}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N139		0.13	0.4	
			HCPL-2731				
	$(I_F = 12 \text{ mA}, I_O = 24 \text{ mA}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N139		0.20	0.4	
			HCPL-2731				
	$(I_F = 1.6 \text{ mA}, I_O = 4.8 \text{ mA}, V_{CC} = 4.5 \text{ V})$ Each Channel		6N138		0.10	0.4	
	HCPL-2730						

\*\* All Typicals at  $T_A = 25^\circ\text{C}$

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<b>SWITCHING CHARACTERISTICS</b> ( $T_A = 0$ to $70^\circ\text{C}$ unless otherwise specified., $V_{CC} = 5\text{ V}$ )								
Parameter	Test Conditions	Symbol	Device	Min	Typ**	Max	Unit	
Propagation delay time to logic low (Note 2) (Fig. 22)	( $R_L = 4.7\text{ k}\Omega$ , $I_F = 0.5\text{ mA}$ ) $T_A = 25^\circ\text{C}$	$T_{PHL}$	6N139			30	$\mu\text{s}$	
				4	25			
	( $R_L = 4.7\text{ k}\Omega$ , $I_F = 0.5\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		HCPL-2731			120		
				3	100			
	( $R_L = 270\ \Omega$ , $I_F = 12\text{ mA}$ ) $T_A = 25^\circ\text{C}$		6N139			2		
				0.2	1			
	( $R_L = 270\ \Omega$ , $I_F = 12\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		HCPL-2730			3		
			HCPL-2731			0.3		2
Propagation delay time to logic high (Note 2) (Fig. 22)	( $R_L = 2.2\text{ k}\Omega$ , $I_F = 1.6\text{ mA}$ ) $T_A = 25^\circ\text{C}$	$T_{PLH}$	6N138			15	$\mu\text{s}$	
				1.5	10			
	( $R_L = 2.2\text{ k}\Omega$ , $I_F = 1.6\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		HCPL-2731			25		
			HCPL-2730			1		20
	( $R_L = 4.7\text{ k}\Omega$ , $I_F = 0.5\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		6N139			90		
			HCPL-2731					
	( $R_L = 4.7\text{ k}\Omega$ , $I_F = 0.5\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		6N139			12		60
			HCPL-2731			22		
Propagation delay time to logic high (Note 2) (Fig. 22)	( $R_L = 270\ \Omega$ , $I_F = 12\text{ mA}$ ) $T_A = 25^\circ\text{C}$	$T_{PLH}$	6N139			10	$\mu\text{s}$	
				1.3	7			
	( $R_L = 270\ \Omega$ , $I_F = 12\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		HCPL-2730			15		
			HCPL-2731			5		10
	( $R_L = 2.2\text{ k}\Omega$ , $I_F = 1.6\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		6N138			50		
			HCPL-2730/1					
	( $R_L = 2.2\text{ k}\Omega$ , $I_F = 1.6\text{ mA}$ ) Each Channel $T_A = 25^\circ\text{C}$		6N138			7		35
			HCPL-2730/1			16		
Common mode transient immunity at logic high	( $I_F = 0\text{ mA}$ , $ V_{CM}  = 10\text{ V}_{P-P}$ ) $T_A = 25^\circ\text{C}$ , ( $R_L = 2.2\text{ k}\Omega$ ) (Note 3) (Fig. 23)	$ICM_{HI}$	6N138 6N139	1,000	10,000		$\text{V}/\mu\text{s}$	
	Each Channel		HCPL-2730 HCPL-2731					
Common mode transient immunity at logic low	( $I_F = 1.6\text{ mA}$ , $ V_{CM}  = 10\text{ V}_{P-P}$ , $R_L = 2.2\text{ k}\Omega$ ) $T_A = 25^\circ\text{C}$ , (Note 3) (Fig. 23)	$ICM_{LI}$	6N138 6N139	1,000	10,000		$\text{V}/\mu\text{s}$	
	Each Channel		HCPL-2730 HCPL-2731					

\*\* All Typical at  $T_A = 25^\circ\text{C}$

**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

<b>ISOLATION CHARACTERISTICS</b> ( $T_A = 0$ to $70^\circ\text{C}$ Unless otherwise specified)						
<b>Characteristics</b>	<b>Test Conditions</b>	<b>Symbol</b>	<b>Min</b>	<b>Typ**</b>	<b>Max</b>	<b>Unit</b>
Input-output insulation leakage current	(Relative humidity = 45%) ( $T_A = 25^\circ\text{C}$ , $t = 5$ s) ( $V_{I-O} = 3000$ VDC) (Note 8)	$I_{I-O}$			1.0	$\mu\text{A}$
Withstand insulation test voltage	( $RH \leq 50\%$ , $T_A = 25^\circ\text{C}$ ) (Note 4) ( $t = 1$ min.)	$V_{ISO}$	2500			$V_{RMS}$
Resistance (input to output)	(Note 4) ( $V_{I-O} = 500$ VDC)	$R_{I-O}$		$10^{12}$		$\Omega$
Capacitance (input to output)	(Note 4, 5) ( $f = 1$ MHz)	$C_{I-O}$		0.6		pF
Input-Input Insulation leakage current	( $RH \leq 45\%$ , $V_{I-I} = 500$ VDC) (Note 6) $t = 5$ s, (HCPL-2730/2731 only)	$I_{I-I}$		0.005		$\mu\text{A}$
Input-Input Resistance	( $V_{I-I} = 500$ VDC) (Note 6) (HCPL-2730/2731 only)	$R_{I-I}$		$10^{11}$		$\Omega$
Input-Input Capacitance	( $f = 1$ MHz) (Note 6) (HCPL-2730/2731 only)	$C_{I-I}$		0.03		pF

\*\* All Typicals at  $T_A = 25^\circ\text{C}$

**Notes**

1. Current Transfer Ratio is defined as a ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%.
2. Pin 7 open. (6N138 and 6N139 only)
3. Common mode transient immunity in logic high level is the maximum tolerable (positive)  $dV_{cm}/dt$  on the leading edge of the common mode pulse signal  $V_{CM}$ , to assure that the output will remain in a logic high state (i.e.,  $V_O > 2.0$  V). Common mode transient immunity in logic low level is the maximum tolerable (negative)  $dV_{cm}/dt$  on the trailing edge of the common mode pulse signal,  $V_{CM}$ , to assure that the output will remain in a logic low state (i.e.,  $V_O < 0.8$  V).
4. Device is considered a two terminal device: Pins 1, 2, 3 and 4 are shorted together and Pins 5, 6, 7 and 8 are shorted together.
5. For dual channel devices,  $C_{I-O}$  is measured by shorting pins 1 and 2 or pins 3 and 4 together and pins 5 through 8 shorted together.
6. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise specified)

Current Limiting Resistor Calculations

$$R_1 \text{ (Non-Invert)} = \frac{V_{DD1} - V_{DF} - V_{OL1}}{I_F}$$

$$R_1 \text{ (Invert)} = \frac{V_{DD1} - V_{OH1} - V_{DF}}{I_F}$$

$$R_2 = \frac{V_{DD2} - V_{OLX} (@ I_L - I_2)}{I_L}$$

Where:

$V_{DD1}$  - Input Supply Voltage

$V_{DD2}$  - Output Supply Voltage

$V_{DF}$  - Diode Forward Voltage

$V_{OL1}$  - Logic "0" Voltage of Driver

$V_{OH1}$  - Logic "1" Voltage of Driver

$I_F$  - Diode Forward Current

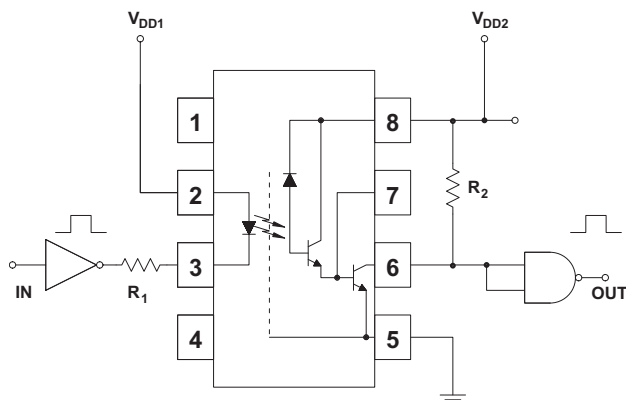
$V_{OLX}$  - Saturation Voltage of Output Transistor

$I_L$  - Load Current Through Resistor R2

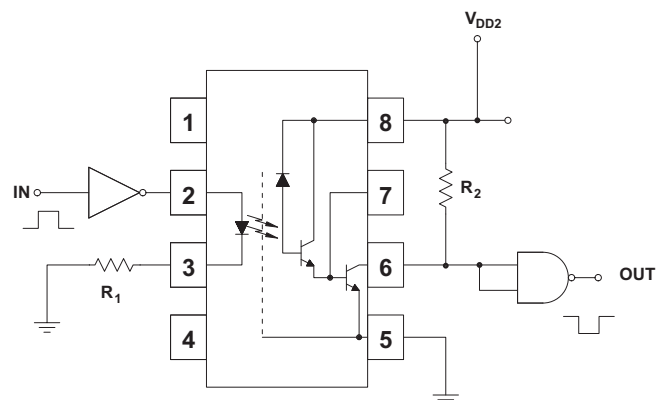
$I_2$  - Input Current of Output Gate

INPUT		R1 (V)	OUTPUT					
			CMOS @ 5 V	CMOS @ 10 V	74XX	74LXX	74SXX	74LSXX
			R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)	R2 (V)
CMOS @ 5 V	NON-INV.	2000	1000	2200	750	1000	1000	560
	INV.	510						
CMOS @ 10 V	NON-INV.	5100						
	INV.	4700						
74XX	NON-INV.	2200						
	INV.	180						
74LXX	NON-INV.	1800						
	INV.	100						
74SXX	NON-INV.	2000						
	INV.	360						
74LSXX	NON-INV.	2000						
	INV.	180						
74HXX	NON-INV.	2000						
	INV.	180						

**Fig. 1 Resistor Values for Logic Interface**



**Fig. 2 Non-Inverting Logic Interface**



**Fig. 3 Inverting Logic Interface**

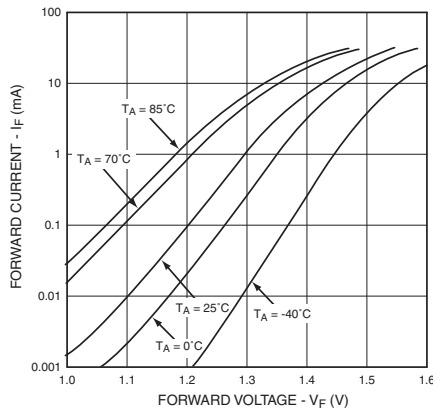
**SINGLE-CHANNEL: 6N138**

**6N139**

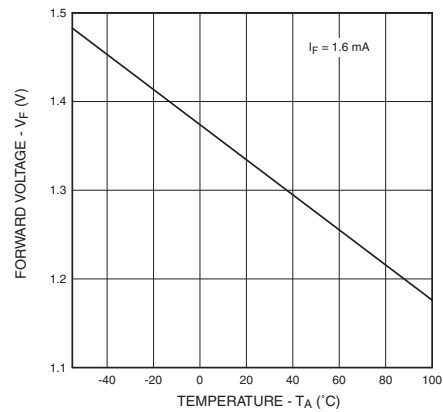
**DUAL-CHANNEL: HCPL-2730**

**HCPL-2731**

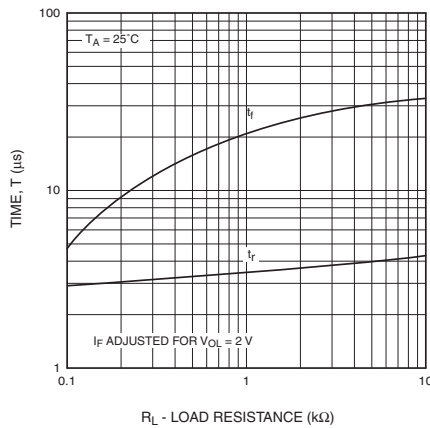
**Fig. 4 LED Forward Current vs. Forward Voltage**



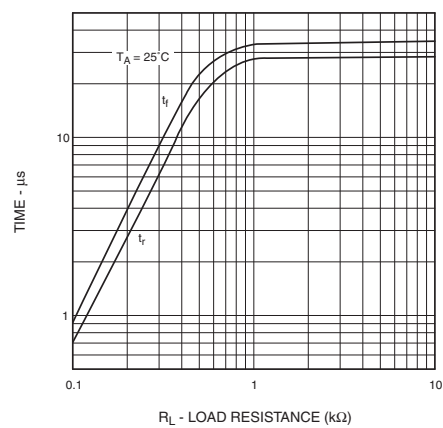
**Fig. 5 LED Forward Voltage vs. Temperature**



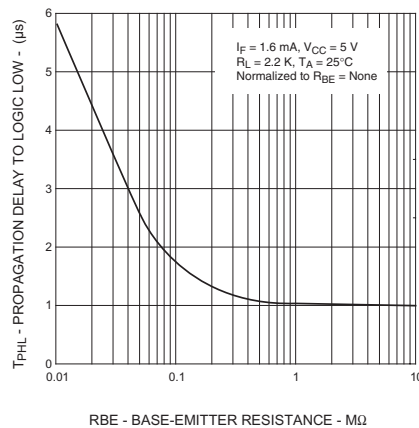
**Fig. 6 Non-saturated Rise and Fall Times vs. Load Resistance (6N138 / 6N139 Only)**



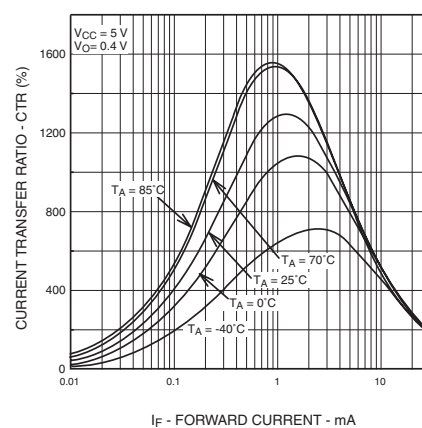
**Fig. 7 Non-saturated Rise and Fall Times vs. Load Resistance (HCPL-2730 / HCPL-2731 Only)**



**Fig. 8 Propagation Delay To Logic Low vs. Base-Emitter Resistance (HCPL-2730 / HCPL-2731 Only)**



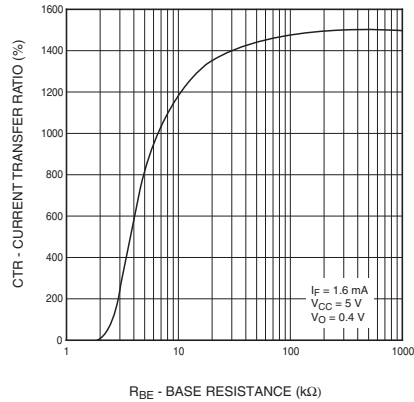
**Fig. 9 Current Transfer Ratio vs. Forward Current (6N138 / 6N139 Only)**



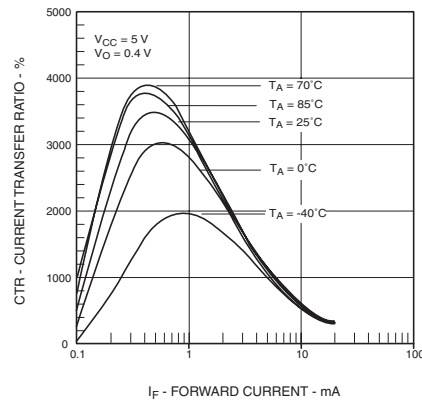
**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

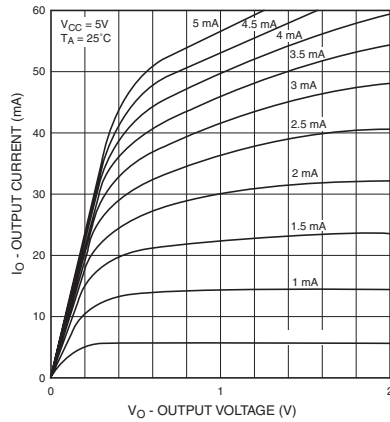
**Fig. 10 Current Transfer Ratio vs. Base-Emitter Resistance  
(6N138 / 6N139 Only)**



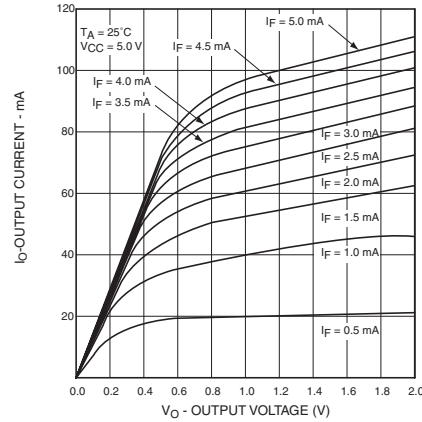
**Fig. 11 Current Transfer Ratio vs. Forward Current  
(HCPL-2730 / HCPL-2731 Only)**



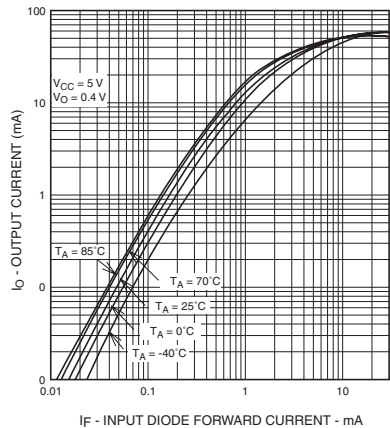
**Fig. 12 Output Current vs Output Voltage  
(6N138 / 6N139 Only)**



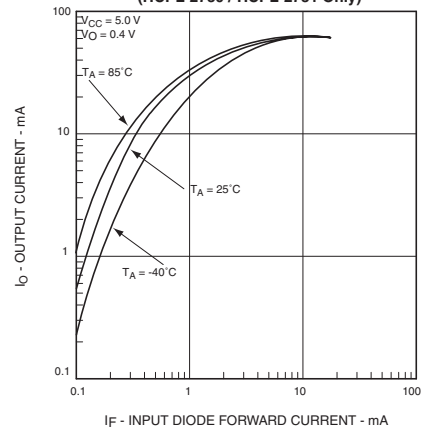
**Fig. 13 Output Current vs Output Voltage  
(HCPL-2730 / HCPL-2731 Only)**



**Fig. 14 Output Current vs. Input Diode Forward Current  
(6N138 / 6N139 Only)**



**Fig. 15 Output Current vs Input Diode Forward Current  
(HCPL-2730 / HCPL-2731 Only)**



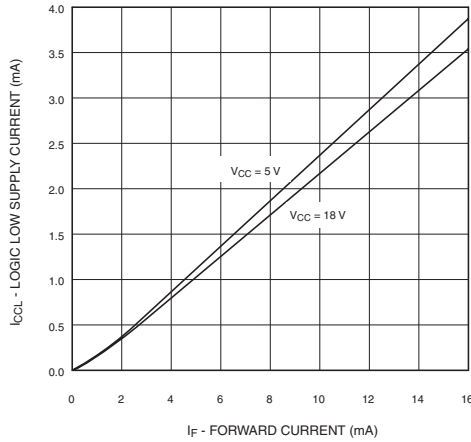
**SINGLE-CHANNEL: 6N138**

**6N139**

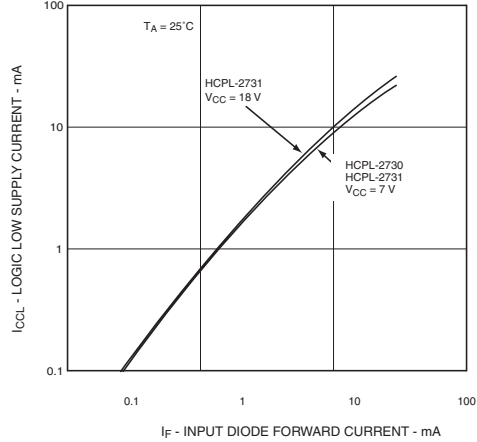
**DUAL-CHANNEL: HCPL-2730**

**HCPL-2731**

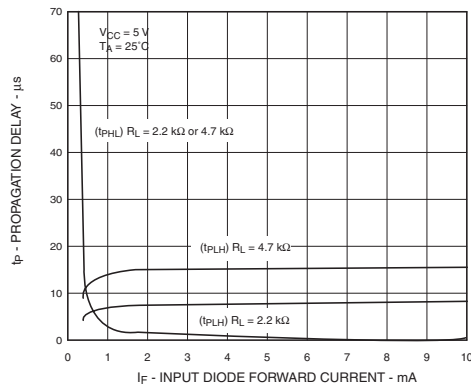
**Fig. 16 Logic Low Supply Current vs. Input Diode Forward Current (6N138 / 6N139 Only)**



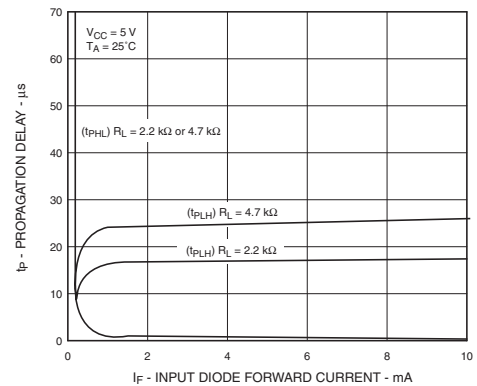
**Fig. 17 Logic Low Supply Current vs. Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)**



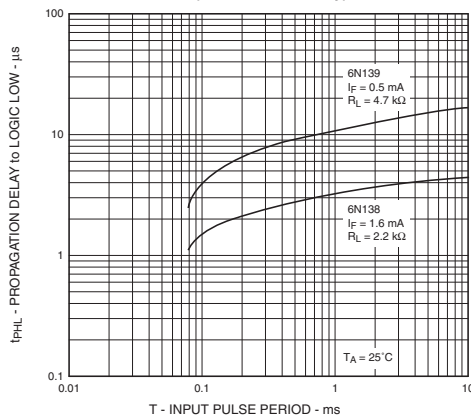
**Fig. 18 Propagation Delay vs. Input Diode Forward Current (6N138 / 6N139 Only)**



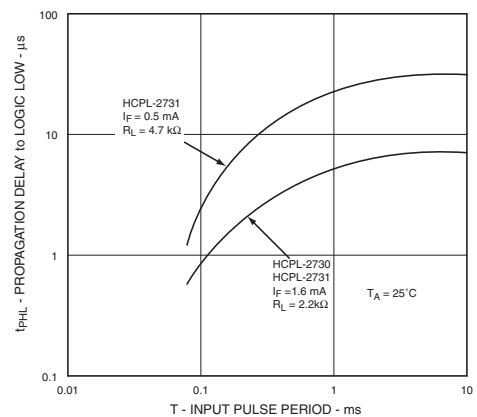
**Fig. 19 Propagation Delay vs. Input Diode Forward Current (HCPL-2730 / HCPL-2731 Only)**



**Fig. 20 Propagation Delay to Logic Low vs. Pulse Period (6N138 / 6N139 Only)**



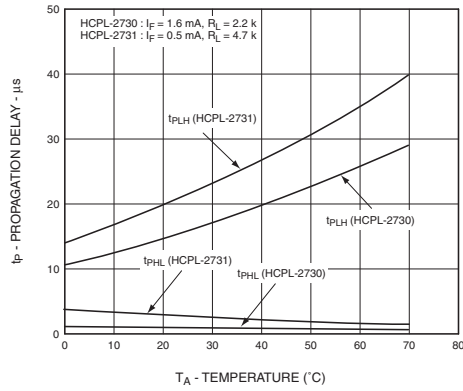
**Fig. 21 Propagation Delay to Logic Low vs. Pulse Period (HCPL-2730 / HCPL-2731 Only)**



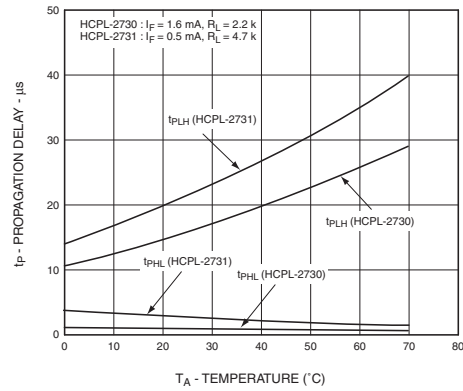
**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

**Fig. 22 Propagation Delay vs. Temperature  
(6N138 / 6N139 Only)**

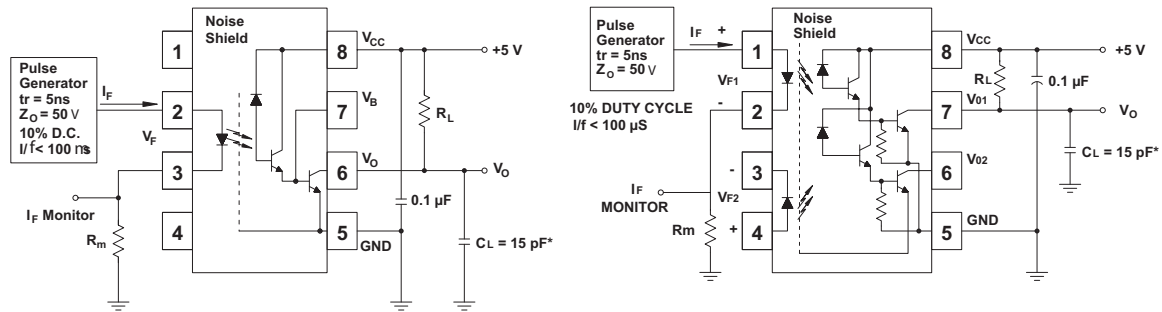


**Fig. 23 Propagation Delay vs. Temperature  
(HCPL-2730 / HCPL-2731 Only)**



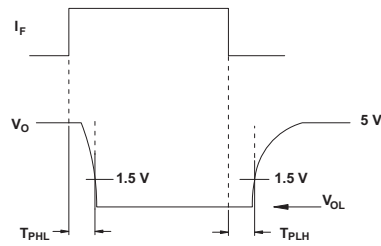
**SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730**

**6N139  
HCPL-2731**

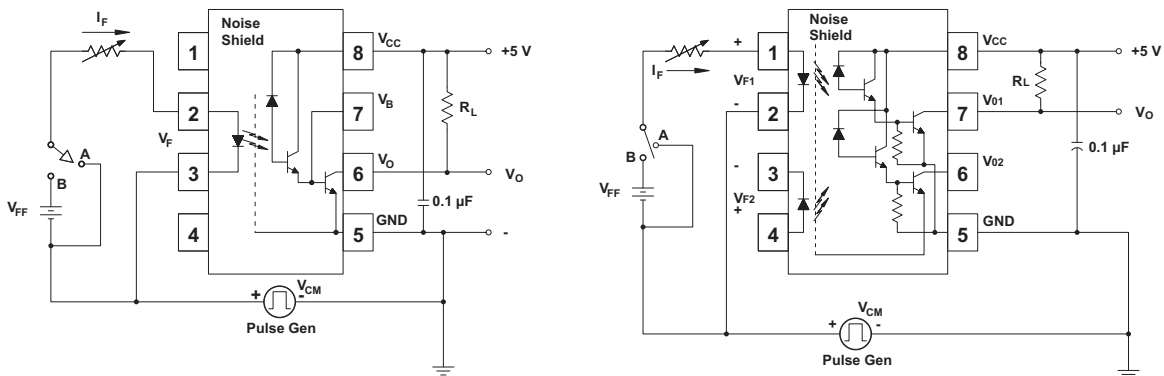


Test Circuit for 6N138, 6N139

Test Circuit for HCPL-2730 and HCPL-2731

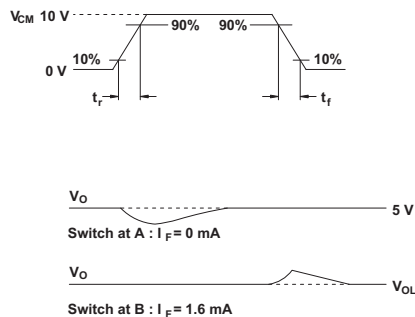


**Fig. 22 Switching Time Test Circuit**



Test Circuit for 6N138 and 6N139

Test Circuit for HCPL-2730 and HCPL-2731



**Fig. 23 Common Mode Immunity Test Circuit**



**SINGLE-CHANNEL: 6N138**

**6N139**

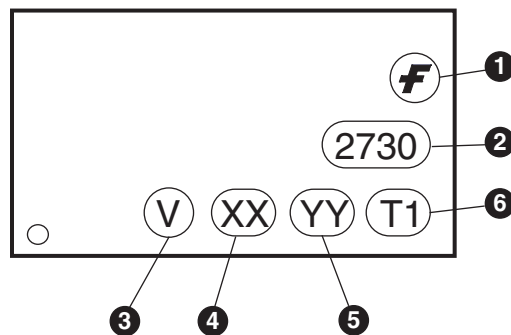
**DUAL-CHANNEL: HCPL-2730**

**HCPL-2731**

**ORDERING INFORMATION**

Option	Example Part Number	Description
S	6N138S	Surface Mount Lead Bend
SD	6N138SD	Surface Mount; Tape and reel
T	6N138T	0.4" Lead Spacing
V	6N138V	VDE0884
TV	6N138TV	VDE0884; 0.4" lead spacing
SV	6N138SV	VDE0884; surface mount
SDV	6N138SDV	VDE0884; surface mount; tape and reel

**MARKING INFORMATION**

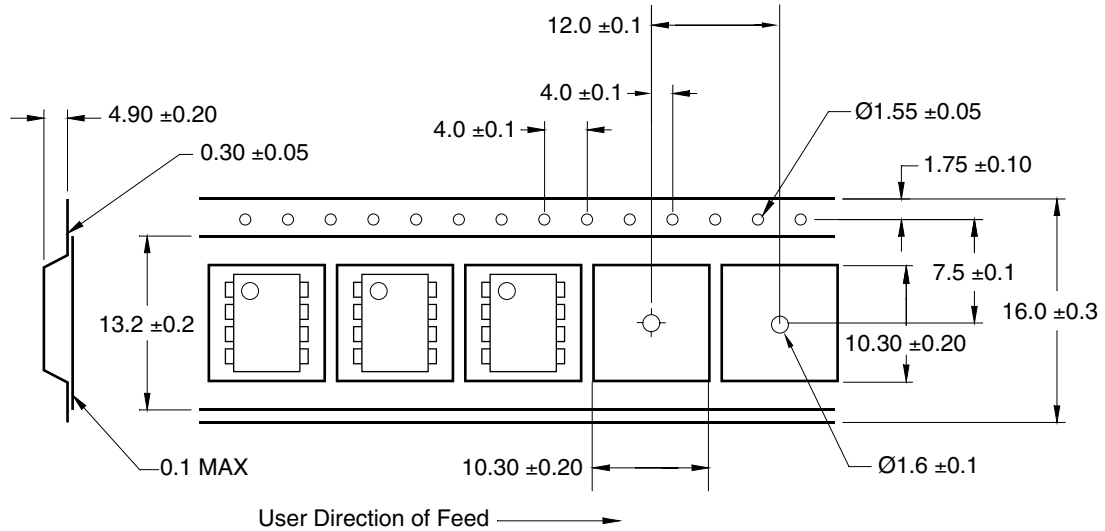


Definitions	
1	Fairchild logo
2	Device number
3	VDE mark (Note: Only appears on parts ordered with VDE option – See order entry table)
4	Two digit year code, e.g., '03'
5	Two digit work week ranging from '01' to '53'
6	Assembly package code

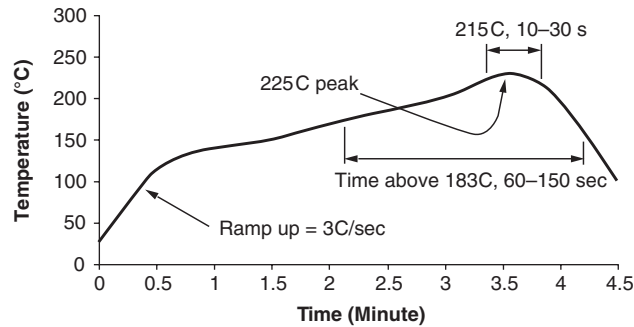
SINGLE-CHANNEL: 6N138  
DUAL-CHANNEL: HCPL-2730

6N139  
HCPL-2731

**Carrier Tape Specifications**



**Reflow Profile**



- Peak reflow temperature: 225C (package surface temperature)
- Time of temperature higher than 183C for 60-150 seconds
- One time soldering reflow is recommended

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**SINGLE-CHANNEL: 6N138**  
**DUAL-CHANNEL: HCPL-2730**

**6N139**  
**HCPL-2731**

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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