THE DATASHEET OF

AD8328ARQ

5 V Upstream Cable Line Driver

AD8328

FEATURES

- Supports DOCSIS and EuroDOCSIS standards for reverse path transmission systems
- Gain programmable in 1 dB steps over a 59 dB range
- Low distortion at 60 dBmV output
  - −57.5 dBc SFDR at 21 MHz
  - −54 dBc SFDR at 65 MHz
- Output noise level @ minimum gain 1.2 nV/√Hz
- Maintains 300 Ω output impedance Tx-enable and Tx-disable condition
- Upper bandwidth: 107 MHz (full gain range)
- 5 V supply operation
- Supports SPI interfaces

APPLICATIONS

- DOCSIS and EuroDOCSIS cable modems
- CATV set-top boxes
- CATV telephony modems
- Coaxial and twisted pair line drivers

FUNCTIONAL BLOCK DIAGRAM

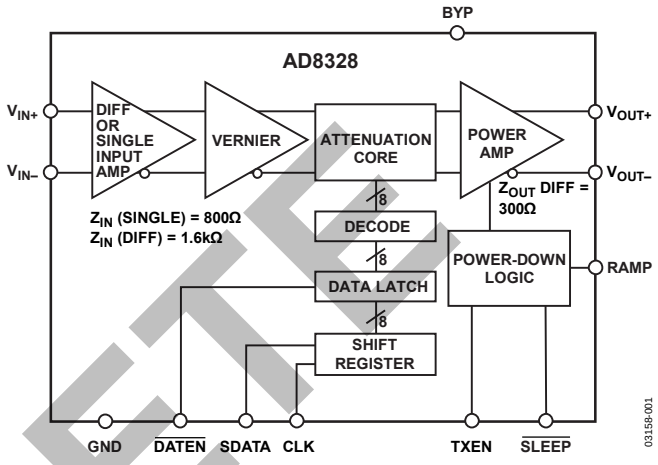

Figure 1.

GENERAL DESCRIPTION

The AD8328 is a low cost amplifier designed for coaxial line driving. The features and specifications make the AD8328 ideally suited for MCNS-DOCSIS and EuroDOCSIS applications. The gain of the AD8328 is digitally controlled. An 8-bit serial word determines the desired output gain over a 59 dB range, resulting in gain changes of 1 dB/LSB.

The AD8328 accepts a differential or single-ended input signal. The output is specified for driving a 75 Ω load through a 2:1 transformer.

Distortion performance of −53 dBc is achieved with an output level up to 60 dBmV at 65 MHz bandwidth over a wide temperature range.

This device has a sleep mode function that reduces the quiescent current to 2.6 mA and a full power-down function that reduces power-down current to 20 µA.

The AD8328 is packaged in a low cost 20-lead LFCSP and a 20-lead QSOP. The AD8328 operates from a single 5 V supply and has an operational temperature range of −40°C to +85°C.

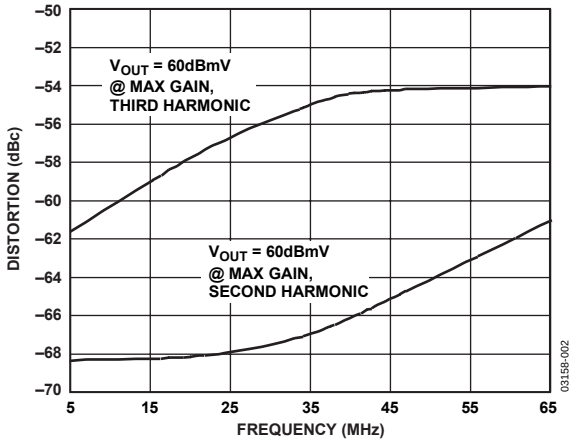

Figure 2. Worst Harmonic Distortion vs. Frequency

Rev. A

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REVISION HISTORY

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11/02—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 5 V, R_L = R_{IN} = 75 Ω, V_{IN} (differential) = 29 dBmV. The AD8328 is characterized using a 2:1 transformer[1] at the device output.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS					
Specified AC Voltage	Output = 60 dBmV, max gain		29		dBmV
Input Resistance	Single-ended input		800		Ω
	Differential input		1600		Ω
Input Capacitance			2		pF
GAIN CONTROL INTERFACE					
Voltage Gain Range		58	59.0	60	dB
Maximum Gain	Gain code = 60 decimal codes	30.5	31.5	32.5	dB
Minimum Gain	Gain code = 1 decimal code	−28.5	−27.5	−26.5	dB
Output Step Size		0.6	1.0	1.4	dB/LSB
Output Step Size Temperature Coefficient	T_A = −40°C to +85°C		±0.0005		dB/°C
OUTPUT CHARACTERISTICS					
Bandwidth (−3 dB)	All gain codes (1 to 60 decimal codes)		107		MHz
Bandwidth Roll-Off	f = 65 MHz		1.2		dB
1 dB Compression Point[2]	Maximum gain, f = 10 MHz, output referred	17.9	18.4		dBm
	Minimum gain, f = 10 MHz, input referred	2.2	3.3		dBm
Output Noise[2]					
Maximum Gain	f = 10 MHz		135	151	nV/√Hz
Minimum Gain	f = 10 MHz		1.2	1.3	nV/√Hz
Tx Disable	f = 10 MHz		1.1	1.2	nV/√Hz
Noise Figure[2]					
Maximum Gain	f = 10 MHz		16.7	17.7	dB
Differential Output Impedance	Tx enable and Tx disable		75 ± 30%[3]		Ω
OVERALL PERFORMANCE					
Second-Order Harmonic Distortion[4, 5]					
	f = 33 MHz, V_{OUT} = 60 dBmV @ maximum gain		−67	−56	dBc
	f = 65 MHz, V_{OUT} = 60 dBmV @ maximum gain		−61	−55	dBc
Third-Order Harmonic Distortion[4, 5]	f = 21 MHz, V_{OUT} = 60 dBmV @ maximum gain		−57.5	−56	dBc
	f = 65 MHz, V_{OUT} = 60 dBmV @ maximum gain		−54	−52.5	dBc
ACPR[2, 6]			−58	−56	dBc
Isolation (Tx Disable)[2]	Maximum gain, f = 65 MHz		−85	−81	dB
POWER CONTROL					
Tx Enable Settling Time	Maximum gain, V_{IN} = 0		2.5		µs
Tx Disable Settling Time	Maximum gain, V_{IN} = 0		3.8		µs
Output Switching Transients[2]	Equivalent output = 31 dBmV		2.5	6	mV p-p
	Equivalent output = 61 dBmV		16	54	mV p-p
Output Settling					
Due to Gain Change	Minimum to maximum gain		60		ns
Due to Input Step Change	Maximum gain, V_{IN} = 29 dBmV		30		ns
POWER SUPPLY					
Operating Range		4.75	5	5.25	V
Quiescent Current	Maximum gain	98	120	140	mA
	Minimum gain	18	26	34	mA
	Tx disable (TXEN = 0)	1	2.6	3.5	mA
	$\overline{\text{SLEEP}}$ mode (power-down)	1	20	100	µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

[1] TOKO 458 PT-1087 used for above specifications. Typical insertion loss of 0.3 dB @ 10 MHz.
[2] Guaranteed by design and characterization to ±4 sigma for T_A = 25°C.
[3] Measured through a 2:1 transformer.
[4] Specification is worst case over all gain codes.
[5] Guaranteed by design and characterization to ±3 sigma for T_A = 25°C.
[6] V_{IN} = 29 dBmV, QPSK modulation, 160 kSPS symbol rate.

LOGIC INPUTS (TTL-/CMOS-COMPATIBLE LOGIC)

$\overline{\text{DATEN}}$, CLK, SDATA, TXEN, $\overline{\text{SLEEP}}$, V_{CC} = 5 V; full temperature range.

Table 2.

Parameter	Min	Typ	Max	Unit
Logic 1 Voltage	2.1		5.0	V
Logic 0 Voltage	0		0.8	V
Logic 1 Current (V_{INH} = 5 V) CLK, SDATA, $\overline{\text{DATEN}}$	0		20	nA
Logic 0 Current (V_{INL} = 0 V) CLK, SDATA, $\overline{\text{DATEN}}$	−600		−100	nA
Logic 1 Current (V_{INH} = 5 V) TXEN	50		190	µA
Logic 0 Current (V_{INL} = 0 V) TXEN	−250		−30	µA
Logic 1 Current (V_{INH} = 5 V) $\overline{\text{SLEEP}}$	50		190	µA
Logic 0 Current (V_{INL} = 0 V) $\overline{\text{SLEEP}}$	−250		−30	µA

TIMING REQUIREMENTS

Full temperature range, V_{CC} = 5 V, $t_R = t_F$ = 4 ns, f_{CLK} = 8 MHz, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit
Clock Pulse Width (t_{WH})	16.0			ns
Clock Period (t_C)	32.0			ns
Setup Time SDATA vs. Clock (t_{DS})	5.0			ns
Setup Time $\overline{\text{DATEN}}$ vs. Clock (t_{ES})	15.0			ns
Hold Time SDATA vs. Clock (t_{DH})	5.0			ns
Hold Time $\overline{\text{DATEN}}$ vs. Clock (t_{EH})	3.0			ns
Input Rise and Fall Times, SDATA, $\overline{\text{DATEN}}$, Clock (t_R, t_F)			10	ns

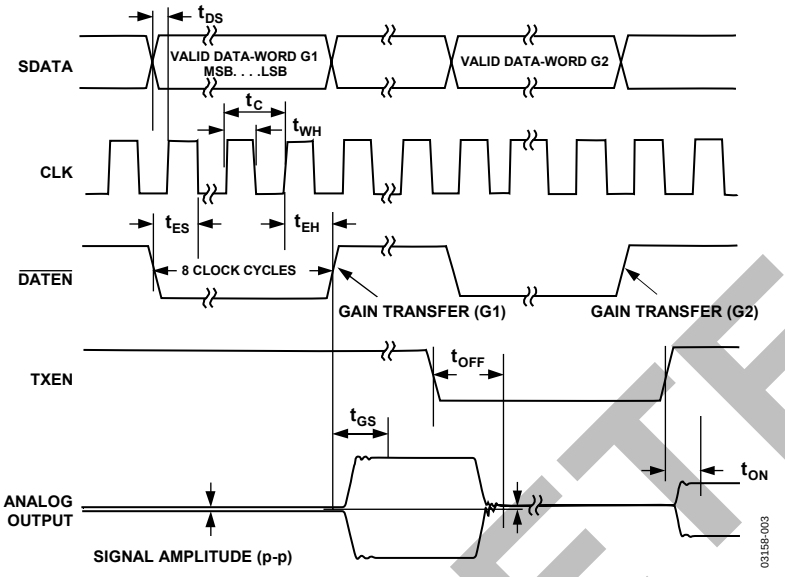


Figure 3. Serial Interface Timing

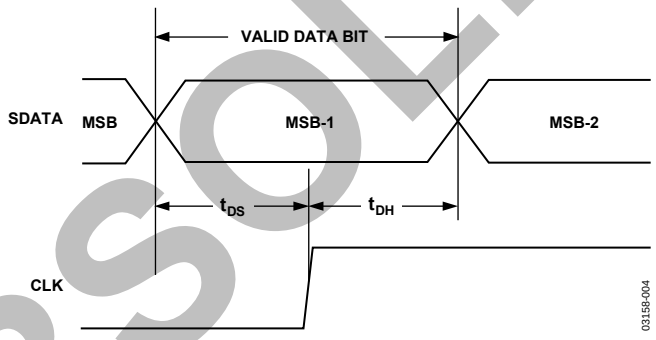


Figure 4. SDATA Timing

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage V_{CC}	6 V
Input Voltage	
V_{IN+}, V_{IN-}	1.5 V p-p
$\overline{DATEN}$, SDATA, CLK, $\overline{SLEEP}$, TXEN	−0.8 V to +5.5 V
Internal Power Dissipation	
QSOP (θ_{JA} = 83.2°C/W)[1]	700 mW
LFCSP (θ_{JA} = 30.4°C/W)[2]	700 mW
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature, Soldering 60 sec	300°C

[1] Thermal resistance measured on SEMI standard 4-layer board.
[2] Thermal resistance measured on SEMI standard 4-layer board, paddle soldered to board.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

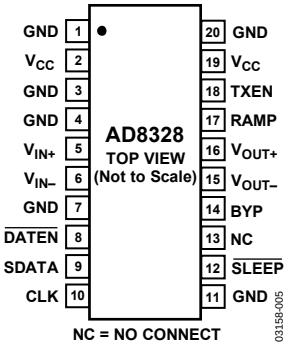


Figure 5. 20-Lead QSOP Pin Configuration

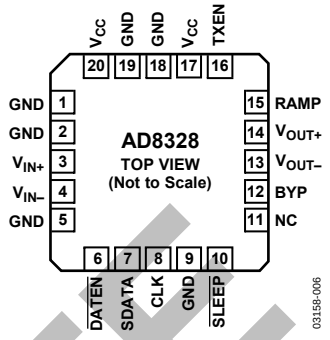


Figure 6. 20-Lead LFCSP Pin Configuration

Table 5. 20-Lead QSOP and 20-Lead LFCSP Pin Function Descriptions

Pin No. 20-Lead QSOP	Pin No. 20-Lead LFCSP	Mnemonic	Description
1, 3, 4, 7, 11, 20	1, 2, 5, 9, 18, 19	GND	Common External Ground Reference.
2, 19	17, 20	V_{CC}	Common Positive External Supply Voltage. A 0.1 µF capacitor must decouple each pin.
5	3	V_{IN+}	Noninverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
6	4	V_{IN-}	Inverting Input. DC-biased to approximately $V_{CC}/2$. Should be ac-coupled with a 0.1 µF capacitor.
8	6	$\overline{\text{DATEN}}$	Data Enable Low Input. This port controls the 8-bit parallel data latch and shift register. A Logic 0-to-Logic 1 transition transfers the latched data to the attenuator core (updates the gain) and simultaneously inhibits serial data transfer into the register. A Logic 1-to-Logic 0 transition inhibits the data latch (holds the previous gain state) and simultaneously enables the register for serial data load.
9	7	SDATA	Serial Data Input. This digital input allows an 8-bit serial (gain) word to be loaded into the internal register with the most significant bit (MSB) first.
10	8	CLK	Clock Input. The clock port controls the serial attenuator data transfer rate to the 8-bit master-slave register. A Logic 0-to-Logic 1 transition latches the data bit, and a Logic 1-to-Logic 0 transfers the data bit to the slave. This requires the input serial data-word to be valid at or before this clock transition.
12	10	$\overline{\text{SLEEP}}$	Low Power Sleep Mode. In the sleep mode, the AD8328's supply current is reduced to 20 µA. A Logic 0 powers down the part (high Z_{OUT} state), and a Logic 1 powers up the part.
13	11	NC	No Connect.
14	12	BYP	Internal Bypass. This pin must be externally ac-coupled (0.1 µF capacitor).
15	13	V_{OUT-}	Negative Output Signal
16	14	V_{OUT+}	Positive Output Signal
17	15	RAMP	External RAMP Capacitor (Optional)
18	16	TXEN	Logic 0 Disables Forward Transmission. Logic 1 enables forward transmission.

TYPICAL PERFORMANCE CHARACTERISTICS

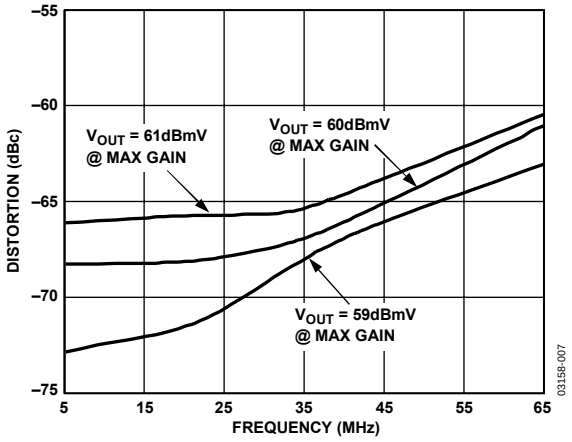


Figure 7. Second-Order Harmonic Distortion vs. Frequency for Various Output Powers

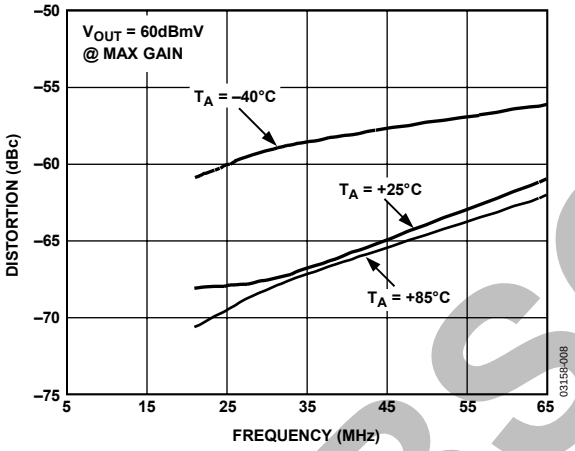


Figure 8. Second-Order Harmonic Distortion vs. Frequency vs. Temperature

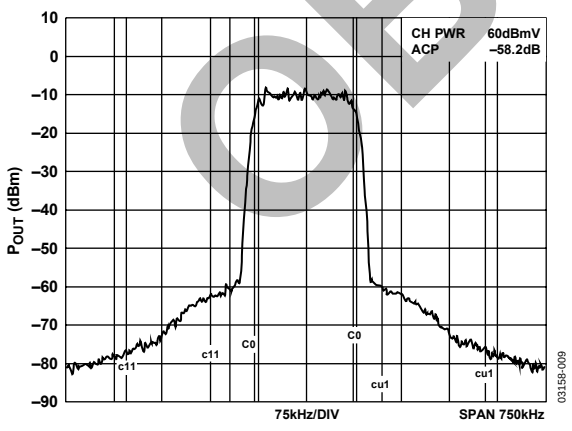


Figure 9. Adjacent Channel Power

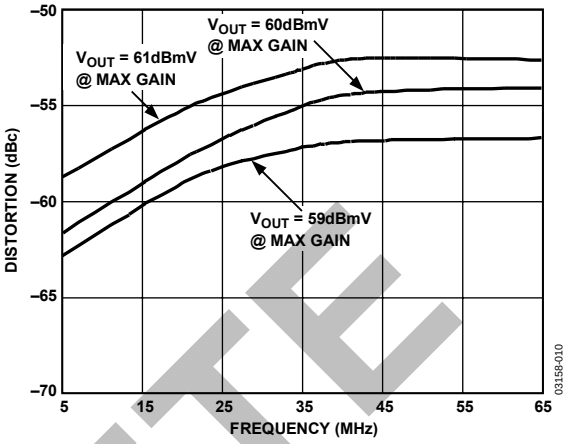


Figure 10. Third-Order Harmonic Distortion vs. Frequency for Various Output Powers

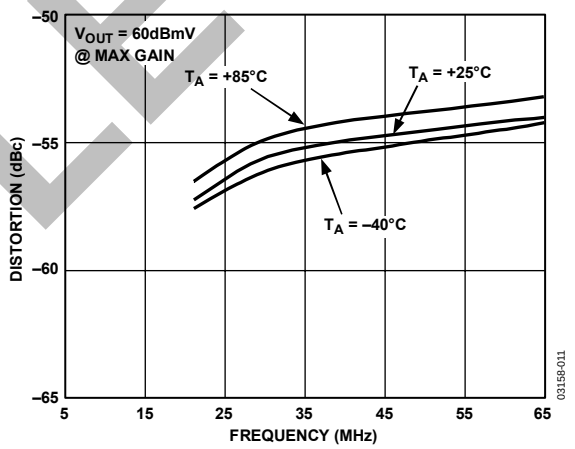


Figure 11. Third-Order Harmonic Distortion vs. Frequency vs. Temperature

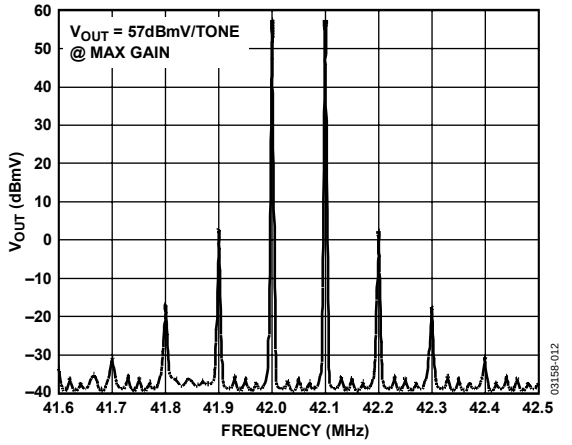


Figure 12. Two-Tone Intermodulation Distortion

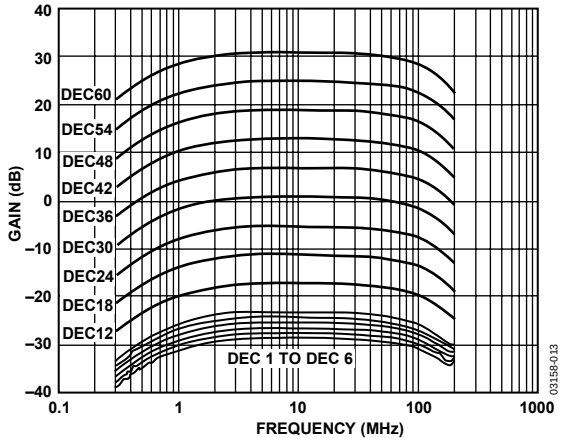


Figure 13. AC Response

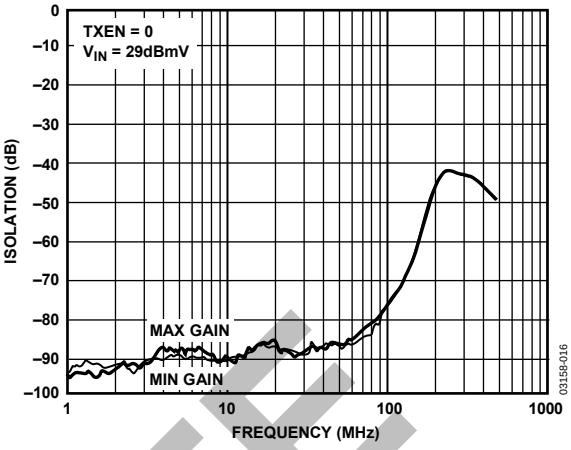


Figure 16. Isolation in Transmit Disable Mode vs. Frequency

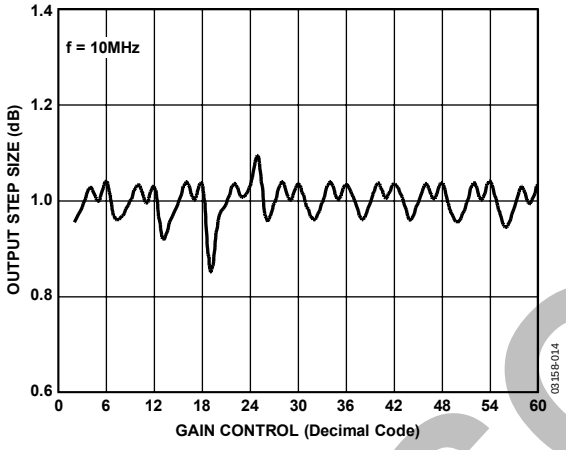


Figure 14. Output Step Size vs. Gain Control

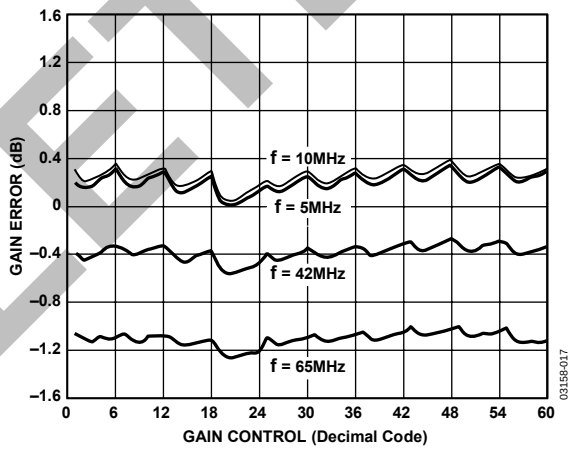


Figure 17. Gain Error vs. Gain Control

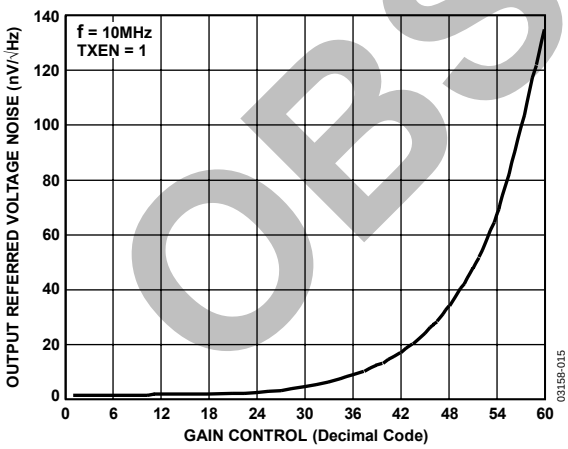


Figure 15. Output Referred Voltage Noise vs. Gain Control

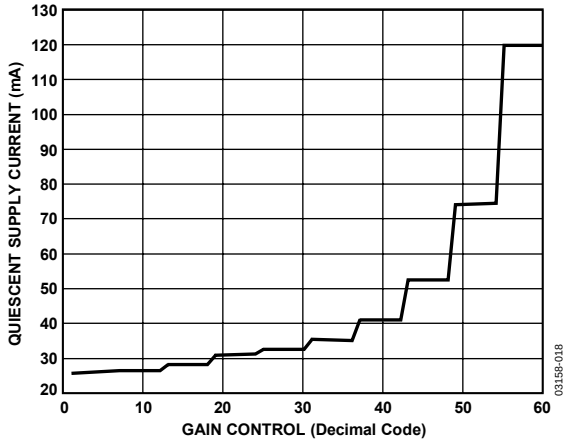


Figure 18. Supply Current vs. Gain Control

APPLICATIONS

GENERAL APPLICATIONS

The AD8328 is primarily intended for use as the power amplifier (PA) in Data Over Cable Service Interface Specification (DOCSIS)-certified cable modems and CATV set-top boxes. The upstream signal is either a QPSK or QAM signal generated by a DSP, a dedicated QPSK/QAM modulator, or a DAC. In all cases, the signal must be low-pass filtered before being applied to the PA to filter out-of-band noise and higher order harmonics from the amplified signal.

Due to the varying distances between the cable modem and the head-end, the upstream PA must be capable of varying the output power by applying gain or attenuation. The ability to vary the output power of the AD8328 ensures that the signal from the cable modem has the proper level once it arrives at the head-end. The upstream signal path commonly includes a diplexer and cable splitters. The AD8328 has been designed to overcome losses associated with these passive components in the upstream cable path.

CIRCUIT DESCRIPTION

The AD8328 is composed of three analog functions in the power-up or forward mode. The input amplifier (preamp) can be used single-ended or differentially. If the input is used in the differential configuration, it is imperative that the input signals be 180° out of phase and of equal amplitude. A vernier is used in the input stage for controlling the fine 1 dB gain steps. This stage then drives a DAC, which provides the bulk of the AD8328's attenuation. The signals in the preamp and DAC gain blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC into the output stage. The output stage maintains 300 Ω differential output impedance, which maintains proper match to 75 Ω when used with a 2:1 balun transformer.

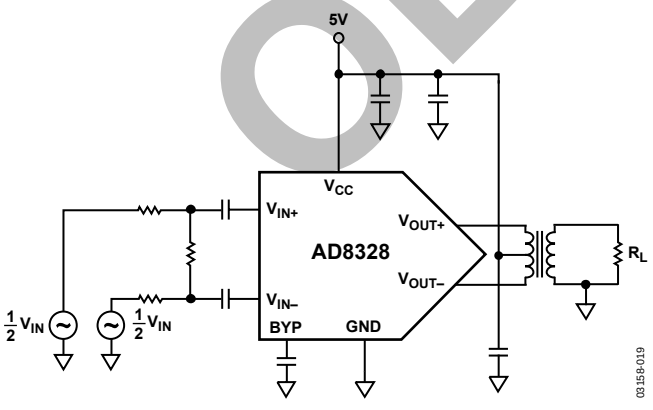


Figure 19. Characterization Circuit

SPI PROGRAMMING AND GAIN ADJUSTMENT

The AD8328 is controlled through a serial peripheral interface (SPI) of three digital data lines: CLK, $\overline{\text{DATEN}}$, and SDATA. Changing the gain requires eight bits of data to be streamed into the SDATA port. The sequence of loading the SDATA register begins on the falling edge of the $\overline{\text{DATEN}}$ pin, which activates the CLK line. With the CLK line activated, data on the SDATA line is clocked into the serial shift register on the rising edge of the CLK pulses, MSB first. The 8-bit data-word is latched into the attenuator core on the rising edge of the $\overline{\text{DATEN}}$ line. This provides control over the changes in the output signal level. The serial interface timing for the AD8328 is shown in Figure 3 and Figure 4. The programmable gain range of the AD8328 is −28 dB to +31 dB with steps of 1 dB per least significant bit (LSB). This provides a total gain range of 59 dB. The AD8328 was characterized with a differential signal on the input and a TOKO 458PT-1087 2:1 transformer on the output. The AD8328 incorporates supply current scaling with gain code, as shown in Figure 18. This allows reduced power consumption when operating in lower gain codes.

INPUT BIAS, IMPEDANCE, AND TERMINATION

The V_{IN+} and V_{IN-} inputs have a dc bias level of $V_{CC}/2$; therefore, the input signal should be ac-coupled as shown in Figure 20. The differential input impedance of the AD8328 is approximately 1.6 kΩ, while the single-ended input is 800 Ω. The high input impedance of the AD8328 allows flexibility in termination and properly matching filter networks. The AD8328 exhibits optimum performance when driven with a pure differential signal.

OUTPUT BIAS, IMPEDANCE, AND TERMINATION

The output stage of the AD8328 requires a bias of 5 V. The 5 V power supply should be connected to the center tap of the output transformer. In addition, the V_{CC} applied to the center tap of the transformer should be decoupled as seen in Figure 20.

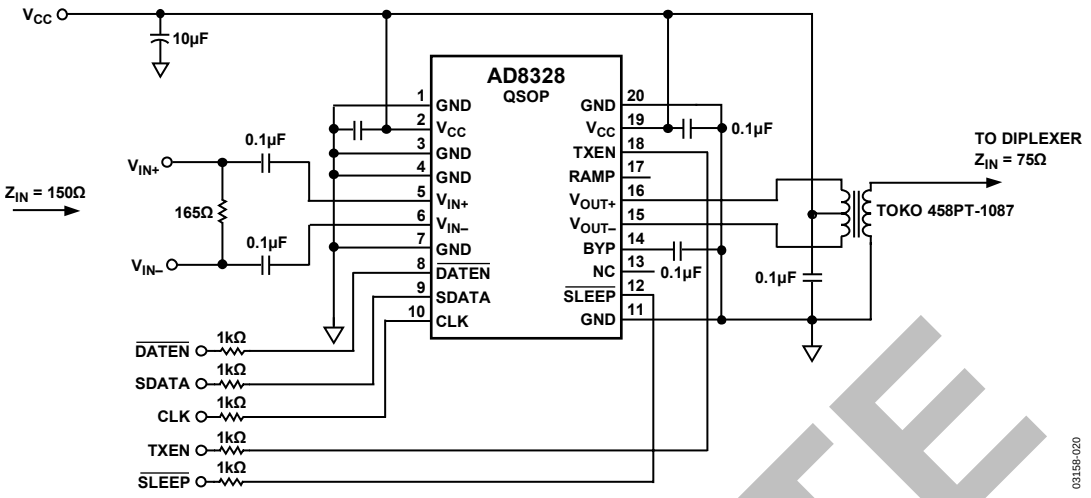


Figure 20. Typical Application Circuit

Table 6. Adjacent Channel Power

	Adjacent Channel Symbol Rate (kSym/s)					
Channel Symbol Rate (kSym/s)	**160**	**320**	**640**	**1280**	**2560**	**5120**
160	−58	−60	−63	−66	−66	−64
320	−58	−59	−60	−64	−66	−65
640	−60	−58	−59	−61	−64	−65
1280	−62	−60	−59	−60	−61	−63
2560	−64	−62	−60	−59	−60	−61
5120	−66	−65	−62	−61	−59	−60

The output impedance of the AD8328 is 300 Ω, regardless of whether the amplifier is in transmit enable or transmit disable mode. This, when combined with a 2:1 voltage ratio (4:1 impedance ratio) transformer, eliminates the need for external back termination resistors. If the output signal is being evaluated using standard 50 Ω test equipment, a minimum loss 75 Ω to 50 Ω pad must be used to provide the test circuit with the proper impedance match. The AD8328 evaluation board provides a convenient means to implement a matching attenuator. Soldering a 43.3 Ω resistor in the R15 placeholder and an 86.6 Ω resistor in the R16 placeholder allows testing on a 50 Ω system. When using a matching attenuator, it should be noted that there is a 5.7 dB of power loss (7.5 dB voltage) through the network.

POWER SUPPLY

The 5 V supply should be delivered to each of the V_{CC} pins via a low impedance power bus to ensure that each pin is at the same potential. The power bus should be decoupled to ground using a 10 µF tantalum capacitor located close to the AD8328. In addition to the 10 µF capacitor, each V_{CC} pin should be individually decoupled to ground with ceramic chip capacitors located close to the pins. The bypass pin, BYP, should also be decoupled. The PCB should have a low impedance ground plane covering all unused portions of the board, except in areas of the board where input and output traces are in close proximity to the AD8328 and the output transformer. All AD8328 ground pins must be connected to the ground plane to ensure proper grounding of all internal nodes.

SIGNAL INTEGRITY LAYOUT CONSIDERATIONS

Careful attention to printed circuit board layout details will prevent problems due to board parasitics. Proper RF design techniques are mandatory. The differential input and output traces should be kept as short as possible. Keeping the traces short minimizes parasitic capacitance and inductance. This is most critical between the outputs of the AD8328 and the 2:1 output transformer. It is also critical that all differential signal paths be symmetrical in length and width. In addition, the input and output traces should be adequately spaced to minimize coupling (crosstalk) through the board. Following these guidelines optimizes the overall performance of the AD8328 in all applications.

INITIAL POWER-UP

When the supply voltage is first applied to the AD8328, the gain of the amplifier is initially set to Gain Code 1. Since power is first applied to the amplifier, the TXEN pin should be held low (Logic 0) to prevent forward signal transmission. After power is applied to the amplifier, the gain can be set to the desired level by following the procedure provided in the SPI Programming and Gain Adjustment section. The TXEN pin can then be brought from Logic 0 to Logic 1, enabling forward signal transmission at the desired gain level.

RAMP PIN AND BYP PIN FEATURES

The RAMP pin is used to control the length of the burst on and off transients. By default, leaving the RAMP pin unconnected results in a transient that is fully compliant with DOCSIS 2.0 Section 6.2.21.2, *Spurious Emissions During Burst On/Off Transients*. DOCSIS requires that all between-burst transients must be dissipated no faster than 2 µs; and adding capacitance to the RAMP pin adds more time to the transient.

The BYP pin is used to decouple the output stage at midsupply. Typically, for normal DOCSIS operation, the BYP pin should be decoupled to ground with a 0.1 µF capacitor. However, in applications that require transient on/off times faster than 2 µs, smaller capacitors can be used, but it should be noted that the BYP pin should always be decoupled to ground.

TRANSMIT ENABLE (TXEN) AND $\overline{\text{SLEEP}}$

The asynchronous TXEN pin is used to place the AD8328 into between-burst mode. In this reduced current state, the output impedance of 75 Ω is maintained. Applying Logic 0 to the TXEN pin deactivates the on-chip amplifier, providing a 97.8% reduction in consumed power. For 5 V operation, the supply current is typically reduced from 120 mA to 2.6 mA. In this mode of operation, between-burst noise is minimized and high input to output isolation is achieved. In addition to the TXEN pin, the AD8328 also incorporates an asynchronous $\overline{\text{SLEEP}}$ pin, which can be used to further reduce the supply current to approximately 20 µA. Applying Logic 0 to the $\overline{\text{SLEEP}}$ pin places the amplifier into $\overline{\text{SLEEP}}$ mode. Transitioning into or out of $\overline{\text{SLEEP}}$ mode can result in a transient voltage at the output of the amplifier.

DISTORTION, ADJACENT CHANNEL POWER, AND DOCSIS

To deliver the DOCSIS required 58 dBmV of QPSK signal and 55 dBmV of 16 QAM signal, the PA is required to deliver up to 60 dBmV. This added power is required to compensate for losses associated with the diplex filter or other passive components that may be included in the upstream path of cable modems or set-top boxes. It should be noted that the AD8328 was characterized with a differential input signal. Figure 7 and Figure 10 show the AD8328 second and third harmonic distortion performance vs. the fundamental frequency for various output power levels. These figures are useful for determining the in-band harmonic levels from 5 MHz to 65 MHz. Harmonics higher in frequency (above 42 MHz for DOCSIS and above 65 MHz for EuroDOCSIS) are sharply attenuated by the low-pass filter function of the diplexer.

Another measure of signal integrity is adjacent channel power, commonly referred to as ACP. DOCSIS 2.0, Section 6.2.21.1.1 states, "Spurious emissions from a transmitted carrier may occur in an adjacent channel that could be occupied by a carrier of the same or different symbol rates." Figure 9 shows the measured ACP for a 60 dBmV QPSK signal taken at the output of the AD8328 evaluation board. The transmit channel width and adjacent channel width in Figure 9 correspond to the symbol rates of 160 kSym/s. Table 6 shows the ACP results for the AD8328 driving a QPSK 60 dBmV signal for all conditions in DOCSIS Table 6-9, *Adjacent Channel Spurious Emissions*.

NOISE AND DOCSIS

At minimum gain, the AD8328 output noise spectral density is 1.2 nV/√Hz measured at 10 MHz. DOCSIS Table 6-10, *Spurious Emissions in 5 MHz to 42 MHz*, specifies the output noise for various symbol rates. The calculated noise power in dBmV for 160 kSym/s is

$$\left[20\times\log\left(\sqrt{\left(\frac{1.2\text{ nV}}{\sqrt{\text{Hz}}}\right)^2\times 160\text{ kHz}}\right)\right]+60=-66.4\text{ dBmV} \quad (1)$$

Comparing the computed noise power of −66.4 dBmV to the +8 dBmV signal yields −74.4 dBc, which meets the required level set forth in DOCSIS Table 6-10. As the AD8328 gain is increased above this minimum value, the output signal increases at a faster rate than the noise, resulting in a signal-to-noise ratio that improves with gain. In transmit disable mode, the output noise spectral density is 1.1 nV/√Hz, which results in −67 dBmV when computed over 160 kSym/s. The noise power was measured directly at the output of the AD8328AR-EVAL board.

EVALUATION BOARD FEATURES AND OPERATION

The AD8328 evaluation board and control software can be used to control the AD8328 upstream cable driver via the parallel port of a PC. A standard printer cable connected to the parallel port of the PC is used to feed all the necessary data to the AD8328 using the Windows®-based control software. This package provides a means of controlling the gain and the power mode of the AD8328. With this evaluation kit, the AD8328 can be evaluated in either a single-ended or differential input configuration. See Figure 26 for a schematic of the evaluation board.

DIFFERENTIAL SIGNAL SOURCE

Typical applications for the AD8328 use a differential input signal from a modulator or a DAC. See Table 7 for common values of R4, or calculate other input configurations using Equation 2. This circuit configuration will give optimal distortion results due to the symmetric input signals. Note that this configuration was used to characterize the AD8328.

$$R4 = \frac{Z_{IN} \times 1.6\ \text{k}\Omega}{1.6\ \text{k}\Omega - Z_{IN}} \quad (2)$$

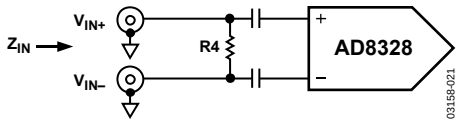


Figure 21. Differential Circuit

DIFFERENTIAL SIGNAL FROM SINGLE-ENDED SOURCE

The default configuration of the evaluation board implements a differential signal drive from a single-ended signal source. This configuration uses a 1:1 balun transformer to approximate a differential signal. Because of the nonideal nature of real transformers, the differential signal is not purely equal and opposite in amplitude. Although this circuit slightly sacrifices even-order harmonic distortion due to asymmetry, it does provide a convenient way to evaluate the AD8328 with a single-ended source.

The AD8328 evaluation board is populated with a TOKO 617DB-A0070 1:1 for this purpose (T1). Table 7 provides typical R4 values for common input configurations. Other input impedances can be calculated using Equation 3. See Figure 26 for a schematic of the evaluation board. To use the transformer for converting a single-ended source into a differential signal, the input signal must be applied to V_{IN+}.

$$R4 = \frac{Z_{IN} \times 1.6\ \text{k}\Omega}{1.6\ \text{k}\Omega - Z_{IN}} \quad (3)$$

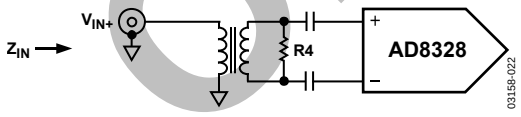


Figure 22. Single-to-Differential Circuit

SINGLE-ENDED SOURCE

Although the AD8328 was designed to have optimal DOCSIS performance when used with a differential input signal, the AD8328 can also be used as a single-ended receiver, or an IF digitally controlled amplifier. However, as with the single-ended-to-differential configuration previously noted, even-order harmonic distortion is slightly degraded.

When operating the AD8328 in a single-ended input mode, V_{IN+} and V_{IN-} should be terminated as shown in Figure 23. On the AD8328 evaluation boards, this termination method requires the removal of R2 and R3 to be shorted with R4 open, as well as the addition of 82.5 Ω at R1 and 39.2 Ω at R17 for 75 Ω termination. Table 7 shows the correct values for R11 and R12 for some common input configurations. Other input impedance configurations can be accommodated using Equation 4 and Equation 5.

$$R1 = \frac{Z_{IN} \times 800}{800 - Z_{IN}} \quad (4)$$

$$R17 = \frac{Z_{IN} \times R1}{R1 + Z_{IN}} \quad (5)$$

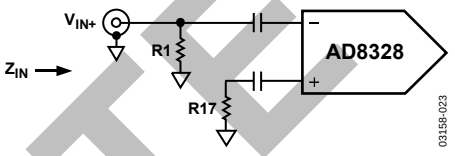


Figure 23. Single-Ended Circuit

Table 7. Common Matching Resistors

Differential Input Termination			
Z_{IN} (Ω)	**R2/R3**	**R4 (Ω)**	**R1/R17**
50	Open	51.1	Open/Open
75	Open	78.7	Open/Open
100	Open	107.0	Open/Open
150	Open	165.0	Open/Open
Single-Ended Input Termination			
Z_{IN} (Ω)	**R2 (Ω)/R3 (Ω)**	**R4 (Ω)**	**R1 (Ω)/R17 (Ω)**
50	0/0	Open	53.6/25.5
75	0/0	Open	82.5/39.2

OVERSHOOT ON PC PRINTER PORTS

The data lines on some PC parallel printer ports have excessive overshoot that can cause communication problems when presented to the CLK pin of the AD8328. The evaluation board was designed to accommodate a series resistor and shunt capacitor (R2 and C5 in Figure 26) to filter the CLK signal if required.

INSTALLING VISUAL BASIC CONTROL SOFTWARE

Install the CabDrive_28 software by running the setup.exe file on Disk One of the AD8328 evaluation software. Follow the on-screen directions and insert Disk Two when prompted. Choose the installation directory and then select the icon in the upper left to complete the installation.

RUNNING AD8328 SOFTWARE

To load the control software, go to Start, Programs, CABDRIVE_28 or select the AD8328.exe file from the installed directory. Once loaded, select the proper parallel port to communicate with the AD8328 (see Figure 24).

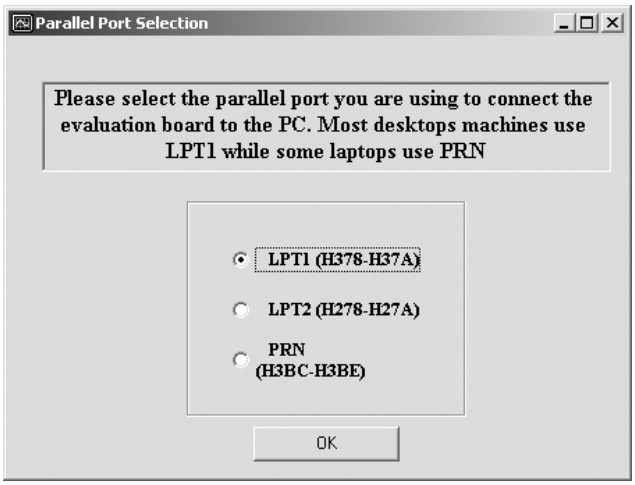


Figure 24. Parallel Port Selection

CONTROLLING GAIN/ATTENUATION OF THE AD8328

The SLIDER controls the gain/attenuation of the AD8328, which is displayed in dB and in V/V. The gain scales 1 dB per LSB. The gain code from the position of the SLIDER is displayed in decimal, binary, and hexadecimal (see Figure 25).

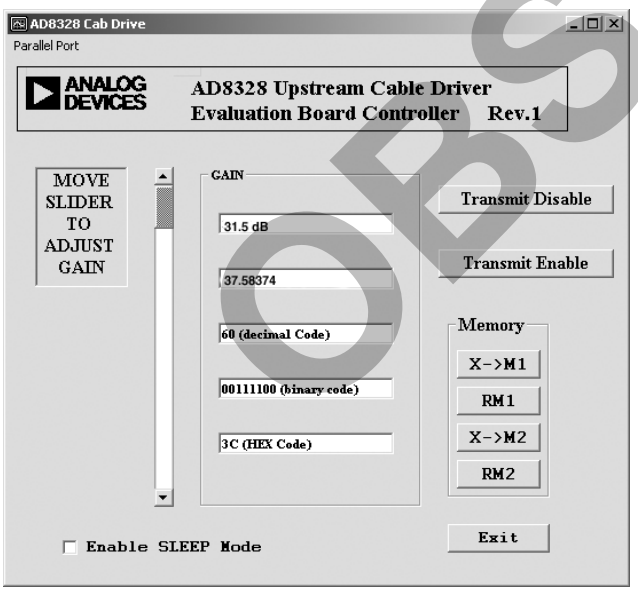


Figure 25. Control Software Interface

TRANSMIT ENABLE AND SLEEP MODE

The Transmit Enable and Transmit Disable buttons select the mode of operation of the AD8328 by asserting logic levels on the asynchronous TXEN pin. The Transmit Disable button applies Logic 0 to the TXEN pin, disabling forward transmission. The Transmit Enable button applies Logic 1 to the TXEN pin, enabling the AD8328 for forward transmission. Checking the Enable $\overline{\text{SLEEP}}$ Mode box applies Logic 0 to the asynchronous $\overline{\text{SLEEP}}$ pin, setting the AD8328 for $\overline{\text{SLEEP}}$ mode.

MEMORY FUNCTIONS

The Memory section of the software provides a way to alternate between two gain settings. The X→M1 button stores the current value of the GAIN SLIDER into memory, while the RM1 button recalls the stored value, returning the gain SLIDER to the stored level. The same applies to the X→M2 and RM2 buttons.

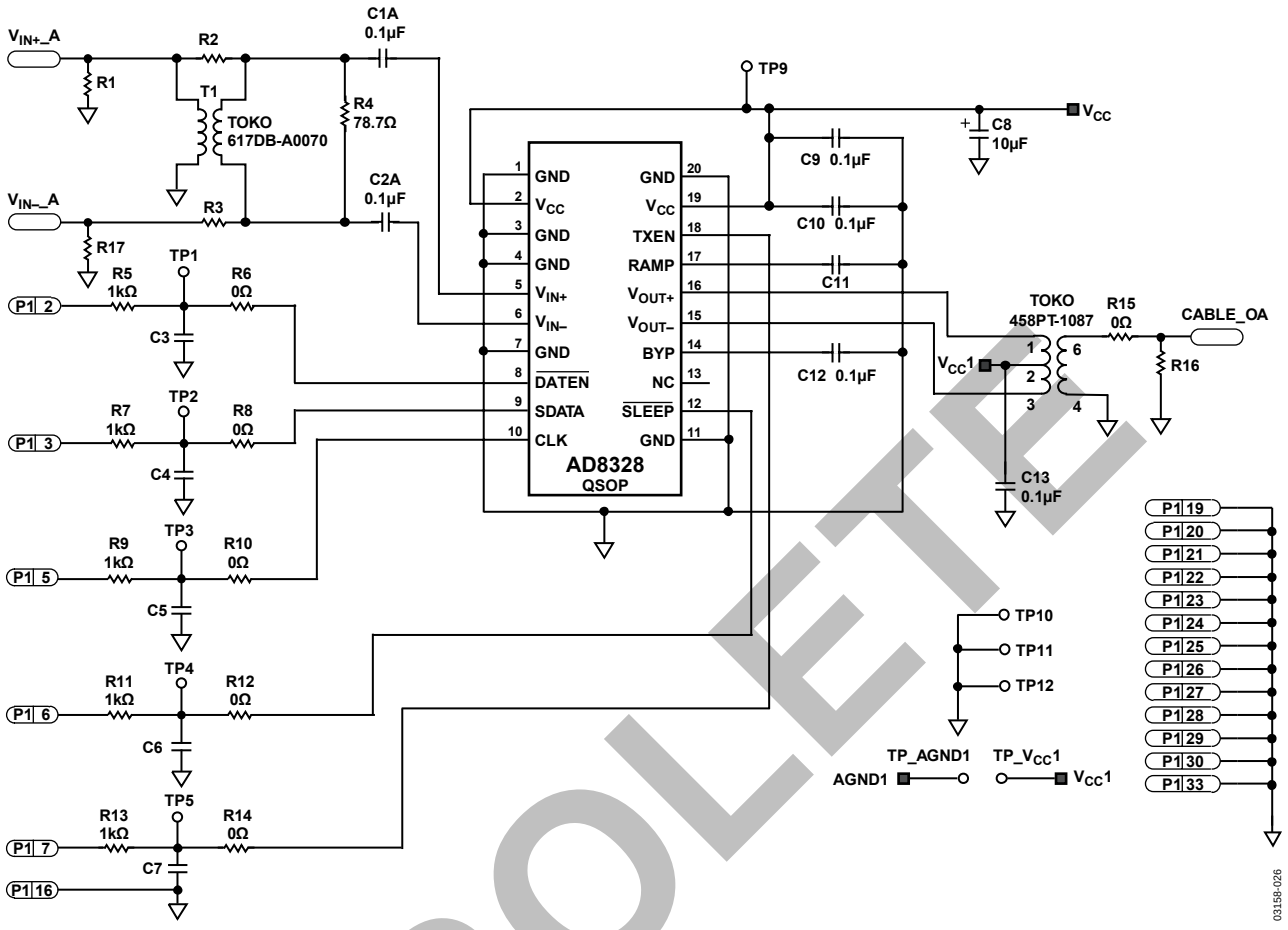


Figure 26. AD8328 Evaluation Board Schematic

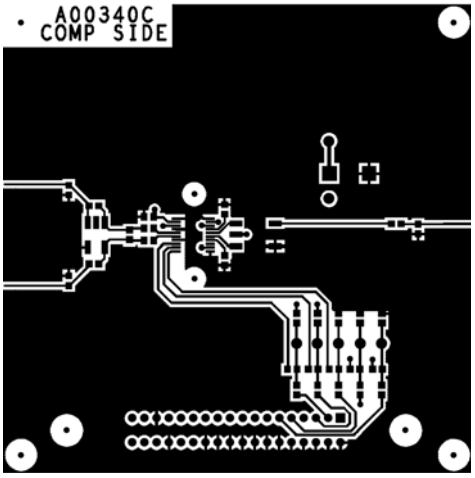


Figure 27. Primary Side

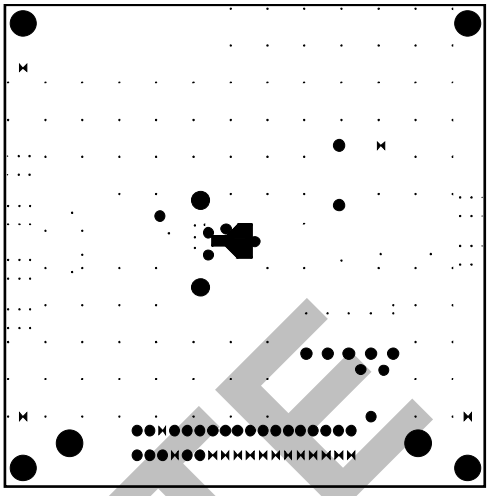


Figure 30. Internal Ground Plane

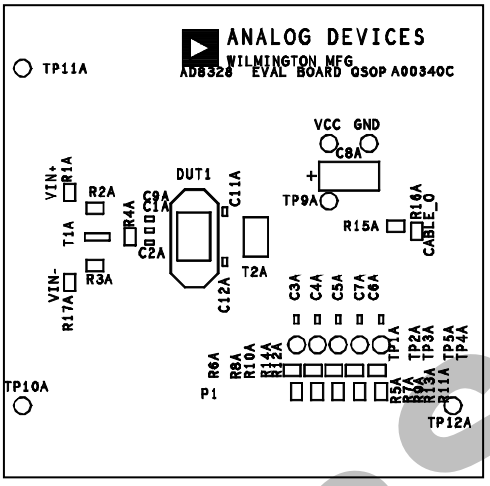


Figure 28. Component Side Silkscreen

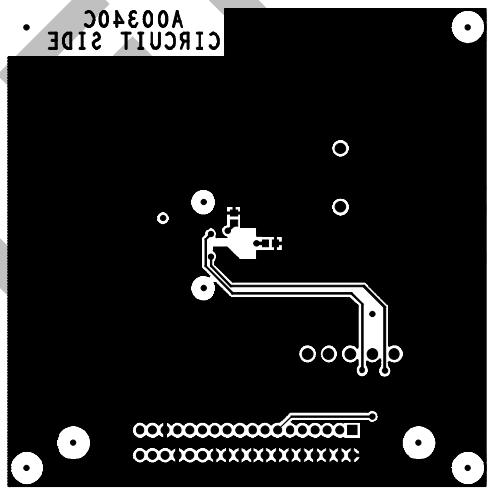


Figure 31. Secondary Side

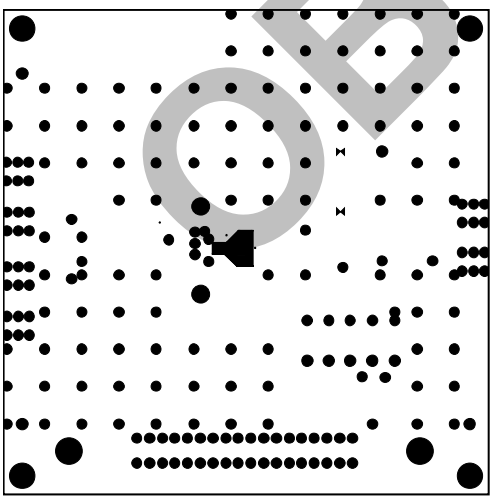


Figure 29. Internal Power Plane

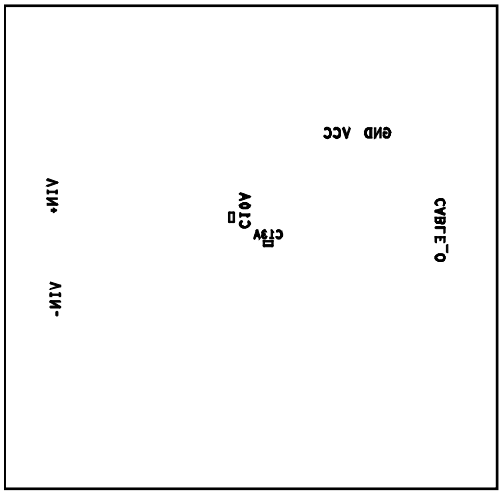
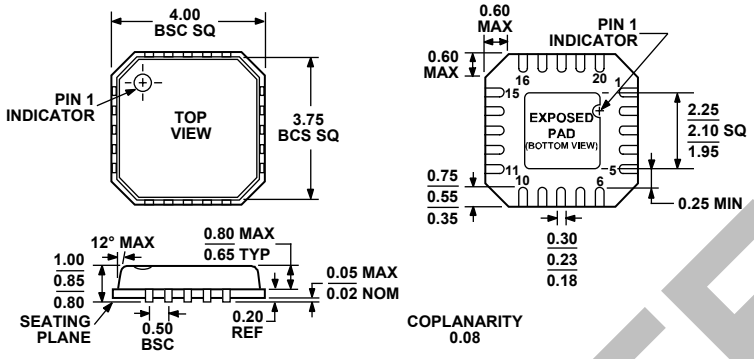


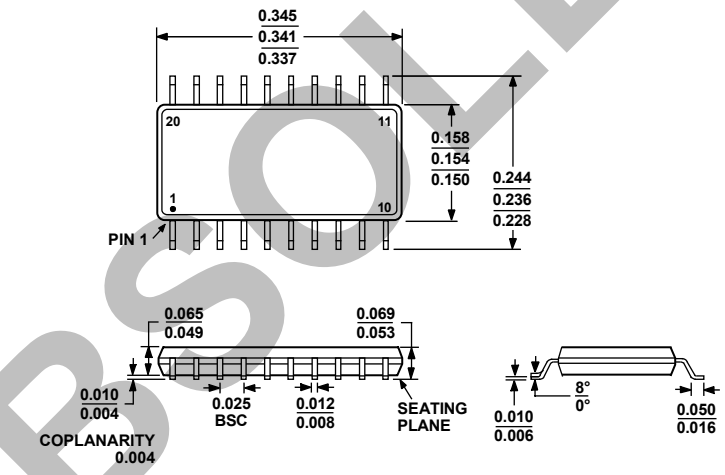
Figure 32. Secondary Side Silkscreen

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 33. 20-Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-137-AD

Figure 34. 20-Lead Shrink Small Outline Package [QSOP]
(RQ-20)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8328ARQ	–40°C to +85°C	20-Lead QSOP	RQ-20
AD8328ARQ-REEL	–40°C to +85°C	20-Lead QSOP	RQ-20
AD8328ARQZ[1]	–40°C to +85°C	20-Lead QSOP	RQ-20
AD8328ARQZ-REEL[1]	–40°C to +85°C	20-Lead QSOP	RQ-20
AD8328ACP	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACP-REEL	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACP-REEL7	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACPZ[1]	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACPZ-REEL[1]	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACPZ-REEL7[1]	–40°C to +85°C	20-Lead LFCSP_VQ	CP-20-1
AD8328ACP-EVAL		Evaluation Board	
AD8328ARQ-EVAL		Evaluation Board	

[1] Z = Pb-free part.

NOTES

NOTES

C03158–0–10/05(A)

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