



**THE DATASHEET OF  
IRL3303LPBF**



# International IOR Rectifier

- Logic-Level Gate Drive
- Advanced Process Technology
- Surface Mount (IRL3303S)
- Low-profile through-hole (IRL3303L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

## Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRL3303L) is available for low-profile applications.

## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	38	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	27	
$I_{DM}$	Pulsed Drain Current $\text{①}^{\text{⑤}}$	140	
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 16$	V
$E_{AS}$	Single Pulse Avalanche Energy $\text{②}^{\text{⑤}}$	130	mJ
$I_{AR}$	Avalanche Current $\text{①}$	20	A
$E_{AR}$	Repetitive Avalanche Energy $\text{①}$	6.8	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ $\text{③}^{\text{⑤}}$	5.0	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	---	2.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient ( PCB Mounted, steady-state)**	---	40	

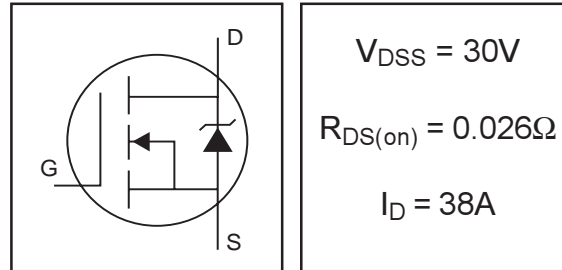
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PD - 95578

## IRL3303LPbF

## IRL3303SPbF

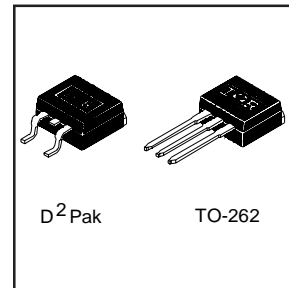
HEXFET® Power MOSFET



$$V_{DSS} = 30\text{V}$$

$$R_{DS(on)} = 0.026\Omega$$

$$I_D = 38\text{A}$$



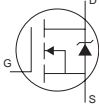
D<sup>2</sup>Pak

TO-262

## Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.035	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA <sup>①</sup>
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.026	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 20A <sup>④</sup>
		—	—	0.040		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 17A <sup>④</sup> T <sub>J</sub> = 150°C
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	12	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 20A <sup>④</sup>
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	26	nC	I <sub>D</sub> = 20A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	8.8		V <sub>DS</sub> = 24V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	15		V <sub>GS</sub> = 4.5V, See Fig. 6 and 13 <sup>④⑤</sup>
t <sub>d(on)</sub>	Turn-On Delay Time	—	7.4	—		V <sub>DD</sub> = 15V
t <sub>r</sub>	Rise Time	—	200	—	I <sub>D</sub> = 20A R <sub>G</sub> = 6.5Ω R <sub>D</sub> = 0.7Ω, See Fig. 10 <sup>④⑤</sup>	
t <sub>d(off)</sub>	Turn-Off Delay Time	—	14	—		
t <sub>f</sub>	Fall Time	—	36	—		
L <sub>S</sub>	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
C <sub>iss</sub>	Input Capacitance	—	870	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	340	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	170	—		f = 1.0MHz, See Fig. 5 <sup>⑤</sup>

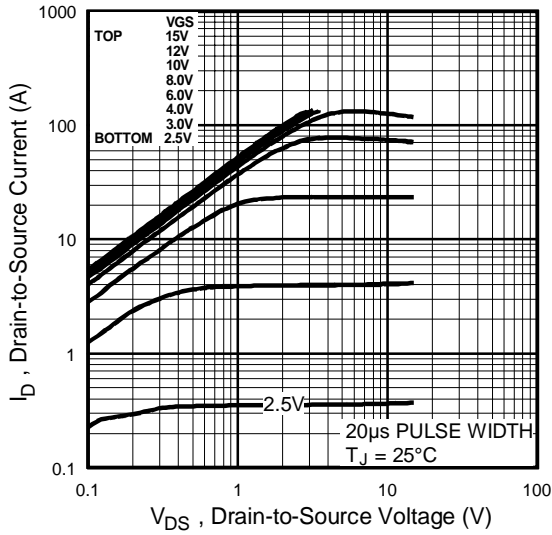
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>①</sup>	—	—	140		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 20A, V <sub>GS</sub> = 0V <sup>④</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	72	110	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 20A
Q <sub>rr</sub>	Reverse Recovery Charge	—	180	280	nC	di/dt = 100A/μs <sup>④⑤</sup>
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

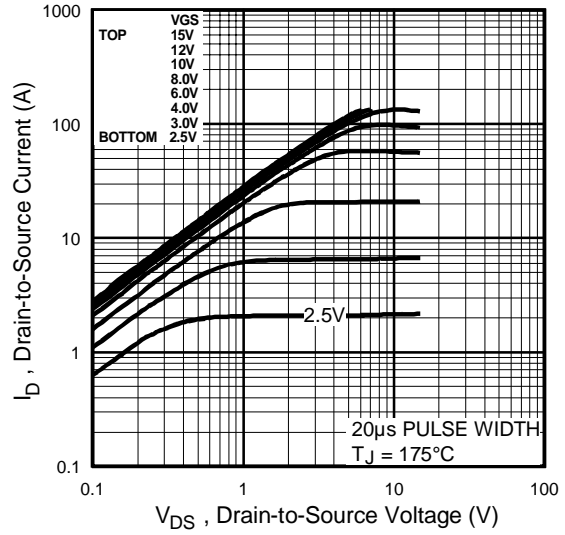
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 15V, starting T<sub>J</sub> = 25°C, L = 470μH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 20A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 20A, di/dt ≤ 140A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>,  
T<sub>J</sub> ≤ 175°C
- ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ⑤ Uses IRL3303 data and test conditions.

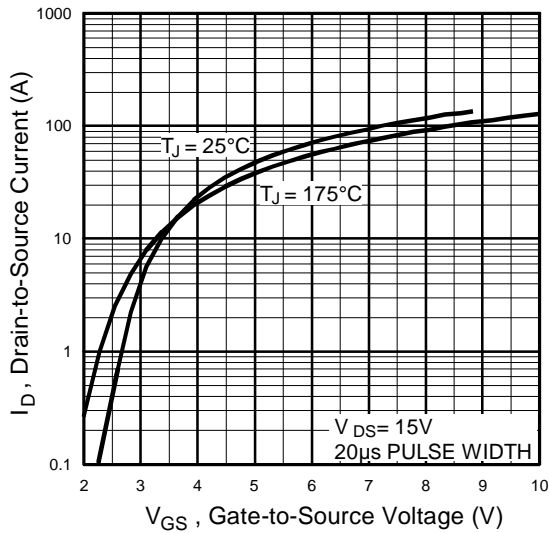
\*\* When mounted on 1" square PCB ( FR-4 or G-10 Material ).  
For recommended footprint and soldering techniques refer to application note #AN-994.



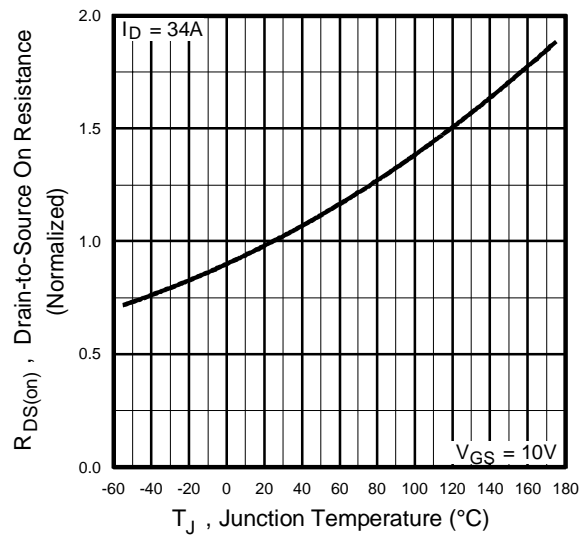
**Fig 1.** Typical Output Characteristics



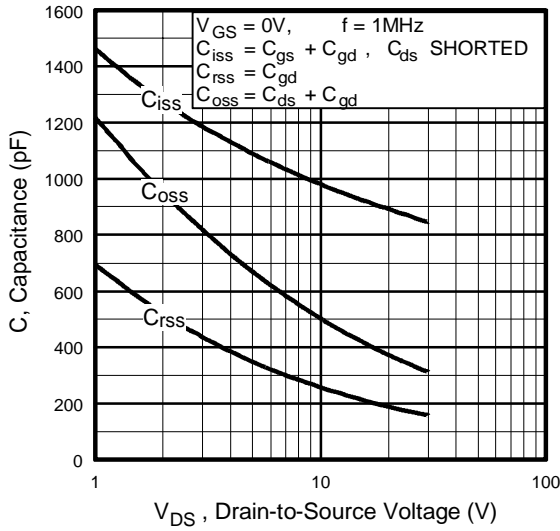
**Fig 2.** Typical Output Characteristics



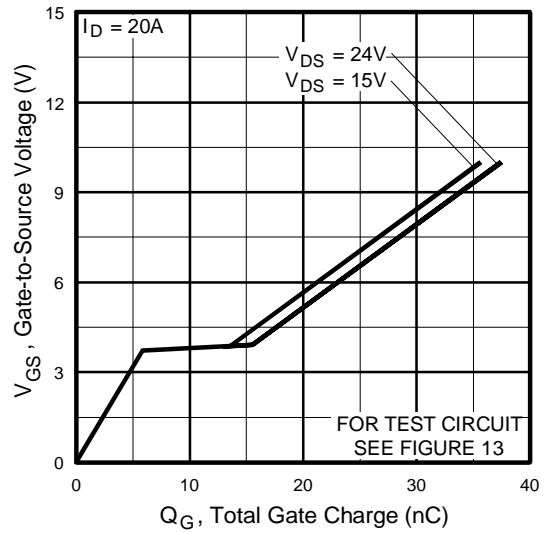
**Fig 3.** Typical Transfer Characteristics



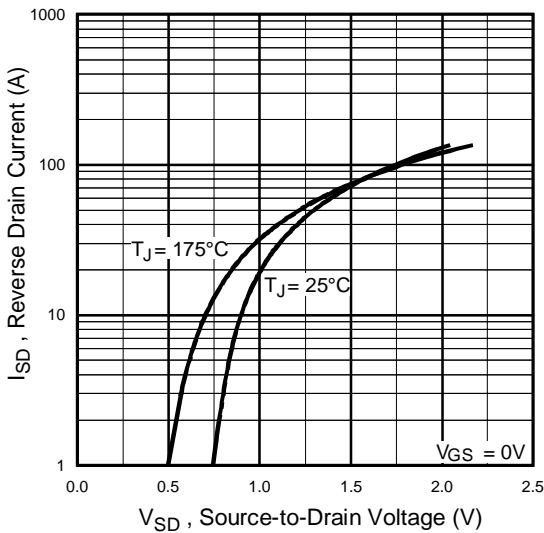
**Fig 4.** Normalized On-Resistance Vs. Temperature



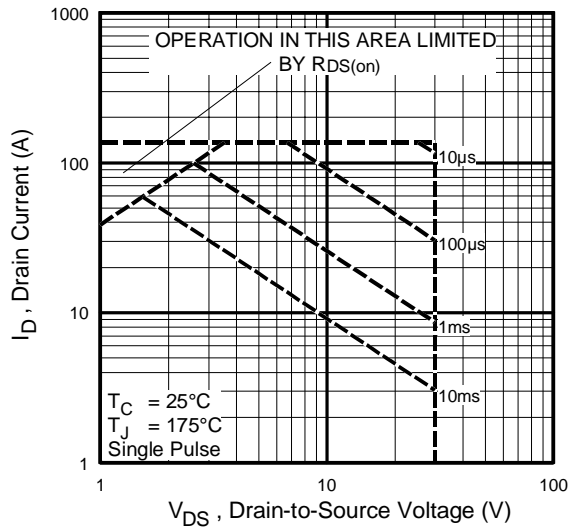
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



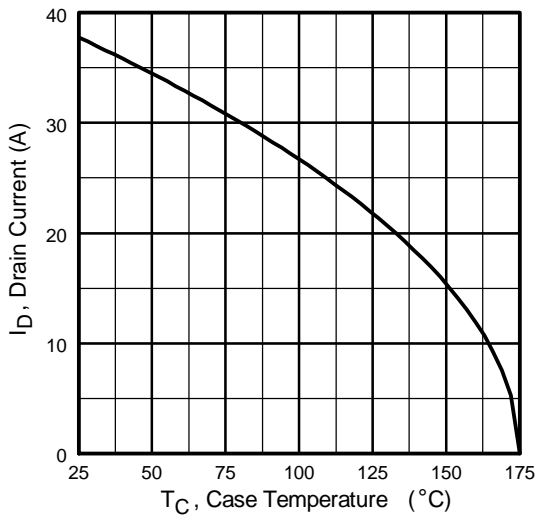
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



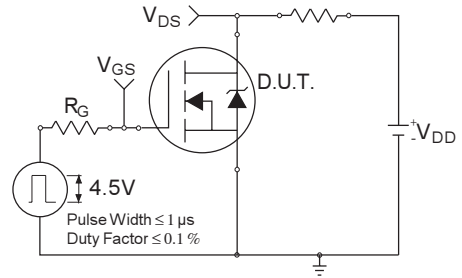
**Fig 7.** Typical Source-Drain Diode Forward Voltage



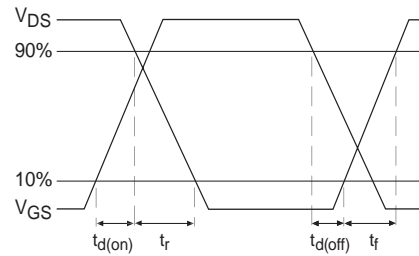
**Fig 8.** Maximum Safe Operating Area



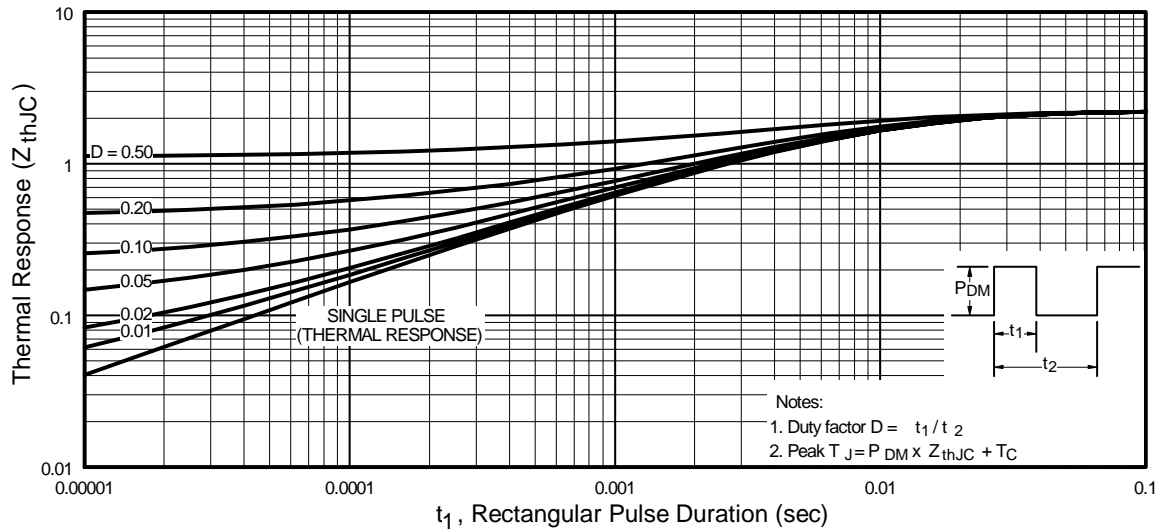
**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



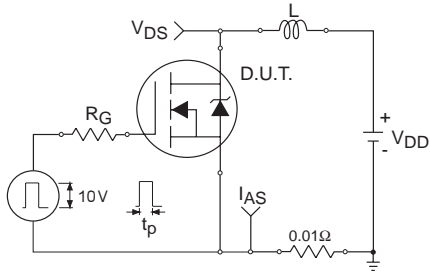
**Fig 10b.** Switching Time Waveforms



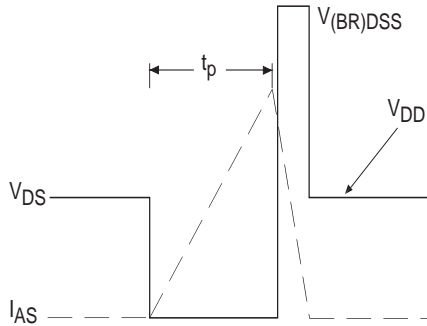
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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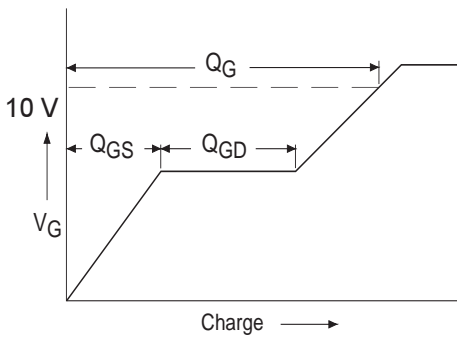
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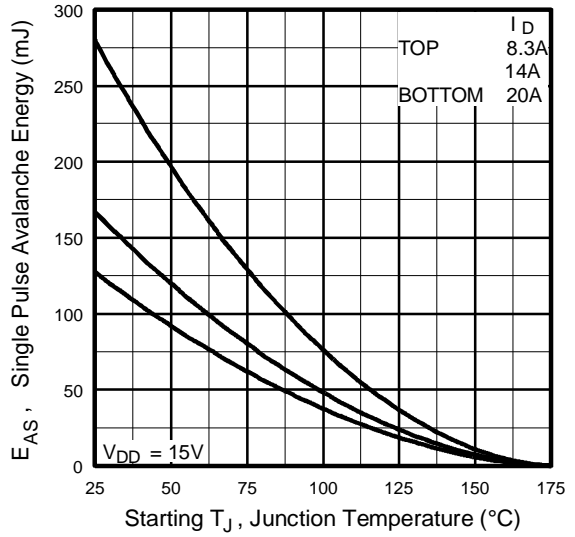
**Fig 12a.** Unclamped Inductive Test Circuit



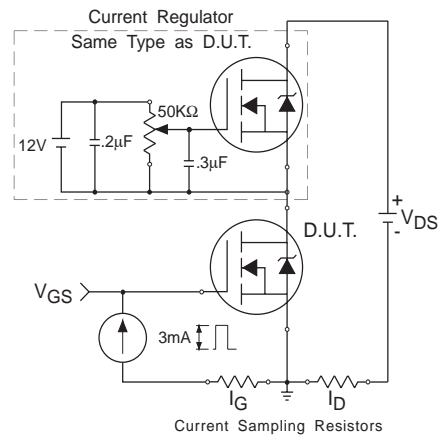
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

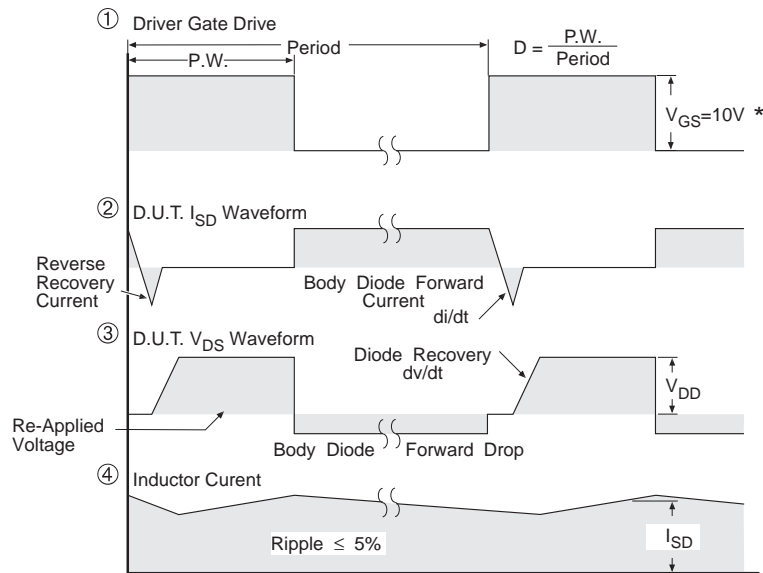
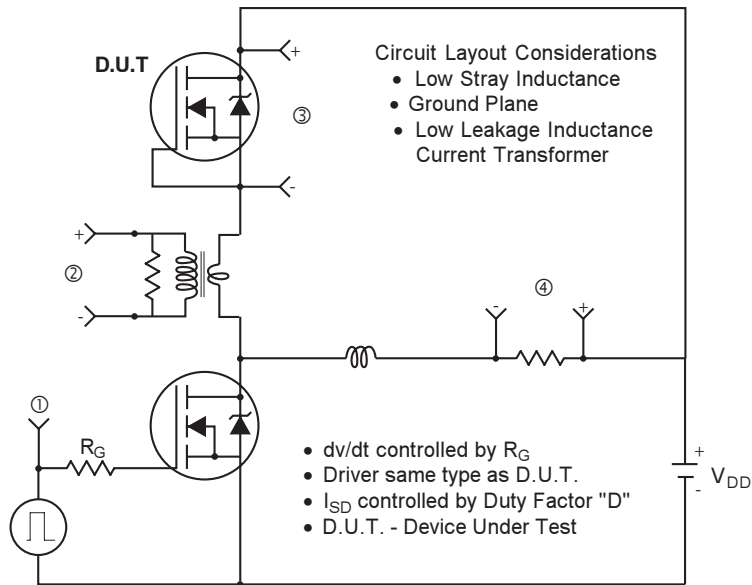


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\*  $V_{GS} = 5V$  for Logic Level Devices

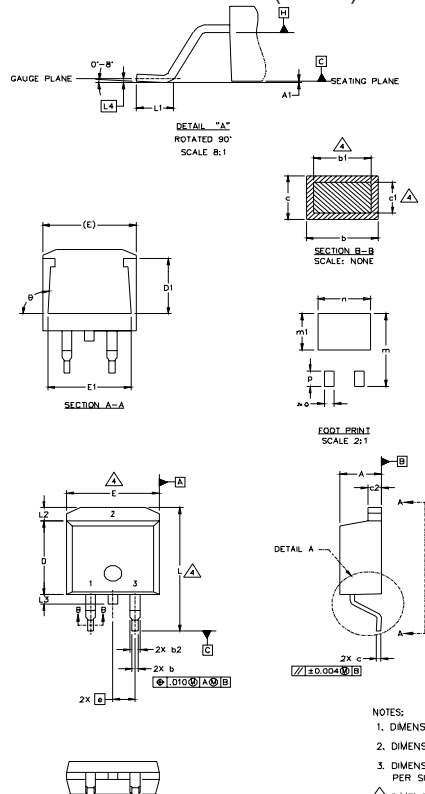
**Fig 14.** For N-Channel HEXFETS

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## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1	0.127			.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	3
D	8.51	9.65	.335	.380	
D1	5.33		.210		3
E	9.65	10.67	.380	.420	
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2			1.65	.065	
L3	1.27	1.78	.050	.070	
L4	0.25	BSC	.010	BSC	
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

### LEAD ASSIGNMENTS

HEXFET	IGBTs, CoPACK	DIODES
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

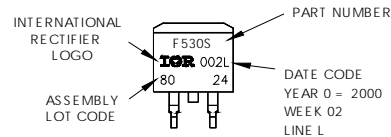
\* PART DEPENDENT

### NOTES:

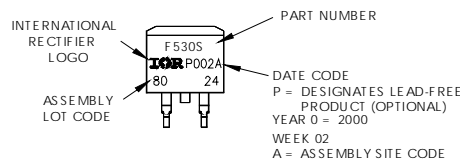
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"  
Note: "P" in assembly line  
position indicates "Lead-Free"

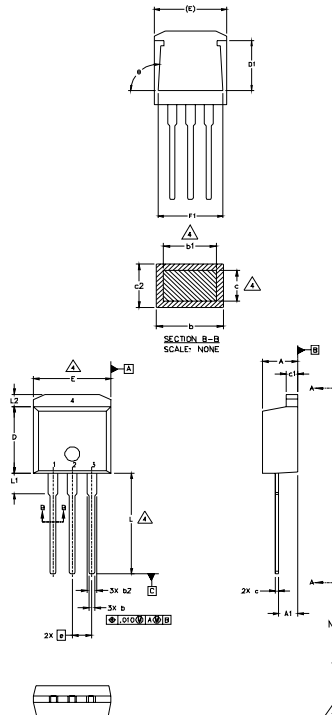


**OR**



## TO-262 Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	2.92	.080	.115	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	4
b2	1.14	1.40	.045	.055	
c	0.38	0.63	.015	.025	4
c1	1.14	1.40	.045	.055	
c2	0.43	.063	.017	.029	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54	BSC	.100	BSC	
L	13.46	14.09	.530	.555	
L1	3.56	3.71	.140	.146	
L2		1.65		.065	

### LEAD ASSIGNMENTS

#### HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

#### IGBT

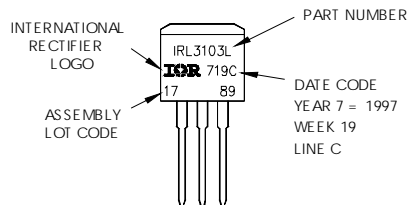
- 1 - GATE
- 2 - COLLECTOR
- 3 - EMITTER

#### NOTES:

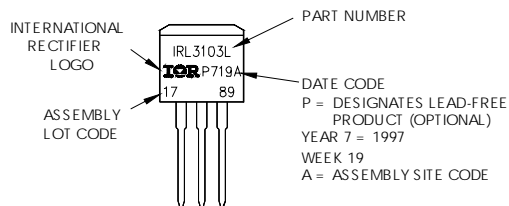
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
 Note: "P" in assembly line  
 position indicates "Lead-Free"



**OR**

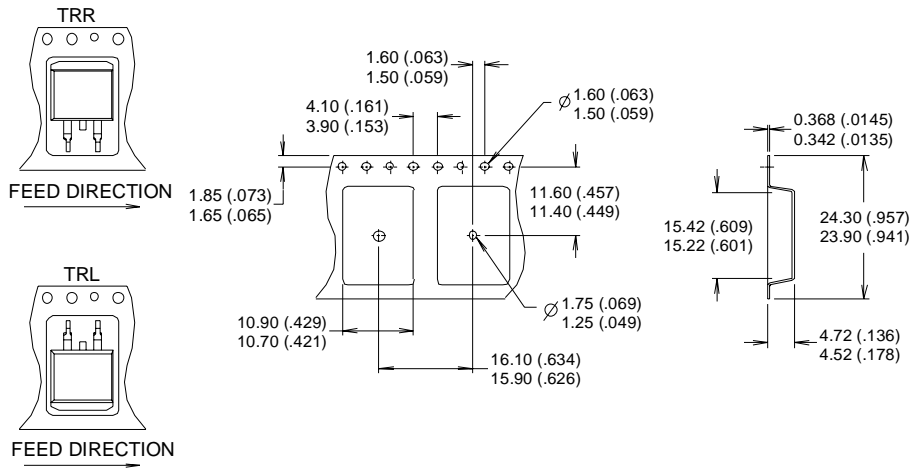


# IRL3303S/LPbF

International  
**IR** Rectifier

## D<sup>2</sup>Pak Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONFORMS TO EIA-418.
2. CONTROLLING DIMENSION: MILLIMETER.
- ③ DIMENSION MEASURED @ HUB.
- ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.

Data and specifications subject to change without notice.

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**IR** Rectifier

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TAC Fax: (310) 252-7903

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Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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