

Dual Synchronous 800 mA/800 mA Step-Down DC/DC Regulator

Features

- High Efficiency: Over 96%
- Ultra-Low Quiescent Current: Only 28 μ A
- Ultra-Low Shutdown Current: Less Than 1 μ A
- Fast Transient Performance
- 2.5 MHz PWM Operation
- High Output Current Capability per Channel: 800 mA
- No Schottky Diodes Required
- Stable with 2.2 μ H Inductor, 10 μ F Ceramic Capacitor
- Adjustable Output Voltage Down to 0.8V
- Built-In Soft-Start Circuitry
- Current-Limit Protection
- Automatic Switching into Light Load Mode Operation
- /FPWM Pin allows Low-Noise Forced PWM Mode Operation
- Power Good Output with Internal 5 μ A Current Source allows Sequencing with Programmable Delay Time
- Small Thermally Enhanced 3 mm \times 3 mm TDFN-12L Package

Applications

- MPU & ASIC Power
- PDAs
- Digital Cameras
- PC Cards
- Wireless and DSL Modems

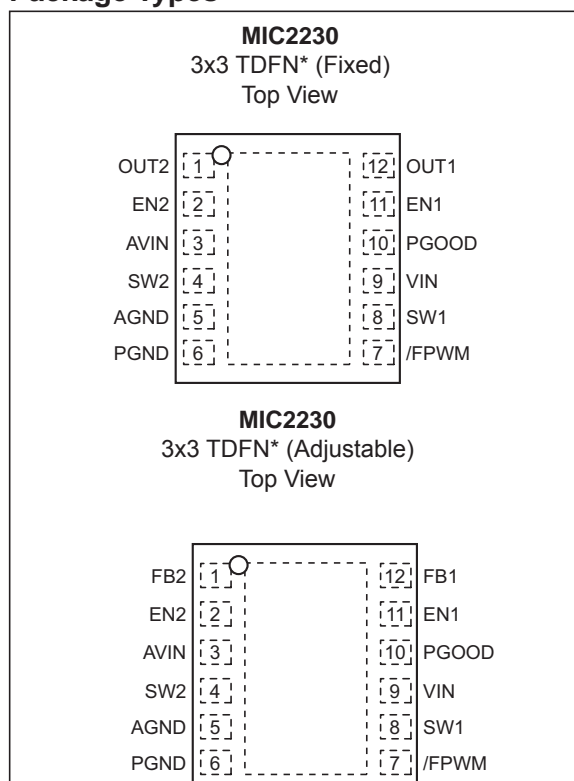
General Description

The MIC2230 is a dual output, high-efficiency synchronous step-down DC/DC converter. The MIC2230 is ideally suited for portable and embedded systems that demand high power conversion efficiencies and fast transient performance, while offered in a very small package. The MIC2230 offers an ultra-low quiescent current in light load mode, assuring minimum current draw from battery powered applications in standby modes. The MIC2230 was designed to only require miniature 2.2 μ H inductors and 10 μ F ceramic capacitors.

The MIC2230 features a selectable mode that allows the user to trade-off lowest noise performance for low power efficiency. Trickle mode operation provides ultra-high efficiency at light loads, while PWM operation provides very low ripple noise performance. To maximize battery life in low-dropout conditions, MIC2230 can operate with a maximum duty cycle of 100%.

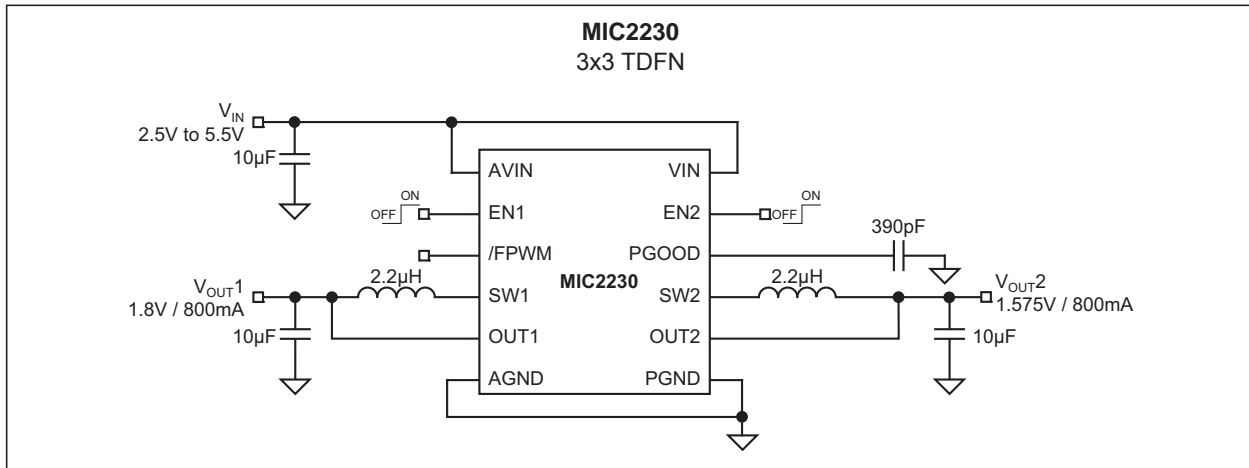
The MIC2230 is available in a space-saving 3 mm \times 3 mm TDFN-12L package with a junction temperature range from -40°C to $+125^{\circ}\text{C}$.

Package Types

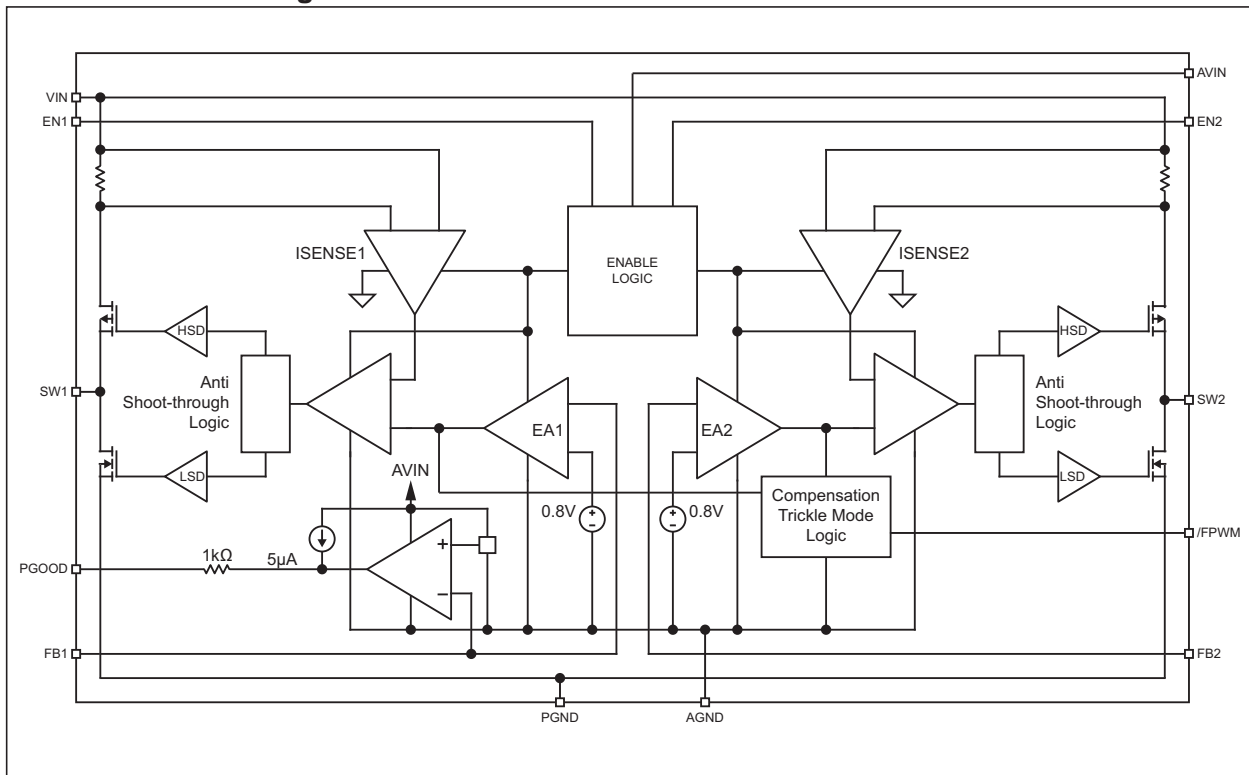


MIC2230

Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

| | |
|--|----------------|
| Supply Voltage, (V_{IN}) | +6V |
| Enable 1 Voltage | +6V |
| Enable 2 Voltage | +6V |
| Logic Input Voltage, (V_{EN} , V_{FPWM}) | 0V to V_{IN} |
| ESD Protection | +2 kV |

Operating Ratings ††

| | |
|--------------------------------|---------------|
| Supply Voltage, V_{IN} | +2.5V to 5.5V |
|--------------------------------|---------------|

† Notice: Exceeding the absolute maximum rating may damage the device.

†† Notice: The device is not guaranteed to function outside its operating rating.

DC CHARACTERISTICS (Note 1)

Electrical Characteristics: Unless otherwise indicated, $T_A = 25^\circ\text{C}$ with $V_{IN} = V_{EN1} = V_{EN2} = 3.6\text{V}$, V_{OUT1} , V_{OUT2} : $L = 2.2 \mu\text{H}$, $C = 10 \mu\text{F}$. **Bold** values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|-----------------------------------|------|--------------|------|--------------|---------------|--|
| Supply Voltage and Current | | | | | | |
| Supply Voltage Range | | 2.5 | — | 5.5 | V | — |
| UVLO (Rising) | | 2.3 | 2.4 | 2.5 | V | — |
| UVLO Hysteresis | | — | 100 | — | mV | — |
| PWM Mode Supply Current | | — | 560 | 950 | μA | /FPWM = Low; V_{OUT1} , $V_{OUT2} = 1.03 * V_{NOM}$ (not switching) |
| Trickle Mode Supply Current | | — | 28 | 50 | μA | /FPWM = High; V_{OUT1} , $V_{OUT2} = 1.03 * V_{NOM}$ (not switching) |
| Shutdown Quiescent Current | | — | 0.1 | 1 | μA | $V_{EN} = 0\text{V}$ |
| Output Voltage Accuracy | | | | | | |
| Feedback Voltage, V_{FB} | | 0.780 | 0.8 | 0.820 | V | Adjustable |
| Output Voltage, V_{OUT} | | -2.5 | — | +2.5 | % | Fixed Output Options |
| Feedback Bias Current | | — | 10 | — | nA | — |
| Output Voltage Line Regulation | | — | 0.1 | 0.5 | % | $2.5\text{V} \leq V_{IN} \leq 5.5\text{V}$ |
| Output Voltage Load Regulation | | — | 0.5 | — | % | $V_{IN} = 5\text{V}$, $I_{OUT} = 10 \text{ mA}$ to 800 mA , /FPWM = 0V $V_{IN} = 3\text{V}$, $I_{OUT} = 10 \text{ mA}$ to 800 mA , /FPWM = 0V |
| Ripple in Trickle Mode | | — | 40 | — | mV | $V_{IN}=3.6\text{V}$; $I_{OUT} = 1 \text{ mA}$; $C_{OUT} = 10 \mu\text{F}$, $L = 2.2 \mu\text{H}$. |

Note 1: Specification for packaged product only.

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DC CHARACTERISTICS (Note 1) (CONTINUED)

Electrical Characteristics: Unless otherwise indicated, $T_A = 25^\circ\text{C}$ with $V_{IN} = V_{EN1} = V_{EN2} = 3.6\text{V}$, V_{OUT1} , V_{OUT2} : $L = 2.2\ \mu\text{H}$, $C = 10\ \mu\text{F}$. **Bold values indicate $-40^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$.**

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|----------------------------|------|---------------------------------------|------|---------------------------------------|---------------|----------------------------------|
| Logic Inputs | | | | | | |
| EN Input Threshold | | — | 0.8 | 1.2 | V | On |
| | | 0.3 | 0.7 | — | V | Off |
| EN Input Current | | — | 0.01 | 1 | μA | — |
| /FPWM Input Threshold | | — | — | $0.6 \times V_{IN}$ | V | On |
| | | $0.3 \times V_{IN}$ | — | — | V | Off |
| /FPWM Input Current | | — | 0.01 | 1 | μA | — |
| Protection | | | | | | |
| Current-Limit | | 0.9 | 1.2 | 1.8 | A | — |
| Control | | | | | | |
| Maximum Duty Cycle | | 100 | — | — | % | — |
| Oscillator | | | | | | |
| PWM Mode Frequency | | 2.125 | 2.5 | 2.875 | MHz | — |
| Power Good | | | | | | |
| Power Good Reset Threshold | | — | 6.25 | 12 | % | Upper Threshold |
| | | -14 | -8.5 | — | % | Lower Threshold |
| PGOOD Series Resistance | | — | 1 | 1.4 | k Ω | — |
| PGOOD Pull-Up Current | | — | 5 | — | μA | Output within 8.5% of regulation |
| Power Switch | | | | | | |
| Switch On-Resistance | | — | 0.4 | — | Ω | $I_{SW} = 150\ \text{mA}$ (PFET) |
| | | — | 0.35 | — | Ω | $I_{SW} = 150\ \text{mA}$ (NFET) |

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS (Note 1)

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|------------------------------------|---------------|------|------|------|-------|------------|
| Temperature Ranges | | | | | | |
| Storage Temperature Range | T_A | -65 | — | +150 | °C | — |
| Junction Operating Temperature | T_J | -40 | — | +125 | °C | — |
| Package Thermal Resistances | | | | | | |
| Thermal Resistance, 3 x 3 QFN-12Ld | θ_{JA} | — | 60 | — | °C/W | — |
| | θ_{JC} | — | 15 | — | °C/W | — |

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A , T_J , θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

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2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

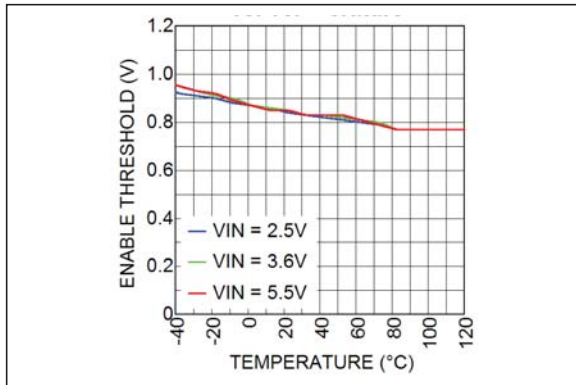


FIGURE 2-1: Enabled Threshold vs. Temperature.

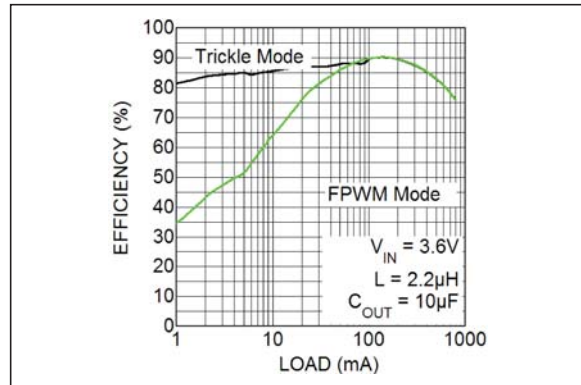


FIGURE 2-4: MIC2230 Efficiency
 $V_{OUT} = 1.575V$.

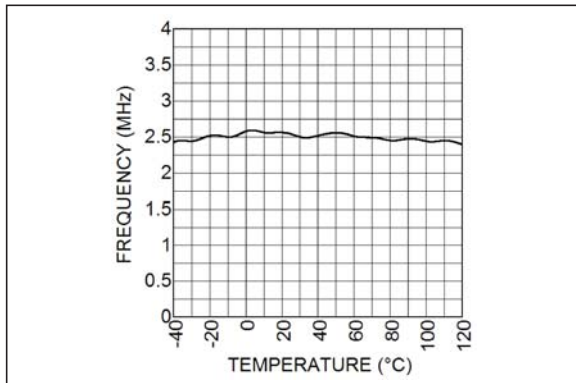


FIGURE 2-2: Frequency vs. Temperature.

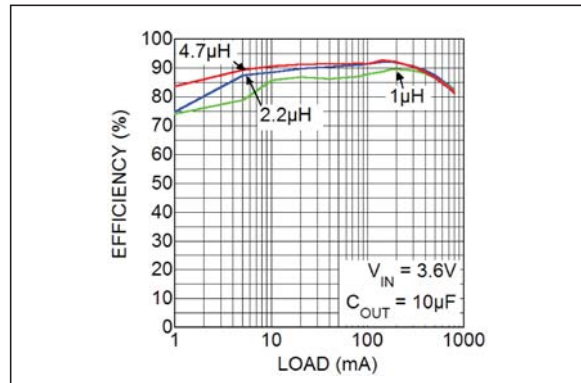


FIGURE 2-5: MIC2230 Efficiency
 $V_{OUT} = 1.8V$.

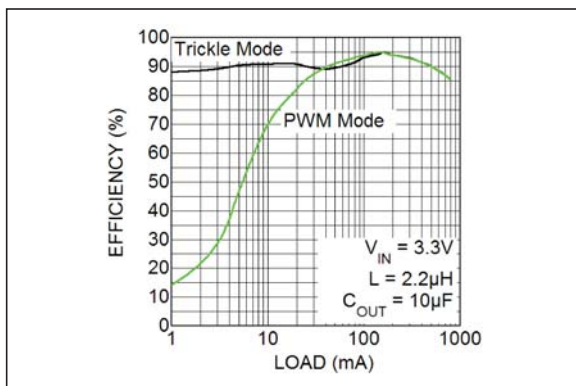


FIGURE 2-3: Efficiency.

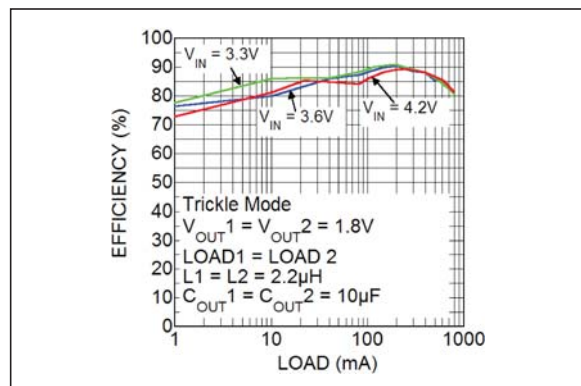


FIGURE 2-6: MIC2230 Efficiency
 $V_{OUT1} = V_{OUT2} = 1.8V$.

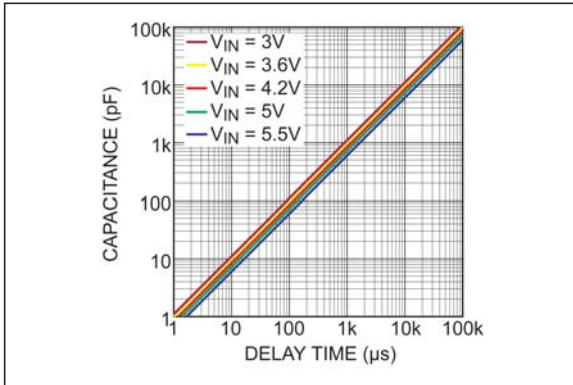


FIGURE 2-7: Capacitance vs. Delay Time.

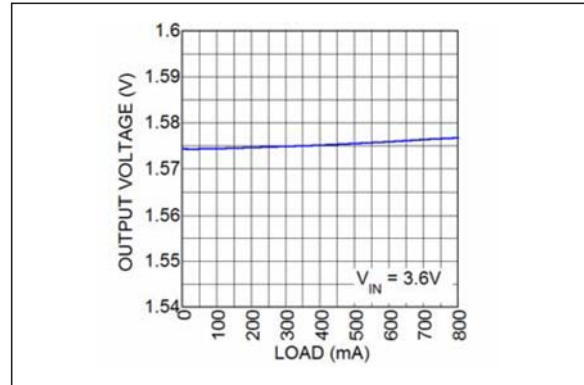


FIGURE 2-10: Output Voltage vs. Load.

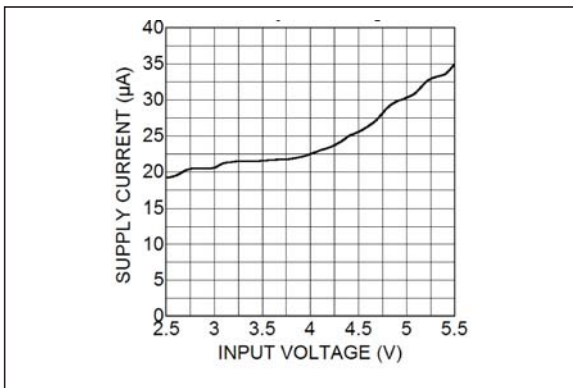


FIGURE 2-8: Trickle Mode Current vs. Input Voltage.

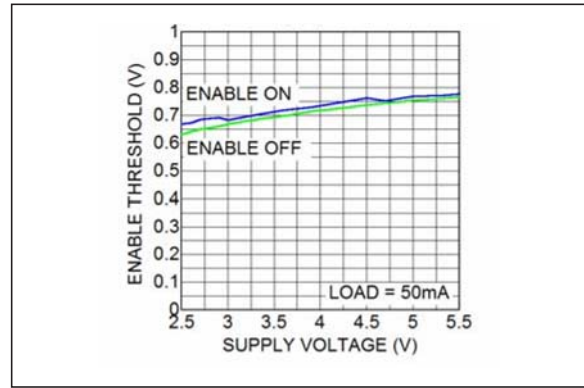


FIGURE 2-11: Enable Threshold vs. Supply Voltage.

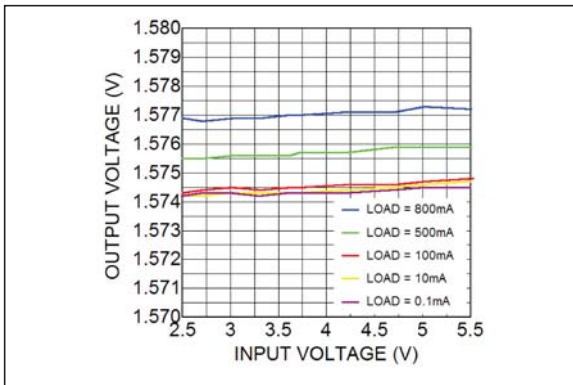


FIGURE 2-9: Output Voltage vs. Input Voltage.

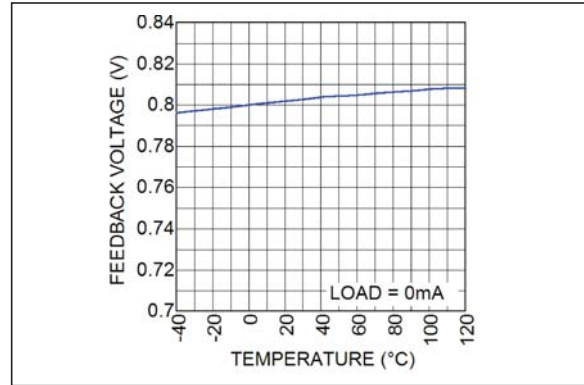


FIGURE 2-12: Feedback Voltage vs. Temperature.

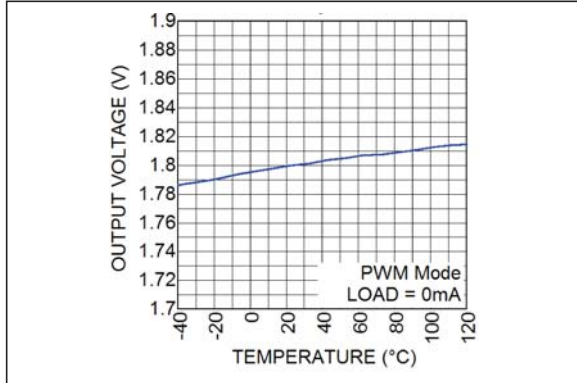


FIGURE 2-13: Output Voltage vs. Temperature.

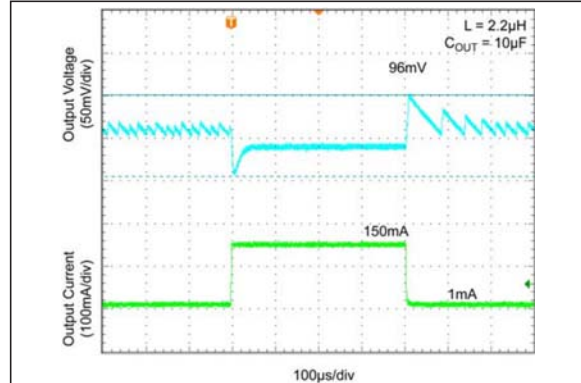


FIGURE 2-16: Load Transient Trickle Mode.

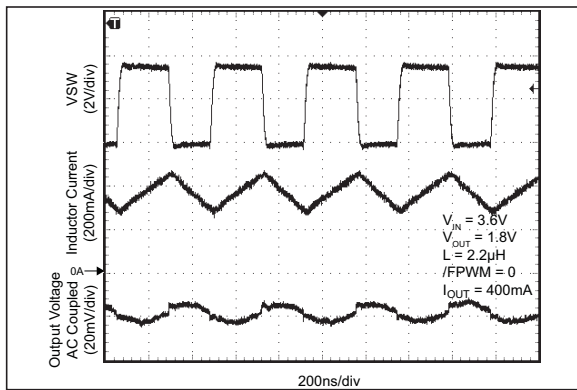


FIGURE 2-14: FPWM Mode.

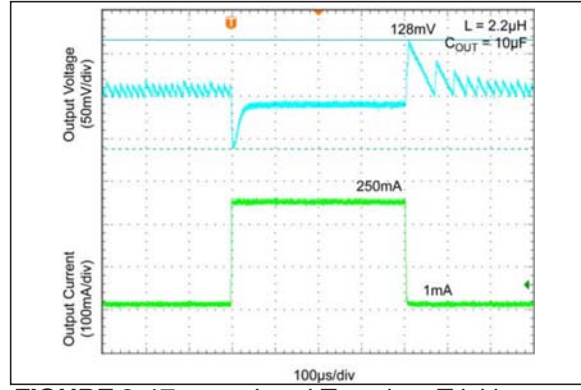


FIGURE 2-17: Load Transient Trickle Mode.

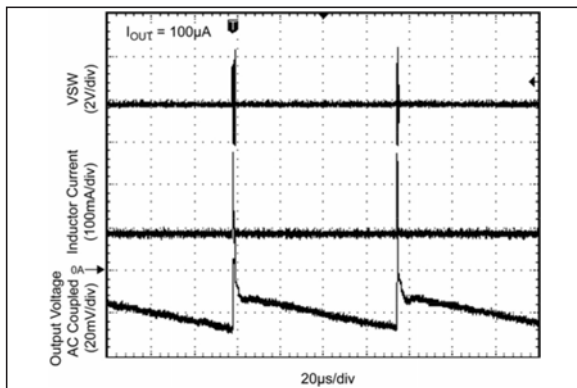


FIGURE 2-15: Trickle Mode.

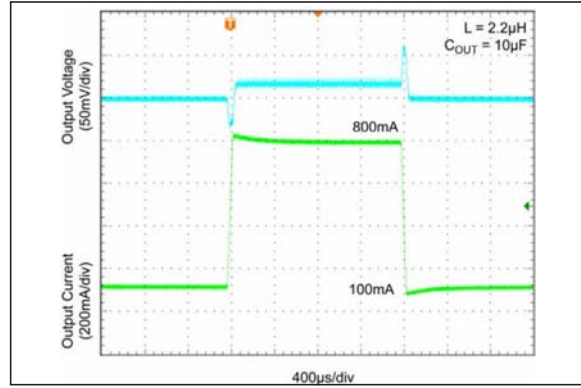


FIGURE 2-18: Load Transient PWM Mode.

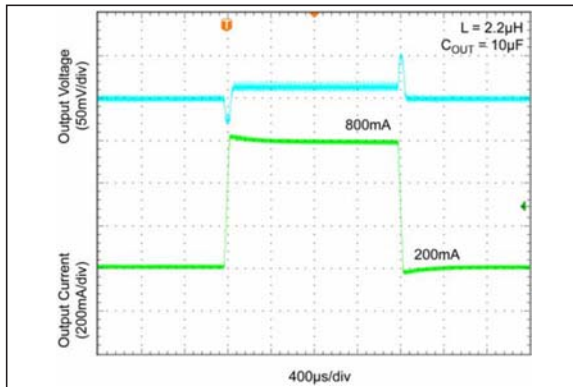


FIGURE 2-19: Load Transient PWM Mode.

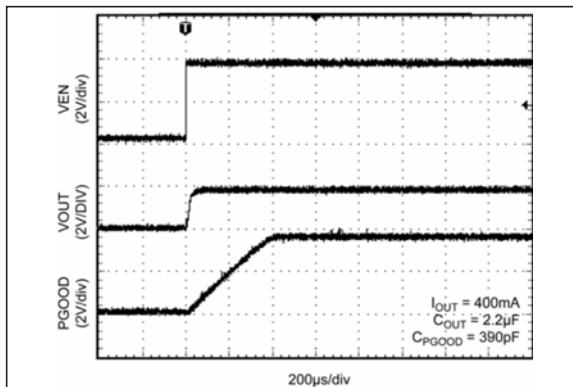


FIGURE 2-20: Enable Response.

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3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in [Table 3-1](#).

TABLE 3-1: PIN FUNCTION TABLE

| MIC2230 Adjustable 3X3 QFN | MIC2230 Fixed 3X3 QFN | Symbol | Description |
|----------------------------|-----------------------|--------|---|
| 1 | — | FB2 | Feedback 2: For adjustable voltage options connect the external resistor divider network to FB2 to set the output voltage of regulator 2. Nominal value is 0.8V. |
| 2 | 2 | EN2 | Enable 2 input. Logic low powers down regulator 2. Logic high powers up regulator 2. MIC2230 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. |
| 3 | 3 | AVIN | Analog Supply Voltage: Supply voltage for the analog control circuitry. Requires bypass capacitor to GND. |
| 4 | 4 | SW2 | Switch node for regulator 2, connected to external inductor. |
| 5 | 5 | AGND | Analog (signal) ground. |
| 6 | 6 | PGND | Power ground. |
| 7 | 7 | /FPWM | Forced PWM Mode Bar. Grounding this pin forces the device to stay in constant frequency PWM mode only. Pulling this pin high enables automatic Trickle Mode operation. |
| 8 | 8 | SW1 | Switch node for regulator 1, connected to external inductor. |
| 9 | 9 | VIN | Supply Voltage: Supply voltage for the internal switches and drivers. Requires bypass capacitor to GND. |
| 10 | 10 | PGOOD | Power Good Output. This output is pulled down unless the regulator 1 output voltage is within +6.25% and -8.5% of regulation. After the output voltage is in regulation, the output starts to go high with an internal 5 μ A current source. A delay time could be programmed by tying a capacitor to this pin. |
| 11 | 11 | EN1 | Enable 1 input. Logic low powers down regulator 1. Logic high powers up regulator 1. MIC2230 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start up. |
| 12 | — | FB1 | Feedback 1: For adjustable voltage options connect to the external resistor divider network to FB1 to set the output voltage of regulator 1. Nominal value is 0.8V. |
| — | 1 | OUT2 | Output Voltage 2. For fixed output voltage options connect OUT2 to the output voltage of regulator 2. |
| — | 12 | OUT1 | Output Voltage 1. For fixed output voltage options connect OUT1 to the output voltage of regulator 1. |
| EP | EP | EP | Exposed Thermal pad. Should be connected to the Ground plane. |

4.0 FUNCTIONAL DESCRIPTION

4.1 V_{IN}

V_{IN} provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a 10 μ F capacitor is recommended close to V_{IN} and the power ground (PGND) pin for bypassing.

4.2 AV_{IN}

Analog V_{IN} (AV_{IN}) provides power to the analog supply circuitry. AV_{IN} and V_{IN} must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by V_{IN} is reduced before reaching AV_{IN} . A 1 μ F capacitor as close to AV_{IN} as possible is recommended.

4.3 EN1

Enable 1 controls the on and off state of regulator 1. A high logic on Enable 1 (EN1) activates regulator 1 while a low logic deactivates regulator 1. MIC2230 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start-up.

4.4 EN2

Enable 2 controls the on and off state of regulator 2. A high logic on Enable 2 (EN2) activates regulator 2 while a low logic deactivates regulator 2. MIC2230 features built-in soft-start circuitry that reduces in-rush current and prevents the output voltage from overshooting at start-up.

4.5 /FPWM

The Forced PWM Mode selects the mode of operation for this device. Grounding this pin forces the device to stay in constant frequency PWM mode only. Pulling this pin high enables automatic selection of Trickle or PWM mode operation, depending on the load. While /FPWM is high and the load is below 100 mA, the device will go into Trickle Mode. If the load is above 100 mA, PWM mode will automatically be selected. Do not leave this pin floating.

4.6 PGOOD

The Power Good Output is pulled down unless the regulator 1 output voltage is within +6.25% or -8.5% of regulation. When the output voltage is in regulation, the PGOOD capacitor will be charged to AV_{IN} by an internal 5 μ A current source through a 1 k Ω resistor. The charge time is approximately 1 μ s per 1 pF of capacitance. For example, a 390 pF capacitor at the PGOOD pin will cause the PGOOD pin voltage to rise from low to high in around 390 μ s. A PGOOD capacitor

is recommended to prevent large output voltage transients from triggering the PGOOD flag unexpectedly.

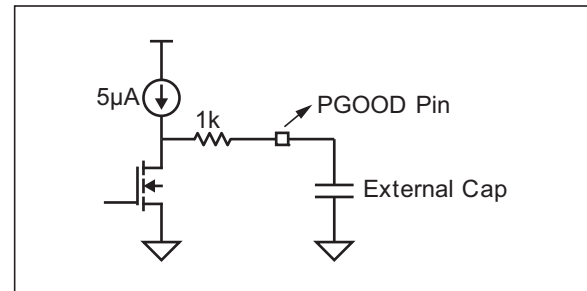


FIGURE 4-1: Power Good Circuit.

4.7 FB1/FB2

The feedback pin (FB) provides the control path to control the output. For adjustable versions, a resistor divider connecting the feedback to the output is used to adjust the desired output voltage. The output voltage is calculated as follows:

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left(\frac{R1}{R2} + 1 \right)$$

Where:

$$V_{REF} = 0.8V$$

The external feedback resistors add some quiescent current consumption for adjustable versions. To reduce battery current draw, high resistance values are recommended in the feedback divider. A feedforward capacitor should be connected between the output and feedback (across R1) because of the high resistance value. The large resistor value and the parasitic capacitance of the FB pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feedforward capacitor, these effects can be significantly reduced. Refer to the [Feedback](#) section for recommended feedforward capacitor values.

4.8 SW1/SW2

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

4.9 PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop.

4.10 AGND

Signal ground (AGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop.

5.0 APPLICATION INFORMATION

5.1 Input Capacitor

A minimum 2.2 μF ceramic is recommended on the V_{IN} pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics, aside from losing most of their capacitance over temperature, they also become resistive at high frequencies. This reduces their ability to filter out high frequency noise.

5.2 Output Capacitor

The MIC2230 was designed specifically for use with a 10 μF or greater ceramic output capacitor. The output capacitor requires either an X7R or X5R dielectric. Y5V and Z5U dielectric capacitors, aside from the undesirable effect of their wide variation in capacitance over temperature, become resistive at high frequencies.

5.3 Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance):

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC2230 was designed for use with a 2.2 μH inductor.

Maximum current ratings of the inductor are generally given in two methods: permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10 to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor.

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss. Refer to the [Efficiency Considerations](#).

5.4 Compensation

The MIC2230 is an internally compensated, current mode buck regulator. Current mode is achieved by sampling the peak current and using the output of the error amplifier to pulse width modulate the switch node and maintain output voltage regulation.

The MIC2230 is designed to be stable with a 2.2 μH inductor with a 10 μF ceramic (X5R) output capacitor.

5.5 Feedback

The MIC2230 provides a feedback pin to adjust the output voltage to the desired level. This pin connects internally to an error amplifier. The error amplifier then compares the voltage at the feedback to the internal 0.8V reference voltage and adjusts the output voltage to maintain regulation. Calculating the resistor divider network for the desired output is shown in [Equation 5-1](#).

EQUATION 5-1:

$$R2 = \frac{R1}{\left(\frac{V_{OUT}}{V_{REF}} - 1\right)}$$

Where:

| | | |
|-----------|---|------------------------|
| V_{REF} | = | 0.8V |
| V_{OUT} | = | Desired Output Voltage |

For adjustable versions, the FB bias current (10 nA typical) should be a negligible fraction of the current flowing in the feedback resistor divider. This improves the accuracy of the output voltage setting. A small current, in the range of a few microamperes, is typically sufficient and does not significantly increase the operating quiescent current in battery-operated applications. This choice leads to high resistance values.

If operating quiescent current is less of a concern, lower resistance values can be used. Larger resistor values require an additional capacitor (feed-forward) from the output to the feedback. The large high-side resistor value and the parasitic capacitance on the feedback pin (~10 pF) can cause an additional pole in the control loop. The additional pole can create a phase loss at high frequencies. This phase loss degrades transient response by reducing phase margin. Adding feed-forward capacitance negates the parasitic capacitive effects of the feedback pin. See [Table 5-1](#) for recommended feedforward capacitor values.

TABLE 5-1: RECOMMENDED FEED-FORWARD CAPACITOR

| Recommended C_{FF} | Total Feedback Resistance |
|----------------------|---------------------------------|
| 22 pF | 1 M Ω - 2 M Ω |
| 47 pF | 500 k Ω - 1 M Ω |
| 100 pF | 100 k Ω - 500 k Ω |
| 180 pF | 10 k Ω - 100 k Ω |

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Large feedback resistor values increase impedance, making the feedback node more susceptible to noise pick-up. A feed forward capacitor would also reduce noise pick-up by providing a low impedance path to the output. Refer to [Table 5-1](#) for recommended feedforward capacitor values

5.6 Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

EQUATION 5-2:

$$\text{Efficiency}_{\%} = \left(\frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} \right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters: DC losses and switching losses. DC losses are simply the power dissipation of I^2R . Power is dissipated in the high-side switch during the on cycle. Power loss is equal to the high side MOSFET $R_{DS(ON)}$ multiplied by the Switch Current². During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss. The current required driving the gates on and off at a constant 2.5 MHz frequency and the switching transitions make up the switching losses.

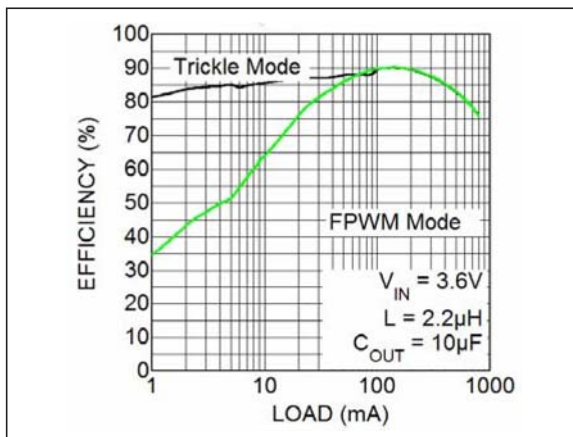


FIGURE 5-1: MIC2230 Efficiency
 $V_{OUT} = 1.575$.

The figure above shows an efficiency curve. From no load to 100 mA, efficiency losses are dominated by quiescent current losses, gate drive and transition losses. By forcing the MIC2230 into Trickle Mode (/FPWM = High), the buck regulator significantly reduces the required switching current by entering into a PFM (Pulse Frequency Modulation) mode. This significantly increases efficiency at low output currents.

Over 100 mA, efficiency loss is dominated by MOSFET $R_{DS(ON)}$ and inductor losses. Higher input supply voltages will increase the Gate-to-Source threshold on the internal MOSFETs, reducing the internal $R_{DS(ON)}$. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as shown in Equation 5-3.

EQUATION 5-3:

$$L_{Pd} = I_{OUT}^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as shown in Equation 5-4.

EQUATION 5-4:

$$\text{Efficiency}_{Loss} = \left[1 - \left(\frac{V_{OUT} \times I_{OUT}}{V_{OUT} \times I_{OUT} + L_{Pd}} \right) \right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

5.7 Trickle Mode Operation

Trickle Mode operation is achieved by clamping the minimum peak current to approximately 150 mA. This forces a PFM mode by comparing the output voltage to the internal reference. If the feedback voltage is less than 0.8V, the MIC2230 turns on the high side until the peak inductor current reaches approximately 150 mA. A separate comparator then monitors the output voltage. If the feedback voltage is greater than 0.8V, the high side switch is then used as a 10 μ A current source, never turning off completely. This creates a highly efficient light load mode by increasing the time it takes for the output capacitor to discharge, delaying the amount of switching required and increasing light load efficiency. While operating in this mode without any load, the output voltage may rise over the nominal operating voltage range. For applications that require tight voltage tolerances, a minimum load of 150 μ A is recommended.

This load may either be used by the attached system, by lowering the feedback resistors or by adding an additional load resistor in parallel with the output capacitor.

MIC2230

When the load current is greater than approximately 100 mA, the MIC2230 automatically switches to PWM mode.

5.8 FPWM Operation

In forced PWM Mode (/FPWM = LOW) the MIC2230 is forced to provides constant switching at 2.5 MHz with synchronous internal MOSFETs throughout the load current. In FPWM Mode, the output ripple can be as low as 7 mV.

6.0 MIC2230 EVALUATION BOARD SCHEMATIC

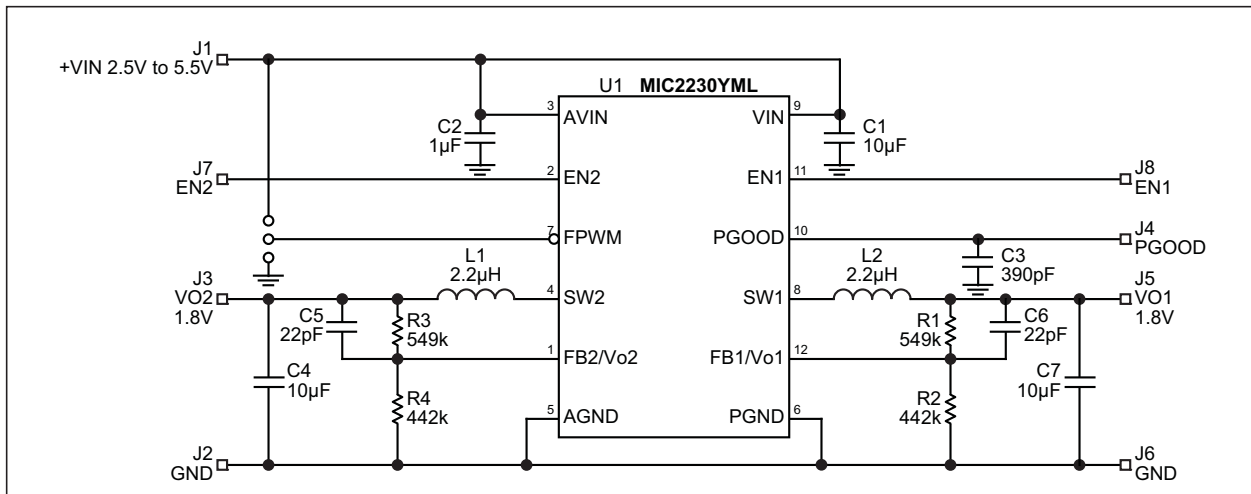


FIGURE 6-1: MIC2230 Adjustable Option (1.8V, 1.8V).

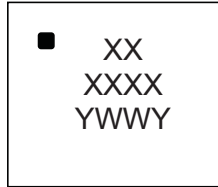
TABLE 6-1: BILL OF MATERIALS

| Item | Part Number | Manufacturer | Description | Qty |
|--------|----------------------|--------------|--|-----|
| C1 | C1608X5R0J106K | TDK | 10 µF Ceramic Capacitor, 6.3V, X5R, Size 0603 | 1 |
| C2 | C1005X5R0J105K | TDK | 1 µF Ceramic Capacitor, 6.3V, X5R, Size 0402 | 1 |
| C3 | C0603Y391KXXA | Vishay | 390 pF Ceramic Capacitor, 25V, X7R, Size 0603 | 1 |
| C4, C5 | 0603ZD106MAT | AVX | 10 µF Ceramic Capacitor, 6.3V, X5R, Size 0603 | 2 |
| L1, L2 | CDRH2D11/HPNP-2 R2NC | Sumida | 2.2 µH, 1.1A I _{SAT} , 120 mΩ, (1.2 mm × 3.2 mm × 3.2 mm) | 2 |
| | LQH43CN2R2M03 | Murata | 2.2 µH, 900 mA I _{SAT} , 110 mΩ, (2.6 mm × 3.2 mm × 4.5 mm) | |
| | EPL2014-222MLB | Coilcraft | 2.2 µH, 1.3A I _{SAT} , 120 mΩ, (1.4 mm × 1.8 mm × 2.0 mm) | |
| R2, R4 | CRCW06034423FT1 | Vishay | 442 kΩ, 1%, Size 0603 | 2 |
| R1, R3 | CRCW06035493FT1 | Vishay | 549 kΩ, 1%, Size 0603 | 2 |
| U1 | MIC2230-AAYML | Microchip | 2.5 MHz Dual Phase PWM Buck Regulator | 1 |
| L1, L2 | CDRH2D11/HPNP-2 R2NC | Sumida | 2.2 µH, 1.1A I _{SAT} , 120 mΩ, (1.2 mm × 3.2 mm × 3.2 mm) | 2 |

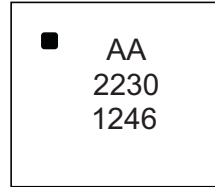
7.0 PACKAGING INFORMATION

7.1 Package Marking Information

12-lead QFN*



Example

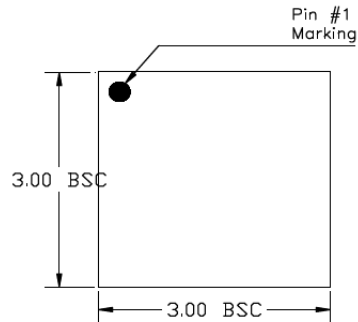


| | | |
|----------------|--|--|
| Legend: | XX...X | Product code or customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package. |
| | ●, ▲, ▼ | Pin one index is identified by a dot, delta up, or delta down (triangle mark). |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo. | |
| | Underbar (̄) and/or Overbar (¯) symbol may not be to scale. | |

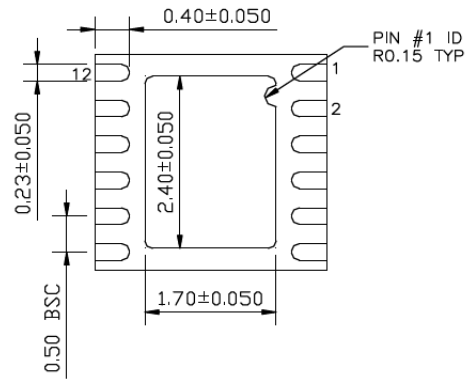
TITLE

12 LEAD DFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

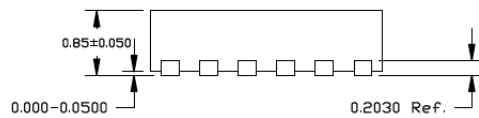
| DRAWING # | DFN33-12LD-PL-1 | UNIT | MM |
|-----------|-----------------|------|----|
|-----------|-----------------|------|----|



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3



SIDE VIEW
NOTE: 1, 2, 3

NOTE:

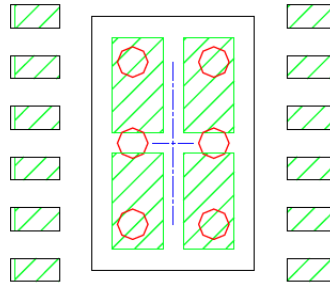
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076 MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.50x0.95 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

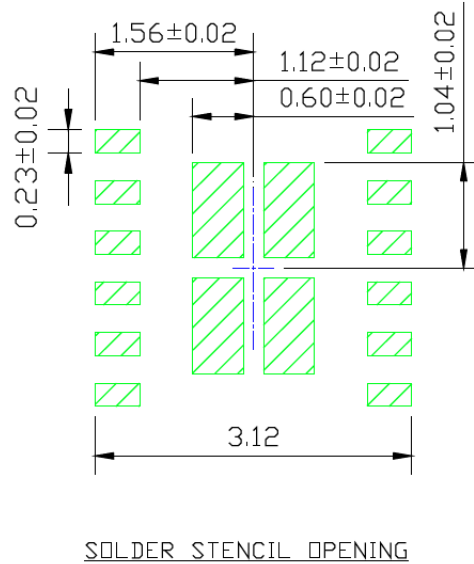
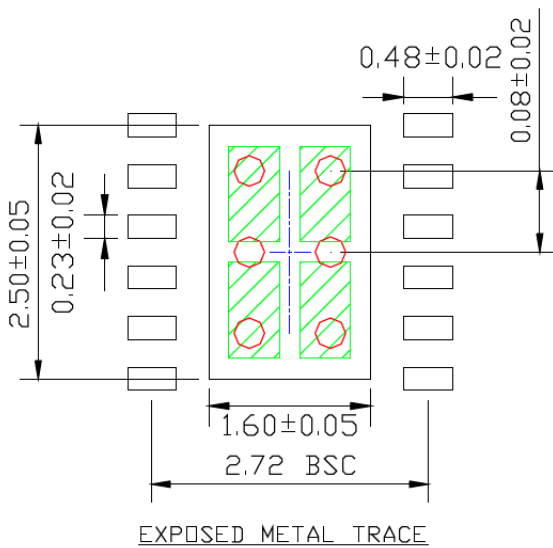
POD-Land Pattern drawing # DFN33-12LD-PL-1

RECOMMENDED LAND PATTERN

NOTE: 4, 5



STACKED-UP



Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.

APPENDIX A: REVISION HISTORY

Revision A (April 2017)

- Converted Micrel document MIC2230 to Microchip data sheet template DS20005748A.
- Minor grammatical text changes throughout.

MIC2230

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>-XX</u> | <u>X</u> | <u>XX</u> | Examples: |
|---|-----------------------|--|----------------|---|
| Device | Output Voltage | Temperature Range | Package | |
| Device: | MIC2230: | Dual Synchronous 800 mA/800 mA Step-Down DC/DC Regulator | | a) MIC2230-AAYML TR: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, Adjustable Output Voltage, -40°C to +125°C, 12LD TDFN, Tape and Reel |
| Output Voltages: (V _{OUT1} , V _{OUT2}) | AA = | Adjustable | | b) MIC2230-G4YML TR: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 1.8V/1.2V Output Voltage, -40°C to +125°C, 12LD TDFN, Tape and Reel |
| | G4 = | 1.8V / 1.2V | | c) MIC2230-GFHYML TR: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 1.8V/1.575V Output Voltage, -40°C to +125°C, 12LD TDFN |
| | GFH = | 1.8V / 1.575V | | d) MIC2230-GSYML: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 1.8V/3.3V Output Voltage, -40°C to +125°C, 12LD TDFN |
| | GS = | 1.8V / 3.3V | | e) MIC2230-J4YML: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 2.5V/1.2V Output Voltage, -40°C to +125°C, 12LD TDFN |
| | J4 = | 2.5V / 1.2V | | f) MIC2230-S4YML: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 3.3V/1.2V Output Voltage, -40°C to +125°C, 12LD TDFN |
| | S4 = | 3.3V / 1.2V | | g) MIC2230-SSYML: Dual Synchronous 800 mA/800 mA, Step-Down DC/DC Regulator, 3.3V/3.3V Output Voltage, -40°C to +125°C, 12LD TDFN |
| | SS = | 3.3V / 3.3V | | |
| Temperature Range: | Y = | -40°C to +125°C | | |
| Packages: | ML = | 12-Lead, 3 mm × 3 mm TDFN | | |
| Media Type: | TR = | Tape and Reel; 5000/reel. | | |
| | | | | Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option. |

MIC2230

NOTES:

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