CS5378

Low-power Single-channel Decimation Filter

Features

- Single-channel Digital Decimation Filter
  - Multiple On-chip FIR and IIR Coefficient Sets
  - Programmable Coefficients for Custom Filters
  - Synchronous Operation
- Integrated PLL for Clock Generation
  - 1.024 MHz, 2.048 MHz, or 4.096 MHz Input
  - Standard Clock or Manchester Input
- Selectable Output Word Rate
  - 4000, 2000, 1000, 500, 333, 250 SPS
  - 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS
- Digital Gain and Offset Corrections
- Test DAC Bit-stream Generator
  - Digital Sine Wave Output
- Time Break Controller, General-purpose I/O
- Microcontroller or EEPROM Configuration
- Small-footprint, 28-pin SSOP Package
- Low Power Consumption
  - 16 mW at 500 SPS OWR
- Flexible Power Supplies
  - I/O Interface and PLL: 3.3 V or 5.0 V
  - Digital Logic Core: 2.5 V, 3.3 V or 5.0 V

Description

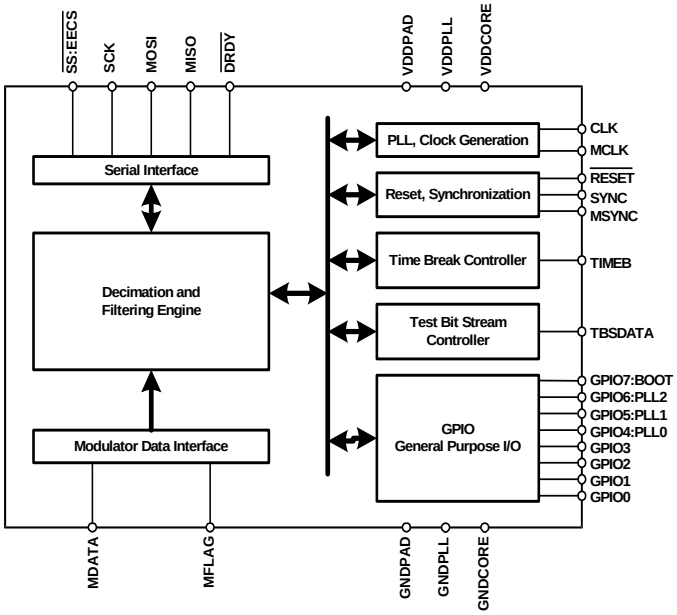
The CS5378 is a multi-function digital filter utilizing a low-power signal processing architecture to achieve efficient filtering for a delta-sigma-type modulator. By combining the CS5378 with a CS3301A/02A differential amplifier and a CS5373A modulator + test DAC, a synchronous high-resolution, self-testing, single-channel measurement system can be designed quickly and easily.

Digital filter coefficients for the CS5378 FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400 mHz when using the on-chip coefficient sets.

The CS5378 includes integrated peripherals to simplify system design: a low-jitter PLL for standard clock or Manchester inputs, offset and gain corrections, a test DAC bit stream generator, a time break controller, and eight general-purpose I/O pins.

ORDERING INFORMATION

See page 86.



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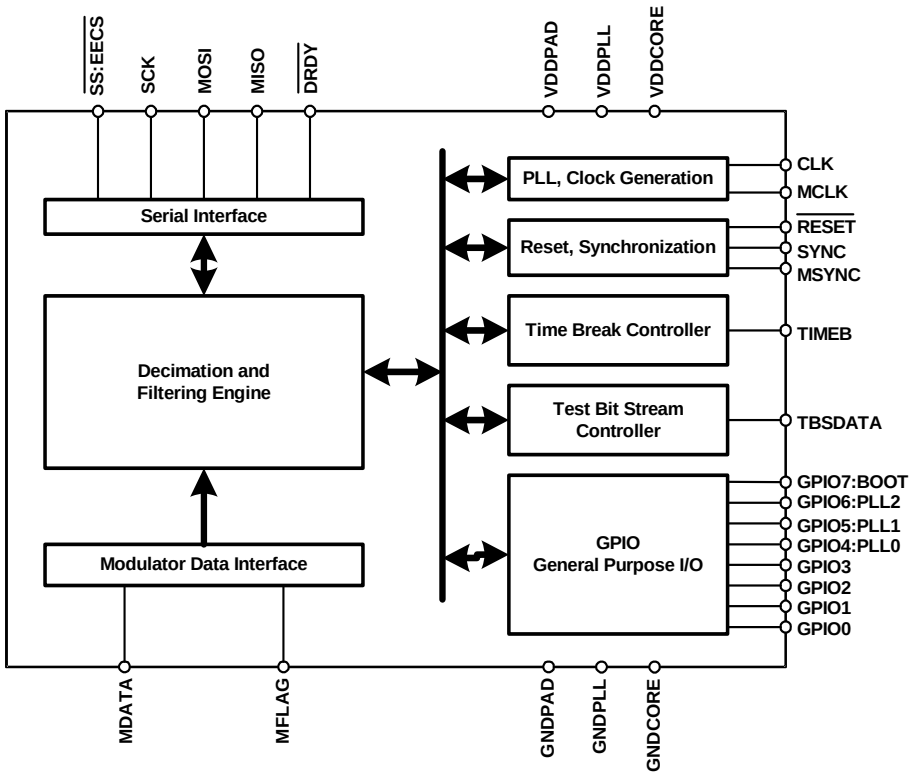


Figure 1. CS5378 Block Diagram

1. GENERAL DESCRIPTION

The CS5378 is a single channel digital filter with integrated system peripherals. Figure 1 illustrates a simplified block diagram of the CS5378.

1.1 Digital Filter Features

- Single channel decimation filter for CS5373A ΔΣ modulator.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - Internal synchronization of digital filter phase to an external SYNC signal.
- Output word rates, including low bandwidth rates.
  - Standard output rates: 4000, 2000, 1000, 500, 333, 250 SPS.
  - Low bandwidth rates: 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS.
- Flexible digital filter configuration. (See Figure 2)
  - Cascaded SINC, FIR, and IIR filters with selectable output stage.
  - Linear and minimum phase FIR low-pass filter coefficients included.
  - 3 Hz Butterworth IIR high-pass filter coefficients included.
  - FIR and IIR coefficients programmable to create a custom filter response.
- Digital gain correction to normalize sensor gain.
- Digital offset correction and calibration.
  - Offset correction to remove measurement

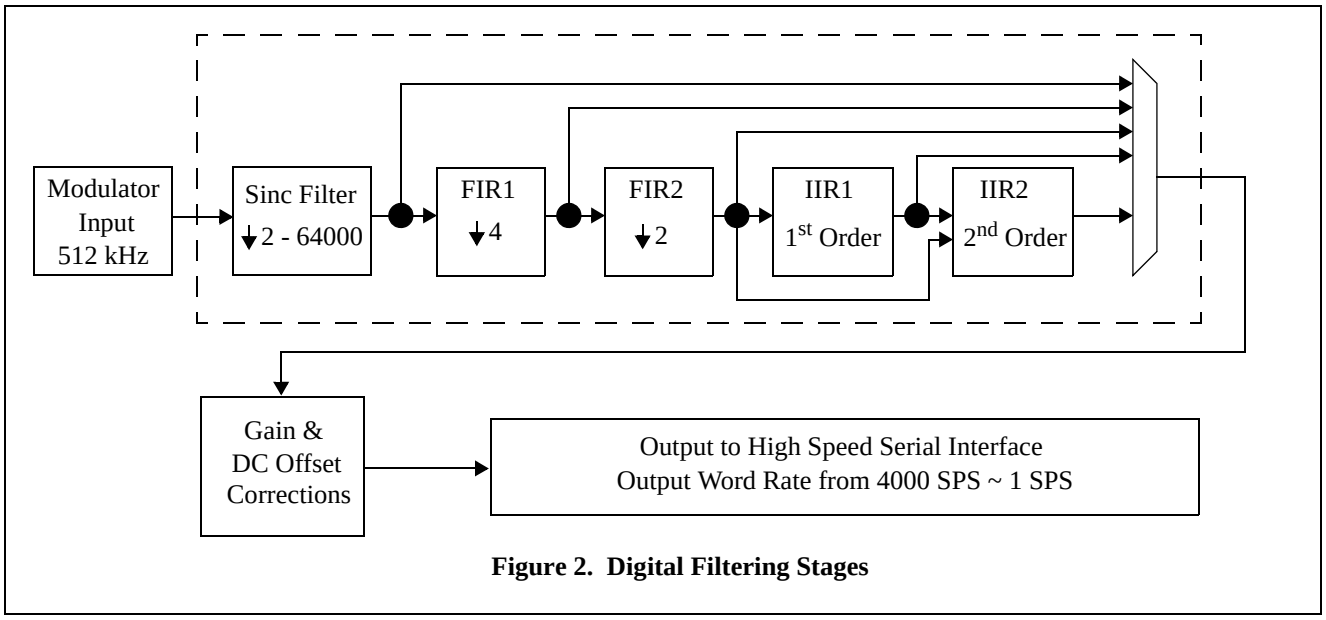


Figure 2. Digital Filtering Stages

DC offset.

- Calibration engine for automatic calculation of offset correction factor.

1.2 Integrated Peripheral Features

- Low jitter PLL to generate local clocks.
  - 1.024 MHz, 2.048 MHz, 4.096 MHz standard clock or Manchester encoded input.
- Synchronous operation for simultaneous sampling in multi-sensor systems.
  - MCLK / MSYNC output signals to synchronize external components.
- High speed serial data output.
  - Asynchronous operation to 4 MHz for direct connection to system telemetry.
  - Internal 8-deep data FIFO for flexible output timing.
  - Selectable 24-bit data only or 32-bit status+data output.
- Digital test bit stream signal generator suitable for CS5373A ΔΣ test DAC.
  - Sine wave output mode for testing total harmonic distortion.
- Time break controller to record system timing information.
  - Dedicated TB status bit in the output data stream.
  - Programmable output delay to match system group delay.
- 8 General Purpose I/O (GPIO) pins for local hardware control.

1.3 System Level Features

- Flexible configuration options.
  - Configuration 'on-the-fly' via microcontroller or system telemetry.
  - Fixed configuration via stand-alone boot EEPROM.
- Low power consumption.
  - 16 mW at 500 SPS OWR.
  - 100 µW standby mode.
- Flexible power supply configurations.
  - Separate digital logic core, telemetry I/O, and PLL power supplies.
  - Telemetry I/O and PLL interfaces operate

from 3.3 V or 5 V.

- Digital logic core operates from 2.5 V, 3.3 V or 5 V.

- Small 28-pin SSOP package.
  - Total footprint 8 mm x 10 mm plus three bypass capacitors.

1.4 Configuration Interface

- Configuration from microcontroller or stand-alone boot EEPROM.
  - Microcontroller boot permits reconfiguration during operation.
  - EEPROM boot sets a fixed operational configuration.
- Configuration commands written through the serial interface. (See Table 1)
  - Standardized microcontroller interface using SPI™ registers. (See Table 3)
  - Commands write digital filter registers and FIR / IIR filter coefficients.
  - Digital filter registers set hardware configuration options.

Microcontroller Boot Configuration Commands

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
NOP	000006	-	-	No Operation
NOP	000007	-	-	No Operation
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

EEPROM Boot Configuration Commands

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
NOP	05	-	No Operation
NOP	06	-	No Operation
FILTER START	07	-	Start Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 1. Microcontroller and EEPROM Configuration Commands

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 3. FIR and IIR Coefficient Set Selection Word

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 2. TBS Configurations Using On-Chip Data

SPI Registers

Name	Addr.	Type	# Bits	Description
SPICTRL	00 - 02	R/W	8, 8, 8	SPI Control
SPICMD	03 - 05	R/W	8, 8, 8	SPI Command
SPIDAT1	06 - 08	R/W	8, 8, 8	SPI Data 1
SPIDAT2	09 - 0B	R/W	8, 8, 8	SPI Data 2

Digital Filter Registers

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG	0E	R/W	24	GPIO[7:0] Direction, Pull-up Enable, and Data
RESERVED	0F-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN	21	R/W	24	Gain Correction
RESERVED	22-24	R/W	24	Reserved
OFFSET	25	R/W	24	Offset Correction
RESERVED	26-28	R/W	24	Reserved
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

Table 3. SPI and Digital Filter Registers

PLL[2:0]	Mode Selection on Reset
111	32.768 MHz clock input (PLL bypass).
110	1.024 MHz clock input.
101	2.048 MHz clock input.
100	4.096 MHz clock input.
011	32.768 MHz clock input (PLL bypass).
010	1.024 MHz Manchester input.
001	2.048 MHz Manchester input.
000	4.096 MHz Manchester input.

BOOT	Mode Selection on Reset
1	EEPROM boot
0	Microcontroller boot

Configuration Note:

States of the PLL[2:0] and BOOT pins are latched immediately after reset to select modes.

These pins have a weak (~100 kΩ) pull-up resistor enabled by default. An external 10 kΩ pull-down is required to set a low condition.

Table 4. PLL and BOOT Mode Reset Configurations

2. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the Specified Operating Conditions.
- Typical performance characteristics and specifications are derived from measurements taken at nominal supply voltages and T_A = 25°C.
- GND, GND1, GND2 = 0 V, all voltages with respect to 0 V.

SPECIFIED OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Logic Core Power Supply		VDDCORE	2.375	2.5	5.25	V
PLL Power Supply		VDDPLL	3.135	3.3	5.25	V
I/O Power Supply		VDDPAD	3.135	3.3	5.25	V
Ambient Operating Temperature	Industrial (-IQ)	T_A	-40	-	85	°C

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Min	Max	Units
DC Power Supplies	Logic Core	VDDCORE	-0.3	6.0	V
	PLL	VDDPLL	-0.3	6.0	V
	I/O	VDDPAD	-0.3	6.0	V
Input Current, Any Pin Except Supplies	(Note 1)	I_{IN}	-	±10	mA
Input Current, Power Supplies	(Note 1)	I_{IN}	-	±50	mA
Output Current	(Note 1)	I_{OUT}	-	±25	mA
Power Dissipation		P_{DN}	-	500	mW
Digital Input Voltages		V_{IND}	-0.3	VDD+0.3	V
Ambient Operating Temperature (Power Applied)		T_A	-40	85	°C
Storage Temperature Range		T_{STG}	-65	150	°C

1. Transient currents up to 100 mA will not cause SCR latch-up.

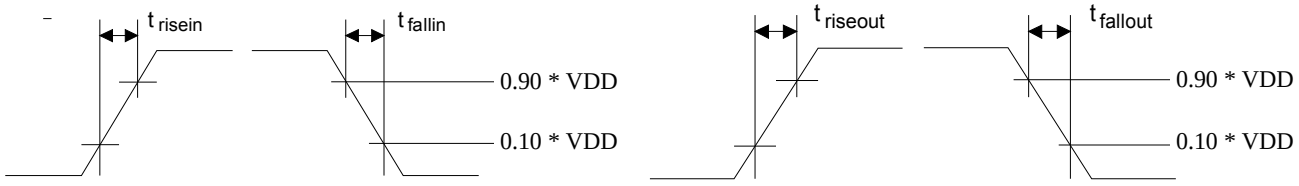
THERMAL CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Allowable Junction Temperature	T_J	-	-	135	°C
Junction to Ambient Thermal Impedance (4-Layer PCB)	Θ_{JA}	-	50		°C / W
Ambient Operating Temperature (Power Applied)	T_A	-40	-	+85	°C

DIGITAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Drive Voltage		V_{IH}	0.6 * VDD	-	VDD	V
Low-Level Input Drive Voltage		V_{IL}	0.0	-	0.8	V
High-Level Output Drive Voltage	I_{out} = -40 µA	V_{OH}	VDD - 0.3	-	VDD	V
Low-Level Output Drive Voltage	I_{out} = +40 µA	V_{OL}	0.0	-	0.3	V
Rise Times, Digital Inputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Inputs		t_{FALL}	-	-	100	ns
Rise Times, Digital Outputs		t_{RISE}	-	-	100	ns
Fall Times, Digital Outputs		t_{FALL}	-	-	100	ns
Input Leakage Current	(Note 2)	I_{IN}	-	±	± 10	µA
3-State Leakage Current		I_{OZ}	-	-	± 10	µA
Digital Input Capacitance		C_{IN}	-	9	-	pF
Digital Output Pin Capacitance		C_{OUT}	-	9	-	pF

Notes: 2. Maximum leakage for pins with pull-up resistors ($\overline{\text{RESET}}$, $\overline{\text{SS:EECS}}$, GPIO, MOSI, SCK) is ±250 µA.



POWER CONSUMPTION

Parameter	Symbol	Min	Typ	Max	Unit
Operational Power Consumption					
1.024 MHz Digital Filter Clock	PWR_1	-	12	-	mW
2.048 MHz Digital Filter Clock	PWR_2	-	14	-	mW
4.096 MHz Digital Filter Clock	PWR_4	-	16	-	mW
8.192 MHz Digital Filter Clock	PWR_8	-	24	-	mW
Standby Power Consumption					
32 kHz Digital Filter Clock, Filter Stopped	PWR_S	-	100	-	µW

SWITCHING CHARACTERISTICS

Serial Configuration Interface Timing (External Master)

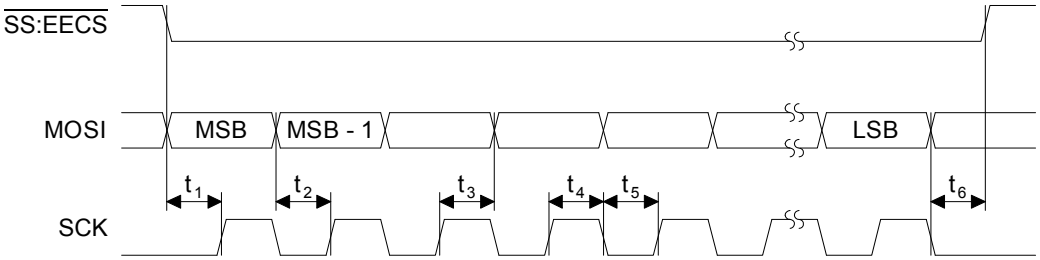


Figure 4. MOSI Write Timing in SPI Slave Mode

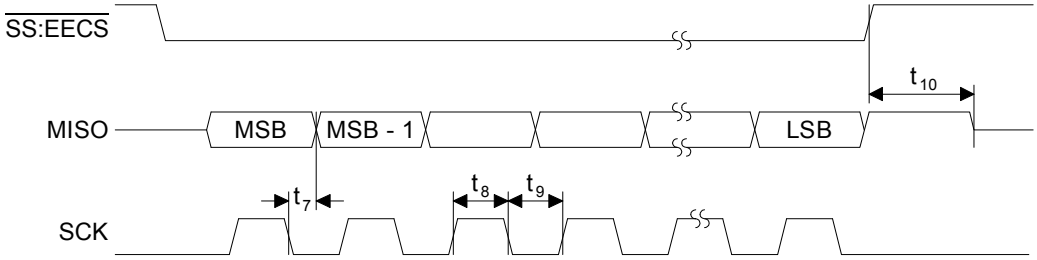


Figure 5. MISO Read Timing in SPI Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
MOSI Write Timing					
$\overline{\text{SS:EECS}}$ Enable to Valid Latch Clock	t_1	60	-	-	ns
Data Set-up Time Prior to SCK Rising	t_2	60	-	-	ns
Data Hold Time After SCK Rising	t_3	120	-	-	ns
SCK High Time	t_4	120	-	-	ns
SCK Low Time	t_5	120	-	-	ns
SCK Falling Prior to $\overline{\text{SS:EECS}}$ Disable	t_6	60	-	-	ns
MISO Read Timing					
SCK Falling to New Data Bit	t_7	-	-	60	ns
SCK High Time	t_8	120	-	-	ns
SCK Low Time	t_9	120	-	-	ns
$\overline{\text{SS:EECS}}$ Rising to MISO Hi-Z	t_{10}	-	-	150	ns

SWITCHING CHARACTERISTICS

Serial Data Interface Timing

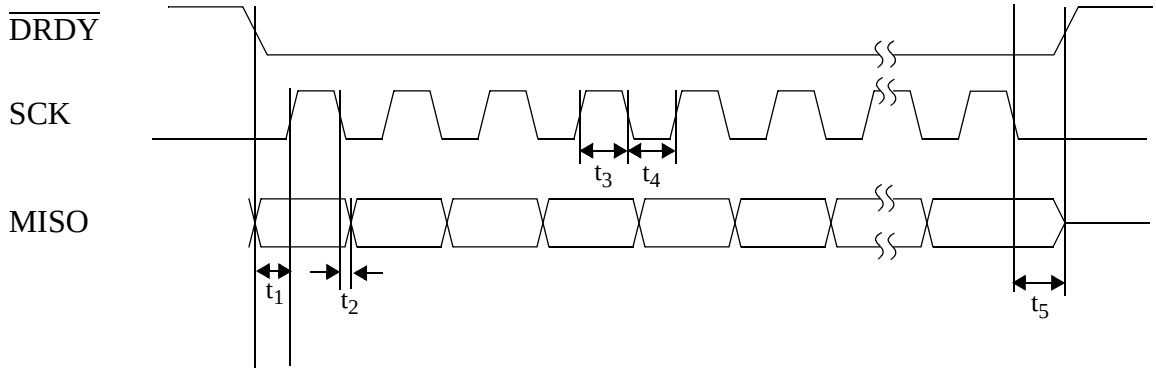
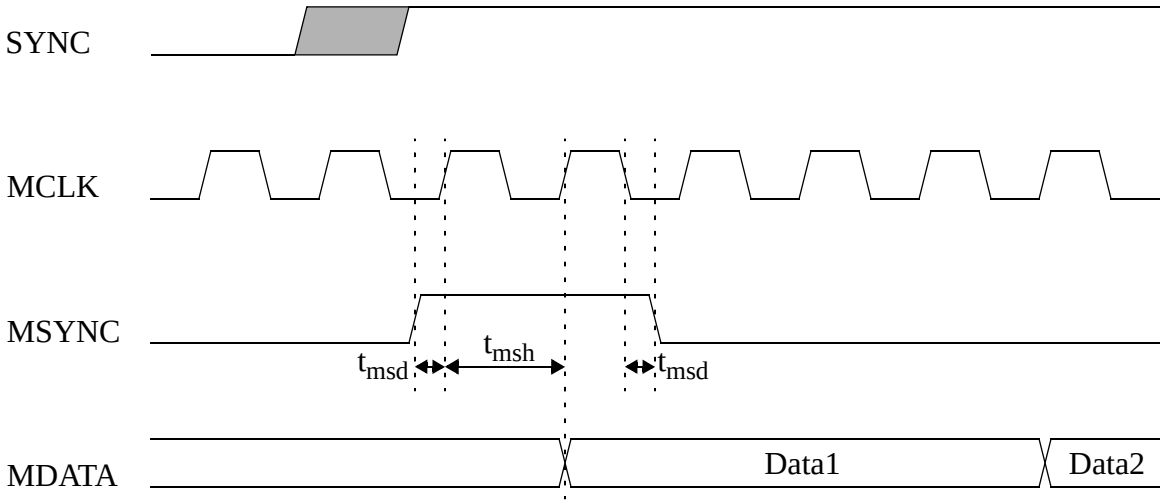


Figure 6. Serial Data Read Timing

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{DRDY}}$ Falling Edge to SCK Rising	t_1	60	-	-	ns
SCK Falling to New Data Bit	t_2	-	-	120	ns
SCK High Time	t_3	120	-	-	ns
SCK Low Time	t_4	120	-	-	ns
Final SCK Falling to $\overline{\text{DRDY}}$ Rising	t_5	60	-	-	ns

SWITCHING CHARACTERISTICS

CLK, SYNC, MCLK, MSYNC, and MDATA



Note: SYNC input latched on MCLK rising edge. MSYNC output triggered by MCLK falling edge.

f_{MCLK}	2.048 MHz	1.024 MHz
$t_{msd} = T_{MCLK} / 4$	t_{msd} = 122 ns	t_{msd} = 244 ns
$t_{msh} = T_{MCLK}$	t_{msh} = 488 ns	t_{msh} = 976 ns

Figure 7. SYNC, MCLK, MSYNC, MDATA Interface Timing

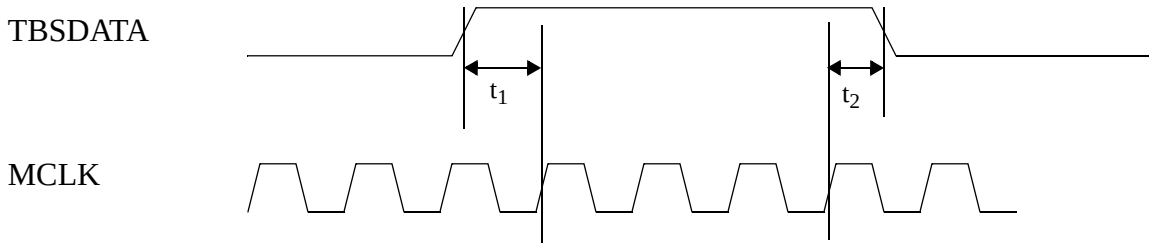
Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	(Note 3)	CLK	32	32.768	33	MHz
Master Clock Duty Cycle		DTY	40	-	60	%
Master Clock Rise Time		t_{RISE}	-	-	20	ns
Master Clock Fall Time		t_{FALL}	-	-	20	ns
Master Clock Jitter		JTR	-	-	300	ps
Synchronization after SYNC rising	(Note 4)	SYNC	-2	-	2	µs
MSYNC Setup Time to MCLK rising		t_{mss}	20	-	-	ns
MCLK rising to Valid MDATA		t_{mdv}	-	-	75	ns
MSYNC falling to MCLK rising		t_{msf}	20	-	-	ns

Notes: 3. PLL bypass mode. The PLL generates a 32.768 MHz master clock when enabled.

4. Sampling synchronization between multiple CS5378 devices receiving identical SYNC signals.

SWITCHING CHARACTERISTICS

Test Bit Stream (TBS)



Note: Example timing shown for a 256 kHz output rate and no programmable delays.

Figure 8. TBS Output Data Timing

Parameter	Symbol	Min	Typ	Max	Unit
TBS Data Output Timing					
TBS Data Bit Rate		-	256	-	kbps
TBS Data Rising to MCLK Rising Setup Time	t_1	60	-	-	ns
MCLK Rising to TBS Data Falling Hold Time (Note 5)	t_2	60	-	-	ns

5. TBSDATA can be delayed from 0 to 63 full bit periods. The timing diagram shows no TBSDATA delay.

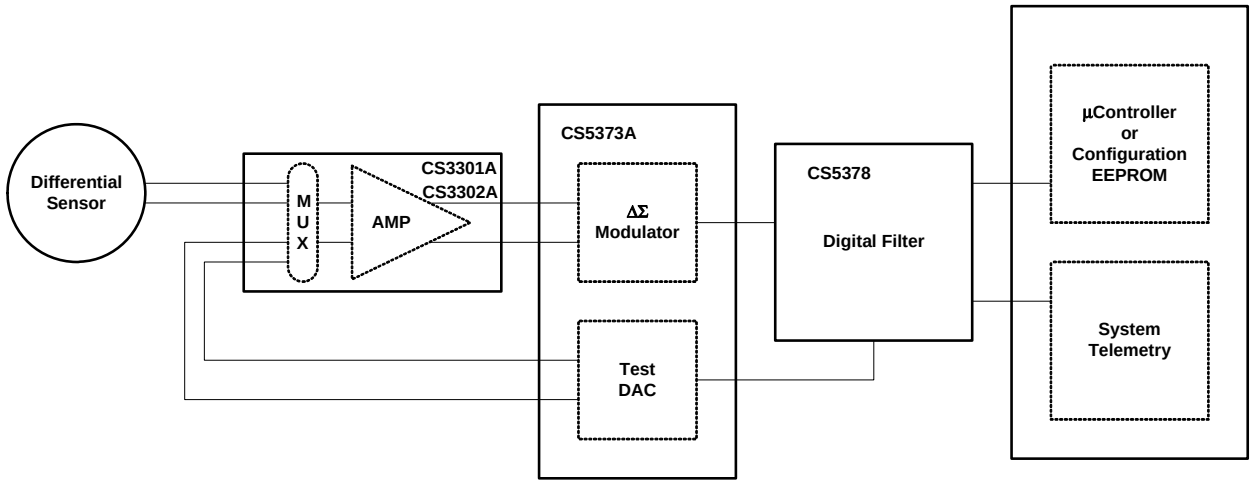


Figure 9. Single-Channel System Block Diagram

3. SYSTEM DESIGN WITH CS5378

Figure 9 illustrates a simplified block diagram of the CS5378 in a single channel measurement system.

A differential sensor is connected through the CS3301A/02A differential amplifiers to the CS5373A ΔΣ modulator, where analog to digital conversion occurs. The modulator's 1-bit output connects to the CS5378 MDATA input, where the oversampled ΔΣ data is decimated and filtered to 24-bit output samples at a programmed output rate. These output samples are buffered into an 8-deep data FIFO and then passed to the system telemetry.

System self tests are performed by connecting the CS5378 test bit stream (TBS) generator to the CS5373A test DAC. Analog tests drive differential signals from the CS5373A test DAC into the multiplexed inputs of the CS3301A/02A amplifiers or directly to the differential sensor. Digital loopback tests internally connect the TBS digital output directly to the CS5378 modulator input.

3.1 Power Supplies

The system shown in Figure 9 typically operates from a ±2.5 V analog power supply and a 3.3 V digital power supply. The CS5378 logic core can be powered from 2.5 V to minimize power consumption, if required.

3.2 Reset Control

System reset is required only for the CS5378 device, and is a standard active low signal that can be generated by a power supply monitor or microcontroller. Other system devices default to a power-down state when the CS5378 is reset.

3.3 PLL and Clock Generation

A PLL is included on the CS5378 to generate an internal 32.768 MHz master clock from a 1.024 MHz, 2.048 MHz, or 4.096 MHz standard clock or Manchester encoded input. Clock inputs for other system devices are driven by clock outputs from the CS5378.

3.4 Synchronization

Digital filter phase and analog sample timing of the ΔΣ modulator connected to the CS5378 are synchronized by a rising edge on the SYNC pin. If a synchronization signal is received identically by all CS5378 devices in a measurement network, synchronous sampling across the network is guaranteed.

3.5 System Configuration

Through the serial configuration interface, filter coefficients and digital filter register settings can either be programmed by a microcontroller or automatically loaded from an external EEPROM after reset. System configuration is only required for the CS5378 device, as other devices are configured via the CS5378 General Purpose I/O pins.

Two registers in the digital filter, SYSTEM1 and SYSTEM2 (0x2C, 0x2D), are provided for user defined system information. These are general purpose registers that will hold any 24-bit data values written to them.

3.6 Digital Filter Operation

After analog to digital conversion occurs in the modulator, the oversampled 1-bit ΔΣ data is read into the CS5378 through the MDATA pin. The digital filter then processes data through the enabled filter stages, decimating it to 24-bit words at a programmed output word rate. The final 24-bit samples are concatenated with 8-bit status words and placed into an output FIFO.

3.7 Data Collection

Data is collected from the CS5378 through the serial data interface. When data is available, serial transactions are automatically initiated to transfer 24-bit data or 32-bit status+data from the output FIFO to the system telemetry. The output FIFO has eight data locations to permit latency in data collection.

3.8 Integrated peripherals

Test Bit Stream (TBS)

A digital signal generator built into the CS5378 produces a 1-bit ΔΣ sine wave. This digital test bit stream is connected to the CS5373A test DAC to create high quality analog test signals or internally looped back to the CS5378 MDATA input to test the digital filter and data collection circuitry.

Time Break

Timing information is recorded during data collection by strobing the TIMEB pin. A dedicated flag in the sample status bits, TB, is set high to indicate during which measurement the timing event occurred.

General Purpose I/O (GPIO)

Eight general purpose pins are available on the CS5378 for system control. Each pin can be set as input or output, high or low, with an internal pull-up enabled or disabled. The CS3301A/02A and CS5373A devices in Figure 9 are configured by simple pin settings controlled through the CS5378 GPIO pins.

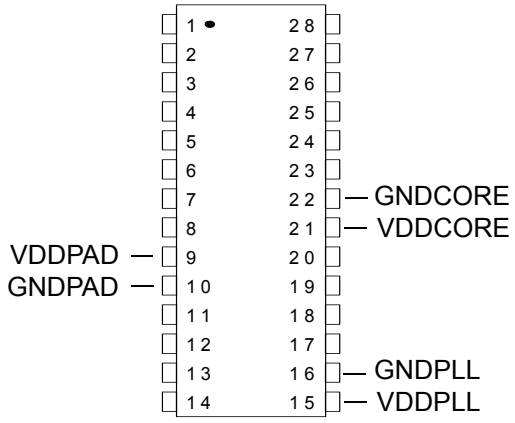


Figure 10. Power Supply Block Diagram

4. POWER SUPPLIES

The CS5378 has three sets of power supply inputs. One set supplies power to the I/O pins of the device (VDDPAD), another supplies power to the logic core (VDDCORE) and the third supplies power to the PLL (VDDPLL). The I/O pin power supplies determine the maximum input and output voltages when interfacing to peripherals, the logic core power supply largely determines the power consumption of the CS5378 and the PLL power supply powers the internal PLL circuitry.

4.1 Pin Descriptions

VDDPAD, GNDPAD - Pins 9, 10

Sets the interface voltage to a microcontroller, system telemetry, modulator, and test DAC. VDDPAD can be driven with voltages from 3.3 V to 5 V.

VDDPLL, GNDPLL - Pins 15, 16

Sets the operational voltage of the internal CS5378 PLL circuitry. Can be driven with voltages from 3.3 V to 5 V.

VDDCORE, GNDCORE - Pins 21, 22

Sets the operational voltage of the CS5378 logic core. VDDCORE can be driven with voltages from 2.5 V to 5 V. A 2.5 V supply will minimize total power consumption.

4.2 Bypass Capacitors

Each power supply pin should be bypassed with parallel 1 µF and 0.01 µF caps, or by a single 0.1 µF cap, placed as close as possible to the CS5378. Bypass capacitors should be ceramic (X7R, C0G), tantalum, or other good quality dielectric type.

4.3 Power Consumption

Power consumption of the CS5378 depends primarily on the power supply voltage of the logic core (VDDCORE) and the programmed digital filter clock rate. Digital filter clock rates are selected based on the required output word rate as explained in “Digital Filter Initialization” on page 38.

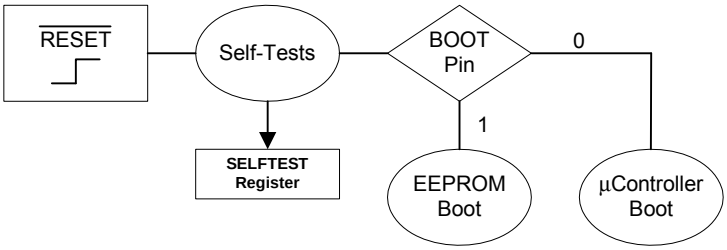


Figure 11. Reset Control Block Diagram

5. RESET CONTROL

The CS5378 reset signal is active low. When released, a series of self-tests are performed and the device either actively boots from an external EEPROM or enters an idle state waiting for microcontroller configuration.

5.1 Pin Descriptions

$\overline{RESET}$ - Pin 18

Reset input, active low.

GPIO7:BOOT - Pin 28

Boot mode select, latched immediately following reset. Weak (~100 kΩ) internal pull-up defaults high, external 10 kΩ pull-down required to set low.

BOOT	Reset Mode
1	EEPROM boot
0	Microcontroller boot

5.2 Reset Self-Tests

After $\overline{RESET}$ is released but before booting, a series of digital filter self-tests are run. Results are combined into the SELFTEST register (0x2F), with 0x0AAAAA indicating all passed. Self-tests require 60 ms to complete.

Self-Test Type	Pass Code	Fail Code
Program ROM	0x00000A	0x00000F
Data ROM	0x0000A0	0x0000F0
Program RAM	0x000A00	0x000F00
Data RAM	0x00A000	0x00F000
Execution Unit	0x0A0000	0x0F0000

5.3 Boot Configurations

The logic state of the BOOT pin after reset determines if the CS5378 actively reads configuration information from EEPROM or enters an idle state waiting for a microcontroller to write configuration commands.

EEPROM Boot

When the BOOT pin is high after reset, the CS5378 actively reads data from an external serial EEPROM and then begins operation in the specified configuration. Configuration commands and data are encoded in the EEPROM as specified in the 'Configuration By EEPROM' section of this data sheet, starting on page 25.

Microcontroller Boot

When the BOOT pin is low after reset, the CS5378 enters an idle state waiting for a microcontroller to write configuration commands and initialize filter operation. Configuration commands and data are written as specified in the 'Configuration By Microcontroller' section of this data sheet, starting on page 30.

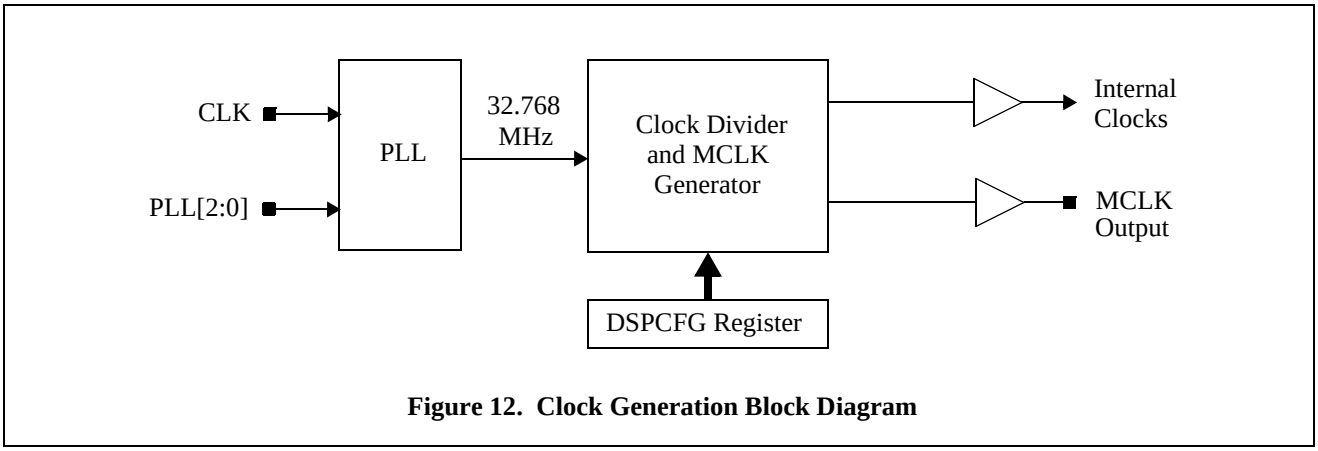


Figure 12. Clock Generation Block Diagram

6. PLL AND CLOCK GENERATION

The CS5378 requires a 32.768 MHz master clock, which can be supplied directly or from an internal phase locked loop. This master clock is used to generate an internal digital filter clock and an external modulator clock.

The internal PLL will lock to standard clock or Manchester encoded input signals. The input type and input frequency are selected by the reset state of the PLL mode select pins.

6.1 Pin Descriptions

CLK - Pin 17

Clock or PLL input, standard clock or Manchester.

GPIO[4:6]:PLL[0:2] - Pins 5, 6, 7

PLL mode select, latched immediately after reset. Weak (~100 kΩ) internal pull-ups default high, external 10 kΩ pull-downs required to set low.

6.2 PLL Mode Select

The CS5378 PLL operational mode and frequency are selected immediately after reset based on the state of the PLL[0:2] pins. On the rising edge of the reset signal, the digital high or low state of the PLL[0:2] pins is latched and used to program the clock input type and frequency.

A weak internal pull-up resistor (~100 kΩ) will hold the PLL mode select pins high by default. To force the pin low on reset, an external 10 kΩ pull-down resistor should be connected. Once the pin state is latched following reset, the GPIO[4:6] pins function without affecting PLL operation.

6.3 Synchronous Clocking

To guarantee synchronous measurements throughout a sensor network, a system clock should be distributed to arrive at all nodes in phase. The distributed system clock can either be the full 32.768 MHz master clock, or the CS5378 PLL can create a synchronous 32.768 MHz clock from a slower clock. To ensure the generated clock remains synchronous with the network, the CS5378 PLL uses a phase/frequency detector architecture.

PLL[2:0]	PLL Mode
111	32.768 MHz clock input (PLL bypass).
110	1.024 MHz clock input.
101	2.048 MHz clock input.
100	4.096 MHz clock input.
011	32.768 MHz clock input (PLL bypass).
010	1.024 MHz Manchester input.
001	2.048 MHz Manchester input.
000	4.096 MHz Manchester input.

Table 5. PLL Mode Selections

6.4 Master Clock Jitter and Skew

Care must be taken to minimize jitter and skew on the distributed system clock as both parameters affect measurement performance.

Jitter on the input clock causes jitter in the generated modulator clock, resulting in sample timing errors and increased noise.

Skew between input clocks from node to node creates a sample timing offset, resulting in systematic measurement errors in a reconstructed signal.

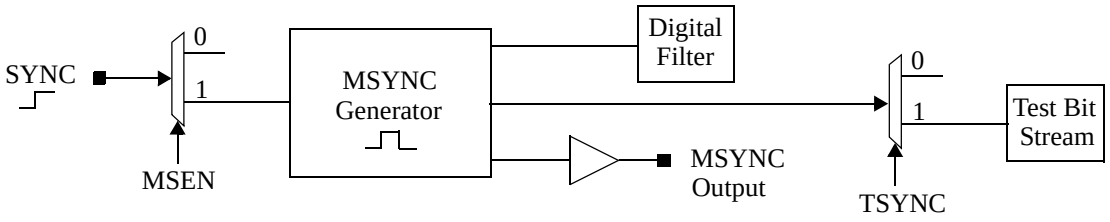


Figure 13. Synchronization Block Diagram

7. SYNCHRONIZATION

The CS5378 has a dedicated SYNC input that aligns the internal digital filter phase and generates an external signal for synchronizing modulator analog sampling. By providing simultaneous rising edges to the SYNC pins of multiple CS5378 devices, synchronous sampling across a network can be guaranteed.

7.1 Pin Description

SYNC - Pin 19

Synchronization input, rising edge triggered.

7.2 MSYNC Generation

The SYNC signal rising edge is used to generate a retimed synchronization signal, MSYNC. The MSYNC signal reinitializes internal digital filter phase and is driven onto the MSYNC output pin to phase align modulator analog sampling.

The MSEN bit in the digital filter CONFIG register (0x00) enables MSYNC generation. See "Modulator Interface" on page 36 for more information about MSYNC.

7.3 Digital Filter Synchronization

The internal MSYNC signal resets the digital filter state machine to establish a known digital filter phase. Filter convolutions restart, and the next output word is available one full sample period later.

Repetitive synchronization is supported when SYNC events occur at exactly the selected output rate. In this case, re-synchronization will occur at the start of a convolution cycle when the digital filter state machine is already reset.

7.4 Modulator Synchronization

The external MSYNC signal phase aligns modulator analog sampling when connected to the CS5373A MSYNC input. This ensures synchronous analog sampling relative to MCLK.

Repetitive synchronization of the modulators is supported when SYNC events occur at exactly the selected output rate. In this case, re-synchronization always occurs at the start of analog sampling.

7.5 Test Bit Stream Synchronization

When the test bit stream generator is enabled, an MSYNC signal can reset the internal data pointer. This restarts the test bit stream from the first data point to establish a known output signal phase.

The TSYNC bit in the digital filter TBSCFG register (0x2A) enables synchronization of the test bit stream by MSYNC. When TSYNC is disabled, the test bit stream phase is not affected by MSYNC.

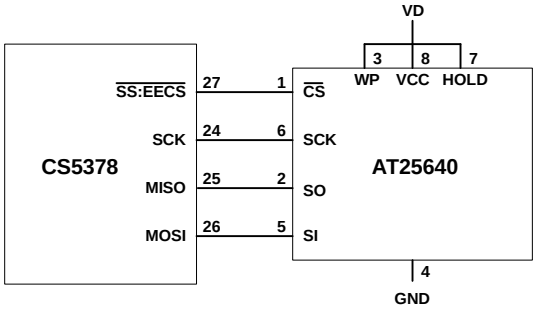


Figure 14. EEPROM Configuration Block Diagram

8. CONFIGURATION BY EEPROM

After reset, the CS5378 reads the state of the GPIO7:BOOT pin to determine a source for configuration commands. If BOOT is high, the CS5378 initiates serial transactions to read configuration information from an external EEPROM.

8.1 Pin Descriptions

Pins required for EEPROM boot are listed here, other serial pins are inactive.

SCK - Pin 24

Serial clock output, nominally 1.024 MHz.

MISO - Pin 25

Serial data input pin. Valid on rising edge of SCK, transition on falling edge.

MOSI - Pin 26

Serial data output pin. Valid on rising edge of SCK, transition on falling edge.

$\overline{\text{SS:EECS}}$ - Pin 27

EEPROM chip select output, active low.

8.2 EEPROM Hardware Interface

When booting from EEPROM the CS5378 actively performs serial transactions, as shown in Figure 15, to read configuration commands and data. 8-bit SPI opcodes and 16-bit addresses are combined to read back 8-bit configuration commands and 24-bit configuration data.

System design should include a connection to the configuration EEPROM for in-circuit reprogramming. The CS5378 serial pins tri-state when inactive to support external connections to the serial bus.

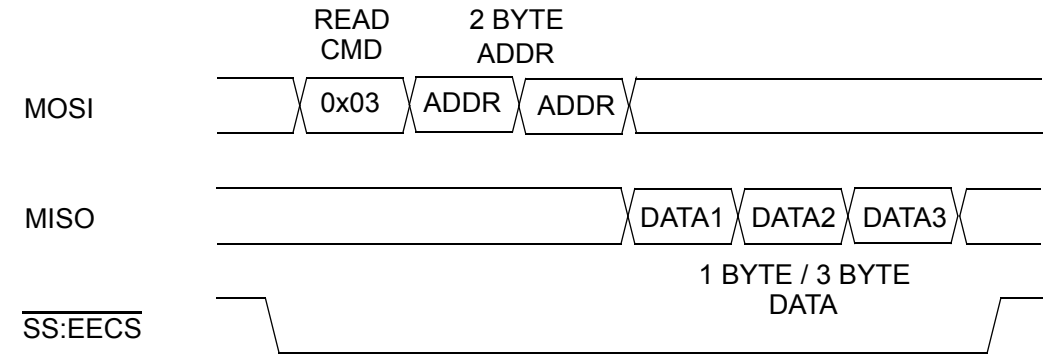
8.3 EEPROM Organization

The boot EEPROM holds the 8-bit commands and 24-bit data required to initialize the CS5378 into an operational state. Configuration information starts at memory location 0x10, with addresses 0x00 to 0x0F free for use as manufacturing header information.

The first serial transaction reads a 1-byte command from memory location 0x10 and then, depending on the command type, reads multiple 3-byte data words to complete the command. Command and data reads continue until the 'Filter Start' command is recognized.

Instruction	Opcode	Address	Definition
Read	0x03	ADDR[15:0]	Read data beginning at the address given in ADDR.

Serial Read from EEPROM



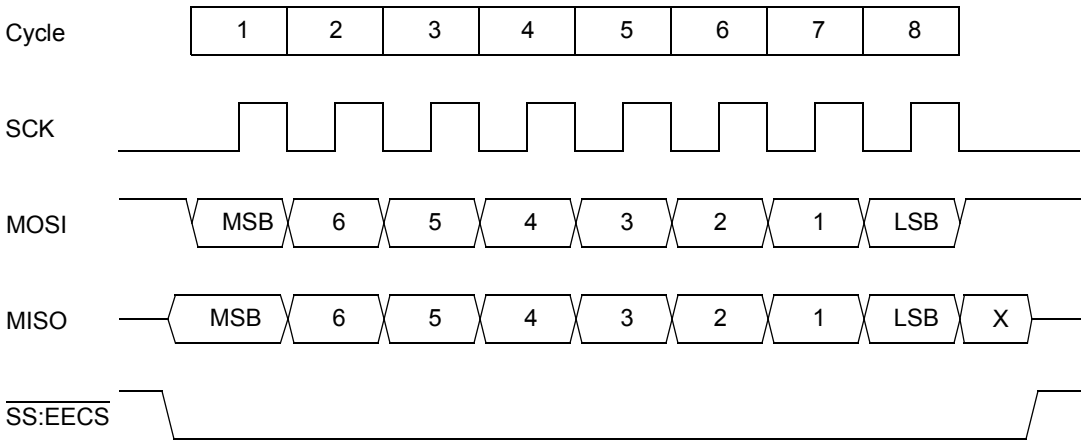


Figure 15. EEPROM Serial Read Transactions

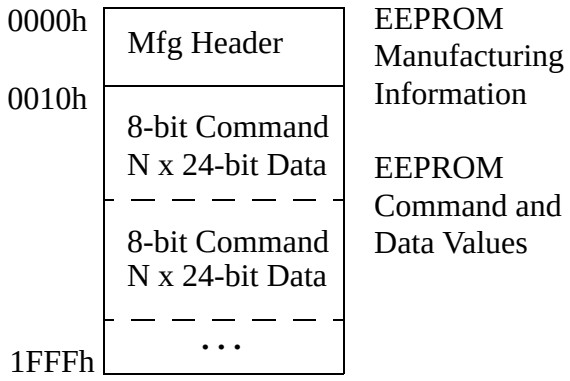


Figure 16. 8 Kbyte EEPROM Memory Organization

The maximum number of bytes that will be written for a single configuration is less than 2 KByte (16 Kbit), including command overhead:

Memory Requirement	Bytes
Digital Filter Registers (12)	84
FIR Coefficients (255+255)	1537
IIR Coefficients (3+5)	25
'Filter Start' Command	1
Total Bytes	**1647**

Table 6. Maximum EEPROM Configuration

Supported serial configuration EEPROMs are SPI mode 0 (0,0) compatible, 16-bit addresses, 8-bit data, larger than 2 KByte (16 KBit). ATMEL AT25640, AT25128, or similar serial EEPROMs are recommended.

8.4 EEPROM Configuration Commands

A summary of available EEPROM commands is shown in Table 7.

Write DF Register - 0x01

This EEPROM command writes a data value to the specified digital filter register. Digital filter registers control hardware peripherals and filtering functions. See "Digital Filter Registers" on page 71 for the bit definitions of the digital filter registers.

Sample Command:

Write digital filter register 0x00 with data value 0x060431. Then write 0x20 with data 0x000240.

01 00 00 00 06 04 31

01 00 00 20 00 02 40

Write FIR Coefficients - 0x02

This EEPROM command writes custom coefficients for the FIR1 and FIR2 filters. The first two data words set the number of FIR1 and FIR2 coefficients to be written. The remaining data words are the concatenated FIR1 and FIR2 coefficients.

A maximum of 255 coefficients can be written for each FIR filter, though the available digital filter computation cycles will limit their practical size. See "FIR Filter" on page 44 for more information about FIR filter coefficients.

Sample Command:

Write FIR1 coefficients 0x00022E, 0x000771 then FIR2 coefficients 0xFFFFB9, 0xFFFE8D.

02 00 00 02 00 00 02

00 02 2E 00 07 71 FF FF B9 FF FE 8D

Write IIR Coefficients - 0x03

This EEPROM command writes custom coefficients for the two stage IIR filter. The IIR architecture and number of coefficients is fixed, so eight data words containing coefficient values always immediately follow the command byte. The IIR coefficient write order is: a11, b10, b11, a21, a22, b20, b21, and b22. See "IIR Filter" on page 52 for more information about IIR filter coefficients.

Sample Command:

Write IIR1 coefficients 0x84BC9D, 0x7DA1B1, 0x825E4F, and IIR2 coefficients 0x83694F, 0x3CAD5F, 0x3E5104, 0x835DF8, 0x3E5104.

03

84 BC 9D 7D A1 B1 82 5E 4F 83 69 4F

3C AD 5F 3E 51 04 83 5D F8 3E 51 04

Write ROM Coefficients - 0x04

This EEPROM command selects the on-chip coefficients for the FIR1, FIR2, IIR 1st order, and IIR 2nd order filters for use by the digital filter. One data word is required to select which internal coefficient sets to use. See "Filter Coefficient Selection" on page 38 for information about selecting on-chip FIR and IIR coefficient sets.

Sample Command:

Select IIR1 and IIR2 3 Hz @ 500 SPS low-cut coefficients, with FIR1 and FIR2 linear phase high-cut coefficients. Data word 0x002200.

04 00 22 00

Filter Start - 0x07

This EEPROM command initializes and starts the digital filter. Measurement data becomes available one full sample period after this command is issued. No data words are required for this EEPROM command.

Sample Command:

07

Name	CMD 8-bit	DATA 24-bit	Description
NOP	00	-	No Operation
WRITE DF REGISTER	01	REG DATA	Write Digital Filter Register
WRITE FIR COEFFICIENTS	02	NUM FIR1 NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	03	a11 b10 b11 a21 a22 b20 b21 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	04	COEF SEL	Use On-Chip Coefficients
NOP	05	-	No Operation
NOP	06	-	No Operation
FILTER START	07	-	Start Digital Filter Operation

(DATA) indicates multiple words of this type are to be written.

Table 7. EEPROM Boot Configuration Commands

8.5 Example EEPROM Configuration

Table 8 shows an example EEPROM file for a minimal CS5378 configuration.

Addr	Data	Description
00	00	Mfg header
01	00	
02	00	
03	00	
04	00	
05	00	
06	00	
07	00	
08	00	
09	00	
0A	00	
0B	00	
0C	00	
0D	00	
0E	00	
0F	00	
10	04	Write ROM Coefficients
11	00	
12	22	
13	00	
14	01	Write CONFIG Register
15	00	
16	00	
17	00	
18	06	
19	04	
1A	31	
1B	01	Write FILTCFG Register
1C	00	
1D	00	
1E	20	
1F	00	

Addr	Data	Description
21	02	
22	40	
23	01	Write TBSCFG Register
24	00	
25	00	
26	2A	
27	07	
28	40	
29	40	
2A	01	Write TBSGAIN Register
2B	00	
2C	00	
2D	2B	
2E	04	
2F	B0	
30	00	
31	07	Filter Start

Table 8. Example EEPROM File

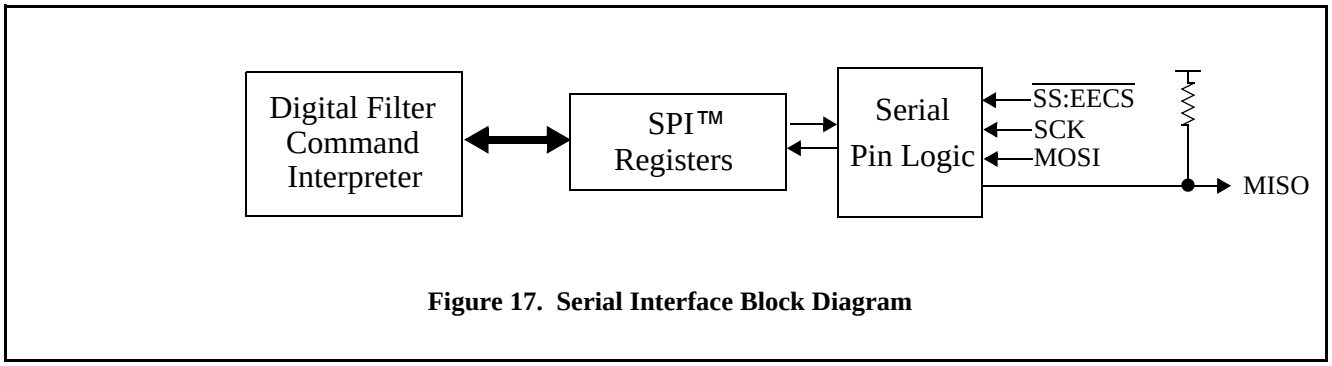


Figure 17. Serial Interface Block Diagram

9. CONFIGURATION BY MICROCONTROLLER

After reset, the CS5378 reads the state of the GPIO7:BOOT pin to determine a source for configuration commands. If BOOT is low, the CS5378 receives configuration commands from a microcontroller.

9.1 Pin Descriptions

Pins required for microcontroller boot are listed here, other serial pins are inactive.

$\overline{\text{SS:EECS}}$ - Pin 27

Slave select input pin, active low. Serial chip select input from a microcontroller.

MOSI - Pin 26

Serial data input pin. Valid on rising edge of SCK, transition on falling edge.

MISO - Pin 25

Serial data output pin. Valid on rising edge of SCK, transition on falling edge. Open drain output requiring a 10 kΩ pull-up resistor.

SCK - Pin 24

Serial clock input pin. Serial clock input from microcontroller, maximum 4.096 MHz.

9.2 Microcontroller Hardware Interface

When booting from a microcontroller the CS5378 receives configuration commands and configuration data through serial transactions, as shown in Figure 18. 8-bit SPI opcodes and 8-bit addresses are combined to read and write 24-bit configuration commands and data.

Microcontroller serial transactions require toggling the $\overline{\text{SS:EECS}}$ pin as the CS5378 chip select and writing a serial clock to the SCK input. Serial data is input to the CS5378 on the MOSI pin, and output on the MISO pin.

9.3 Microcontroller Serial Transactions

Microcontroller configuration commands are written to the digital filter through SPI registers. A 24-bit command and two 24-bit data words can be written to the SPI registers in any single serial transaction. Some commands require additional data words through additional serial transactions to complete.

9.3.1 SPI opcodes

A microcontroller communicates with the CS5378 serial port using standard 8-bit SPI opcodes and an 8-bit address. The standard SPI ‘Read’ and ‘Write’ opcodes are listed in Figure 18.

Instruction	Opcode	Address	Definition
Write	0x02	ADDR[7:0]	Write SPI registers beginning at the address in ADDR.
Read	0x03	ADDR[7:0]	Read SPI registers beginning at the address in ADDR.

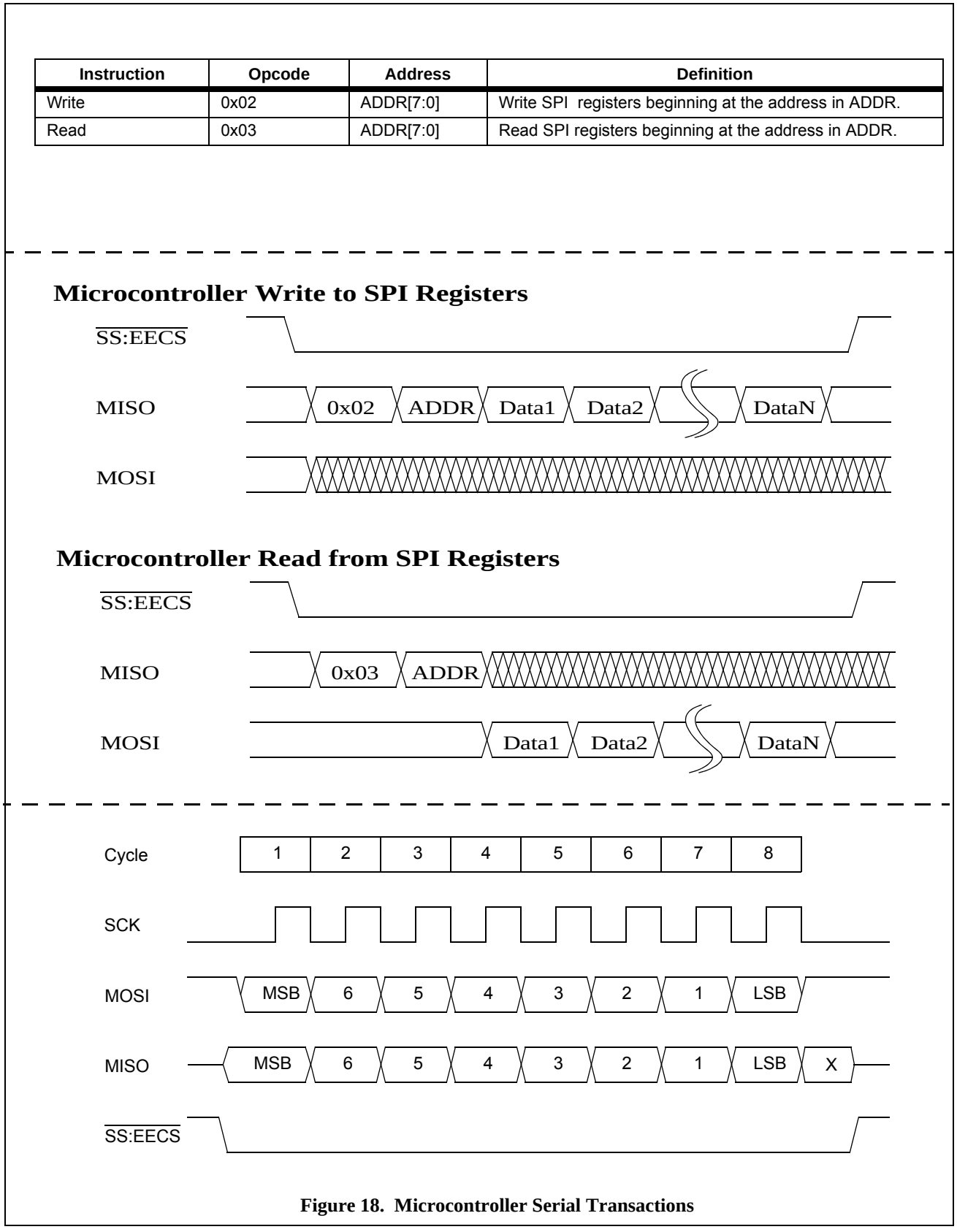


Figure 18. Microcontroller Serial Transactions

9.3.2 SPI registers

The SPI registers are shown in Figure 19 and are 24-bit registers mapped into an 8-bit register space as high, mid, and low bytes. See “SPI Registers” on page 66 for the bit definitions of the SPI registers.

9.3.3 Serial transactions

A serial transaction to the SPI registers starts with an SPI opcode, followed by an address, and then some number of data bytes written or read starting at that address.

Typical serial write transactions require sending groups of 5, 8, or 11 total bytes to the SPICMD or SPIDAT1 registers:

5-byte write to SPICMD

02 03 12 34 56

5-byte write to SPIDAT1

02 06 12 34 56

8-byte write to SPICMD, SPIDAT1

02 03 12 34 56 AB CD EF

8-byte write to SPIDAT1, SPIDAT2

02 06 12 34 56 AB CD EF

11-byte write to SPICMD, SPIDAT1, SPIDAT2

02 03 12 34 56 AB CD EF 65 43 21

Typical serial read transactions require groups of 3 or 5 bytes, split between writing into MOSI and reading from MISO.

3-byte read of mid-byte of SPICTRL

MOSI: 03 01 00

MISO: xx xx 12

5-byte read of SPIDAT1

MOSI: 03 06 00 00 00

MISO: xx xx 12 34 56

9.3.4 Multiple serial transactions

Some configuration commands require multiple serial transactions to complete. There must be a small delay between transactions for the CS5378 to process the incoming data. Two methods can be used to ensure the CS5378 is ready to receive the next configuration command.

1) Delay a fixed 1 ms period to guarantee enough time for the command to be completed.

2) Verify the status of the E2DREQ bit by reading the SPICTRL register. When low, the CS5378 is ready for the next command.

9.3.5 Polling E2DREQ

One transaction type that can always be performed no matter the delay from the previous configuration command is reading E2DREQ in the mid-byte of the SPICTRL register. A 3-byte read transaction.

MOSI: 03 01 00

MISO: xx xx 01 <- E2DREQ bit high

MISO: xx xx 00 <- E2DREQ bit low

The E2DREQ bit reads high while a serial transaction is being processed. When low, the digital filter is ready to receive a new serial transaction.

Name	Addr.	Type	# Bits	Description
SPICTRL	00 - 02	R/W	8, 8, 8	SPI Control
SPICMD	03 - 05	R/W	8, 8, 8	SPI Command
SPIDAT1	06 - 08	R/W	8, 8, 8	SPI Data 1
SPIDAT2	09 - 0B	R/W	8, 8, 8	SPI Data 2

Figure 19. SPI Registers

9.4 Microcontroller Configuration Commands

A summary of available microcontroller configuration commands is listed in Table 9.

Write DF Register - 0x01

This configuration command writes a specified digital filter register. Digital filter registers control hardware peripherals and filtering functions. See “Digital Filter Registers” on page 71 for the bit definitions of the digital filter registers.

Sample Command:

Write digital filter register 0x00 with data value 0x060431. Then write 0x20 with data 0x000240.

02 03 00 00 01 00 00 00 06 04 31

Delay 1 ms or poll E2DREQ

02 03 00 00 01 00 00 20 00 02 40

Delay 1 ms or poll E2DREQ

Read DF Register - 0x02

This command reads a specified digital filter register. The register value is requested in the first serial transaction, with the register value copied to SPIDAT1 and read in a subsequent serial transaction.

Sample Command:

Read digital filter registers 0x00 and 0x20.

02 03 00 00 02 00 00 00

Delay 1 ms or poll E2DREQ

MOSI: 03 06 00 00 00

MISO: xx xx 06 04 31

02 03 00 00 02 00 00 20

Delay 1 ms or poll E2DREQ

MOSI: 03 06 00 00 00

MISO: xx xx 00 02 40

Name	CMD 24-bit	DAT1 24-bit	DAT2 24-bit	Description
NOP	000000	-	-	No Operation
WRITE DF REGISTER	000001	REG	DATA	Write Digital Filter Register
READ DF REGISTER	000002	REG [DATA]	- -	Read Digital Filter Register
WRITE FIR COEFFICIENTS	000003	NUM FIR1 (FIR COEF)	NUM FIR2 (FIR COEF)	Write Custom FIR Coefficients
WRITE IIR COEFFICIENTS	000004	a11 b11 a22 b21	b10 a21 b20 b22	Write Custom IIR Coefficients
WRITE ROM COEFFICIENTS	000005	COEF SEL	-	Use On-Chip Coefficients
NOP	000006	-	-	No Operation
NOP	000007	-	-	No Operation
FILTER START	000008	-	-	Start Digital Filter Operation
FILTER STOP	000009	-	-	Stop Digital Filter Operation

[DATA] indicates data word returned from digital filter.

(DATA) indicates multiple words of this type are to be written.

Table 9. Microcontroller Boot Configuration Commands

Write FIR Coefficients - 0x03

This command writes custom coefficients for the FIR1 and FIR2 filters. The first two data words set the number of FIR1 and FIR2 coefficients to be written. The remaining data words are the concatenated FIR1 and FIR2 coefficients.

A maximum of 255 coefficients can be written for each FIR filter, though the available digital filter computation cycles will limit their practical size. See "FIR Filter" on page 44 for more information about FIR filter coefficients.

Sample Command:

Write FIR1 coefficients 0x00022E, 0x000771 then FIR2 coefficients 0xFFFFB9, 0xFFFE8D.

02 03 00 00 03 00 00 02 00 00 02

Delay 1 ms or poll E2DREQ

02 06 00 02 2E 00 07 71

Delay 1 ms or poll E2DREQ

02 06 FF FF B9 FF FE 8D

Delay 1 ms or poll E2DREQ

Write IIR Coefficients - 0x04

This command writes custom coefficients for the two stage IIR filter. The IIR architecture and number of coefficients is fixed, so eight coefficient values immediately follow this command. The IIR coefficient write order is: a11, b10, b11, a21, a22, b20, b21, and b22. See "IIR Filter" on page 52 for more information about IIR filter coefficients.

Sample Command:

Write IIR1 coefficients 0x84BC9D, 0x7DA1B1, 0x825E4F, and IIR2 coefficients 0x83694F, 0x3CAD5F, 0x3E5104, 0x835DF8, 0x3E5104.

02 03 00 00 04 84 BC 9D 7D A1 B1

Delay 1 ms or poll E2DREQ

02 06 82 5E 4F 83 69 4F

Delay 1 ms or poll E2DREQ

02 06 3C AD 5F 3E 51 04

Delay 1 ms or poll E2DREQ

02 06 83 5D F8 3E 51 04

Delay 1 ms or poll E2DREQ

Write ROM Coefficients - 0x05

This configuration command selects the on-chip coefficients for FIR1, FIR2, IIR 1st order, and IIR 2nd order filters for use by the digital filter. One data word is required to select which internal coefficient sets to use. See "Filter Coefficient Selection" on page 38 for information about selecting on-chip FIR and IIR coefficient sets.

Sample Command:

Select IIR1 and IIR2 3 Hz @ 500 SPS low-cut coefficients, with FIR1 and FIR2 linear phase high-cut coefficients. Data word 0x002200.

02 03 00 00 05 00 22 00

Delay 1 ms or poll E2DREQ

Filter Start - 0x08

This command initializes and starts the digital filter. Measurement data becomes available one full sample period after this command is issued. No data words are required for this command.

Sample Command:

02 03 00 00 08

Delay 1 ms or poll E2DREQ

Filter Stop - 0x09

This command disables the digital filter. Measurement data output stops immediately after this command is issued. No data words are required for this command.

Sample Command:

02 03 00 00 09

Delay 1 ms or poll E2DREQ

9.5 Example Microcontroller Configuration

Table 10 shows an example microcontroller transactions for a minimal CS5378 configuration.

Transaction	SPI Data	Description
01	02 03 00 00 05 00 22 00	Write ROM coefficients
02	Delay 1ms or poll E2DREQ	
03	02 03 00 00 01 00 00 00 06 04 31	Write CONFIG Register
04	Delay 1ms or poll E2DREQ	
05	02 03 00 00 01 00 00 20 00 02 40	Write FILTCFG Register
06	Delay 1ms or poll E2DREQ	
07	02 03 00 00 01 00 00 2A 07 40 40	Write TBSCFG Register
08	Delay 1ms or poll E2DREQ	
09	02 03 00 00 01 00 00 2B 04 B0 00	Write TBSGAIN Register
10	Delay 1ms or poll E2DREQ	
11	02 03 00 00 08	Filter Start

Table 10. Example Microcontroller Configuration

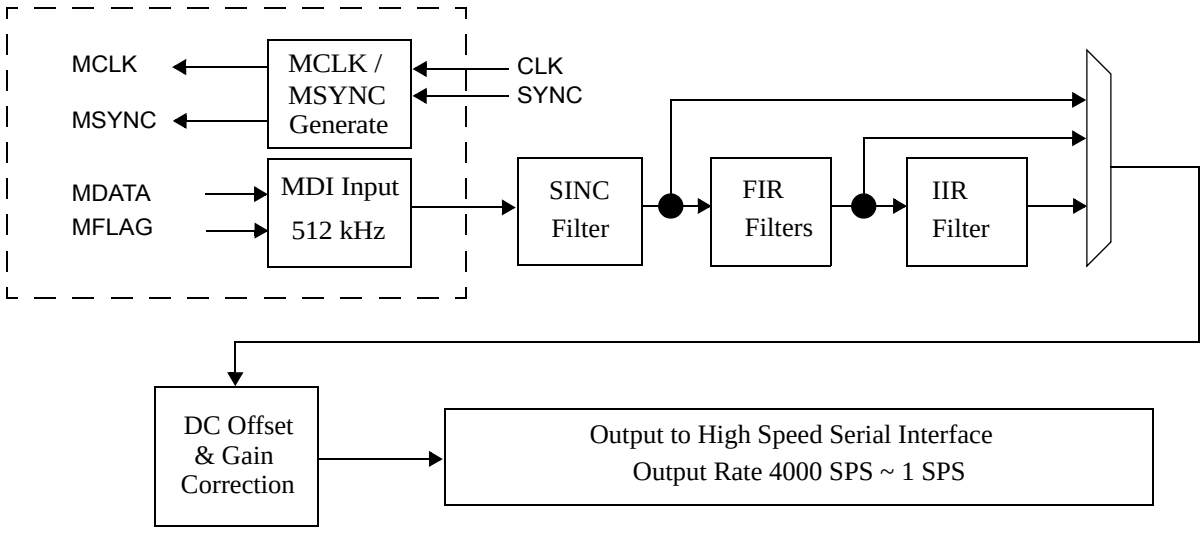


Figure 20. Modulator Data Interface

10. MODULATOR INTERFACE

The CS5378 performs digital filtering for a ΔΣ type modulator. Signals from the ΔΣ modulators are connected through the modulator data interface (MDI).

10.1 Pin Descriptions

MCLK - Pin 11

Modulator clock output. Nominally 2.048 MHz or 1.024 MHz.

MSYNC - Pin 12

Modulator synchronization signal output. Generated from the SYNC input.

MDATA - Pin 13

Modulator data input, nominally 512 kbit/s.

MFLAG - Pin 14

Modulator flag input. Driven high when the modulator is unstable due to an analog over-range condition.

10.2 Modulator Clock Generation

The MCLK output is a low-jitter, low-skew modulator clock generated from the 32.768 MHz master clock.

MCLK typically operates at 2.048 MHz unless analog low-power modes require a 1.024 MHz modulator clock.

The MCLK rate is selected and the MCLK output is enabled by bits in the digital filter CONFIG register (0x00). By default MCLK is disabled and driven low.

10.3 Modulator Synchronization

The MSYNC output signal follows an input to the SYNC pin. MSYNC phase aligns the modulator sampling instant to guarantee synchronous analog sampling across a measurement network.

MSYNC is enabled by a bit in the CONFIG register (0x00). By default SYNC inputs do not cause an MSYNC output.

10.4 Modulator Data Input

The MDATA input expects 1-bit ΔΣ data at a 512 kHz or 256 kHz rate. The input rate is selected by a bit in the CONFIG register (0x00). By default, MDATA is expected at 512 kHz.

The MDATA input one's density is designed for full scale positive at 86% and full scale negative at 14%, with absolute maximum over-range capability to 93% and 7%. These raw ΔΣ inputs are decimated and filtered by the digital filter to create 24-bit samples at the output rate.

10.5 Modulator Flag Input

A high MFLAG input signal indicates the ΔΣ modulator has become unstable due to an analog over-range input signal. Once the over-range signal is reduced, the modulator recovers stability and the MFLAG signal is cleared.

The MFLAG input is mapped to a status bit in the serial data output stream, and is associated with each sample when written. See "Serial Data Interface" on page 58 for more information on the MFLAG error bit in the serial data status byte.

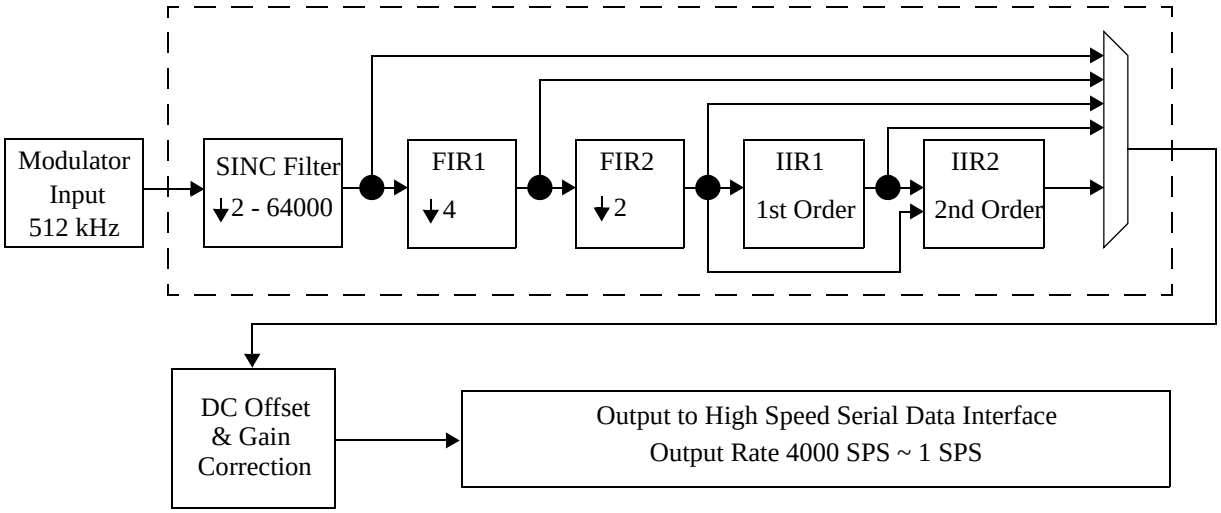


Figure 21. Digital Filter Stages

11. DIGITAL FILTER INITIALIZATION

The CS5378 digital filter consists of three multi-stage sections: a three stage SINC filter, a two stage FIR filter, and a two stage IIR filter.

To initialize the digital filter, FIR and IIR coefficient sets are selected using configuration commands and the FILTCFG register (0x20) is written to select the output filter stage, the output word rate, and the number of enabled channels. The digital filter clock rate is then selected by writing the CONFIG register (0x00).

11.1 Filter Coefficient Selection

Selection of SINC filter coefficients is not required as they are selected automatically based on the programmed output word rate.

Digital filter FIR and IIR coefficients are selected using the 'Write FIR Coefficients' and 'Write IIR Coefficients', or the 'Write ROM Coefficients' configuration commands. When writing the FIR and IIR coefficients from ROM, a data word selects an on-chip coefficient set for each filter stage. Figure 22 shows the format of the coefficient selection word, and the available coefficient sets for each selection.

Characteristics of the on-chip digital filter coefficients are discussed in the 'SINC Filter', 'FIR Filter', and 'IIR Filter' sections of this data sheet.

11.2 Filter Configuration Options

Digital filter parameters are selected by bits in the FILTCFG register (0x20), and the digital filter clock rate is selected by bits in the CONFIG register (0x00).

11.2.1 Output Filter Stage

The digital filter can output data following any stage in the filter chain. The output filter stage is selected by the FSEL bits in the FILTCFG register.

Taking data from the SINC or FIR1 filter stages reduces the overall decimation of the filter chain and increases the output rate, as discussed in the next section. Taking data from FIR2, IIR1, IIR2, or IIR3 results in data at the selected rate.

Bits	23:20	19:16	15:12	11:8	7:4	3:0
Selection	0000	0000	IIR2	IIR1	FIR2	FIR1

Bits 15:12	IIR2 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 11:8	IIR1 Coefficients
0000	3 Hz @ 2000 SPS
0001	3 Hz @ 1000 SPS
0010	3 Hz @ 500 SPS
0011	3 Hz @ 333 SPS
0100	3 Hz @ 250 SPS

Bits 3:0	FIR1 Coefficients
0000	Linear Phase
0001	Minimum Phase

Bits 7:4	FIR2 Coefficients
0000	Linear Phase
0001	Minimum Phase

Figure 22. FIR and IIR Coefficient Set Selection Word

11.2.2 Output Word Rate

The CS5378 digital filter supports output word rates (OWRs) between 4000 SPS and 1 SPS. The output word rate is selected by the DEC bits in the FILTCFG register.

When taking data directly from the SINC filter, the decimation of the FIR1 and FIR2 stages is bypassed and the actual output word rate is multiplied by a factor of eight compared with the register selection. When taking data directly from FIR1, the decimation of the FIR2 stage is bypassed and the actual output word rate is multiplied by a factor of two. Data taken from the FIR2, IIR1, IIR2, or IIR3 filtering stages is output at the selected rate.

11.2.3 Digital Filter Clock

The digital filter clock rate is programmable between 8.192 MHz and 32 kHz by bits in the CONFIG register.

Computation Cycles

The minimum digital filter clock rate for a configuration depends on the computation cycles required to complete digital filter convolutions at the selected output word rate. All configurations work for a maximum digital filter clock, but lower clock rates consume less power.

Standby Mode

The CS5378 can be placed in a low-power standby mode by sending the ‘Filter Stop’ configuration command and programming the digital filter clock to 32 kHz. In this mode the digital filter idles, consuming minimal power until re-enabled by later configuration commands.

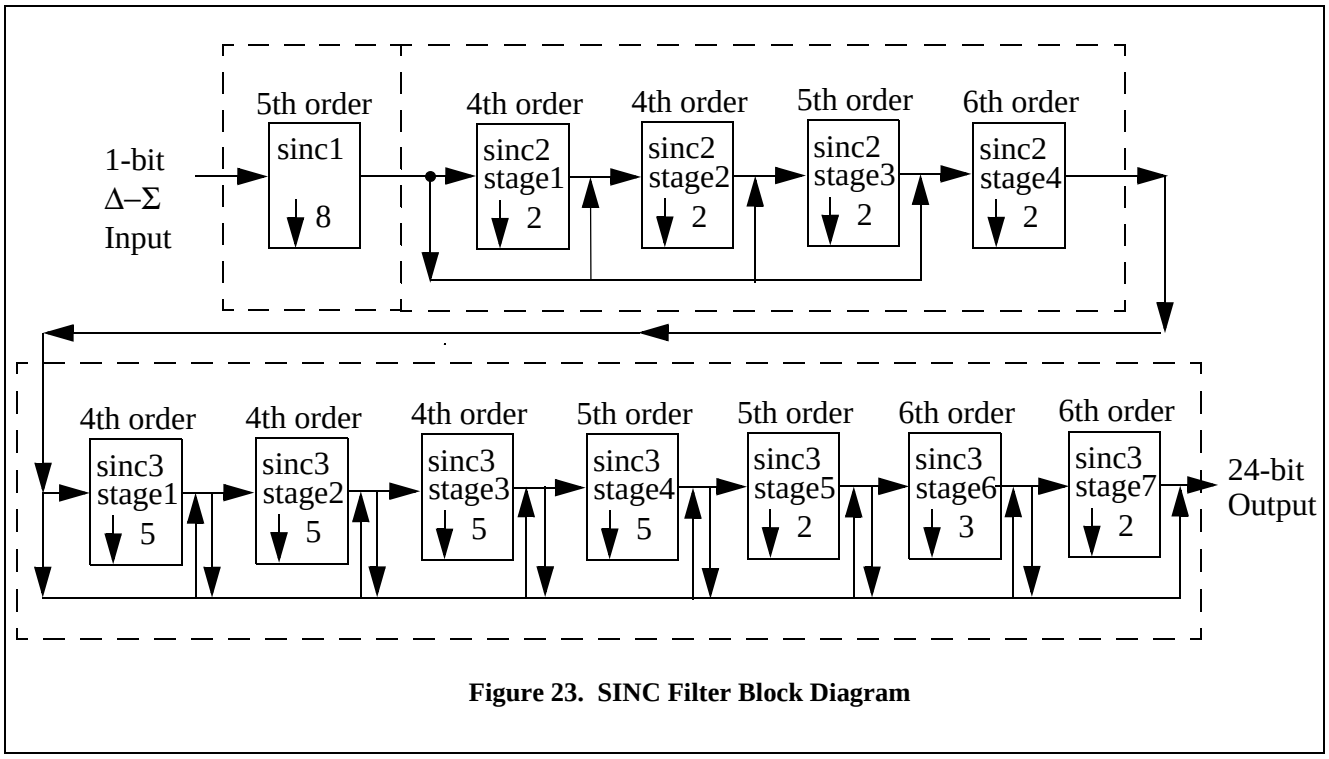


Figure 23. SINC Filter Block Diagram

12. SINC FILTER

The SINC filter primary purpose is to attenuate out-of-band noise components from the ΔΣ modulators. While doing so, they decimate 1-bit ΔΣ data into lower frequency 24-bit data suitable for the FIR and IIR filters.

The SINC filter has three cascaded sections, SINC1, SINC2, and SINC3, which are each made up of the smaller stages shown in Figure 23.

The selected output word rate in the FILTCFG register automatically determines the coefficients and decimation ratios selected for the SINC filters.

12.1 SINC1 Filter

The first section is SINC1, a single stage 5th order fixed decimate by 8 SINC filter. This SINC filter decimates the incoming 1-bit ΔΣ bit stream from the modulators down to a 64 kHz rate.

12.2 SINC2 Filter

The second section is SINC2, a multi-stage, variable order, variable decimation SINC filter. Depending on the selected output word rate in the FILTCFG register, different cascaded SINC2 stages are enabled, as shown in Table 11.

12.3 SINC3 Filter

The last section is SINC3, a flexible multi-stage variable order, variable decimation SINC filter. Depending on the selected output word rate in the FILTCFG register, different SINC3 stages are enabled, as shown in Table 11.

12.4 SINC Filter Synchronization

The SINC filter is synchronized to the external system by the MSYNC signal, which is generated from the SYNC input. The MSYNC signal sets a reference time (time 0) for all filter operations, and the SINC filter is restarted to phase align with this reference time.

SINC1 – Single stage, fixed decimate by 8

5th order decimate by 8, 36 coefficients

SINC2 – Multi-stage, variable decimation

Stage 1: 4th order decimate by 2, 5 coefficients
Stage 2: 4th order decimate by 2, 5 coefficients
Stage 3: 5th order decimate by 2, 6 coefficients
Stage 4: 6th order decimate by 2, 7 coefficients

SINC3 – Multi-stage, variable decimation

Stage 1: 4th order decimate by 5, 17 coefficients
Stage 2: 4th order decimate by 5, 17 coefficients
Stage 3: 4th order decimate by 5, 17 coefficients
Stage 4: 5th order decimate by 5, 21 coefficients
Stage 5: 5th order decimate by 2, 6 coefficients
Stage 6: 6th order decimate by 3, 13 coefficients
Stage 7: 6th order decimate by 2, 7 coefficients

Figure 24. SINC Filter Stages

SINC filters

FIR2 Output Word Rate	DEC Bit Setting	SINC1 Deci-mation	SINC2 Deci-mation	SINC2 Stages	SINC3 Deci-mation	SINC3 Stages
4000	0111	8	2	4	-	-
2000	0110	8	4	3,4	-	-
1000	0101	8	8	2,3,4	-	-
500	0100	8	16	1,2,3,4	-	-
333	0011	8	8	2,3,4	3	6
250	0010	8	16	1,2,3,4	2	7
200	0001	8	4	3,4	10	4,7
125	0000	8	16	1,2,3,4	4	5,7
100	1111	8	4	3,4	20	3,5,7
50	1110	8	8	2,3,4	20	3,5,7
40	1101	8	4	3,4	50	3,4,7
25	1100	8	16	1,2,3,4	20	3,5,7
20	1011	8	4	3,4	100	2,3,5,7
10	1010	8	8	2,3,4	100	2,3,5,7
5	1001	8	16	1,2,3,4	100	2,3,5,7
1	1000	8	16	1,2,3,4	500	1,2,3,5,7

Table 11. SINC Filter Configurations

Filter Type	System Function	Filter Coefficients
SINC1 5th order decimate by 8 36 coefficients	$H(z) = \left(\frac{1-z^{-8}}{1-z^{-1}}\right)^5$	h_0 = 1 h_{18} = 2460 h_1 = 5 h_{19} = 2380 h_2 = 15 h_{20} = 2226 h_3 = 35 h_{21} = 2010 h_4 = 70 h_{22} = 1750 h_5 = 126 h_{23} = 1470 h_6 = 210 h_{24} = 1190 h_7 = 330 h_{25} = 926 h_8 = 490 h_{26} = 690 h_9 = 690 h_{27} = 490 h_{10} = 926 h_{28} = 330 h_{11} = 1190 h_{29} = 210 h_{12} = 1470 h_{30} = 126 h_{13} = 1750 h_{31} = 70 h_{14} = 2010 h_{32} = 35 h_{15} = 2226 h_{33} = 15 h_{16} = 2380 h_{34} = 5 h_{17} = 2460 h_{35} = 1

Filter Type	System Function	Filter Coefficients
SINC2 (Stage 1) SINC2 (Stage 2) 4th order decimate by 2 5 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^4$	h_0 = 1 h_1 = 4 h_2 = 6 h_3 = 4 h_4 = 1
SINC2 (Stage 3) 5th order decimate by 2 6 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^5$	h_0 = 1 h_1 = 5 h_2 = 10 h_3 = 10 h_4 = 5 h_5 = 1
SINC2 (Stage 4) 6th order decimate by 2 7 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^6$	h_0 = 1 h_1 = 6 h_2 = 15 h_3 = 20 h_4 = 15 h_5 = 6 h_6 = 1

Table 12. SINC1 and SINC2 Filter Coefficients

Filter Type	System Function	Filter Coefficients
SINC3 (Stage 1) SINC3 (Stage 2) SINC3 (Stage 3) 4^{th} order decimate by 5 17 coefficients	$H(z) = \left(\frac{1-z^{-5}}{1-z^{-1}}\right)^4$	h_0 = 1 h_9 = 80 h_1 = 4 h_{10} = 68 h_2 = 10 h_{11} = 52 h_3 = 20 h_{12} = 35 h_4 = 35 h_{13} = 20 h_5 = 52 h_{14} = 10 h_6 = 68 h_{15} = 4 h_7 = 80 h_{16} = 1 h_8 = 85
SINC3 (Stage 4) 5^{th} order decimate by 5 21 coefficients	$H(z) = \left(\frac{1-z^{-5}}{1-z^{-1}}\right)^5$	h_0 = 1 h_{11} = 365 h_1 = 5 h_{12} = 320 h_2 = 15 h_{13} = 255 h_3 = 35 h_{14} = 185 h_4 = 70 h_{15} = 121 h_5 = 121 h_{16} = 70 h_6 = 185 h_{17} = 35 h_7 = 255 h_{18} = 15 h_8 = 320 h_{19} = 5 h_9 = 365 h_{20} = 1 h_{10} = 381
SINC3 (Stage 5) 5^{th} order decimate by 2 6 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^5$	h_0 = 1 h_1 = 5 h_2 = 10 h_3 = 10 h_4 = 5 h_5 = 1
SINC3 (Stage 6) 6^{th} order decimate by 3 13 coefficients	$H(z) = \left(\frac{1-z^{-3}}{1-z^{-1}}\right)^6$	h_0 = 1 h_7 = 126 h_1 = 6 h_8 = 90 h_2 = 21 h_9 = 50 h_3 = 50 h_{10} = 21 h_4 = 90 h_{11} = 6 h_5 = 126 h_{12} = 1 h_6 = 141
SINC3 (Stage 7) 6^{th} order decimate by 2 7 coefficients	$H(z) = \left(\frac{1-z^{-2}}{1-z^{-1}}\right)^6$	h_0 = 1 h_1 = 6 h_2 = 15 h_3 = 20 h_4 = 15 h_5 = 6 h_6 = 1

Table 13. SINC3 Filter Coefficients

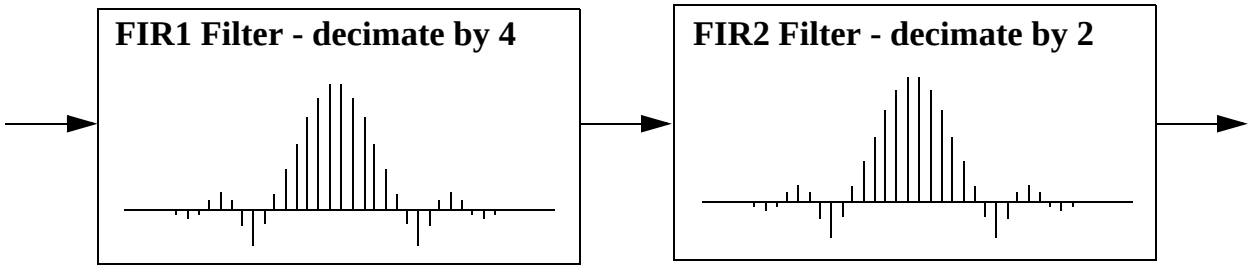


Figure 25. FIR Filter Block Diagram

13. FIR FILTER

The finite impulse response (FIR) filter block consists of two cascaded stages, FIR1 and FIR2. It compensates for SINC filter droop and creates a low-pass corner to block aliased components of the input signal.

On-chip linear phase or minimum phase coefficients can be selected using a configuration command, or the coefficients can be programmed for a custom filter response.

13.1 FIR1 Filter

The FIR1 filter stage has a decimate by four architecture. It compensates for SINC filter droop and flattens the magnitude response of the pass band.

The on-chip linear and minimum phase coefficient sets are 48-tap, with a maximum 255 programmable coefficients. All coefficients are normalized to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equation for FIR1 is a convolution of the input values, X(n), and the filter coefficients, h(k), to produce an output value, Y.

$Y = [h(k)*X(n-k)] + [h(k+1)*X(n-(k+1))] + ...$

13.2 FIR2 Filter

The FIR2 filter stage has a decimate by two architecture. It creates a low-pass brick wall filter to block aliased components of the input signal.

The on-chip linear and minimum phase coefficient sets are 126-tap, with a maximum 255 programmable coefficients. All coefficients are normalized to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equation for FIR2 is a convolution of the input values, X(n), and the filter coefficients, h(k), to produce an output value, Y.

$Y = [h(k)*X(n-k)] + [h(k+1)*X(n-(k+1))] + ...$

13.3 On-Chip FIR Coefficients

Two sets of on-chip coefficients, linear phase and minimum phase, are available for FIR1 and FIR2. Performance of the on-chip coefficient sets is very good, with excellent ripple and stop band characteristics as described in Figure 26 and Table 14.

Which on-chip coefficient set to use is selected by a data word following the 'Write ROM Coefficients' configuration command. See "Filter Coefficient Selection" on page 38 for information about selecting on-chip coefficient sets.

13.4 Programmable FIR Coefficients

A maximum of 255 + 255 coefficients can be programmed into FIR1 and FIR2 to create a custom filter response. The total number of coefficients for the FIR filter is fundamentally limited by the available computation cycles in the digital filter, which itself is determined by the digital filter clock rate.

Custom filter sets should normalize the maximum coefficient value to 24-bit two's complement full scale, 0x7FFFFF, and scale all other coefficients accordingly. To maintain maximum internal dynamic range, the CS5378 FIR filter performs double precision calculations with an automatic gain correction to scale the final output.

Custom FIR coefficients are uploaded using the 'Write FIR Coefficients' configuration command. See "EEPROM Configuration Commands" on page 27 or "Microcontroller Configuration Commands" on page 33 for information about writing custom FIR coefficients.

13.5 FIR Filter Synchronization

The FIR1 and FIR2 filters are synchronized to the external system by the MSYNC signal, which is generated from the SYNC input. The MSYNC signal sets a reference time (time 0) for all filter operations, and the FIR filters are restarted to phase align with this reference time.

FIR1 – Single stage, fixed decimate by 4

Coefficient set 0: linear phase decimate by 4, 48 coefficients
Coefficient set 1: minimum phase decimate by 4, 48 coefficients
SINC droop compensation filter

FIR2 – Single stage, fixed decimate by 2

Coefficient set 0: linear phase decimate by 2, 126 coefficients
Coefficient set 1: minimum phase decimate by 2, 126 coefficients
Brick wall low-pass filter, flat to 40% f_s

Combined SINC + FIR digital filter specifications

Passband ripple less than +/- 0.01 dB below 40% f_s
Transition band -3 dB frequency at 42.89% f_s
Stopband attenuation greater than 130 dB above 50% f_s

Figure 26. FIR Filter Stages

SINC + FIR filters

FIR2 Output Word Rate	SINC Deci-mation	FIR1 Deci-mation	FIR2 Deci-mation	Total Deci-mation	Passband Ripple (± dB)	Stopband Atten-uation (dB)
4000	16	4	2	128	0.0042	130.38
2000	32	4	2	256	0.0045	130.38
1000	64	4	2	512	0.0040	130.42
500	128	4	2	1024	0.0041	130.42
333	192	4	2	1536	0.0080	130.45
250	256	4	2	2048	0.0064	130.43
200	320	4	2	2560	0.0043	130.44
125	512	4	2	4096	0.0046	130.42
100	640	4	2	5120	0.0040	130.43
50	1280	4	2	10240	0.0040	130.43
40	1600	4	2	12800	0.0040	130.44
25	2560	4	2	20480	0.0040	132.98
20	3200	4	2	25600	0.0036	130.43
10	6400	4	2	51200	0.0036	130.43
5	12800	4	2	102400	0.0036	130.43
1	64000	4	2	512000	0.0029	134.31

Table 14. FIR Filter Characteristics

Individual filter stage group delay (no IIR)

	Decimation Ratios	Number of Coefficients	Group Delay (Input Rate)
SINC1	8	36	17.5
SINC2			
Stage 4	2	7	3.0
Stages 3,4	2,2	6,7	8.5
Stages 2,3,4	2,2,2	5,6,7	19.0
Stages 1,2,3,4	2,2,2,2	5,5,6,7	40.0
SINC3			
Stage 7	2	7	3.0
Stage 6	3	13	6.0
Stages 5,7	2,2	6,7	8.5
Stages 4,7	5,2	21,7	25.0
Stages 3,5,7	5,2,2	17,6,7	50.5
Stages 3,4,7	5,5,2	17,21,7	133.0
Stages 2,3,5,7	5,5,2,2	17,17,6,7	260.5
Stages 1,2,3,5,7	5,5,5,2,2	17,17,17,6,7	1310.5
FIR1			
Coefficient Set 0	4	48	23.5
Coefficient Set 1	4	48	See Figure
FIR2			
Coefficient Set 0	2	126	62.5
Coefficient Set 1	2	126	See Figure

Cumulative linear phase group delay (no IIR)

FIR2 Output Word Rate	SINC Output Group Delay (SINC Filter Input Rate)	FIR1 Output Group Delay (SINC Filter Input Rate)	FIR2 Output Group Delay (SINC Filter Input Rate)	FIR2 Output Group Delay (FIR2 Output Word Rate)
4000	41.5	417.5	4417.5	34.5117
2000	85.5	837.5	8837.5	34.5215
1000	169.5	1673.5	17673.5	34.5186
500	337.5	3345.5	35345.5	34.5171
333	553.5	5065.5	53065.5	34.5479
250	721.5	6737.5	70737.5	34.5398
200	885.5	8405.5	88405.5	34.5334
125	1425.5	13457.5	141457.5	34.5355
100	1701.5	16741.5	176741.5	34.5198
50	3401.5	33481.5	353481.5	34.5197
40	4341.5	41941.5	441941.5	34.5267
25	6801.5	66961.5	706961.5	34.5196
20	8421.5	83621.5	883621.5	34.5165
10	16841.5	167241.5	1767241.5	34.5164
5	33681.5	334481.5	3534481.5	34.5164
1	168081.5	1672081.5	17672081.5	34.5158

Table 15. SINC + FIR Group Delay

Minimum phase group delay

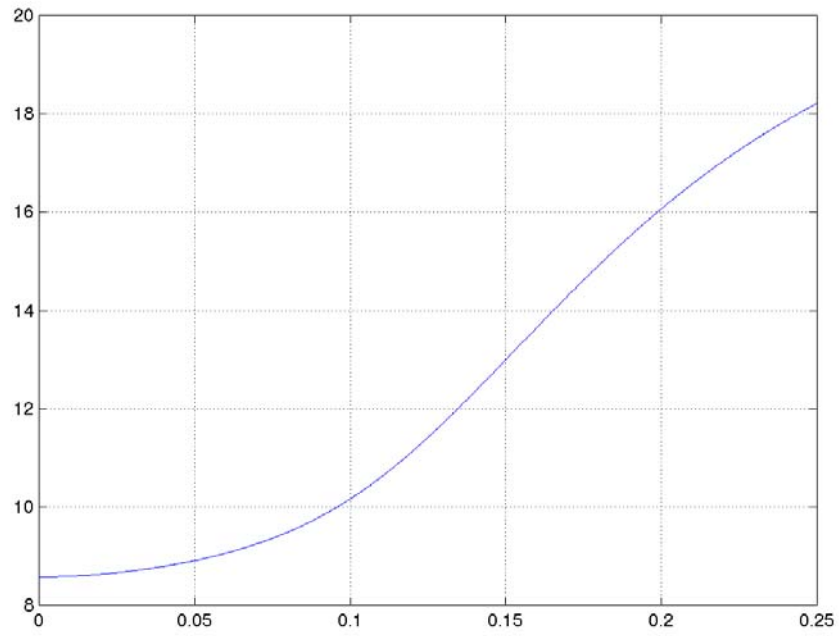
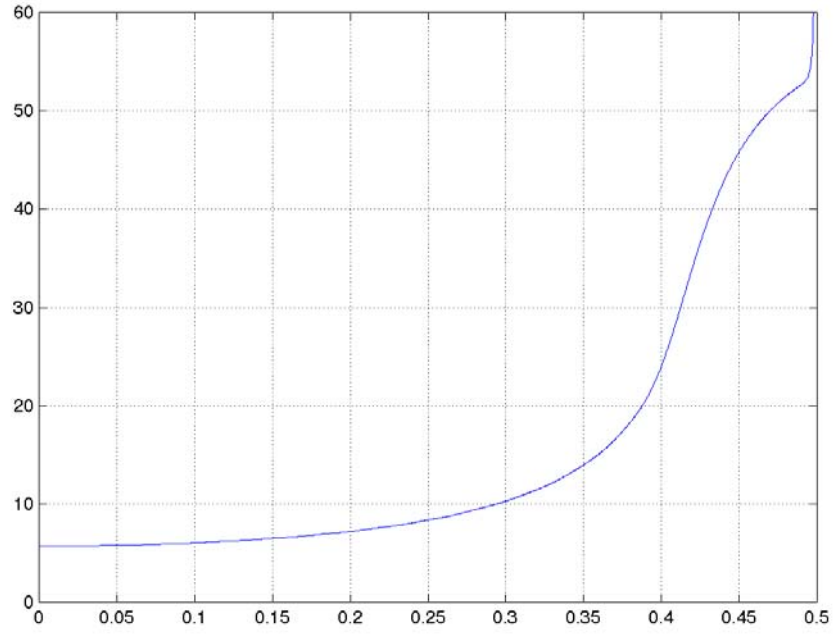
FIR1 Minimum Phase Group Delay (Normalized frequency)	
FIR2 Minimum Phase Group Delay (Normalized frequency)	

Table 16. Minimum Phase Group Delay

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR1 (Coefficient set 0) Low pass, SINC compensation Linear phase decimate by 4 48 coefficients	h_0 = 558	h_{24} = 8388607
	h_1 = 1905	h_{25} = 7042723
	h_2 = 3834	h_{26} = 4768946
	h_3 = 5118	h_{27} = 2266428
	h_4 = 365	h_{28} = 189436
	h_5 = -14518	h_{29} = -1053303
	h_6 = -39787	h_{30} = -1392827
	h_7 = -67365	h_{31} = -1084130
	h_8 = -69909	h_{32} = -496361
	h_9 = -19450	h_{33} = 39864
	h_{10} = 97434	h_{34} = 332367
	h_{11} = 258881	h_{35} = 375562
	h_{12} = 375562	h_{36} = 258881
	h_{13} = 332367	h_{37} = 97434
	h_{14} = 39864	h_{38} = -19450
	h_{15} = -496361	h_{39} = -69909
	h_{16} = -1084130	h_{40} = -67365
	h_{17} = -1392827	h_{41} = -39787
	h_{18} = -1053303	h_{42} = -14518
	h_{19} = 189436	h_{43} = 365
	h_{20} = 2266428	h_{44} = 5118
	h_{21} = 4768946	h_{45} = 3834
	h_{22} = 7042723	h_{46} = 1905
	h_{23} = 8388607	h_{47} = 558
FIR1 (Coefficient set 1) Low pass, SINC compensation Minimum phase decimate by 4 48 coefficients	h_0 = 3337	h_{24} = 555919
	h_1 = 22258	h_{25} = -165441
	h_2 = 88284	h_{26} = -581479
	h_3 = 266742	h_{27} = -617500
	h_4 = 655747	h_{28} = -388985
	h_5 = 1371455	h_{29} = -99112
	h_6 = 2502684	h_{30} = 114761
	h_7 = 4031988	h_{31} = 186557
	h_8 = 5783129	h_{32} = 141374
	h_9 = 7396359	h_{33} = 58582
	h_{10} = 8388607	h_{34} = -12664
	h_{11} = 8325707	h_{35} = -42821
	h_{12} = 6988887	h_{36} = -35055
	h_{13} = 4531706	h_{37} = -16792
	h_{14} = 1507479	h_{38} = 367
	h_{15} = -1319126	h_{39} = 7929
	h_{16} = -3207750	h_{40} = 5926
	h_{17} = -3736028	h_{41} = 2892
	h_{18} = -2980701	h_{42} = 23
	h_{19} = -1421498	h_{43} = -1164
	h_{20} = 237307	h_{44} = -538
	h_{21} = 1373654	h_{45} = -238
	h_{22} = 1711919	h_{46} = 18
	h_{23} = 1322371	h_{47} = 113

Figure 27. FIR1 Coefficients

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR2 (Coefficient set 0) Low pass, passband to 40% f_s Linear phase decimate by 2 126 coefficients	h_0 = -71	h_{63} = 8388607
	h_1 = -371	h_{64} = 3875315
	h_2 = -870	h_{65} = -766230
	h_3 = -986	h_{66} = -1854336
	h_4 = 34	h_{67} = -137179
	h_5 = 1786	h_{68} = 1113788
	h_6 = 2291	h_{69} = 454990
	h_7 = 291	h_{70} = -642475
	h_8 = -2036	h_{71} = -553873
	h_9 = -943	h_{72} = 298975
	h_{10} = 2985	h_{73} = 533334
	h_{11} = 3784	h_{74} = -49958
	h_{12} = -1458	h_{75} = -443272
	h_{13} = -5808	h_{76} = -116005
	h_{14} = -1007	h_{77} = 318763
	h_{15} = 7756	h_{78} = 208018
	h_{16} = 5935	h_{79} = -187141
	h_{17} = -7135	h_{80} = -238025
	h_{18} = -11691	h_{81} = 68863
	h_{19} = 3531	h_{82} = 221211
	h_{20} = 17500	h_{83} = 22850
	h_{21} = 4388	h_{84} = -174452
	h_{22} = -20661	h_{85} = -81993
	h_{23} = -15960	h_{86} = 114154
	h_{24} = 18930	h_{87} = 109009
	h_{25} = 29808	h_{88} = -54172
	h_{26} = -9795	h_{89} = -109189
	h_{27} = -42573	h_{90} = 4436
	h_{28} = -7745	h_{91} = 90744
	h_{29} = 49994	h_{92} = 29702
	h_{30} = 33021	h_{93} = -62651
	h_{31} = -47092	h_{94} = -47092
	h_{32} = -62651	h_{95} = 33021
	h_{33} = 29702	h_{96} = 49994
	h_{34} = 90744	h_{97} = -7745
	h_{35} = 4436	h_{98} = -42573
	h_{36} = -109189	h_{99} = -9795
	h_{37} = -54172	h_{100} = 29808
	h_{38} = 109009	h_{101} = 18930
	h_{39} = 114154	h_{102} = -15960
	h_{40} = -81993	h_{103} = -20661
	h_{41} = -174452	h_{104} = 4388
	h_{42} = 22850	h_{105} = 17500
	h_{43} = 221211	h_{106} = 3531
	h_{44} = 68863	h_{107} = -11691
	h_{45} = -238025	h_{108} = -7135
	h_{46} = -187141	h_{109} = 5935
	h_{47} = 208018	h_{110} = 7756
	h_{48} = 318763	h_{111} = -1007
	h_{49} = -116005	h_{112} = -5808
	h_{50} = -443272	h_{113} = -1458
	h_{51} = -49958	h_{114} = 3784
	h_{52} = 533334	h_{115} = 2985
	h_{53} = 298975	h_{116} = -943
	h_{54} = -553873	h_{117} = -2036
	h_{55} = -642475	h_{118} = 291
	h_{56} = 454990	h_{119} = 2291
	h_{57} = 1113788	h_{120} = 1786
	h_{58} = -137179	h_{121} = 34
	h_{59} = -1854336	h_{122} = -986
	h_{60} = -766230	h_{123} = -870
	h_{61} = 3875315	h_{124} = -371
	h_{62} = 8388607	h_{125} = -71

Figure 28. FIR2 Linear Phase Coefficients

Filter Type	Filter Coefficients (normalized 24-bit)	
FIR2 (Coefficient set 1) Low pass, passband to 40% f_s Minimum phase decimate by 2 126 coefficients	h_0 = 4019	h_{63} = 67863
	h_1 = 43275	h_{64} = -190800
	h_2 = 235427	h_{65} = -128546
	h_3 = 848528	h_{66} = 114197
	h_4 = 2240207	h_{67} = 147750
	h_5 = 4525758	h_{68} = -46352
	h_6 = 7077833	h_{69} = -143269
	h_7 = 8388607	h_{70} = -13290
	h_8 = 6885673	h_{71} = 114721
	h_9 = 2483461	h_{72} = 51933
	h_{10} = -2538963	h_{73} = -75952
	h_{11} = -4800543	h_{74} = -68746
	h_{12} = -2761696	h_{75} = 38171
	h_{13} = 1426109	h_{76} = 68492
	h_{14} = 3624338	h_{77} = -7856
	h_{15} = 1820814	h_{78} = -57526
	h_{16} = -1695825	h_{79} = -12540
	h_{17} = -2885148	h_{80} = 41717
	h_{18} = -605252	h_{81} = 23334
	h_{19} = 2135021	h_{82} = -25516
	h_{20} = 1974197	h_{83} = -26409
	h_{21} = -630111	h_{84} = 11717
	h_{22} = -2168177	h_{85} = 24246
	h_{23} = -750147	h_{86} = -1620
	h_{24} = 1516192	h_{87} = -19248
	h_{25} = 1550127	h_{88} = -4610
	h_{26} = -508445	h_{89} = 13356
	h_{27} = -1686937	h_{90} = 7526
	h_{28} = -437822	h_{91} = -7887
	h_{29} = 1308705	h_{92} = -8016
	h_{30} = 1069556	h_{93} = 3559
	h_{31} = -657282	h_{94} = 7023
	h_{32} = -1301014	h_{95} = -598
	h_{33} = -30654	h_{96} = -5350
	h_{34} = 1173754	h_{97} = -1097
	h_{35} = 579643	h_{98} = 3579
	h_{36} = -803111	h_{99} = 1806
	h_{37} = -895851	h_{100} = -2058
	h_{38} = 328399	h_{101} = -1859
	h_{39} = 962522	h_{102} = 936
	h_{40} = 124678	h_{103} = 1558
	h_{41} = -820948	h_{104} = -224
	h_{42} = -466657	h_{105} = -1129
	h_{43} = 545674	h_{106} = -152
	h_{44} = 652827	h_{107} = 718
	h_{45} = -220448	h_{108} = 290
	h_{46} = -680495	h_{109} = -395
	h_{47} = -80886	h_{110} = -290
	h_{48} = 578844	h_{111} = 178
	h_{49} = 306445	h_{112} = 227
	h_{50} = -395302	h_{113} = -53
	h_{51} = -431004	h_{114} = -151
	h_{52} = 181900	h_{115} = -5
	h_{53} = 454403	h_{116} = 86
	h_{54} = 15856	h_{117} = 23
	h_{55} = -395525	h_{118} = -42
	h_{56} = -166123	h_{119} = -22
	h_{57} = 284099	h_{120} = 17
	h_{58} = 253485	h_{121} = 14
	h_{59} = -152407	h_{122} = -5
	h_{60} = -277888	h_{123} = -7
	h_{61} = 28526	h_{124} = 1
	h_{62} = 250843	h_{125} = 3

Figure 29. FIR2 Minimum Phase Coefficients

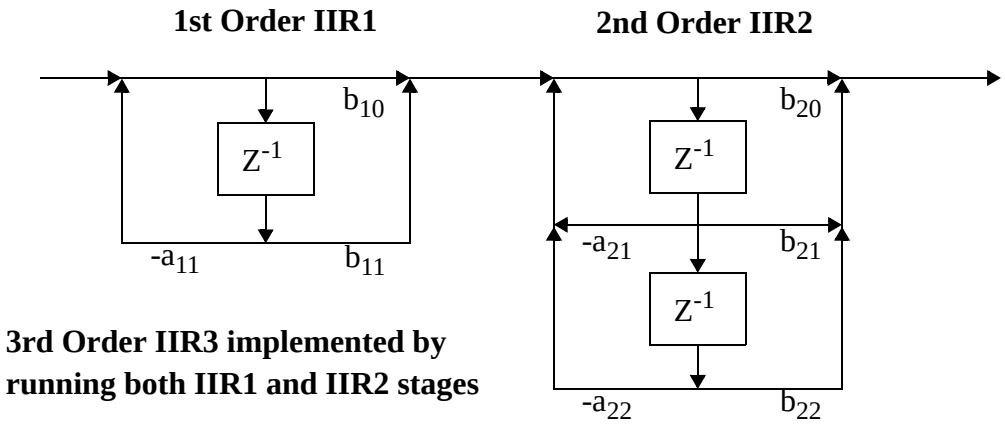


Figure 30. IIR Filter Block Diagram

14. IIR FILTER

The infinite impulse response (IIR) filter block consists of two cascaded stages, IIR1 and IIR2. It creates a high-pass corner to block very low-frequency and DC components of the input signal.

On-chip IIR1 and IIR2 coefficients can be selected using a configuration command, or the coefficients can be programmed for a custom filter response.

14.1 IIR Architecture

The architecture of the IIR filter is automatically determined when the output filter stage is selected in the FILTCFG register. Selecting the 1st order IIR1 filter bypasses the 2nd order stage, while selecting the 2nd order IIR2 filter bypasses the 1st order stage. Selection of the 3rd order IIR3 filter enables both the 1st and 2nd order stages.

14.2 IIR1 Filter

The 1st order IIR filter stage is a direct form filter with three coefficients: a11, b10, and b11. Coefficients of a 1st order IIR are inherently normalized to one, and should be scaled to 24-bit two's complement full scale, 0x7FFFFF.

The characteristic equations for the 1st order IIR include an input value, X, an output value, Y, and two intermediate values, W1 and W2, separated by a delay element (z^{-1}).

W2 = W1

W1 = X + (-a11 * W2)

Y = (W1 * b10) + (W2 * b11)

14.3 IIR2 Filter

The 2nd order IIR filter stage is a direct form filter with five coefficients: a21, a22, b20, b21, and b22. Coefficients of a 2nd order IIR are inherently normalized to two, and should be scaled to 24-bit two's complement full scale, 0x7FFFFF. Normalization effectively divides the 2nd order coefficients in half relative to the input, and requires modification of the characteristic equations.

The characteristic equations for the 2nd order IIR include an input value, X, an output value, Y, and three intermediate values, W3, W4, and W5, each separated by a delay element (z^{-1}). The following

characteristic equations model the operation of the 2nd order IIR filter with unnormalized coefficients.

W5 = W4

W4 = W3

W3 = X + (-a21 * W4) + (-a22 * W5)

Y = (W3 * b20) + (W4 * b21) + (W5 * b22)

Internally, the CS5378 uses normalized coefficients to perform the 2nd order IIR filter calculation, which changes the algorithm slightly. The following characteristic equations model the operation of the 2nd order IIR filter when using normalized coefficients.

W5 = W4

W4 = W3

W3 = 2 * [(X / 2) + (-a21 * W4) + (-a22 * W5)]

Y = 2 * [(W3 * b20) + (W4 * b21) + (W5 * b22)]

14.4 IIR3 Filter

The 3rd order IIR filter is implemented by running both the 1st order and 2nd order IIR filter stages. It can be modeled by cascading the characteristic equations of the 1st order and 2nd order IIR stages.

14.5 On-Chip IIR Coefficients

Five sets of on-chip coefficients are available for IIR1 and IIR2, each providing a 3 Hz high-pass Butterworth response at different output word rates. Characteristics of the on-chip coefficient sets are described in Figure 31 and Table 16.

Which on-chip coefficient set to use is selected by a data word following the 'Write ROM Coefficients' configuration command. See "Filter Coefficient Selection" on page 38 for information about selecting on-chip coefficient sets.

14.6 Programmable IIR Coefficients

A maximum of 3 + 5 coefficients can be programmed into IIR1 and IIR2 to create a custom filter response. Custom filter sets should normalize the coefficients to 24-bit two's complement full scale, 0x7FFFFF. To maintain maximum internal dynamic range, the CS5378 IIR filter performs double precision calculations with an automatic gain correction to scale the final output.

Custom IIR coefficients are uploaded using the 'Write IIR Coefficients' configuration command. See "EEPROM Configuration Commands" on page 27 or "Microcontroller Configuration Commands" on page 33 for information about writing custom IIR coefficients.

14.7 IIR Filter Synchronization

The IIR filter is not synchronized to the external system directly, only indirectly through the synchronization of the SINC and FIR filters. Because IIR filters have 'infinite' memory, a discontinuity in the input data stream from a synchronization event can require significant time to settle out. The exact settling time depends on the size of the discontinuity and the filter coefficient characteristics.

IIR1 - Single stage, no decimation

1st order no decimation, 3 coefficients

Coefficient set 0: high-pass, corner 0.15% f_s (3 Hz at 2000 SPS)
Coefficient set 1: high-pass, corner 0.30% f_s (3 Hz at 1000 SPS)
Coefficient set 2: high-pass, corner 0.60% f_s (3 Hz at 500 SPS)
Coefficient set 3: high-pass, corner 0.90% f_s (3 Hz at 333 SPS)
Coefficient set 4: high-pass, corner 1.20% f_s (3 Hz at 250 SPS)

IIR2 - Single stage, no decimation

2nd order no decimation, 5 coefficients

Coefficient set 0: high-pass, corner 0.15% f_s (3 Hz at 2000 SPS)
Coefficient set 1: high-pass, corner 0.30% f_s (3 Hz at 1000 SPS)
Coefficient set 2: high-pass, corner 0.60% f_s (3 Hz at 500 SPS)
Coefficient set 3: high-pass, corner 0.90% f_s (3 Hz at 333 SPS)
Coefficient set 4: high-pass, corner 1.20% f_s (3 Hz at 250 SPS)

IIR3 - Two stage, no decimation

3rd order no decimation, 8 coefficients
(Combined IIR1 and IIR2 filter responses)

Coefficient set 0,0: high-pass, corner 0.20% f_s (4 Hz at 2000 SPS)
Coefficient set 1,1: high-pass, corner 0.41% f_s (4 Hz at 1000 SPS)
Coefficient set 2,2: high-pass, corner 0.82% f_s (4 Hz at 500 SPS)
Coefficient set 3,3: high-pass, corner 1.22% f_s (4 Hz at 333 SPS)
Coefficient set 4,4: high-pass, corner 1.63% f_s (4 Hz at 250 SPS)

Figure 31. IIR Filter Stages

IIR filters

IIR1 Coeff Selection	IIR1 Corner Frequency	IIR2 Coeff Selection	IIR2 Corner Frequency	IIR3 Coeff Selection	IIR3 Corner Frequency
0	0.15% f_s	0	0.15% f_s	0,0	0.2041% f_s
1	0.30% f_s	1	0.30% f_s	1,1	0.4074% f_s
2	0.60% f_s	2	0.60% f_s	2,2	0.8152% f_s
3	0.90% f_s	3	0.90% f_s	3,3	1.2222% f_s
4	1.20% f_s	4	1.20% f_s	4,4	1.6293% f_s

Table 16. IIR Filter Characteristics

Filter Type	System Function	Filter Coefficients (normalized 24-bit)
IIR1 (Coefficient set 0) 1st order, high pass Corner at 0.15% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8309916 b_{10} = 8349262 b_{11} = -8349262
IIR1 (Coefficient set 1) 1st order, high pass Corner at 0.30% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8231957 b_{10} = 8310282 b_{11} = -8310282
IIR1 (Coefficient set 2) 1st order, high pass Corner at 0.60% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -8078179 b_{10} = 8233393 b_{11} = -8233393
IIR1 (Coefficient set 3) 1st order, high pass Corner at 0.90% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -7927166 b_{10} = 8157887 b_{11} = -8157887
IIR1 (Coefficient set 4) 1st order, high pass Corner at 1.20% f_s 3 coefficients	$H(z)=\left(\frac{b_{10}+b_{11}z^{-1}}{1+a_{11}z^{-1}}\right)$	a_{11} = -7778820 b_{10} = 8083714 b_{11} = -8083714

Filter Type	System Function	Filter Coefficients (normalized 24-bit)
IIR2 (Coefficient set 0) 2nd order, high pass Corner at 0.15% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8332704 a_{22} = 4138771 b_{20} = 4166445 b_{21} = -8332890 b_{22} = 4166445
IIR2 (Coefficient set 1) 2nd order, high pass Corner at 0.30% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8276806 a_{22} = 4083972 b_{20} = 4138770 b_{21} = -8277540 b_{22} = 4138770
IIR2 (Coefficient set 2) 2nd order, high pass Corner at 0.60% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8165041 a_{22} = 3976543 b_{20} = 4083972 b_{21} = -8167944 b_{22} = 4083972
IIR2 (Coefficient set 3) 2nd Order, high pass Corner at 0.90% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -8053350 a_{22} = 3871939 b_{20} = 4029898 b_{21} = -8059796 b_{22} = 4029898
IIR2 (Coefficient set 4) 2nd order, high pass Corner at 1.20% f_s 5 coefficients	$H(z)=\left(\frac{b_{20}+b_{21}z^{-1}+b_{22}z^{-1}}{1+a_{21}z^{-1}+a_{22}z^{-1}}\right)$	a_{21} = -7941764 a_{22} = 3770088 b_{20} = 3976539 b_{21} = -7953078 b_{22} = 3976539

Table 17. IIR Filter Coefficients

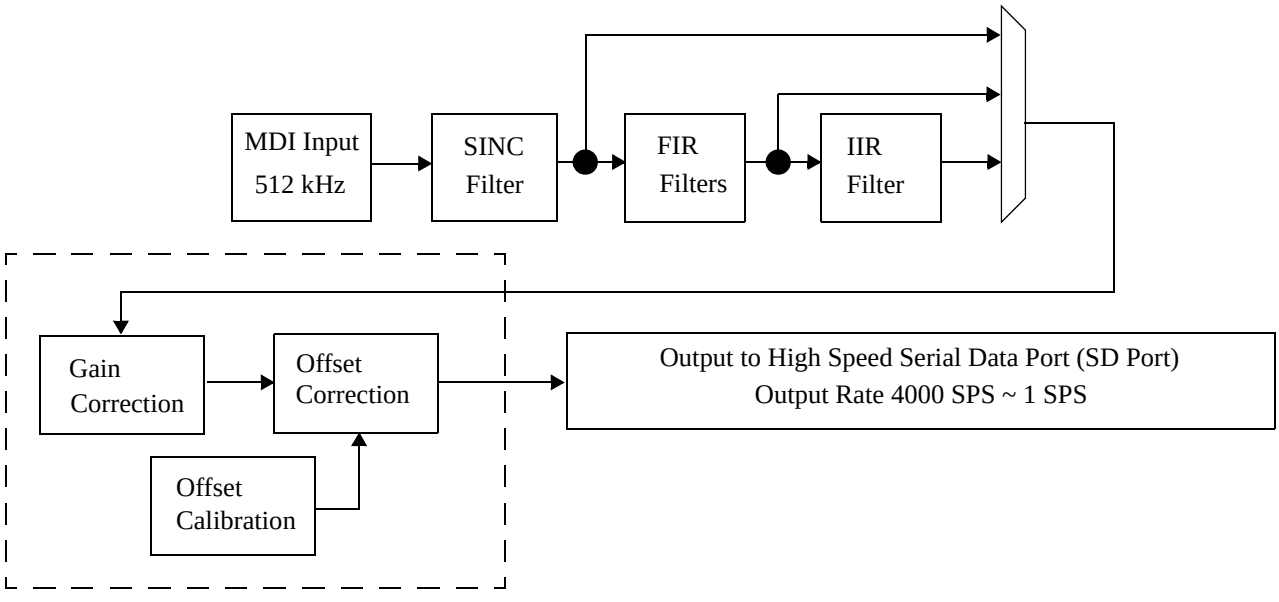


Figure 32. Gain and Offset Correction

15. GAIN AND OFFSET CORRECTION

The CS5378 digital filter can apply gain and offset corrections to the measurement data. Also, an offset calibration algorithm can automatically calculate the offset correction value.

A gain correction value is written to the GAIN registers (0x21), while an offset correction value is written to the OFFSET register (0x25). Gain and offset corrections are enabled by the USEGR and USEOR bits in the FILTCFG register (0x20).

When enabled, the offset calibration algorithm will automatically calculate an offset correction value and write it into the OFFSET register. Offset calibration is enabled by writing the EXP and ORCAL bits in FILTCFG.

15.1 Gain Correction

Gain correction in the CS5378 normalizes sensor gain in multi-sensor networks. It requires an externally calculated correction value to be written into the GAIN register (0x21).

A gain correction value is 24-bit two's complement with unity gain defined as full scale, 0x7FFFFF. Gain correction always scales to a fractional value, and can never gain the digital filter data greater than one.

Output Value = Data * (GAIN / 0x7FFFFF)

Unity Gain: GAIN = 0x7FFFFF

50% Gain: GAIN = 0x3FFFFF

Zero Gain: GAIN = 0x000000

Once the GAIN register is written, the USEGR bit in the FILTCFG register enables gain correction.

15.2 Offset Correction

Offset correction in the CS5378 cancels the DC bias of a measurement channel by subtracting the value in the OFFSET register (0x25) from the digital filter output data word.

An offset correction value is 24-bit two's complement with a maximum positive value of 0x7FFFFF,

and a maximum negative value of 0x800000. If applying an offset correction causes the final result to exceed a 24-bit two's complement maximum, the output data will saturate to that maximum value.

Output Data = Input Data - Offset Correction

Max Positive Output Value = 0x7FFFFF

Max Negative Output Value = 0x800000

Once the OFFSET register is written, the USEOR bit in the FILTCFG register enables offset correction.

15.3 Offset Calibration

An offset calibration algorithm in the CS5378 can automatically calculate an offset correction value. When using the offset calibration algorithm, background noise data should be used as the input signal for calculating the offset of the measurement channel.

The offset calibration algorithm is an exponential averaging function that places increased weight on more recent digital filter data. The exponential weighting factor is set by the EXP bits in the FILTCFG register, with larger exponent values producing a smoother averaging function that requires a longer settling time, and smaller values producing a noisier averaging function that requires a shorter settling time. Typical exponential values range from 0x05 to 0x0F, depending on the available settling time.

The characteristic equations of the offset calibration algorithm include an input value, X, an output value, Y, a summation value, YSUM, a sample index, n, and an exponential value, EXP.

$$Y(n) = X(n) - [YSUM(n-1) >> EXP]$$

$$YSUM(n) = Y(n) + YSUM(n-1)$$

$$\text{Offset Correction} = YSUM >> EXP$$

Once the EXP bits are written, the ORCAL bit in the FILTCFG register is set to enable offset calibration. When enabled, an updated offset correction value is automatically written to the OFFSET register. When the offset calibration algorithm is fully settled, the ORCAL bit should be cleared to maintain the final value in the OFFSET register.

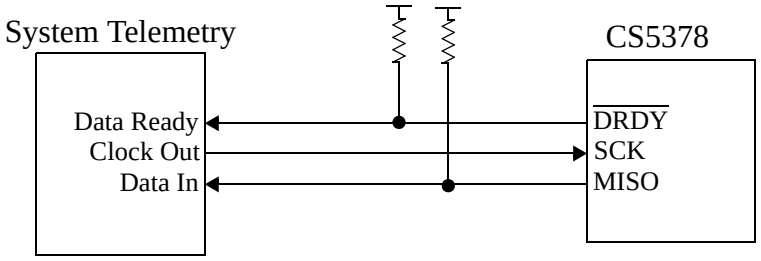


Figure 33. Serial Data Interface Block Diagram

16. SERIAL DATA INTERFACE

Once digital filtering is complete, each 24-bit output sample is combined with an 8-bit status byte. These data words are written to an 8-deep FIFO buffer and then transmitted to the communications channel through a high speed serial data interface.

16.1 Pin Descriptions

$\overline{\text{DRDY}}$ - Pin 23

Data ready output signal, active low. Open drain output requiring an external pull-up resistor.

SCK - Pin 24

Serial clock input.

MISO - Pin 25

Serial data output.

16.2 Serial Data Format

Serial data transactions transfer either 24-bit data words or 32-bit status+data words, depending on the STAT bit in the CONFIG register. When transmitting status information, each 8-bit status byte has an MFLAG bit, a time break bit, and a FIFO overflow bit encoded as shown in Figure 34.

MFLAG Bit - MFLAG

The MFLAG bit is set in the status byte when an signal is received on the MFLAG pin. When re-

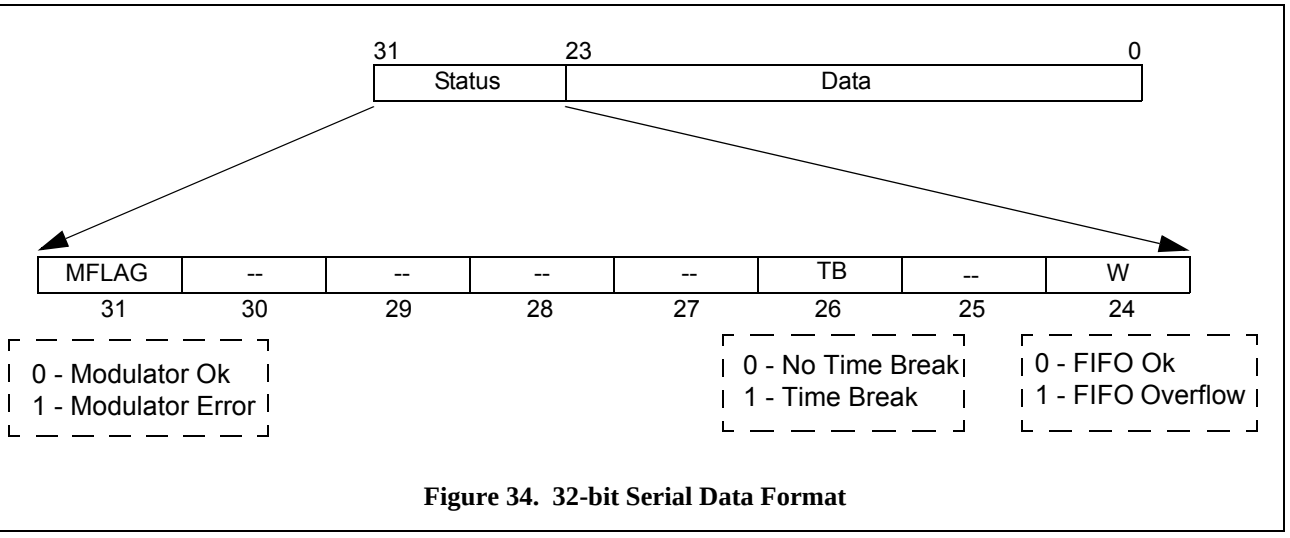


Figure 34. 32-bit Serial Data Format

ceived, the MFLAG bit is set in the next output word. See “Modulator Interface” on page 36 for more information about MFLAG.

Time Break Bit - TB

The time break bit marks a timing reference based on a rising edge into the TIMEB pin. After a programmed delay, the TB bit in the status byte is set for one output sample. The TIMEBRK digital filter register (0x29) programs the sample delay for the TB bit output. See “Time Break Controller” on page 63 for more information about time break.

FIFO Overflow Bit - W

The FIFO overflow bit indicates an error condition in the serial data FIFO, and is set if new digital filter data overwrites a FIFO location containing data which has not yet been sent.

The W bit is sticky, meaning it persists indefinitely once set. Clearing the W bit requires sending the ‘Filter Stop’ and ‘Filter Start’ configuration commands to reinitialize the data FIFO.

Conversion Data Word

The lower 24-bits of the serial data word is the conversion sample for the specified channel. Conversion data is 24-bit two’s complement format.

16.3 Serial Data Transactions

The CS5378 automatically initiates serial data transactions whenever data becomes available in the output FIFO by driving the $\overline{\text{DRDY}}$ pin low. Once a serial data transaction is initiated, serial clocks received into SCK cause data to be output to MISO, as shown in Figure 35. When all available data is read from the serial data FIFO, $\overline{\text{DRDY}}$ is released.

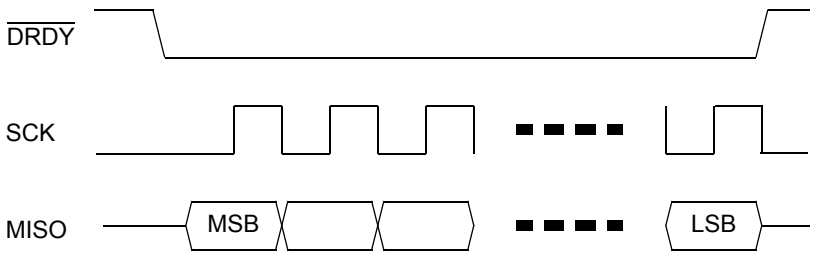


Figure 35. SD Port Transaction

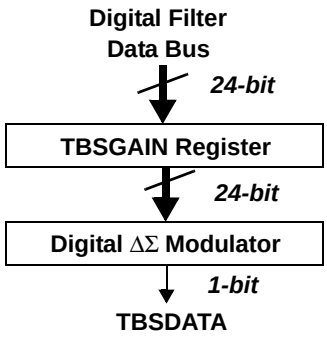


Figure 36. Test Bit Stream Generator Block Diagram

17. TEST BIT STREAM GENERATOR

The CS5378 test bit stream (TBS) generator creates sine wave ΔΣ bit stream data to drive an external test DAC. The TBS digital output can also be internally connected to the MDATA inputs for loopback testing of the digital filter.

17.1 Pin Descriptions

TBSDATA - Pin 8

Test bit stream 1-bit ΔΣ data output.

MCLK - Pin 11

Test bit stream clock output.

17.2 TBS Architecture

The test bit stream generator consists of a data interpolator and a digital ΔΣ modulator. It receives periodic 24-bit data from the digital filter to create a 1-bit ΔΣ data output on the TBSDATA pin.

The TBS input data from the digital filter is scaled by the TBSGAIN register (0x2B). Maximum stable amplitude is 0x04FFFF, with 0x04B000 approximately full scale for the CS5373A test DAC. The full scale 1-bit ΔΣ output from the TBS generator is defined as 25% minimum and 75% maximum one's density.

17.3 TBS Configuration

Configuration options for the TBS generator are set through the TBSCFG register (0x2A). Gain scaling of the TBS generator output is set by the TBSGAIN register (0x2B).

Interpolation Factor - INTP[7:0]

Selects how many times the interpolator uses a data point when generating the output bit stream. Interpolation is zero based and represents one greater than the programmed register value.

Output Rate - RATE[2:0]

Selects the TBSDATA output rate.

Synchronization - TSYNC

Enables synchronization of the TBS output phase to the MSYNC signal.

Loopback - LOOP

Enables digital loopback from the TBS output to the MDATA inputs.

Run - RUN

Enables the test bit stream generator.

Test Bit Stream Characteristic Equation:

*(Signal Freq) * (# TBS Data) * (Interpolation + 1) = Output Rate*

Example: *(31.25 Hz) * (1024) * (0x07 + 1) = 256 kHz*

Signal Frequency (TBSDATA)	Output Rate (TBSCLK)	Output Rate Selection (RATE)	Interpolation Selection (INTP)
10.00 Hz	256 kHz	0x4	0x18
10.00 Hz	512 kHz	0x5	0x31
25.00 Hz	256 kHz	0x4	0x09
25.00 Hz	512 kHz	0x5	0x13
31.25 Hz	256 kHz	0x4	0x07
31.25 Hz	512 kHz	0x5	0x0F
50.00 Hz	256 kHz	0x4	0x04
50.00 Hz	512 kHz	0x5	0x09
125.00 Hz	256 kHz	0x4	0x01
125.00 Hz	512 kHz	0x5	0x03

Table 18. TBS Configurations Using On-chip Data

Data Delay - DDLY[5:0]

Programs full period delays for TBSDATA, up to a maximum of 63 bits.

Gain - TBSGAIN[23:0]

Scales the amplitude of the sine wave output. Maximum 0x04FFFF, nominal 0x04B000.

17.4 TBS Data Source

An on-chip 24-bit 1024 point digital sine wave is stored on the CS5378 which will produce the test signal frequencies listed in Table 18. Additional discrete test frequencies and output rates can be programmed by varying the interpolation factor and output rate.

17.5 TBS Sine Wave Output

The TBS generator uses data from digital filter memory to create a sine wave test signal that can drive a test DAC. Sine wave frequency and output data rate are calculated as shown by the characteristic equation of Table 18.

The sine wave maximum ΔΣ one's density output from the TBS generator is set by the TBSGAIN register. TBSGAIN can be programmed up to a maximum of 0x04FFFF, with the TBS generator unstable for higher amplitudes. For the CS5373A test DAC, a gain value of 0x04B000 produces an approximately full scale sine wave output (5 V_{pp} differential).

17.6 TBS Loopback Testing

Included as part of the CS5378 test bit stream generator is a feedback path to the digital filter MDATA input. This loopback mode provides a fully digital signal path to test the TBS generator, digital filter, and data collection interface. Digital loopback testing expects 512 kHz ΔΣ data into the MDATA input.

A mismatch of the TBS generator full scale output and the MDATA full scale input results in an amplitude mismatch when testing in loopback mode. The TBS generator outputs a 75% maximum one's density, while the MDATA inputs expect an 86% maximum one's density from a ΔΣ modulator, resulting in a measured full scale error of approximately -3.6 dB.

17.7 TBS Synchronization

When the TSYNC bit is set in the TBSCFG register, the MSYNC signal resets the sine wave data pointer and phase aligns the TBS signal output. Once the digital filter is settled, all CS5378 devices receiving the SYNC signal will have identical TBS signal phase. See "Synchronization" on page 24 for more information about the SYNC and MSYNC signals.

If TSYNC is clear, MSYNC has no effect on the TBS data pointer and no change in the TBS output phase will occur during synchronization.

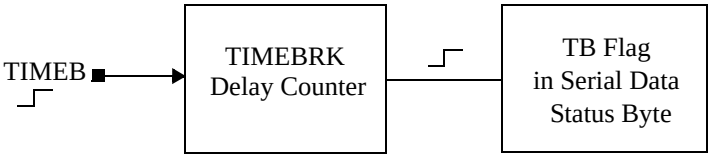


Figure 37. Time Break Block Diagram

18. TIME BREAK CONTROLLER

A time break signal is used to mark timing events that occur during measurement. An external signal sets a flag in the status byte of an output sample to mark when the external event occurred.

A rising edge input to the TIMEB pin causes the TB timing reference flag to be set in the serial data status byte. When set, the TB flag appears for only one output sample in the status byte. The TB flag output can be delayed by programming a sample delay value into the TIMEBRK digital filter register.

18.1 Pin Description

TIMEB - Pin 20

Time break input pin, rising edge triggered.

18.2 Time Break Operation

An externally generated timing reference signal applied to the TIMEB pin initiates an internal sample counter. After a number of output samples have passed, programmed in the TIMEBRK digital filter register (0x29), the TB flag is set in the status byte of the serial data output word. The TB flag is automatically cleared for subsequent data words, and appears for only one output sample.

18.3 Time Break Delay

The TIMEBRK register (0x29) sets a sample delay between a received rising edge on the TIMEB pin and writing the TB flag into the serial data status byte.

The programmable sample counter can compensate for group delay through the digital filters. When the proper group delay value is programmed into the TIMEBRK register, the TB flag will be set in the status byte of the measurement sample taken when the timing reference signal was received.

18.3.1 Step Input and Group Delay

A simple method to empirically measure the step response and group delay of a CS5378 measurement channel is to use the time break signal as both a timing reference input and an analog step input.

When a rising edge is received on the TIMEB pin with no delay programmed into the TIMEBRK register, the TB flag is set in the next serial data status byte. The same rising edge can act as a step input to the analog channel, propagating through the digital filter to appear as a rising edge in the measurement data. By comparing the timing of the TB status flag output and the rising edge in the measurement data, the measurement channel group delay can be determined.

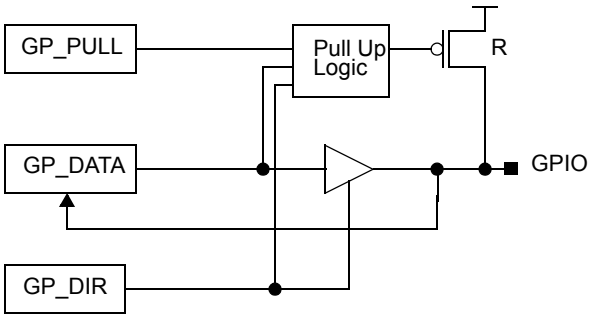


Figure 38. GPIO Block Diagram

19. GENERAL PURPOSE I/O

The General Purpose I/O (GPIO) block provides 8 general purpose pins to interface with external hardware.

19.1 Pin Descriptions

GPIO[3:0] - Pins 4 - 1

Standard GPIO pins.

GPIO[6:4]:PLL[2:0] - Pins 7 - 5

Standard GPIO pins also used to select the PLL mode after reset. Internal pull-ups default high, 10 kΩ external pull-downs required to set low.

GPIO7:BOOT - Pin 28

Standard GPIO pin also used to select boot mode after reset. Internal pull-up defaults high, 10 kΩ external pull-down required to set low.

19.2 GPIO Architecture

Each GPIO pin can be configured as input or output, high or low, with a weak (~100 kΩ) internal pull-up resistor enabled or disabled. Figure 38 shows the structure of a bi-directional GPIO pin.

19.3 GPIO Registers

GPIO pin settings are programmed in the GPCFG register. GP_DIR bits set the input/output mode, GP_PULL bits enable/disable the internal pull-up resistor, and GP_DATA bits set the output data value. After reset, GPIO pins default as inputs with pull-up resistors enabled.

19.4 GPIO Input Mode

When reading a value from the GP_DATA bits, the returned data reports the current state of the pins. If a pin is externally driven high it reads a logical 1, if externally driven low it reads a logical 0. When a GPIO pin is used as an input, the pull-up resistor should be disabled to save power if it isn't required.

19.5 GPIO Output Mode

When a GPIO pin is programmed as an output with a data value of 0, the pin is driven low and the internal pull-up resistor is automatically disabled. When programmed as an output with a data value of 1, the pin is driven high and the pull-up resistor is inconsequential.

Any GPIO pin can be used as an open-drain output by setting the data value to 0, enabling the pull-up, and using the GP_DIR direction bits to control the pin value. This open-drain output configuration uses the internal pull-up resistor to hold the pin high when GP_DIR is set as an input, and drives the pin low when GP_DIR is set as an output.

19.5.1 GPIO Reads in Output Mode

When reading GPIO pins the GP_DATA register value always reports the current state of the pins, so a value written in output mode does not necessarily read back the same value. If a pin in output mode is written as a logical 1, the CS5378 attempts to drive the pin high. If an external device forces the pin low, the read value reflects the pin state and returns a logical 0. Similarly, if an output pin is written as a logical 0 but forced high externally, the read value reflects the pin state and returns a logical 1. In both cases the CS5378 is in contention with the external device resulting in increased power consumption.

20. REGISTER SUMMARY

20.1 SPI Registers

The CS5378 SPI registers interface the serial port to the digital filter.

Name	Addr.	Type	# Bits	Description
SPICTRLH	00	R/W	8	SPI Control Register, High Byte
SPICTRLM	01	R/W	8	SPI Control Register, Middle Byte
SPICTRLL	02	R/W	8	SPI Control Register, Low Byte
SPICMDH	03	R/W	8	SPI Command, High Byte
SPICMDM	04	R/W	8	SPI Command, Middle Byte
SPICMDL	05	R/W	8	SPI Command, Low Byte
SPIDAT1H	06	R/W	8	SPI Data 1, High Byte
SPIDAT1M	07	R/W	8	SPI Data 1, Middle Byte
SPIDAT1L	08	R/W	8	SPI Data 1, Low Byte
SPIDAT2H	09	R/W	8	SPI Data 2, High Byte
SPIDAT2M	0A	R/W	8	SPI Data 2, Middle Byte
SPIDAT2L	0B	R/W	8	SPI Data 2, Low Byte

20.1.1 SPICTRL : 0x00, 0x01, 0x02

Figure 39. SPI Control Register SPICTRL

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	--	--	--	--
R/W	R/W1	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	1

15	14	13	12	11	10	9	8
SMODF	--	--	EMOP	SWEF	--	--	E2DREQ
R	R/W	R	R	R	R/W	R/W	R/W
0	0	0	0	0	0	1	0

7	6	5	4	3	2	1	(LSB) 0
--	--	--	--	--	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	1	0	0	0	0	0

SPI Address: 0x00 0x01 0x02

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	--	reserved	15	SMODF	SPI mode fault flag	7:0	--	reserved
			14:13	--	reserved			
			12	EMOP	External master to SPI operation in progress flag			
			11	SWEF	SPI write collision error flag			
			10:9	--	reserved			
			8	E2DREQ	External master to digital filter request flag			

20.1.2 SPICMD : 0x03, 0x04, 0x05

Figure 40. SPI Command Register SPICMD

(MSB) 23	22	21	20	19	18	17	16
SCMD23	SCMD22	SCMD21	SCMD20	SCMD19	SCMD18	SCMD17	SCMD16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SCMD15	SCMD14	SCMD13	SCMD12	SCMD11	SCMD10	SCMD9	SCMD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SCMD7	SCMD6	SCMD5	SCMD4	SCMD3	SCMD2	SCMD1	SCMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI Address: 0x03 0x04 0x05

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	SCMD[23:16]	SPI Command High Byte	15:8	SCMD[15:8]	SPI Command Middle Byte	15:8	SCMD[7:0]	SPI Command Low Byte

20.1.3 SPIDAT1 : 0x06, 0x07, 0x08

Figure 41. SPI Data Register SPIDAT1

(MSB) 23	22	21	20	19	18	17	16
SDAT23	SDAT22	SDAT21	SDAT20	SDAT19	SDAT18	SDAT17	SDAT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SDAT15	SDAT14	SDAT13	SDAT12	SDAT11	SDAT10	SDAT9	SDAT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI Address: 0x06 0x07 0x08

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 SDAT[23:16] SPI Data High Byte	15:8 SDAT[15:8] SPI Data Middle Byte	15:8 SDAT[7:0] SPI Data Low Byte

20.1.4 SPIDAT2 : 0x09, 0x0A, 0x0B

Figure 42. SPI Data Register SPIDAT2

(MSB) 23	22	21	20	19	18	17	16
SDAT23	SDAT22	SDAT21	SDAT20	SDAT19	SDAT18	SDAT17	SDAT16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SDAT15	SDAT14	SDAT13	SDAT12	SDAT11	SDAT10	SDAT9	SDAT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SDAT7	SDAT6	SDAT5	SDAT4	SDAT3	SDAT2	SDAT1	SDAT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

SPI Address: 0x09
0x0A
0x0B

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 SDAT[23:16] SPI Data High Byte	15:8 SDAT[15:8] SPI Data Middle Byte	15:8 SDAT[7:0] SPI Data Low Byte

20.2 Digital Filter Registers

The CS5378 digital filter registers control hardware peripherals and filtering functions.

Name	Addr.	Type	# Bits	Description
CONFIG	00	R/W	24	Hardware Configuration
RESERVED	01-0D	R/W	24	Reserved
GPCFG	0E	R/W	24	GPIO[7:0] Direction, Pull-Up Enable, and Data
RESERVED	0F-1F	R/W	24	Reserved
FILTCFG	20	R/W	24	Digital Filter Configuration
GAIN	21	R/W	24	Gain Correction
RESERVED	22-24	R/W	24	Reserved
OFFSET	25	R/W	24	Offset Correction
RESERVED	26-28	R/W	24	Reserved
TIMEBRK	29	R/W	24	Time Break Delay
TBSCFG	2A	R/W	24	Test Bit Stream Configuration
TBSGAIN	2B	R/W	24	Test Bit Stream Gain
SYSTEM1	2C	R/W	24	User Defined System Register 1
SYSTEM2	2D	R/W	24	User Defined System Register 2
VERSION	2E	R/W	24	Hardware Version ID
SELFTEST	2F	R/W	24	Self-Test Result Code

20.2.1 CONFIG : 0x00

Figure 43. Hardware Configuration Register CONFIG

(MSB)23	22	21	20	19	18	17	16
--	--	--	--	--	DFS2	DFS1	DFS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	1

15	14	13	12	11	10	9	8
--	--	--	--	--	MCKFS2	MCKFS1	MCKFS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	0	0

7	6	5	4	3	2	1	(LSB)0
STAT	--	--	MCKEN	MDIFS	--	BOOT	MSEN
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
0	0	0	0	0	0	0	1

DF Address: 0x00

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:19	--	reserved
18:16	DFS [2:0]	Digital filter frequency select 111: Reserved 110: 8.192 MHz 101: 4.096 MHz 100: 2.048 MHz 011: 1.024 MHz 010: 512 kHz 001: 256 kHz 000: 32 kHz
15:11	--	reserved
10:8	MCKFS [2:0]	MCLK frequency select 111: reserved 110: reserved 101: 4.096 MHz 100: 2.048 MHz 011: 1.024 MHz 010: 512 kHz 001: reserved 000: reserved
7:6	STAT	Serial Data Status Byte 1: Disabled (24-bit output) 0: Enabled (32-bit output)
5	--	reserved
4	MCKEN	MCLK output enable 1: Enabled 0: Disabled
3	MDIFS	MDATA input frequency select 1: 256 kHz 0: 512 kHz
2	--	reserved
1	BOOT	Boot source indicator 1: Booted from EEPROM 0: Booted from Micro
0	MSEN	MSYNC enable 1: MSYNC generated 0: MSYNC remains low

20.2.2 GPCFG : 0x0E

Figure 44. GPIO Configuration Register GPCFG

(MSB) 23	22	21	20	19	18	17	16
GP_DIR7	GP_DIR6	GP_DIR5	GP_DIR4	GP_DIR3	GP_DIR2	GP_DIR1	GP_DIR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
GP_PULL7	GP_PULL6	GP_PULL5	GP_PULL4	GP_PULL3	GP_PULL2	GP_PULL1	GP_PULL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

7	6	5	4	3	2	1	(LSB) 0
GP_DATA7	GP_DATA6	GP_DATA5	GP_DATA4	GP_DATA3	GP_DATA2	GP_DATA1	GP_DATA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	1	1	1	1

DF Address: 0x0E

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	GP_DIR [7:0]	GPIO pin direction 1: Output 0: Input	15:8	GP_PULL [7:0]	GPIO pullup resistor 1: Enabled 0: Disabled	7:0	GP_DATA [7:0]	GPIO data value 1: VDD 0: GND

Notes:

GPIO[7] also used as BOOT mode select after reset

GPIO[6:4] also used as PLL mode select after reset.

20.2.3 FILTCFG : 0x20

Figure 45. Filter Configuration Register FILTCFG

(MSB) 23	22	21	20	19	18	17	16
--	--	--	EXP4	EXP3	EXP2	EXP1	EXP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
--	ORCAL	USEOR	USEGR	--	FSEL2	FSEL1	FSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
DEC3	DEC2	DEC1	DEC0	--	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x20

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:21	--	reserved	15	--	reserved	7:4	DEC[3:0]	Decimation selection (Output word rate)
20:16	EXP[4:0]	OFFSET calibration exponent	14	ORCAL	Run OFFSET calibration 1: Enable 0: Disable			0111: 4000 SPS 0110: 2000 SPS 0101: 1000 SPS 0100: 500 SPS 0011: 333 SPS
			13	USEOR	Use OFFSET correction 1: Enable 0: Disable			0010: 250 SPS 0001: 200 SPS 0000: 125 SPS 1111: 100 SPS 1110: 50 SPS
			12	USEGR	Use GAIN correction 1: Enable 0: Disable			1101: 40 SPS 1100: 25 SPS 1011: 20 SPS 1010: 10 SPS 1001: 5 SPS 1000: 1 SPS
			11	--	reserved	3:0	--	reserved
			10:8	FSEL[2:0]	Output filter stage select 111: reserved 110: reserved 101: IIR 3rd Order 100: IIR 2nd Order 011: IIR 1st Order 010: FIR2 Output 001: FIR1 Output 000: SINC Output			

20.2.4 GAIN : 0x21

Figure 46. Gain Correction Register GAIN

(MSB) 23	22	21	20	19	18	17	16
GAIN23	GAIN22	GAIN21	GAIN20	GAIN19	GAIN18	GAIN17	GAIN16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
GAIN15	GAIN14	GAIN13	GAIN12	GAIN11	GAIN10	GAIN9	GAIN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
GAIN7	GAIN6	GAIN5	GAIN4	GAIN3	GAIN2	GAIN1	GAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x21

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 GAIN[23:16] Gain Correction Upper Byte	15:8 GAIN[15:8] Gain Correction Middle Byte	15:8 GAIN[7:0] Gain Correction Lower Byte

20.2.5 OFFSET : 0x25

Figure 47. Offset Correction Register OFFSET

(MSB) 23	22	21	20	19	18	17	16
OFST23	OFST22	OFST21	OFST20	OFST19	OFST18	OFST17	OFST16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
OFST15	OFST14	OFST13	OFST12	OFST11	OFST10	OFST9	OFST8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
OFST7	OFST6	OFST5	OFST4	OFST3	OFST2	OFST1	OFST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x25

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 OFST[23:16] Offset Correction Upper Byte	15:8 OFST[15:8] Offset Correction Middle Byte	15:8 OFST[7:0] Offset Correction Lower Byte

20.2.6 TIMEBRK : 0x29

Figure 48. Time Break Counter Register TIMEBRK

(MSB) 23	22	21	20	19	18	17	16
TBRK23	TBRK22	TBRK21	TBRK20	TBRK19	TBRK18	TBRK17	TBRK16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
TBRK15	TBRK14	TBRK13	TBRK12	TBRK11	TBRK10	TBRK9	TBRK8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
TBRK7	TBRK6	TBRK5	TBRK4	TBRK3	TBRK2	TBRK1	TBRK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x29

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 TBRK[23:16] Time Break Counter Upper Byte	15:8 TBRK[15:8] Time Break Counter Middle Byte	15:8 TBRK[7:0] Time Break Counter Lower Byte

20.2.7 TBSCFG : 0x2A

Figure 49. Test Bit Stream Configuration Register TBSCFG

(MSB) 23	22	21	20	19	18	17	16
INTP7	INTP6	INTP5	INTP4	INTP3	INTP2	INTP1	INTP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
--	RATE2	RATE1	RATE0	TSYNC	--	--	--
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
LOOP	RUN	DDLY5	DDLY4	DDLY3	DDLY2	DDLY1	DDLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2A

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	INTP[7:0]	Interpolation factor 0xFF: 256 0xFE: 255 ... 0x01: 2 0x00: 1 (use once)	15	--	reserved	7	LOOP	Loopback TBSDATA output to MDATA inputs 1: Enabled 0: Disabled
			14:12	RATE[2:0]	TBSDATA and TBSCLK output rate. 111: 2.048 MHz 110: 1.024 MHz 101: 512 kHz 100: 256 kHz 011: 128 kHz 010: 64 kHz 001: 32 kHz 000: 4 kHz	6	RUN	Run Test Bit Stream 1: Enabled 0: Disabled
			11	TSYNC	Synchronization 1: Sync enabled 0: No sync	5:0	DDLY[5:0]	TBSDATA output delay 0x3F: 63 bits 0x3E: 62 bits ... 0x01: 1 bit 0x00: 0 bits (no delay)
			10:8	--	reserved			

20.2.8 TBSGAIN : 0x2B

Figure 50. Test Bit Stream Gain Register TBSGAIN

(MSB) 23	22	21	20	19	18	17	16
TGAIN23	TGAIN22	TGAIN21	TGAIN20	TGAIN19	TGAIN18	TGAIN17	TGAIN16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
TGAIN15	TGAIN14	TGAIN13	TGAIN12	TGAIN11	TGAIN10	TGAIN9	TGAIN8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
TGAIN7	TGAIN6	TGAIN5	TGAIN4	TGAIN3	TGAIN2	TGAIN1	TGAIN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2B

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16 TGAIN[23:16] Test Bit Stream Gain Upper Byte	15:8 TGAIN[15:8] Test Bit Stream Gain Middle Byte	15:8 TGAIN[7:0] Test Bit Stream Gain Lower Byte

20.2.9 SYSTEM1, SYSTEM2 : 0x2C, 0x2D

Figure 51. User Defined System Register SYSTEM1

(MSB) 23	22	21	20	19	18	17	16
SYS23	SYS22	SYS21	SYS20	SYS19	SYS18	SYS17	SYS16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

15	14	13	12	11	10	9	8
SYS15	SYS14	SYS13	SYS12	SYS11	SYS10	SYS9	SYS8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

7	6	5	4	3	2	1	(LSB) 0
SYS7	SYS6	SYS5	SYS4	SYS3	SYS2	SYS1	SYS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

DF Address: 0x2C

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	SYS[23:16]	System Register Upper Byte	15:8	SYS[15:8]	System Register Middle Byte	15:8	SYS[7:0]	System Register Lower Byte

20.2.10 VERSION : 0x2E

Figure 52. Hardware Version ID Register VERSION

(MSB) 23	22	21	20	19	18	17	16
TYPE7	TYPE6	TYPE5	TYPE4	TYPE3	TYPE2	TYPE1	TYPE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	1	1	1	1	0	0	0

15	14	13	12	11	10	9	8
HW7	HW6	HW5	HW4	HW3	HW2	HW1	HW0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

7	6	5	4	3	2	1	(LSB) 0
ROM7	ROM6	ROM5	ROM4	ROM3	ROM2	ROM1	ROM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	0

DF Address: 0x2E

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:16	TYPE [7:0]	Chip Type 78 - CS5378	15:8	HW [7:0]	Hardware Revision 01 - CS5378 Rev A 02 - CS5378 Rev B	7:4	ROM [7:0]	ROM Version 01 - Ver 1.0 02 - Ver 2.0

20.2.11 SELFTEST : 0x2F

Figure 53. Self Test Result Register SELFTEST

(MSB) 23	22	21	20	19	18	17	16
--	--	--	--	EU3	EU2	EU1	EU0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	1	0

15	14	13	12	11	10	9	8
DRAM3	DRAM2	DRAM1	DRAM0	PRAM3	PRAM2	PRAM1	PRAM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

7	6	5	4	3	2	1	(LSB) 0
DROM3	DROM2	DROM1	DROM0	PROM3	PROM2	PROM1	PROM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

DF Address: 0x2F

--	Not defined; read as 0
R	Readable
W	Writable
R/W	Readable and Writable

Bits in bottom rows are reset condition

Bit definitions:

23:20	--	reserved	15:12	DRAM [3:0]	Data RAM Test 'A': Pass 'F': Fail	7:4	DROM [3:0]	Data ROM Test 'A': Pass 'F': Fail
19:16	EU [3:0]	Execution Unit Test 'A': Pass 'F': Fail	11:8	PRAM [3:0]	Program RAM Test 'A': Pass 'F': Fail	3:0	PROM [3:0]	Program ROM Test 'A': Pass 'F': Fail

21. PIN DESCRIPTION

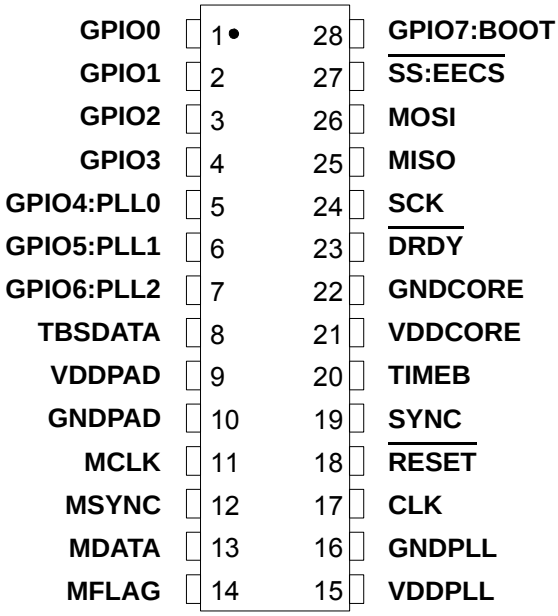


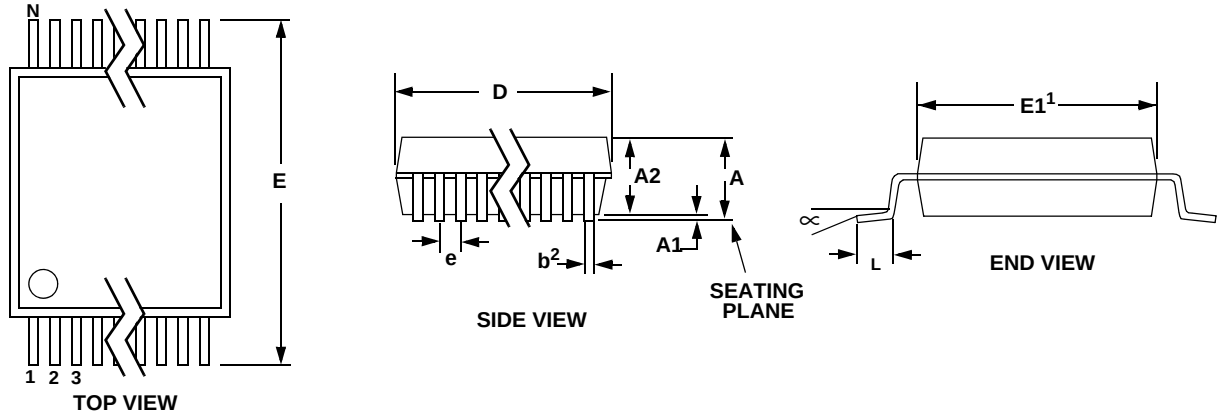
Figure 54. CS5378 Pin Assignments

<table>
<tr><th>Pin Name</th><th>Pin Number</th><th>Pin Type</th><th>Pin Description</th></tr>
<tr><td colspan="4">General Purpose Input / Output</td></tr>
<tr><td>GPIO[0:3]</td><td>1, 2, 3, 4</td><td>Input / Output</td><td>General Purpose I/O.</td></tr>
<tr><td>GPIO[4:6]:PLL[0:2]</td><td>5, 6, 7</td><td>Input / Output</td><td>General Purpose I/O with PLL mode select.
GPIO pins have weak (~100 kΩ) internal pull-ups.
PLL mode selection latched immediately after reset.
<table>
<tr><th>PLL[2:0]</th><th>Reset Mode</th></tr>
<tr><td>111</td><td>32.768 MHz clock input (PLL bypass).</td></tr>
<tr><td>110</td><td>1.024 MHz clock input.</td></tr>
<tr><td>101</td><td>2.048 MHz clock input.</td></tr>
<tr><td>100</td><td>4.096 MHz clock input.</td></tr>
<tr><td>011</td><td>32.768 MHz clock input (PLL bypass).</td></tr>
<tr><td>010</td><td>1.024 MHz Manchester input.</td></tr>
<tr><td>001</td><td>2.048 MHz Manchester input.</td></tr>
<tr><td>000</td><td>4.096 MHz Manchester input.</td></tr>
</table></td></tr>
<tr><td>GPIO7:BOOT</td><td>28</td><td>Input / Output</td><td>General Purpose I/O with boot mode select.
GPIO pins have weak (~100 kΩ) internal pull-ups.
Boot mode selection latched immediately after reset.
<table>
<tr><th>BOOT</th><th>Reset Mode</th></tr>
<tr><td>1</td><td>EEPROM boot</td></tr>
<tr><td>0</td><td>Microcontroller boot</td></tr>
</table></td></tr>
</table>

Pin Name	Pin Number	Pin Type	Pin Description
Test Bit Stream			
TBSDATA	8	Output	Test bit stream data output.
Modulator Interface			
MCLK	11	Output	Modulator clock output.
MSYNC	12	Output	Modulator sync output.
MDATA	13	Input	Modulator data input.
MFLAG	14	Input	Modulator flag input.
Telemetry Interface			
CLK	17	Input	Clock input.
RESET	18	Input	Reset, active low.
SYNC	19	Input	Sync input.
TIMEB	20	Input	Time break input.
Serial Interface			
$\overline{\text{DRDY}}$	23	Output	Data ready, active low.
SCK	24	Input / Output	Serial clock.
MISO	25	Input / Output	Serial data, master in / slave out.
MOSI	26	Input / Output	Serial data, master out / slave in.
$\overline{\text{SS:EECS}}$	27	Input	Slave select with EEPROM chip select, active low.
Power Supplies			
VDDPAD, GNDPAD	9, 10	Supply	Pin power supply.
VDDPLL, GNDPLL	15, 16	Supply	PLL power supply.
VDDCORE, GNDCORE	21, 22	Supply	Logic core power supply.

22.PACKAGE DIMENSIONS

28L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.15	0.25	
A2	0.064	0.069	0.074	1.62	1.75	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.390	0.4015	0.413	9.90	10.20	10.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.0354	0.041	0.63	0.90	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters

23.ORDERING INFORMATION

Model	Temperature	Package
CS5378-ISZ (Lead Free)	-40 to +85 °C	28-pin SSOP

24.ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5378-ISZ (Lead Free)	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

25.REVISION HISTORY

Revision	Date	Changes
PP1	FEB 2004	Initial “Preliminary Product” release.
F1	OCT 2005	Added lead-free device ordering information. Added MSL data.
F2	SEP 2008	Rev B. Update Single-S part numbers. Remove TBS impulse mode.
F3	OCT 2010	Removed lead-containing device ordering information.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
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