THE DATASHEET OF

LM2657MTC/NOPB

LM2657 Dual Synchronous Buck Regulator Controller

Check for Samples: LM2657

FEATURES

- **Input Voltage Range from 4.5V to 28V**
- **Synchronous Dual-Channel Interleaved Switching**
- **Forced-PWM or Pulse-Skip Modes**
- **Lossless Bottom-Side FET Current Sensing**
- **Adaptive Duty Cycle Clamp**
- **High Current N-Channel FET Drivers**
- **Low Shutdown Supply Current**
- **Reference Voltage Accurate to within ±1.5%**
- **Output Voltage Adjustable Down to 0.6V**
- **Power Good Flag and Chip Enable**
- **Under-Voltage Lockout**
- **Over-Voltage/Under-Voltage Protection**
- **Soft-Start**
- **Switching Frequency Adjustable 200kHz-500kHz**
- **28-Pin TSSOP Package**

APPLICATIONS

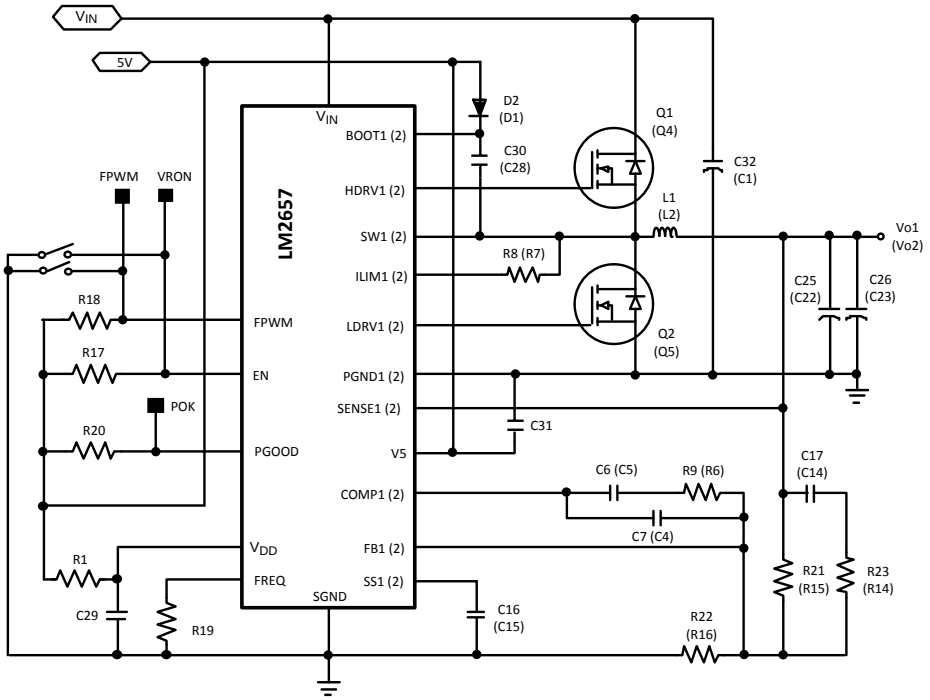
- **Low Output Voltage High-Efficiency Buck Regulators**

DESCRIPTION

The LM2657 is an adjustable 200kHz-500kHz dual channel voltage-mode controlled high-speed synchronous buck regulator controller ideally suited for high current applications. The LM2657 requires only N-channel FETs for both the upper and lower positions of each stage. It features line feedforward to improve the response to input transients. At very light loads, the user can choose between the high-efficiency Pulse-skip mode or the constant frequency Forced-PWM mode. Lossless current limiting without the use of external sense resistors is made possible by sensing the voltage drop across the bottom FET. A unique adaptive duty cycle clamping technique is incorporated to significantly reduce peak currents under abnormal load conditions. The two independently programmable outputs switch 180° out of phase (interleaved switching) reducing the input capacitor and filter requirements. The input voltage range is 4.5V to 28V while the output voltages are adjustable down to 0.6V.

Standard supervisory and control features include Soft-start, Power Good, output Under-voltage and Over-voltage protection, Under-voltage Lockout, and chip Enable.

Typical Application (Channel 2 in parenthesis)



Connection Diagram

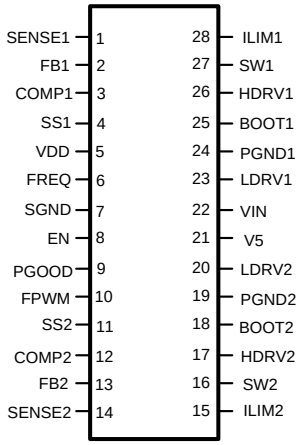


Figure 1. 28-Pin TSSOP (Top View)
See PW Package

PIN DESCRIPTION

Pin 1, SENSE1:	Output voltage sense pin for Channel 1. It is tied directly to the output rail. The SENSE pin voltage is used by the IC, together with the VIN voltage (Pin 22) to calculate the CCM (continuous conduction mode) duty cycle. This is used by the IC to set the minimum duty cycle in the SKIP mode to 85% of the CCM value. It is also used to set the adaptive duty cycle clamp (see Pin 3).
Pin 2, FB1:	Feedback pin for Channel 1. This is the inverting input of the channel's error amplifier. The voltage on this pin under regulation is nominally at 0.6V. A 'Power Good window' on this pin determines if the output voltage is within regulation limits (±13%). If the voltage (on either channel) falls outside this window for more than 7µs, 'Power Not Good' is signaled on the PGOOD pin (Pin 9). Additionally, if the FB voltage is above the upper limit, an over-voltage fault condition occurs which turns on the low-side FET. The part will resume normal operation on the next high side cycle in which no fault is detected. When single channel operation is desired (one channel is used, the other is disabled), the feedback pins of both channels must be connected together, near the IC. All other pins specific to the unused channel should be left floating (not connected to each other, either).

PIN DESCRIPTION (continued)

Pin 3, COMP1:	Compensation pin for Channel 1. This is the output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to set the duty cycle for normal regulation. Since the Feedback pin is the inverting input of the same error amplifier, the appropriate control loop compensation components are placed between this pin and the Feedback pin. The COMP pin is internally pulled low during Soft-start to limit the duty cycle. Once Soft-start is completed, the voltage on this pin can take up the value required to maintain output regulation. Note that an internal voltage clamp does not allow the pin to go much higher than the steady-state requirement. This forms the 'adaptive duty cycle clamp' circuit, which serves to limit the maximum allowable duty cycle and peak currents under sudden overloads. Also note that this clamp has been designed with enough 'headroom' to permit an adequate response to step loads within normal operating range.
Pin 4, SS1:	Channel 1 Soft-start pin. A Soft-start capacitor is placed between this pin and ground. A typical capacitance of 0.1µF is recommended. During startup using chip Enable/power-up, soft-start is reset by connecting an internal 1.8 kΩ resistor between this pin and ground (R_{SS_DCHG}, see ELECTRICAL CHARACTERISTICS table). It discharges any remaining charge on the Soft-start capacitors to ensure that the voltage on both Soft-start pins is below 100mV. Reset having thus been obtained, an 11µA current source at this pin charges up the Soft-start capacitor. The voltage on this pin controls the maximum duty cycle, and this produces a gradual ramp-up of the output voltage, thereby preventing large inrush currents into the output capacitors. The voltage on this pin finally clamps close to 5V. During current limit, V_{DD} UVLO, or V_{IN} UVLO this pin is connected to an internal 115µA current sink whenever a current limit event is in progress. This sink current quickly discharges the Soft-start capacitor and forces the duty cycle low to protect the power components.
Pin 5, VDD:	5V supply rail for the control and logic sections of both channels. For normal operation to start, the voltage on this pin must be brought above 4.5V. Subsequently, the voltage on this pin (including any ripple component) should not be allowed to fall below 4V for a duration longer than 7µs. Since this pin is also the supply rail for the internal control sections, it should be well-decoupled particularly at high frequencies. A minimum 0.1µF-0.47µF (ceramic) capacitor should be placed on the component side very close to the IC with no intervening vias between this capacitor and the V_{DD}/SGND pins. If the voltage on Pin 5 falls below the lower UVLO threshold, the upper and lower FETs are both turned OFF. 'Power Not Good' is also signaled immediately (on Pin 9.) Normal operation will resume once the fault condition has cleared. Additionally if the voltage on this pin falls below the minimum voltage required for logic operation (about 1.8V typ) the part will shutdown identically to enable (see pin 8) being pulled low.
Pin 6, FREQ:	Frequency adjust pin. The switching frequency (for both channels) is set by a resistor connected between this pin and ground. A value of 22.1kΩ sets the frequency to 300kHz (nominal). If the resistance is increased, the switching frequency falls. An approximate relationship is that for every 7.3kΩ increase (or decrease) in the value of the frequency adjust resistance, the time period (1/f) increases (or decreases) by about 1µs.
Pin 7, SGND:	Signal Ground pin. This is the lower rail for the control and logic sections of both channels. SGND should be connected on the PCB to the system ground, which in turn is connected to PGND1 and PGND2. The layout is important and the recommendations in the section LAYOUT GUIDELINES should be followed.
Pin 8, EN:	IC Enable pin. When EN is taken high, both channels are enabled by means of a Soft-start power-up sequence (see Pin 4). When EN is brought low, 'Power Not Good' is signaled within 100ns. The Soft-start capacitor is then discharged by an internal 1.8kΩ resistor (R_{SS_DCHG}, see ELECTRICAL CHARACTERISTICS table) to ground.
Pin 9, PGOOD:	Power Good output pin. An open-Drain logic output that is pulled high with an external pull-up resistor, indicating that both output voltages are within a pre-defined 'Power Good' window, V_{IN} and V_{DD} are within required operating range, and enable is high. Outside this window, this pin is internally pulled low ('Power Not Good' signaled) provided the output error lasts for more than 7µs. The pin also goes low within 100ns of the Enable pin being taken low, or V_{DD} going below UVLO, or V_{IN} going below UVLO irrespective of the output voltage level. Regulation on both channels must be achieved first before fault monitoring becomes active (i.e. PGOOD must have been high prior to occurrence of the fault condition for a fault to be asserted). For correct signaling on this pin under single-channel operation, see description of Pin 2.
Pin 10, FPWM:	Logic input for selecting either the Forced PWM ('FPWM') Mode or Pulse-skip Mode ('SKIP') for both channels (together). When the pin is driven high, the IC operates in the FPWM mode, and when pulled low or left floating, the SKIP mode is enabled. In FPWM mode, the lower FET of a given channel is always ON whenever the upper FET is OFF (except for a narrow shoot-through protection deadband). This leads to continuous conduction mode of operation, which has a fixed frequency and (almost) fixed duty cycle down to very light loads. But this does reduce efficiency at light loads. The alternative is the SKIP mode, where the lower FET remains ON only till the voltage on the Switch pin (see Pin 27 or Pin 16) goes above -2.2mV (typical). So for example, for a 21mΩ FET, this translates to a current threshold of 2.2/21 = 0.1A. Therefore if the (instantaneous) inductor current falls below this value, the lower FET will turn OFF every cycle at this point (when operated in SKIP mode). This threshold is set by the 'Zero-cross Comparator' in the Block Diagram. Note that if the inductor current waveform is high enough to cause the SW pin to be always below this 'zero-cross threshold' (see ELECTRICAL CHARACTERISTICS table), there will be no observable difference between FPWM and SKIP mode settings (in steady-state). SKIP mode, when it occurs, is clearly a discontinuous mode of operation. However, in conventional discontinuous mode, the duty cycle keeps falling (towards zero) as the load decreases. But the LM2657 does not 'allow' the duty cycle to fall by more than 15% of its original value (at the CCM-DCM boundary). This leads to pulse-skipping, and so the average frequency decreases as the load decreases. This mode of operation improves efficiency at light loads, but the frequency is effectively no longer a constant. Note that a minimum preload of 0.1mA should be maintained on the output of each channel to ensure regulation in SKIP mode. The resistive divider from output to ground used to set the output voltage could be designed to serve as this preload.
Pin 11, SS2:	Soft-start pin for Channel 2. See Pin 4.
Pin 12, COMP2:	Compensation pin for Channel 2. See Pin 3.
Pin 13, FB2:	Feedback pin for Channel 2. See Pin 2.

PIN DESCRIPTION (continued)

Pin 14, SENSE2:	Output voltage sense pin for Channel 2. See Pin 1.
Pin 15, ILIM2:	Channel 2 Current Limit pin. When the bottom FET is ON, a 62µA (typical) current flows out of this pin into an external current limit setting resistor connected to the drain of the lower FET. This is a current source so the drop across this resistor tries to push the voltage on this pin to a more positive value. However, the drain of the lower FET, which is connected to the other side of the same resistor, is trying to go more negative as the load current increases. Therefore at some value of current, the voltage on this pin will cross zero and start to go negative. This is the current limiting condition and it is detected by the 'Current Limit Comparator' seen in the BLOCK DIAGRAM. When a current limit condition has been detected, the next ON-pulse of the upper FET will be omitted. The lower FET will again be monitored to determine if the current has fallen below the threshold. If it has, the next ON-pulse will be permitted. If not, the upper FET will stay OFF, and remain so for several cycles if necessary, until the current returns to normal. Eventually, if the overcurrent condition persists and the upper FET has not been turned ON, the output will start to fall eventually triggering "Power not Good".
Pin 16, SW2:	The Switching node of the buck regulator of Channel 2. Also serves as the lower rail of the floating driver of the upper FET.
Pin 17, HDRV2:	Gate drive pin for the upper FET of Channel 2 (High-side drive). The top gate driver is interlocked with the bottom gate driver to prevent shoot-through/cross-conduction.
Pin 18, BOOT2:	Bootstrap pin for Channel 2. This is the upper supply rail for the floating driver of the upper FET. It is bootstrapped by means of a ceramic capacitor connected to the channel Switching node. This capacitor is charged up by the IC to a value of about 5V as derived from the V5 pin (Pin 21).
Pin 19, PGND2:	Power Ground pin of Channel 2. This is the return path for the bottom FET gate drive. Both the PGND's are to be connected on the PCB to the system ground and also to the Signal ground (Pin 7) in accordance with the recommended Layout Guidelines .
Pin 20, LDRV2:	Gate drive pin for the Channel 2 bottom FET (Low-side drive). The bottom gate driver is interlocked with the top gate driver to prevent shoot-through/cross-conduction.
Pin 21, V5:	Upper rail of the lower FET drivers of both channels. Also used to charge up the bootstrap capacitors of the upper FET drivers. This is connected to an external 5V supply. The 5V rail may be the same as the rail used to provide power to the VDD pin (Pin 5). If these rails are connected, the VDD pin must be well-decoupled so that it does not interact with the V5 pin. A minimum 0.1µF (ceramic) capacitor should be placed on the component side very close to the IC with no intervening vias between this capacitor and the V5/PGND pins.
Pin 22, VIN:	The input that powers both the buck regulator channels. It also is used by the internal ramp generator to implement the line 'feedforward' feature. The VIN pin is also used with the SENSE pin voltage to predict the CCM (continuous conduction mode) duty cycle and to thereby set the minimum allowed DCM duty cycle to 85% of the CCM value (in SKIP mode, see Pin 10). This is a high input impedance pin, drawing only about 115µA from the input rail. A fault condition will occur if this voltage drops below its UVLO threshold.
Pin 23, LDRV1:	LDRV pin of Channel 1. See Pin 20.
Pin 24, PGND1:	PGND pin for Channel 1.See Pin 19.
Pin 25, BOOT1:	Boot pin of Channel 1. See Pin 18.
Pin 26, HDRV1:	HDRV pin of Channel 1. See Pin 17.
Pin 27, SW1:	SW pin of Channel 1. See Pin 16.
Pin 28, ILIM1:	Channel 1 Current Limit pin. See Pin 15.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS[1][2]

Voltages from the indicated pins to GND unless otherwise indicated[3]:		
VIN		-0.3V to 30V
V5		-0.3V to 7V
VDD		-0.3V to 7V
BOOT1, BOOT2		-0.3V to 36V
BOOT1 to SW1, BOOT2 to SW2		-0.3V to 7V
SW1, SW2		-0.3V to 30V
ILIM1, ILIM2		-0.3V to 30V
SENSE1, SENSE2, FB1, FB2		-0.3V to 7V
PGOOD		-0.3V to 7V
EN		-0.3V to 7V
Junction Temperature		+150°C
ESD Rating[4]		2kV
Ambient Storage Temperature Range		-65°C to +150°C
Soldering Dwell Time, Temperature	Wave	4 sec, 260°C
	Infrared	10 sec, 240°C
	Vapor Phase	75 sec, 219°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. For specified performance limits and associated test conditions, see the Electrical Characteristics table.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/ Distributors for availability and specifications.
(3) PGND1, PGND2 and SGND are all electrically connected together on the PCB.
(4) ESD is applied by the human body model, which is a 100pF capacitor discharged through a 1.5 kΩ resistor into each pin.

OPERATING RATINGS[1]

VIN	4.5V to 28V
VDD, V5	4.5V to 5.5V
Junction Temperature	-40°C to +125°C

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is specified. For specified performance limits and associated test conditions, see the Electrical Characteristics table.

ELECTRICAL CHARACTERISTICS

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** apply over full **Operating Junction Temperature** range. VDD = V5 = 5V, V_{SGND} = V_{PGND} = 0V, VIN = 15V, V_{EN} = 3V, R_{FADJ} = 22.1kΩ unless otherwise stated[1]. Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typical[2]	Max	Units
Reference						
V_{FB}	FB Pin Voltage at Regualtion (either FB Pin)	VDD = 4.5V to 5.5V, VIN = 4.5V to 28V	**591**	600	**609**	mV
$V_{FB\_LINE\ REG}$	V_{FB} Line Regulation (ΔV_{FB})	VDD = 4.5V to 5.5V, VIN = 4.5V to 28V		0.5		
I_{FB}	FB Pin Current (sourcing)	V_{FB} at regulation		20	**100**	nA
Chip Supply						
I_{Q_VIN}	VIN Quiescent Current	V_{FB1} = V_{FB2} = 0.7V		100	**200**	µA
I_{SD_VIN}	VIN Shutdown Current	V_{EN} = 0V		0	**5**	µA
I_{Q_VDD}	VDD Quiescent Current	V_{FB1} = V_{FB2} = 0.7V		2.5	**4**	mA
I_{SD_VDD}	VDD Shutdown Current	V_{EN} = 0V		6	**15**	µA
I_{Q_V5}	V5 Normal Operating Current	V_{FB1} = V_{FB2} = 0.7V		0.3	**0.5**	mA
		V_{FB1} = V_{FB2} = 0.5V		1	**1.5**	

(1) R_{FADJ} is the frequency adjust resistor between FREQ pin and SGND pin.
(2) Typical numbers are at 25°C and represent the most likely norm.

ELECTRICAL CHARACTERISTICS (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** apply over full **Operating Junction Temperature** range. VDD = V5 = 5V, V_{SGND} = V_{PGND} = 0V, VIN = 15V, V_{EN} = 3V, R_{FADJ} = 22.1kΩ unless otherwise stated(1). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typical(2)	Max	Units
I_{SD_V5}	V5 Shutdown Current	V_{EN} = 0V		0	**5**	µA
I_{Q_BOOT}	BOOT Quiescent Current	V_{FB1} = V_{FB2} = 0.7V		2	**5**	µA
		V_{FB1} = V_{FB2} = 0.5V		300	**500**	
I_{SD_BOOT}	BOOT Shutdown Current	V_{EN} = 0V		1	**5**	µA
V_{DD_UVLO}	VDD UVLO Threshold	VDD rising up to V_{UVLO}	**3.9**	4.2	**4.5**	V
	VDD UVLO Hysteresis	VDD = V5 falling from V_{UVLO}	**0.5**	0.7	**0.9**	V
V_{IN_UVLO}	VIN UVLO Threshold	VIN rising up to V_{UVLO}	**3.9**	4.2	**4.5**	V
	VIN UVLO Hysteresis	VIN falling from V_{UVLO}		0.1	**0.3**	V
Logic						
I_{EN}	EN Input Current	V_{EN} = 0 to 5V		0		µA
V_{EN_HI}	Minimum EN Input Logic High		**2**			V
V_{EN_LO}	Maximum EN Input Logic Low				**0.8**	V
R_{FPWM}	FPWM Pull-down	V_{FPWM} = 2V	**100**	200	**1000**	kΩ
V_{FPWM_HI}	Minimum FPWM Input Logic High		**2**			V
V_{FPWM_LO}	Maximum FPWM Input Logic Low				**0.8**	V
Power Good and OVP						
V_{PGOOD_HI}	Power Good Upper Threshold as a Percentage of Internal Reference	FB voltage rising above V_{FB}	**110**	113	**116**	%
V_{PGOOD_LOW}	Power Good Lower Threshold as a Percentage of Internal Reference	FB voltage falling below V_{FB}	**84**	87	**90**	%
HYS_{PGOOD}	Power Good Hysteresis			7		%
Δt_{PG_OK}	Power Good Delay	From both output voltages “good” to PGOOD assertion.	**10**	20	**30**	µs
Δt_{PG_NOK}		From the first output voltage “bad” to PGOOD de-assertion	**4**	7	**10**	
Δt_{SD}		From Enable low to PGOOD low		0.03	**0.1**	
V_{PGOOD_SAT}	PGOOD Saturation Voltage	PGOOD de-asserted (Power Not Good) and sinking 1.5mA		0.12	**0.4**	V
I_{PGOOD_LEAK}	PGOOD Leakage Current	PGOOD = 5V and asserted		0	**1**	µA
Soft-start						
I_{SS_CHG}	Soft-start Charging Current	V_{SS} = 1V	**8**	11	**14**	µA
R_{SS_DCHG}	Soft-shutdown Resistance (SS pin to SGND, either channel)	V_{EN} = 0V, V_{SS} = 1V		1800		Ω
I_{SS_DCHG}	Soft-start Discharge Current	In Current Limit	**80**	115	**160**	µA
V_{SS_RESET}	Soft-start pin reset voltage(3)	SS charged to 0.5V, EN low to high		100		mV
V_{OS}	SS to COMP Offset Voltage	V_{SS} = 0.5V and 1V, V_{FB1} = V_{FB2} = 0V		600		mV

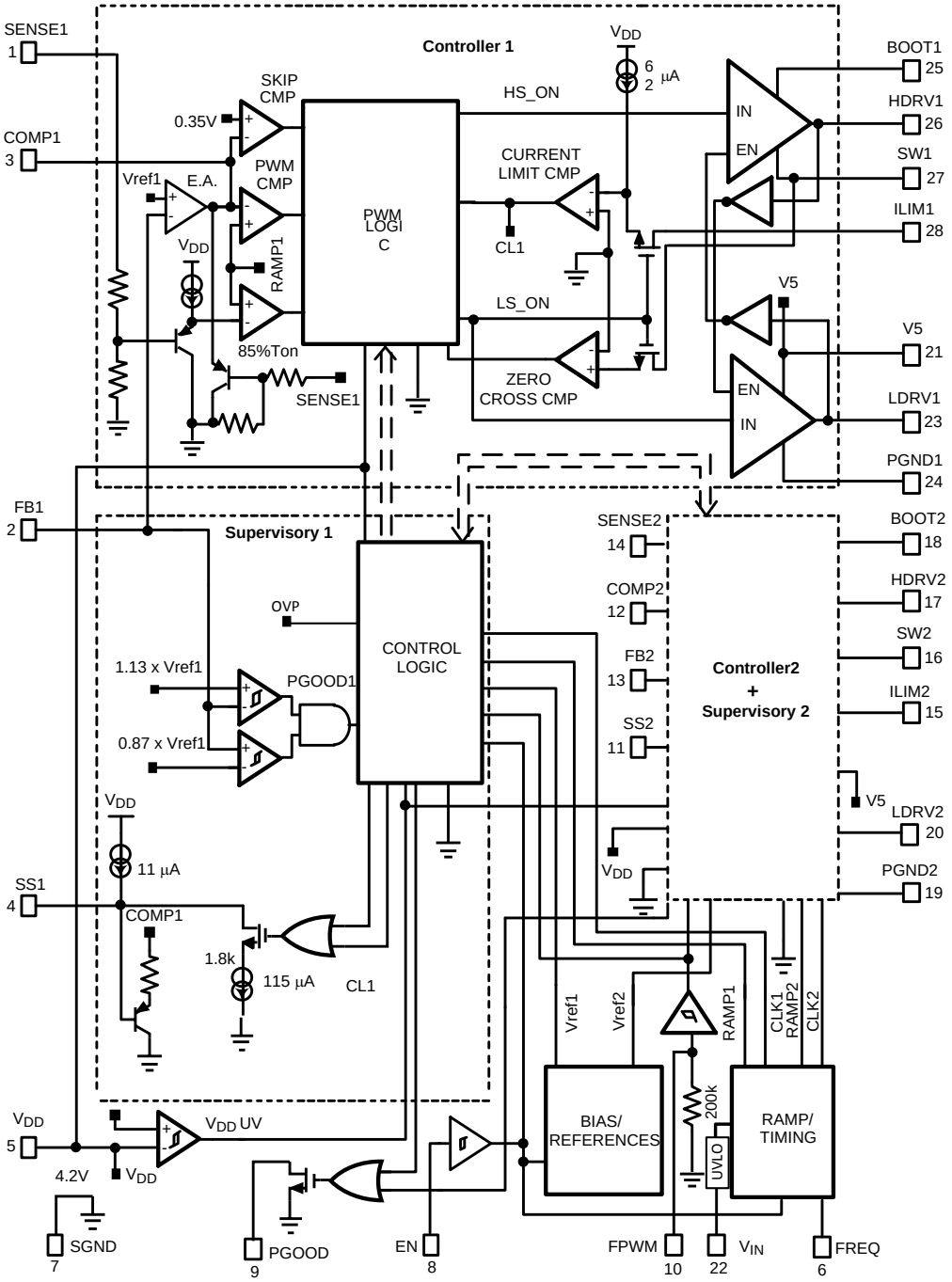
(3) If the LM2657 starts up with a pre-charged soft start capacitor, it will first discharge the capacitor to V_{SS_RESET} and then begin the normal Soft-start process.

ELECTRICAL CHARACTERISTICS (continued)

Specifications with standard typeface are for T_J = 25°C, and those with **boldface** apply over full **Operating Junction Temperature** range. VDD = V5 = 5V, V_{SGND} = V_{PGND} = 0V, VIN = 15V, V_{EN} = 3V, R_{FADJ} = 22.1kΩ unless otherwise stated(1). Datasheet min/max specification limits are specified by design, test, or statistical analysis.

Symbol	Parameter	Conditions	Min	Typical(2)	Max	Units
Error Amplifier						
GAIN	DC Gain			70		dB
V_{SLEW}	Voltage Slew Rate	COMP rising		4.45		V/µs
		COMP falling		2.25		
BW	Unity Gain Bandwidth			6.5		MHz
I_{COMP_SOURCE}	COMP Source Current	V_{FB} = lower COMP = 0.5V	**2**	5		mA
I_{COMP_SINK}	COMP Sink Current	V_{FB} = higher than internal reference COMP = 5V	**7**	14		mA
Current Limit and Zero-Cross						
I_{ILIM}	ILIM Pin Current (sourcing, either ILIM pin)	V_{ILIM1} = V_{ILIM2} = 0V	**46**	62	**76**	µA
V_{ILIM_TH}	ILIM Threshold Voltage		**-10**	0	**10**	mV
V_{SW_ZERO}	Zero-cross Threshold (SW Pin)	LDRV goes low		-2.2		mV
Oscillator						
F_{OSC}	PWM Frequency	R_{FADJ} = 22.1kΩ	**255**	300	**345**	kHz
		R_{FADJ} = 12.4kΩ		500		
		R_{FADJ} = 30.9kΩ		200		
V_{RAMP}	PWM Ramp Peak-to-peak Amplitude	VIN = 4.5V		0.48		V
		VIN = 15V		1.6		
		VIN = 28V		3.0		
V_{VALLEY}	PWM Ramp Valley			0.8		V
Δ_{FOSC_VIN}	Frequency Change with VIN	VIN = 4.5V to 28V		±1		%
Δ_{FOSC_VDD}	Frequency Change with VDD	VDD = 4.5V to 5.5V		±2		%
$ø_{CH}$	Phase Shift Between Channels	Phase from HDRV1 to HDRV2	**165**	180	**195**	deg
V_{FREQ_VIN}	FREQ Pin Voltage vs. VIN			0.107		V/V
System						
$t_{on\text{-}min}$	Minimum ON Time	V_{FPWM} = 3V		30		ns
D_{MAX}	Maximum Duty Cycle	VIN = 4.5V	**60**	70		%
		VIN = 15V	**40**	50		%
		VIN = 28V, VDD= 4.5V	**24**	30		%
Gate Drivers						
R_{HDRV_SOURCE}	HDRV Source Impedance	HDRV Pin Current (sourcing)= 1.2A		7		Ω
R_{HDRV_SINK}	HDRV Sink Impedance	HDRV Pin Current (sinking) = 1A		2		Ω
R_{LDRV_SOURCE}	LDRV Source Impedance	LDRV Pin Current (sourcing) = 1.2A		7		Ω
R_{LDRV_SINK}	LDRV Sink Impedance	LDRV Pin Current (sinking) = 2A		1		Ω
t_{DEAD}	Cross-conduction Protection Delay (deadtime)	HDRV Falling to LDRV Rising		40		ns
		LDRV Falling to HDRV Rising		70		

BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

The system efficiency plots below were measured using input voltages of 15V, 20V, 24V, 28V. These input voltages correspond with the uppermost curve to lowermost curve, respectively. The output current (I_O) refers to simultaneous loading of both channels.

System Efficiency for 5V/3.3V Outputs

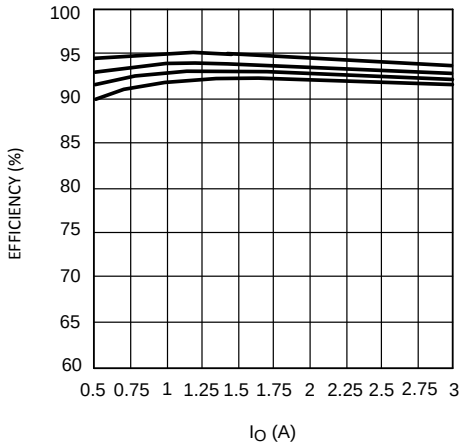


Figure 2.

System Efficiency for 2.5V/3.3V Outputs

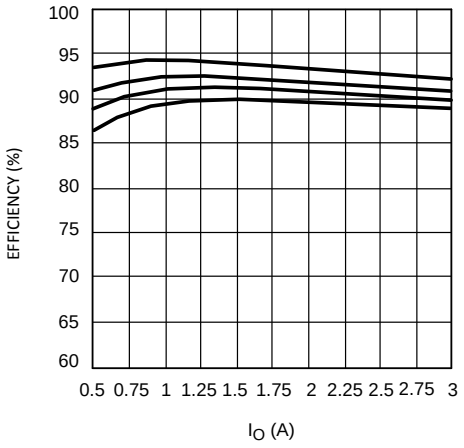


Figure 3.

System Efficiency for 1.8V/1.2V Outputs

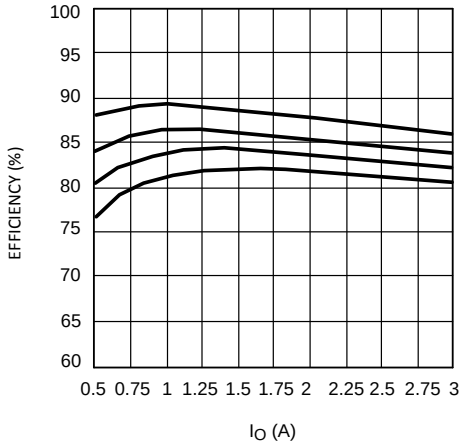


Figure 4.

System Max V_{OUT} For A Given V_{IN}
T_J = 25°C

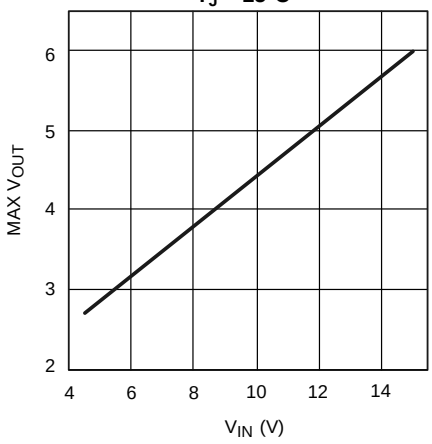


Figure 5.

Modulator (Plant) Gain

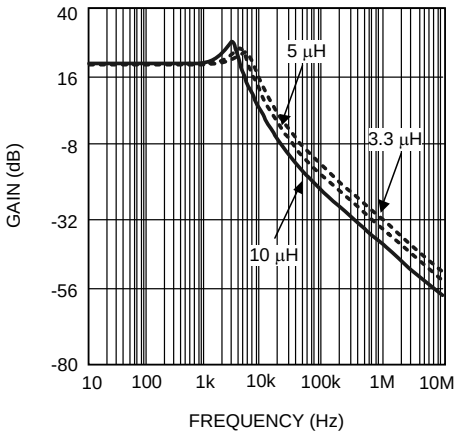


Figure 6.

OPERATION DESCRIPTIONS

GENERAL

The LM2657 provides two identical synchronously switched buck regulator channels that operate 180° out of phase. A voltage-mode control topology was selected to provide fixed-frequency PWM regulation at very low duty cycles, in preference to current-mode control, because the latter has inherent limitations in being able to achieve low pulse widths due to blanking time requirements. Because of a minimum pulse width of about 30ns for the LM2657, very low duty cycles (low output, high input) are possible. The main advantage of current-mode control is the fact that the slope of its ramp (derived from the switch current), automatically increases with an increase in input voltage. This leads to improved line rejection and fast response to line variations. In typical voltage-mode control, the ramp is derived from the clock, not from the switch current. But by using the input voltage together with the clock signal to generate the ramp as in the LM2657, this advantage of current-mode control can in fact be completely replicated. The technique is called line feedforward. In addition, the LM2657 features a user-selectable Pulse-skip mode that significantly improves efficiency at light loads by reducing switching losses and driver consumption, both of which are proportional to switching frequency.

INPUT VOLTAGE FEEDFORWARD

The feedforward circuit of the LM2657 adjusts the slope of the internal PWM ramp in proportion to the regulator input voltage. See Figure 7 for an illustration of how the duty cycle changes as a result of the change in the slope of the ramp, even though the error amplifier output has not had time to react to the line disturbance. The almost instantaneous duty cycle correction provided by the feedforward circuit significantly improves line transient rejection.

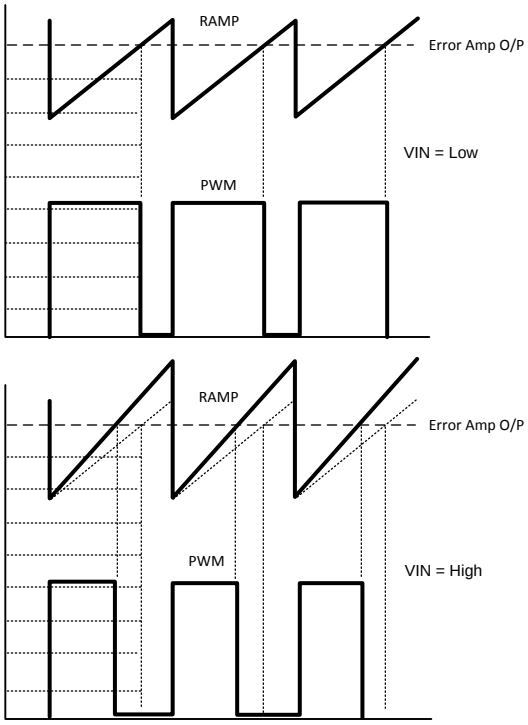
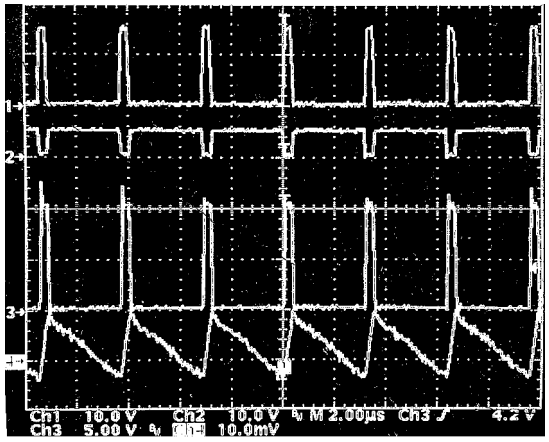


Figure 7. Voltage Feedforward

FORCED-PWM MODE AND PULSE-SKIP MODE

Forced-PWM mode (FPWM) leads to Continuous Conduction Mode (CCM) even at very light loads. It is one of two user-selectable modes of operation provided by the LM2657. When FPWM is chosen (FPWM pin high), the bottom FET will always be turned ON whenever the top FET is OFF. See Figure 8 for a typical FPWM plot.



CH1: HDRV, CH2: LDRV, CH3: SW, CH4: I_L (0.2A/div)
Output 1V @ 0.04A, VIN = 10V, FPWM, L = 10µH, f = 300kHz

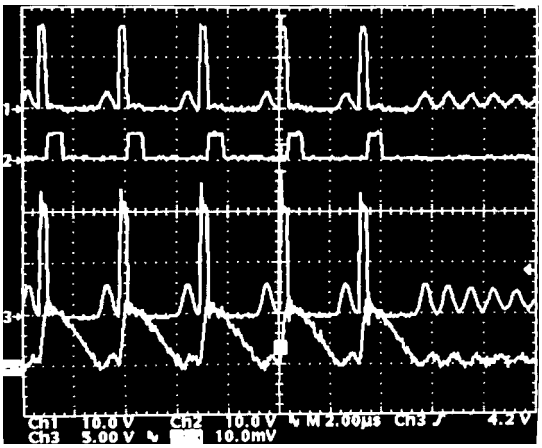
Figure 8. Normal FPWM Mode Operation at Light Loads

In a conventional converter, as the load is decreased to about 10-30% of maximum load current, DCM (Discontinuous Conduction Mode) occurs. In this condition the inductor current falls to zero during the OFF-time, and stays there until the start of the next switching cycle. In this mode, if the load is decreased further, the duty cycle decreases (pinches off), and ultimately may decrease to the point where the required pulse width becomes less than the minimum ON-time achievable by the converter (controller + FETs). Then a sort of random skipping behavior occurs as the error amplifier struggles to maintain regulation. There are two ways to prevent random pulse skipping from occuring.

One way is to keep the lower FET ON until the start of the next cycle (as in the LM2657 operated in FPWM mode). This allows the inductor current to drop to zero and then actually reverse direction (negative direction through inductor, passing from drain to source of lower FET, see Channel 4 in Figure 8). Now the current can continue to flow continuously until the end of the switching cycle. This maintains CCM and the duty cycle does not start to pinch off as in typical DCM. Nor does it lead to the undesirable random skipping described above. Note that the pulse width (duty cycle) for CCM is virtually constant for any load and therefore does not usually run into the minimum ON-time restriction. But it can happen, especially when the application consists of a very high input voltage, a low output voltage rail, and the switching frequency is set high. Let us check the LM2657 to rule out this remote possibility. For example, with an input of 24V, an output of 1V, the duty cycle is 1/24 = 4.2%. This leads to a required ON-time of 0.042* 3.3µs = 0.14 µs at a switching frequency of 300kHz (T=3.3 µs). Since 140ns exceeds the minimum ON-time of 30ns of the LM2657, normal constant frequency CCM mode of operation is assured in FPWM mode at virtually any load.

The second way to prevent random pulse skipping in discontinuous mode is the Pulse-skip (SKIP) Mode. In SKIP Mode, a zero-cross detector at the SW pin turns off the bottom FET when the inductor current decays to zero (actually at V_{SW_ZERO}, see ELECTRICAL CHARACTERISTICS table). This, however, would still amount to conventional DCM, with its attendant idiosyncrasies at extremely light loads as described earlier. The LM2657 avoids the random skipping behavior and replaces it with a more consistent SKIP mode. In conventional DCM, a converter would try to reduce its duty cycle from the CCM value as the load decreases, as explained previously. So it would start with the CCM duty cycle value (at the CCM-DCM boundary), but as the load decreases, the duty cycle would try to shrink to zero. However, in the LM2657, the DCM duty cycle is not allowed to fall below 85% of the CCM value. So when the theoretically required DCM duty cycle value falls below what the LM2657 is allowed to deliver (in this mode), pulse-skipping starts. It will be seen that several of these excess pulses may be delivered until the output capacitors charge up enough to notify the error amplifier and cause its output to reverse. Thereafter, several pulses could be skipped entirely until the output of the error amplifier again reverses. The SKIP mode therefore leads to a reduction in the average switching frequency. Switching losses and FET driver losses, both of which are proportional to frequency, are significantly reduced at very light loads and efficiency is boosted. SKIP mode also reduces the circulating currents and energy associated with the FPWM

mode. See Figure 9 for a typical plot of SKIP mode at very light loads. Note the bunching of several fixed-width pulses followed by skipped pulses. The average frequency can actually fall very low at very light loads. When this happens the inductor core is seeing only very mild flux excursions, and no significant audible noise is created. But if EMI is a particularly sensitive issue for the particular application, the user can simply opt for the slightly less efficient, constant frequency FPWM mode.



CH1: HDRV, CH2: LDRV, CH3: SW, CH4: I_L (0.2A/div)
Output 1V @ 0.04A, VIN = 10V, SKIP, L = 10µH, f = 300kHz

Figure 9. Normal SKIP Mode Operation at Light Loads

The SKIP mode is enabled when the FPWM pin is held low (or left floating). At higher loads, and under steady state conditions (above CCM-DCM boundary), there will be absolutely no difference in the behavior of the LM2657 or the associated converter waveforms based on the voltage applied on the FPWM pin. The differences show up only at light loads.

Also, under startup, since the currents are high until the output capacitors have charged up, there will be no observable difference in the shape of the ramp-up of the output rails in either SKIP mode or FPWM mode. The design has thus forced the startup waveforms to be identical irrespective of whether the FPWM mode or the SKIP mode has been selected.

The designer must realize that even at zero load condition, there is circulating current when operating in FPWM mode. This is illustrated in Figure 10. Since duty cycle is the same as for conventional CCM, from $V = L^* \Delta I / \Delta t$ it can be seen that ΔI (or Ipp in Figure 10) must remain constant for any load, including zero. At zero load, the average current through the inductor is zero, so the geometric center of the sawtooth waveform (the center being always equal to load current) is along the x-axis. At critical conduction (boundary between conventional CCM and what should have been DCM were it not in FPWM mode), the load current is equal to Ipp/2. Note that excessively low values of inductance will produce much higher current ripple and this will lead to higher circulating currents and dissipation.

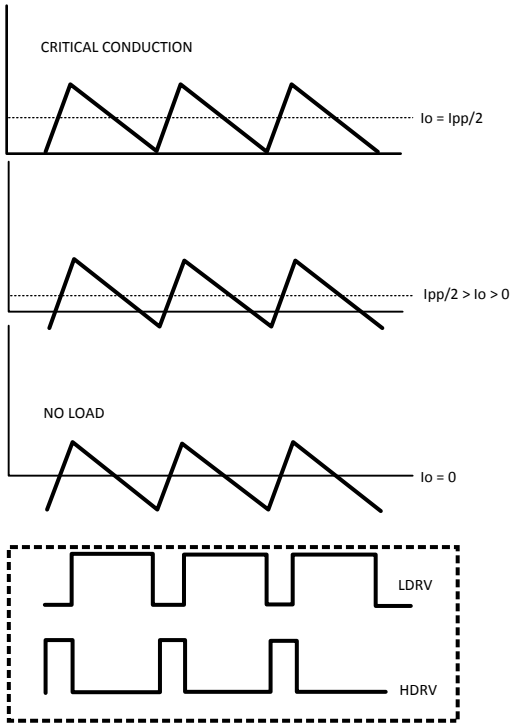
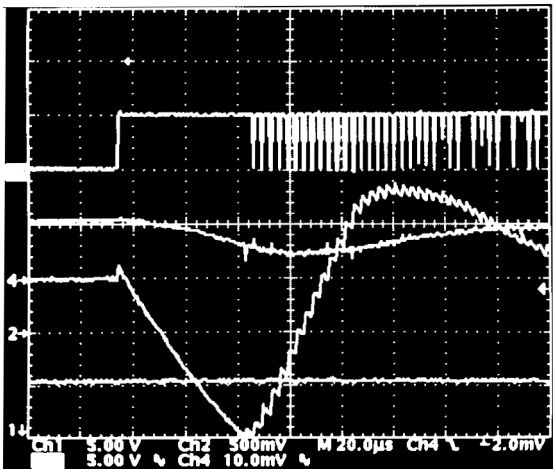


Figure 10. Inductor Current in FPWM Mode

START-UP AND STATE-TRANSITIONS AT LIGHT LOADS

During startup the LM2657 is allowed to operate in SKIP mode regardless of the voltage on the FPWM pin. Starting in SKIP mode prevents the low-side FET from having to sink excessive amounts of negative current during start-up. This would occur if the output was pre-biased and the converter operated in FPWM mode. The FB pin would sense that the output was high and force a very low duty cycle, which would keep the low-side FET on longer than it should be in steady state. Without a load on the output the inductor current will reverse and become negative. This negative inductor current can be quite large depending on the voltage on the output and the size of the output capacitor.

A similar situation can occur if the converter transitions from SKIP mode to FPWM mode under a light load condition (converter is operating below the DCM boundary). This can occur after startup if FPWM mode is selected for use in a light load condition or if the FPWM pin is toggled high during normal operation at light load. The problem occurs because in SKIP mode the converter is operating at a set duty cycle and a lower average frequency. When the converter is forced into FPWM mode, this represents a change to the system. The pulse widths and frequency need to readjust suddenly and in the process momentary imbalances can be created. Like the case of a pre-biased load, there can be negative surge current passing from drain to source of the lower FET. It must be kept in mind *that though the LM2657 has current limiting for current passing in the 'positive' direction (positive with regards to the inductor, i.e. passing from source to drain of the lower FET), there is no limit for reverse currents*. The amount of reverse current when the FPWM pin is toggled 'on the fly' can be very high. This current is determined by several factors. One key factor is the output capacitance. Large output capacitances will lead to higher peak reverse currents. The reverse swing will be higher for lighter loads because of the bigger difference between the duty cycles/average frequency in the two modes. See Figure 11 for a plot of what happened in going from SKIP to FPWM mode at 0A load (worst case). The peak reverse current was as high as 3A, lasting about 0.1ms. The inductor could also saturate severely at this point if designed for light loads. In general, if the designer wants to toggle the FPWM pin while the converter is operating or if FPWM mode is required for a light load application, the low side FET and inductor should be closely evaluated under this specific condition.



CH1: PGOOD, CH2: Vo, CH3: LDRV, CH4: I_L (1A/div)
Output 1V @ 0A, VIN = 10V, L = 10µH, f = 300kHz

Figure 11. SKIP to FPWM 'On The Fly'

If the part is operated in FPWM mode with a light load the user will experience lower efficiency and negative current during the transition (as discussed). The user may also experience a momentary drop on Vout when the transition is made from SKIP to FPWM mode. This only occurs for no load or very light load conditions (above the DCM boundary there is no difference between SKIP FPWM modes).

In some cases, such as low Vout (<1.5V), a glitch may be present on PGOOD. If this is problematic, the glitch may be eliminated by either operating in SKIP mode or using a small sized soft start capacitor. See the following section for selecting soft start capacitors.

SOFT-START

The maximum output voltage of the error amplifier is limited during start-up by the voltage on the 0.1µF capacitor connected between the SS pin and ground. When the controller is enabled (by taking EN pin high), the following steps may occur. First, the SS capacitor is discharged (if it has a pre-charge) by a 1.8 kΩ internal resistor (R_{SS_DCHG}, see ELECTRICAL CHARACTERISTICS). This ensures that reset is obtained. Note that reset is said to occur only when the voltage on *both* the SS pins falls below 100mV (V_{SS_RESET}, see ELECTRICAL CHARACTERISTICS table). Then a charging current source I_{SS_CHG} of 11µA is applied at this pin to bring up the voltage of the Soft-start capacitor gradually. This causes the (maximum allowable) duty cycle to increase slowly, thereby limiting the charging current into the output capacitor and also ensuring that the inductor does not saturate. The Soft-start capacitor will eventually charge up close to the 5V input rail. When EN is pulled low the Soft-start capacitor is discharged by the same 1.8 kΩ internal resistor and the controller is shutdown. Now the sequence is allowed to repeat the next time EN is taken high.

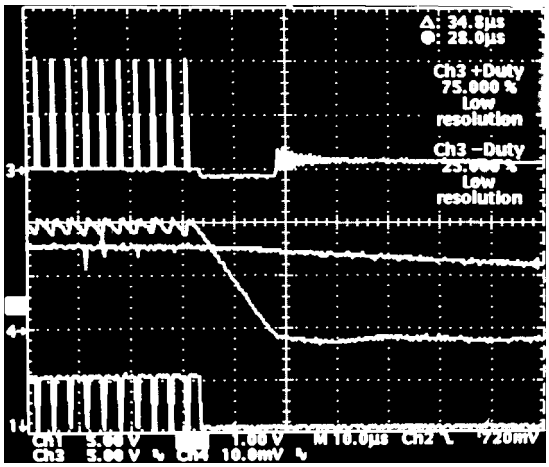
One must be careful in selecting a soft start capacitor. Selecting a value that is too small will cause the switcher to go into current limit during startup. The minimum startup time may be estimated by the capacitor charging equation:

$$\Delta t_{STARTUP} = C_{OUT} \frac{\Delta V_{OUT}}{I_{CurrentLimit}} \quad (1)$$

SHUTDOWN

When the EN pin is driven low, the LM2657 initiates shutdown by turning OFF both upper and lower FETs completely (this occurs irrespective of FPWM or SKIP modes). See Figure 12 for a typical shutdown plot and note that the LDRV goes to zero (and stays there). Though not displayed, Power Good also goes low within less than 100ns of the EN pin going low (Δt_{SD}, see ELECTRICAL CHARACTERISTICS table). Therefore in this case, the controller is NOT waiting for the output to actually fall out of the Power Good window before it signals Power Not Good.

When the part is shutdown with a constant current load, the time taken for the output to decay may be calculated using the equation ΔV/Δt = i/C. For example, there is a constant current 2A load applied at the output and the charge stored on the output capacitor continues to discharge into the load. From ΔV/Δt = i/C = 2A/330µF, it can be seen that the output voltage (say 1V) will fall to zero in about 165µs.



CH1: LDRV, CH2: Vo, CH3: SW, CH4: I_L (1A/div)
Output 1V @ 2A, VIN = 10V, FPWM/SKIP, L = 10µH, f = 300kHz, C_{OUT} = 330µF

Figure 12. Shutdown

POWER GOOD/NOT GOOD SIGNALING

PGOOD is an open-drain output pin with an external pull-up resistor connected to 5V. It goes high (non-conducting) when both the outputs are within the regulation band as determined by the Power Good window detector stage on the feedback pin (see BLOCK DIAGRAM). PGOOD goes low (conducting) when either of the two outputs falls out of this window. This signal is referred to as Power Not Good. A glitch filter of 7µs filters out noise, and helps prevent spurious PGOOD responses. So Power Not Good is not asserted until 7µs after either of the two outputs have fallen out of the Power Good window (see Δt_{PG_NOK} in ELECTRICAL CHARACTERISTICS table). During power-up/Enable/recovery from a fault, the feedback pin voltage rises towards the regulation value. With the feedback pin rising, there is a 20µs delay between both the outputs being in regulation and the signaling of Power Good (see Δt_{PG_OK} in ELECTRICAL CHARACTERISTICS table).

Power Not Good is signaled within 100ns of the Enable pin being pulled low (see Δt_{SD} in ELECTRICAL CHARACTERISTICS table), irrespective of the fact that the outputs could still be in regulation. The Soft-start capacitor is also then discharged as explained earlier.

VIN POWER-OFF (UVLO)

The LM2657 has an internal comparator that monitors Vin. If Vin falls to approximately 4.2V, switching ceases and both top and bottom FETs are turned OFF. 'Power Not Good' has meanwhile already been signaled and a fault condition asserted shortly thereafter.

VDD POWER-OFF (UVLO)

If VDD falls below approximately 4V, switching ceases and both top and bottom FETs are turned OFF. If VDD falls below about 1.8V, the part is disabled identically to EN being pulled low and the soft-start sequence is reset.

OVER-VOLTAGE PROTECTION

In addition to a Power Not Good fault being asserted, if the FB pin is above the PGOOD window, an over-voltage fault occurs. The low-side FET is turned ON and the high-side FET is turned OFF immediately. Normal operation will resume upon the next switching cycle where an over-voltage fault is not detected. If the fault persists, the low-side FET will stay on and the high-side FET will not turn back on until the FB pin falls within the power good window.

CURRENT LIMIT AND PROTECTION

Output current limiting is achieved by sensing the negative Vds drop across the low side FET when the FET is turned ON. The Current Limit Comparator (see BLOCK DIAGRAM) monitors the voltage at the ILIM pin with 62µA (typical value) of current being sourced from the pin. The 62µA source flows through an external resistor connected between ILIM and the drain of the lower FET. The voltage drop across the ILIM resistor is compared with the drop across the lower FET and the current limit comparator trips when the two are of the same magnitude. This determines the threshold of current limiting. For example, if excessive inductor current causes the voltage across the lower FET to exceed the voltage drop across the ILIM resistor, the ILIM pin will go negative (with respect to ground) and trip the comparator. The comparator then sets a latch that prevents the top FET from turning ON during the next PWM clock cycle. The top FET will resume switching only if the current limit comparator was not tripped in the previous switching cycle. This operates identically to an over-voltage fault.

Additionally, the Soft-start capacitor at the SS pin is discharged with a 115µA current source when an overcurrent event is in progress. The purpose of discharging the Soft-start capacitor during an overcurrent event is to eventually allow the voltage on the SS pin to fall low enough to cause additional duty cycle limiting.

Application Information

SETTING OUTPUT VOLTAGE

When setting the output voltage, one should consider the maximum duty cycle constraints. The maximum duty cycle limits the maximum output voltage for a given input voltage (see ELECTRICAL CHARACTERISTICS) according to the formula:

$$V_{OUT\_MAX} = D_{MAX} \times V_{IN} \quad (2)$$

One should also note that resistors R21,R15 are involved in setting the gain of the error amplifier for their respective channels. For the following example the value of R_T has been set to 43.2kΩ for both channels. In general, only the bottom resistor should be adjusted unless the compensation is modified. Open-loop gain information is provided in the next section should it be necessary to change both top and bottom resistor values.

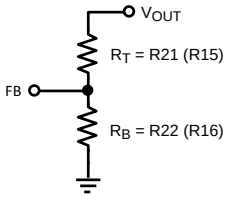


Figure 13. Component Designation

Output Voltage equation:

$$V_{OUT} = \frac{R_T + R_B}{R_B} V_{FB} \quad (3)$$

Rearranging, we can express the value of RB as simply:

$$R_B = \frac{R_T \times V_{FB}}{V_{OUT} - V_{FB}} \quad (4)$$

Therefore from the Bill of Materials (High Current Board, Table 3):

For **Channel #1** (V_{OUT1} = 1.8V),

R_T = R21 = 43.2kΩ

$$R_B = \frac{43.2\ k\Omega \times 0.6V}{1.8V - 0.6V} \quad (5)$$

R_B = 21.6kΩ, however the closest standard value is 21.5kΩ. Therefore

R_B = R22 = 21.5kΩ

For **Channel #2** (V_{OUT2} = 1.2V),

R_T = R15 = 43.2kΩ

$$R_B = \frac{43.2\ k\Omega \times 0.6V}{1.2V - 0.6V} \quad (6)$$

R_B = 43.2kΩ which is a standard value. Therefore

R_B = R16 = 43.2kΩ

Looking again at the output voltage equation:

$$V_{OUT1} = \frac{(43.2 + 21.5) \times 0.6}{21.5} = 1.806V \quad (7)$$

$$V_{OUT2} = \frac{(43.2 + 43.2) \times 0.6}{43.2} = 1.2V \quad (8)$$

OUTPUT FILTER

At this point the designer must consider the load requirements for output voltage ripple (V_{RIPPLE}), voltage droop (V_{DROOP}), and current ripple (I_{RIPPLE}).

The following equation may be used in calculating an appropriate inductor value:

$$L = \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN} I_{RIPPLE} f_{SW}} 10^3 \quad (9)$$

Where

- f_{SW} is in kHz and L is in µH.

From the relationship above it becomes apparent that there is a tradeoff between ripple current and inductor size. A good starting point for selecting an inductor is to set I_{RIPPLE} equal to 30% of the maximum load current.

Once an inductor has been selected, the capacitor value may be determined by considering the maximum load step (difference between maximum and minimum currents drawn by the load) and the acceptable level that the voltage will droop during that load step (typically not more than 2% of the output voltage). This relationship is given by the following:

$$C = \frac{L(I_{MAX} - I_{MIN})^2}{2V_{DROOP}(V_{IN} - V_{OUT})} \quad (10)$$

Where

- L is in µH and C is in µF.

Capacitors have a parasitic series resistance (ESR) that is responsible for voltage ripple in the output. To ensure that the capacitor will meet the given requirements, it must have an ESR not greater than the following:

$$ESR = \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (11)$$

The output capacitor must be able to withstand the load requirements by having a voltage and RMS current rating higher than the output voltage and RMS load current respectively. The RMS load current may be determined using the following relationship:

$$I_{RMS\_OUT} = \frac{I_{RIPPLE}}{\sqrt{12}} \quad (12)$$

Iteration is usually required to ensure the best overall solution for a given application.

Should the designer require a more detailed set of equations, application notes AN-1197 SNVA038 and AN-1207 SNOA406 available from www.ti.com are an excellent resource.

MOSFET SELECTION

Selection of FETs for the controller must be done carefully taking into account efficiency, thermal dissipation and drive requirements. Typically the component selection is made according to the most efficient FET for a given price.

When looking for a FET, it is often helpful to compose a spreadsheet of key parameters. These parameters may be summarized as on resistance (R_{DS_ON}), gate charge (Q_{GS}), rise and fall times (t_r and t_f). The power dissipated in a given device may then be calculated according to the following equations:

High side FET:

$P = P_C + P_{GC} + P_{SW}$

Where

- $P_C = D \times (I_{OUT}^2 \times R_{DS\_ON})$
- $P_{GC} = 5V \times Q_{GS} \times f$
- $P_{SW} = 0.5 \times V_{IN} \times I_{OUT} \times (t_r + t_f) \times f$ (13)

Low side FET:

$P = P_C + P_{GC}$

Where

- $P_C = (1 - D) \times (I_{OUT}^2 \times R_{DS\_ON})$
- $P_{GC} = 5V \times Q_{GS} \times f$ (14)

One will note that the gate charge requirements should be low to ensure good efficiency. However, if a FET's gate charge requirement is too low (less than 8nC), the FET can turn on spuriously. A good starting point for a 10A load is to use a high side and low side FET each with an on resistance of 5mΩ (FET on resistance is a function of temperature, therefore it is advisable to apply the appropriate correction factor provided in the FET datasheet), gate to source charge of 8nC (total gate charge of 36 nC), t_r = 11ns, t_f = 47ns, and temp coefficient of 1.4. For a 5V input and 1.2V/10A output (f = 300kHz), this yields a power dissipation of 0.62 W (high side FET) and 0.54 W (low side FET). The efficiency (Efficiency = P_{OUT}/P_{OUT} + P_Low_Side_FET+P_High_Side_FET + V_{IN} * I_Q)) is then 91%. While the same FET may be used for both the high side and low side, optimal performance may not be realized.

CURRENT LIMIT RESISTOR

The timing scheme implemented in the LM2657 makes it possible for the IC to continue monitoring an overcurrent condition and to respond appropriately every cycle. This is explained as follows:

Consider the LM2657 working under normal conditions, just before an overload occurs. After the end of a given ON-pulse (say 'ton1'), the LM2657 starts sampling the current in the low-side FET. This is the OFF-duration called 'toff1' in this analysis. If an overcurrent condition is detected during this OFF-duration 'toff1' the controller will decide to omit the next ON-pulse (which would have occurred during the duration 'ton2'). This is done by setting an internal 'overcurrent latch' which will keep HDRV low. The LDRV will now not only stay high during the present OFF-duration ('toff1') but during the duration of the next (omitted) ON-pulse ('ton2'), and then as expected also during the succeeding OFF-duration ('toff2'). But the 'overcurrent latch' is reset at the very start of the next OFF-duration 'toff2'. Therefore, if the overcurrent condition persists, it can be recognized during 'toff2' and a decision to skip the next ON-pulse (duration 'ton3') can be taken. Finally, several ON-pulses may get skipped until the current in the lower FET falls below the current limit threshold.

Note that about 150ns after LDRV first goes high (start of low-side conduction), the current monitoring starts. The peak current seen by the current limit detector is slightly lower than the peak inductor current.

To set the value of the current limiting resistor (RLIM, between ILIM pin and SW pin), the function of the ILIM pin must be understood. Refer to Figure 14 to see how the voltage on the ILIM pin changes as current ramps up.

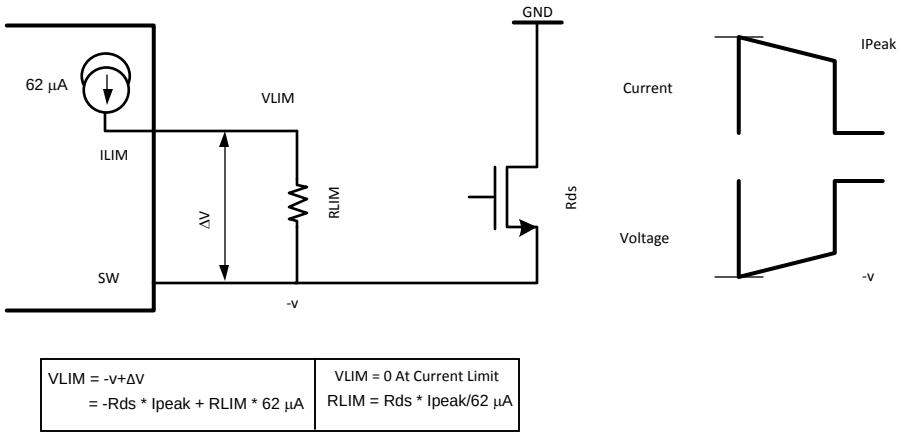


Figure 14. Understanding Current Sensing

For this analysis, the nominal value of current sourced (ILIM, see ELECTRICAL CHARACTERISTICS table) and the R_{DS_ON} of the lower FET at 100°C should be used. This will ensure adequate headroom without the need for excessively large components. For the chosen low-side FET of the high current Evaluation board (Si4442DY), the typical R_{DS_ON} at room temperature is 4.1mΩ, but this is not to be used here. The MAX FET R_{DS_ON} at room temperature is 5mΩ. From the datasheet, at 100°C the R_{DS_ON} goes up typically 1.4 times. Therefore, the R_{DS_ON} to be used in the actual current limit calculation is 1.4*5mΩ = 7mΩ.

Using I_{ILIM} = 62µA (see ELECTRICAL CHARACTERISTICS table) and 7mΩ here will provide the lowest possible value of current limit considering tolerances and temperature (for a given RLIM resistor). This limit must be set higher than the actual peak current in the converter under normal operation to ensure that full rated power can be delivered under all conditions by the converter without reaching the set current limit value.

At the point where current limiting occurs (peak inductor current becomes equal to current limit) the resistor for setting the current limit can be calculated. The (peak) current limit value depends on two factors:

a) The peak current in the inductor with the converter delivering maximum rated load. This should be calculated at Vinmax.

b) The 'overload margin' (above maximum load) that needs to be maintained. This will depend on the step loads likely to be seen in the application and the response expected.

The peak inductor current under normal operation (maximum load) depends on the load and the inductance. It is given by

$$I_{peak} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (15)$$

where

- I_{RIPPLE} was determined in the output filter section.

Example: Let I_{RIPPLE} be 2A. The peak current under normal operation is

$$I_{peak} = 10A + \frac{2A}{2} = 11A \quad (16)$$

Usually it is necessary to set the current limit about 20% higher than the peak inductor current. This overload margin helps handle sudden load changes. A 20% margin will require a current limit of 11A*1.2 = 13.2A so RLIM will need to be

$$RLIM = \frac{Rds_{100} \times I_{CLIM}}{62\ \mu A} \tag{17}$$

$$RLIM = \frac{7\ m\Omega \times 13.2A}{62\ \mu A} = 1.49\ k\Omega \tag{18}$$

A standard value of 1.5kΩ may be chosen.

A larger overload margin greater than 20% (say 40%) would help in obtaining good dynamic response. This is necessary if the load steps from an extremely low value (say zero) up to maximum load current. A larger current limit will, however, generate stresses in the FETs during abnormal load condition (such as a shorted output). A 40% overload margin equates to setting I_{CLIM} at 15.4A (I_{CLIM} = 11A*1.4 = 15.4A). This requires RLIM be 7mΩ*15.4A/62µA = 1.73kΩ (a standard value of 1.74kΩ may be chosen).

Summarizing, for a 1.2V/10A rated output, using a 1.9µH inductor and any low side equivalent FET (same R_{DS_ON} as Si4442DY):

- For 20% overload margin, select current limit resistor to be 1.5kΩ
- For 40% overload margin, select current limit resistor to be 1.74kΩ

Repeating the calculation for a 1µH inductor for a 1.8V/20A rated output, and any low side equivalent FET (with the same R_{DS_ON} as Si4838DY) we get the following requirement:

- For 20% overload margin, select current limit resistor to be 1.87kΩ
- For 40% overload margin, select current limit resistor to be 2.15kΩ

Note that if the lower FET R_{DS_ON} is different from the one used on the Evaluation board, the current limit resistor RLIM must be recalculated according the new R_{DS_ON}.

INPUT CAPACITOR

For buck regulators, the input capacitor provides most of the pulsed current waveform demanded by the switch.

For the LM2657, there are two ways of calculating and meeting the input capacitance requirement. They are to use separate input capacitors for each channel or use a single capacitor for both channels.

By keeping separate input capacitors the possibility of interaction between the two channels is reduced, and the layout is less critical. Using two components also requires more board space and may be more costly.

The reason cost can be reduced when using one input capacitor in the LM2657 is because the two channels run 180° out of phase (interleaved switching). It can be shown that this dramatically reduces the ripple current requirement at the input. See Figure 15 for typical waveforms to understand how this happens.

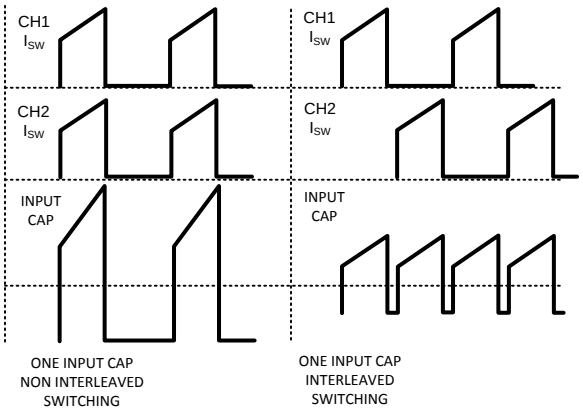


Figure 15. Switch and Input Capacitor Currents

Example: Consider two channels running at 1.8V/20A and 1.2V/10A. What is the worst case input capacitor RMS current if the input varies from 5V to 28V?

Step 1: Call the output with the higher voltage as V_{OUT1} and the other as V_{OUT2}. Then find the ratio 'y' as shown below

$$y = \frac{V_{OUT2}}{V_{OUT1}} = \frac{1.2}{1.8} = 0.67 \tag{19}$$

As a check, y should be less than or equal to 1 (since we said $V_{OUT2} \leq V_{OUT1}$) .

Step 2: The equation for the input current reveals that the worst-case occurs when the duty cycle of the first channel is:

$$D1 = \frac{I_{OUT1}^2 + (y \times I_{OUT2}^2)}{2 \times (I_{OUT1} + (I_{OUT2} \times y))^2} \tag{20}$$

So

$$D1 = \frac{20^2 + (0.67 \times 10^2)}{2 \times (20 + (10 \times 0.67))^2} = 0.33 \tag{21}$$

Therefore, the input voltage to calculate the worst case RMS input current is:

$$V_{IN} = \frac{V_{OUT1}}{D1} = \frac{1.8}{0.33} = 5.49V \tag{22}$$

Step 3: Calculate the duty cycle of the other channel when this happens

$$D2 = \frac{V_{OUT2}}{V_{IN}} = 0.24 \tag{23}$$

Step 4: Calculate input capacitor RMS current by using the known equation

$$I_{IN} = \sqrt{(I_{OUT1}^2 \times D1) + (I_{OUT2}^2 \times D2) - [I_{OUT1} \times D1 + I_{OUT2} \times D2]^2}$$

$$I_{IN} = \sqrt{(20^2 \times 0.33) + (10^2 \times 0.24) - [(20 \times 0.33) + (10 \times 0.24)]^2} \tag{24}$$

Solving

$$I_{IN} = 8.66A \tag{25}$$

Step 5: The current calculated in Step 4 might not be the maximum current provided by the input capacitor. This is because we have only considered the case when both channels are loaded. In some cases, the maximum current is drawn from the input capacitor when a single channel is loaded.

Suppose one channel was completely unloaded. So in effect there is only a single output of 1.2V/10A. The equation for the RMS current through the input capacitor is then

$$I_{IN} = I_{OUT} \sqrt{D(1\text{-}D)} \tag{26}$$

The function D(1-D) has a maxima at D = 0.5. This would correspond to an input voltage of 1.2V/0.5 = 2.4V (although the switcher is not operational at this input voltage, we will continue with the calculation). The input capacitor current at this worst case input voltage would be

$$I_{IN} = 10 \sqrt{0.5(1 - 0.5)} = 10 \times 0.5 = 5A \tag{27}$$

We must always take the higher of the two values calculated to ensure proper component selection.

Note, step 5 is used to calculate the input capacitor current requirements for either single channel operation or when using separate input capacitors.

In all cases, the input capacitor(s) must be positioned physically close to their respective stages. If separate input capacitors are being used for each channel, the input traces to the two inputs must be long and thin so as to introduce a measure of high frquency decoupling between the now separated stages.

The equations used in the above sections apply only if the duty cycles of both channels are less than or equal to 50% (and there is no overlap in the current waveforms).

MODULATOR GAIN/COMPENSATION

The LM2657 may be used with type 3 compensation. A model illustrating the use of type 3 compensation is shown in Figure 16. Using this model we obtain the modulator transfer function:

$$H(s) = k \frac{(sA_1 + 1)(sA_2 + 1)}{s(sA_3 + A_4)(sA_5 + 1)}$$

where

- $A1 = R_3C_2$
- $A2 = C_1(R_1 + R_2)$
- $A3 = R_2R_3C_2C_3$
- $A4 = R_2(C_2 + C_3)$
- $A5 = R_1C_1$
- $k = 10V/V$
- $s = j\omega$ (28)

From this equation we make some approximations and say that

$A_1 = 1/\omega_1 = R_3C_2$

$A_2 = 1/\omega_2 \cong R_2C_1$

$A_3 = 1/\omega_3 \cong R_3C_3$

$A_4 = 1$

$A_5 = 1/\omega_4 \cong R_1C_1$

$k \cong 10\omega_1(R_1 / R_2)$

Since the unity gain bandwidth of the error amplifier is taken as 6.5MHz, its effect on frequency response is ignored in this analysis.

The output filter transfer function may be espressed as:

$$H_O(s) = \frac{\frac{s}{\omega_{2A}} + 1}{\frac{s^2}{\omega_{1A}^2} + \frac{1}{Q}\frac{s}{\omega_{1A}} + 1}$$

Where

- $\omega_{1A} = \frac{1}{\sqrt{LC}}$
- $\omega_{2A} = \frac{1}{CR_{esr}}$
- $Q = \frac{R_{LOAD}}{\sqrt{L/C}}$
- $s = j\omega$ (29)

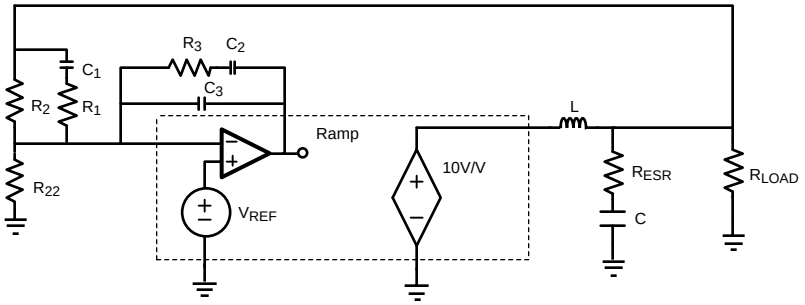


Figure 16. LM2657 Closed Loop Model with Type 3 Compensation

Component values may be selected according to the following guideline:

$\omega_3 = \omega_{2A}$, $\omega_4 = 6.28 \times f_{SW}/2$, $\omega_1 = \omega_2 = \omega_{1A}$.

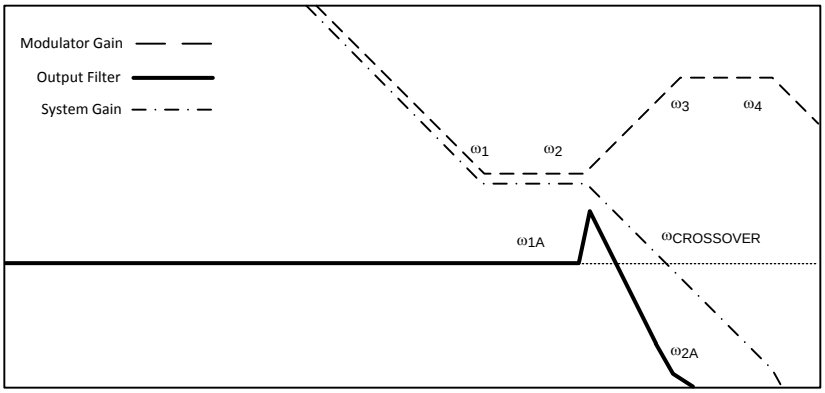


Figure 17. Bode Magnitude Plot of Relative Pole and Zero Locations

We start with an initial value for R2 and midband gain (gain between zeros ω_1 and ω_2). These values are typically $R_2 = 43.2k\Omega$ and Midband gain = 15dB. To calculate the remaining component values

$$R_1 = \frac{1}{\omega_4 C_1} \tag{30}$$

$$R_3 = 10 \left(\frac{\text{MidbandGain}}{20} - 1 \right) R_2 \tag{31}$$

$$C_1 = \frac{1}{\omega_2 R_2} \tag{32}$$

$$C_2 = \frac{\omega_2 R_2}{\omega_1 R_3} C_1 \tag{33}$$

$$C_3 = \frac{1}{\omega_3 R_3} \tag{34}$$

This provides the user a fast and easy way of compensating the switcher.

When applying this guide, there are several things to keep in mind. The crossover frequency ($f_{CROSSOVER} = \omega_{CROSSOVER}/6.28$) should be less than 1/5 the switching frequency. The designer should also consider the control loop damping. A phase margin (ϕ_m) of 52° is typically considered optimal. While this is typical, any phase margin between 45° and 90° should provide acceptable performance.

If a specific phase margin is desired, a more detailed design procedure may be employed.

A straightline approximation of the output filter, modulator, and system frequency response is shown in Figure 17. While the specific pole and zero locations will depend on the system variables, this plot may be used as a general guide.

A helpful approach in finding the appropriate values is to draw a straightline approximation of the output filters Bode phase plot. Using the approximate compensator pole and zero locations given, the designer may concern himself/herself only with the placement of these poles and zeros. This is done to achieve the desired phase margin at the desired $f_{CROSSOVER}$.

Once a satisfactory phase margin is realized, the designer may concern himself/herself with the compensator gain. Since the pole and zero locations are known, all that remains is to make a Bode magnitude plot. A good starting point is at the crossover frequency. Starting at the crossover frequency the gain (zero at fcrossover) and slope (-20 dB/Decade) are known. At this point it becomes quite easy to draw the remainder of the plot and calculate component values.

This approach is quite intuitive and provides an accurate way of compensating the switcher for a variety of component values.

SNUBBER CIRCUITS

Some users may experience ringing on the switch pin. Ringing is caused by parasitic resonances in the circuit. Such resonances may produce excessive EMI or reduce efficiency. To prevent such problems, a 'snubber' circuit may be used as shown in Figure 18.

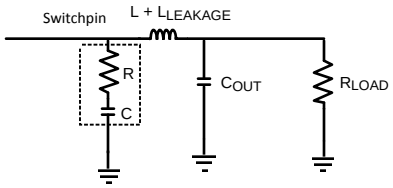


Figure 18. Portion Of Circuit Containing Snubber (RC network in boxed diagram)

Values are typically C ≅ 4 x Transistor Output Capacitance (C_{DS}) and

$$R \approx \sqrt{L_{Leakage}/C_{Transistor\_Output}} \quad (35)$$

Typical values are C ≅ 3300pF and R ≅ 4.7Ω. The snubber resistor should be able to dissipate at least P ≅ $f_{SW}CV_{SW}^2$.

LAYOUT GUIDELINES

When laying out the board, one should carefully consider the routing of the freq trace and surrounding traces. Any noise induced into this trace can cause jitter problems. These same routing guidelines and troubles apply to the VDD and V5 traces. A minimum 0.1µF (ceramic) capacitor should be placed on the component side very close to the IC with no intervening vias between these capacitors and the VDD/SGND and V5/PGND pins respectively.

For high current applications, it is particularly important that C_{IN} be placed near the FETs. Also, the traces for each channel should be well separated to minimize cross talk between channels. In the critical path (path of highest current) the size of the traces should be carefully considered. Should thermal dissipation or resistive losses be a problem, one may connect layers of the board in parallel using vias.

For applications requiring low R_{DS_ON} FETs, users may experience difficulty setting the current limit. This is due to the relative magnitude of the FETs resistance in comparison with the trace resistance. In instances such as this, the designer should minimize parasitic sources of resistance in the current limit traces.

For more information on layout, consult 'Layout Guidelines' Application Note AN-1229 SNVA054.

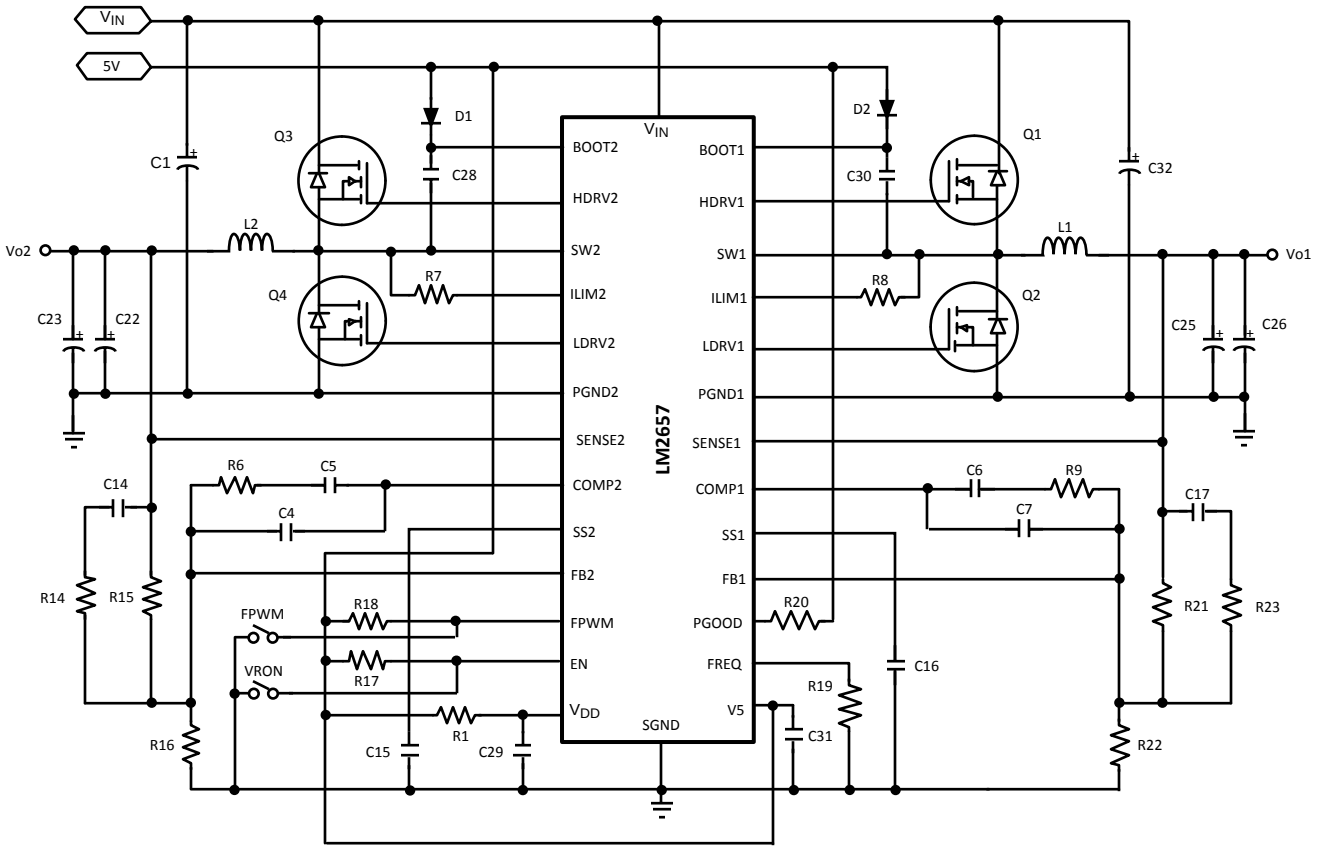


Figure 19. Typical Application (Expanded View)

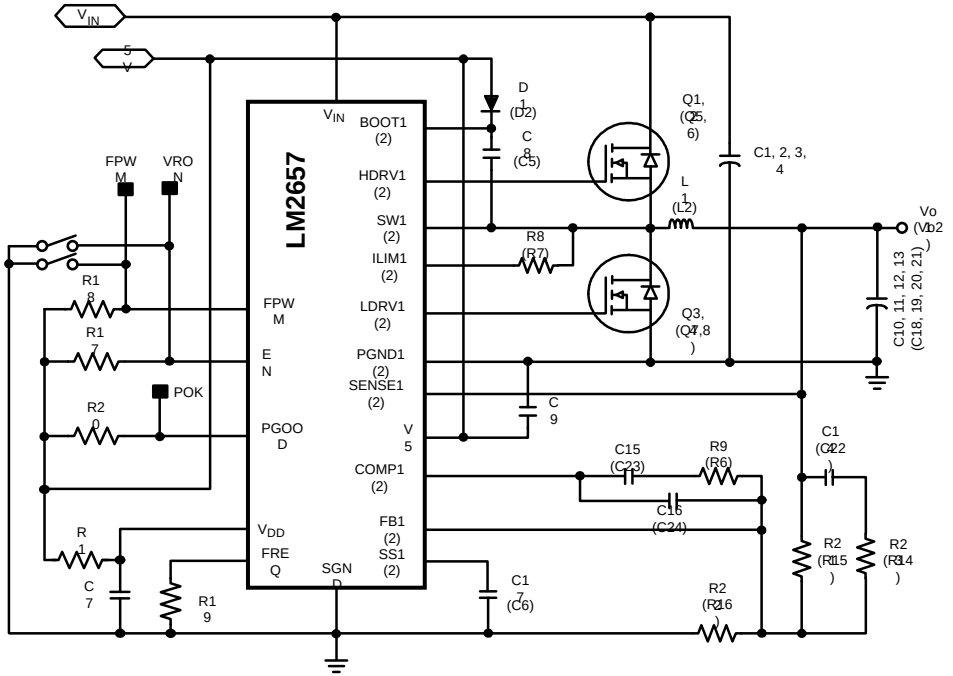


Figure 20. High Current Application Circuit

Table 1. Bill of Materials (Figure 19)
(Low Current Board, 5V-to-2.5V at 1A and 5V-to-1.2V at 1A conversion)(1)

Designator	Function	Description	Vendor	Part Number
C1	Cin	470µF	Sanyo	6MV470WG
C4	Comp Cap	180pF	Vishay	
C5	Comp Cap	2.7nF	Vishay	
C6	Comp Cap	2.7nF	Vishay	
C7	Comp Cap	150pF	Vishay	
C14	Cff (Ch2)	560pF	Vishay	
C15	Soft-start cap (Ch 2)	0.1µF	Vishay	
C16	Soft-start cap (Ch 1)	0.1µF	Vishay	
C17	Cff (Ch1)	680pf	Vishay	
C22	Output Cap (Ch2)	68µF	Sanyo	10TPE68M
C25	Output Cap (Ch1)	68µF	Sanyo	10TPE68M
C28	Cboot (Ch2)	0.1µF	Vishay	Ceramic
C29	V5 Decoupling	0.1µF	Vishay	Ceramic
C30	Cboot (Ch2)	0.1µF	Vishay	Ceramic
C31	V5 Decoupling	0.1µF	Vishay	Ceramic
C32	Cin - Optonal	470µF	Sanyo	6MV470WG
R1	V5 to VDD Series pass	10, 5%	Vishay	
R6	Comp res (series with C, Ch2)	9.09k 1%	Vishay	
R7	Rlim (Ch 2)	909 1%	Vishay	
R8	Rlim (Ch 1)	866, 1%	Vishay	
R9	Comp Res (Series with C, Ch1)	11k 1%	Vishay	
R14	Rff (Ch 2)	1.74k 1%	Vishay	
R15	Res divider, upper (Ch 2)	43.2k 1%	Vishay	
R16	Res divider, lower (Ch 2)	43.2k 1%	Vishay	
R17	Enable pullup	12.7k 1%	Vishay	
R18	FPWM pullup	12.7k 1%	Vishay	
R19	Freq adj	22.1k 1%	Vishay	
R20	Pgood pullup	12.7k 1%	Vishay	
R21	Res divider, upper (Ch1)	43.2k 1%	Vishay	
R22	Res divider, lower (Ch1)	13.7k 1%	Vishay	
R23	Rff (Ch 1)	1.37k 1%	Vishay	
L1	Output Inductor (Ch1)	15µH	Coilcraft	DO1813P-472HC
L2	Output Inductor (Ch2)	10µH	Coilcraft	DO1813P-472HC
D1	Cboot diode (Ch 1)		Central	CMPD6263C-NST
D2	Cboot diode (Ch 2)		Central	CMPD6263C-NST
Q1	Upper FET (Ch 1)	Power FET	Vishay	Si9804DY
Q2	Lower FET (Ch1)	Power FET	Vishay	Si9804DY
Q4	Upper FET (Ch2)	Power FET	Vishay	Si9804DY
Q5	Lower FET (Ch2)	Power FET	Vishay	Si9804DY
U1	Controller	Controller	TI	LM2657

(1) In the BOMs listed above, the user has the option of using certain components in parallel. For example, in the typical apps board, C22 is a 100µF capacitor and C23 is optional. The user now has the option of using (2) 47µF capacitors. If this is done the compensation will need to be changed accordingly (C4 will be approximately half its original value.)

Table 2. Bill of Materials (Figure 19)
(Typical Apps Board, 5V-to-2.5V at 5A and 5V-to-1.2V at 5A conversion)(1)

Designator	Function	Description	Vendor	Part Number
C1	Cin	470µF	Sanyo	6MV470WG
C4	Comp Cap	4.7pF	Vishay	
C5	Comp Cap	1.2nF	Vishay	
C6	Comp Cap	1.2nF	Vishay	
C7	Comp Cap	4.7pF	Vishay	
C14	Cff (Ch2)	100pF	Vishay	
C15	Soft-start cap (Ch 2)	0.1µF	Vishay	
C16	Soft-start cap (Ch 1)	0.1µF	Vishay	
C17	Cff (Ch1)	100pf	Vishay	
C22	Output Cap (Ch2)	100µF	MuRata	GRM31CR60J226KE19L
C25	Output Cap (Ch1)	100µF	MuRata	GRM31CR60J226KE19L
C28	Cboot (Ch2)	0.1µF	Vishay	Ceramic
C29	V5 Decoupling	0.1µF	Vishay	Ceramic
C30	Cboot (Ch1)	0.1µF	Vishay	Ceramic
C31	V5 Decoupling	0.1µF	Vishay	Ceramic
C32	Cin - Optonal	470µF	Sanyo	6MV470WG
R1	V5 to VDD Series pass	10, 5%	Vishay	
R6	Comp res (series with C, Ch2)	136k 1%	Vishay	
R7	Rlim (Ch 2)	4.22k 1%	Vishay	
R8	Rlim (Ch 1)	4.32k, 1%	Vishay	
R9	Comp Res (Series with C, Ch1)	136k 1%	Vishay	
R14	Rff (Ch 2)	5.11k 1%	Vishay	
R15	Res divider, upper (Ch 2)	43.2k 1%	Vishay	
R16	Res divider, lower (Ch 2)	43.2k 1%	Vishay	
R17	Enable pullup	12.7k 1%	Vishay	
R18	FPWM pullup	12.7k 1%	Vishay	
R19	Freq adj	22.1k 1%	Vishay	
R20	Pgood pullup	12.7k 1%	Vishay	
R21	Res divider, upper (Ch1)	43.2k 1%	Vishay	
R22	Res divider, lower (Ch1)	13.7k 1%	Vishay	
R23	Rff (Ch 1)	5.1k 1%	Vishay	
L1	Output Inductor (Ch1)	4.7µH	Coilcraft	DO3316P-472HC
L2	Output Inductor (Ch2)	2.2µH	Coilcraft	DO3316P-472HC
D1	Cboot diode (Ch 1)		Central	CMPD6263C-NST
D2	Cboot diode (Ch 2)		Central	CMPD6263C-NST
Q1	Upper FET (Ch 1)	Power FET	Vishay	Si9804DY
Q2	Lower FET (Ch1)	Power FET	Vishay	Si9804DY
Q4	Upper FET (Ch2)	Power FET	Vishay	Si9804DY
Q5	Lower FET (Ch2)	Power FET	Vishay	Si9804DY
U1	Controller	Controller	TI	LM2657

(1) In the BOMs listed above, the user has the option of using certain components in parallel. For example, in the typical apps board, C22 is a 100µF capacitor and C23 is optional. The user now has the option of using (2) 47µF capacitors. If this is done the compensation will need to be changed accordingly (C4 will be approximately half its original value.)

Table 3. Bill of Materials (Figure 20)
(High Current Board, 5V-to-1.8V@20A and 5V-to-1.2V@10A conversion)(1)

Designator	Function	Description	Vendor	Part Number
C1,2,3,4	Cin (Ch 2)	(4) 1800µF	TDK	10MV1800WG
C5	Cboot (Ch2)	0.1µF	Vishay	Ceramic
C6	Soft-start cap (Ch 2)	0.1µF	Vishay	
C7	V5 Decoupling	0.1µF	Vishay	Ceramic
C8	Cboot (Ch2)	0.1µF	Vishay	Ceramic
C9	V5 Decoupling	0.1µF	Vishay	Ceramic
C10,11,12	Output Cap (Ch1)	2200µF	Sanyo	6MV2200WG
C14	Cff (Ch1)	680pf	Vishay	
C15	Comp Cap	680pF	Vishay	
C16	Comp Cap	15pF	Vishay	
C17	Soft-start cap (Ch 1)	0.1µF	Vishay	
C18,19,20	Output Cap (Ch2)	2200µF	Sanyo	6MV2200WG
C22	Cff (Ch2)	680pF	Vishay	
C23	Comp Cap	680pF	Vishay	
C24	Comp Cap	15pF	Vishay	
R1	V5 to VDD Series pass	10, 5%	Vishay	
R6	Comp res (series with C, Ch2)	57.6k 1%	Vishay	
R7	Rlim (Ch 2)	1.74k 1%	Vishay	
R8	Rlim (Ch 1)	2.15k, 1%	Vishay	
R9	Comp Res (Series with C, Ch1)	57.6k 1%	Vishay	
R14	Rff (Ch 2)	12.7k 1%	Vishay	
R15	Res divider, upper (Ch 2)	43.2k 1%	Vishay	
R16	Res divider, lower (Ch 2)	43.2k 1%	Vishay	
R17	Enable pullup	12.7k 1%	Vishay	
R18	FPWM pullup	12.7k 1%	Vishay	
R19	Freq adj	22.1k 1%	Vishay	
R20	Pgood pullup	12.7k 1%	Vishay	
R21	Res divider, upper (Ch1)	43.2k 1%	Vishay	
R22	Res divider, lower (Ch1)	21.5k 1%	Vishay	
R23	Rff (Ch 1)	12.7k 1%	Vishay	
L1	Output Inductor (Ch1)	1µH	Coilcraft	SER2009-102MX
L2	Output Inductor (Ch2)	1.9µH	TDK	RLF12560T-1R9N120
D1	Cboot diode (Ch 1)		Central	CMPD6263C-NST
D2	Cboot diode (Ch 2)		Central	CMPD6263C-NST
Q1	Upper FET (Ch 1)	Power FET	Vishay	Si4838Dy
Q2	Lower FET (Ch1)	Power FET	Vishay	Si4838Dy
Q4	Upper FET (Ch2)	Power FET	Vishay	Si4442Dy
Q5	Lower FET (Ch2)	Power FET	Vishay	Si4442Dy
U1	Controller	Controller	TI	LM2657

(1) In the BOMs listed above, the user has the option of using certain components in parallel. For example, in the typical apps board, C22 is a 100µF capacitor and C23 is optional. The user now has the option of using (2) 47µF capacitors. If this is done the compensation will need to be changed accordingly (C4 will be approximately half its original value.)

REVISION HISTORY

Changes from Revision A (March 2013) to Revision B	Page
• Changed layout of National Data Sheet to TI format	29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2657MTC/NOPB	OBSOLETE	TSSOP	PW	28		TBD	Call TI	Call TI	-40 to 125	LM2657 MTC	
LM2657MTCX/NOPB	OBSOLETE	TSSOP	PW	28		TBD	Call TI	Call TI	-40 to 125	LM2657 MTC	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

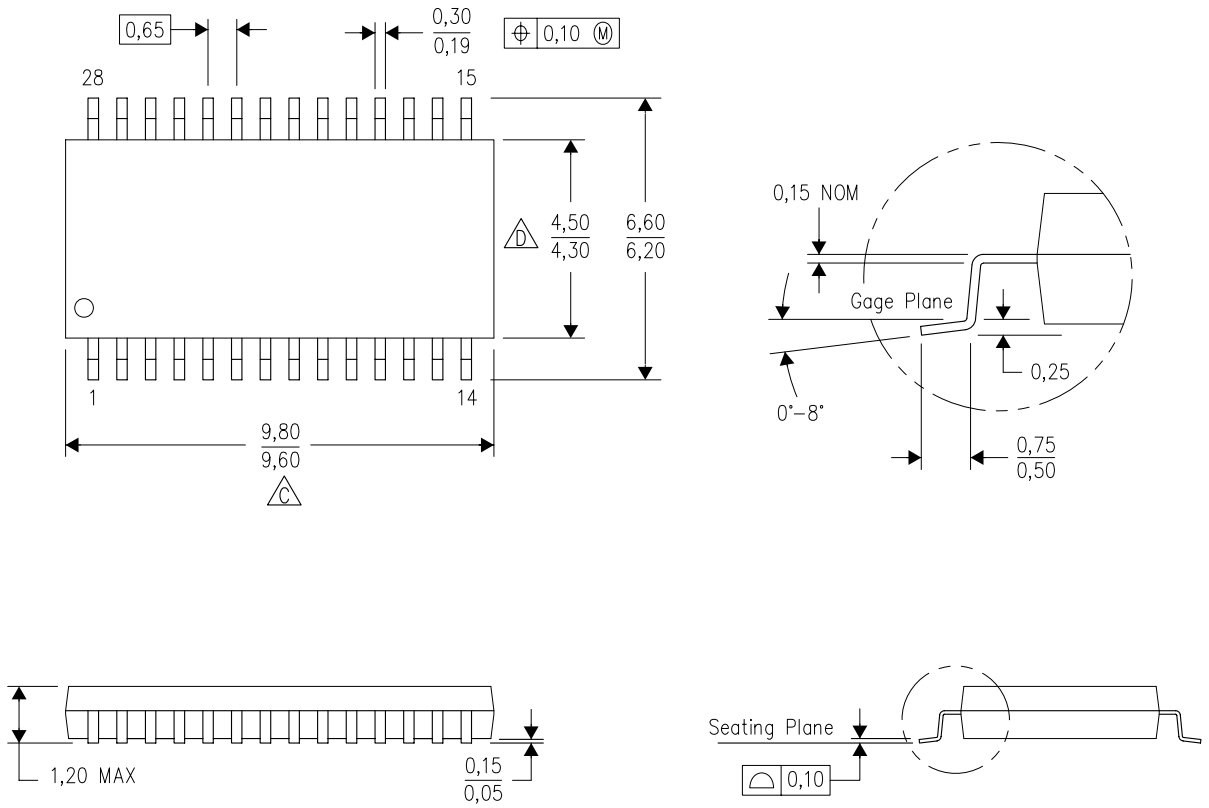
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PW (R–PDSO–G28) PLASTIC SMALL OUTLINE



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NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

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