



THE DATASHEET OF TLC2274AMPWREP



TLC227x-EP, TLC227xA-EP Advanced LinCMOS™ RAIL-TO-RAIL OPERATIONAL AMPLIFIERS

SGLS131B – JULY 2002 – REVISED DECEMBER 2003

- **Controlled Baseline**
 - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product Change Notification**
- **Qualification Pedigree†**
- **Output Swing Includes Both Supply Rails**
- **Low Noise . . . 9 nV/√Hz Typ at f = 1 kHz**
- **Low Input Bias Current . . . 1 pA Typ**
- **Fully Specified for Both Single-Supply and Split-Supply Operation**
- **Common-Mode Input Voltage Range Includes Negative Rail**
- **High-Gain Bandwidth . . . 2.2 MHz Typ**
- **High Slew Rate . . . 3.6 V/μs Typ**
- **Low Input Offset Voltage**
950 μV Max at T_A = 25°C
- **Macromodel Included**
- **Performance Upgrades for the TS272, TS274, TLC272, and TLC274**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

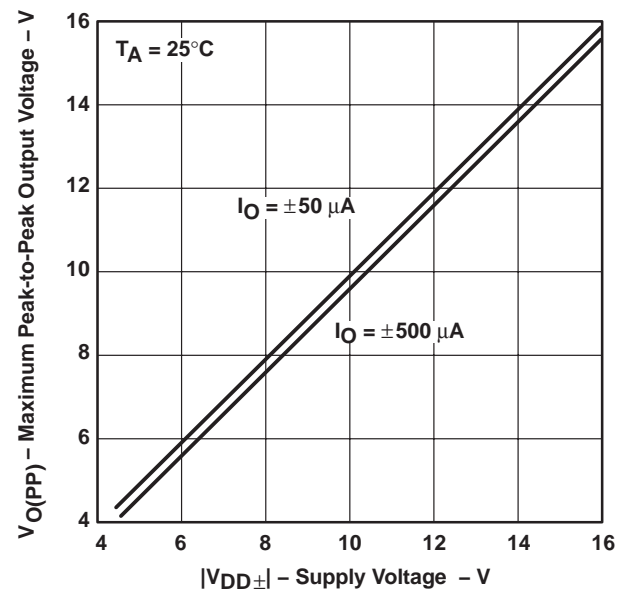
description

The TLC2272A and TLC2274A are dual and quadruple operational amplifiers from Texas Instruments. Both devices exhibit rail-to-rail output performance for increased dynamic range in single- or split-supply applications. The TLC227xA family offers 2 MHz of bandwidth and 3 V/μs of slew rate for higher speed applications. These devices offer comparable ac performance while having better noise, input offset voltage, and power dissipation than existing CMOS operational amplifiers. The TLC227xA has a noise voltage of 9 nV/√Hz, two times lower than competitive solutions.

The TLC227xA, exhibiting high input impedance and low noise, is excellent for small-signal conditioning for high-impedance sources, such as piezoelectric transducers. Because of the micro-power dissipation levels, these devices work well in hand-held monitoring and remote-sensing applications. In addition, the rail-to-rail output feature, with single- or split-supplies, makes this family a great choice when interfacing with analog-to-digital converters (ADCs). For precision applications, the TLC227xA family has a maximum input offset voltage of 950 μV. This family is fully characterized at 5 V and ±5 V.

The TLC2272/4 also makes great upgrades to the TLC272/4 or TS272/4 in standard designs. They offer increased output dynamic range, lower noise voltage, and lower input offset voltage. This enhanced feature set allows them to be used in a wider range of applications.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
VS
SUPPLY VOLTAGE



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Advanced LinCMOS is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2002 Texas Instruments Incorporated

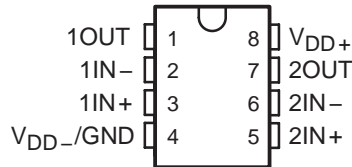
TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

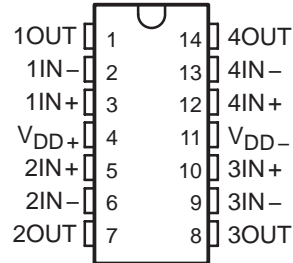
AVAILABLE OPTIONS

T _A	V _{IO} max At 25°C	PACKAGED DEVICES	
		SMALL OUTLINE (D)	TSSOP (PW)
-55°C to 125°C	950 μV 2.5 mV	TLC2272AMDREP TLC2272MDREP	TLC2272AMPWREP TLC2272MPWREP
-55°C to 125°C	950 μV 2.5 mV	TLC2274AMDREP TLC2274MDREP	TLC2274AMPWREP TLC2274MPWREP

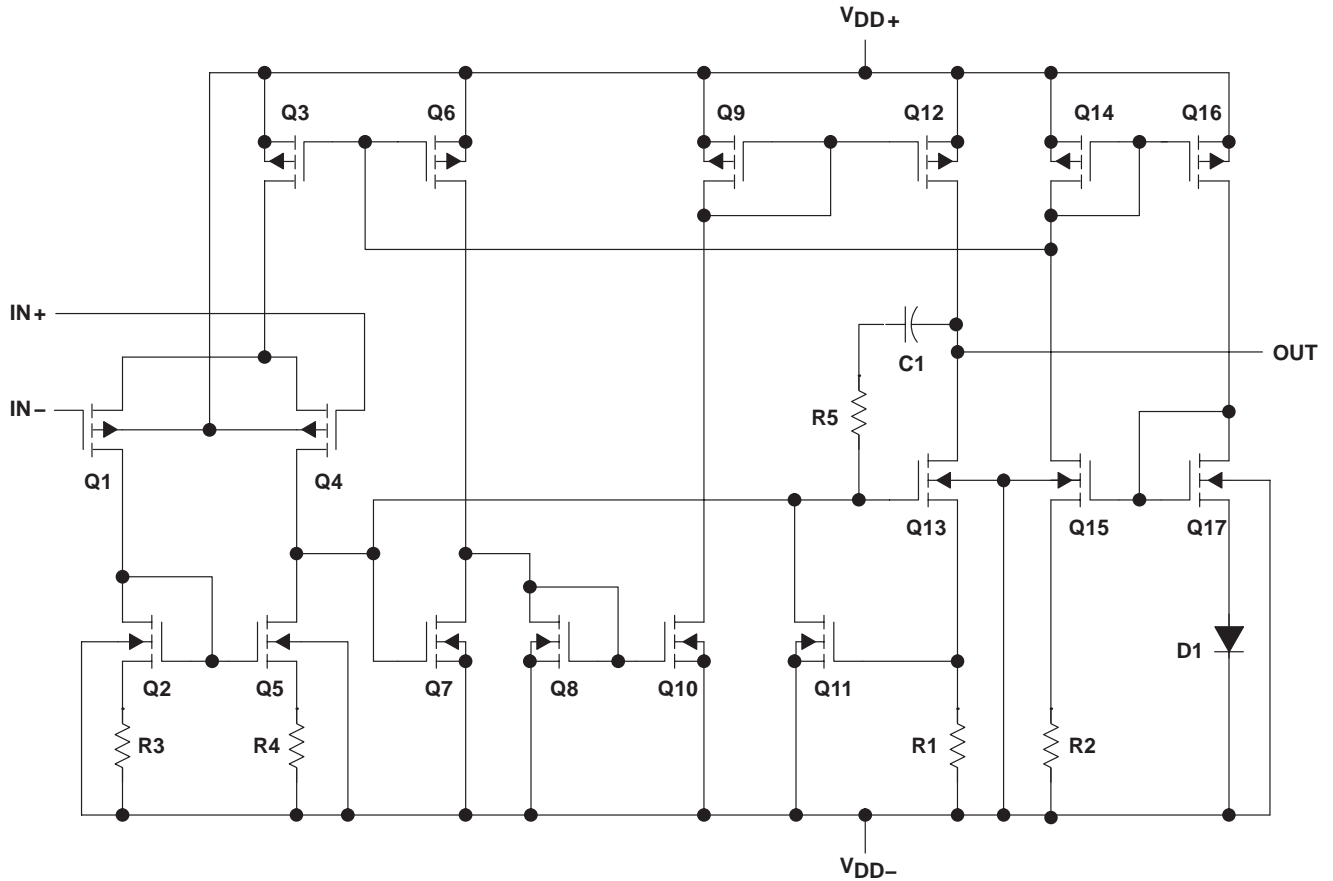
TLC2272
D OR PW PACKAGE
(TOP VIEW)



TLC2274
D OR PW PACKAGE
(TOP VIEW)



equivalent schematic (each amplifier)



ACTUAL DEVICE COMPONENT COUNT†		
COMPONENT	TLC2272	TLC2274
Transistors	38	76
Resistors	26	52
Diodes	9	18
Capacitors	3	6

† Includes both amplifiers and all ESD, bias, and trim circuitry

TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD+} (see Note 1)	8 V
Supply voltage, V_{DD-} (see Note 1)	-8 V
Differential input voltage, V_{ID} (see Note 2)	± 16 V
Input voltage range, V_I (any input, see Note 1)	$V_{DD-} - 0.3$ V to V_{DD+}
Input current, I_I (any input)	± 5 mA
Output current, I_O	± 50 mA
Total current into V_{DD+}	± 50 mA
Total current out of V_{DD-}	± 50 mA
Duration of short-circuit current at (or below) 25°C (see Note 3)	unlimited
Continuous total dissipation	See Dissipation Rating Table
Operating free-air temperature range, T_A	-55°C to 125°C
Storage temperature range (see Note 4)	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D or PW package	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between V_{DD+} and V_{DD-} .
 2. Differential voltages are at $IN+$ with respect to $IN-$. Excessive current will flow if input is brought below $V_{DD-} - 0.3$ V.
 3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
 4. Long term high-temperature storage and/or extended use at maximum recommended operating conditions may result in a reduction of overall device life. See http://www.ti.com/ep_quality for additional information on enhanced plastic packaging.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D-8	725 mW	5.8 mW/°C	464 mW	337 mW	145 mW
D-14	950 mW	7.6 mW/°C	608 mW	494 mW	190 mW
PW-8	525 mW	4.2 mW/°C	336 mW	273 mW	105 mW
PW-14	700 mW	5.6 mW/°C	448 mW	364 mW	—

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{DD\pm}$	± 2.2	± 8	V
Input voltage, V_I	V_{DD-}	$V_{DD+} - 1.5$	V
Common-mode input voltage, V_{IC}	V_{DD-}	$V_{DD+} - 1.5$	V
Operating free-air temperature, T_A	-55	125	°C



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2272-EP electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V},$ $V_O = 0\text{ V},$ $V_{DD\pm} = \pm 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 5)		25°C	0.002			0.002		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range			800		800		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range			800		800			
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2	V	
		Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$ $I_{OH} = -200\ \mu\text{A}$ $I_{OH} = -1\text{ mA}$	25°C	4.99			4.99		V	
		25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
		25°C	4.25	4.65		4.25	4.65		
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V},$ $I_{OL} = 50\ \mu\text{A}$ $V_{IC} = 2.5\text{ V},$ $I_{OL} = 500\ \mu\text{A}$ $V_{IC} = 2.5\text{ V},$ $I_{OL} = 5\text{ mA}$	25°C	0.01			0.01		V	
		25°C	0.09	0.15		0.09	0.15		
		Full range			0.15		0.15		
		25°C	0.9	1.5		0.9	1.5		
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V},$ $V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega$ ‡	25°C	10	35		10	35	V/mV
			Full range	10			10		
		$R_L = 1\text{ m}\Omega$ ‡	25°C	175			175		
r_{id} Differential input resistance		25°C	10^{12}			10^{12}		Ω	
r_i Common-mode input resistance		25°C	10^{12}			10^{12}		Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz},$ P package	25°C	8			8		pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz},$ $A_V = 10$	25°C	140			140		Ω	
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V},$ $V_O = 2.5\text{ V},$ $R_S = 50\ \Omega$	25°C	70	75		70	75	dB	
		Full range	70			70			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V},$ $V_{IC} = V_{DD}/2,$ No load	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load	25°C	2.2	3		2.2	3	mA	
		Full range			3		3		

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2272-EP operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 1.25\text{ V to } 2.75\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	2.3	3.6		2.3	3.6	V/ μ s	
		Full range	1.7			1.7			
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		50			50	nV/ $\sqrt{\text{Hz}}$	
		25°C		9			9		
V_{NPP}	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to } 1\text{ Hz}$ $f = 0.1\text{ Hz to } 10\text{ Hz}$	25°C		1			1	μ V	
		25°C		1.4			1.4		
I_n	Equivalent input noise current	25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to } 2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ‡	25°C	$A_V = 1$	0.0013%		0.0013%			
			$A_V = 10$	0.004%		0.004%			
			$A_V = 100$	0.03%		0.03%			
	Gain-bandwidth product $f = 10\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		2.18			2.18	MHz	
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		1			1	MHz	
t_s	Settling time $A_V = -1$, Step = $0.5\text{ V to } 2.5\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	To 0.1%	1.5		1.5		μ s	
			To 0.01%	2.6		2.6			
ϕ_m	Phase margin at unity gain $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C		50°			50°		
		25°C		10			10		
	Gain margin	25°C		10			10	dB	

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2272-EP electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V},$ $R_S = 50\ \Omega$ $V_O = 0\text{ V},$	25°C	300	2500		300	950	μV	
		Full range			3000		1500		
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2		$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 5)		25°C	0.002			0.002		$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA	
		Full range			800		800		
I_{IB} Input bias current	25°C	1	60		1	60	pA		
	Full range			800		800			
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega,$ $ V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V	
		Full range	-5 to 3.5			-5 to 3.5			
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$ $I_O = -200\ \mu\text{A}$ $I_O = -1\text{ mA}$	25°C		4.99			4.99	V	
		25°C	4.85	4.93		4.85	4.93		
		Full range	4.85			4.85			
		25°C	4.25	4.65		4.25	4.65		
V_{OM-} Maximum negative peak output voltage	$V_{IC} = 0\text{ V},$ $I_O = 50\ \mu\text{A}$ $V_{IC} = 0\text{ V},$ $I_O = 500\ \mu\text{A}$ $V_{IC} = 0\text{ V},$ $I_O = 5\text{ mA}$	25°C		-4.99			-4.99	V	
		25°C	-4.85	-4.91		-4.85	-4.91		
		Full range	-4.85			-4.85			
		25°C	-3.5	-4.1		-3.5	-4.1		
A_{VD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$ $R_L = 10\ \text{k}\Omega$ $R_L = 1\ \text{m}\Omega$	25°C	20	50		20	50	V/mV	
		Full range	20			20			
		25°C		300			300		
r_{id} Differential input resistance		25°C		10^{12}			10^{12}	Ω	
r_i Common-mode input resistance		25°C		10^{12}			10^{12}	Ω	
c_i Common-mode input capacitance	$f = 10\ \text{kHz},$ P package	25°C		8			8	pF	
z_o Closed-loop output impedance	$f = 1\ \text{MHz},$ $A_V = 10$	25°C		130			130	Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V},$ $V_O = 0\text{ V},$ $R_S = 50\ \Omega$	25°C	75	80		75	80	dB	
		Full range	75			75			
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD} = \pm 2.2\text{ V to } \pm 8\text{ V},$ $V_{IC} = 0\text{ V},$ No load	25°C	80	95		80	95	dB	
		Full range	80			80			
I_{DD} Supply current	$V_O = 2.5\text{ V},$ No load	25°C		2.4	3		2.4	3	mA
		Full range			3		3		

† Full range is -55°C to 125°C for M level part.

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2272-EP operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2272-EP			TLC2272A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 1\text{ V}$, $C_L = 100\text{ pF}$ $R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6	V/ μ s	
		Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		50			50	nV/ $\sqrt{\text{Hz}}$	
		$f = 1\text{ kHz}$	25°C		9		9		
V_{NPP}	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$	25°C		1		1	μ V	
		$f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1.4		1.4		
I_n	Equivalent input noise current		25°C		0.6		0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$ $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	$A_V = 1$	25°C		0.0011%		0.0011%		
		$A_V = 10$			0.004%		0.004%		
		$A_V = 100$			0.03%		0.03%		
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$ $R_L = 10\text{ k}\Omega$	25°C		2.25		2.25	MHz	
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54		0.54	MHz	
t_s	Settling time	$A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	To 0.1%	25°C		1.5		1.5	μ s
			To 0.01%			3.2		3.2	
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		52°		52°		
	Gain margin		25°C		10		10	dB	

† Full range is -55°C to 125°C for M level part.



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2274-EP electrical characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2274-EP			TLC2274A-EP			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_{DD} \pm \pm 2.5\text{ V}, V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950		μV	
		Full range			3000		1500			
α_{VIO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 5)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60		pA	
		Full range			800		800			
I_{IB} Input bias current		25°C	1	60		1	60		pA	
		Full range			800		800			
V_{ICR} Common-mode input voltage		$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	0 to 4	-0.3 to 4.2		0 to 4	-0.3 to 4.2		V
			Full range	0 to 3.5			0 to 3.5			
V_{OH} High-level output voltage	$I_{OH} = -20\ \mu\text{A}$	25°C	4.99		4.99			V		
		25°C	4.85	4.93		4.85	4.93			
		Full range	4.85		4.85					
		25°C	4.25	4.65		4.25	4.65			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 50\ \mu\text{A}$	25°C	0.01		0.01			V		
		25°C	0.09	0.15		0.09	0.15			
		Full range	0.15		0.15					
		25°C	0.9	1.5		0.9	1.5			
V_{OL} Low-level output voltage	$V_{IC} = 2.5\text{ V}, I_{OL} = 500\ \mu\text{A}$	25°C	0.01		0.01			V		
		25°C	0.09	0.15		0.09	0.15			
		Full range	0.15		0.15					
		25°C	0.9	1.5		0.9	1.5			
A_{VD} Large-signal differential voltage amplification	$V_{IC} = 2.5\text{ V}, V_O = 1\text{ V to }4\text{ V}$	$R_L = 10\text{ k}\Omega$ ‡	25°C	10	35		10	35	V/mV	
			Full range	10		10				
		$R_L = 1\text{ M}\Omega$ ‡	25°C	175		175				
r_{id} Differential input resistance		25°C	10^{12}			10^{12}		Ω		
r_i Common-mode input resistance		25°C	10^{12}			10^{12}		Ω		
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C	8			8		pF		
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C	140			140		Ω		
CMRR Common-mode rejection ratio	$V_{IC} = 0\text{ V to }2.7\text{ V}, V_O = 2.5\text{ V}, R_S = 50\ \Omega$	25°C	70	75		70	75	dB		
		Full range	70		70					
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)	$V_{DD} = 4.4\text{ V to }16\text{ V}, V_{IC} = V_{DD}/2, \text{ No load}$	25°C	80	95		80	95	dB		
		Full range	80		80					
I_{DD} Supply current	$V_O = 2.5\text{ V}, \text{ No load}$	25°C	4.4	6		4.4	6	mA		
		Full range	6		6					

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.



TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2274-EP operating characteristics at specified free-air temperature, $V_{DD} = 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2274-EP			TLC2274A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = 0.5\text{ V to }2.5\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	25°C	2.3	3.6		2.3	3.6		V/ μ s
		Full range	1.7			1.7			
V_n	Equivalent input noise voltage	$f = 10\text{ Hz}$		50			50		nV/ $\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage	$f = 0.1\text{ Hz to }1\text{ Hz}$		1			1		μ V
		$f = 0.1\text{ Hz to }10\text{ Hz}$		1.4			1.4		
I_n	Equivalent input noise current	25°C		0.6			0.6	fA/ $\sqrt{\text{Hz}}$	
THD + N	Total harmonic distortion plus noise $V_O = 0.5\text{ V to }2.5\text{ V}$, $f = 20\text{ kHz}$, $R_L = 10\text{ k}\Omega$ ‡	$A_V = 1$		0.0013%			0.0013%		
		$A_V = 10$	25°C		0.004%			0.004%	
		$A_V = 100$			0.03%			0.03%	
	Gain-bandwidth product	$f = 10\text{ kHz}$, $C_L = 100\text{ pF}$ ‡	$R_L = 10\text{ k}\Omega$ ‡,	25°C		2.18		2.18	MHz
BOM	Maximum output-swing bandwidth	$V_{O(PP)} = 2\text{ V}$, $R_L = 10\text{ k}\Omega$ ‡,	$A_V = 1$, $C_L = 100\text{ pF}$ ‡	25°C		1		1	MHz
t_s	Settling time	$A_V = -1$, Step = 0.5 V to 2.5 V, $R_L = 10\text{ k}\Omega$ ‡, $C_L = 100\text{ pF}$ ‡	To 0.1%	25°C		1.5		1.5	μ s
			To 0.01%			2.6		2.6	
ϕ_m	Phase margin at unity gain	$R_L = 10\text{ k}\Omega$ ‡,	$C_L = 100\text{ pF}$ ‡	25°C		50°		50°	
	Gain margin			25°C		10		10	dB

† Full range is -55°C to 125°C for M level part.

‡ Referenced to 2.5 V



TLC2274-EP electrical characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	T_A †	TLC2274-EP			TLC2274A-EP			UNIT	
			MIN	TYP	MAX	MIN	TYP	MAX		
V_{IO} Input offset voltage	$V_{IC} = 0\text{ V}, V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	300	2500		300	950	μV		
		Full range			3000		1500			
αV_{IO} Temperature coefficient of input offset voltage		25°C to 125°C	2			2			$\mu\text{V}/^\circ\text{C}$	
Input offset voltage long-term drift (see Note 5)		25°C	0.002			0.002			$\mu\text{V}/\text{mo}$	
I_{IO} Input offset current		25°C	0.5	60		0.5	60	pA		
		Full range			800		800			
I_{IB} Input bias current		25°C	1	60		1	60	pA		
		Full range			800		800			
V_{ICR} Common-mode input voltage	$R_S = 50\ \Omega, V_{IO} \leq 5\text{ mV}$	25°C	-5 to 4	-5.3 to 4.2		-5 to 4	-5.3 to 4.2	V		
		Full range	-5 to 3.5			-5 to 3.5				
V_{OM+} Maximum positive peak output voltage	$I_O = -20\ \mu\text{A}$	25°C	4.99		4.99		V			
		25°C	4.85	4.93	4.85	4.93				
		Full range	4.85		4.85					
		25°C	4.25	4.65	4.25	4.65				
V_{OM-} Maximum negative peak output voltage	$I_O = -1\text{ mA}$	25°C	-4.99		-4.99		V			
		25°C	-4.85	-4.91	-4.85	-4.91				
		Full range	-4.85		-4.85					
		25°C	-3.5	-4.1	-3.5	-4.1				
V_{AVD} Large-signal differential voltage amplification	$V_O = \pm 4\text{ V}$	$R_L = 10\text{ k}\Omega$	25°C	20	50	20	50	V/mV		
			Full range	20		20				
		$R_L = 1\text{ M}\Omega$	25°C	300			300			
			Full range	300			300			
r_{id} Differential input resistance		25°C	10^{12}			10^{12}			Ω	
r_i Common-mode input resistance		25°C	10^{12}			10^{12}			Ω	
c_i Common-mode input capacitance	$f = 10\text{ kHz}, \text{ N package}$	25°C	8			8			pF	
z_o Closed-loop output impedance	$f = 1\text{ MHz}, A_V = 10$	25°C	130			130			Ω	
CMRR Common-mode rejection ratio	$V_{IC} = -5\text{ V to } 2.7\text{ V}$ $V_O = 0\text{ V}, R_S = 50\ \Omega$	25°C	75	80		75	80	dB		
		Full range	75			75				
k_{SVR} Supply-voltage rejection ratio ($\Delta V_{DD\pm}/\Delta V_{IO}$)	$V_{DD\pm} = \pm 2.2\text{ V to } \pm 8\text{ V}, V_{IC} = 0\text{ V}, \text{ No load}$	25°C	80	95		80	95	dB		
		Full range	80			80				
I_{DD} Supply current	$V_O = 0\text{ V}, \text{ No load}$	25°C	4.8	6		4.8	6	mA		
		Full range	6			6				

† Full range is -55°C to 125°C for M level part.

NOTE 5: Typical values are based on the input offset voltage shift observed through 168 hours of operating life test at $T_A = 150^\circ\text{C}$ extrapolated to $T_A = 25^\circ\text{C}$ using the Arrhenius equation and assuming an activation energy of 0.96 eV.

TLC227x-EP, TLC227xA-EP
Advanced LinCMOS™ RAIL-TO-RAIL
OPERATIONAL AMPLIFIERS

SGLS131A – JULY 2002 – REVISED NOVEMBER 2003

TLC2274-EP operating characteristics at specified free-air temperature, $V_{DD\pm} = \pm 5\text{ V}$

PARAMETER	TEST CONDITIONS	T_A †	TLC2274-EP			TLC2274A-EP			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew rate at unity gain $V_O = \pm 2.3\text{ V}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$	25°C	2.3	3.6		2.3	3.6		V/ μ s
		Full range	1.7			1.7			
V_n	Equivalent input noise voltage $f = 10\text{ Hz}$ $f = 1\text{ kHz}$	25°C		50			50		nV/ $\sqrt{\text{Hz}}$
		25°C		9			9		
$V_{N(PP)}$	Peak-to-peak equivalent input noise voltage $f = 0.1\text{ Hz to }1\text{ Hz}$ $f = 0.1\text{ Hz to }10\text{ Hz}$	25°C		1			1		μ V
		25°C		1.4			1.4		
I_n	Equivalent input noise current	25°C		0.6			0.6		fA/ $\sqrt{\text{Hz}}$
THD + N	Total harmonic distortion plus noise $V_O = \pm 2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $f = 20\text{ kHz}$	25°C		$A_V = 1$		0.0011%		0.0011%	
				$A_V = 10$		0.004%		0.004%	
				$A_V = 100$		0.03%		0.03%	
	Gain-bandwidth product $f = 10\text{ kHz}$, $C_L = 100\text{ pF}$, $R_L = 10\text{ k}\Omega$	25°C		2.25			2.25		MHz
BOM	Maximum output-swing bandwidth $V_{O(PP)} = 4.6\text{ V}$, $R_L = 10\text{ k}\Omega$, $A_V = 1$, $C_L = 100\text{ pF}$	25°C		0.54			0.54		MHz
t_s	Settling time $A_V = -1$, Step = $-2.3\text{ V to }2.3\text{ V}$, $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		To 0.1%		1.5		1.5	μ s
				To 0.01%		3.2		3.2	
ϕ_m	Phase margin at unit gain $R_L = 10\text{ k}\Omega$, $C_L = 100\text{ pF}$	25°C		52°			52°		
		25°C		10			10		dB

† Full range is $-55^\circ\text{C to }125^\circ\text{C}$ for M level part.



TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
V_{IO}	Input offset voltage	Distribution vs Common-mode voltage 1 – 4 5, 6
α_{VIO}	Input offset voltage temperature coefficient	Distribution 7 – 10
I_{IB}/I_{IO}	Input bias and input offset current	vs Free-air temperature 11
V_I	Input voltage	vs Supply voltage vs Free-air temperature 12 13
V_{OH}	High-level output voltage	vs High-level output current 14
V_{OL}	Low-level output voltage	vs Low-level output current 15, 16
V_{OM+}	Maximum positive peak output voltage	vs Output current 17
V_{OM-}	Maximum negative peak output voltage	vs Output current 18
$V_{O(PP)}$	Maximum peak-to-peak output voltage	vs Frequency 19
I_{OS}	Short-circuit output current	vs Supply voltage vs Free-air temperature 20 21
V_O	Output voltage	vs Differential input voltage 22, 23
A_{VD}	Large-signal differential voltage amplification	vs Load resistance 24
	Large-signal differential voltage amplification and phase margin	vs Frequency 25, 26
	Large-signal differential voltage amplification	vs Free-air temperature 27, 28
z_o	Output impedance	vs Frequency 29, 30
CMRR	Common-mode rejection ratio	vs Frequency 31
		vs Free-air temperature 32
k_{SVR}	Supply-voltage rejection ratio	vs Frequency 33, 34
		vs Free-air temperature 35
I_{DD}	Supply current	vs Supply voltage 36, 37
		vs Free-air temperature 38, 39
SR	Slew rate	vs Load capacitance 40
		vs Free-air temperature 41
V_O	Inverting large-signal pulse response	42, 43
	Voltage-follower large-signal pulse response	44, 45
	Inverting small-signal pulse response	46, 47
	Voltage-follower small-signal pulse response	48, 49
V_n	Equivalent input noise voltage	vs Frequency 50, 51
	Noise voltage over a 10-second period	52
	Integrated noise voltage	vs Frequency 53
THD + N	Total harmonic distortion plus noise	vs Frequency 54
	Gain-bandwidth product	vs Supply voltage 55
		vs Free-air temperature 56
ϕ_m	Phase margin	vs Load capacitance 57
	Gain margin	vs Load capacitance 58

NOTE: For all graphs where $V_{DD} = 5\text{ V}$, all loads are referenced to 2.5 V.

TYPICAL CHARACTERISTICS

**DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE**

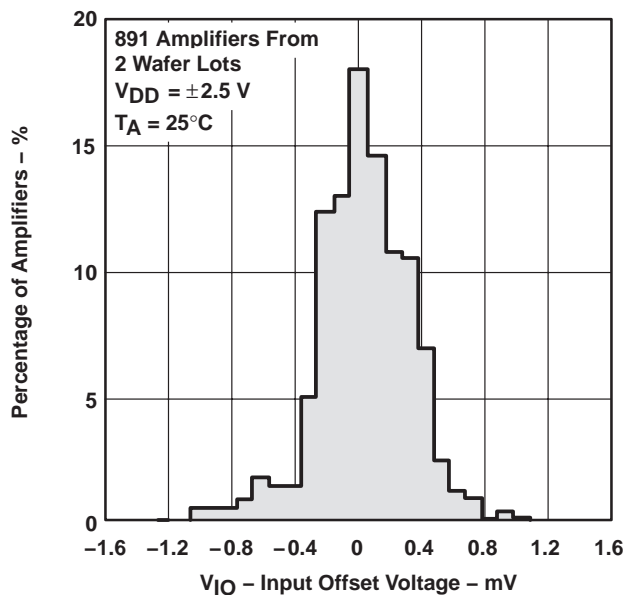


Figure 1

**DISTRIBUTION OF TLC2272
INPUT OFFSET VOLTAGE**

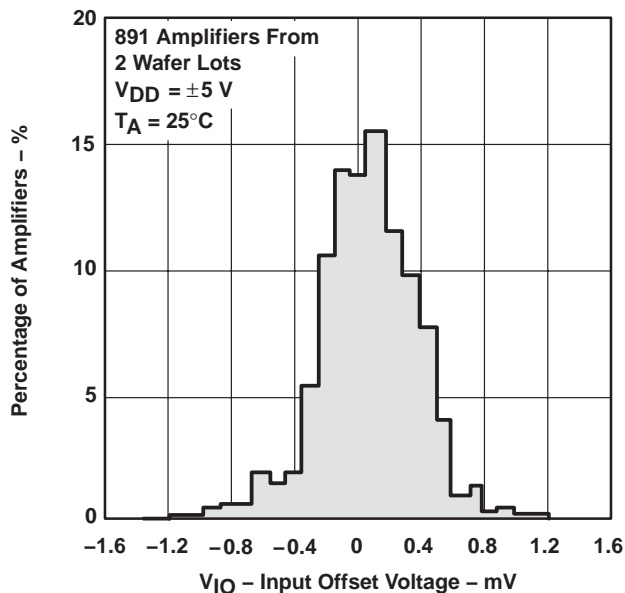


Figure 2

**DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE**

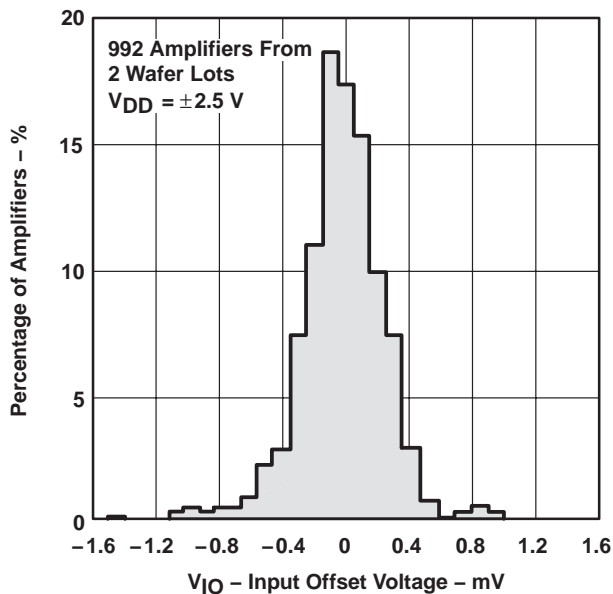


Figure 3

**DISTRIBUTION OF TLC2274
INPUT OFFSET VOLTAGE**

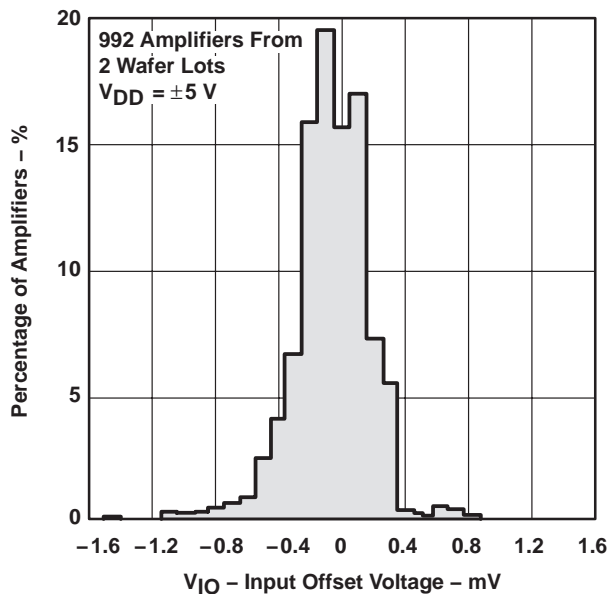


Figure 4

TYPICAL CHARACTERISTICS

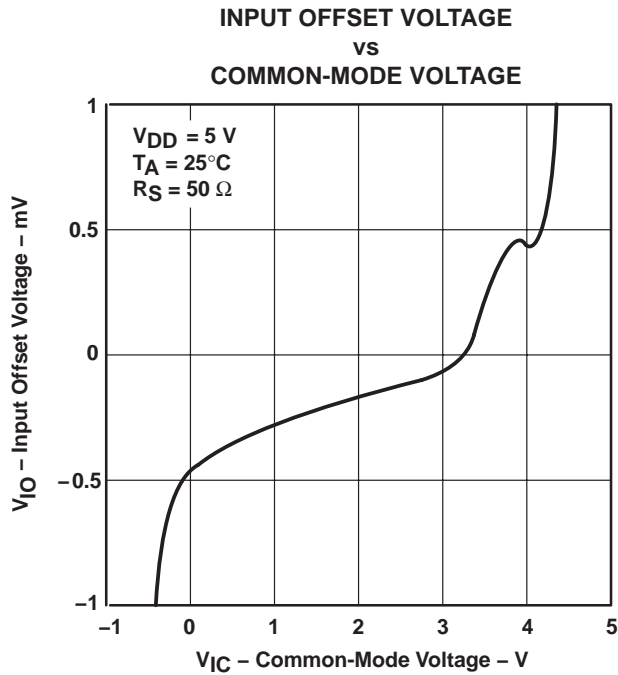


Figure 5

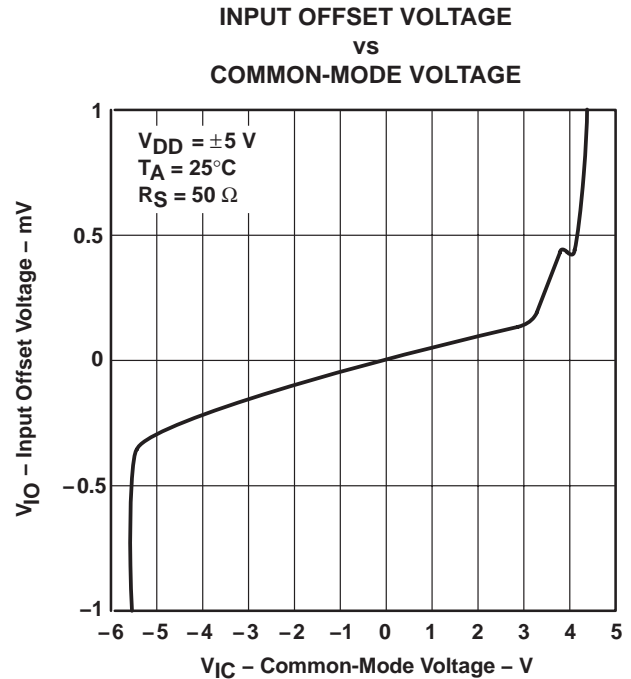


Figure 6

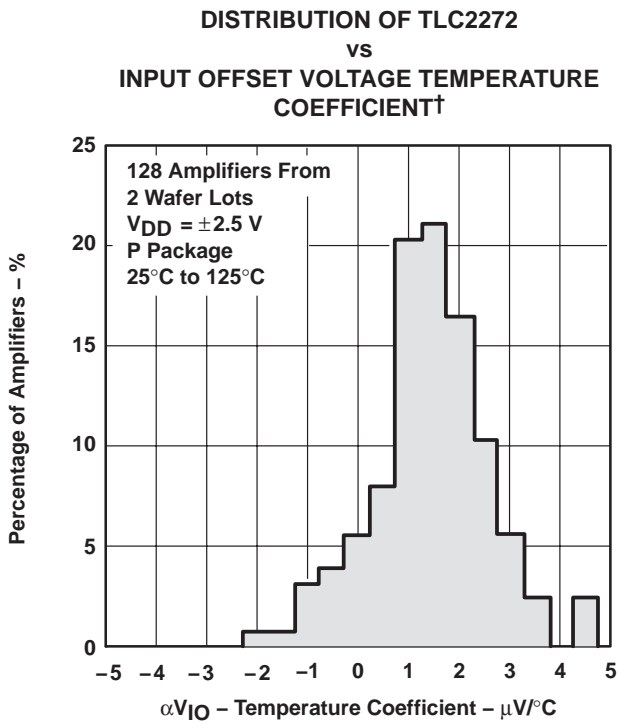


Figure 7

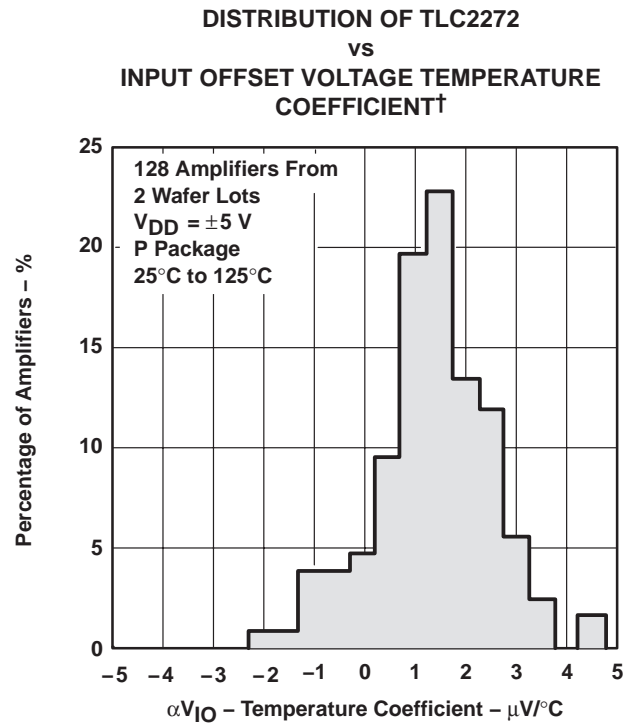


Figure 8

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

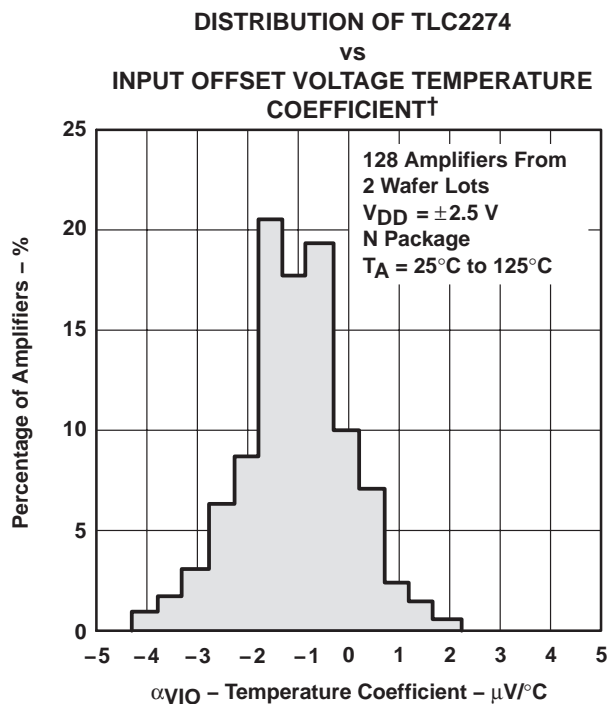


Figure 9

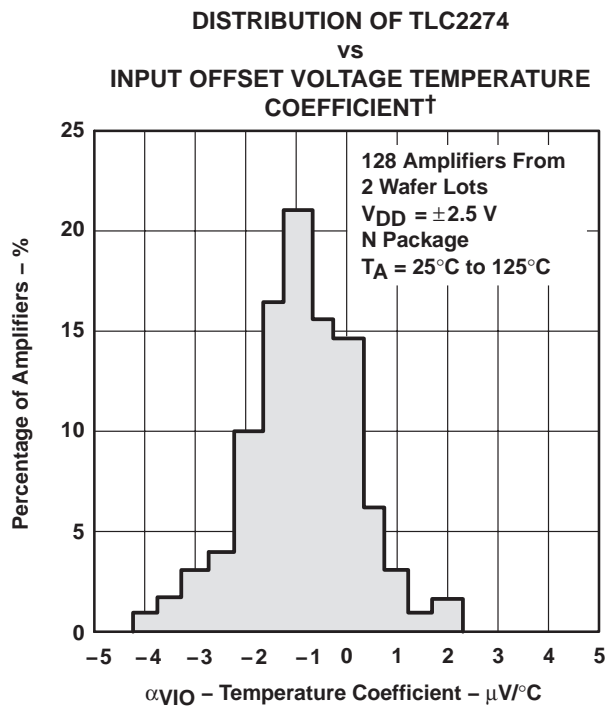


Figure 10

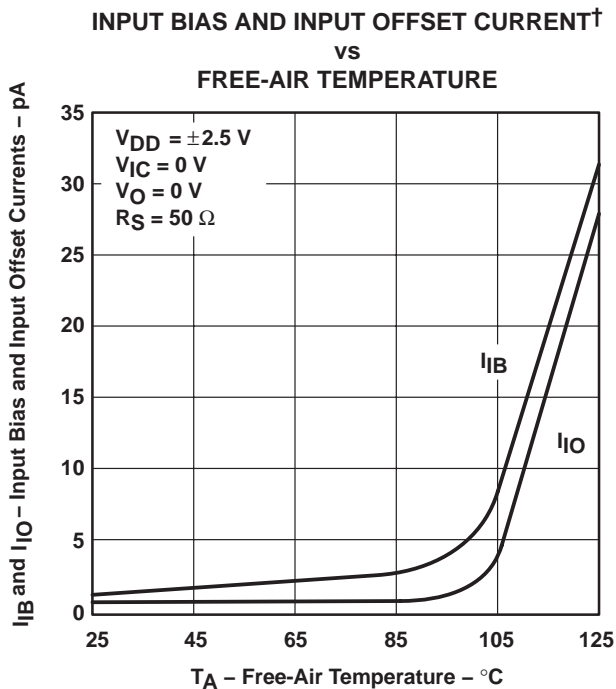


Figure 11

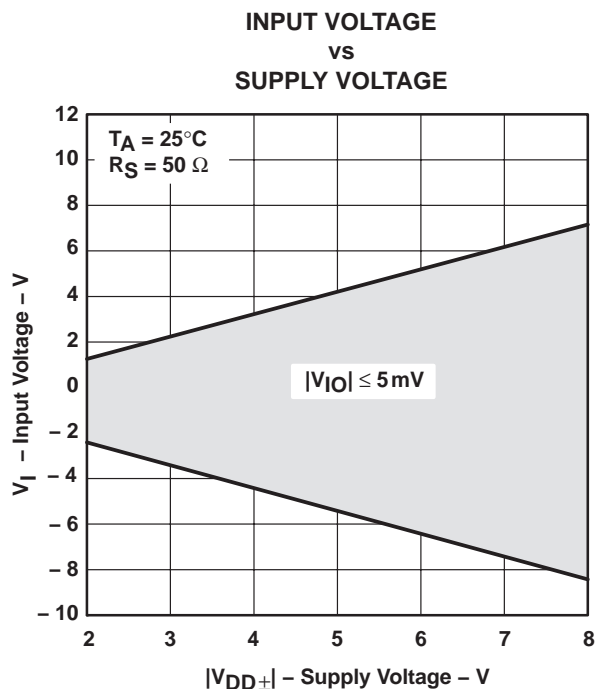


Figure 12

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

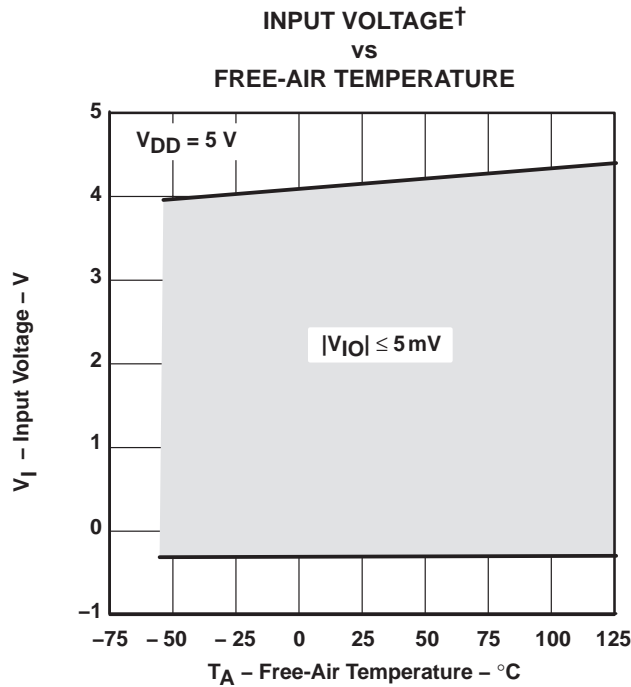


Figure 13

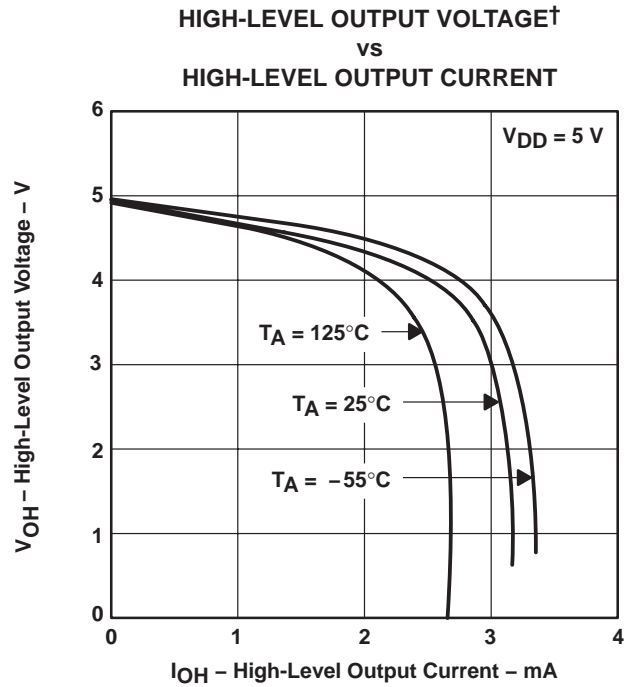


Figure 14

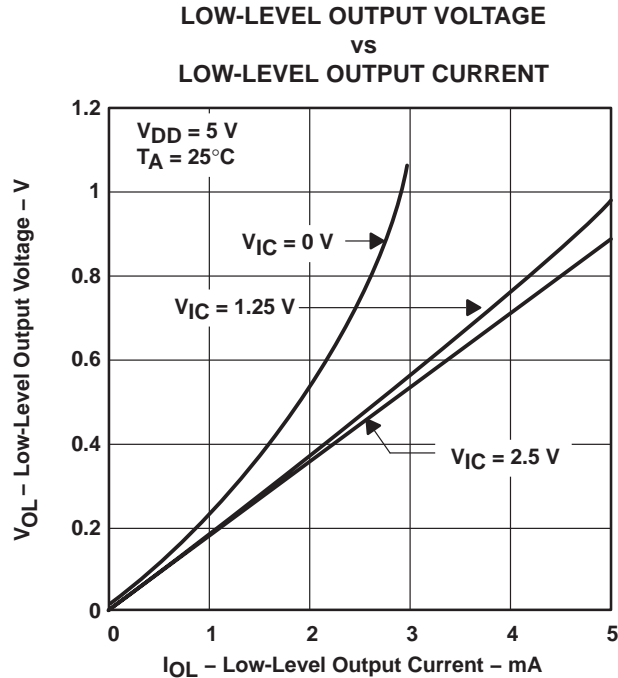


Figure 15

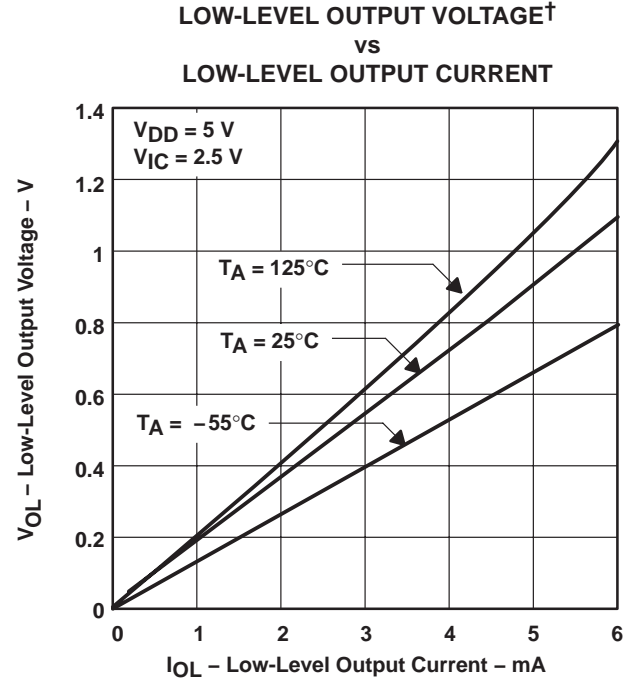


Figure 16

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

MAXIMUM POSITIVE PEAK OUTPUT VOLTAGE†
vs
OUTPUT CURRENT

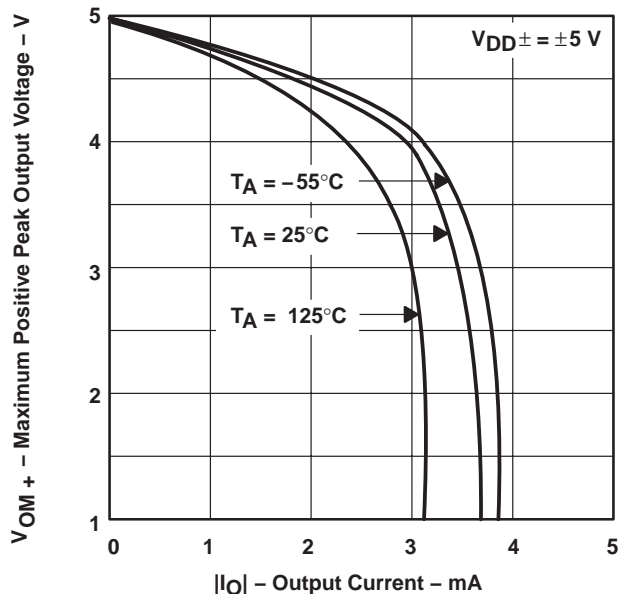


Figure 17

MAXIMUM NEGATIVE PEAK OUTPUT VOLTAGE†
vs
OUTPUT CURRENT

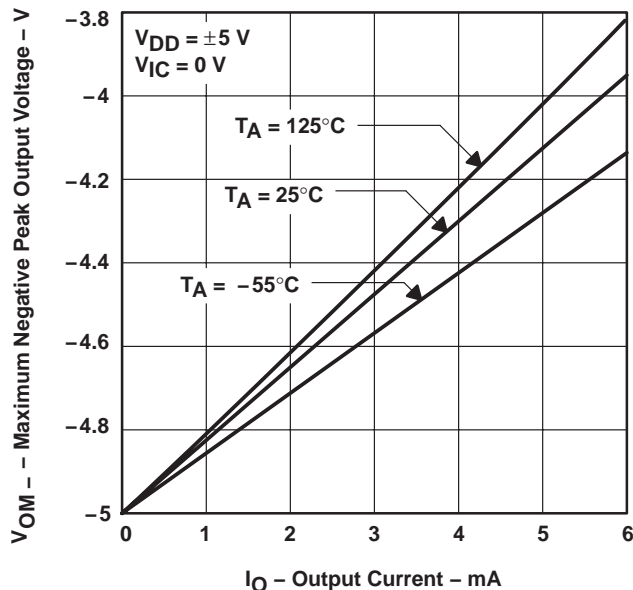


Figure 18

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE
vs
FREQUENCY

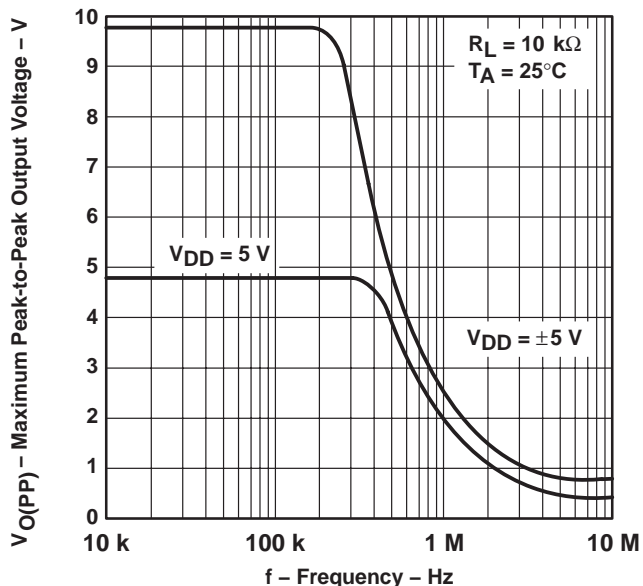


Figure 19

SHORT-CIRCUIT OUTPUT CURRENT
vs
SUPPLY VOLTAGE

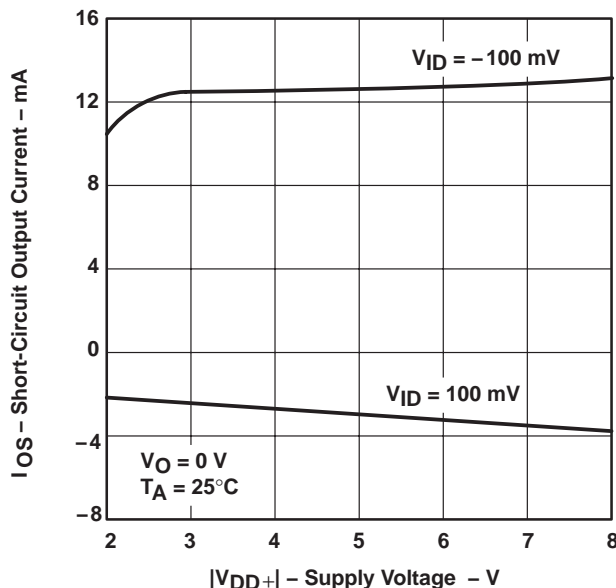


Figure 20

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

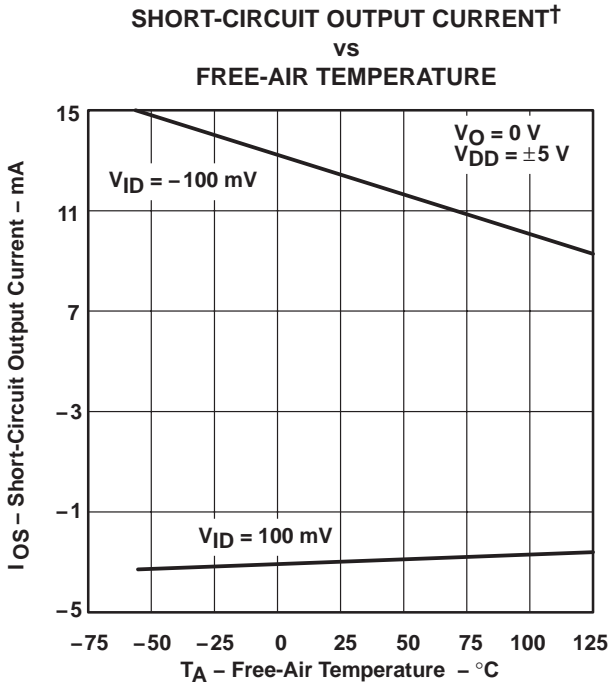


Figure 21

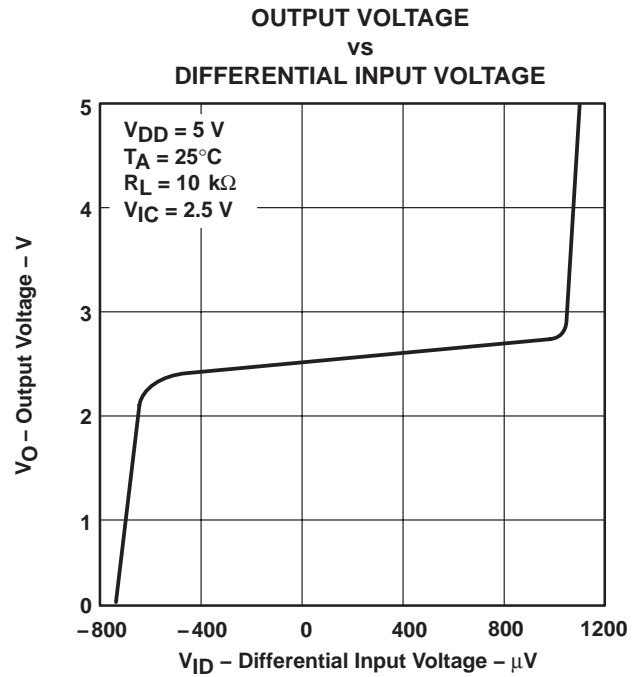


Figure 22

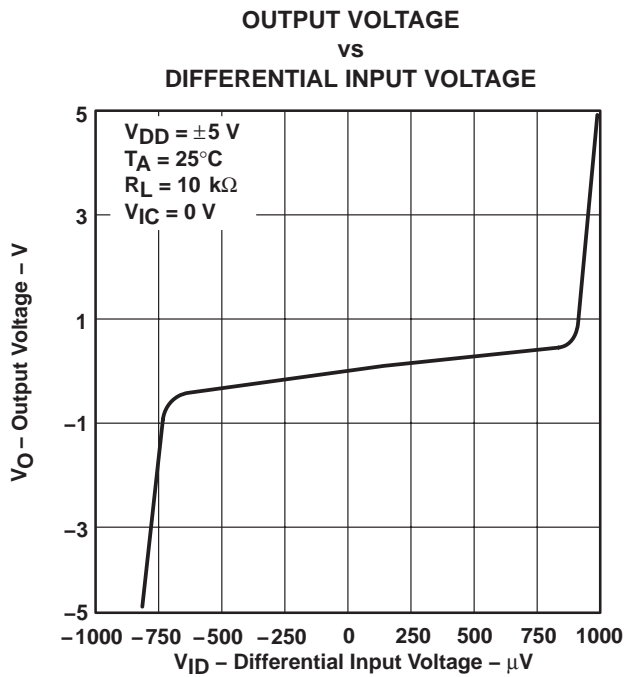


Figure 23

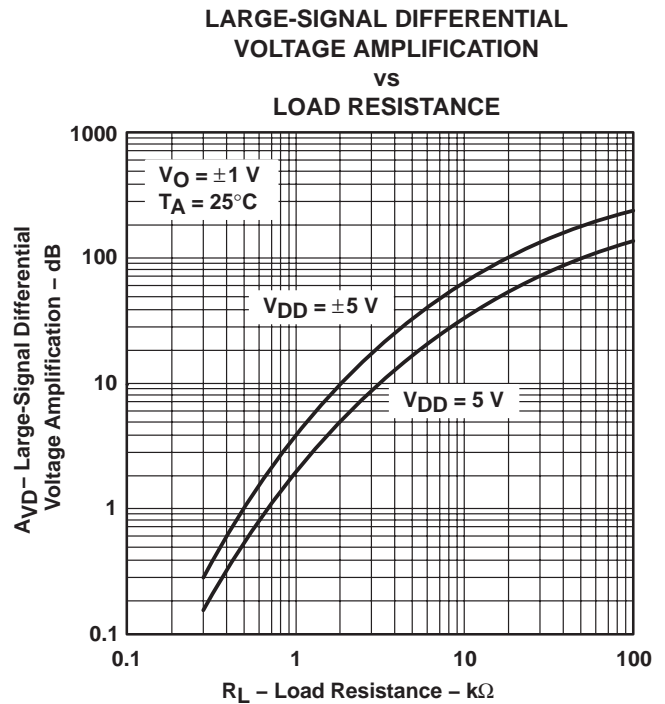


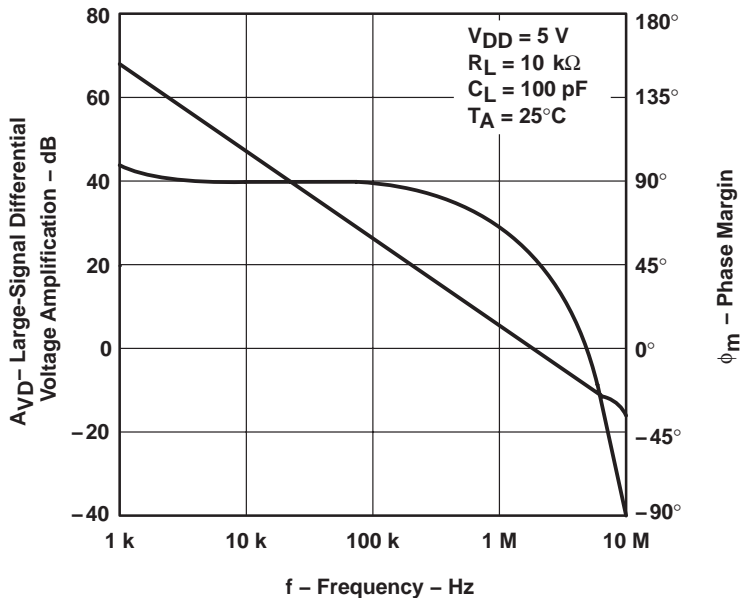
Figure 24

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

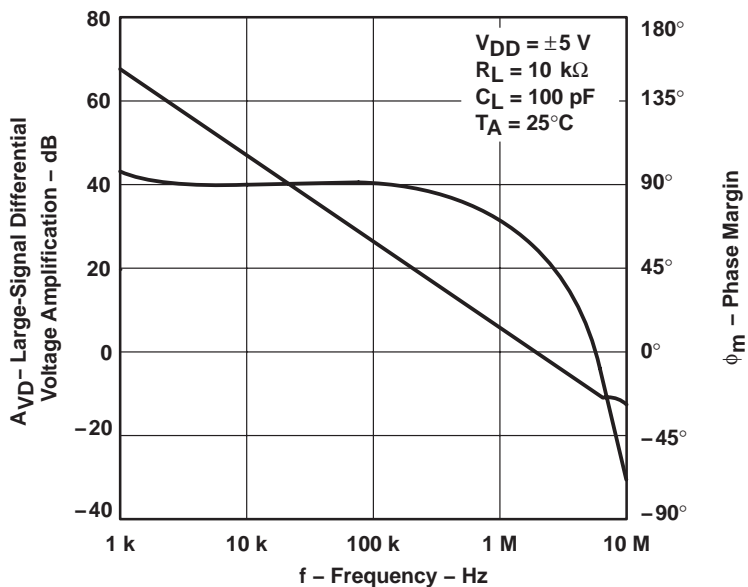
**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN**

**vs
FREQUENCY**



**LARGE-SIGNAL DIFFERENTIAL VOLTAGE
AMPLIFICATION AND PHASE MARGIN**

**vs
FREQUENCY**



TYPICAL CHARACTERISTICS

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

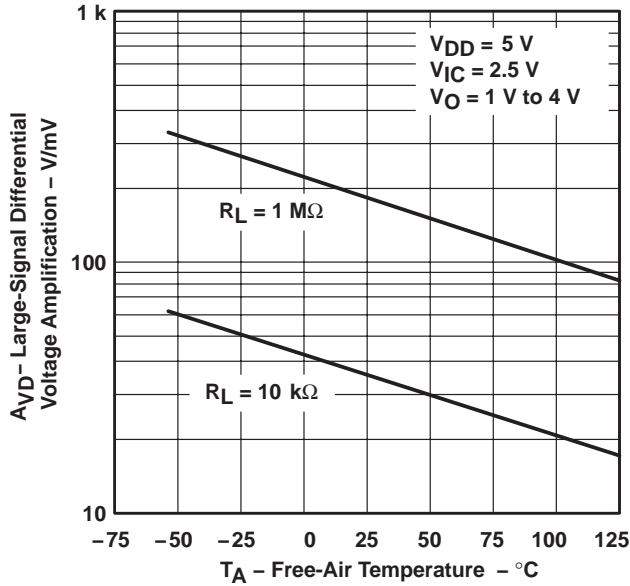


Figure 27

LARGE-SIGNAL DIFFERENTIAL
VOLTAGE AMPLIFICATION†
vs
FREE-AIR TEMPERATURE

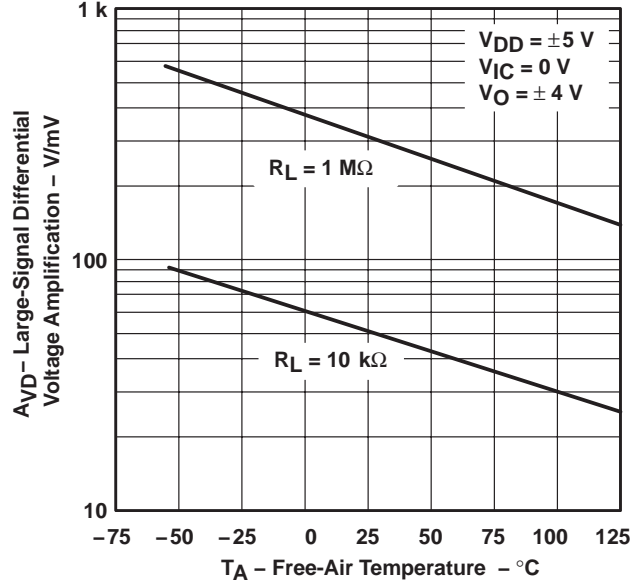


Figure 28

OUTPUT IMPEDANCE
vs
FREQUENCY

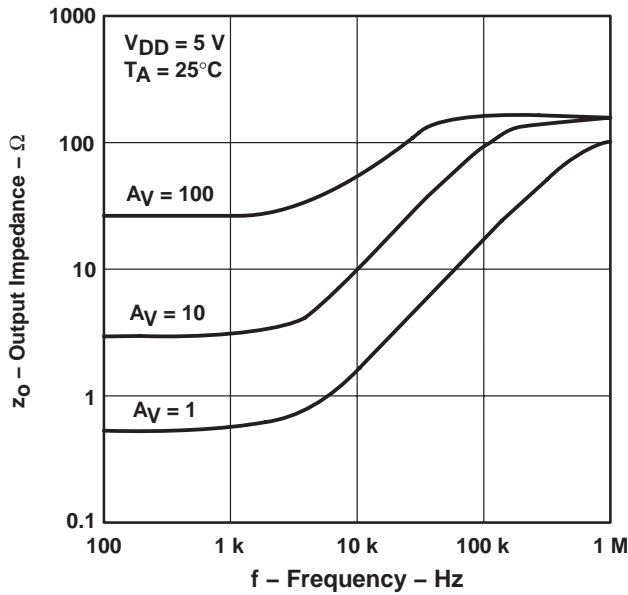


Figure 29

OUTPUT IMPEDANCE
vs
FREQUENCY

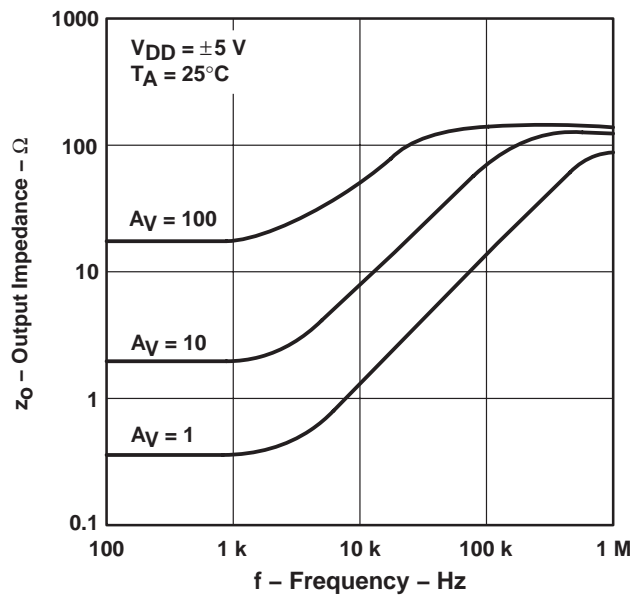


Figure 30

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

**COMMON-MODE REJECTION RATIO
vs
FREQUENCY**

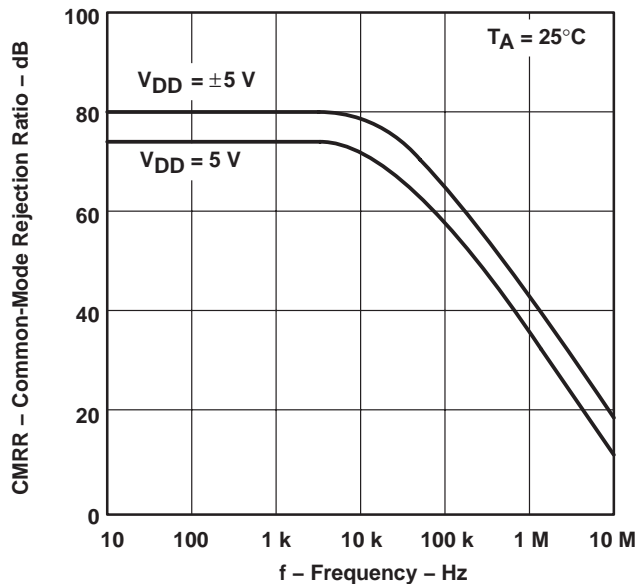


Figure 31

**COMMON-MODE REJECTION RATIO
vs
FREE-AIR TEMPERATURE**

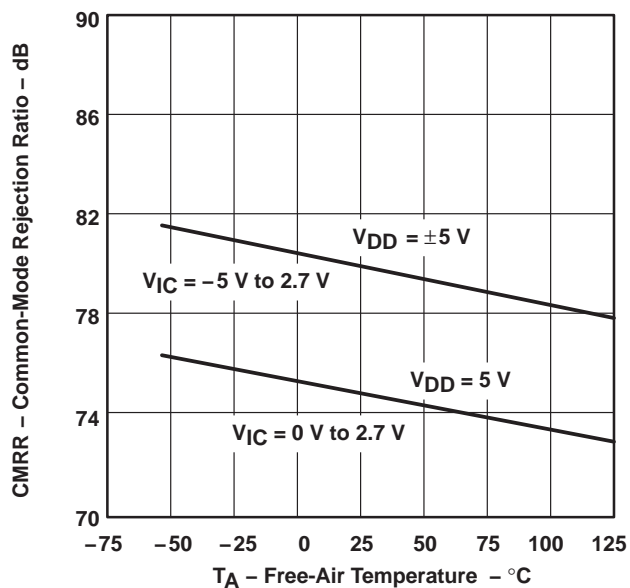


Figure 32

**SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY**

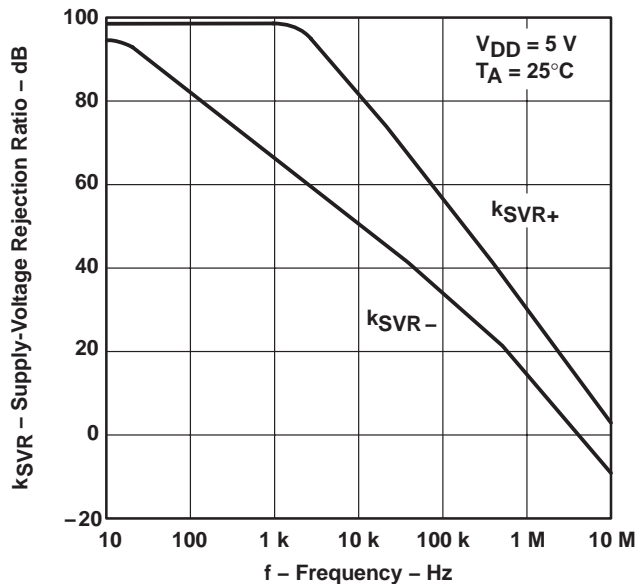


Figure 33

**SUPPLY-VOLTAGE REJECTION RATIO
vs
FREQUENCY**

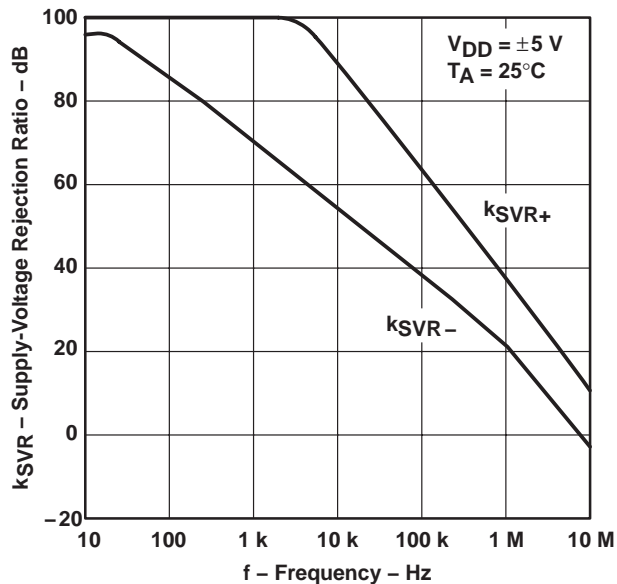
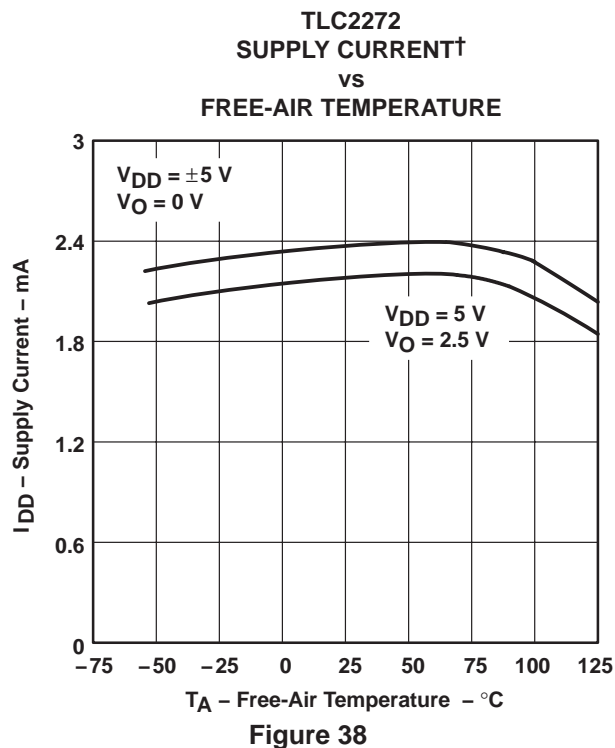
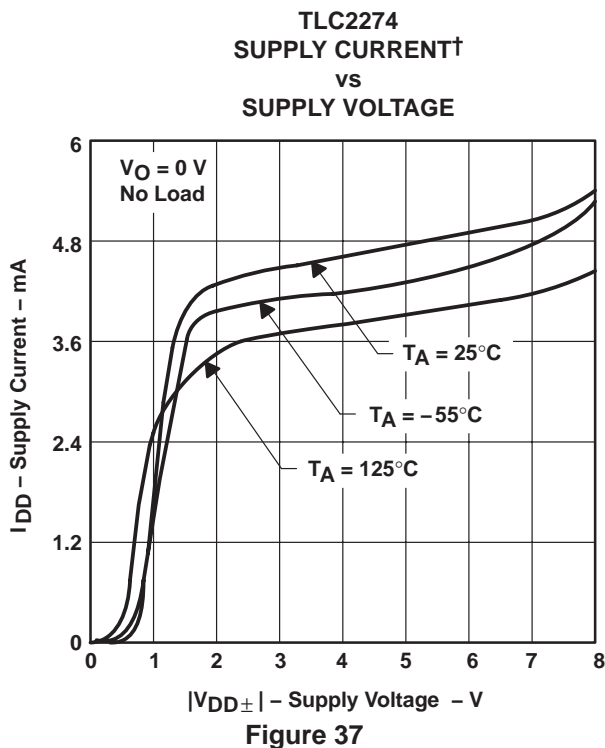
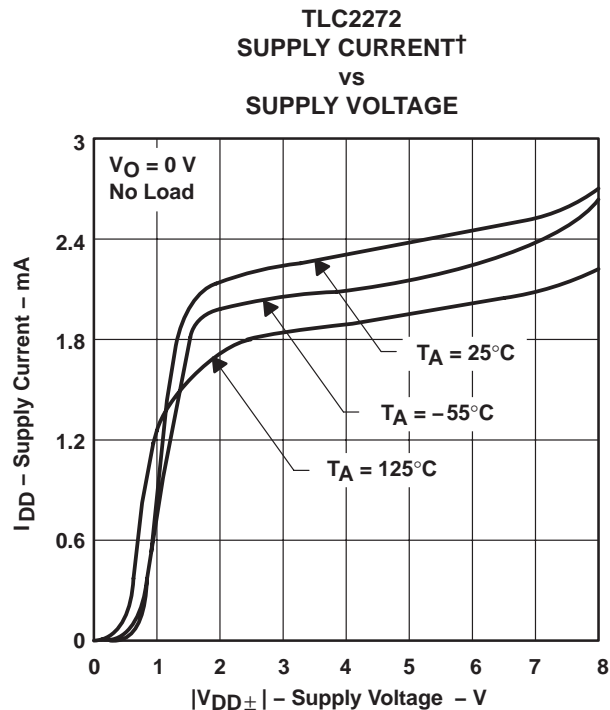
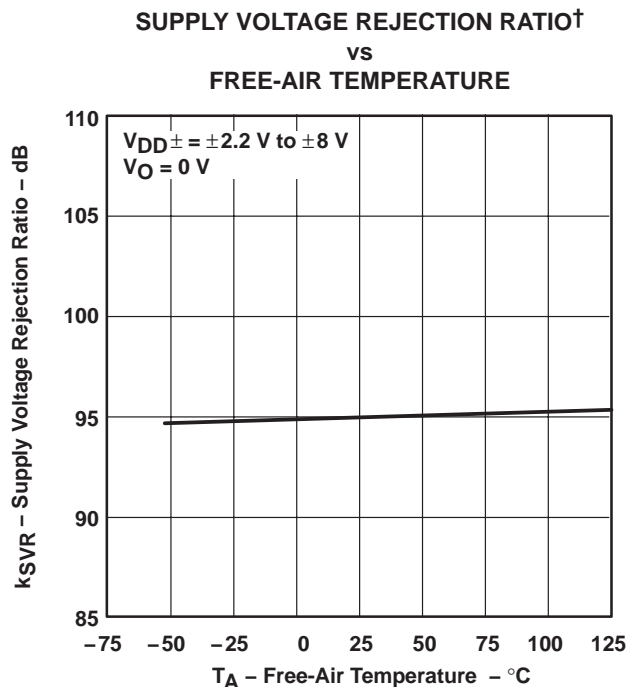


Figure 34

TYPICAL CHARACTERISTICS



† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

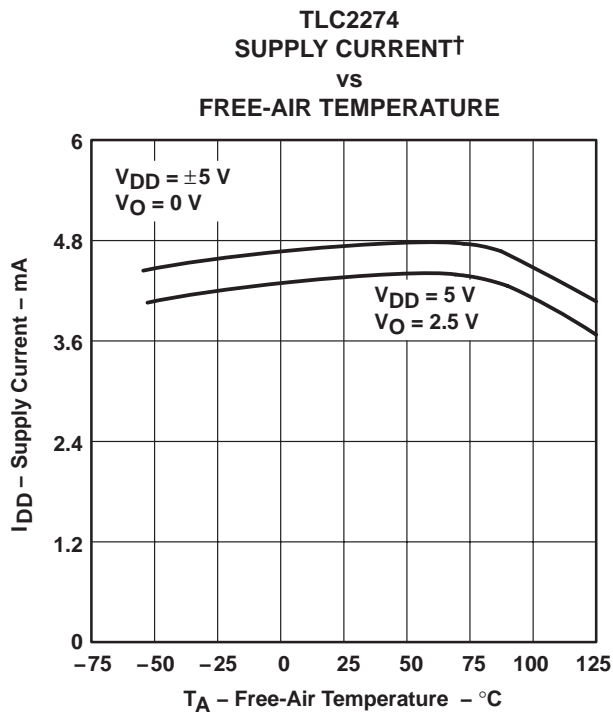


Figure 39

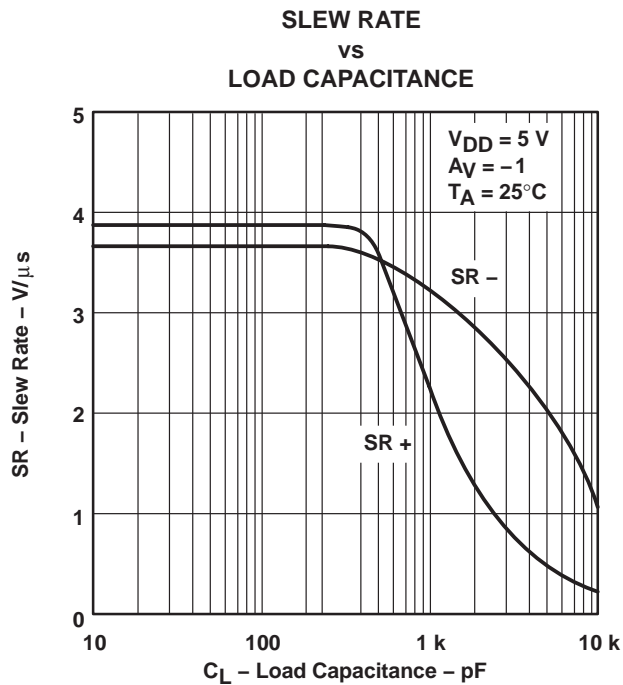


Figure 40

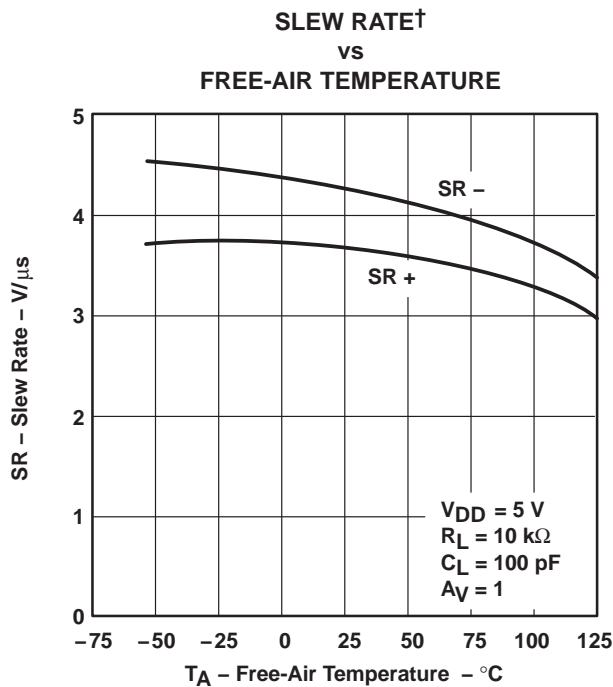


Figure 41

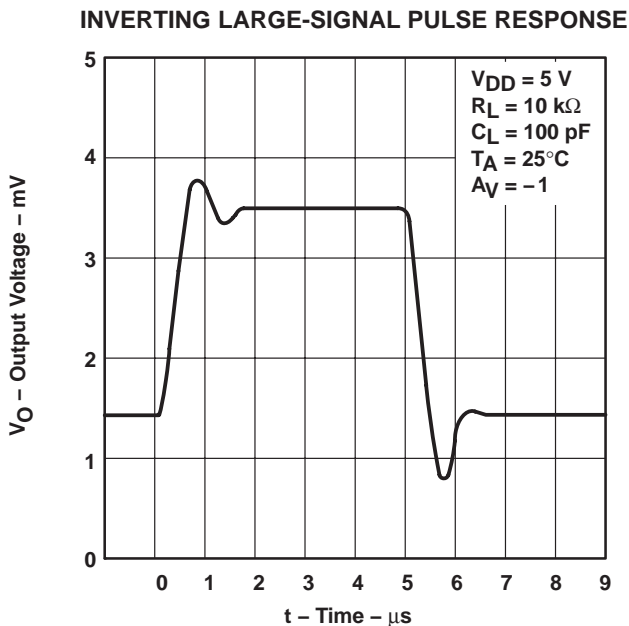


Figure 42

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

TYPICAL CHARACTERISTICS

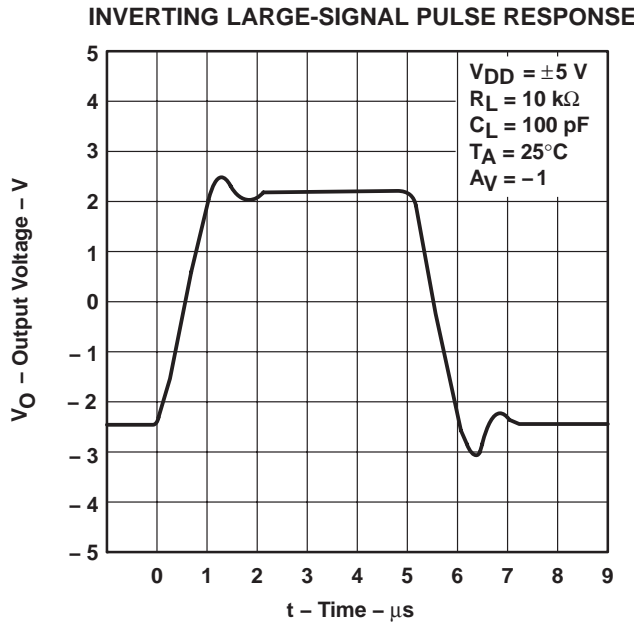


Figure 43

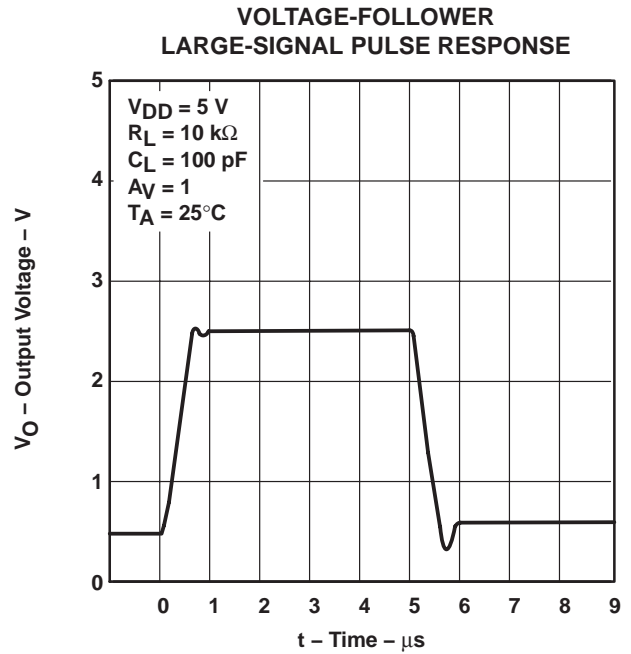


Figure 44

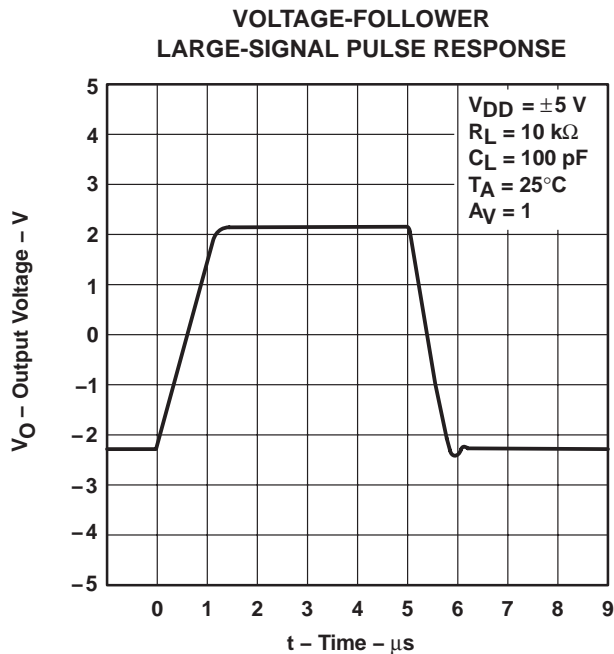


Figure 45

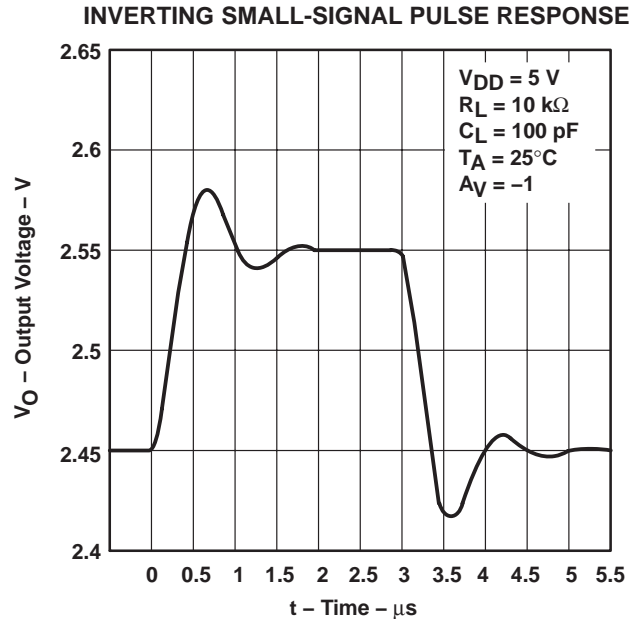


Figure 46

TYPICAL CHARACTERISTICS

INVERTING SMALL-SIGNAL PULSE RESPONSE

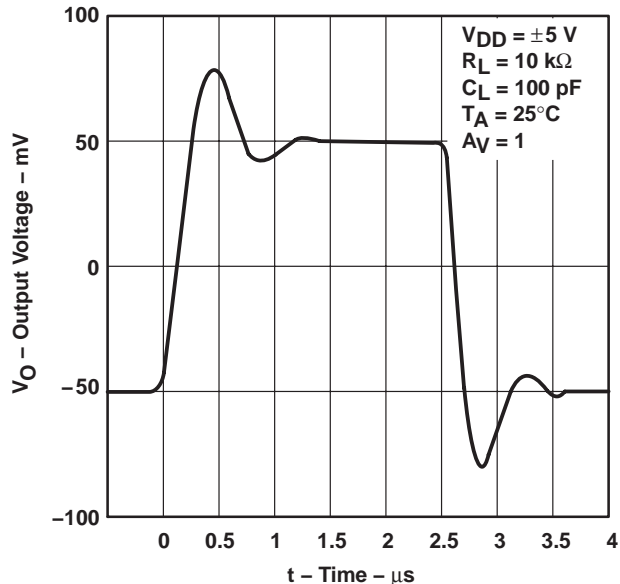


Figure 47

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

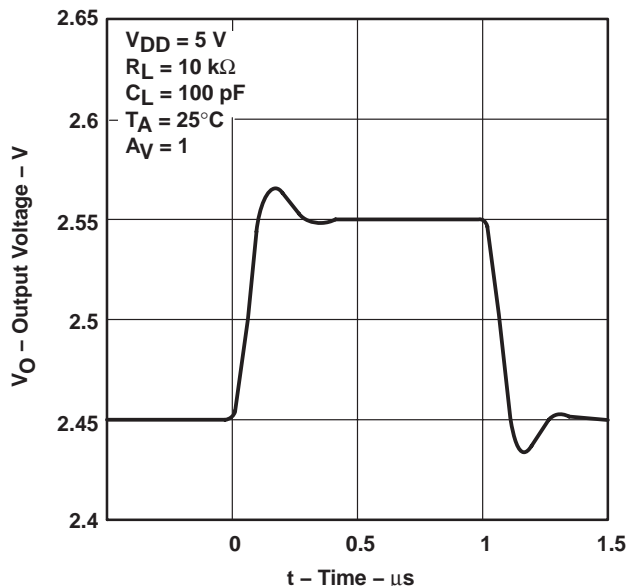


Figure 48

VOLTAGE-FOLLOWER SMALL-SIGNAL PULSE RESPONSE

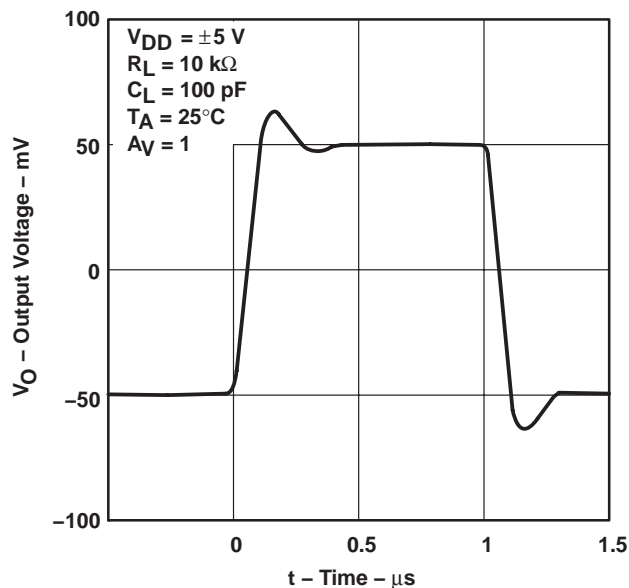


Figure 49

EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

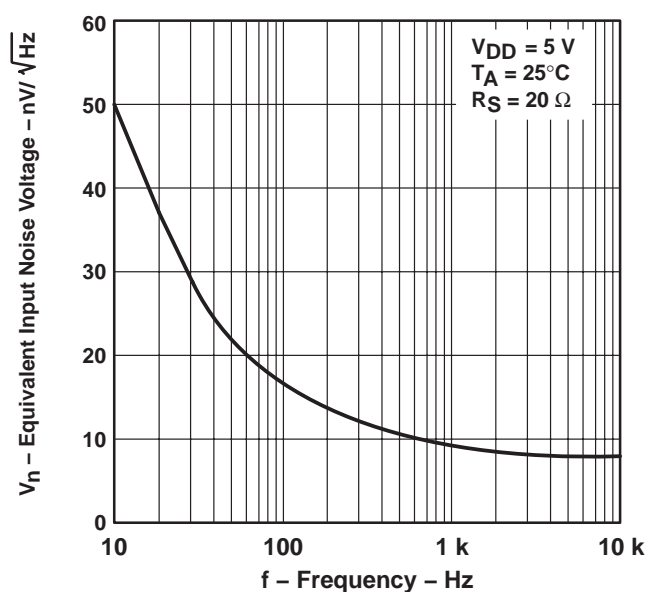


Figure 50

TYPICAL CHARACTERISTICS

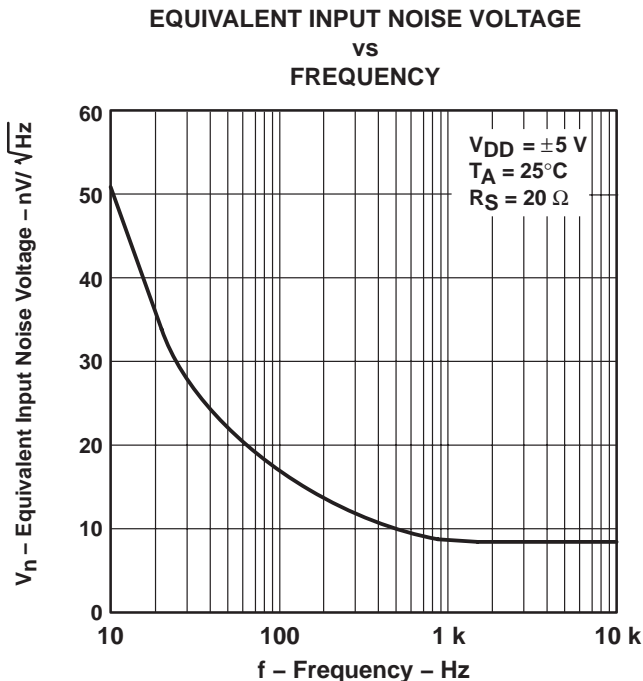


Figure 51

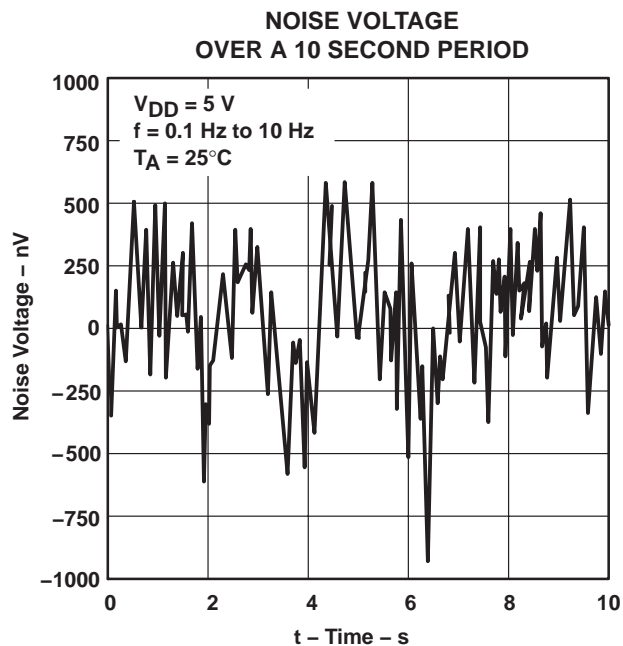


Figure 52

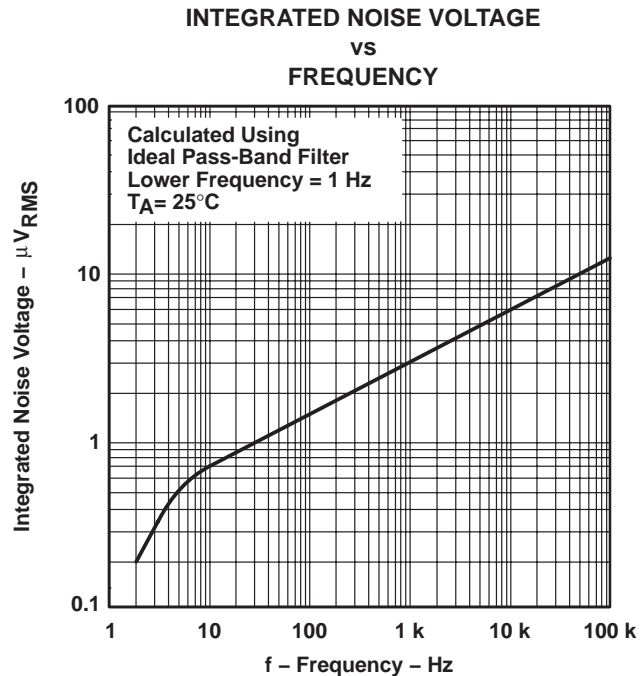


Figure 53

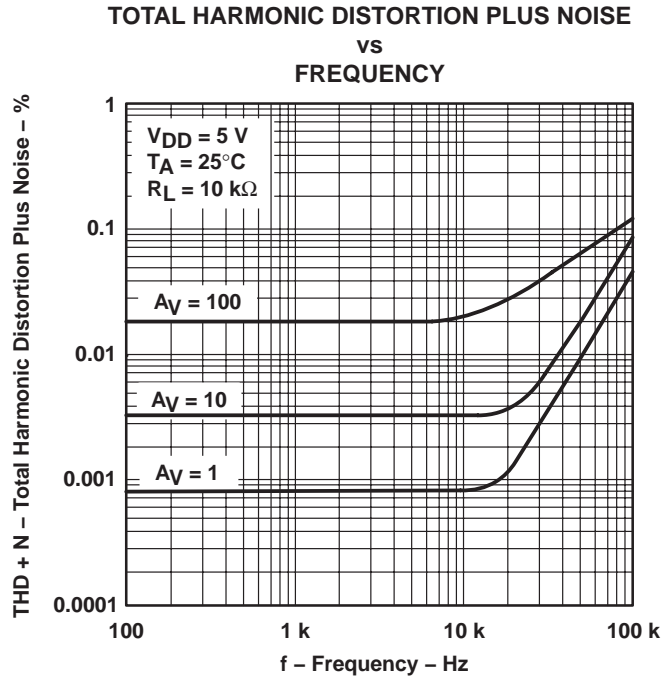


Figure 54

TYPICAL CHARACTERISTICS

GAIN-BANDWIDTH PRODUCT
vs
SUPPLY VOLTAGE

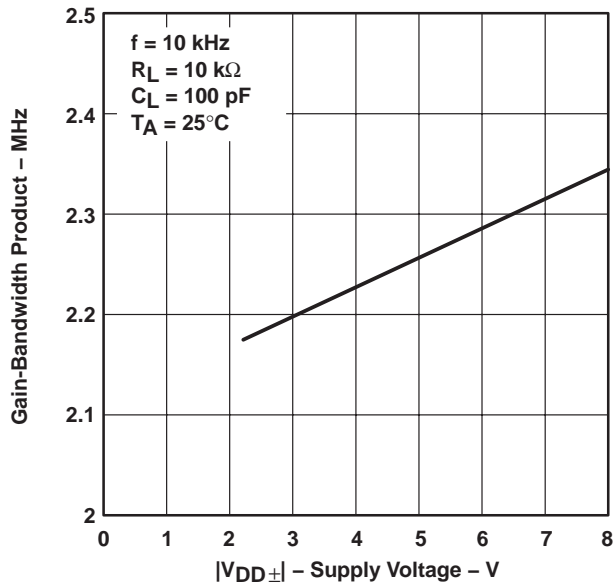


Figure 55

GAIN-BANDWIDTH PRODUCT†
vs
FREE-AIR TEMPERATURE

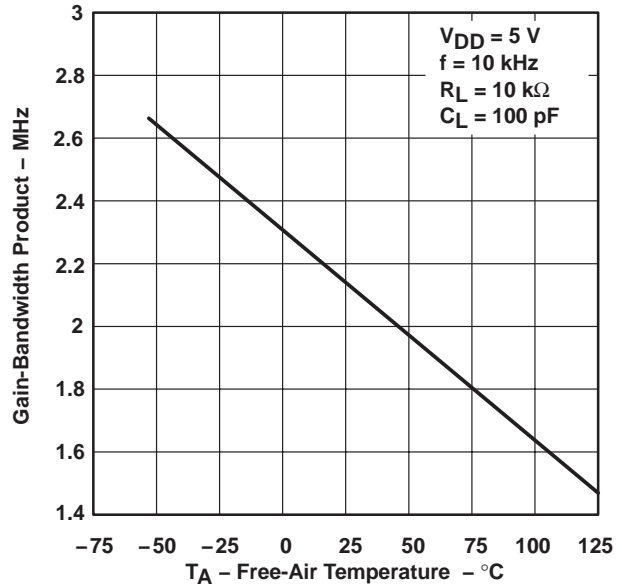


Figure 56

PHASE MARGIN
vs
LOAD CAPACITANCE

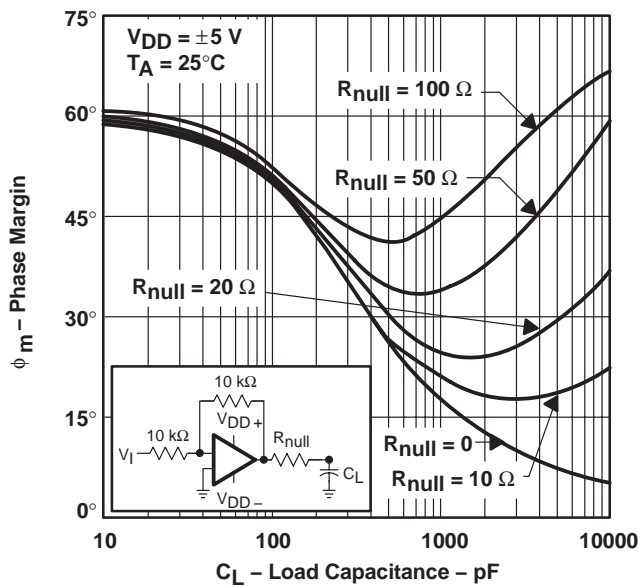


Figure 57

GAIN MARGIN
vs
LOAD CAPACITANCE

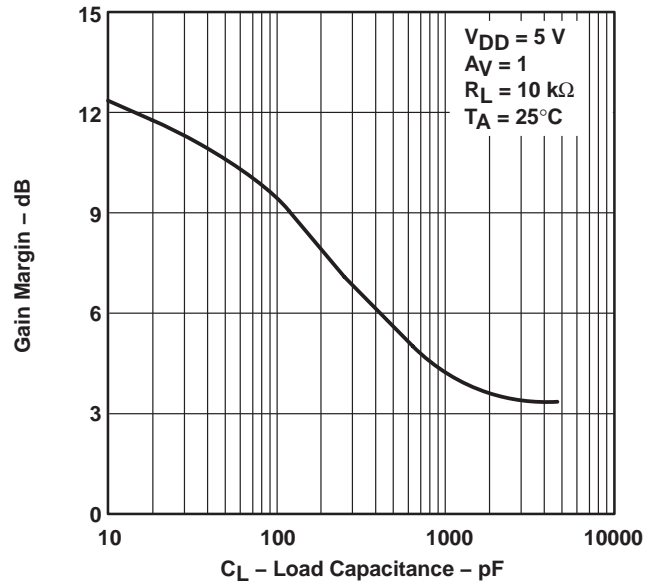


Figure 58

† Data at high and low temperatures are applicable only within the rated operating free-air temperature ranges of the various devices.

APPLICATION INFORMATION

macromodel information

Macromodel information provided was derived using Microsim *Parts*™, the model generation software used with Microsim *PSpice*™. The Boyle macromodel (see Note 6) and subcircuit in Figure 59 were generated using the TLC227x typical electrical and operating characteristics at $T_A = 25^\circ\text{C}$. Using this information, output simulations of the following key parameters can be generated to a tolerance of 20% (in most cases):

- Maximum positive output voltage swing
- Maximum negative output voltage swing
- Slew rate
- Quiescent power dissipation
- Input bias current
- Open-loop voltage amplification
- Unity gain frequency
- Common-mode rejection ratio
- Phase margin
- DC output resistance
- AC output resistance
- Short-circuit output current limit

NOTE 6: G. R. Boyle, B. M. Cohn, D. O. Pederson, and J. E. Solomon, "Macromodeling of Integrated Circuit Operational Amplifiers", *IEEE Journal of Solid-State Circuits*, SC-9, 353 (1974).

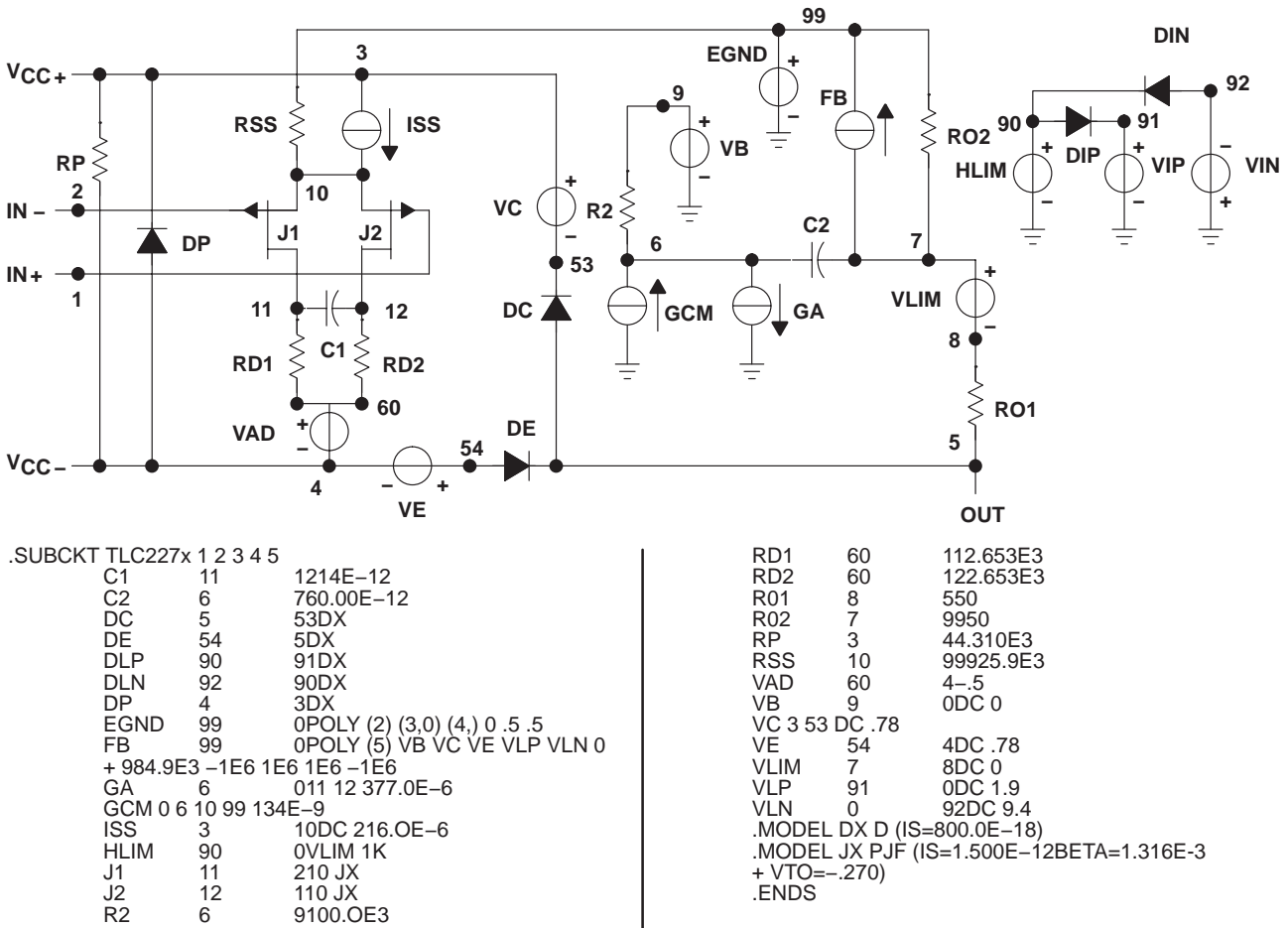


Figure 59. Boyle Macromodel and Subcircuit

PSpice and *Parts* are trademarks of MicroSim Corporation.

Macromodels, simulation models, or other models provided by TI, directly or indirectly, are not warranted by TI as fully representing all of the specification and operating characteristics of the semiconductor product to which the model relates.



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC2272AMDREP	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE	Samples
TLC2272AMDREPG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE	Samples
TLC2274AMDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME	Samples
TLC2274AMPWREP	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME	Samples
TLC2274MDREP	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274ME	Samples
V62/03618-01XE	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2272AE	Samples
V62/03618-02UE	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME	Samples
V62/03618-02YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274AME	Samples
V62/03618-04YE	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	2274ME	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

- (3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

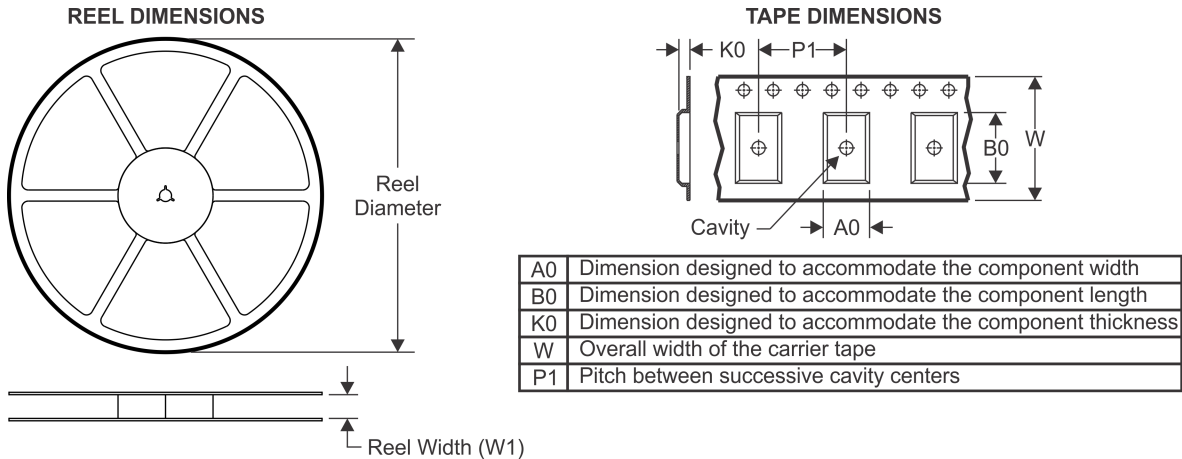
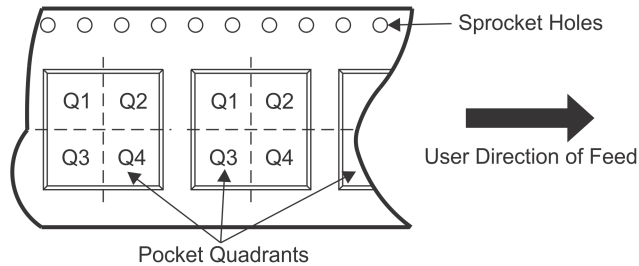
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLC2272A-EP, TLC2274-EP, TLC2274A-EP :

- Catalog: [TLC2272A](#), [TLC2274](#), [TLC2274A](#)
- Automotive: [TLC2272A-Q1](#), [TLC2274-Q1](#), [TLC2274A-Q1](#)
- Military: [TLC2272AM](#), [TLC2274M](#), [TLC2274AM](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC2272AMDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLC2274AMDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC2274AMPWREP	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLC2274MDREP	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC2272AMDREP	SOIC	D	8	2500	350.0	350.0	43.0
TLC2274AMDREP	SOIC	D	14	2500	333.2	345.9	28.6
TLC2274AMPWREP	TSSOP	PW	14	2000	367.0	367.0	35.0
TLC2274AMDREP	SOIC	D	14	2500	333.2	345.9	28.6

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

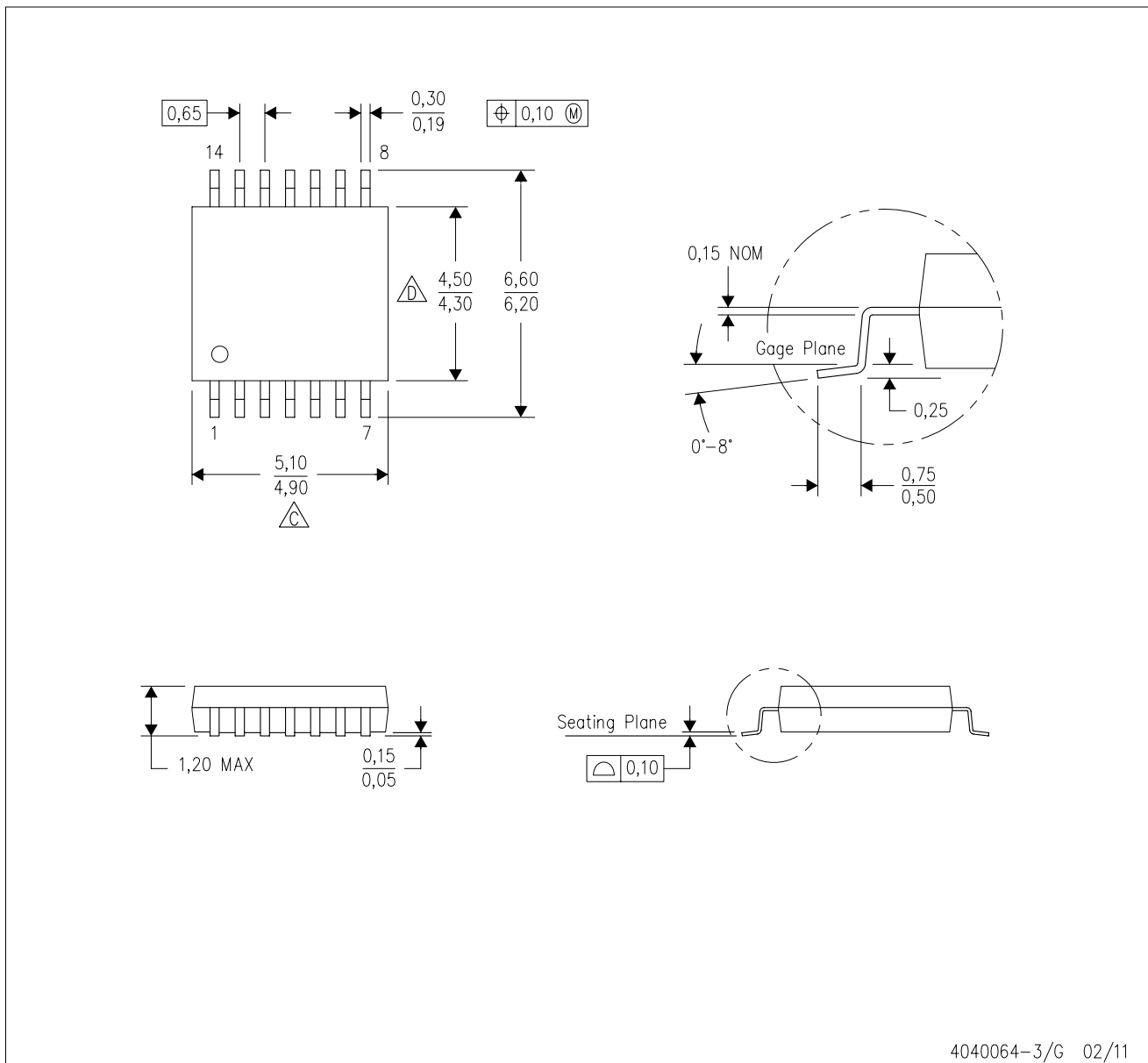


4211283-3/E 08/12



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View TLC2274AMPWREP on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management