

DS42BR400 Quad 4.25 Gbps CML Transceiver with Transmit De-Emphasis and Receive Equalization

Check for Samples: [DS42BR400](#)

FEATURES

- 250 Mbps – 4.25 Gbps Fully Differential Data Paths
- Optional Fixed Input Equalization
- Selectable Output De-emphasis
- Individual Loopback Controls
- On-Chip Termination
- Lead-less WQFN-60 Pin Package (9 mm x 9 mm x 0.8 mm, 0.5 mm Pitch)
- –40°C to +85°C Industrial Temperature Range
- 6 kV ESD Rating, HBM

APPLICATIONS

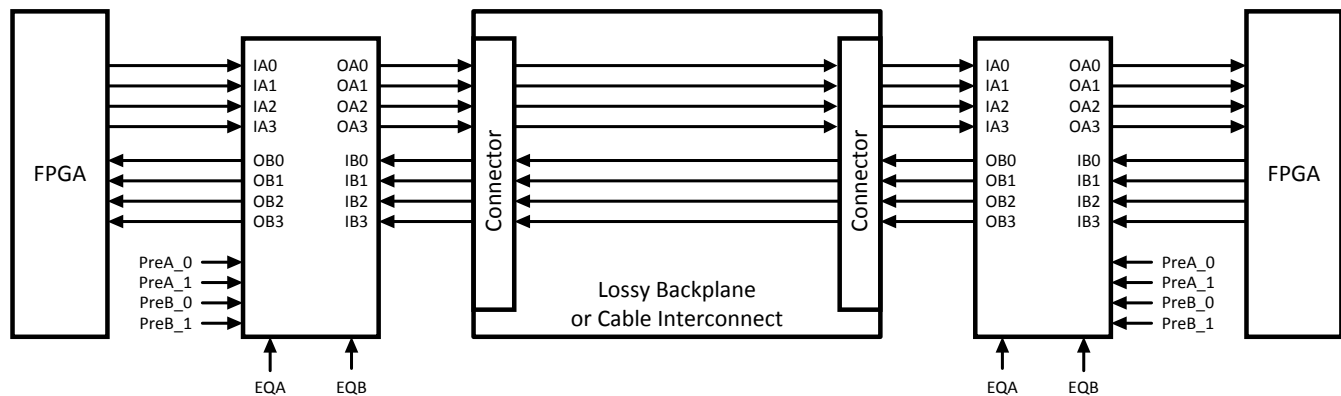
- Backplane Driver or Cable Driver
- Signal Repeating, Buffering and Conditioning Applications

DESCRIPTION

The DS42BR400 is a quad 250 Mbps – 4.25 Gbps CML transceiver, or 8-channel buffer, for use in backplane and cable applications. With operation down to 250 Mbps, the DS42BR400 can be used in applications requiring both low and high frequency data rates. Each input stage has a fixed equalizer to reduce ISI distortion from board traces. The equalizers are grouped in fours and are enabled through two control pins. These control pins provide customers flexibility where ISI distortion may vary from one direction to another.

All output drivers have four selectable steps of de-emphasis to compensate against transmission loss across long FR4 backplanes. The de-emphasis blocks are also grouped in fours. In addition, the DS42BR400 also has loopback control capability on four channels. All CML drivers have 50Ω termination to V_{CC} . All receivers are internally terminated with differential 100Ω.

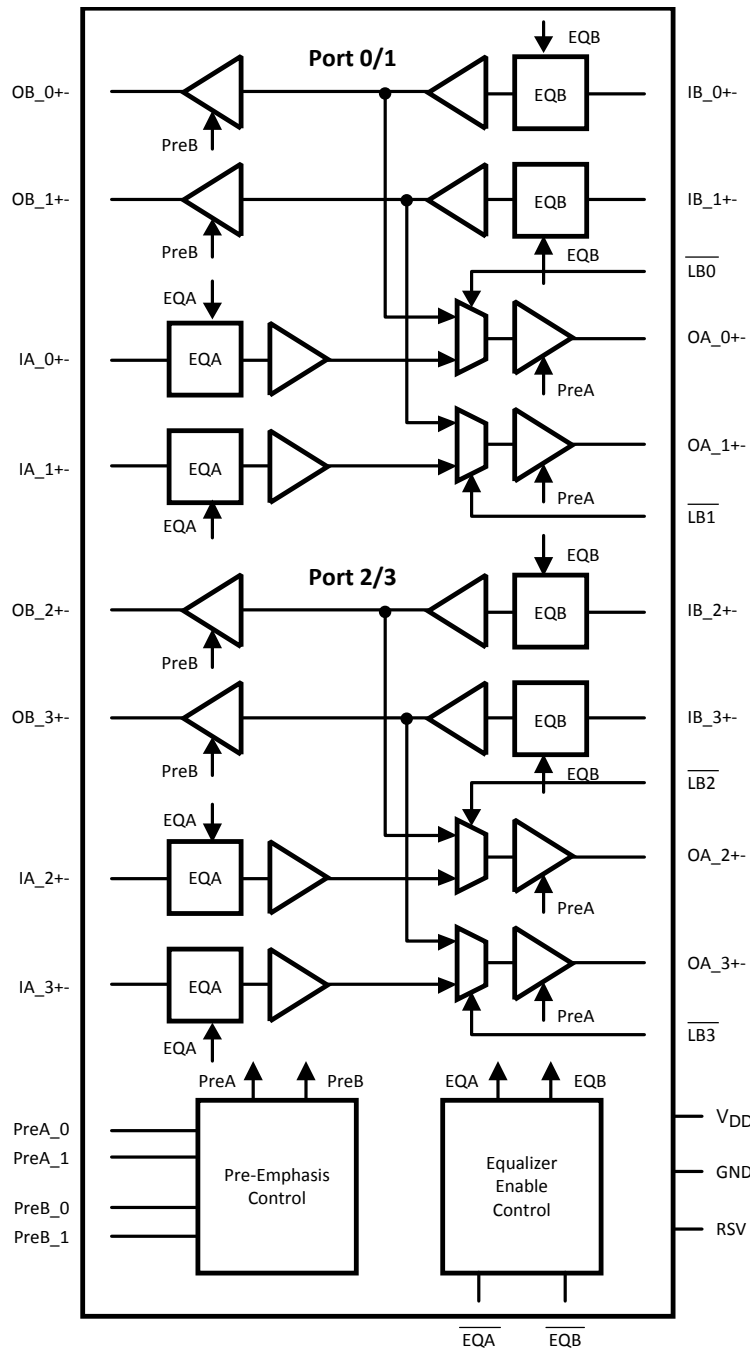
Simplified Application Diagram



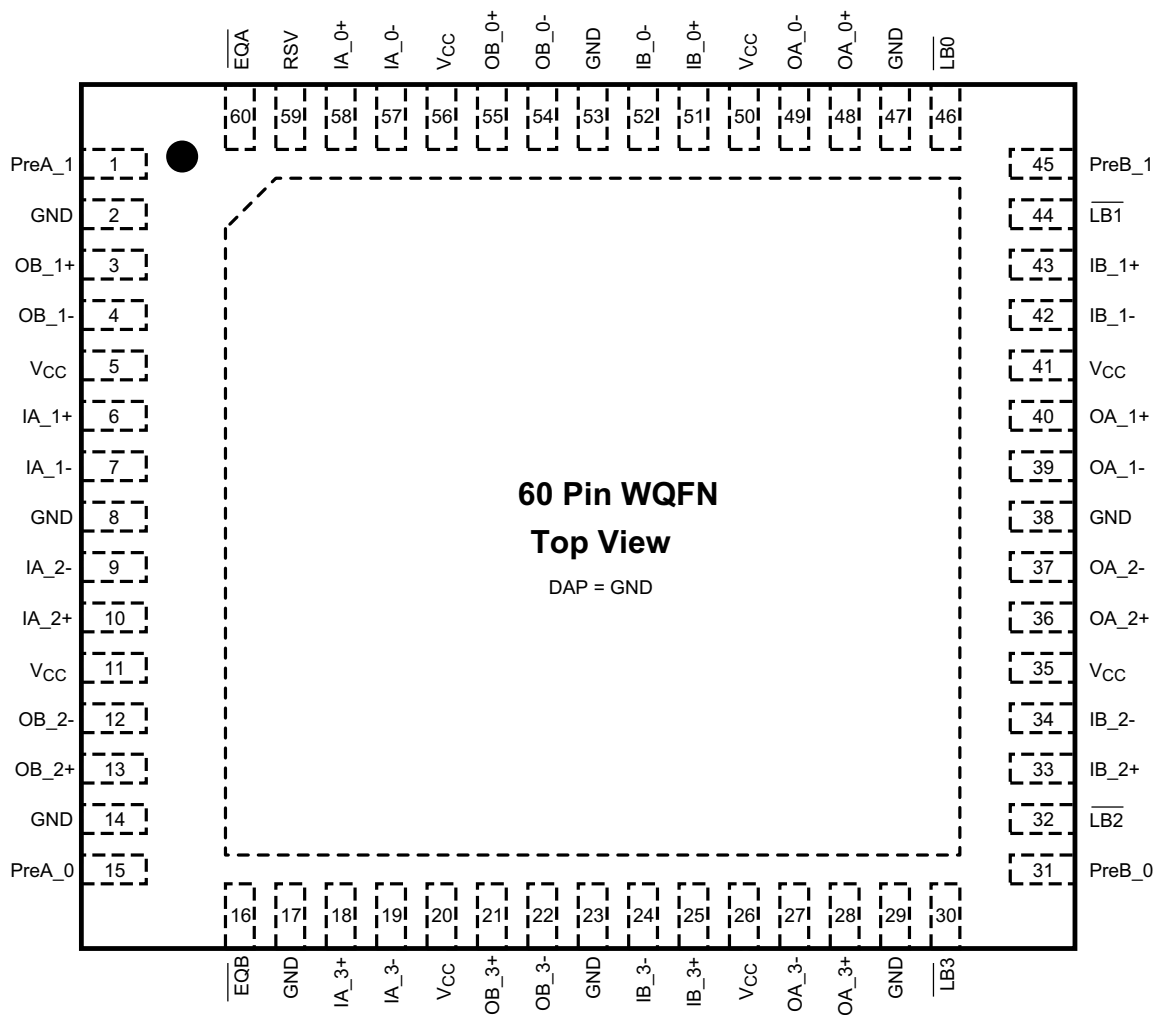
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Functional Block Diagram



Connection Diagram



**Figure 1. Leadless WQFN-60 Pin Package
(9 mm x 9 mm x 0.8 mm, 0.5 mm pitch)
See Package Number NKA0060A**

PIN DESCRIPTIONS

Pin Name	Pin Number	I/O ⁽¹⁾	Description
DIFFERENTIAL I/O			
IB_0+ IB_0–	51 52	I	Inverting and non-inverting differential inputs of port_0. IB_0+ and IB_0– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OA_0+ OA_0–	48 49	O	Inverting and non-inverting differential outputs of port_0. OA_0+ and OA_0– are connected to V _{CC} through a 50Ω resistor.
IB_1+ IB_1–	43 42	I	Inverting and non-inverting differential inputs of port_1. IB_1+ and IB_1– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OA_1+ OA_1–	40 39	O	Inverting and non-inverting differential outputs of port_1. OA_1+ and OA_1– are connected to V _{CC} through a 50Ω resistor.
IB_2+ IB_2–	33 34	I	Inverting and non-inverting differential inputs of port_2. IB_2+ and IB_2– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OA_2+ OA_2–	36 37	O	Inverting and non-inverting differential outputs of port_2. OA_2+ and OA_2– are connected to V _{CC} through a 50Ω resistor.
IB_3+ IB_3–	25 24	I	Inverting and non-inverting differential inputs of port_3. IB_3+ and IB_3– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OA_3+ OA_3–	28 27	O	Inverting and non-inverting differential outputs of port_3. OA_3+ and OA_3– are connected to V _{CC} through a 50Ω resistor.
IA_0+ IA_0–	58 57	I	Inverting and non-inverting differential inputs of port_0. IA_0+ and IA_0– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OB_0+ OB_0–	55 54	O	Inverting and non-inverting differential outputs of port_0. OB_0+ and OB_0– are connected to V _{CC} through a 50Ω resistor.
IA_1+ IA_1–	6 7	I	Inverting and non-inverting differential inputs of port_1. IA_1+ and IA_1– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OB_1+ OB_1–	3 4	O	Inverting and non-inverting differential outputs of port_1. OB_1+ and OB_1– are connected to V _{CC} through a 50Ω resistor.
IA_2+ IA_2–	10 9	I	Inverting and non-inverting differential inputs of port_2. IA_2+ and IA_2– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OB_2+ OB_2–	13 12	O	Inverting and non-inverting differential outputs of port_2. OB_2+ and OB_2– are connected to V _{CC} through a 50Ω resistor.
IA_3+ IA_3–	18 19	I	Inverting and non-inverting differential inputs of port_3. IA_3+ and IA_3– are internally connected to a reference voltage through a 50Ω resistor. Refer to Figure 8 .
OB_3+ OB_3–	21 22	O	Inverting and non-inverting differential outputs of port_3. OB_3+ and OB_3– are connected to V _{CC} through a 50Ω resistor.
CONTROL (3.3V LVCMOS)			
$\overline{\text{EQA}}$	60	I	This pin is active LOW. A logic LOW at $\overline{\text{EQA}}$ enables equalization for input channels IA_0±, IA_1±, IA_2±, and IA_3±. By default, this pin is internally pulled high and equalization is disabled.
$\overline{\text{EQB}}$	16	I	This pin is active LOW. A logic LOW at $\overline{\text{EQB}}$ enables equalization for input channels IB_0±, IB_1±, IB_2±, and IB_3±. By default, this pin is internally pulled high and equalization is disabled.
PreA_0 PreA_1	15 1	I	PreA_0 and PreA_1 select the output de-emphasis levels (OA_0±, OA_1±, OA_2±, and OA_3±). PreA_0 and PreA_1 are internally pulled high. Please see Table 2 for de-emphasis levels.
PreB_0 PreB_1	31 45	I	PreB_0 and PreB_1 select the output de-emphasis levels (OB_0±, OB_1±, OB_2±, and OB_3±). PreB_0 and PreB_1 are internally pulled high. Please see Table 2 for de-emphasis levels.
$\overline{\text{LB0}}$	46	I	This pin is active LOW. A logic LOW at $\overline{\text{LB0}}$ enables the internal loopback path from IB_0± to OA_0±. $\overline{\text{LB0}}$ is internally pulled high. Please see Table 1 for more information.
$\overline{\text{LB1}}$	44	I	This pin is active LOW. A logic LOW at $\overline{\text{LB1}}$ enables the internal loopback path from IB_1± to OA_1±. $\overline{\text{LB1}}$ is internally pulled high. Please see Table 1 for more information.
$\overline{\text{LB2}}$	32	I	This pin is active LOW. A logic LOW at $\overline{\text{LB2}}$ enables the internal loopback path from IB_2± to OA_2±. $\overline{\text{LB2}}$ is internally pulled high. Please see Table 1 for more information.
$\overline{\text{LB3}}$	30	I	This pin is active LOW. A logic LOW at $\overline{\text{LB3}}$ enables the internal loopback path from IB_3± to OA_3±. $\overline{\text{LB3}}$ is internally pulled high. Please see Table 1 for more information.
RSV	59	I	Reserve pin to support factory testing. This pin can be left open, tied to GND, or tied to GND through an external pull-down resistor.

(1) **Note:** I = Input, O = Output, P = Power

PIN DESCRIPTIONS (continued)

Pin Name	Pin Number	I/O ⁽¹⁾	Description
POWER			
V _{CC}	5, 11, 20, 26, 35, 41, 50, 56	P	V _{CC} = 3.3V ± 5%. Each V _{CC} pin should be connected to the V _{CC} plane through a low inductance path, typically with a via located as close as possible to the landing pad of the V _{CC} pin. It is recommended to have a 0.01 µF or 0.1 µF, X7R, size-0402 bypass capacitor from each V _{CC} pin to ground plane.
GND	2, 8, 14, 17, 23, 29, 38, 47, 53	P	Ground reference. Each ground pin should be connected to the ground plane through a low inductance path, typically with a via located as close as possible to the landing pad of the GND pin.
GND	DAP	P	DAP is the metal contact at the bottom side, located at the center of the WQFN-60 pin package. It should be connected to the GND plane with at least 4 via to lower the ground impedance and improve the thermal performance of the package.

Functional Description
Table 1. Logic Table for Loopback Controls

LB0	Loopback Function
0	Enable loopback from IB_0± to OA_0±.
1 (default)	Normal mode. Loopback disabled.
LB1	Loopback Function
0	Enable loopback from IB_1± to OA_1±.
1 (default)	Normal mode. Loopback disabled.
LB2	Loopback Function
0	Enable loopback from IB_2± to OA_2±.
1 (default)	Normal mode. Loopback disabled.
LB3	Loopback Function
0	Enable loopback from IB_3± to OA_3±.
1 (default)	Normal mode. Loopback disabled.

Table 2. De-Emphasis Controls

PreA_[1:0]	Default VOD Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	De-Emphasis in dB (VODPE/VODB)
0 0	1200	1200	0
0 1	1200	850	-3
1 0	1200	600	-6
1 1 (Default)	1200	426	-9
PreB_[1:0]	Default VOD Level in mV_{PP} (VODB)	De-Emphasis Level in mV_{PP} (VODPE)	De-Emphasis in dB (VODPE/VODB)
0 0	1200	1200	0
0 1	1200	850	-3
1 0	1200	600	-6
1 1 (Default)	1200	426	-9

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage (V_{CC})		-0.3V to 4V
CMOS/TTL Input Voltage		-0.3V to ($V_{CC} + 0.3V$)
CML Input/Output Voltage		-0.3V to ($V_{CC} + 0.3V$)
Junction Temperature		+150°C
Storage Temperature		-65°C to +150°C
Lead Temperature Soldering, 4 sec		+260°C
Thermal Resistance, θ_{JA}		22.3°C/W
Thermal Resistance, θ_{JC}		3.2°C/W
Thermal Resistance, Φ_{JB}		10.3°C/W
ESD Ratings ⁽³⁾	HBM	6kV
	CDM	1kV
	MM	350V

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. For ensured specifications and the test conditions, see the [Electrical Characteristics](#) Tables. Operation of the device beyond the maximum Operating Ratings is not recommended.
- (2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
- (3) ESD tests conform to the following standards: Human Body Model (HBM) applicable standard: MIL-STD-883, Method 3015.7 Machine Model (MM) applicable standard: JESD22-A115-A (ESD MM std. of JEDEC) Field -Induced Charge Device Model (CDM) applicable standard: JESD22-C101-C (ESD FICDM std. of JEDEC)

Recommended Operating Ratings

	Min	Typ	Max	Units
Supply Voltage (V_{CC-GND})	3.135	3.3	3.465	V
Supply Noise Amplitude 10 Hz to 2 GHz			100	mV _{PP}
Ambient Temperature	-40		+85	°C
Case Temperature			100	°C

Electrical Characteristics⁽¹⁾⁽²⁾

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ ⁽³⁾	Max	Units
LVC MOS DC SPECIFICATIONS						
V _{IH}	High Level Input Voltage		2.0		V _{CC} + 0.3	V
V _{IL}	Low Level Input Voltage		-0.3		0.8	V
I _{IH}	High Level Input Current	V _{IN} = V _{CC}	-10		10	μA
I _{IL}	Low Level Input Current	V _{IN} = GND	75	94	124	μA
R _{PU}	Pull-High Resistance			35		kΩ
RECEIVER SPECIFICATIONS						
V _{ID}	Differential Input Voltage Range	AC Coupled Differential Signal. Below 1.25 Gb/s At 1.25 Gbps–3.125 Gbps Above 3.125 Gbps This parameter is not production tested.	100 100 100		1750 1560 1200	mV _{P-P} mV _{P-P} mV _{P-P}
V _{ICM}	Common Mode Voltage at Receiver Inputs	Measured at receiver inputs reference to ground.		1.3		V
R _{ITD}	Input Differential Termination	On-chip differential termination between IN+ or IN-. See Figure 8	84	100	116	Ω
DRIVER SPECIFICATIONS						
V _{ODB}	Output Differential Voltage Swing without De-Emphasis	R _L = 100Ω ±1% PreA_1 = 0; PreA_0 = 0 PreB_1 = 0; PreB_0 = 0 Driver de-emphasis disabled. Running K28.7 pattern at 4 Gbps. See Figure 7	1000	1200	1400	mV _{P-P}
V _{PE}	Output De-Emphasis Voltage Ratio 20*log(V _{ODPE} /V _{ODB})	R _L = 100Ω ±1% Running K28.7 pattern at 4.25 Gbps PreX_[1:0] = 00 PreX_[1:0] = 01 PreX_[1:0] = 10 PreX_[1:0] = 11 X = A/B channel de-emphasis drivers See Figure 2/ Figure 7		0 -3 -6 -9		dB dB dB dB
t _{PE}	De-Emphasis Width	Tested at -9 dB de-emphasis level, PreX[1:0] = 11 X = A/B channel de-emphasis drivers See Figure 6 on measurement condition.	125	200	250	ps
R _{OTSE}	Output Termination	On-chip termination from OUT+ or OUT- to V _{CC}	42	50	58	Ω
R _{OTD}	Output Differential Termination	On-chip differential termination between OUT+ and OUT-		100		Ω
ΔR _{OTSE}	Mis-Match in Output Termination Resistors	Mis-match in output termination resistors			5	%
V _{OCM}	Output Common Mode Voltage			2.7		V
POWER DISSIPATION						
P _D	Power Dissipation	V _{DD} = 3.465V All outputs terminated by 100Ω ±1%. PreB_[1:0] = 0, PreA_[1:0] = 0 Running PRBS 2 ⁷ -1 pattern at 4.25 Gbps			1.3	W

- (1) IN+ and IN- are generic names that refer to one of the many pairs of complementary inputs of the DS42BR400. OUT+ and OUT- are generic names that refer to one of the many pairs of the complementary outputs of the DS42BR400. Differential input voltage V_{ID} is defined as |IN+ - IN-|. Differential output voltage V_{OD} is defined as |OUT+ - OUT-|.
- (2) K28.7 pattern is a 10-bit repeating pattern of K28.7 code group {001111 1000} K28.5 pattern is a 20-bit repeating pattern of +K28.5 and -K28.5 code groups {110000 0101 001111 1010}
- (3) Typical specifications are at TA=25 C, and represent most likely parametric norms at the time of product characterization. The typical specifications are not ensured.

Electrical Characteristics⁽¹⁾⁽²⁾ (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

Parameter		Test Conditions	Min	Typ (3)	Max	Units
AC CHARACTERISTICS						
t _R	Differential Low to High Transition Time	Measured with a clock-like pattern at 4.25 Gbps, between 20% and 80% of the differential output voltage. De-emphasis disabled. Transition time is measured with the fixture shown in Figure 7 adjusted to reflect the transition time at the output pins.		80		ps
t _F	Differential High to Low Transition Time			80		ps
t _{PLH}	Differential Low to High Propagation Delay	Measured at 50% differential voltage from input to output.			1	ns
t _{PHL}	Differential High to Low Propagation Delay				1	ns
t _{SKP}	Pulse Skew	t _{PHL} - t _{PLH}			20	ps
t _{SKO}	Output Skew ⁽⁴⁾	Difference in propagation delay between channels on the same part (Channel-to-Channel Skew) ⁽⁴⁾			100	ps
t _{SKPP}	Part-to-Part Skew ⁽⁴⁾	Difference in propagation delay between devices across all channels operating under identical conditions			165	ps
t _{LB}	Loopback Delay Time	Delay from enabling loopback mode to signals appearing at the differential outputs See Figure 5			4	ns
RJ	Device Random Jitter ⁽⁵⁾	At 0.25 Gbps At 1.5 Gbps At 4.25 Gbps Alternating-10 pattern. De-emphasis disabled. See Figure 7			2 2 2	ps rms ps rms ps rms
DJ	Device Deterministic Jitter ⁽⁶⁾	At 0.25 Mbps, PRBS7 pattern At 1.5 Gbps, K28.5 pattern At 4.25 Gbps, K28.5 pattern At 4.25 Gbps, PRBS7 pattern De-emphasis disabled. See Figure 7			25 25 25 25	ps pp ps pp ps pp ps pp
DR	Data Rate ⁽⁷⁾	Alternating-10 pattern	0.25		4.25	Gbps

(4) t_{SKO} is the magnitude difference in propagation delays between all data paths on one device. This is channel-to-channel skew. t_{SKPP} is the worst case difference in propagation delay across multiple devices on all channels and operating under identical conditions. For example, for two devices operating under the same conditions, t_{SKPP} is the magnitude difference between the shortest propagation delay measurement on one device to the longest propagation delay measurement on another device.

(5) Device output random jitter is a measurement of random jitter contributed by the device. It is derived by the equation $\text{SQRT}[(\text{RJ}_{\text{OUT}})^2 - (\text{RJ}_{\text{IN}})^2]$, where RJ_{OUT} is the total random jitter measured at the output of the device in ps(rms), RJ_{IN} is the random jitter of the pattern generator driving the device. Below 400 Mbps, system jitter and device jitter could not be separated. The 250 Mbps specification includes system random jitter. Please see [Figure 7](#) for the AC test circuit.

(6) Device output deterministic jitter is a measurement of the deterministic jitter contribution from the device. It is derived by the equation (DJ_{OUT} - DJ_{IN}), where DJ_{OUT} is the total peak-to-peak deterministic jitter measured at the output of the device in ps(p-p). DJ_{IN} is the peak-to-peak deterministic jitter at the input of the test board. Please see [Figure 7](#) for the AC test circuit.

(7) This parameter is specified by design and/or characterization and is not tested in production.

TIMING DIAGRAMS

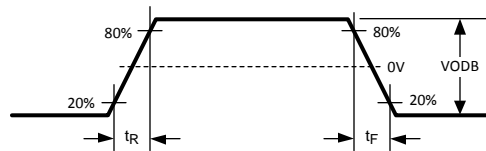


Figure 3. Driver Output Transition Time

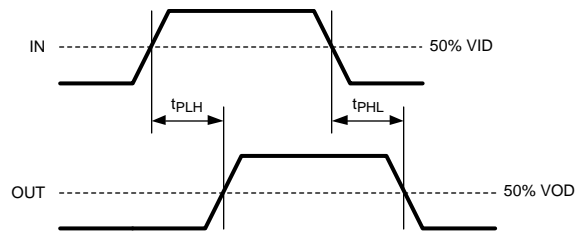


Figure 4. Propagation Delay

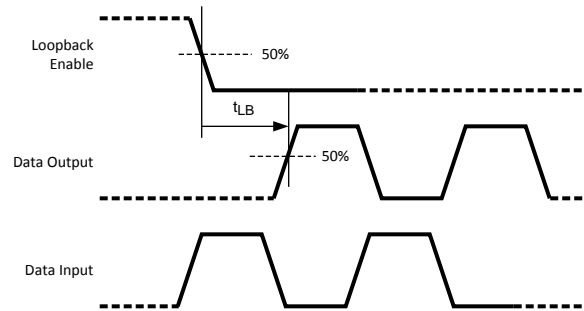


Figure 5. Loopback Delay Timing

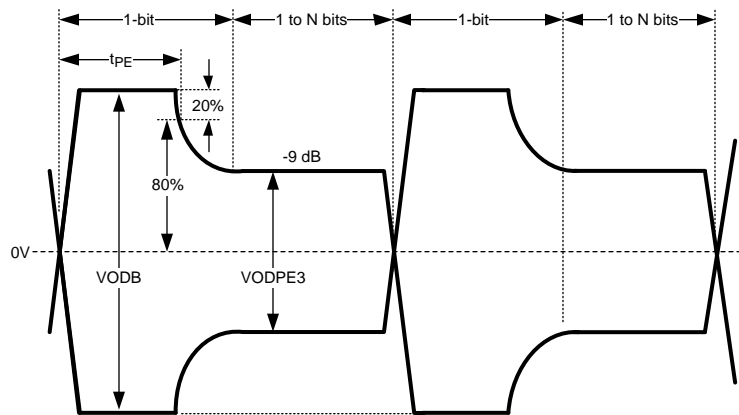


Figure 6. Output De-Emphasis Duration

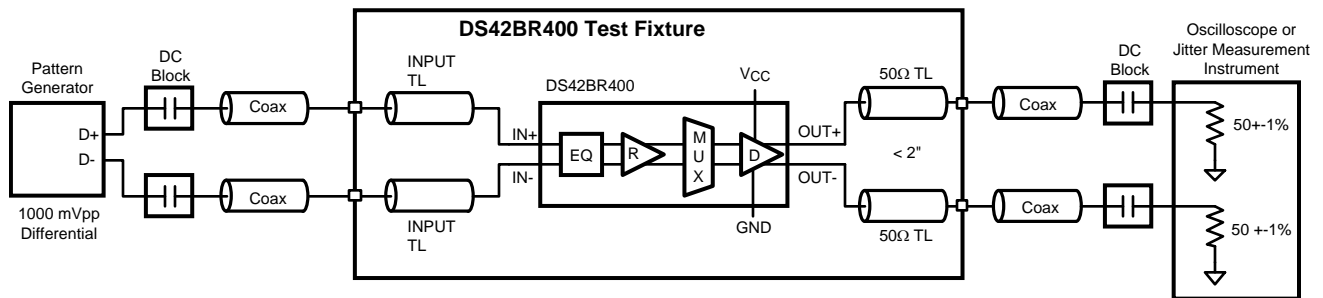


Figure 7. AC Test Circuit

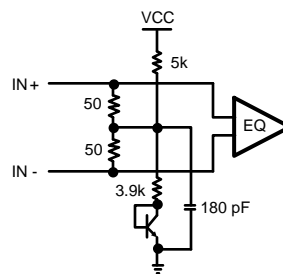



Figure 8. Receiver Input Termination

REVISION HISTORY

Changes from Revision I (April 2013) to Revision J	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DS42BR400TSQ/NOPB	ACTIVE	WQFN	NKA	60	250	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	DS42BR400 TSQ	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS42BR400TSQ/NOPB	WQFN	NKA	60	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

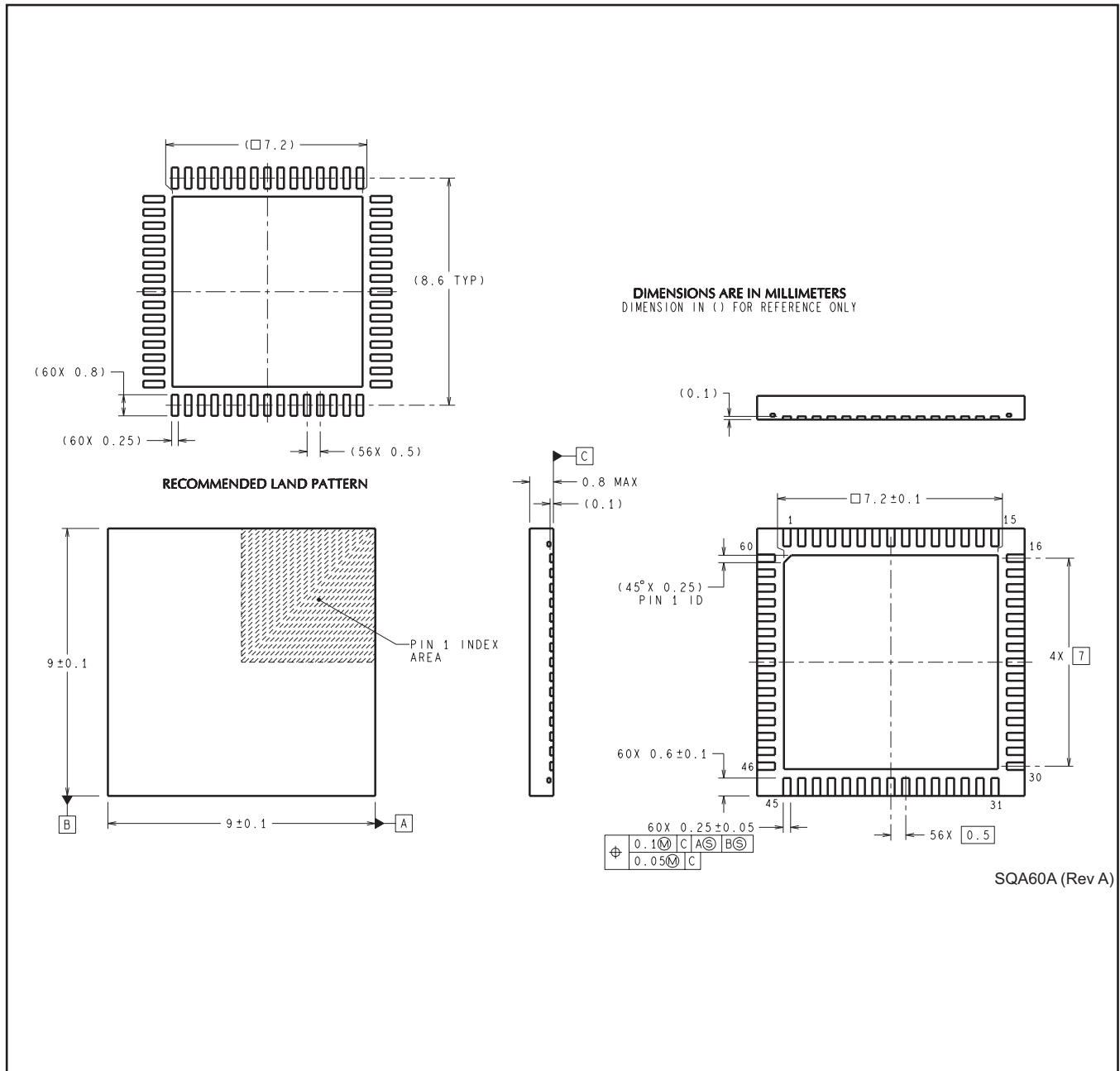
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS42BR400TSQ/NOPB	WQFN	NKA	60	250	210.0	185.0	35.0

NKA0060A



IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View DS42BR400TSQ/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management