MIC23099

Single AA/AAA Cell Step-up/Step-Down Regulators with Battery Monitoring

Features

- V_{IN} Range from 0.85V to 1.6V
- V_{OUT1} (step-up) Adjustable from 1.8V to 3.3V
- V_{OUT2} (step-down) Adjustable from 1.0V to V_{OUT1}
- V_{OUT1}/400 mW and V_{OUT2}/30 mA from a Single Cell
- Minimizes Switching Noise in the Audio Band
- Step-up Regulator with Output Disconnect in Shutdown
- V_{OUT1}, Above 90% Efficiency for 5 mA to 200 mA
- Anti-Ringing Control Circuit to Minimize EMI
- Turn-On Inrush Current-Limiting and Soft Start
- Automatic Output Discharge
- Low-Battery Indicator
- Power Good (PG) Output
- Low Output Ripple < 10 mV
- Short-Circuit and Thermal Protection
- 14-Pin, 2.5 mm x 2.5 mm x 0.55 mm Thin QFN (TQFN) Package
- -40°C to +125°C Junction Temperature Range

Applications

- Audio Headsets
- Portable Applications

General Description

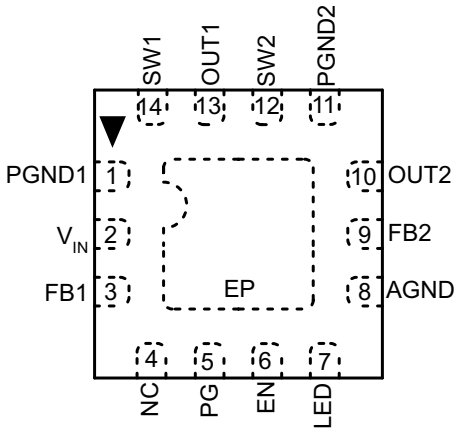
The MIC23099 is a high-efficiency, low-noise, dual output, integrated power management solution for single-cell alkaline or NiMH battery applications. The synchronous boost output voltage (V_{OUT1}) is enabled first and is powered from the battery. Next, the synchronous buck output (V_{OUT2}), which is powered from the boost output voltage, is enabled. This configuration allows V_{OUT2} to be independent of battery voltage, thereby allowing the buck output voltage to be higher or lower than the battery voltage.

To minimize switching artifacts in the audio band, both the converters are designed to operate with a minimum switching frequency of 80 kHz for the buck and 100 kHz for the boost. The high-current boost has a maximum switching frequency of 1 MHz, minimizing the solution footprint.

The MIC23099 incorporates both battery management functions and Fault protection. The low-battery level is indicated by an external LED connected to the LED pin. In addition, a supervisory circuit monitors each output and asserts a Power Good (PG) signal when the sequencing is done or deasserted when a Fault condition occurs.

Data sheets and other support documentation can be found on the Microchip web site at: www.microchip.com.

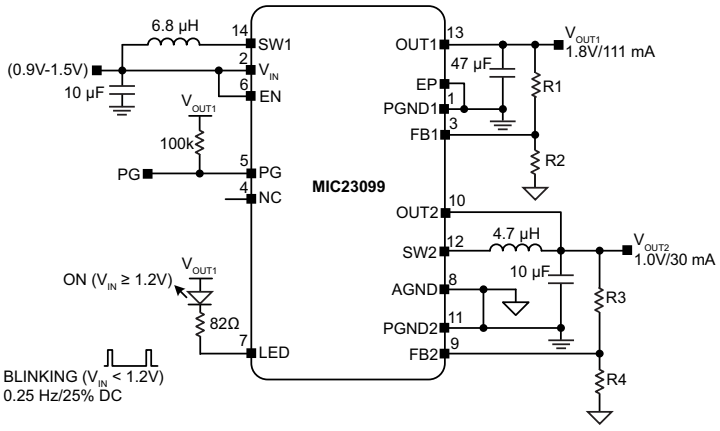
Package Type

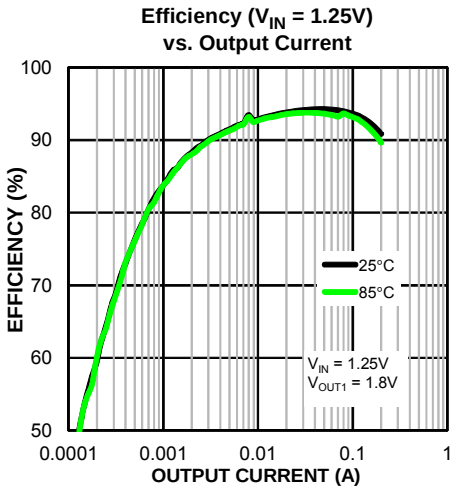


14-Pin 2.5 mm x 2.5 mm QFN (FT)
(Top View)

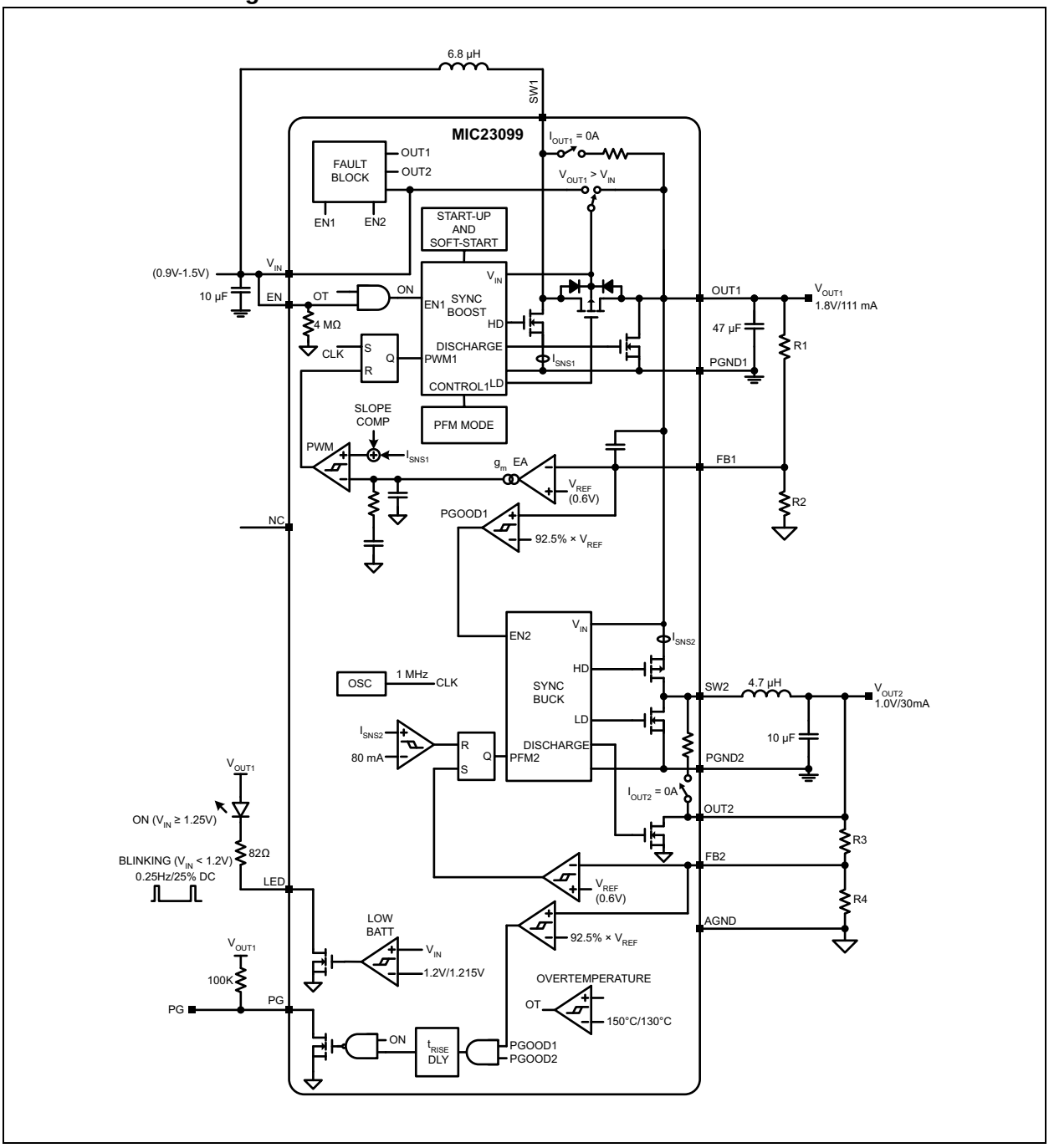
Note: Thin QFN Pin 1 identifier = "▲".

Typical Application Schematic





Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Supply Voltage (V_{IN}) ..... -0.3V to +6.0V
Switch Voltage (V_{SW1}) ..... -0.3V to +6.0V
Switch Voltage (V_{SW2}) ..... -0.8V to +6.0V
Enable Voltage (V_{EN}) ..... -0.3V to V_{IN}
Feedback Voltage (V_{FB}) ..... -0.3V to +6.0V
LED Output (V_{LED}) ..... -0.3V to +6.0V
Power Good (V_{PG}) ..... -0.3V to +6.0V
AGND to PGND1, PGND2 ..... -0.3V to +0.3V
Ambient Storage Temperature (T_S) ..... -65°C to +150°C
ESD HBM Rating[1] ..... 2 kV
ESD MM Rating 200V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: Devices are ESD-sensitive. Handling precautions are recommended. Human body model, 1.5 kΩ in series with 100 pF.

Operating Ratings[1]

Input Voltage after Start-up (V_{IN}) ..... +0.875V to +1.6V
Enable Voltage (V_{EN}) ..... 0V to V_{IN}
LED Output (V_{LED}) ..... 0V to V_{OUT1}
Output Voltage Range (V_{OUT1}) ..... +1.8V to +3.3V
Output Voltage Range (V_{OUT2}) ..... +1.0V to V_{OUT1}
Junction Temperature (T_J)[2] ..... -40°C to +125°C
Junction Thermal Resistance
2.5 mm x 2.5 mm Thin QFN-14 (θ_{JA}) ..... +70°C/W
2.5 mm x 2.5 mm Thin QFN-14 (θ_{JC}) ..... +25°C/W

Note 1: The device is not ensured to function outside the operating range.
2: The maximum allowable power dissipation is a function of the maximum junction temperature ($T_{J(MAX)}$), the junction-to-ambient thermal resistance (θ_{JA}) and the ambient temperature (T_A). The maximum allowable power dissipation will result in excessive die temperature and the regulator will go into thermal shutdown.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1]

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{EN} = +1.25V$; $V_{OUT1} = +1.8V$; $V_{OUT2} = +1.0V$; $L_{OUT1} = 6.8\ \mu H$; $L_{OUT2} = 4.7\ \mu H$; $C_{OUT1} = 47\ \mu F$; $C_{OUT2} = 10\ \mu F$; $T_A = +25°C$. **Boldface** values indicate $-40°C \le T_J \le +125°C$.						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Input Supply (V_{IN})						
$V_{START(MIN)}$	Minimum Start-up Voltage	—	0.75	**0.9**	V	V_{IN} rising, $R_{LOAD} \ge 500\Omega$, $I_{OUT2} = 0$ mA
I_{Q_PFM}	Quiescent Current – PFM Mode	—	200	**270**	µA	I_{OUT1}, $I_{OUT2} = 0$ mA (switching, closed loop), measured at V_{IN} with LED pin open
		—	12.6	—	mA	$I_{OUT1} = 2$ mA, $I_{OUT2} = 10$ mA (switching, closed loop), measured at V_{IN}
I_{SHDN}	Shutdown Current	—	0.02	**2**	µA	$V_{EN} = 0V$, $V_{IN} = 1.6V$, measured at V_{IN}
Enable Input (EN)						
EN_{HIGH}	EN Logic Level High to Start-up	**0.8**	0.58	—	V	V_{EN} rising, regulator enabled
EN_{LOW}	EN Logic Level Low	—	0.5	**0.2**	V	V_{EN} falling, regulator shutdown
I_{ENBIAS}	EN Bias Current	—	0.3	**1**	µA	$V_{EN} = 0V$ (regulator shutdown)
R_{EN_PD}	EN Pull-Down Resistance	**3.0**	4.0	**5.0**	MΩ	$I_{EN} = 0.5\ \mu A$ into pin
Solution Efficiency						
	System Efficiency	—	88	—	%	$V_{IN} = 1.25V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 1.0V$, $P_{OUT1} = 8$ mW, $P_{OUT2} = 20$ mW
		—	92	—		$V_{IN} = 1.25V$, $V_{OUT1} = 1.8V$, $V_{OUT2} = 1.0V$, $P_{OUT1} = 80$ mW, $P_{OUT2} = 20$ mW

Note 1: Specifications are for packaged product only.

2: Ensured by design.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{EN}$ = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = +1.0V; L_{OUT1} = 6.8 µH; L_{OUT2} = 4.7 µH; C_{OUT1} = 47 µF; C_{OUT2} = 10 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Fault Conditions						
V_{IN} and V_{OUT1}, V_{OUT2} Fault Conditions						
V_{VIN_OFF}	V_{IN} Turn-Off Threshold Voltage	0.825	0.85	0.875	V	V_{IN} falling, after start-up
$V_{PG\_DLY(DEG)}$	PG Deglitch Delay, V_{IN} Fault	120	—	180	ms	V_{IN} falling below 0.85V to V_{PG} = Low
$V_{PG\_DLY(DEG)}$	PG Deglitch Delay, V_{OUT1}, V_{OUT2} Fault	60	—	120	ms	V_{OUT1} or V_{OUT2} falling below 90% of target value to V_{PG} = Low
T_{COFF_DLY}	Cool-Off Delay Time	750	1300	2250	ms	V_{PG} = Low to V_{OUT1} enabled, C_{OUT1} = 47 µF, C_{OUT2} = 10 µF
	Hiccup Cycles before Latch-Off	—	15	—	Cycles	Counts cool-off cycles
R_{OUT1_DCHG}	OUT1 Active Discharge Resistance	—	500	700	Ω	V_{EN} = 0V
R_{OUT2_DCHG}	OUT2 Active Discharge Resistance	—	500	700	Ω	V_{EN} = 0V
Power Good Output (PG)						
V_{PG_TH}	PG Threshold Voltage	90	92.5	95	$\%V_{REF1}$	V_{REF1} rising or falling
		90	92.5	95	$\%V_{REF2}$	V_{REF2} rising or falling
V_{PG_LOW}	PG Output Low Voltage	—	0.1	**0.5**	V	I_{PG} = 1 mA (sinking), V_{EN} = 0V
I_{PG_LEAK}	PG Leakage Current	**-1**	0.01	**1**	µA	V_{PG} = 1.8V, V_{EN} = 1.8V
t_{PG_DLY}	PG Turn-On Delay	10	—	50	ms	
LED Low-Battery Indicator Output (LED)						
V_{LBVD}	Low-Battery Threshold	**1.15**	1.2	**1.25**	V	V_{IN} falling
L_{B_HYST}	Low-Battery Hysteresis	—	—	31	mV	V_{IN} rising
$f_{LEDFLASH}$	LED Flash Frequency	0.125	0.25	0.5	Hz	V_{IN} = 1.15V, V_{EN} = 1.15V
$D_{LEDFLASH}$	LED Flash Duty Cycle	22.5	25	27.5	%	V_{IN} = 1.15V, V_{EN} = 1.15V
I_{LK_LED}	LED Output Leakage Current	—	0.01	1	µA	V_{LED} = 4.0V, V_{EN} = 0V
$R_{LED(ON)}$	LED Switch-On Resistance	—	—	25	Ω	$V_{IN} = V_{EN}$ = 1.25V, I_{LED} = 1.0 mA
Thermal Protection						
T_{SHD}	Thermal Shutdown	—	150	—	°C	T_J rising
T_{SHD_HYST}	Thermal Hysteresis	—	20	—	°C	Temperature decreasing

Note 1: Specifications are for packaged product only.

2: Ensured by design.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{EN}$ = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = +1.0V; L_{OUT1} = 6.8 µH; L_{OUT2} = 4.7 µH; C_{OUT1} = 47 µF; C_{OUT2} = 10 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Boost						
Boost Reference (FB1)						
V_{FB}	Feedback Regulation Voltage	**0.579**	0.6	**0.621**	V	V_{IN} = 0.9V to 1.5V, PWM mode
I_{FB_BIAS}	FB Bias Current	—	1	500	nA	V_{FB1} = 0.6V
T_{SS_BOOST}	Soft Start Time	—	5	—	ms	V_{OUT1}: 10% to 90% of target value, R_{LOAD} = 500Ω; C_{OUT1} = 47 µF
Boost Internal MOSFETs						
R_{HS}	High-Side On Resistance	—	200	—	mΩ	I_{SW1} = 100 mA, V_{IN} = 1.25V
R_{LS}	Low-Side On Resistance	—	140	—	mΩ	I_{SW1} = 100 mA, V_{IN} = 1.25V
I_{SW1_LEAK}	Leakage Current into SW1	—	0.01	**2**	µA	V_{SW} = 4.0V, V_{OUT1} = 0V, V_{EN} = 0V, V_{IN} = 4.0V
R_{AR_BOOST}	Anti-Ringing Resistance	—	80	140	Ω	
Boost Switching Frequency						
f_{SW}	Switching Frequency	0.9	1.0	1.1	MHz	PWM mode
$f_{SW(MIN)\_BOOST}$	Minimum Switching Frequency[2]	100	—	—	kHz	P_{OUT1} = 20 mW (PFM mode)
D_{MIN_BOOST}	Minimum Duty Cycle	—	15	—	%	V_{FB1} = 0.7V
D_{MAX_BOOST}	Maximum Duty Cycle	—	85	—	%	V_{FB1} = 0.5V
Boost Current Limit						
$I_{OUT(MAX)\_BOOST}$	Maximum Output Power	—	450	—	mW	V_{OUT1} > 1.8V, I_{OUT2} = 0 mA
I_{LIM_NMOS}	Current-Limit Threshold (NMOS)	**1.0**	1.5	**2.0**	A	V_{FB1} = 0.5V
I_{LIM_PMOS}	Current-Limit Threshold (PMOS)	1.5	2.5	3.0	A	V_{FB1} = 0.5V
$I_{LIM\_LINEAR(PMOS)}$	Linear Mode Current Limit (PMOS)	56	80	180	mA	V_{IN} = 1.25V, V_{OUT1} = 0V
Boost Power Supply Rejection						
	PSRR ($\Delta V_{IN}/\Delta V_{OUT1}$)	—	50	—	dB	ΔV_{IN} = 200 mVp-p, f = 217 Hz, I_{OUT1} = PFM
		—	50	—		ΔV_{IN} = 200 mVp-p, f = 1.0 kHz, I_{OUT1} = PFM
		—	42	—		ΔV_{IN} = 200 mVp-p, f = 20 kHz, I_{OUT1} = PFM

Note 1: Specifications are for packaged product only.

2: Ensured by design.

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1] (CONTINUED)

Electrical Specifications: unless otherwise specified, $V_{IN} = V_{EN}$ = +1.25V; V_{OUT1} = +1.8V; V_{OUT2} = +1.0V; L_{OUT1} = 6.8 µH; L_{OUT2} = 4.7 µH; C_{OUT1} = 47 µF; C_{OUT2} = 10 µF; T_A = +25°C. **Boldface** values indicate -40°C ≤ T_J ≤ +125°C.						
Symbol	**Parameter**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Buck						
Buck Reference (FB2)						
V_{FB2}	Feedback Regulation Voltage	**0.579**	0.6	**0.621**	V	V_{OUT1} = 1.8V to 3.3V, I_{OUT2} = 6 mA to 30 mA (±3.5%)
I_{FB2_BIAS}	FB Bias Current	—	1	500	nA	V_{FB2} =0.6V
t_{SS}	Soft Start Time	—	0.1	—	ms	V_{OUT2}: 10% to 90% of target value, I_{OUT2} = 0 mA, C_{OUT2} = 10 µF
Buck Internal MOSFETs						
R_{HS_BUCK}	High-Side On Resistance	—	560	—	mΩ	I_{SW2} = 100 mA, V_{OUT1} = 1.8V
R_{LS_BUCK}	Low-Side On Resistance	—	380	—	mΩ	I_{SW2} = 100 mA, V_{OUT1} = 1.8V
I_{SW2LK_IN}	Leakage Current into SW2	—	0.01	2	µA	V_{OUT1} = 3.3V, V_{SW2} = 3.3V, V_{EN} = 0V, V_{OUT2} = 3.3V
I_{SW2LK_OUT}	Leakage Current out of SW2	—	0.01	0.5	µA	V_{OUT1} = 3.3V, V_{SW2} = 0V, V_{EN} = 0V, V_{OUT2} = 0V
R_{AR_BUCK}	Anti-Ringing Resistance	—	80	140	W	
Buck Switching Frequency						
$f_{SW(MIN)\_BUCK}$	Minimum Switching Frequency[2]	80	—	—	kHz	P_{OUT2} = 8 mW (PFM mode)
D_{MAX_BUCK}	Maximum Duty Cycle	—	100	—	%	V_{FB2} = 0.5V
Buck Current Limit						
$I_{OUT(MAX)\_BUCK}$	Maximum Output Current	—	30	—	mA	
I_{LIM_PMOS}	Current-Limit Threshold (PMOS)	—	80	120	mA	V_{FB2} = 0.5V
Buck Power Supply Rejection						
	PSRR ($\Delta V_{OUT1}/\Delta V_{OUT2}$)	—	50	—	dB	ΔV_{OUT1} = 200 mVp-p, f = 217 Hz, I_{OUT2} = 10 mA
		—	50	—		ΔV_{OUT1} = 200 mVp-p, f = 1.0 kHz, I_{OUT2} = 10 mA
		—	42	—		ΔV_{OUT1} = 200 mVp-p, f = 20 kHz, I_{OUT2} = 10 mA

Note 1: Specifications are for packaged product only.

2: Ensured by design.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

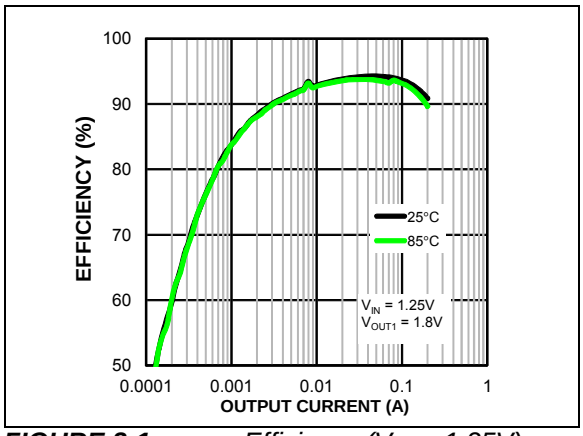


FIGURE 2-1: *Efficiency (V_{IN} = 1.25V) vs. Output Current.*

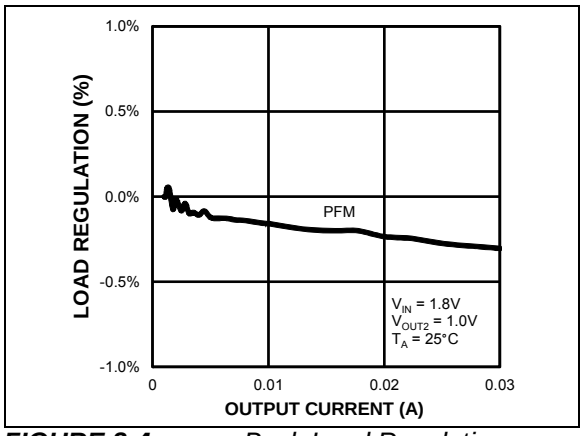


FIGURE 2-4: *Buck Load Regulation vs. Output Current.*

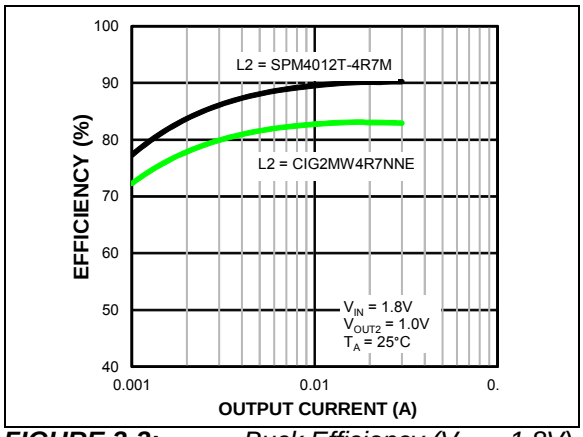


FIGURE 2-2: *Buck Efficiency (V_{IN} = 1.8V) vs. Output Current.*

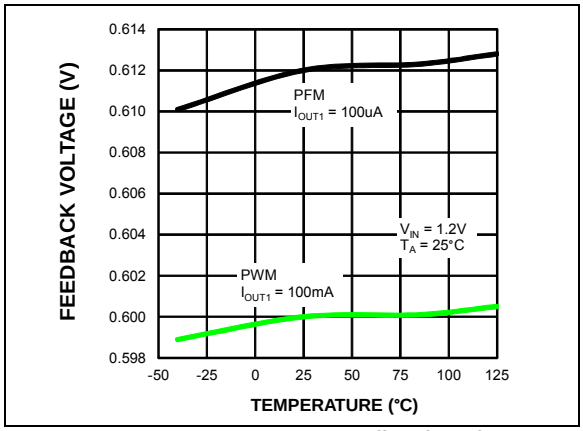


FIGURE 2-5: *Boost Feedback Voltage vs. Temperature.*

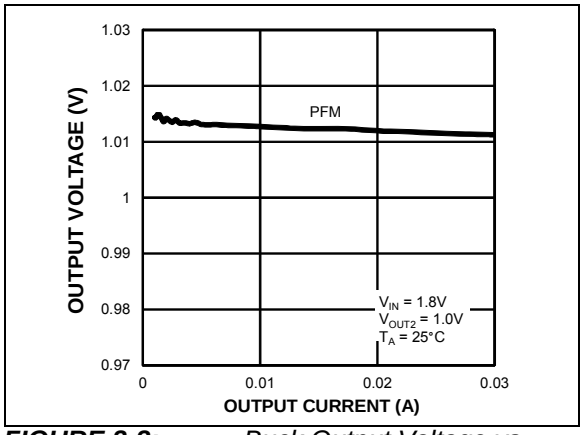


FIGURE 2-3: *Buck Output Voltage vs. Output Current.*

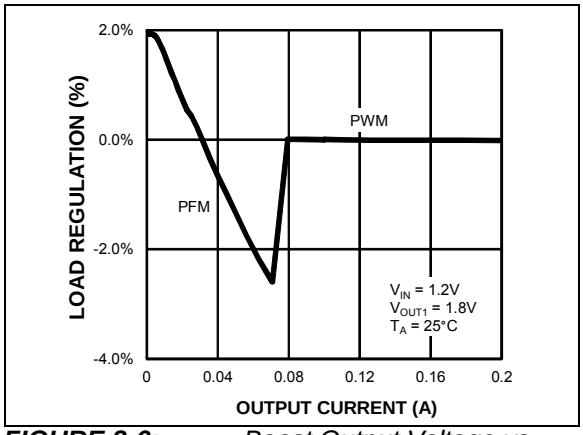


FIGURE 2-6: *Boost Output Voltage vs. Output Current.*

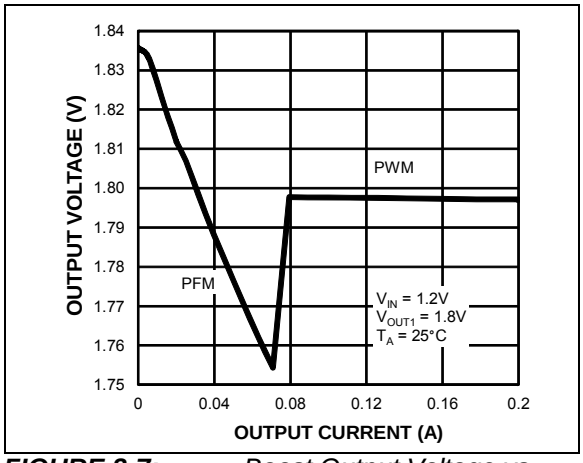


FIGURE 2-7: *Boost Output Voltage vs. Output Current.*

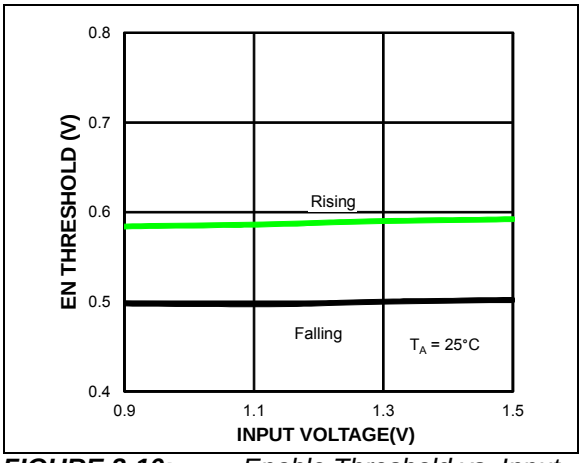


FIGURE 2-10: *Enable Threshold vs. Input Voltage.*

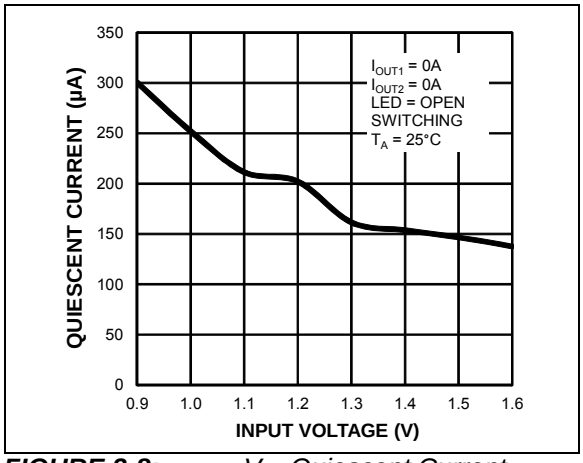


FIGURE 2-8: *V_{IN} Quiescent Current (Switching) vs. Input Voltage.*

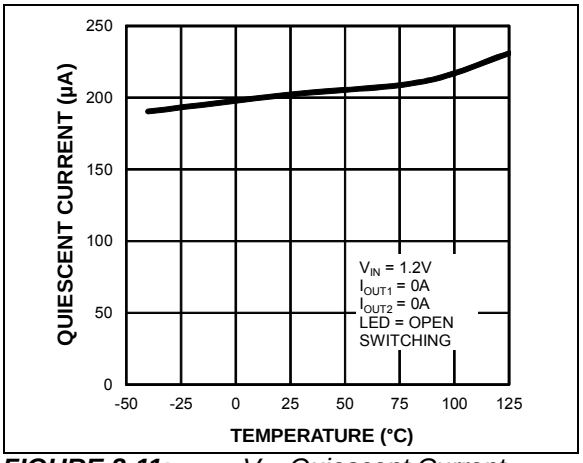


FIGURE 2-11: *V_{IN} Quiescent Current (Switching) vs. Temperature.*

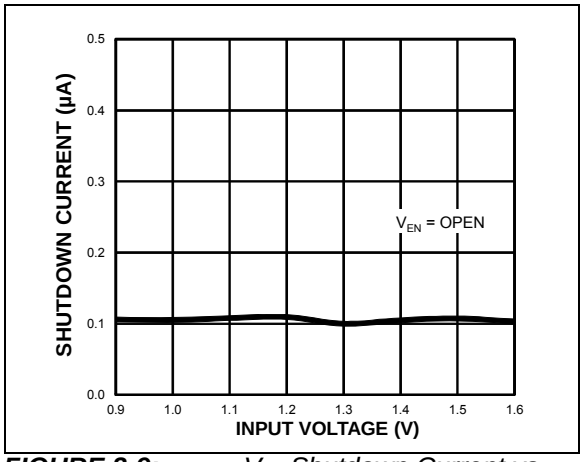


FIGURE 2-9: *V_{IN} Shutdown Current vs. Input Voltage.*

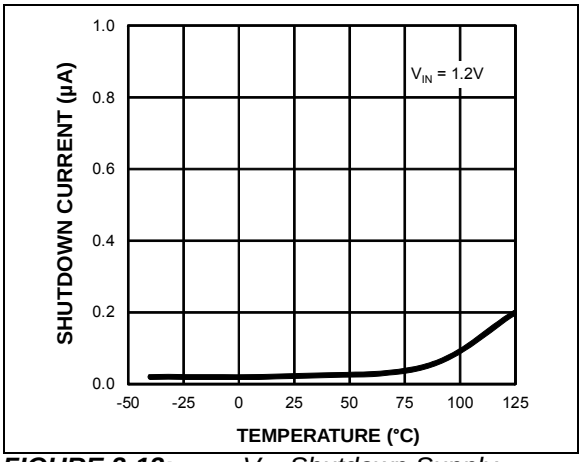


FIGURE 2-12: *V_{IN} Shutdown Supply Current vs. Temperature.*

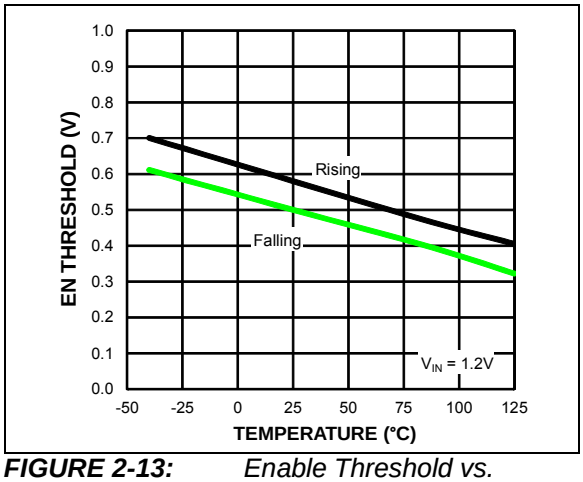


FIGURE 2-13: *Enable Threshold vs. Temperature.*

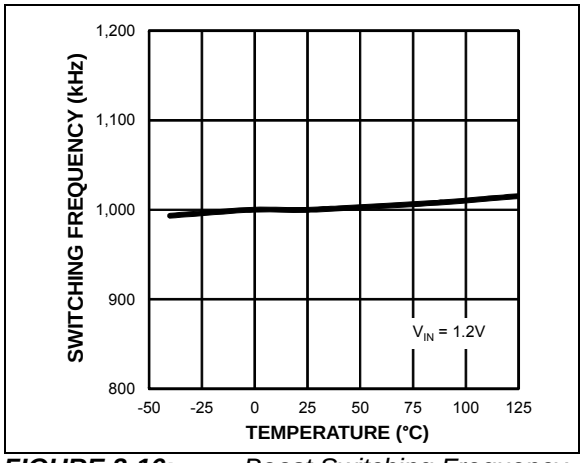


FIGURE 2-16: *Boost Switching Frequency (PWM) vs. Temperature.*

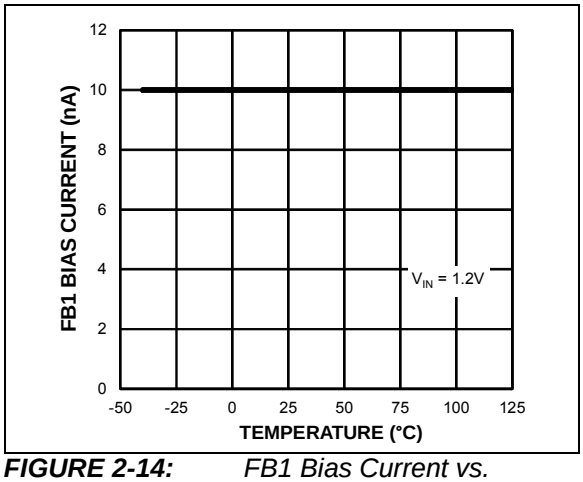


FIGURE 2-14: *FB1 Bias Current vs. Temperature.*

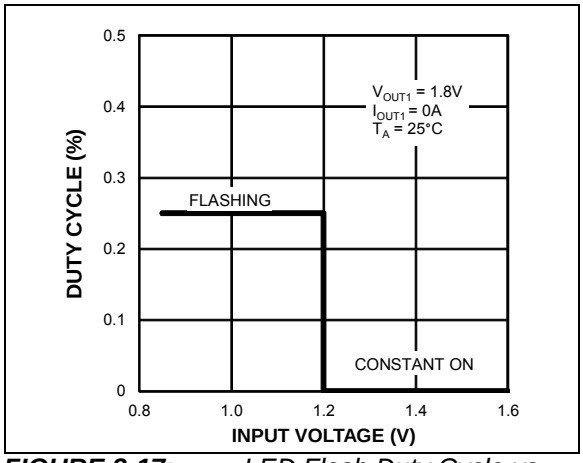


FIGURE 2-17: *LED Flash Duty Cycle vs. Input Voltage.*

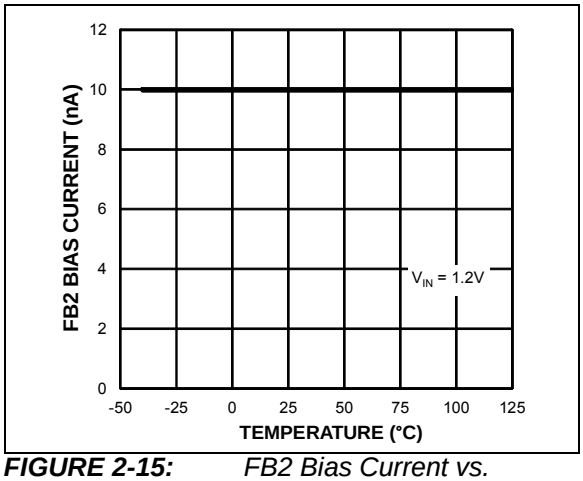


FIGURE 2-15: *FB2 Bias Current vs. Temperature.*

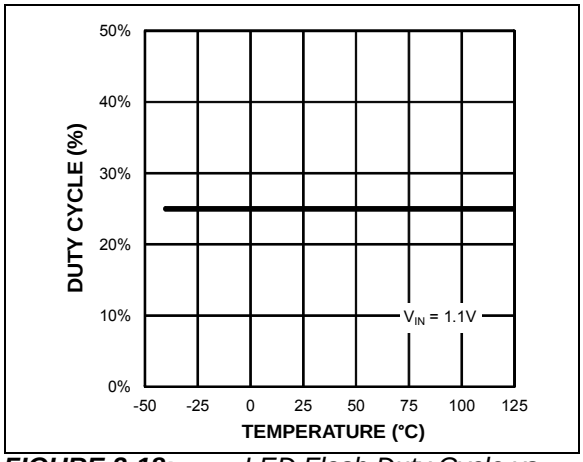


FIGURE 2-18: *LED Flash Duty Cycle vs. Temperature.*

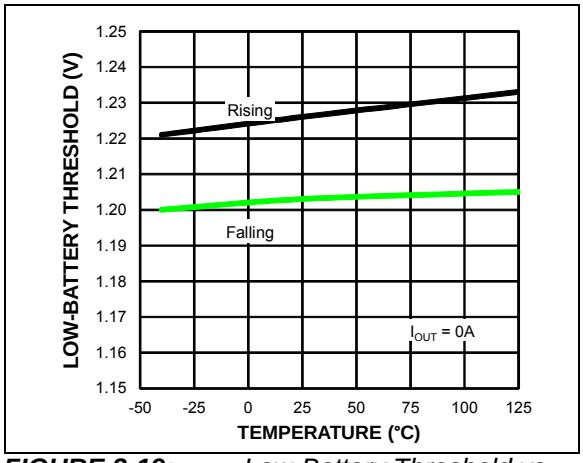


FIGURE 2-19: *Low-Battery Threshold vs. Temperature.*

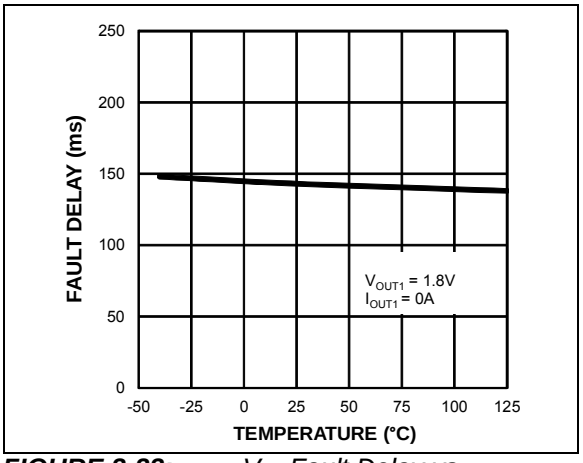


FIGURE 2-22: *V_{IN} Fault Delay vs. Temperature.*

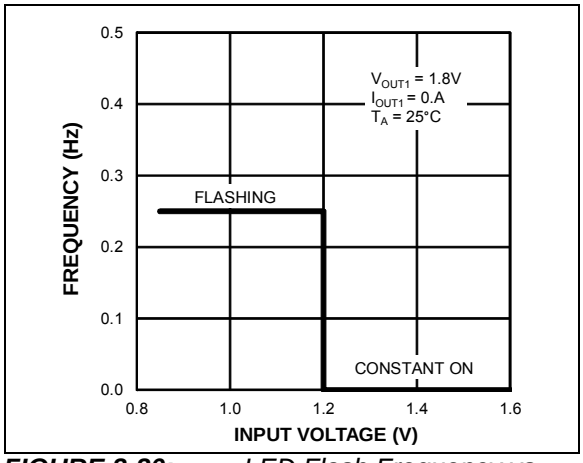


FIGURE 2-20: *LED Flash Frequency vs. Input Voltage.*

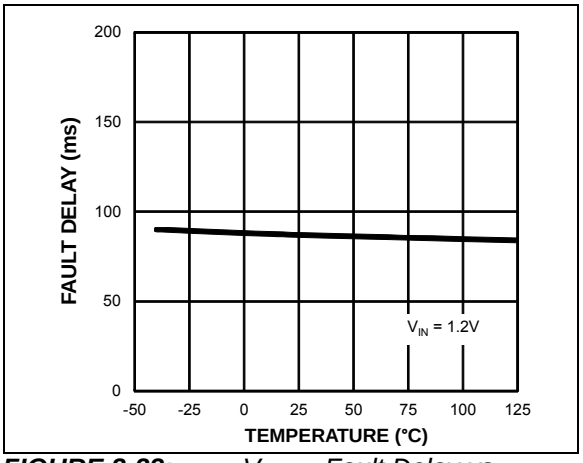


FIGURE 2-23: *V_{OUT1} Fault Delay vs. Temperature.*

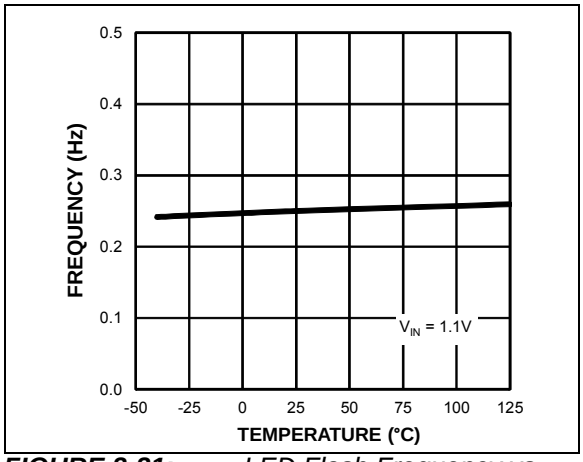


FIGURE 2-21: *LED Flash Frequency vs. Temperature.*

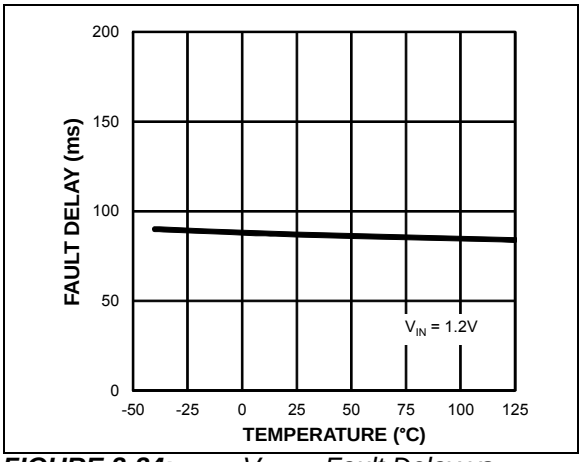


FIGURE 2-24: *V_{OUT2} Fault Delay vs. Temperature.*

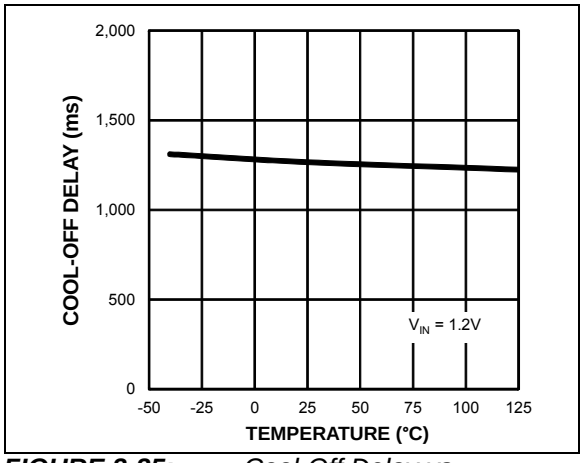


FIGURE 2-25: *Cool-Off Delay vs. Temperature.*

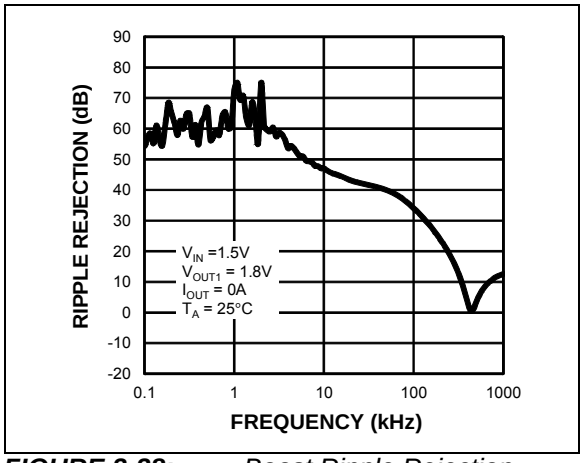


FIGURE 2-28: *Boost Ripple Rejection.*

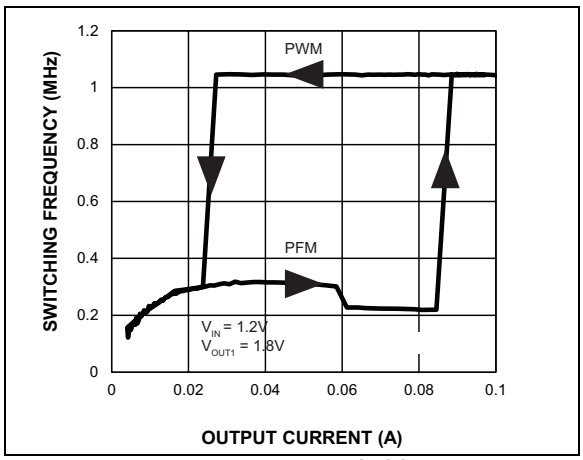


FIGURE 2-26: *Boost Switching Frequency vs. Output Current.*

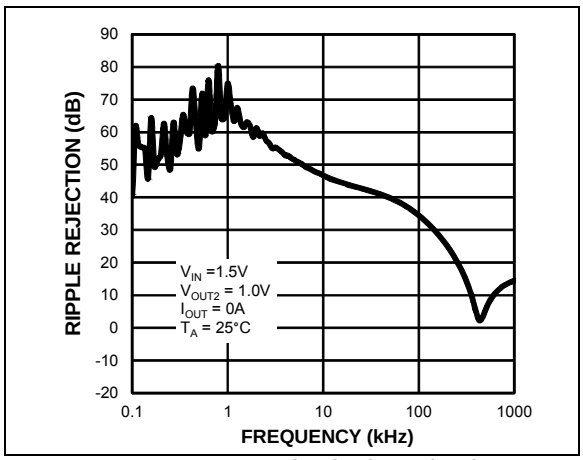


FIGURE 2-29: *Buck Ripple Rejection.*

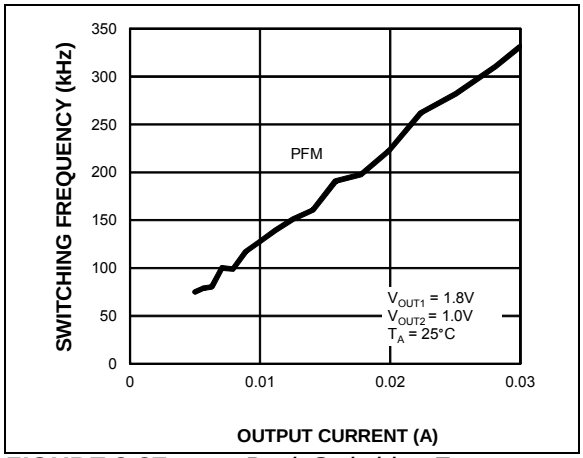


FIGURE 2-27: *Buck Switching Frequency vs. Output Current.*

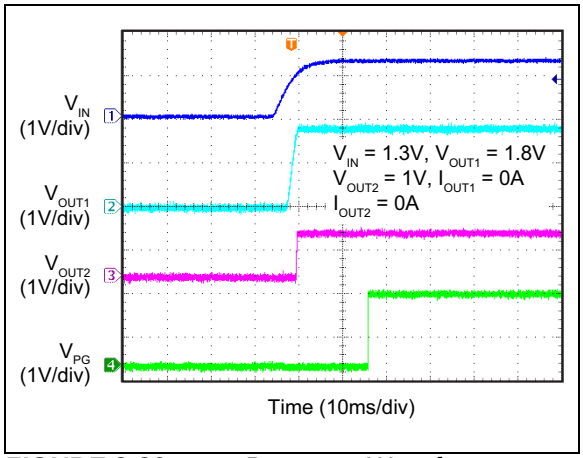


FIGURE 2-30: *Power-up Waveforms.*

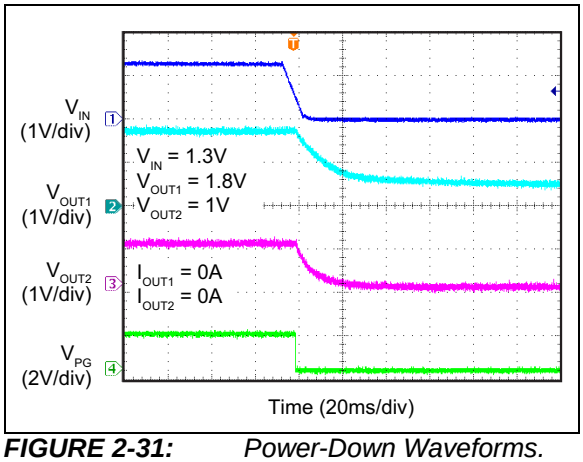


FIGURE 2-31: *Power-Down Waveforms.*

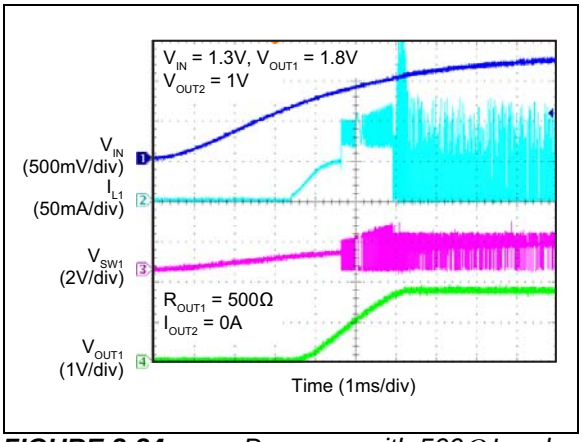


FIGURE 2-34: *Power-up with 500Ω Load.*

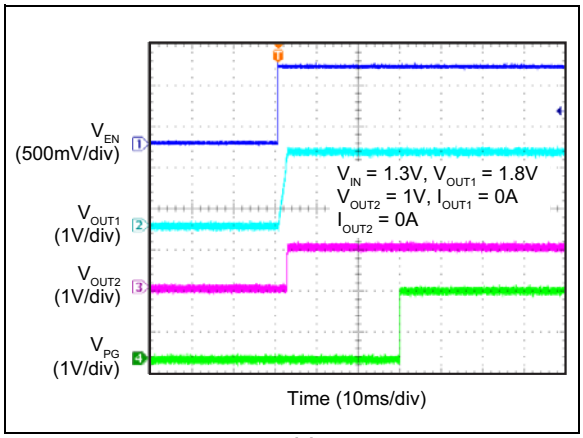


FIGURE 2-32: *Enable Turn-On.*

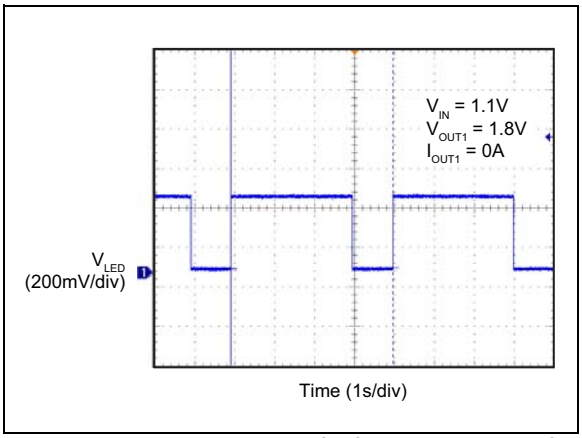


FIGURE 2-35: *LED Flash Frequency and Duty Cycle.*

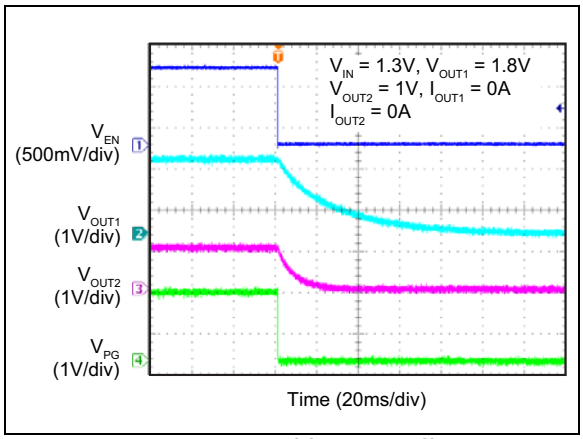


FIGURE 2-33: *Enable Turn-Off.*

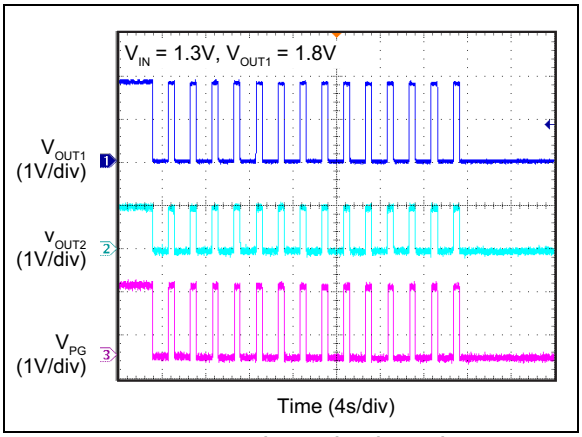


FIGURE 2-36: *Short-Circuit Cycles – V_{OUT1}.*

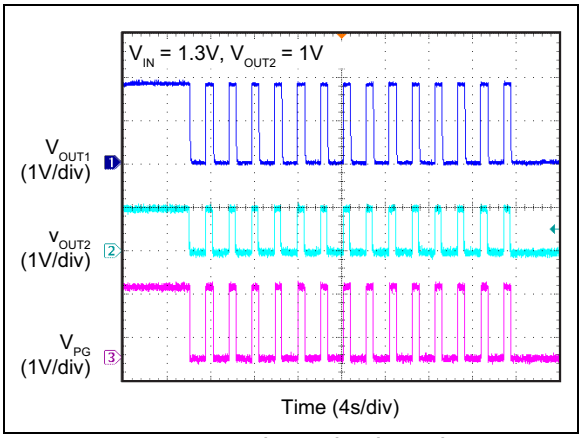


FIGURE 2-37: *Short-Circuit Cycles – V_{OUT2}.*

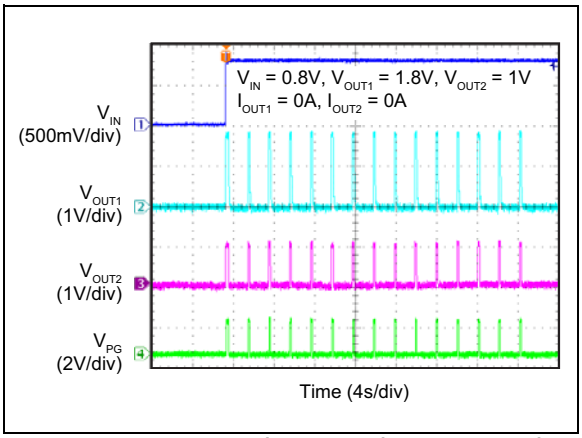


FIGURE 2-38: *Hiccup Cycles – V_{IN} Fault.*

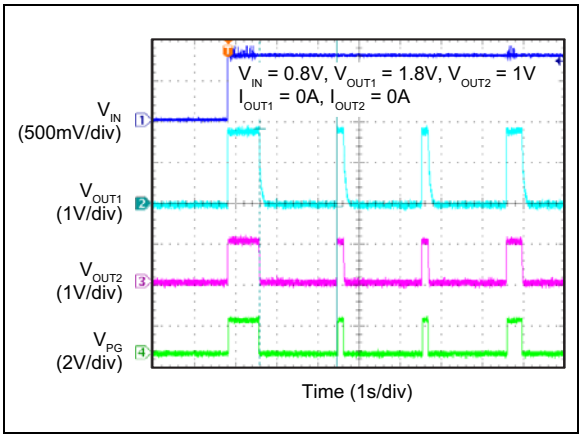


FIGURE 2-39: *Cool-Off Delay – V_{IN} Fault.*

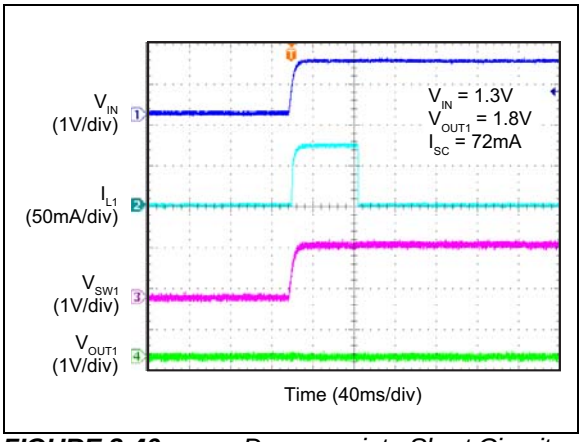


FIGURE 2-40: *Power-up into Short Circuit – V_{OUT1}.*

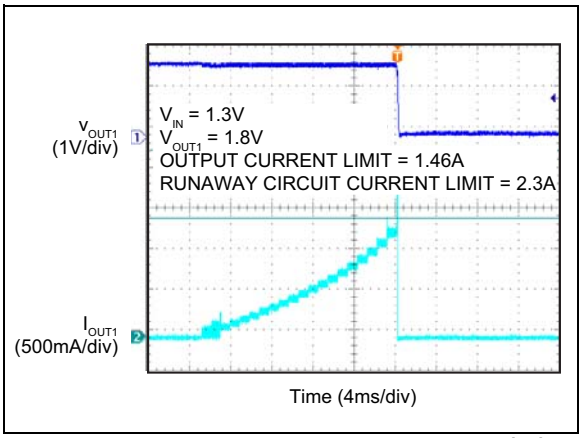


FIGURE 2-41: *Boost Output Current Limit – V_{OUT1}.*

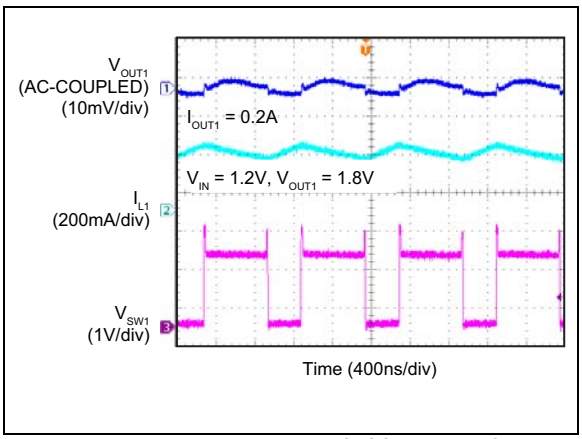


FIGURE 2-42: *Boost Switching Waveforms – 200 mA.*

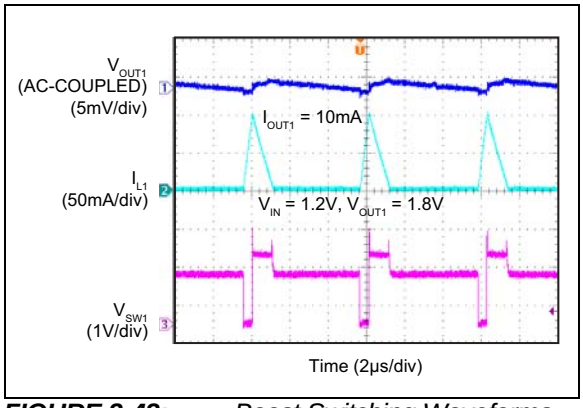


FIGURE 2-43: *Boost Switching Waveforms – 10 mA.*

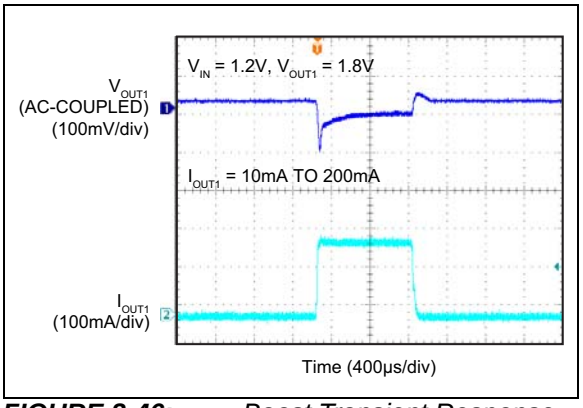


FIGURE 2-46: *Boost Transient Response.*

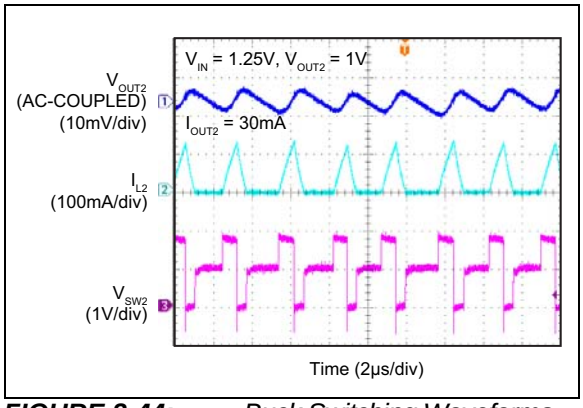


FIGURE 2-44: *Buck Switching Waveforms – 30 mA.*

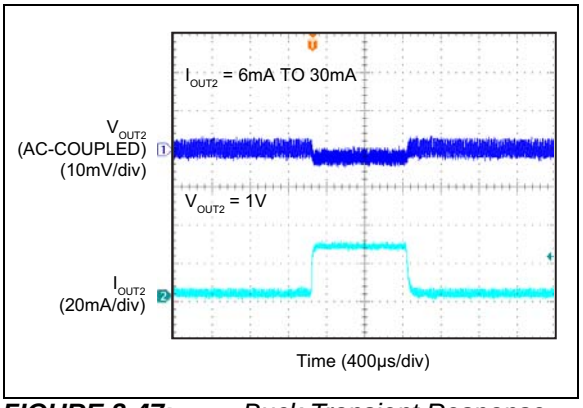


FIGURE 2-47: *Buck Transient Response.*

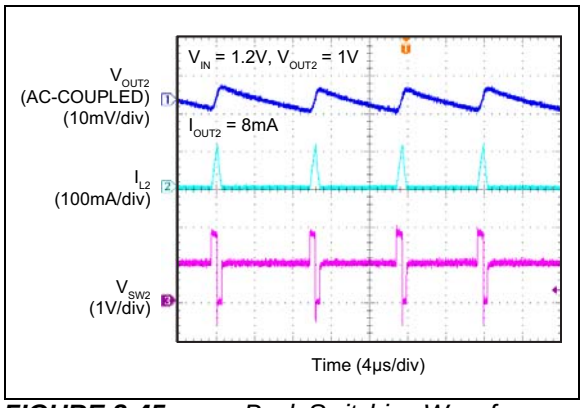


FIGURE 2-45: *Buck Switching Waveforms – 8 mA.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Pin Function
1	PGND1	Power Ground 1: The Power Ground for the synchronous boost DC/DC converter power stage.
2	V_{IN}	Battery Voltage Supply (Input): The internal circuitry operates from the battery voltage during start-up. Once V_{OUT1} exceeds V_{IN}, the bias current comes from V_{OUT1}. The start-up sequence is initiated once the battery voltage is above 0.9V. The boost output (V_{OUT1}) is powered up first, then the buck output (V_{OUT2}) follows. If the battery voltage falls below 0.85V for more than 15 cool-off cycles, both outputs are simultaneously turned off and an internal resistor discharges the output capacitors to 0V.
3	FB1	Feedback 1 (Input): Connect a resistor divider network to this pin to set the output voltage for the synchronous boost regulator. Resistors should be selected based on a nominal V_{FB1} = 0.6V.
4	NC	No Connect Pin (NC): Leave open, do not connect to ground.
5	PG	Power Good (Output): This is an open-drain, active-high output. When V_{IN}, V_{FB1} or V_{FB2} is below its nominal voltage, the Power Good output gets pulled low after a deglitch period. The PG pin will be pulled low without delay when the enable is set low.
6	EN	Enable (Input): A logic level control of both outputs. The EN pin is CMOS-compatible. Logic high = enable, logic low = shutdown. In the OFF state, the supply current of the device is greatly reduced (typically 1 µA). When the EN pin goes high, the start-up sequence is initiated. The boost output (V_{OUT1}) is powered up first, then the buck output (V_{OUT2}) follows. When EN goes low, both outputs are immediately turned off and the boost output (V_{OUT1}) is completely disconnected from the input voltage. Then, both converters' output capacitors are discharged to ground through an internal pull-down circuit. The EN pin has a 4 MΩ resistance to AGND.
7	LED	LED (Output): This is an open-drain output that is used for a low-battery indicator. Under normal conditions, the LED is always on. If the battery voltage is between 1.2V to 0.85V, the external LED will blink with a duty cycle of 25% at 0.25 Hz. The LED will be off if the battery voltage falls below 0.85V for more than 15 cool-off cycles or the EN pin is low.
8	AGND	Analog Ground: The Analog Ground for both regulator control loops.
9	FB2	Feedback 2 (Input): Connect a resistor divider network to this pin to set the output voltage for the synchronous buck regulator. Resistors should be selected based on a nominal V_{FB2} = 0.6V.
10	OUT2	Output Voltage 2 (Input): If the EN pin is low or the Power Good output is pulled low, an internal resistor discharges the V_{OUT2} output capacitance to 0V. Also, if the inductor current falls to zero, an internal anti-ringing switch is connected between the SW2 and OUT2 pins to minimize the Switch node ringing.
11	PGND2	Power Ground 2: The Power Ground for the synchronous buck DC/DC converter power stage.
12	SW2	Switch Pin 2 (Input): Inductor connection for the synchronous step-down regulator. Connect the inductor between V_{OUT2} and the SW2 pin. Due to the high-speed switching on this pin, the SW2 pin should be routed away from sensitive nodes, and trace length should be kept as short and wide as possible to reduce EMI. If the inductor current falls to zero or EN is low, then an internal anti-ringing switch is connected between the SW2 and V_{OUT2} pins to minimize the switch node ringing.
13	OUT1	Output 1 (Output): Output of the synchronous boost regulator and is the bias supply once V_{OUT1} is greater than V_{IN}. The boost output also serves as the supply input for the buck converter (V_{OUT2}). If the EN pin is low or the Power Good output is pulled low, an internal resistor discharges the V_{OUT1} output capacitance to 0V.
14	SW1	Switch Pin 1 (Input): Inductor connection for the synchronous boost regulator. Connect the inductor between V_{IN} and SW1. Due to the high-speed switching on this pin, the SW1 pin should be routed away from sensitive nodes, and trace length should be kept as short and wide as possible to reduce EMI. If the inductor current falls to zero, an internal anti-ringing switch is connected between the SW1 and V_{IN} pins to minimize the switch node ringing.
EP	GND	Exposed Pad (Power): Must make a full connection to a GND plane.

4.0 APPLICATION INFORMATION

4.1 Overview

The MIC23099 is a dual output voltage, power management IC (PMIC) that has excellent light load efficiency, which operates from a single cell battery. The PMIC has a synchronous boost regulator, a synchronous buck regulator, inrush current limiting, Fault detection, a low-battery monitor and warning circuitry. The synchronous boost output voltage (V_{OUT1}) is enabled first and is powered from the battery. Next, the synchronous buck output (V_{OUT2}), which is powered from the boost output voltage, is enabled. This configuration allows V_{OUT2} to be independent of the battery voltage, thereby allowing the buck output voltage to be higher or lower than the battery voltage.

The boost regulator is a Current mode PWM design that incorporates a high-efficiency PFM Light Load mode, while the buck operates in PFM mode with constant peak current control. The boost employs adaptive pulse-width control that minimizes output ripple and avoids output ripple chatter commonly found in conventional micropower boost regulators. In addition, the MIC23099 incorporates a frequency control scheme that minimizes switching noise in the audio band.

The MIC23099 has an integrated low-battery monitor function. The low-battery level is indicated by an external LED connected to the LED pin. The LED is on when the battery voltage is above the 1.2V threshold and flashes when the battery voltage falls below the threshold. In addition, a supervisor circuit monitors each output and asserts a Power Good signal when the sequencing is done or the Power Good output is pulled low when a Fault condition occurs.

4.2 Boost Regulator

The high-efficiency, micropower synchronous boost regulator operates from one alkaline or NiMH battery. It offers true output disconnect to achieve a shutdown quiescent current of less than 1.0 µA, extending battery life.

The boost regulator achieves high efficiency over a wide output current range by operating in either PWM or PFM mode. PFM mode provides the best efficiency at light loads and PWM mode at heavy loads. The operating mode is automatically selected according to output load conditions. In PWM mode, the switching frequency is 1.0 MHz, minimizing the solution footprint.

The Current mode PWM design is internally compensated, simplifying the design. Current mode provides excellent line and load regulation, as well as cycle-by-cycle current limiting.

Also, an inrush current-limiting feature is provided to reduce the inrush current, which minimizes the voltage droop on the battery when the device is turned on.

4.3 Buck Regulator

The buck converter is designed to operate in PFM mode with constant peak current control. When the buck regulator high-side switch turns on, the inductor current starts to rise. When the inductor current hits the current-limit threshold, an RS flip-flop is reset, turning off the high-side switch and turning on the low-side synchronous switch. The low-side switch will remain on until the inductor current falls to zero; at which time, it is turned off. Both switches will remain off until the cycle repeats itself when the buck feedback voltage falls below the internal 0.6V reference and the internal comparator sets the RS flip-flop Q output high.

4.4 Low-Battery Voltage Monitoring

The internal low input voltage monitor determines when the input voltage is below the internally set 1.2V (typical) threshold. When the input voltage falls below the internally set threshold, the external LED connected to the LED pin begins to blink at a frequency of 0.25 Hz with a duty cycle of 25%. The low input voltage threshold of 1.2V has a ±50 mV variation.

4.5 Anti-Ringing Control

Both the buck and boost converters have an anti-ringing control circuit that minimizes the ringing on the Switching node caused by the inductor, and the parasitic capacitance of the Switch node when the synchronous MOSFET turns off. When the inductor current falls to zero, an internal anti-ringing switch is connected across the inductor. This temporarily shorts the inductor and eliminates the ringing on the Switch node.

4.6 True Micropower Shutdown

This shutdown feature disconnects the boost output from the battery. This feature eliminates power draw from the battery through the synchronous switch during shutdown. In conventional boost regulators, there is a catch diode that provides a current path from the battery, through the inductor, to the output of the boost regulator that can draw current even when the regulator is shut down.

4.7 Power-up Sequencing

When the Enable pin (EN) voltage rises above the enable threshold voltage, the MIC23099 enters its start-up sequence. Initially, the boost converter high-side PMOS switch operates in Linear mode and emulates a current-limited switch until the Output Voltage, V_{OUT1}, reaches V_{IN}. Then, a fixed duty cycle clock controls the boost converter until V_{OUT1} reaches 1.6V. When V_{OUT1} is greater than 1.6V, the boost PFM control circuitry takes over until the output reaches its regulated voltage value.

When V_{OUT1} reaches 92.5% of its nominal value, V_{OUT2} is enabled. The Power Good output goes high, 10 ms to 50 ms, after V_{OUT2} reaches the programmed value. Figure 4-1 waveforms detail the circuits' operation.

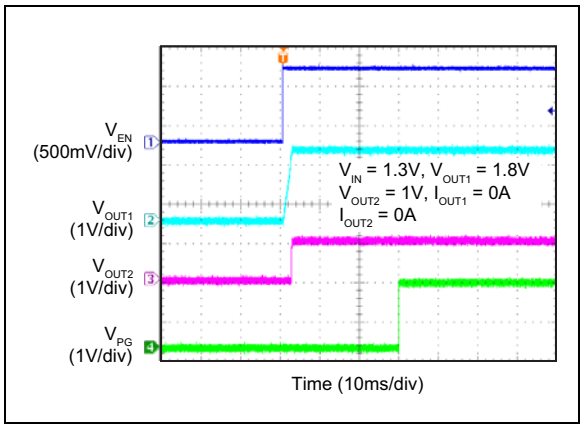


FIGURE 4-1: *Power-up Sequencing.*

4.8 Power Good (PG)

The Power Good (PG) circuitry monitors the battery voltage and Feedback pin voltage of the boost and buck regulators. The PG pin output goes logic high when the FB1 and FB2 pin voltages are both greater than 92.5% (typical) of the internal reference voltage, and the input voltage is greater than 0.85V (typical). To minimize false triggering, the Power Good output has both a turn-on delay and a falling deglitch delay.

4.9 Boost Switching Frequency

To reduce switching artifacts in the audio band, the buck and boost regulators' switching frequency is controlled to minimize overlap. Figure 4-2 shows the boost switching frequency versus the output load current and Figure 4-3 shows the buck switching frequency versus the output load current.

The boost regulator operates in either PWM or PFM mode. To avoid PWM to PFM chatter, the PWM entry and exit points are not the same. When in PFM mode, the output current needs to reach 90 mA to enter into PWM mode and exits at 30 mA. The boost switching frequency is greater than 100 kHz, with loads greater than 20 mW.

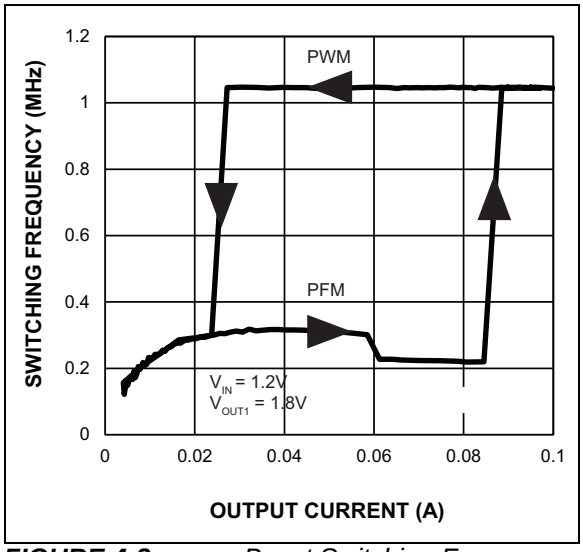


FIGURE 4-2: *Boost Switching Frequency vs. Output Current.*

4.10 Buck Switching Frequency

The buck converter is designed to operate in PFM mode only. It has peak current control, which turns off the high-side switch when the inductor current hits the current-limit threshold. The cycle repeats itself when the output voltage falls below its regulated value. As a result, the switching frequency varies linearly with output current, as shown in Figure 4-3. The buck switching frequency is greater than 80 kHz with loads greater than 8 mW.

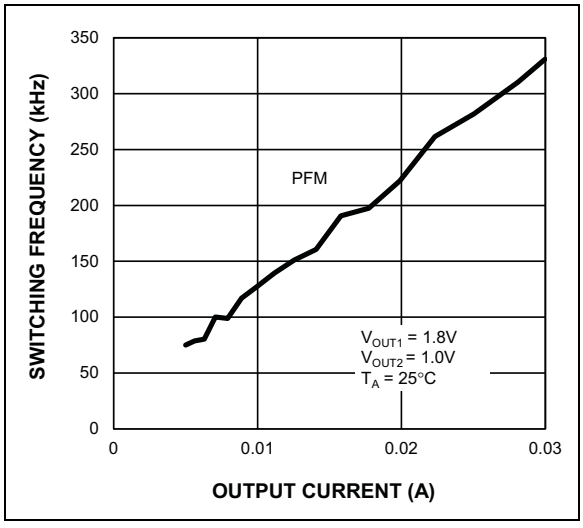


FIGURE 4-3: *Buck Switching Frequency vs. Output Current.*

4.11 Low-Battery Detection and Output Latch-Off

Figure 4-4 shows the low-battery power cycling operation. If the battery voltage (V_{IN}) drops below 0.85V for more than 100 ms to 150 ms, the PG deasserts (goes low) and outputs, V_{OUT1} and V_{OUT2}, are disabled. Then, the 500Ω active discharge resistors are enabled and discharge V_{OUT1} and V_{OUT2} to ground. Finally, the MIC23099 enters a cool-off or Sleep period. After a cool-off period of about 1.3 seconds, if the battery voltage is above the 0.85V threshold, then the outputs will power up again. This cycle repeats itself until the end of the 15th cycle, when both outputs are latched off for the last time.

The outputs can be turned back on by recycling the input power or by toggling the Enable pin. If the battery voltage is still low, the MIC23099 will turn itself off again after 15 power-up cycles.

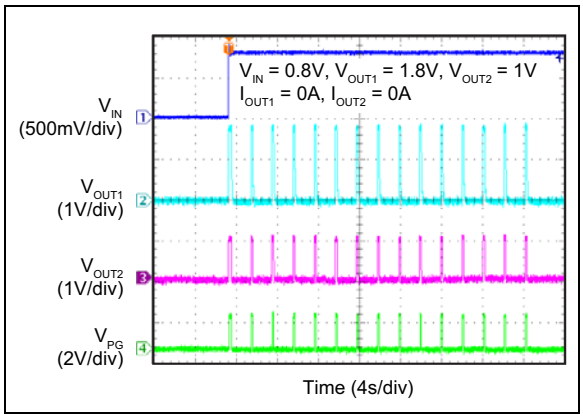


FIGURE 4-4: *Low-Battery Power Cycling.*

4.12 Output Fault and Power Cycling

If either the V_{OUT1} or V_{OUT2} output is out of tolerance for longer than the Power Good deglitch delay of between 60 ms to 120 ms, both outputs are disabled. The power-down procedure is the same as the low-battery Fault detection, as shown in Figure 4-5. The outputs can be turned back on by recycling the input power or by toggling the Enable pin. The latch-off feature eliminates the thermal stress on the MIC23099 and the external inductors during a Fault event.

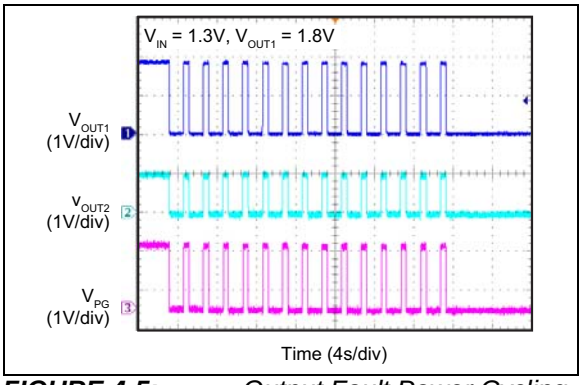


FIGURE 4-5: *Output Fault Power Cycling.*

4.13 Boost Short-Circuit Protection

The low-side current limit protects the IC from transient overload conditions, but not from a direct short to ground. The high-side MOSFET current limit provides the protection from a short to ground. In this Fault condition, the high-side PMOS switch operates in Linear mode and limits the current to approximately 80 mA. If the short-circuit condition lasts for more than 30 ms, the PMOS switch is latched off, as shown in Figure 4-6. The outputs are not re-enabled until the input power is recycled or the Enable pin is toggled.

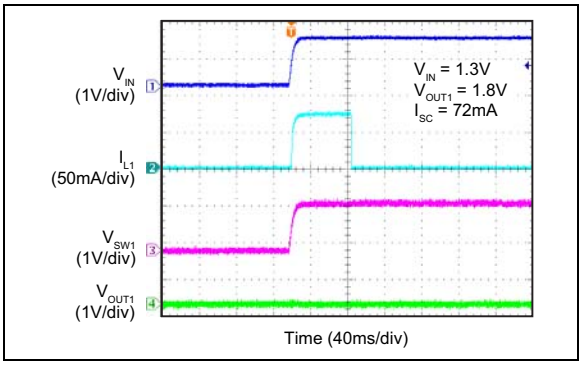


FIGURE 4-6: *Power-up into Short Circuit.*

4.14 Boost Overcurrent Protection

The boost converter has current-limit protection on both the high-side and low-side MOSFETs. The low-side MOSFET provides cycle-by-cycle current limiting. When the peak switch current exceeds the NMOS current-limit threshold, the low-side switch is immediately turned off and the high-side switch is turned on. Peak switch current is limited to approximately 1.5A. The low-side switch is allowed to turn on again on the next clock cycle. If the overload condition lasts more than 60 ms to 120 ms, both outputs are disabled and the IC enters its Power Cycling mode.

5.0 COMPONENT SELECTION

5.1 Resistors

An external resistive divider network (R1 and R2), with its center tap connected to the Feedback pin, sets the output voltage for each regulator. R1 is the top resistor and R2 is the bottom resistor in the divider string. The resistor values for the desired output voltage are calculated as illustrated in Equation 5-1. Large resistor values are recommended to reduce light load operating current and improve efficiency. The recommended resistor value for R1 should be around: $R_{top} \approx 150\ k\Omega$.

EQUATION 5-1: CALCULATING RESISTOR VALUES FOR THE OUTPUT VOLTAGE

$$R_{bot} = \frac{R_{top}}{\left(\frac{V_{OUT}}{0.6V} - 1\right)}$$

EXAMPLE 5-1:

$V_{OUT1} = 1.8V$
$V_{OUT2} = 1.0V$
R1 = 150 kΩ
R2 = 75 kΩ
R3 = 150 kΩ
R4 = 220 kΩ

EXAMPLE 5-2:

$V_{OUT1} = 3.3V$
$V_{OUT2} = 1.8V$
R1 = 150 kΩ
R2 = 33 kΩ
R3 = 150 kΩ
R4 = 75 kΩ

In the case of the boost converter, Equation 5-1 sets the output voltage to its PWM value, as shown in Figure 5-1. The no load PFM output voltage is 2% higher than the PWM value. This higher PFM output voltage value is necessary to prevent PFM to PWM mode skipping, which can introduce noise into the audio band.

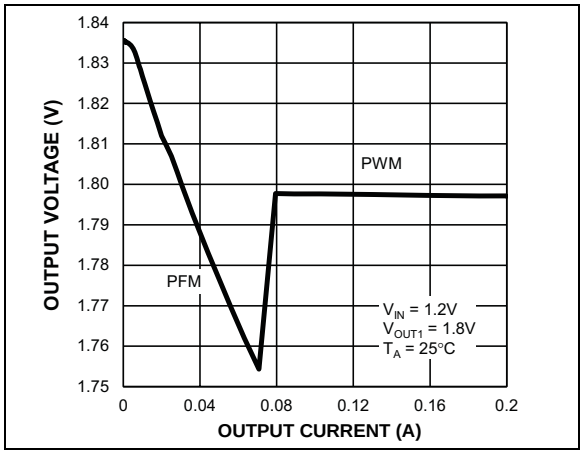


FIGURE 5-1: *Boost Load Regulation.*

Figure 5-2 shows the buck load regulation.

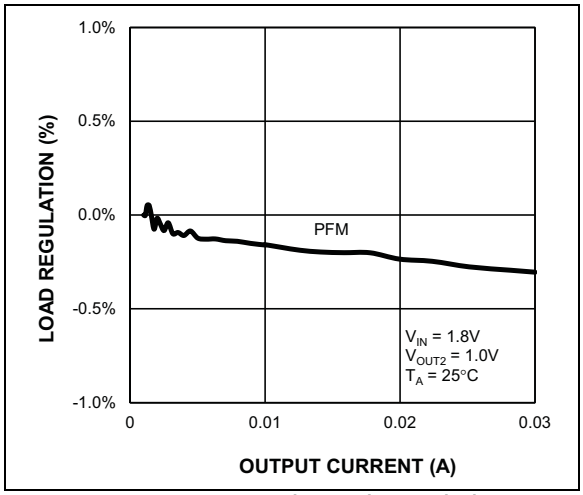


FIGURE 5-2: *Buck Load Regulation.*

5.2 Inductor

Inductor selection is a balance between efficiency, cost, size, switching frequency and rated current. For most applications, inductors in the range 4.7 µH to 6.8 µH are recommended. Larger inductance values reduce the peak-to-peak ripple current, thereby reducing both the DC losses and AC losses for better efficiency. The inductor's DC Resistance (DCR) also plays an important role. Since the majority of the input current (minus the MIC23099 operating current) is passed through the inductor, higher DCR inductors will reduce efficiency at higher load currents.

The switch current limit for the MIC23099 is typically 1.5A. The saturation current rating of the selected inductor should be 20-30% higher than the current-limit specification for the respective regulator.

5.3 Input Capacitor

The step-up converter exhibits a triangular, or sawtooth, current waveform at its input, so an input capacitor is required to decouple this waveform and thereby reduce the input voltage ripple. A 4.7 µF to 10 µF ceramic capacitor should be sufficient for most applications. A minimum input capacitance of 1 µF is recommended. The input capacitor should be as close as possible to the inductor, V_{IN} pin and PGND1 pin of the MIC23099. Short, and wide PCB traces are good for noise performance.

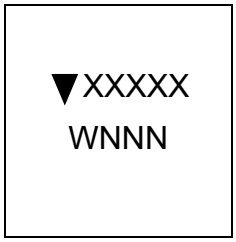
5.4 Output Capacitor

Output capacitor selection is also a trade-off between performance, size and cost. Increasing the output capacitor will lead to an improved transient response performance. X5R and X7R ceramic capacitors are recommended. For most applications, 10 µF to 47 µF should be sufficient.

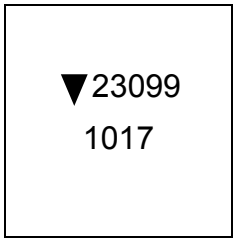
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

14-Lead 2.5 mm x 2.5 mm FTQFN



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

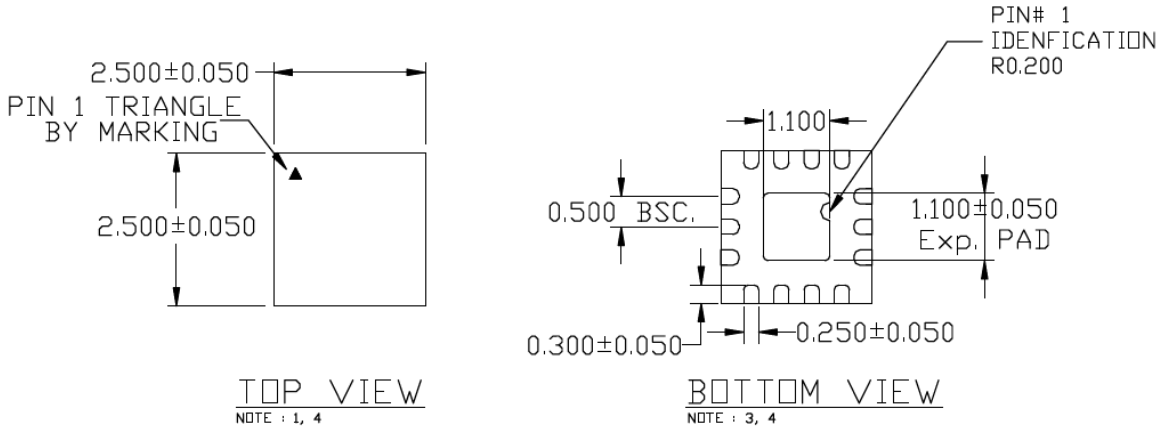
Underbar (_) and/or Overbar (¯) symbol may not be to scale.

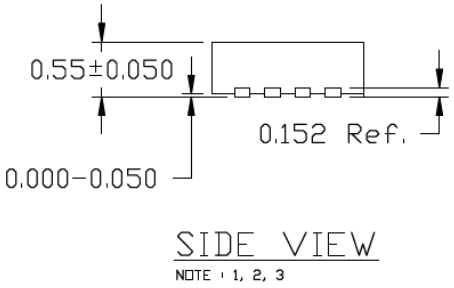
6.2 Package Details

The following sections give the technical details of the packages.

TITLE
14 LEAD FTQFN 2.5x2.5mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

DRAWING #	FTQFN2525-14LD-PL-1	UNIT	MM



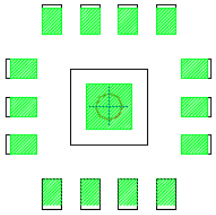


NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.08 mm.
3. MAXIMUM ALLOWABE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID WILL BE LASER MARKED.
5. RED CIRCLE INDICATE THERMAL VIA. SIZE IS 0.300-0.350 mm IN DIAMETER AND SHOULD BE CONNECTED TO GND PLANE FOR MAXIMUM THERMAL PERFORMANCE.

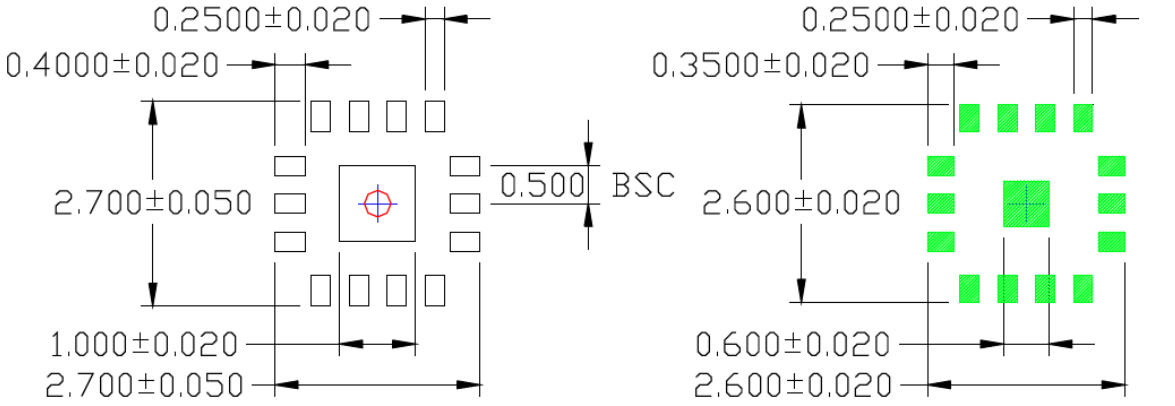
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

RECOMMENDED LAND PATTERN

NOTE : 5



STACKED-UP



EXPOSED METAL TRACE

SOLDER STENCIL OPENING

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (December 2016)

- Converted Micrel document MIC23099 to Microchip data sheet DS20005684A.
- Minor text changes throughout document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–	X	XXX	–	XX
Device		Option	Package		Media Type

Device:	MIC23099:	Single AA/AAA Cell Step-up/Step-Down Regulators with Battery Monitoring
Package:	YFT =	14-Pin 2.5 mm x 2.5 mm FTQFN
Media Type:	T5 =	500/Reel
	TR =	5,000/Reel

Examples:

a) MIC23099YFT-T5: MIC23099, 14-Pin FTQFN, 500/Reel

b) MIC23099YFT-TR: MIC23099, 14-Pin FTQFN, 5,000/Reel

NOTES:

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