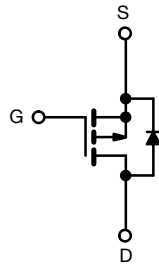




**THE DATASHEET OF
IRFR9010TRLPBF**



Power MOSFET



P-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- Repetitive avalanche ratings
- Surface-mount (IRFR9010, SiHFR9010)
- Straight lead (IRFU9010, SiHFU9010)
- Simple drive requirements
- Ease of paralleling
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

The power MOSFET technology is the key to Vishay's advanced line of power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The power MOSFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface-mount package brings the advantages of power MOSFETs to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9010, SiHFR9010 is provided on 16 mm tape. The straight lead option IRFU9010, SiHFU9010 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, DC/DC converters, and a wide range of consumer products.

PRODUCT SUMMARY	
V _{DS} (V)	-50
R _{DS(on)} (Ω)	V _{GS} = -10 V 0.50
Q _g (Max.) (nC)	9.1
Q _{gs} (nC)	3.0
Q _{gd} (nC)	5.9
Configuration	Single

ORDERING INFORMATION				
Package	DPAK (TO-252)	DPAK (TO-252)	DPAK (TO-252)	IPAK (TO-251)
Lead (Pb)-free and halogen-free	SiHFR9010-GE3	SiHFR9010TR-GE3 ^a	SiHFR9010TRL-GE3 ^a	SiHFU9010-GE3
Lead (Pb)-free	IRFR9010PbF	IRFR9010TRPbF ^a	IRFR9010TRLPbF ^a	IRFU9010PbF

Note

a. See device orientation

ABSOLUTE MAXIMUM RATINGS (T _C = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	-50	V
Gate-source voltage		V _{GS}	± 20	
Continuous drain current	V _{GS} at -10 V	I _D	T _C = 25 °C	-5.3
			T _C = 100 °C	-3.3
Pulsed drain current ^a		I _{DM}	-21	A
Linear derating factor			0.20	
Single pulse avalanche energy ^b		E _{AS}	136	mJ
Drain-source voltage		I _{AR}	-5.3	A
Maximum power dissipation	T _C = 25 °C	E _{AR}	2.5	mJ
Maximum power dissipation (PCB mount) ^e	T _A = 25 °C	P _D	25	W
Peak diode recovery dV/dt ^c		dV/dt	5.8	V/ns
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) ^d	For 10 s		300	

Notes

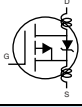

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14)
- V_{DD} = - 25 V, starting T_J = 25 °C, L = 9.7 mH, R_g = 25 Ω, peak I_L = - 5.3 A
- I_{SD} ≤ - 5.3 A, dI/dt ≤ - 80 A/μs, V_{DD} ≤ 40 V, T_J ≤ 150 °C, suggested R_g = 24 Ω
- 0.063" (1.6 mm) from case



THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R _{thJA}	-	-	110	°C/W
Case-to-sink	R _{thCS}	-	1.7	-	
Maximum junction-to-case (drain) ^a	R _{thJC}	-	-	5.0	

Note

a. Mounting pad must cover heatsink surface area

SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA		- 50	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA		- 2.0	-	- 4.0	V
Gate-source leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 500	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = max. rating, V _{GS} = 0 V		-	-	- 250	μA
		V _{DS} = 0.8 x max. rating, V _{GS} = 0 V, T _J = 125		-	-	- 1000	
Drain-source on-state resistance	R _{DS(on)}	V _{GS} = - 10 V	I _D = - 2.8 A ^b	-	0.35	0.5	Ω
Forward transconductance	g _{fs}	V _{DS} ≤ - 50 V, I _{DS} = - 2.8 A		1.1	1.7	-	S
Dynamic							
Input capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = - 25 V, f = 1.0 MHz, see fig. 9		-	240	-	pF
Output capacitance	C _{oss}			-	160	-	
Reverse transfer capacitance	C _{rss}			-	30	-	
Total gate charge	Q _g	V _{GS} = - 10 V	I _D = - 4.7 A, V _{DS} = 0.8 x max. rating, see fig. 16 (Independent operating temperature)	-	6.1	9.1	nC
Gate-source charge	Q _{gs}			-	2.0	3.0	
Gate-drain charge	Q _{gd}			-	3.9	5.9	
Turn-on delay time	t _{d(on)}	V _{DD} = - 25 V, I _D = - 4.7 A, R _g = 24 Ω, R _D = 5.6 Ω, see fig. 15 (Independent operating temperature)		-	6.1	9.2	ns
Rise time	t _r			-	47	71	
Turn-off delay time	t _{d(off)}			-	13	20	
Fall time	t _f			-	35	59	
Internal drain inductance	L _D	Between lead, 6 mm (0.25") from package and center of die contact. 		-	4.5	-	nH
Internal source inductance	L _S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	- 5.3	A
Pulsed diode forward current ^a	I _{SM}			-	-	- 18	
Body diode voltage	V _{SD}	T _J = 25 °C, I _S = - 5.3 A, V _{GS} = 0 V ^b		-	-	- 5.5	V
Body diode reverse recovery time	t _{rr}	T _J = 25 °C, I _F = - 4.7 A, di/dt = 100 A/μs ^b		33	75	160	ns
Body diode reverse recovery charge	Q _{rr}			0.090	0.22	0.52	μC
Forward turn-on time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 14)
- b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

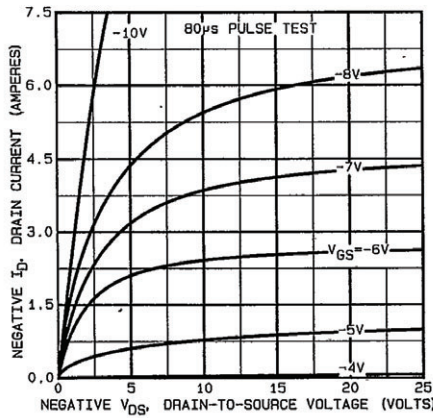


Fig. 1 - Typical Output Characteristics

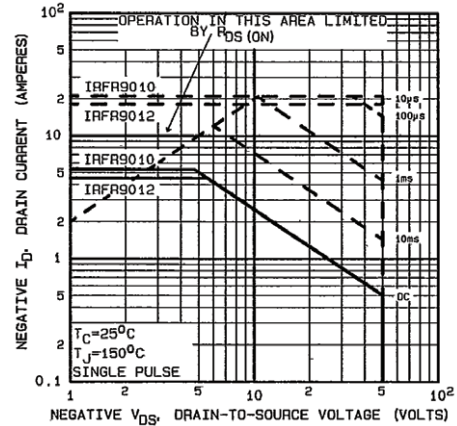


Fig. 3 - Maximum Safe Operating Area

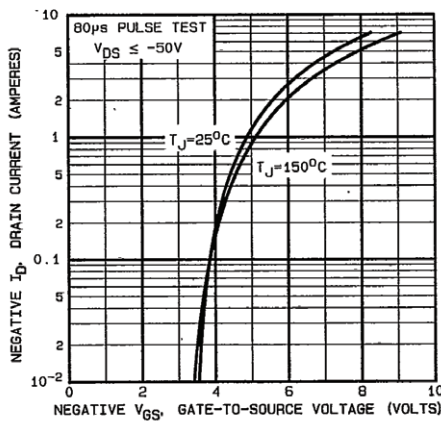


Fig. 1 - Typical Transfer Characteristics

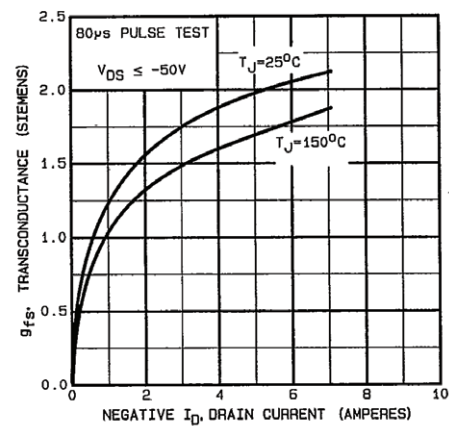


Fig. 4 - Typical Transconductance vs. Drain Current

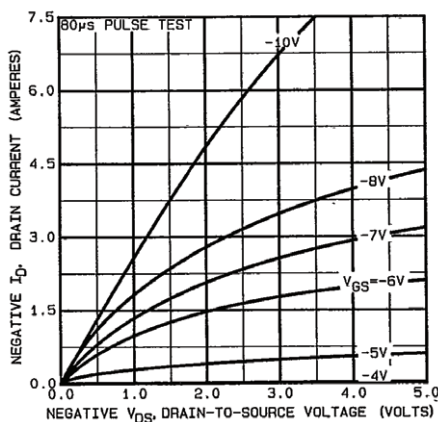


Fig. 2 - Typical Saturation Characteristics

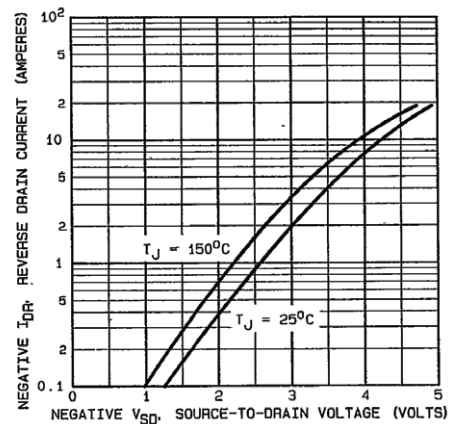


Fig. 5 - Typical Source-Drain Diode Forward Voltage

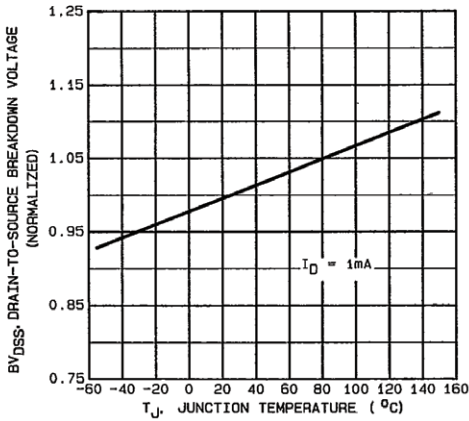


Fig. 6 - Breakdown Voltage vs. Temperature

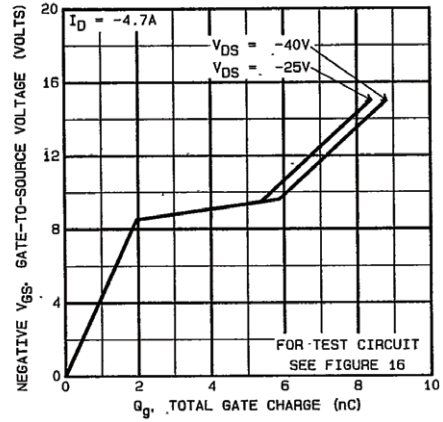


Fig. 9 - Typical Gate Charge vs. Gate-to-Source Voltage

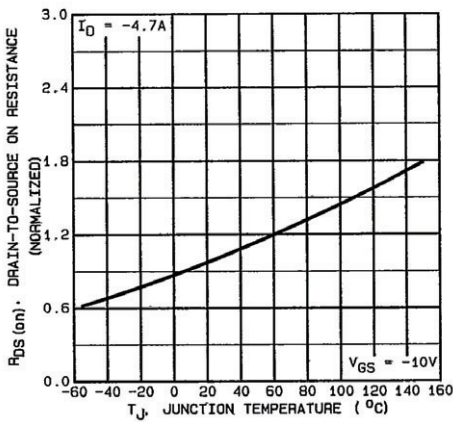


Fig. 7 - Normalized On-Resistance vs. Temperature

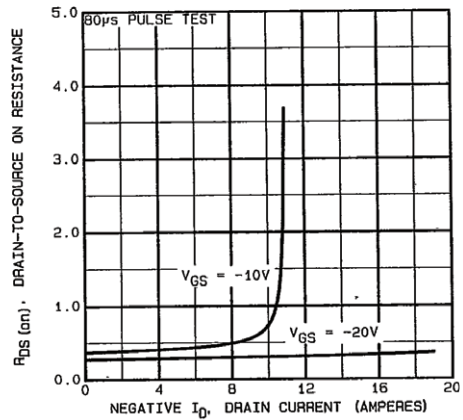


Fig. 10 - Typical On-Resistance vs. Drain Current

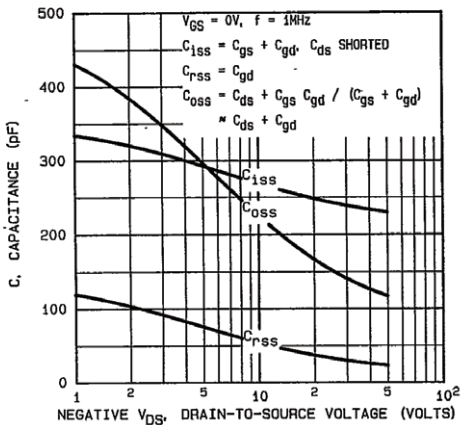


Fig. 8 - Typical Capacitance vs. Drain-to-Source Voltage

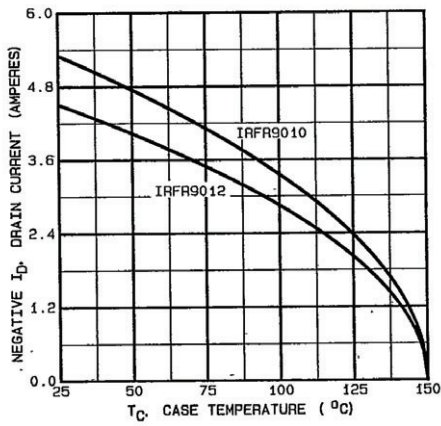


Fig. 11 - Maximum Drain Current vs. Case Temperature

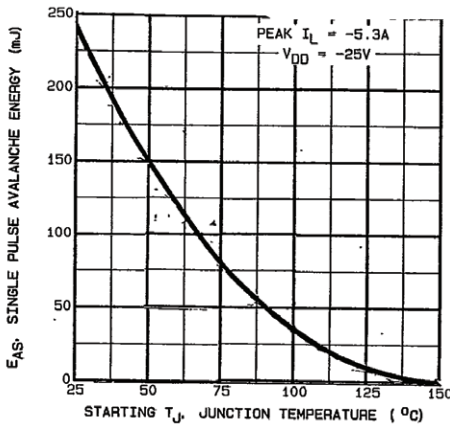


Fig. 2a - Maximum Avalanche vs. Starting Junction Temperature

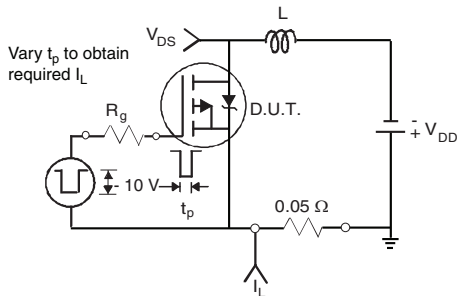


Fig. 13b - Unclamped Inductive Test Circuit

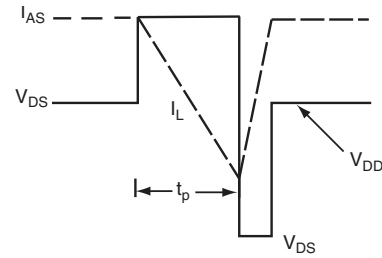


Fig. 13c - Unclamped Inductive Waveforms

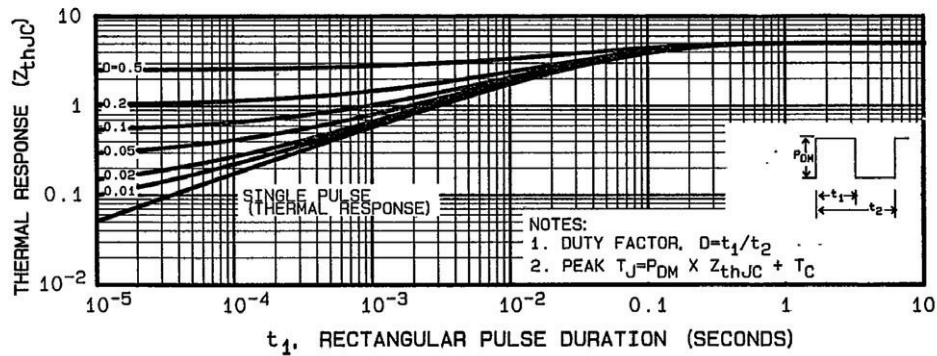


Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case vs. Pulse Duration

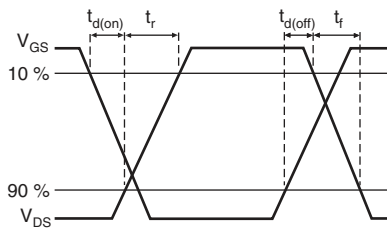


Fig. 14a - Switching Time Waveforms

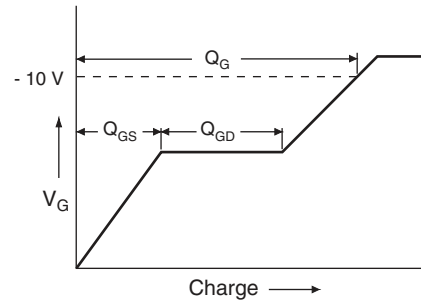


Fig. 16a - Basic Gate Charge Waveform

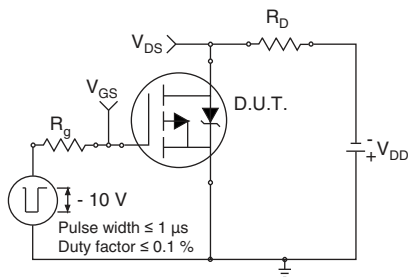


Fig. 15b - Switching Time Test Circuit

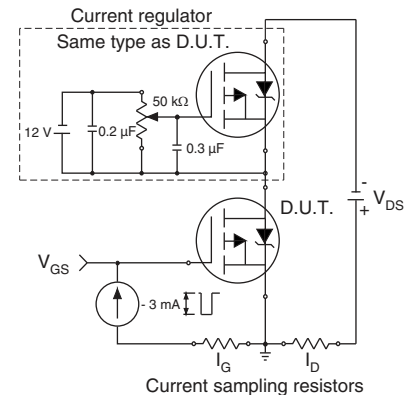
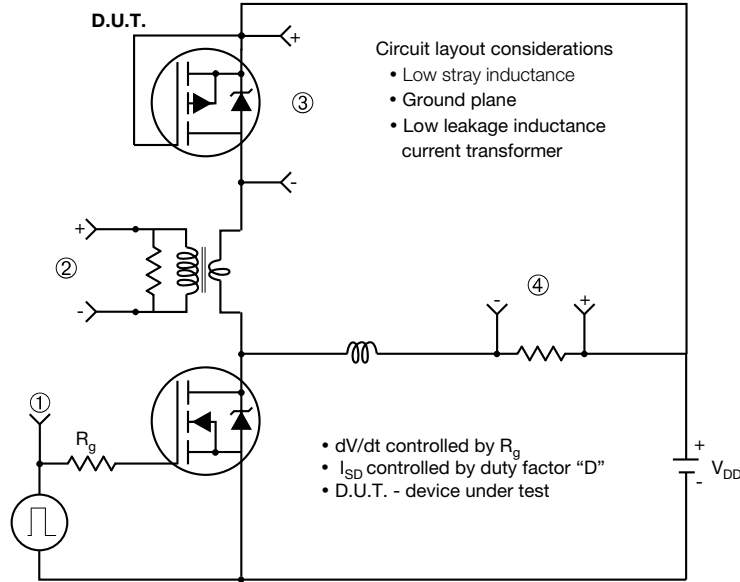
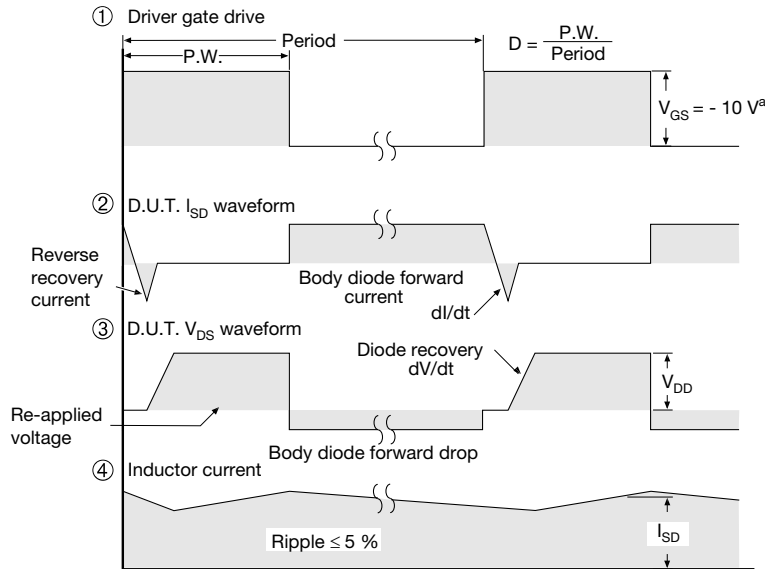


Fig. 16b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



Note
• Compliment N-Channel of D.U.T. for driver



Note
a. $V_{GS} = -5\text{ V}$ for logic level and -3 V drive devices

Fig. 17 - For P-Channel

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TO-252AA Case Outline

VERSION 1: FACILITY CODE = Y



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.38
A1	-	0.127
b	0.64	0.88
b2	0.76	1.14
b3	4.95	5.46
C	0.46	0.61
C2	0.46	0.89
D	5.97	6.22
D1	4.10	-
E	6.35	6.73
E1	4.32	-
H	9.40	10.41
e	2.28 BSC	
e1	4.56 BSC	
L	1.40	1.78
L3	0.89	1.27
L4	-	1.02
L5	1.01	1.52

Note

- Dimension L3 is for reference only



VERSION 2: FACILITY CODE = N



MILLIMETERS		
DIM.	MIN.	MAX.
A	2.18	2.39
A1	-	0.13
b	0.65	0.89
b1	0.64	0.79
b2	0.76	1.13
b3	4.95	5.46
c	0.46	0.61
c1	0.41	0.56
c2	0.46	0.60
D	5.97	6.22
D1	5.21	-
E	6.35	6.73
E1	4.32	-
e	2.29 BSC	
H	9.94	10.34

MILLIMETERS		
DIM.	MIN.	MAX.
L	1.50	1.78
L1	2.74 ref.	
L2	0.51 BSC	
L3	0.89	1.27
L4	-	1.02
L5	1.14	1.49
L6	0.65	0.85
θ	0°	10°
θ1	0°	15°
θ2	25°	35°

Notes

- Dimensioning and tolerance confirm to ASME Y14.5M-1994
- All dimensions are in millimeters. Angles are in degrees
- Heat sink side flash is max. 0.8 mm
- Radius on terminal is optional

ECN: E22-0399-Rev. R, 03-Oct-2022
 DWG: 5347

Case Outline for TO-251AA (High Voltage)

OPTION 1:



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1	0.89	1.14	0.035	0.045
b	0.64	0.89	0.025	0.035
b1	0.65	0.79	0.026	0.031
b2	0.76	1.14	0.030	0.045
b3	0.76	1.04	0.030	0.041
b4	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c1	0.41	0.56	0.016	0.022
c2	0.46	0.86	0.018	0.034
D	5.97	6.22	0.235	0.245

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
e	2.29 BSC		2.29 BSC	
L	8.89	9.65	0.350	0.380
L1	1.91	2.29	0.075	0.090
L2	0.89	1.27	0.035	0.050
L3	1.14	1.52	0.045	0.060
θ1	0°	15°	0°	15°
θ2	25°	35°	25°	35°

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- Dimension are shown in inches and millimeters
- Dimension D and E do not include mold flash. Mold flash shall not exceed 0.13 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- Thermal pad contour optional with dimensions b4, L2, E1 and D1
- Lead dimension uncontrolled in L3
- Dimension b1, b3 and c1 apply to base metal only
- Outline conforms to JEDEC® outline TO-251AA



OPTION 2: FACILITY CODE = N



DIM.	MIN.	NOM.	MAX.
A	2.180	2.285	2.390
A1	0.890	1.015	1.140
b	0.640	0.765	0.890
b1	0.640	0.715	0.790
b2	0.760	0.950	1.140
b3	0.760	0.900	1.040
b4	4.950	5.205	5.460
c	0.460	-	0.610
c1	0.410	-	0.560
c2	0.460	-	0.610
D	5.970	6.095	6.220
D1	4.300	-	-

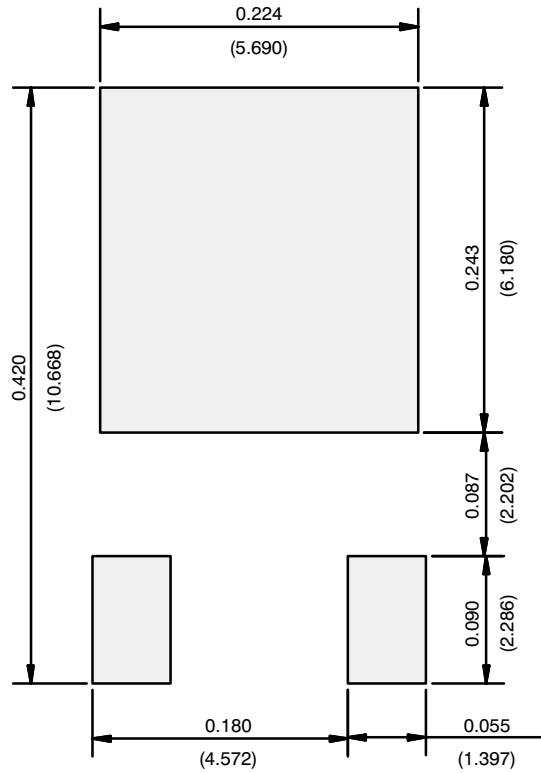
DIM.	MIN.	NOM.	MAX.
D2	5.380	-	-
E	6.350	6.540	6.730
E1	4.32	-	-
e	2.29 BSC		
L	8.890	9.270	9.650
L1	1.910	2.100	2.290
L2	0.890	1.080	1.270
L3	1.140	1.330	1.520
L4	1.300	1.400	1.500
theta 1	0°	7.5°	15°
theta 2	4°	-	-

ECN: E21-0682-Rev. C, 27-Dec-2021
DWG: 5968

Notes

- Dimensioning and tolerancing per ASME Y14.5M-1994
- All dimension are in millimeters, angles are in degrees
- Heat sink side flash is max. 0.8 mm

RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

[Return to Index](#)



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