



**THE DATASHEET OF
ADS7809U/1KG4**





16-Bit 10 μ s Serial CMOS Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

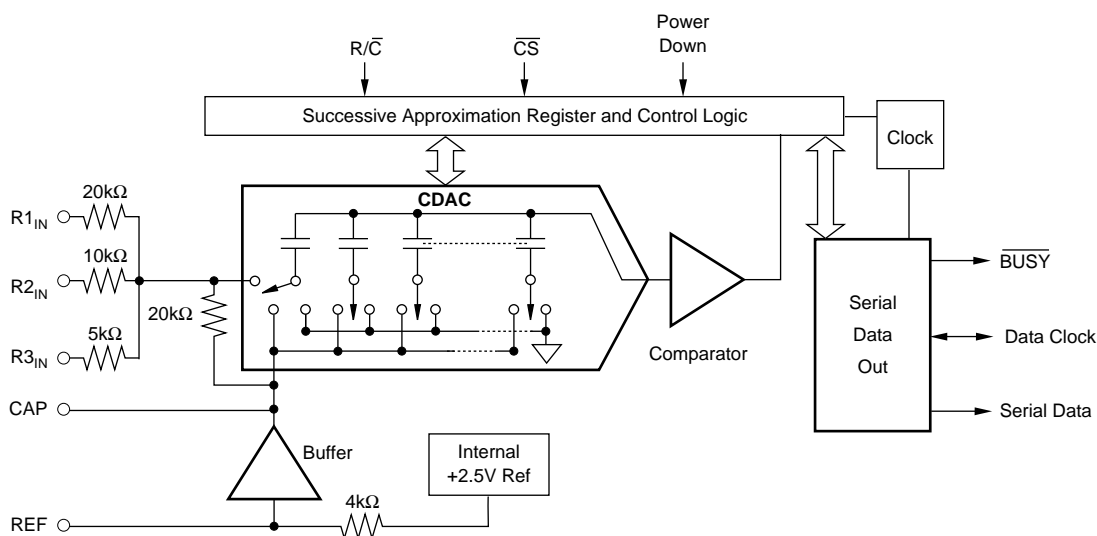
- 100kHz SAMPLING RATE
- 86dB SINAD WITH 20kHz INPUT
- ± 2 LSB INL
- DNL: 16 Bits No Missing Codes
- SIX SPECIFIED INPUT RANGES
- SERIAL OUTPUT
- SINGLE +5V SUPPLY OPERATION
- PIN-COMPATIBLE WITH 12-BIT ADS7808
- USES INTERNAL OR EXTERNAL REFERENCE
- 100mW MAX POWER DISSIPATION
- 0.3" SO-20
- SIMPLE DSP INTERFACE

DESCRIPTION

The ADS7809 is a complete 16-bit sampling Analog-to-Digital (A/D) converter using state-of-the-art CMOS structures. It contains a 16-bit capacitor-based Successive Approximation Register (SAR) A/D converter with sample-and-hold, reference, clock, and a serial data interface. Data can be outputted using the internal clock, or can be synchronized to an external data clock. The ADS7809 also provides an output synchronization pulse for ease of use with standard DSP processors.

The ADS7809 is specified at a 100kHz sampling rate, and specified over the full temperature range. Laser-trimmed scaling resistors provide various input ranges including ± 10 V and 0V to 5V, while an innovative design operates from a single +5V supply, with power dissipation under 100mW.

The ADS7809 is available in a 0.3" SO-20, and is fully specified for operation over the industrial -40°C to $+85^{\circ}\text{C}$ range.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Analog Inputs: R1 _{IN}	±25V
R2 _{IN}	±25V
R3 _{IN}	±25V
REF	V _{ANA} + 0.3V to AGND2 – 0.3V
CAP	Indefinite Short to AGND2, Momentary Short to V _{ANA}
Ground Voltage Differences: DGND, AGND2	±0.3V
V _{ANA}	7V
V _{DIG} to V _{ANA}	+0.3
V _{DIG}	7V
Digital Inputs	–0.3V to V _{DIG} + 0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	700mW
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	MAXIMUM LINEARITY ERROR (LSB)	NO MISSING CODE LEVEL (LSB)	MINIMUM SIGNAL-TO-(NOISE + DISTORTION) RATIO (dB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7809U	±3	15	83	SO-20	DW	–40°C to +85°C	ADS7809U	ADS7809U	Rail, 38
"	"	"	"	"	"	"	"	ADS7809U/1K	Tape and Reel, 1000
ADS7809UB	±2	16	86	"	"	"	ADS7809UB	ADS7809UB	Rail, 38
"	"	"	"	"	"	"	"	ADS7809UB/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ELECTRICAL CHARACTERISTICS

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors (see Figure 4), unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U			ADS7809UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION				16			*	Bits
ANALOG INPUT Voltage Ranges Impedance Capacitance				±10, 0V to 5V, etc. (See Table I) See Table I			*	pF
THROUGHPUT SPEED Complete Cycle Throughput Rate	Acquire and Convert	100		10	*		*	μs kHz
DC ACCURACY Integral Linearity Error Differential Linearity Error No Missing Codes Transition Noise ⁽²⁾ Full-Scale Error ^(3,4) Full-Scale Error Drift Full-Scale Error ^(3,4) Full-Scale Error Drift Bipolar Zero Error ⁽³⁾ Bipolar Zero Error Drift Unipolar Zero Error ⁽³⁾ Unipolar Zero Error ⁽³⁾ Unipolar Zero Error Drift Recovery to Rated Accuracy after Power-Down Power-Supply Sensitivity ($V_{\text{DIG}} = V_{\text{ANA}} = V_{\text{D}}$)	Ext. 2.5000V Ref Ext. 2.5000V Ref Bipolar Ranges Bipolar Ranges 0V to 10V Ranges 0V to 4V, 0V to 5V Ranges Unipolar Ranges 1μF Capacitor to CAP +4.75V < V_{D} < +5.25V	15	1.3	±3 +3, -2 ±0.5 ±0.5 ±10 ±5 ±3 ±8	16	*	±2 ±1 *	LSB ⁽¹⁾ LSB Bits LSB % ppm/°C % ppm/°C mV ppm/°C mV mV ppm/°C ms LSB
AC ACCURACY Spurious-Free Dynamic Range Total Harmonic Distortion Signal-to-(Noise + Distortion) Signal-to-Noise Full-Power Bandwidth ⁽⁶⁾	$f_{\text{IN}} = 20\text{kHz}$ $f_{\text{IN}} = 20\text{kHz}$ $f_{\text{IN}} = 20\text{kHz}$ -60dB Input $f_{\text{IN}} = 20\text{kHz}$	90	100 -100	-90	96	*	*	dB ⁽⁵⁾ dB dB dB kHz
SAMPLING DYNAMICS Aperture Delay Transient Response Overvoltage Recovery ⁽⁷⁾	FS Step		40	2		*	*	ns μs ns
REFERENCE Internal Reference Voltage Internal Reference Source Current (Must use external buffer) External Reference Voltage Range For Specified Linearity External Reference Current Drain	No Load Ext. 2.5000V Ref	2.48	2.5 1	2.52	*	*	*	V μA V μA
DIGITAL INPUTS Logic Levels V_{IL} $V_{\text{IH}}^{(8)}$ I_{IL} I_{IH}	$V_{\text{IL}} = 0\text{V}$ $V_{\text{IH}} = 5\text{V}$	-0.3 +2.0		+0.8 $V_{\text{D}} + 0.3\text{V}$ ±10 ±10	*	*	*	V V μA μA

ELECTRICAL CHARACTERISTICS (Cont.)

At $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $f_S = 100\text{kHz}$, $V_{\text{DIG}} = V_{\text{ANA}} = +5\text{V}$, using internal reference and fixed resistors as shown in Figure 4, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7809U			ADS7809UB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL OUTPUTS								
Data Format								
Data Co								
Pipeline Delay								
Data Clock								
Internal (Output Only When Transmitting Data)	EXT/ $\overline{\text{INT}}$ LOW		2.3			*		MHz
External (Can Run Continually)	EXT/ $\overline{\text{INT}}$ HIGH	0.1		10	*		*	MHz
V_{OL}	$I_{\text{SINK}} = 1.6\text{mA}$			+0.4			*	V
V_{OH}	$I_{\text{SOURCE}} = 500\mu\text{A}$	+4			*		*	V
Leakage Current	High-Z State, $V_{\text{OUT}} = 0\text{V}$ to V_{DIG}			± 5			*	μA
Output Capacitance	High-Z State			15			*	pF
POWER SUPPLIES								
Specified Performance	Must be $\leq V_{\text{ANA}}$	+4.75	+5	+5.25	*	*	*	V
V_{DIG}		+4.75	+5	+5.25	*	*	*	V
V_{ANA}			0.3			*		mA
I_{DIG}			16			*		mA
I_{ANA}				100		*	*	mW
Power Dissipation: PWRD LOW	$V_{\text{ANA}} = V_{\text{DIG}} = 5\text{V}$, $f_S = 100\text{kHz}$					*	*	mW
Power Dissipation: PWRD HIGH			50			*	*	μW
TEMPERATURE RANGE								
Specified Performance		-40		+85	*		*	$^{\circ}\text{C}$
Derated Performance		-55		+125	*		*	$^{\circ}\text{C}$
Storage		-65		+150	*		*	$^{\circ}\text{C}$
Thermal Resistance (θ_{JA})								$^{\circ}\text{C}/\text{W}$
SO			75			*		

* Same as specification for ADS7809U.

NOTES: (1) LSB means Least Significant Bit. For the $\pm 10\text{V}$ input range, one LSB is $305\mu\text{V}$.

(2) Typical rms noise at worst case transitions and temperatures.

(3) As measured with fixed resistors shown in Figure 4. Adjustable to zero with external potentiometer.

(4) For bipolar input ranges, full-scale error is the worst case of -Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions, divided by the transition voltage (not divided by the full-scale range) and includes the effect of offset error. For unipolar input ranges, full-scale error is the deviation of the last code transition divided by the transition voltage. It also includes the effect of offset error.

(5) All specifications in dB are referred to a full-scale $\pm 10\text{V}$ input.

(6) Full-Power Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB.

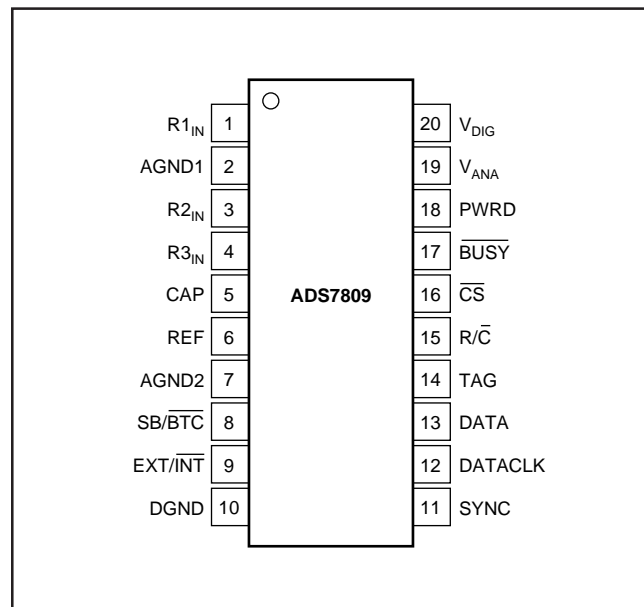
(7) Recovers to specified performance after $2 \cdot \text{FS}$ input overvoltage.

(8) The minimum V_{IH} level for the DATACLK signal is 3V.

PIN ASSIGNMENTS

PIN #	NAME	DESCRIPTION
1	R1 _{IN}	Analog Input. See Table I and Figure 4 for input range connections.
2	AGND1	Analog Ground. Used internally as ground reference point. Minimal current flow.
3	R2 _{IN}	Analog Input. See Table I and Figure 4 for input range connections.
4	R3 _{IN}	Analog Input. See Table I and Figure 4 for input range connections.
5	CAP	Reference Buffer Capacitor. 2.2μF Tantalum to ground.
6	REF	Reference Input/Output. Outputs internal 2.5V reference. Can also be driven by external system reference. In both cases, bypass to ground with a 2.2μF Tantalum capacitor.
7	AGND2	Analog Ground
8	SB/BTC	Select Straight Binary or Binary Two's Complement data output format. If HIGH, data will be output in a Straight Binary format. If LOW, data will be output in a Binary Two's Complement format.
9	EXT/INT	Select External or Internal Clock for transmitting data. If HIGH, data will be output synchronized to the clock input on DATACLK. If LOW, a convert command will initiate the transmission of the data from the previous conversion, along with 16 clock pulses output on DATACLK.
10	DGND	Digital Ground
11	SYNC	Synch Output. If EXT/INT is HIGH, either a rising edge on R/C with CS LOW or a falling edge on CS with R/C HIGH will output a pulse on SYNC synchronized to the external DATACLK.
12	DATACLK	Either an input or an output depending on the EXT/INT level. Output data will be synchronized to this clock. If EXT/INT is LOW, DATACLK will transmit 16 pulses after each conversion, and then remain LOW between conversions.
13	DATA	Serial Data Output. Data will be synchronized to DATACLK, with the format determined by the level of SB/BTC. In the external clock mode, after 16 bits of data, the ADS7809 will output the level input on TAG as long as CS is LOW and R/C is HIGH (see Figure 3). If EXT/INT is LOW, data will be valid on both the rising and falling edges of DATACLK, and between conversions DATA will stay at the level of the TAG input when the conversion was started.
14	TAG	Tag Input for use in external clock mode. If EXT/INT is HIGH, digital data input on TAG will be output on DATA with a delay of 16 DATACLK pulses as long as CS is LOW and R/C is HIGH. See Figure 3.
15	R/C	Read/Convert Input. With CS LOW, a falling edge on R/C puts the internal sample-and-hold into the hold state and starts a conversion. When EXT/INT is LOW, this also initiates the transmission of the data results from the previous conversion. If EXT/INT is HIGH, a rising edge on R/C with CS LOW, or a falling edge on CS with R/C HIGH, transmits a pulse on SYNC and initiates the transmission of data from the previous conversion.
16	CS	Chip Select. Internally OR'ed with R/C.
17	BUSY	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output shift register. CS or R/C must be HIGH when BUSY rises, or another conversion will start without time for signal acquisition.
18	PWRD	Power Down Input. If HIGH, conversions are inhibited and power consumption is significantly reduced. Results from the previous conversion are maintained in the output shift register.
19	V _{ANA}	Analog Supply Input. Nominally +5V. Connect directly to pin 20, and decouple to ground with 0.1μF ceramic and 10μF tantalum capacitors.
20	V _{DIG}	Digital Supply Input. Nominally +5V. Connect directly to pin 19. Must be ≤ V _{ANA} .

PIN CONFIGURATION



ANALOG INPUT RANGE	CONNECT R1 _{IN} VIA 200Ω TO	CONNECT R2 _{IN} VIA 100Ω TO	CONNECT R3 _{IN} TO	IMPEDANCE
±10V	V _{IN}	AGND	CAP	22.9kΩ
±5V	AGND	V _{IN}	CAP	13.3kΩ
±3.33V	V _{IN}	V _{IN}	CAP	10.7kΩ
0V to 10V	AGND	V _{IN}	AGND	13.3kΩ
0V to 5V	AGND	AGND	V _{IN}	10.0kΩ
0V to 4V	V _{IN}	AGND	V _{IN}	10.7kΩ

TABLE I. Input Range Connections. See Figure 4 for complete information.

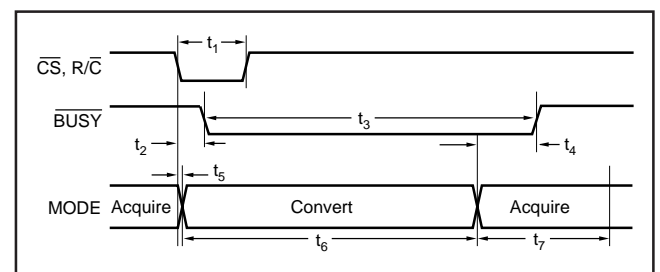


FIGURE 1. Basic Conversion Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40		6000	ns
t_2	$\overline{\text{BUSY}}$ Delay			65	ns
t_3	$\overline{\text{BUSY}}$ LOW			8	μs
t_4	$\overline{\text{BUSY}}$ Delay After End of Conversion		220		ns
t_5	Aperture Delay		40		ns
t_6	Conversion Time		7.6	8	μs
t_7	Acquisition Time			2	μs
$t_6 + t_7$	Throughput Time		9	10	μs
t_8	$\text{R}/\overline{\text{C}}$ LOW to DATACLK Delay		450		ns
t_9	DATACLK Period		440		ns
t_{10}	Data Valid to DATACLK HIGH Delay	20	75		ns
t_{11}	Data Valid After DATACLK LOW Delay	100	125		ns
t_{12}	External DATACLK	100			ns
t_{13}	External DATACLK HIGH	20			ns
t_{14}	External DATACLK LOW	30			ns
t_{15}	DATACLK HIGH Setup Time	20		$t_{12} + 5$	ns
t_{16}	$\text{R}/\overline{\text{C}}$ to $\overline{\text{CS}}$ Setup Time	10			ns
t_{17}	SYNC Delay After DATACLK HIGH	15		35	ns
t_{18}	Data Valid Delay	25		55	ns
t_{19}	$\overline{\text{CS}}$ to Rising Edge Delay	25			ns
t_{20}	Data Available after $\overline{\text{CS}}$ LOW	6			μs

TABLE II. Conversion and Data Timing. $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$.

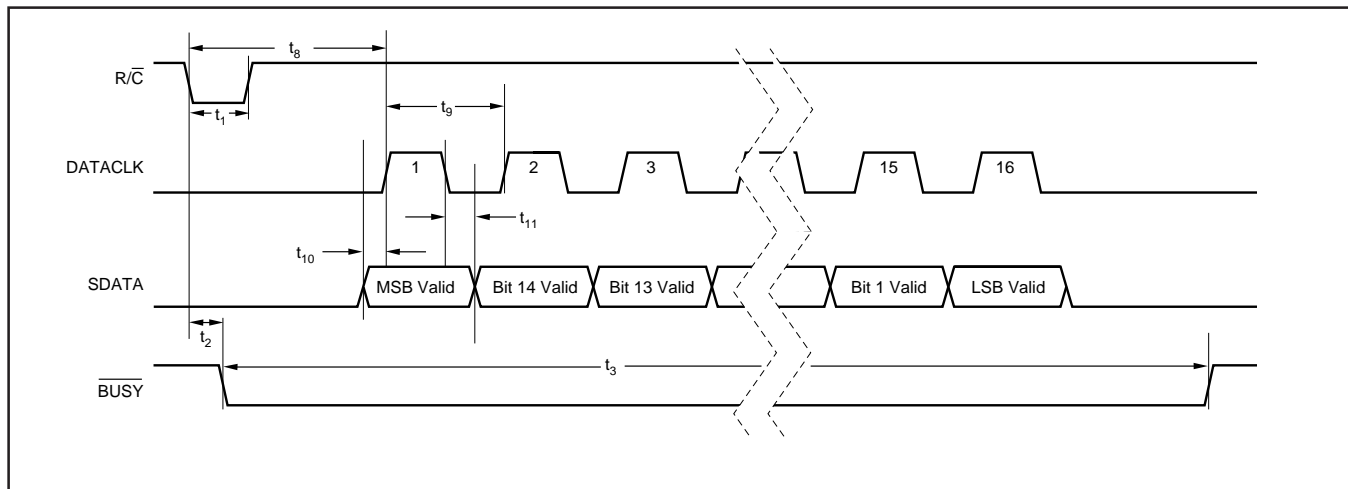


FIGURE 2. Serial Data Timing Using Internal Clock. ($\overline{\text{CS}}$, $\text{EXT}/\overline{\text{INT}}$ and TAG Tied LOW.)

SPECIFIC FUNCTION	\overline{CS}	R/\overline{C}	\overline{BUSY}	$\overline{EXT}/\overline{INT}$	DATACLK	PWRD	SB/ \overline{BTC}	OPERATION
Initiate Conversion and Output Data Using Internal Clock	1 > 0	0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n - 1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
	0	1 > 0	1	0	Output	0	x	Initiates conversion "n". Data from conversion "n - 1" clocked out on DATA synchronized to 16 clock pulses output on DATACLK.
Initiate Conversion and Output Data Using External Clock	1 > 0	0	1	1	Input	0	x	Initiates conversion "n".
	0	1 > 0	1	1	Input	0	x	Initiates conversion "n".
	1 > 0	1	1	1	Input	x	x	Outputs a pulse on SYNC followed by data from conversion "n" clocked out synchronized to external DATACLK.
	1 > 0	1	0	1	Input	0	x	Outputs a pulse on SYNC followed by data from conversion "n - 1" clocked out synchronized to external DATACLK. ⁽¹⁾ Conversion "n" in process.
Incorrect Conversions	0	0	0 > 1	x	x	0	x	\overline{CS} or R/\overline{C} must be HIGH or a new conversion will be initiated without time for acquisition.
	x	x	x	x	x	0	x	Analog circuitry powered. Conversion can proceed.
Power-Down	x	x	x	x	x	1	x	Analog circuitry disabled. Data from previous conversion maintained in output registers.
	x	x	x	x	x	x	1	
Selecting Output Format	x	x	x	x	x	x	0	Serial data is output in Binary Two's Complement format.
	x	x	x	x	x	x	1	Serial data is output in Straight Binary format.

NOTE: (1) See Figure 3b for constraints on previous data valid during conversion.

TABLE III. Control Truth Table.

DESCRIPTION	ANALOG INPUT						DIGITAL OUTPUT			
							BINARY TWO'S COMPLEMENT (SB/ \overline{BTC} LOW)		STRAIGHT BINARY (SB/ \overline{BTC} HIGH)	
							BINARY CODE	HEX CODE	BINARY CODE	HEX CODE
Full-Scale Range	± 10	± 5	$\pm 3.33V$	0V to 10V	0V to 5V	0V to 4V				
Least Significant Bit (LSB)	305 μV	153 μV	102 μV	153 μV	76 μV	61 μV				
+Full Scale (FS - 1LSB)	9.999695V	4.999847V	3.333231V	9.999847V	4.999924V	3.999939V	0111 1111 1111 1111	7FFF	1111 1111 1111 1111	FFFF
Midscale	0V	0V	0V	5V	2.5V	2V	0000 0000 0000 0000	0000	1000 0000 0000 0000	8000
One LSB Below Midscale	-305 μV	-153 μV	-102 μV	4.999847V	2.499924V	1.999939V	1111 1111 1111 1111	FFFF	0111 1111 1111 1111	7FFF
-Full Scale	-10V	-5V	-3.333333V	0V	0V	0V	1000 0000 0000 0000	8000	0000 0000 0000 0000	0000

TABLE IV. Output Codes and Ideal Input Voltages.

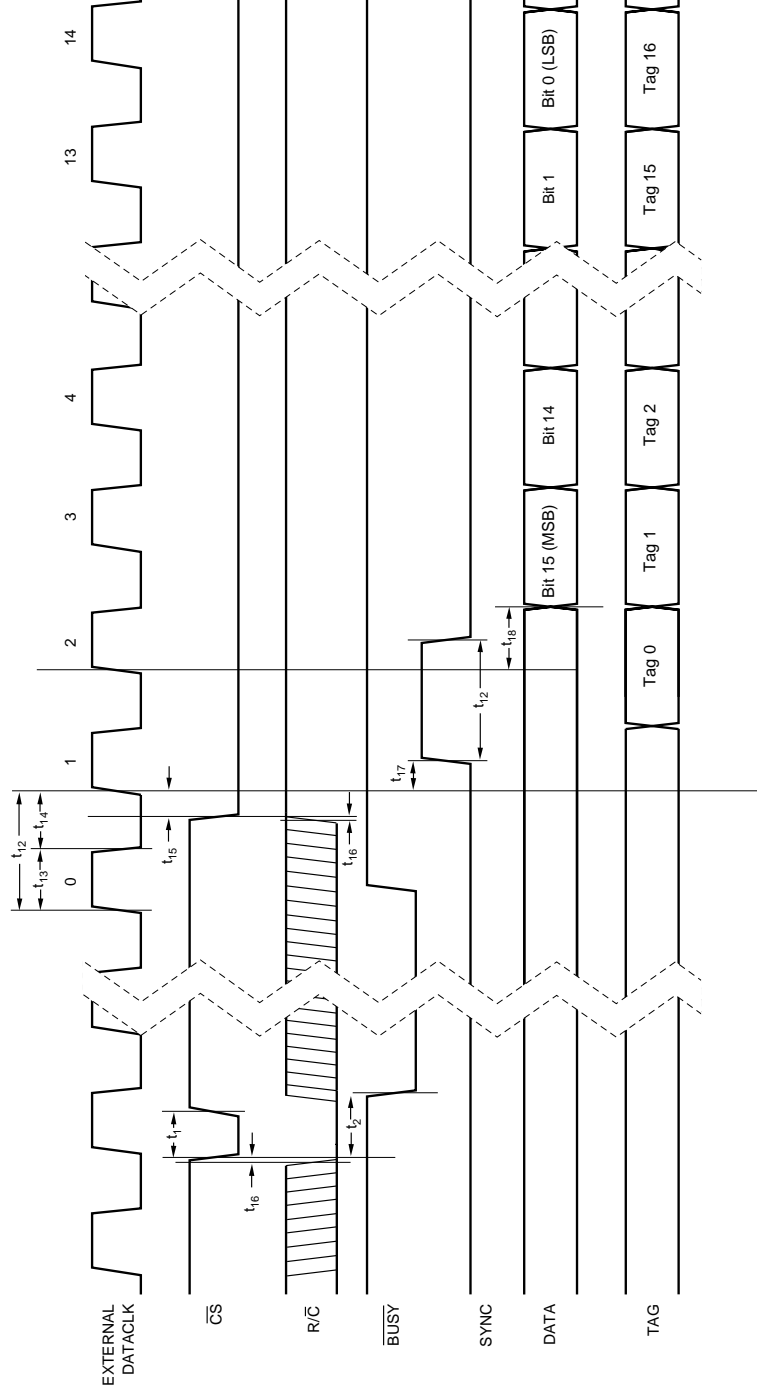


FIGURE 3a. Conversion and Read Timing with External Clock. (EXT/INT Tied High.) Read After Conversion.

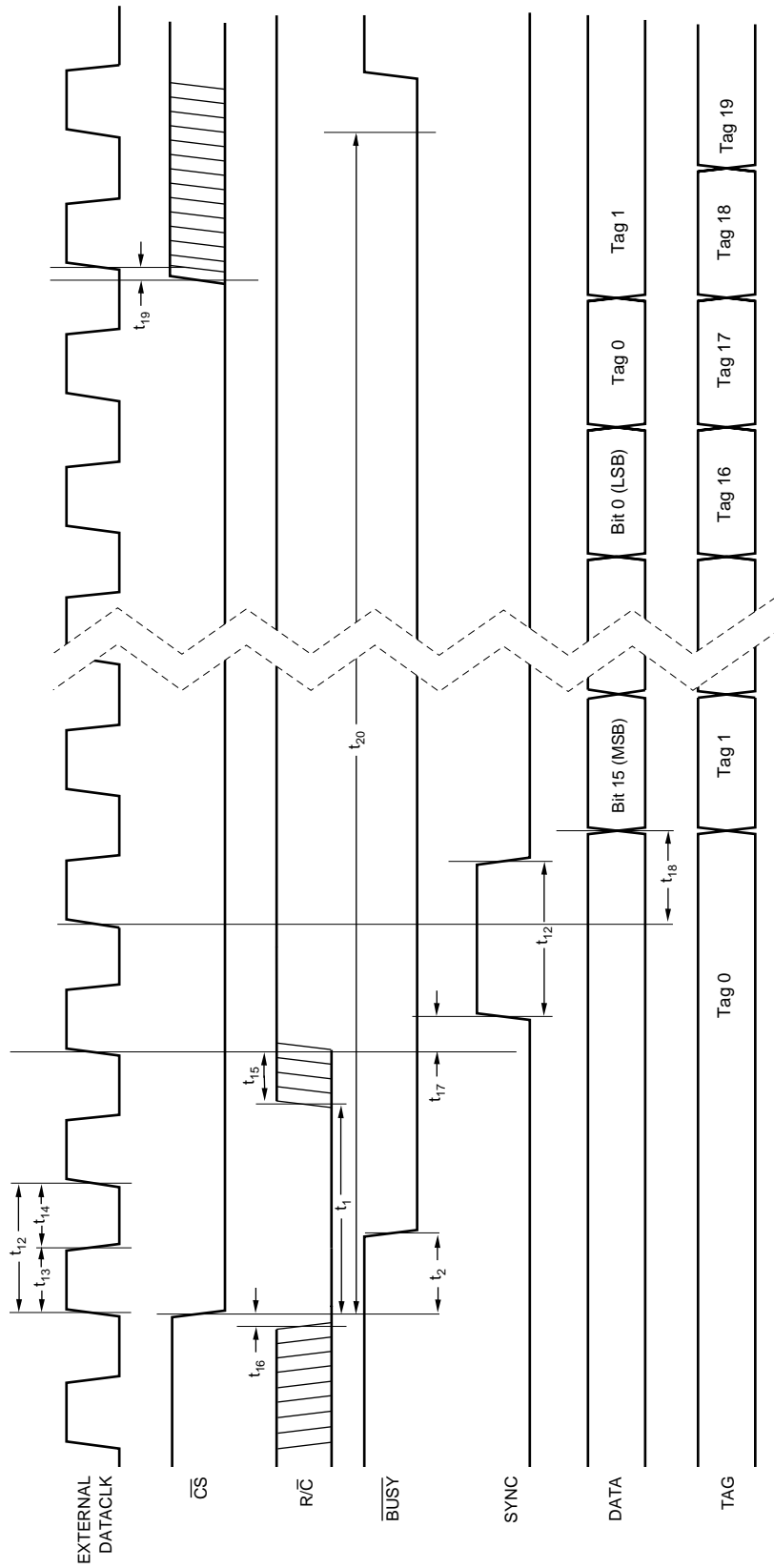


FIGURE 3b. Conversion and Read Timing with External Clock. (EXT/INT Tied High.) Read During Conversion (Previous Conversion Results).

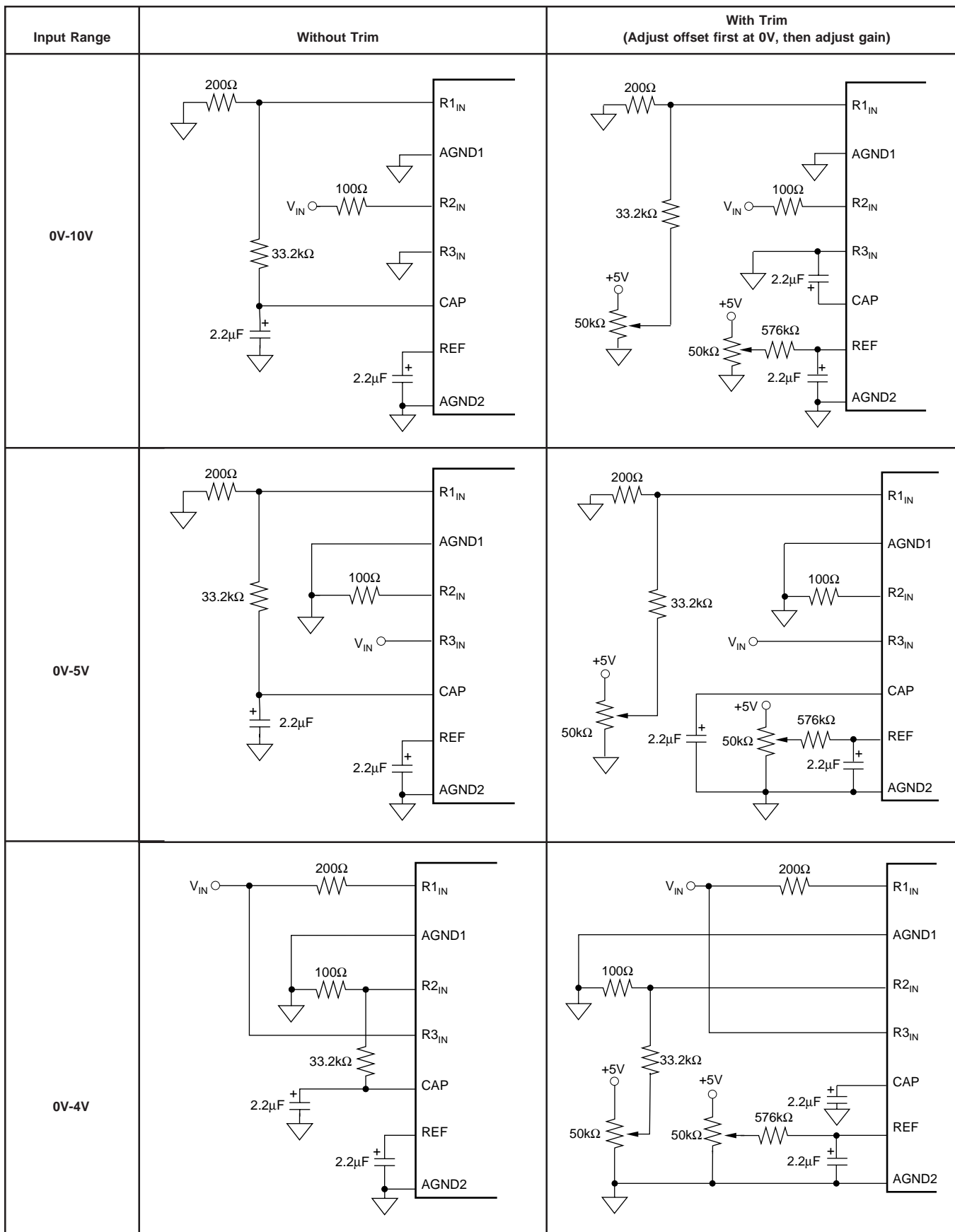


FIGURE 4a. Offset/Gain Circuits for Unipolar Input Ranges.

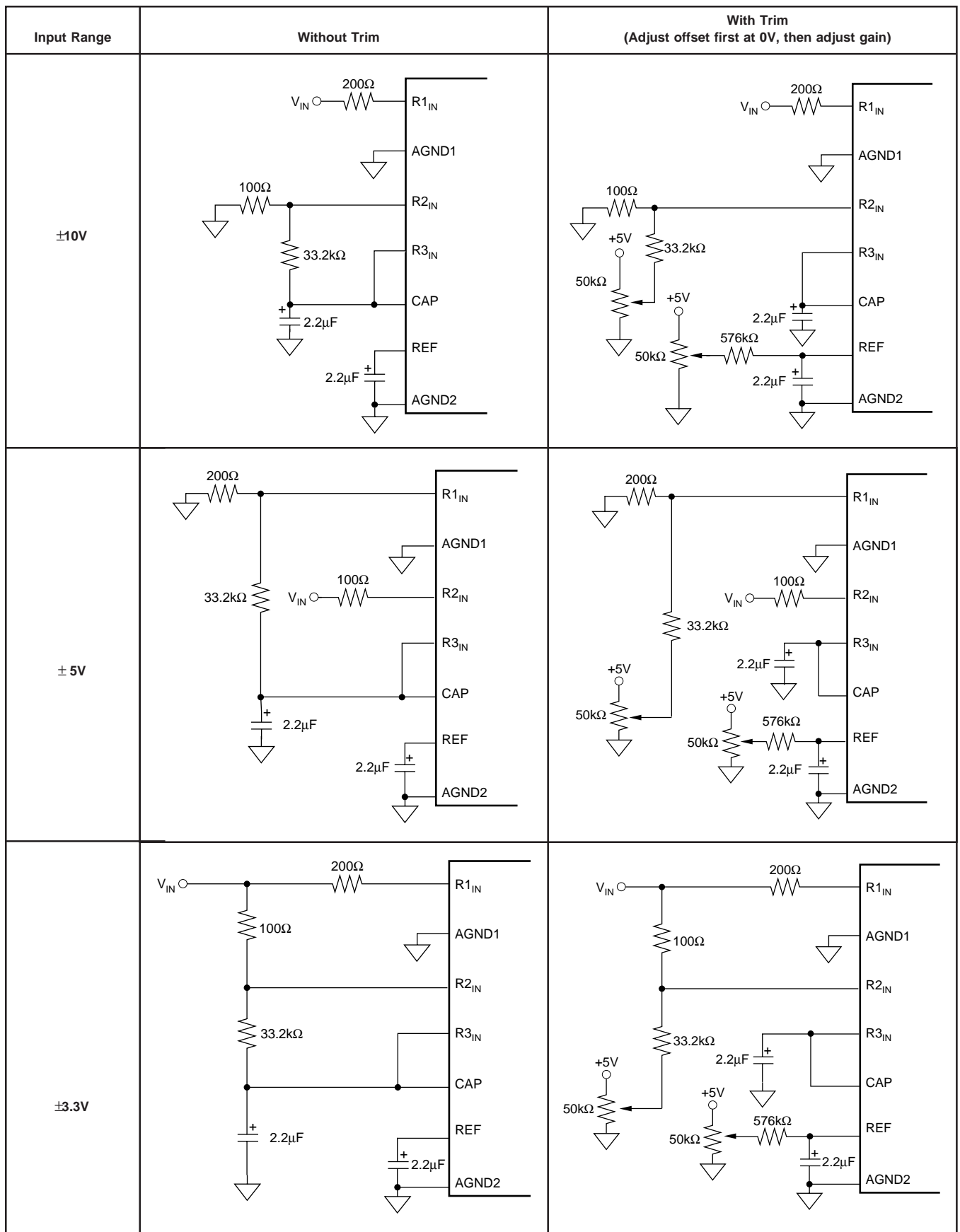


FIGURE 4b. Offset/Gain Circuits for Bipolar Input Ranges.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
10/06	C	3	Absolute Maximum Ratings	CAP and REF were switched.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7809U	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809U/1K	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809U/1KE4	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples
ADS7809UB	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U B	Samples
ADS7809UB/1K	ACTIVE	SOIC	DW	20	1000	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U B	Samples
ADS7809UE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	ADS7809U	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7809U/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
ADS7809UB/1K	SOIC	DW	20	1000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7809U/1K	SOIC	DW	20	1000	367.0	367.0	45.0
ADS7809UB/1K	SOIC	DW	20	1000	367.0	367.0	45.0

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View ADS7809U/1KG4 on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management