



# THE DATASHEET OF AD8504ARUZ-REEL



### FEATURES

**Supply current: 1  $\mu$ A maximum/amplifier**  
**Offset voltage: 3 mV maximum**  
**Single-supply or dual-supply operation**  
**Rail-to-rail input and output**  
**No phase reversal**  
**Unity gain stable**

### APPLICATIONS

**Portable equipment**  
**Remote sensors**  
**Low power filters**  
**Threshold detectors**  
**Current sensing**

### GENERAL DESCRIPTION

The AD8502/AD8504 are low power, precision CMOS operational amplifiers featuring a maximum supply current of 1  $\mu$ A per amplifier. The AD8502/AD8504 have a maximum offset voltage of 3 mV and a typical input bias current of 1 pA operating rail-to-rail on both the input and output. The AD8502/AD8504 can operate from a single-supply voltage of +1.8 V to +5.5 V or a dual-supply voltage of  $\pm 0.9$  V to  $\pm 2.75$  V.

With its low power consumption, low input bias current, and rail-to-rail input and output, the AD8502/AD8504 are ideally suited for a variety of battery-powered portable applications. Potential applications include bedside monitors, pulse monitors, glucose meters, smoke and fire detectors, vibration monitors, and backup battery sensors.

The ability to swing rail-to-rail at both the input and output helps maximize dynamic range and signal-to-noise ratio in systems that operate at very low voltages. The low offset voltage allows use of the AD8502/AD8504 in systems with high gain

### PIN CONFIGURATIONS

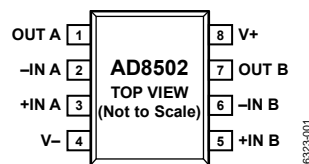


Figure 1. 8-Lead SOT-23

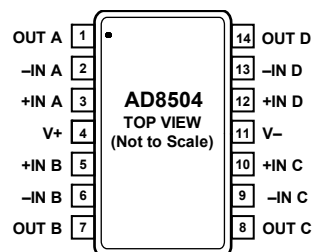


Figure 2. 14-Lead TSSOP (RU-14)

without creating excessively large output offset errors. The AD8502 and AD8504 offer an additional benefit by providing high accuracy without the need for system calibration.

The AD8502/AD8504 are fully specified over the industrial temperature range ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ) and the extended industrial temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ). The AD8502 is available in an 8-lead, SOT-23 surface-mount package. The AD8504 is available in a 14-lead TSSOP surface-mount package.

**Table 1. Low Supply Current Op Amps**

Supply Current	1 $\mu$ A	10 $\mu$ A	20 $\mu$ A
Single	AD8500		
Dual	AD8502	ADA4505-2	AD8506
Quad	AD8504	ADA4505-4	AD8508

#### Rev. A

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**REVISION HISTORY**

**2/09—Rev. 0 to Rev. A**

Changes to General Description Section .....	1
Added Table 1; Renumbered Sequentially .....	1
Changes to Typical Performance Characteristics Section.....	7
Updated Outline Dimensions .....	14

**1/07—Revision 0: Initial Version**

# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

@  $V_S = 5\text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	3 5 5.5	mV mV mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		7 5		$\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	10 100 600	pA pA pA
Input Offset Current	$I_{OS}$	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5 50 100	pA pA pA
Input Voltage Range	IVR		0		5.0	V
Common-Mode Rejection Ratio	CMRR	$0\text{ V} < V_{CM} < 5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	67 65 65	76		dB dB dB
Large Signal Voltage Gain	$A_{VO}$	$0.1\text{ V} < V_{OUT} < 4.9\text{ V}$ ; $R_{LOAD} = 1\text{ M}\Omega$ $0.1\text{ V} < V_{OUT} < 4.9\text{ V}$ ; $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $0.1\text{ V} < V_{OUT} < 4.9\text{ V}$ ; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	98 93 75	120		dB dB dB
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2 4.5		pF pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_{LOAD} = 100\text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$ $R_{LOAD} = 10\text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	4.970 4.960 4.950 4.900 4.810 4.650	4.990		V V V V V V
Output Voltage Low	$V_{OL}$	$R_{LOAD} = 100\text{ k}\Omega$ to $V_S$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$ $R_{LOAD} = 10\text{ k}\Omega$ to $V_S$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		1.6 15	5 20 37 40	mV mV mV mV mV
Short-Circuit Current	$I_{SC}$	$V_{OUT} = \text{GND}$		$\pm 5$		mA
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$1.8\text{ V} < V_S < 5\text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	85 66 66	105		dB dB dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_S/2$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.75	1 1.5 2	$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_{LOAD} = 1\text{ M}\Omega$		0.004		V/ $\mu\text{s}$
Gain Bandwidth Product	GBP			7		kHz
Phase Margin	$\phi_O$			60		Degrees

# AD8502/AD8504

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Noise		0.1 Hz to 10 Hz		6		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1 \text{ kHz}$		190		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1 \text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

@  $V_S = 1.8 \text{ V}$ ,  $V_{CM} = V_S/2$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$0 \text{ V} < V_{CM} < 1.8 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	3	mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		7	5	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$0 \text{ V} < V_{CM} < 1.8 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	10	pA
Input Offset Current	$I_{OS}$	$0 \text{ V} < V_{CM} < 1.8 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	5	pA
Input Voltage Range	IVR		0		1.8	V
Common-Mode Rejection Ratio	CMRR	$0 \text{ V} < V_{CM} < 1.8 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	59	75		dB
Large Signal Voltage Gain	$A_{VO}$	$0.1 \text{ V} < V_{OUT} < 1.7 \text{ V}$ ; $R_{LOAD} = 1 \text{ M}\Omega$ $0.1 \text{ V} < V_{OUT} < 1.7 \text{ V}$ ; $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $0.1 \text{ V} < V_{OUT} < 1.7 \text{ V}$ ; $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	88	110		dB
Input Capacitance	$C_{DIFF}$ $C_{CM}$			2		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_{LOAD} = 100 \text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$ $R_{LOAD} = 10 \text{ k}\Omega$ to GND $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$	1.79 1.78 1.77 1.75 1.70 1.65	1.795   1.764  		V
Output Voltage Low	$V_{OL}$	$R_{LOAD} = 100 \text{ k}\Omega$ to $V_S$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$ $R_{LOAD} = 10 \text{ k}\Omega$ to $V_S$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C}$ to $+125^\circ\text{C}$		1.0   10  	5 6 7 20 28 29	mV
Short-Circuit Current	$I_{SC}$			$\pm 5$		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$1.8 \text{ V} < V_S < 5 \text{ V}$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	85 66 66	105		dB
Supply Current/Amplifier	$I_{SY}$	$V_O = V_S/2$ $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.65	1 1.5 2	$\mu\text{A}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_{LOAD} = 1\text{ M}\Omega$		0.004		V/ $\mu$ s
Gain Bandwidth Product	GBP			7		kHz
Phase Margin	$\phi_0$			60		Degrees
NOISE PERFORMANCE						
Peak-to-Peak Noise		0.1 Hz to 10 Hz		6		$\mu$ V p-p
Voltage Noise Density	$e_n$	f = 1 kHz		190		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	f = 1 kHz		0.1		pA/ $\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 4.**

Parameter	Rating
Supply Voltage	6 V
Input Voltage	$V_{SS} - 0.3\text{ V}$ to $V_{DD} + 0.3\text{ V}$
Differential Input Voltage	$\pm 6\text{ V}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Operating Temperature Range	$-40^\circ\text{C}$ to $+125^\circ\text{C}$
Junction Temperature Range	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^\circ\text{C}$

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply at  $25^\circ\text{C}$ , unless otherwise noted.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 5. Thermal Characteristics**

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOT-23 (RJ-8)	376	126	$^\circ\text{C}/\text{W}$
14-Lead TSSOP (RU-14)	180	35	$^\circ\text{C}/\text{W}$

## ESD CAUTION



### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

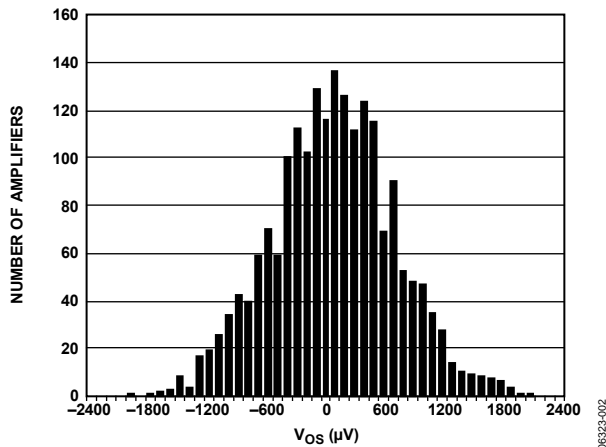


Figure 3. Input Offset Voltage Distribution ( $0\text{ V} < V_{CM} < 5.0\text{ V}$ ),  $V_S = 5\text{ V}$

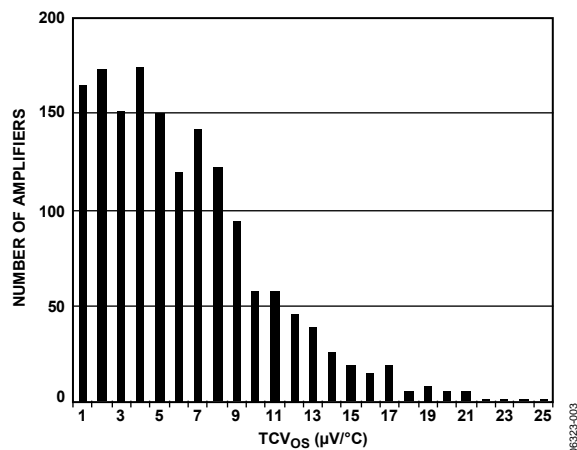


Figure 4. Input Offset Voltage Temperature Drift Distribution ( $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ ),  $V_S = 5\text{ V}$

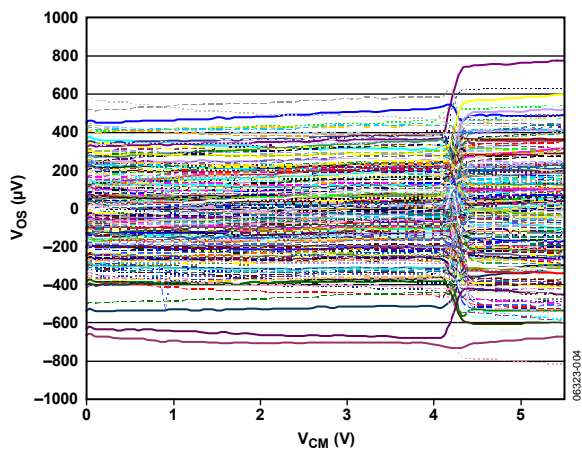


Figure 5. Input Offset Voltage vs. Common-Mode Voltage,  $V_S = 5\text{ V}$

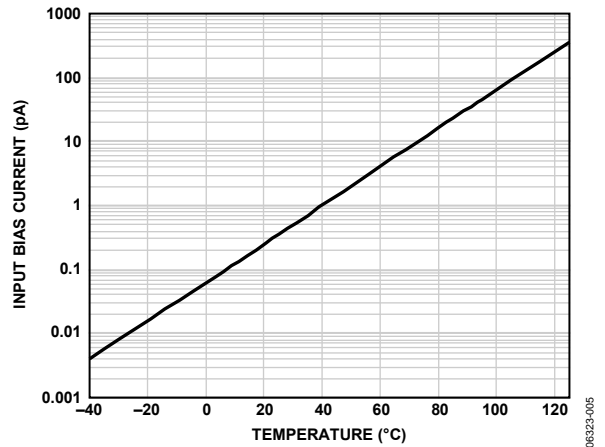


Figure 6. Input Bias Current vs. Temperature ( $V_S = 1.8\text{ V}$  and  $5.0\text{ V}$ )

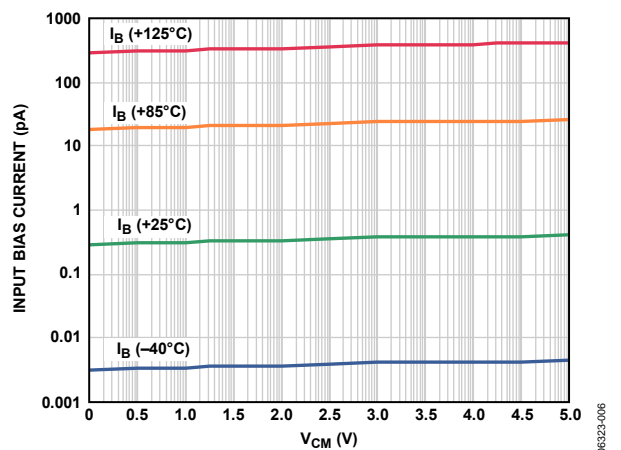


Figure 7. Input Bias Current vs. Common-Mode Voltage,  $V_S = 5\text{ V}$



Figure 8. Supply Current Distribution,  $V_S = 5\text{ V}$

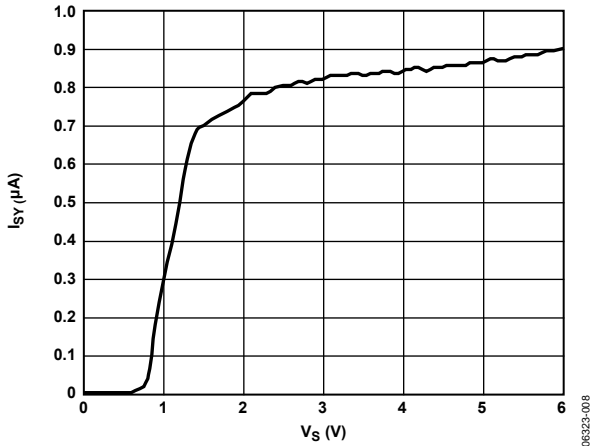


Figure 9. Supply Current vs. Supply Voltage

06323-008

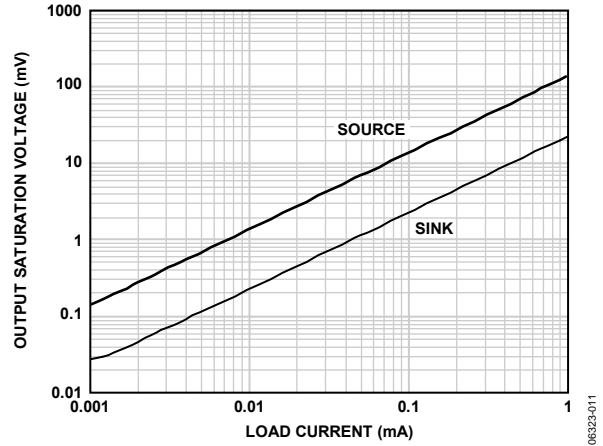


Figure 12. Output Saturation Voltage vs. Load Current,  $V_S = 5\text{ V}$

06323-011

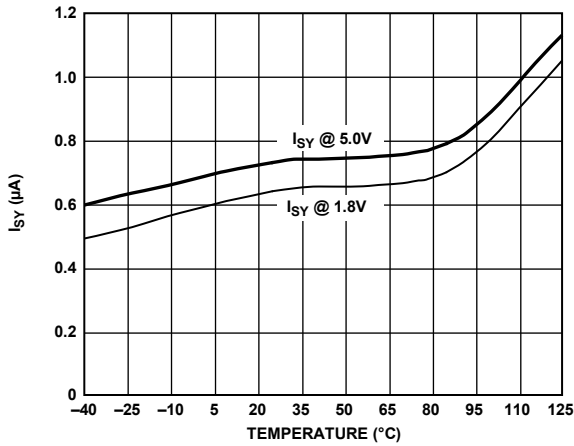


Figure 10. Supply Current vs. Temperature

06323-009

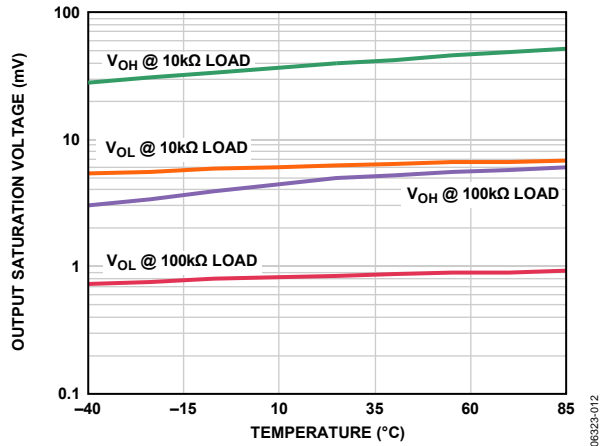


Figure 13. Output Saturation Voltage vs. Temperature,  $V_S = 5\text{ V}$

06323-012

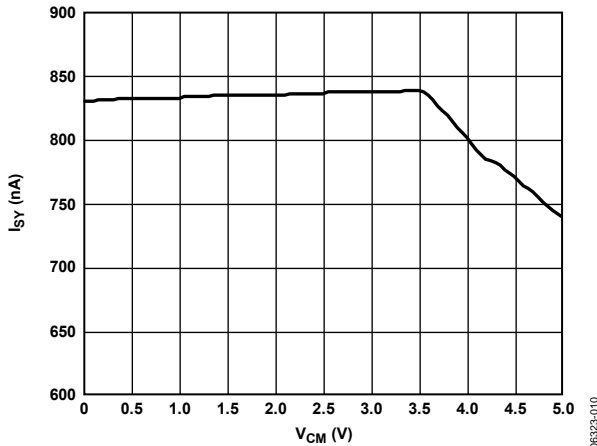


Figure 11. Supply Current vs. Input Common-Mode Voltage,  $V_S = 5\text{ V}$

06323-010

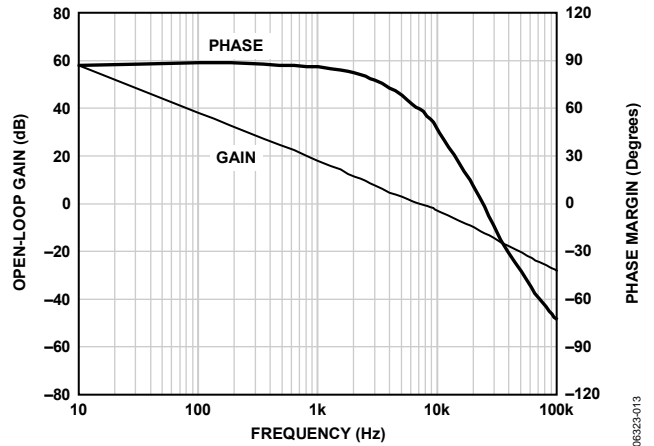


Figure 14. Open-Loop Gain and Phase vs. Frequency,  $V_S = 5\text{ V}$

06323-013

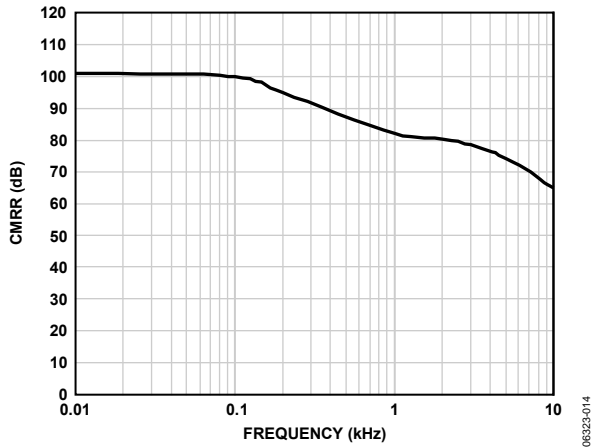


Figure 15. CMRR vs. Frequency,  $V_S = 5\text{ V}$

06323-014

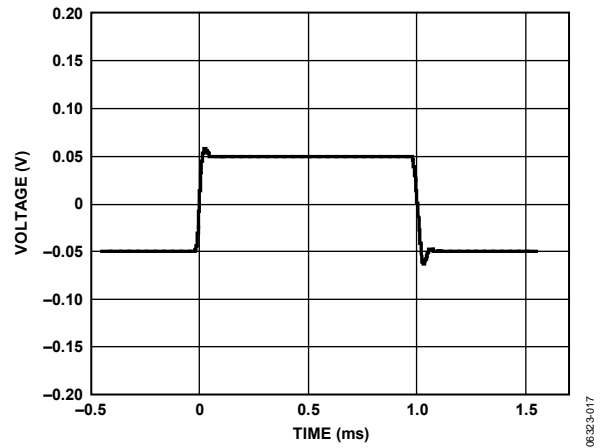


Figure 18. Small Signal Transient Response (No Load),  $V_S = 5\text{ V}$

06323-017

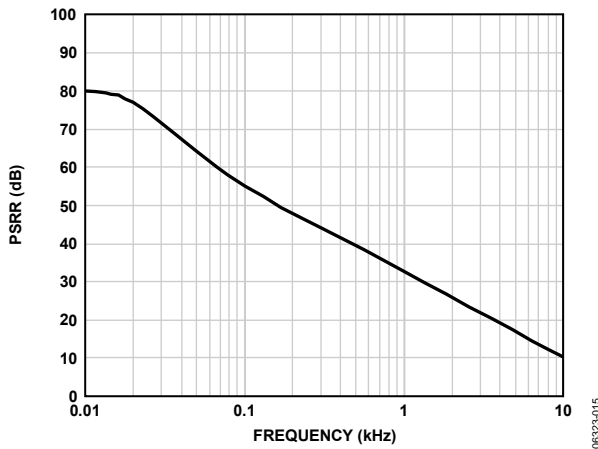


Figure 16. PSRR vs. Frequency,  $V_S = 5\text{ V}$

06323-015

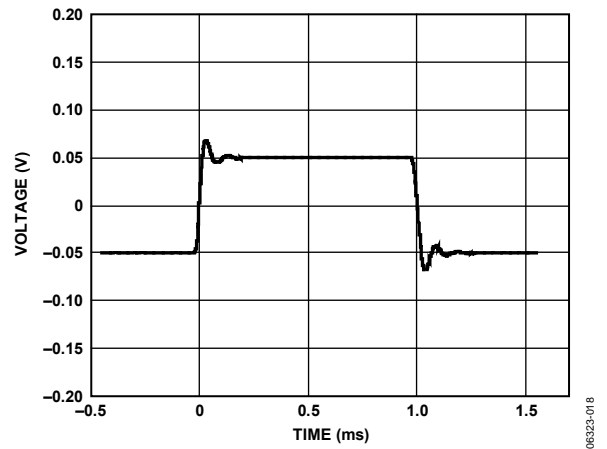


Figure 19. Small Signal Transient Response (100 pF Load Capacitance,  $V_S = 5\text{ V}$ )

06323-018

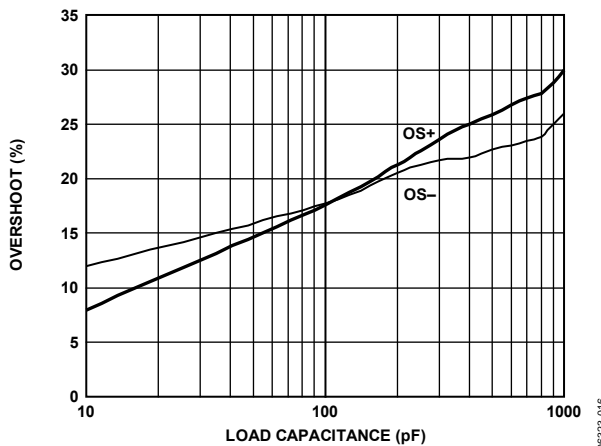


Figure 17. Small Signal Overshoot vs. Load Capacitance,  $V_S = 5\text{ V}$

06323-016

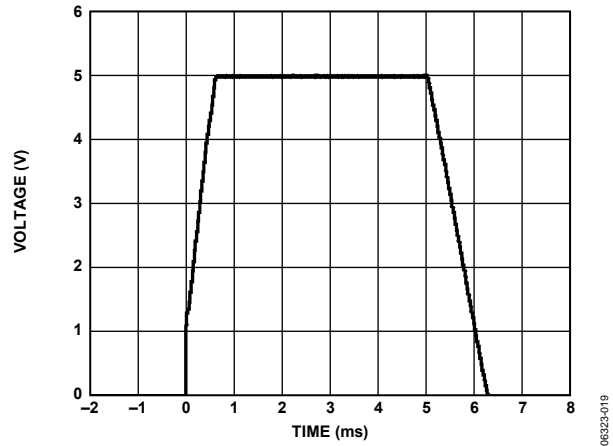


Figure 20. Large Signal Transient Response No Load,  $V_S = 5\text{ V}$

06323-019

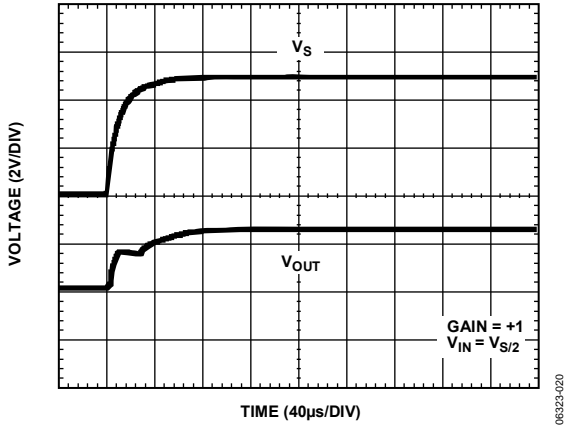


Figure 21. Turn-On Transient Response,  $V_S = 5\text{ V}$

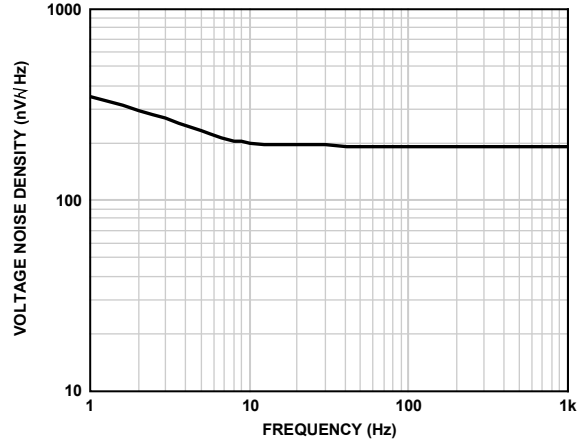


Figure 24. Input Voltage Noise ( $V_S = 5\text{ V}$  and  $1.8\text{ V}$ )

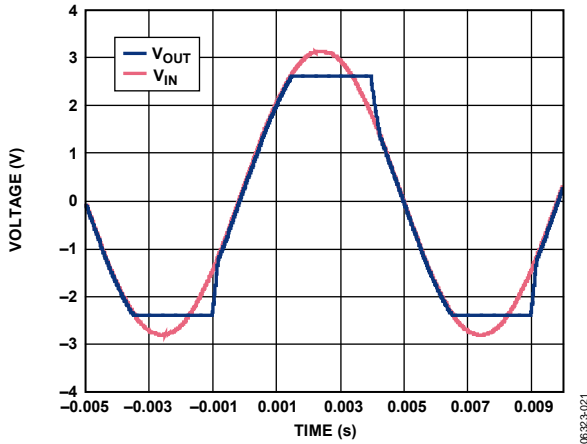


Figure 22. No Phase Reversal,  $V_S = 5\text{ V}$

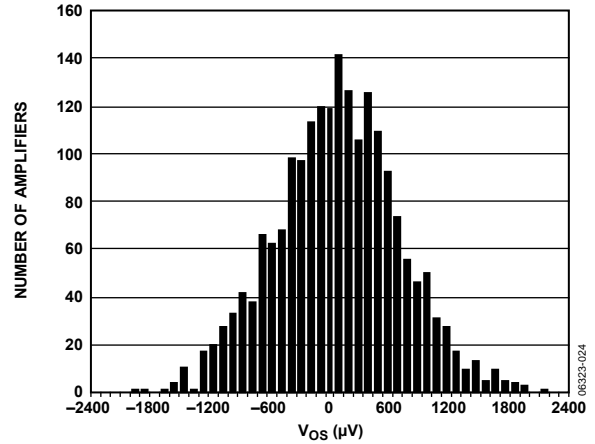


Figure 25. Input Offset Voltage Distribution ( $0\text{ V} < V_{CM} < 1.8\text{ V}$ ),  $V_S = 1.8\text{ V}$

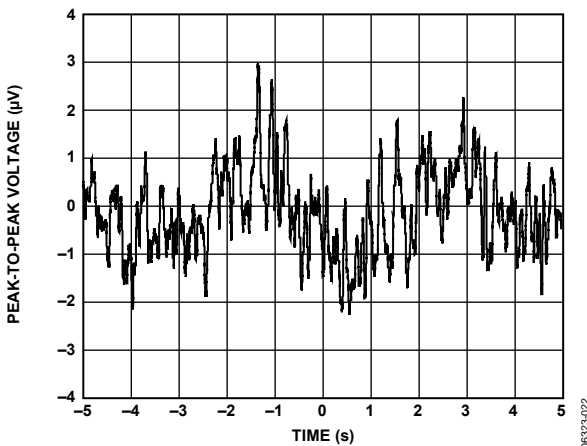


Figure 23. 0.1 Hz to 10 Hz Input Voltage Noise ( $V_S = 5\text{ V}$  and  $1.8\text{ V}$ )

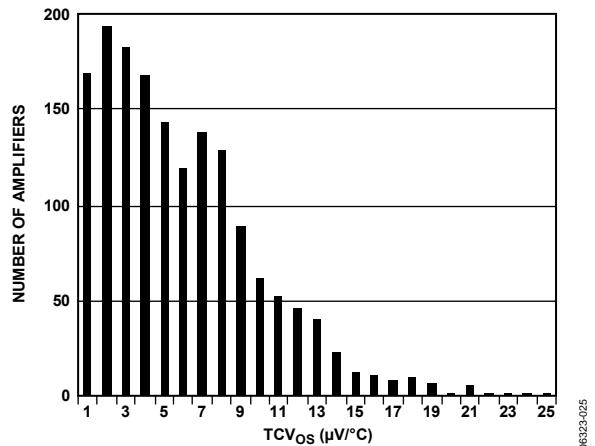


Figure 26. Input Offset Voltage Temperature Drift Distribution ( $-40^\circ\text{C} < T_A < +85^\circ\text{C}$ ),  $V_S = 1.8\text{ V}$

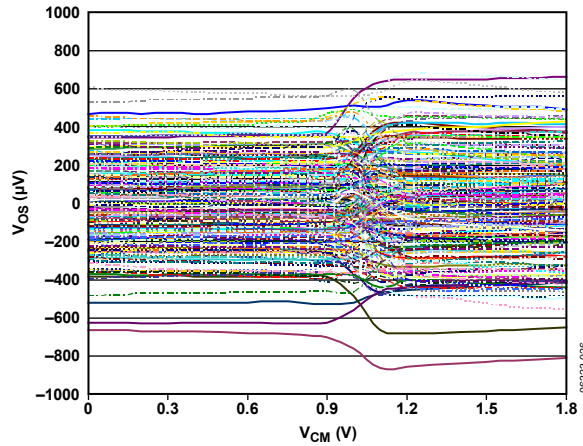


Figure 27. Input Offset Voltage vs. Input Common-Mode Voltage,  $V_S = 1.8\text{ V}$

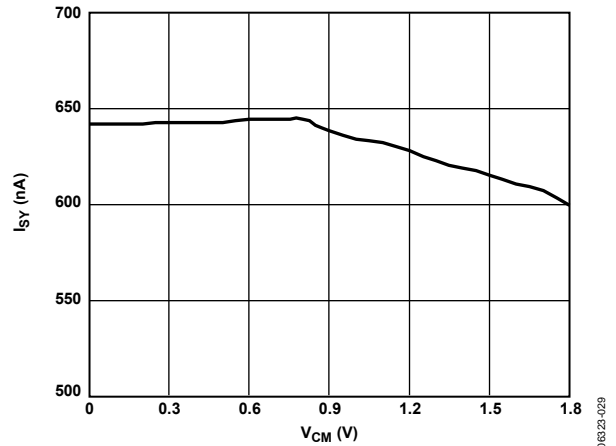


Figure 30. Supply Current vs. Input Common-Mode Voltage,  $V_S = 1.8\text{ V}$

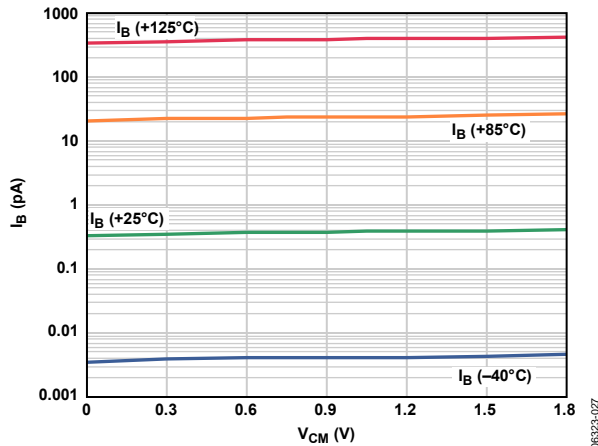


Figure 28. Input Bias Current vs. Input Common-Mode Voltage,  $V_S = 1.8\text{ V}$

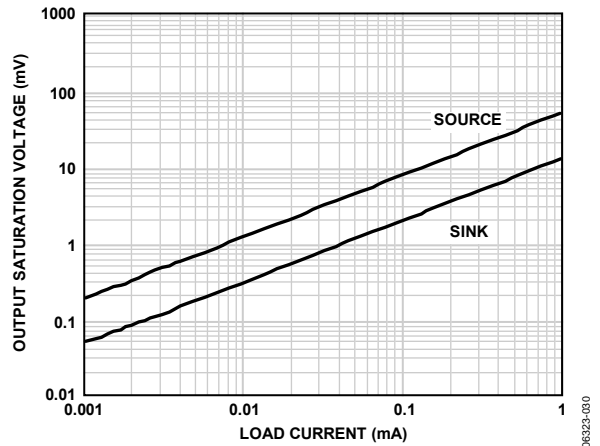


Figure 31. Output Saturation Voltage vs. Load Current  $V_S = 1.8\text{ V}$

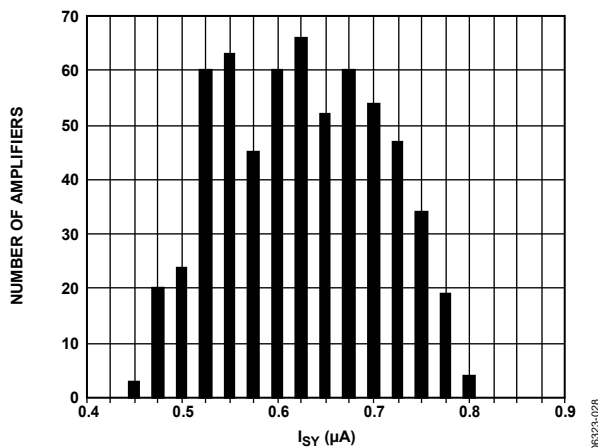


Figure 29. Supply Current Distribution,  $V_S = 1.8\text{ V}$

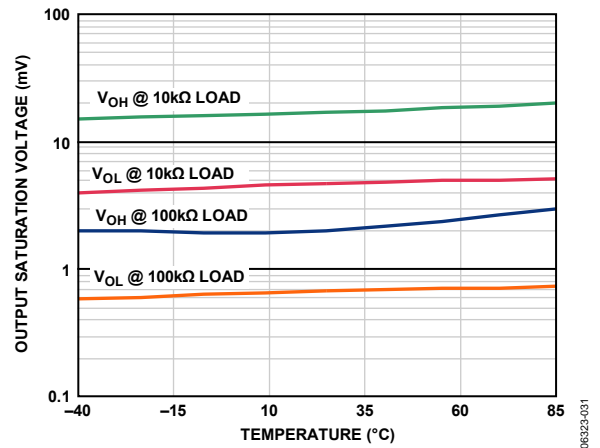


Figure 32. Output Saturation Voltage vs. Temperature,  $V_S = 1.8\text{ V}$

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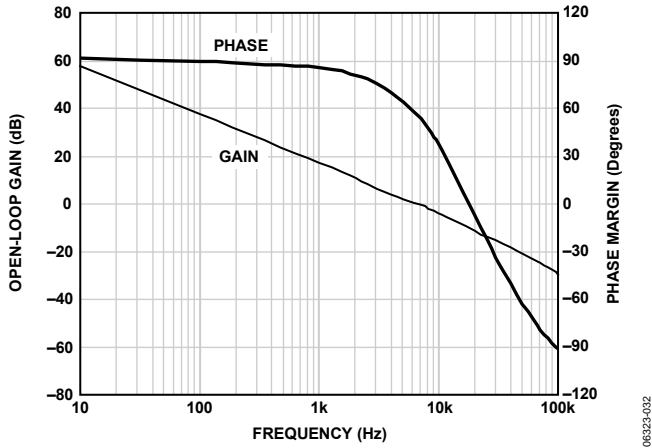


Figure 33. Open-Loop Gain and Phase vs. Frequency,  $V_S = 1.8\text{ V}$

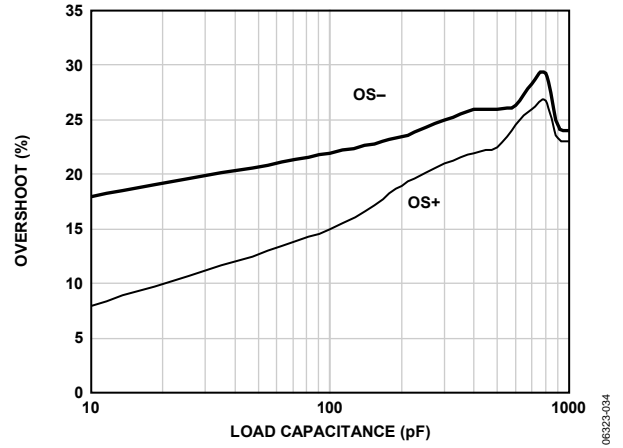


Figure 35. Small Signal Overshoot vs. Load Capacitance,  $V_S = 1.8\text{ V}$

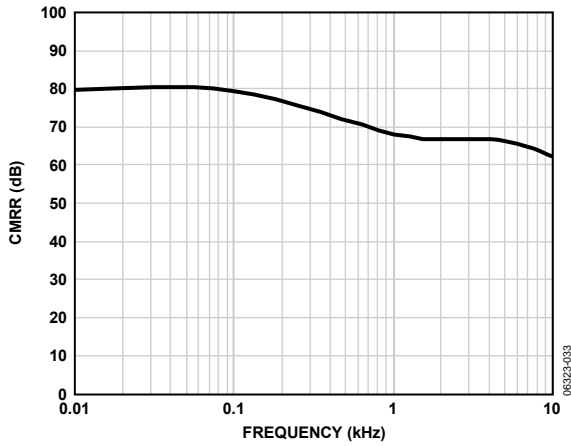


Figure 34. CMRR vs. Frequency,  $V_S = 1.8\text{ V}$

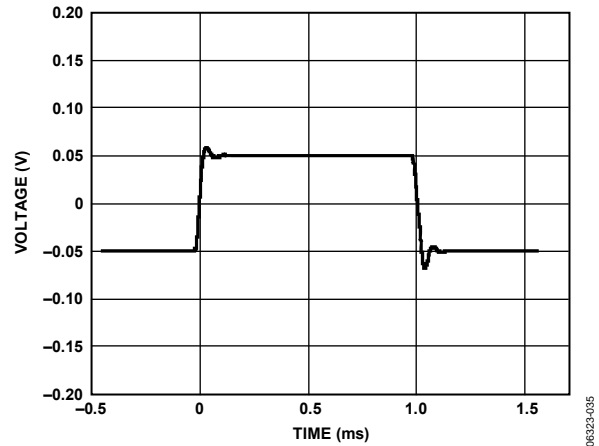


Figure 36. Small Signal Transient Response (No Load),  $V_S = 1.8\text{ V}$

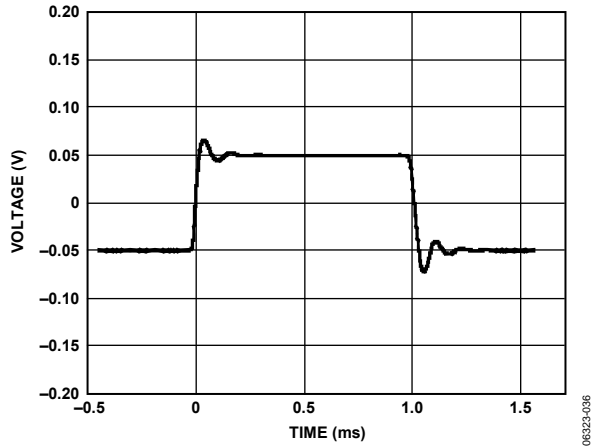


Figure 37. Small Signal Transient Response (100 pF Load Capacitance),  $V_S = 1.8\text{ V}$

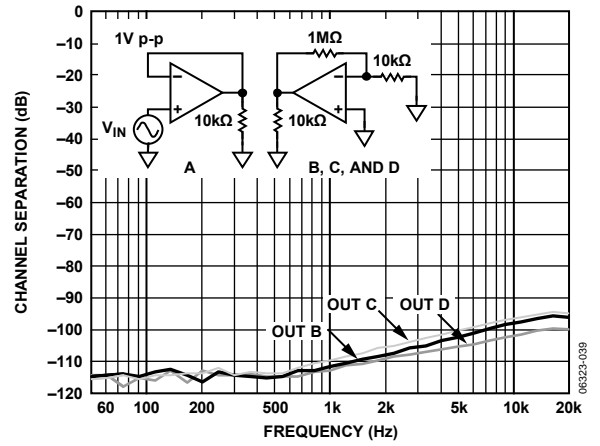


Figure 39. Channel Separation

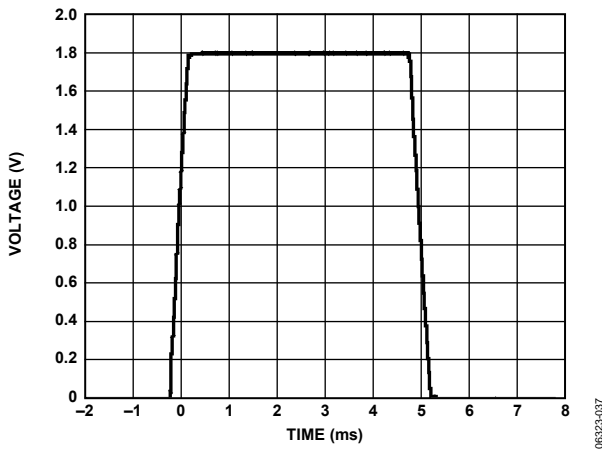
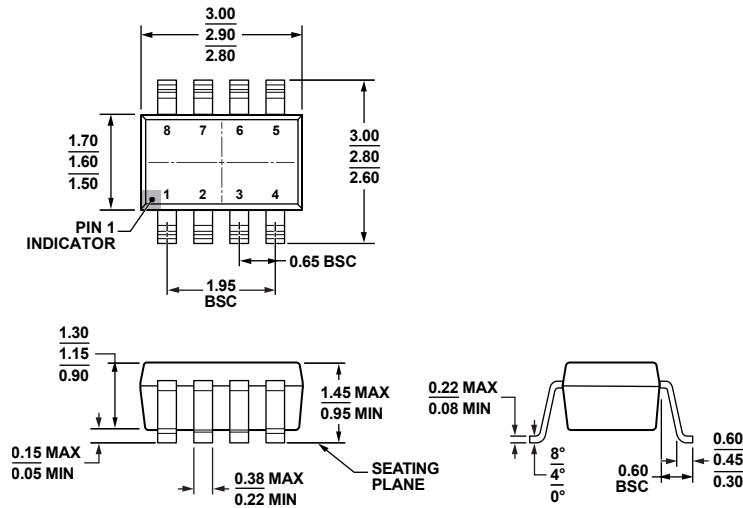


Figure 38. Large Signal Transient Response (No Load),  $V_S = 1.8\text{ V}$

# AD8502/AD8504

## OUTLINE DIMENSIONS

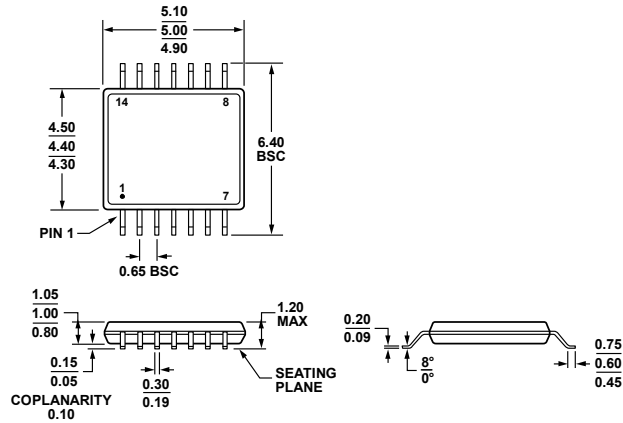


COMPLIANT TO JEDEC STANDARDS MO-178-BA

Figure 40. 8-Lead Small Outline Transistor Package [SOT-23] (RJ-8)

Dimensions shown in millimeters

121608-A



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 41. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061608-A

## ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8502ARJZ-R2 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	A1D
AD8502ARJZ-REEL <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	A1D
AD8502ARJZ-REEL7 <sup>1</sup>	-40°C to +125°C	8-Lead SOT-23	RJ-8	A1D
AD8504ARUZ <sup>1</sup>	-40°C to +125°C	14-Lead TSSOP	RU-14	
AD8504ARUZ-REEL <sup>1</sup>	-40°C to +125°C	14-Lead TSSOP	RU-14	

<sup>1</sup> Z = RoHS Compliant Part.

**NOTES**

**NOTES**

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View AD8504ARUZ-REEL on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management