

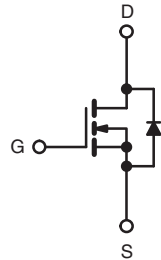
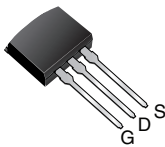


**THE DATASHEET OF
IRL520LPBF**



Power MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	100
$R_{DS(on)}$ (Ω)	$V_{GS} = 5\text{ V}$ 0.27
Q_g (Max.) (nC)	12
Q_{gs} (nC)	3.0
Q_{gd} (nC)	7.1
Configuration	Single

I²PAK (TO-262)


N-Channel MOSFET

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Logic-Level Gate Drive
- $R_{DS(on)}$ Specified at $V_{GS} = 4\text{ V}$ and 5 V
- 175°C Operating Temperature
- Compliant to RoHS Directive 2002/95/EC



RoHS*
COMPLIANT
HALOGEN
FREE
Available

DESCRIPTION

Third generation Power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The I²PAK (TO-262) is a through hole power package capable of accommodating die size up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package.

ORDERING INFORMATION	
Package	I ² PAK (TO-262)
Lead (Pb)-free and Halogen-free	SiHL520L-GE3
Lead (Pb)-free	IRL520LPbF SiHL520L-E3

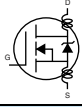
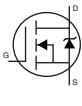
ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage		V_{GS}	± 10		
Continuous Drain Current	V_{GS} at 5 V	I_D	$T_C = 25^\circ\text{C}$	9.2	A
			$T_C = 100^\circ\text{C}$	6.5	
Pulsed Drain Current ^a		I_{DM}	36	W/ $^\circ\text{C}$	
Linear Derating Factor			0.40		
Linear Derating Factor (PCB Mount) ^e			0.025		
Single Pulse Avalanche Energy ^b		E_{AS}	170	mJ	
Avalanche Current ^a		I_{AR}	9.2	A	
Repetitive Avalanche Energy ^a		E_{AR}	6.0	mJ	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	P_D	60	W	
Peak Diode Recovery dV/dt^c		dV/dt	5.5	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 175	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		300 ^d		

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 25\text{ V}$, starting $T_J = 25^\circ\text{C}$, $L = 3.0\text{ mH}$, $R_G = 25\ \Omega$, $I_{AS} = 9.2\text{ A}$ (see fig. 12).
- $I_{SD} \leq 9.2\text{ A}$, $dI/dt \leq 110\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175^\circ\text{C}$.
- 1.6 mm from case.

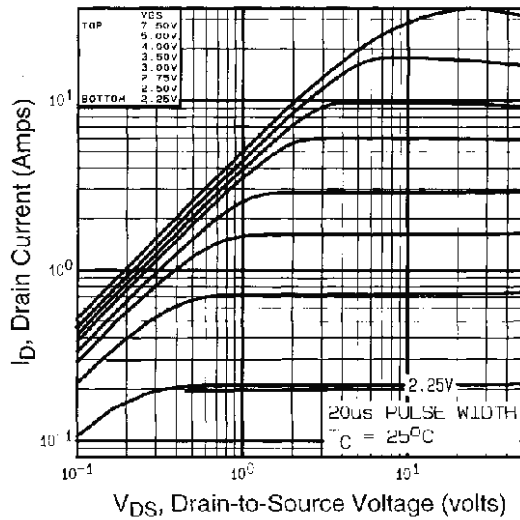
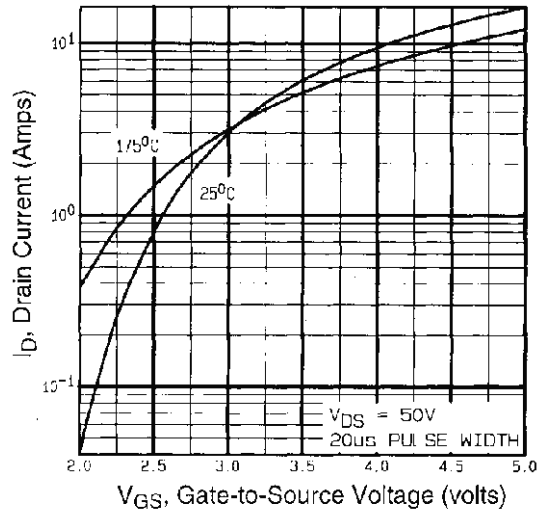
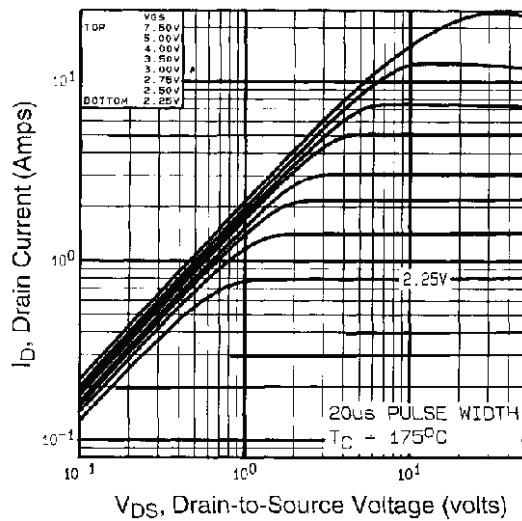
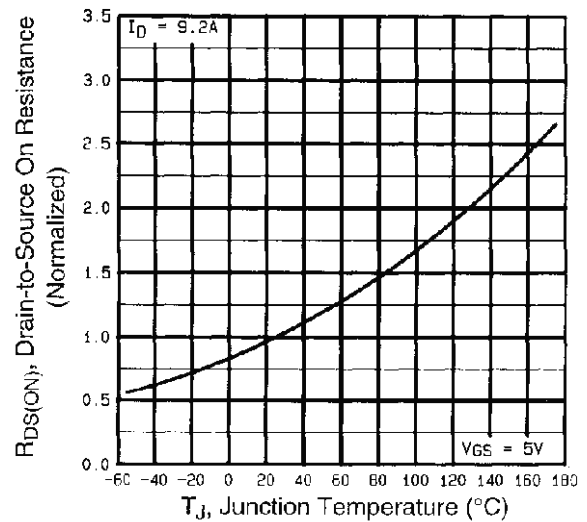
* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	2.5	

SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	100	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$	-	0.12	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	-	2.0	V
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 10\text{ V}$	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$	-	-	25	μA
		$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}, T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 5\text{ V}, I_D = 5.5\text{ A}^b$	-	-	0.27	Ω
		$V_{GS} = 4\text{ V}, I_D = 4.6\text{ A}^b$	-	-	0.38	Ω
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 5.5\text{ A}^b$	3.2	-	-	S
Dynamic						
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$	-	490	-	pF
Output Capacitance	C_{oss}		-	150	-	
Reverse Transfer Capacitance	C_{rss}		-	30	-	
Total Gate Charge	Q_g	$V_{GS} = 5\text{ V}, I_D = 9.2\text{ A}, V_{DS} = 80\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	12	nC
Gate-Source Charge	Q_{GS}		-	-	3.0	
Gate-Drain Charge	Q_{GD}		-	-	7.1	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 50\text{ V}, I_D = 9.2\text{ A}, R_G = 9\text{ }\Omega, R_D = 5.2\text{ }\Omega, \text{ see fig. 10}^b$	-	9.8	-	ns
Rise Time	t_r		-	64	-	
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	
Fall Time	t_f		-	27	-	
Dynamic						
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	9.2	A
Pulsed Diode Forward Current ^a	I_{SM}		-	-	36	
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 9.2\text{ A}, V_{GS} = 0\text{ V}^b$	-	-	2.5	V
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 9.2\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$	-	130	190	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	0.83	1.0	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

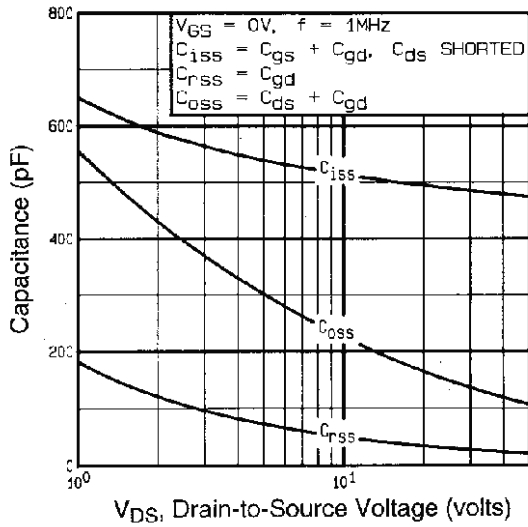


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

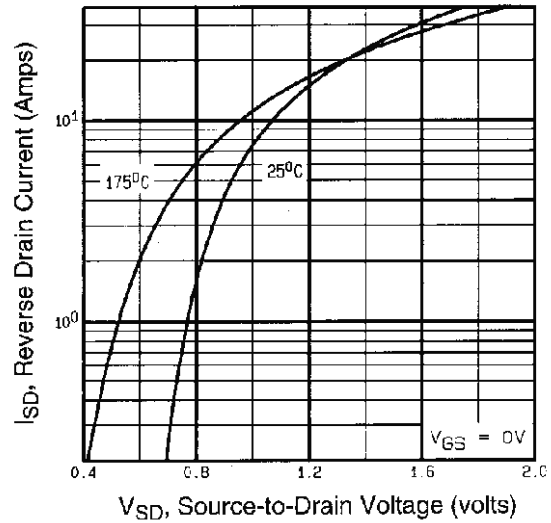


Fig. 7 - Typical Source-Drain Diode Forward Voltage

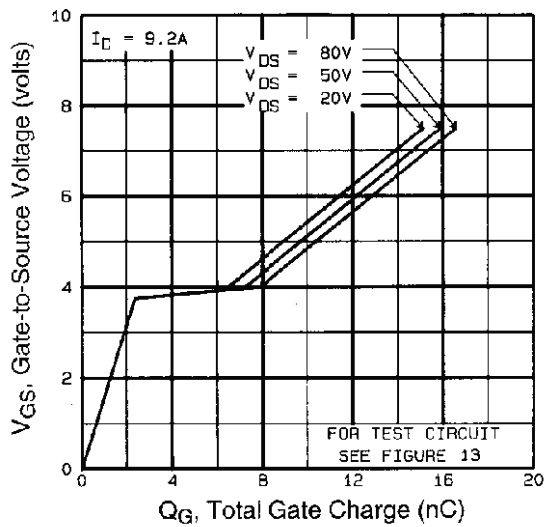


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

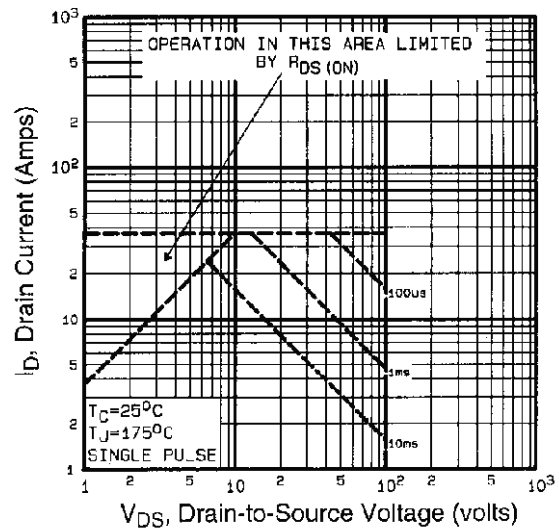


Fig. 8 - Maximum Safe Operating Area

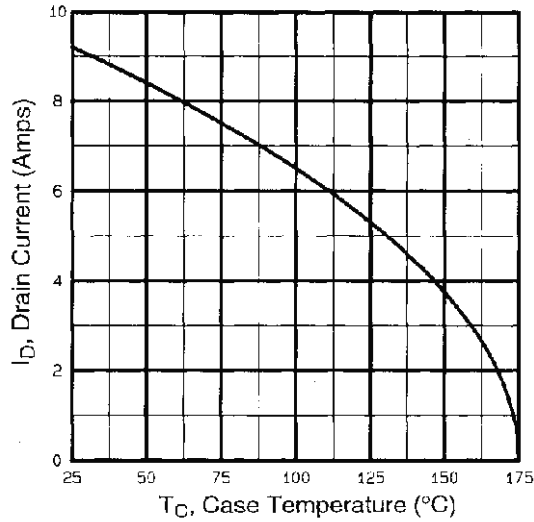


Fig. 9 - Maximum Drain Current vs. Case Temperature

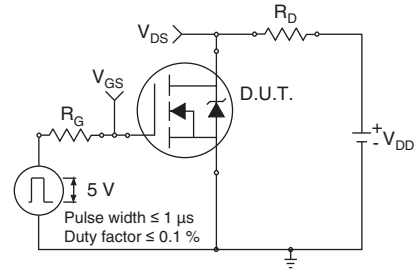


Fig. 10a - Switching Time Test Circuit

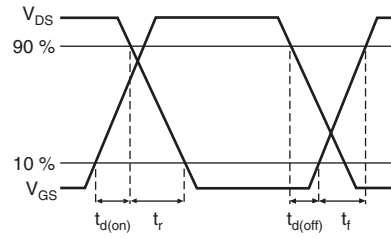


Fig. 10b - Switching Time Waveforms

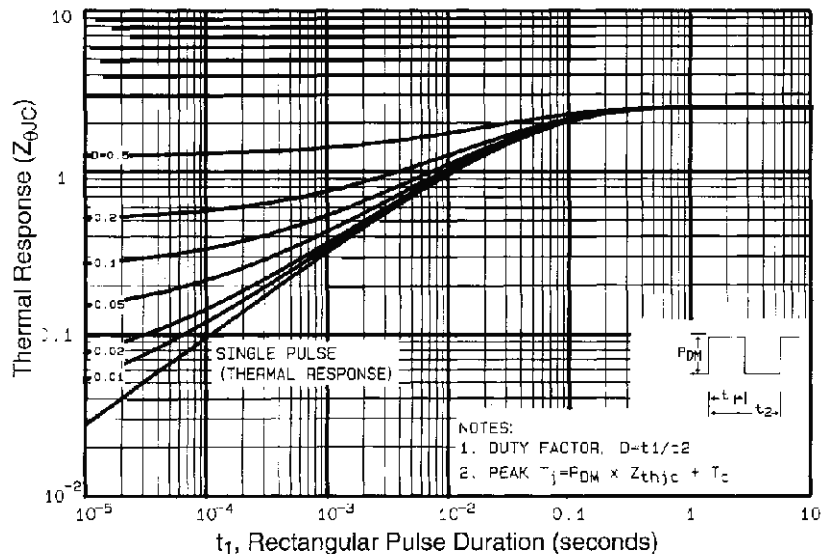


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

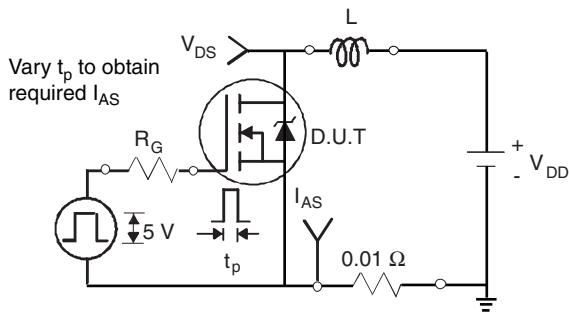


Fig. 12a - Unclamped Inductive Test Circuit

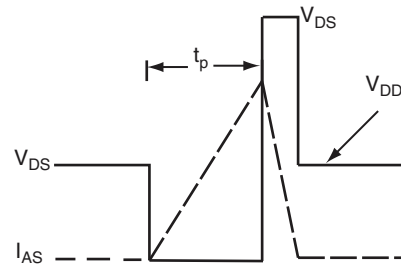


Fig. 12b - Unclamped Inductive Waveforms

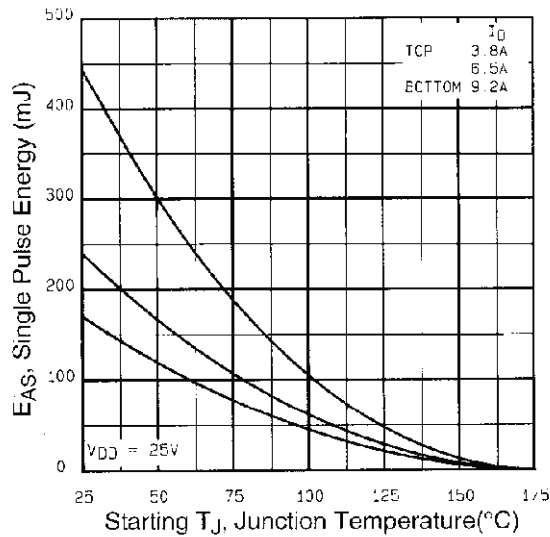


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

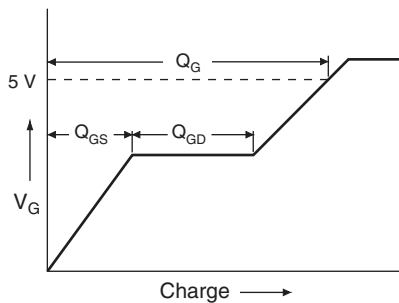


Fig. 13a - Basic Gate Charge Waveform

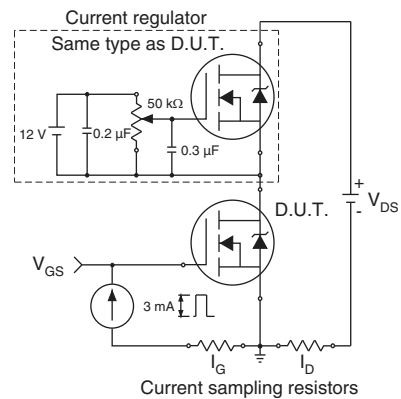
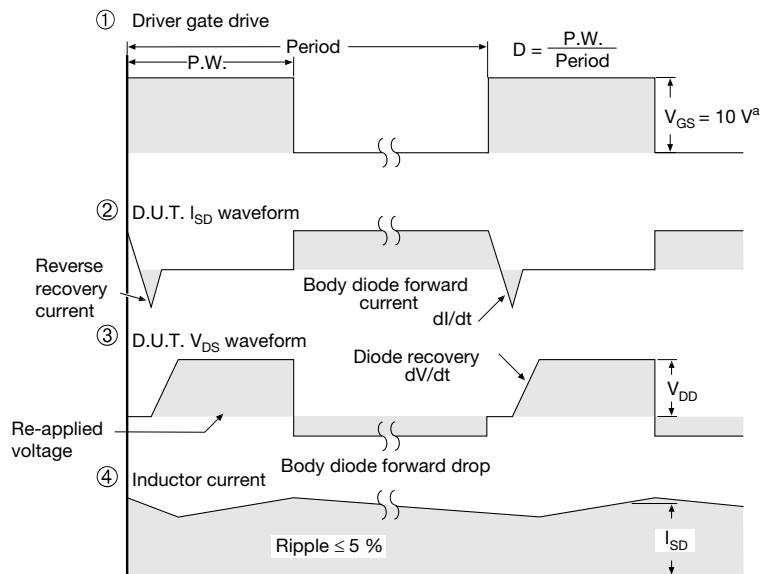
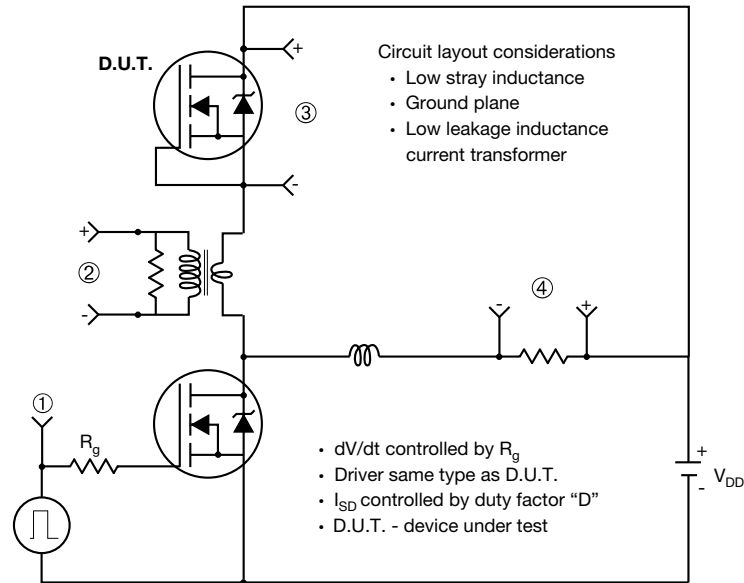


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit



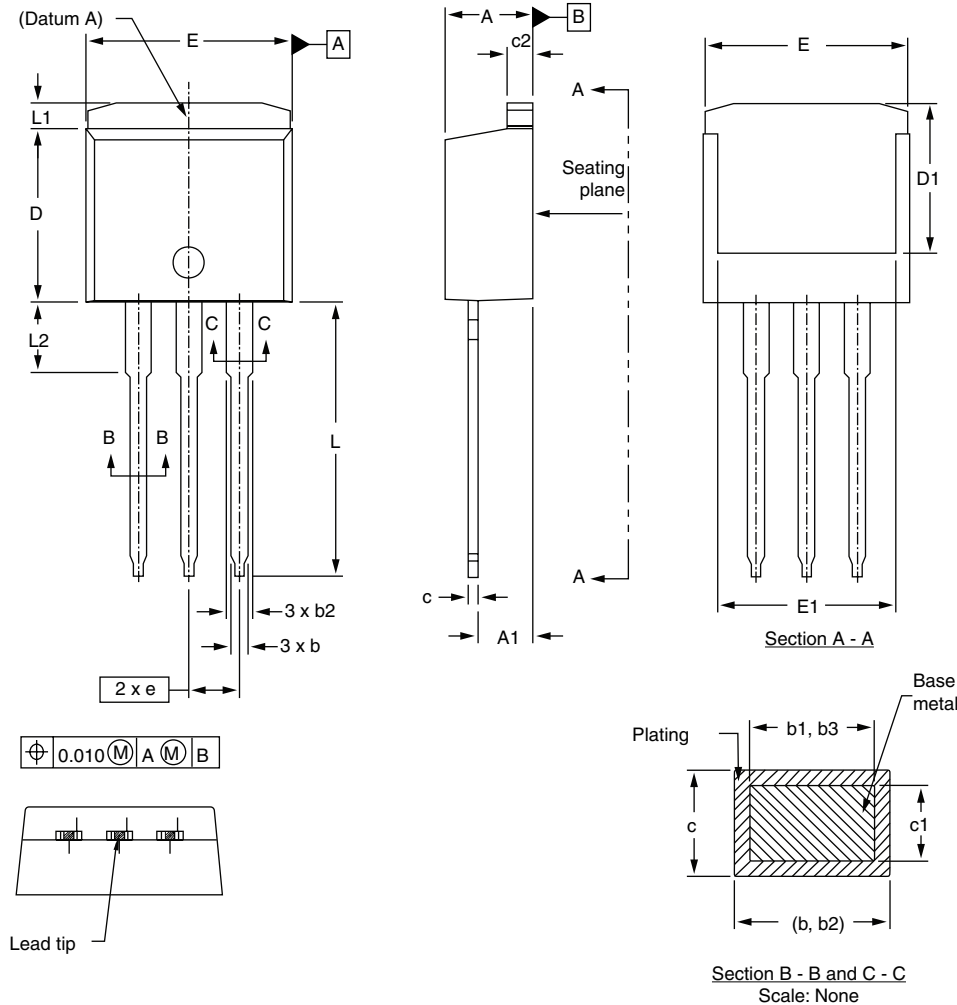
Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?94167.

I²PAK (TO-262) (HIGH VOLTAGE)



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.06	4.83	0.160	0.190
A1	2.03	3.02	0.080	0.119
b	0.51	0.99	0.020	0.039
b1	0.51	0.89	0.020	0.035
b2	1.14	1.78	0.045	0.070
b3	1.14	1.73	0.045	0.068
c	0.38	0.74	0.015	0.029
c1	0.38	0.58	0.015	0.023
c2	1.14	1.65	0.045	0.065

DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
D	8.38	9.65	0.330	0.380
D1	6.86	-	0.270	-
E	9.65	10.67	0.380	0.420
E1	6.22	-	0.245	-
e	2.54 BSC		0.100 BSC	
L	13.46	14.10	0.530	0.555
L1	-	1.65	-	0.065
L2	3.56	3.71	0.140	0.146

ECN: S-82442-Rev. A, 27-Oct-08
DWG: 5977

Notes

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm per side. These dimensions are measured at the outmost extremes of the plastic body.
3. Thermal pad contour optional within dimension E, L1, D1, and E1.
4. Dimension b1 and c1 apply to base metal only.



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