



THE DATASHEET OF 74LVC139D,118

74LVC139

Dual 2-to-4 line decoder/demultiplexer

Rev. 5 — 19 October 2011

Product data sheet

1. General description

The 74LVC139 is a dual 2-to-4 line decoder/demultiplexer. It has two independent decoders, each accepting two binary weighted inputs ($nA0$ and $nA1$) and providing four mutually exclusive outputs ($nY0$ to $nY3$) that are LOW when selected. Each decoder has an active LOW input ($n\bar{E}$). When $n\bar{E}$ is HIGH, every output is forced HIGH. The enable input can be used as the data input for a 1-to-4 demultiplexer application.

2. Features and benefits

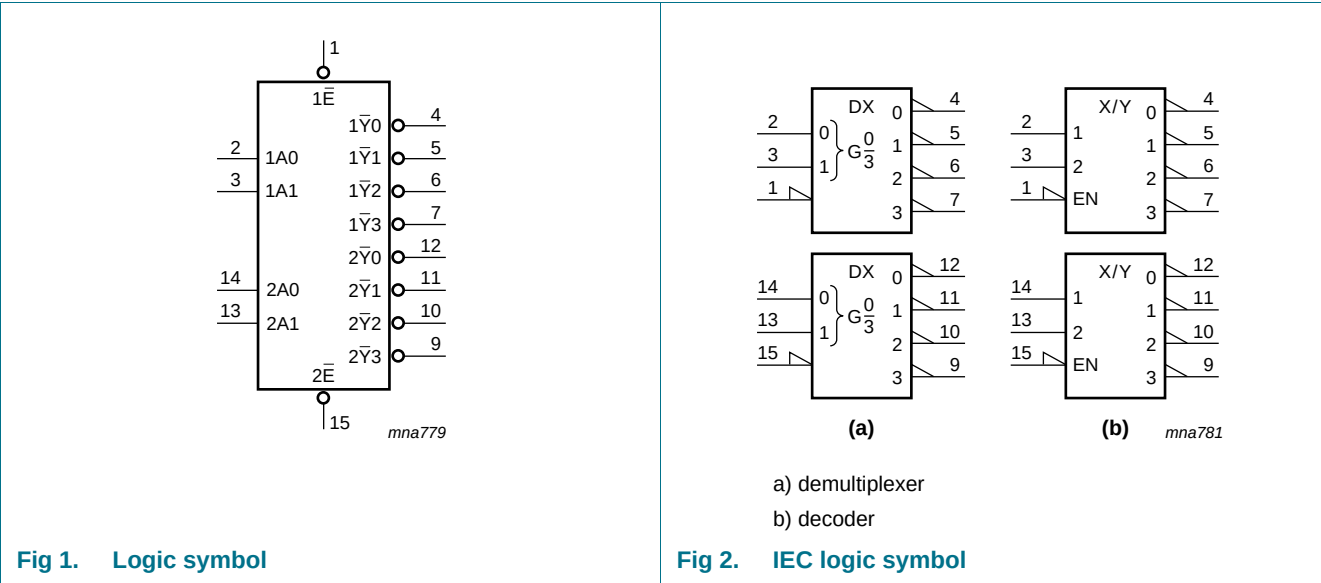
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Two independent 2-to-4 decoders
- Multifunction capability
- Mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
 - ◆ JESD8-7A (1.65 V to 1.95 V)
 - ◆ JESD8-5A (2.3 V to 2.7 V)
 - ◆ JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-B exceeds 200 V
 - ◆ CDM JESD22-C101E exceeds 1000 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

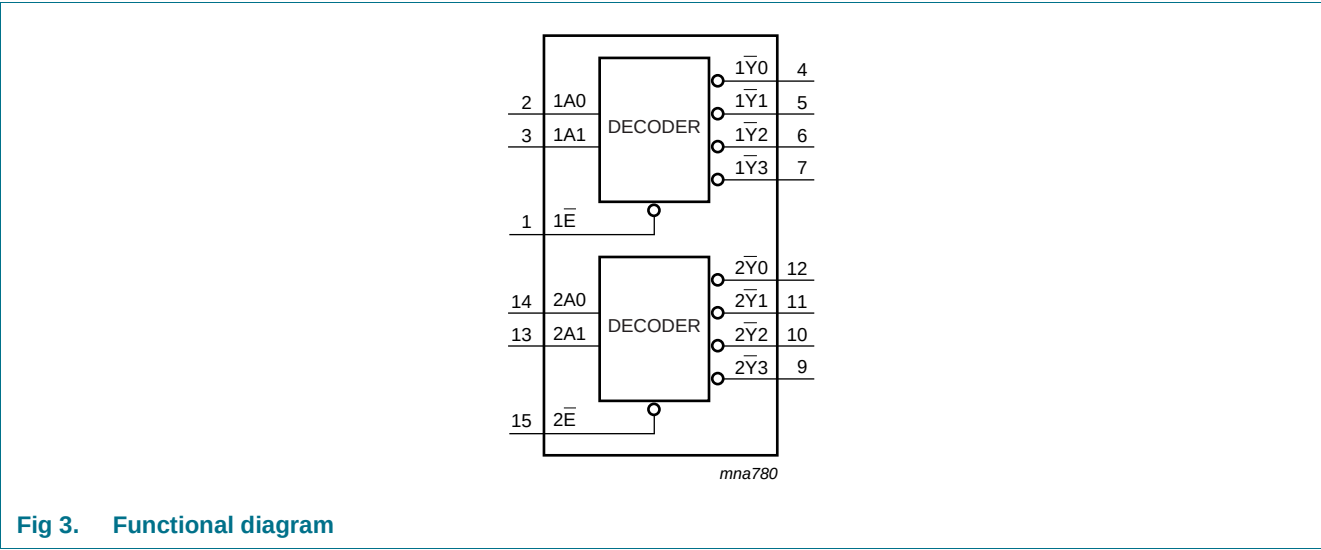
3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC139D	−40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC139DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74LVC139PW	−40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC139BQ	−40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram





5. Pinning information

5.1 Pinning

Fig 4. Pin configuration SO16 and (T)SSOP16

Fig 5. Pin configuration DHVQFN14

5.2 Pin description

Table 2. Pin description

Name	Pin	Description
1E	1	enable input (active LOW)
2E	15	enable input (active LOW)
1A[0:1]	2, 3	address input
2A[0:1]	14, 13	address input
1Y[0:3]	4, 5, 6, 7	output

Table 2. Pin description ...continued

Name	Pin	Description
$\overline{2Y}[0:3]$	12, 11, 10, 9	output
GND	8	ground (0 V)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table^[1]

Input			Output			
n $\overline{E}$	nA0	nA1	n $\overline{Y0}$	n $\overline{Y1}$	n $\overline{Y2}$	n $\overline{Y3}$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	H	L	H	L	H	H
L	L	H	H	H	L	H
L	H	H	H	H	H	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage		^[1] -0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage		^[2] -0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	^[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C derate linearly with 8 mW/K.

For SSOP16 and TSSOP16 packages: above 60 °C derate linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C derate linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40		+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	0.65 × V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
		V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
I _I	input leakage current	I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
		V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA

Table 6. Static characteristics ...continued

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}$; $V_I = V_{CC}$ or GND; $I_O = 0\text{ A}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin ; $V_{CC} = 2.7\text{ V to } 3.6\text{ V}$; $V_I = V_{CC} - 0.6\text{ V}$; $I_O = 0\text{ A}$	-	5	500	-	5000	μA
C_i	input capacitance	$V_{CC} = 0\text{ V to } 3.6\text{ V}$; $V_I = \text{GND to } V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ °C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristicsVoltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			–40 °C to +125 °C		Unit
			Min	Typ ^[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to $\bar{Y}_n$; see Figure 6 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	0.5	4.7	10.4	0.5	11.3	ns
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.0	2.8	5.9	1.0	6.5	ns
		$V_{CC} = 2.7\text{ V}$	1.0	3.0	6.3	1.0	8.0	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.5	5.3	1.0	7.0	ns
		$n\bar{E}$ to $\bar{Y}_n$; see Figure 7 ^[2]						
		$V_{CC} = 1.2\text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	1.5	4.5	9.8	1.5	10.7	ns
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	2.1	2.7	5.6	2.1	6.1	ns
		$V_{CC} = 2.7\text{ V}$	1.0	2.8	5.4	1.0	7.0	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.4	5.0	1.0	6.5	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$ ^[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ ^[4]						
		$V_{CC} = 1.65\text{ V to } 1.95\text{ V}$	-	5.6	-	-	-	pF
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	-	11.3	-	-	-	pF
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	-	16.4	-	-	-	pF

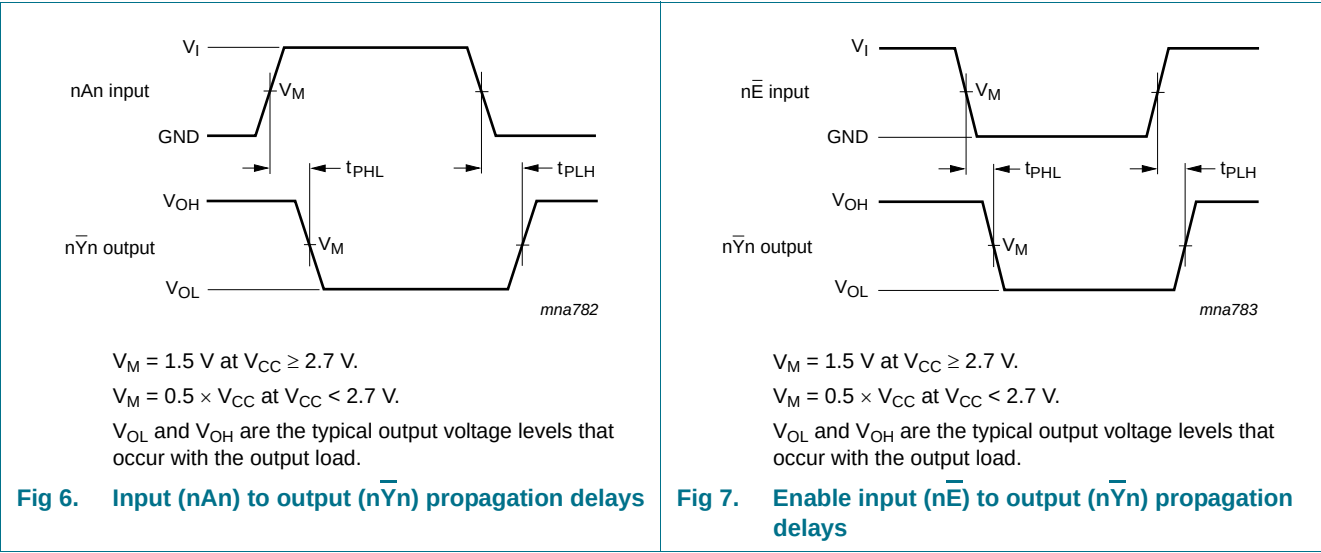
[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and $V_{CC} = 1.2\text{ V}$, 1.8 V , 2.5 V , 2.7 V , and 3.3 V respectively.[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

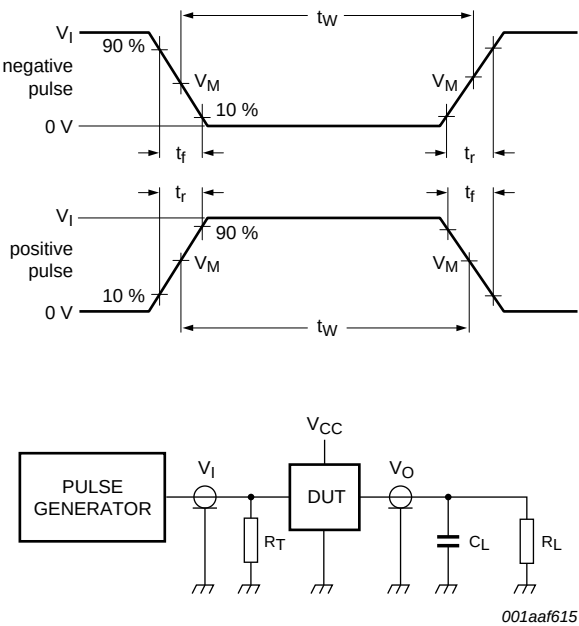
[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; f_o = output frequency in MHz C_L = output load capacitance in pF V_{CC} = supply voltage in V N = number of inputs switching,

$\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

11. Waveforms





Test data is given in [Table 8](#).
Definitions for test circuit:
 R_L = Load resistance.
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Load circuitry for switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	$\leq 2 \text{ ns}$	30 pF	500 Ω
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

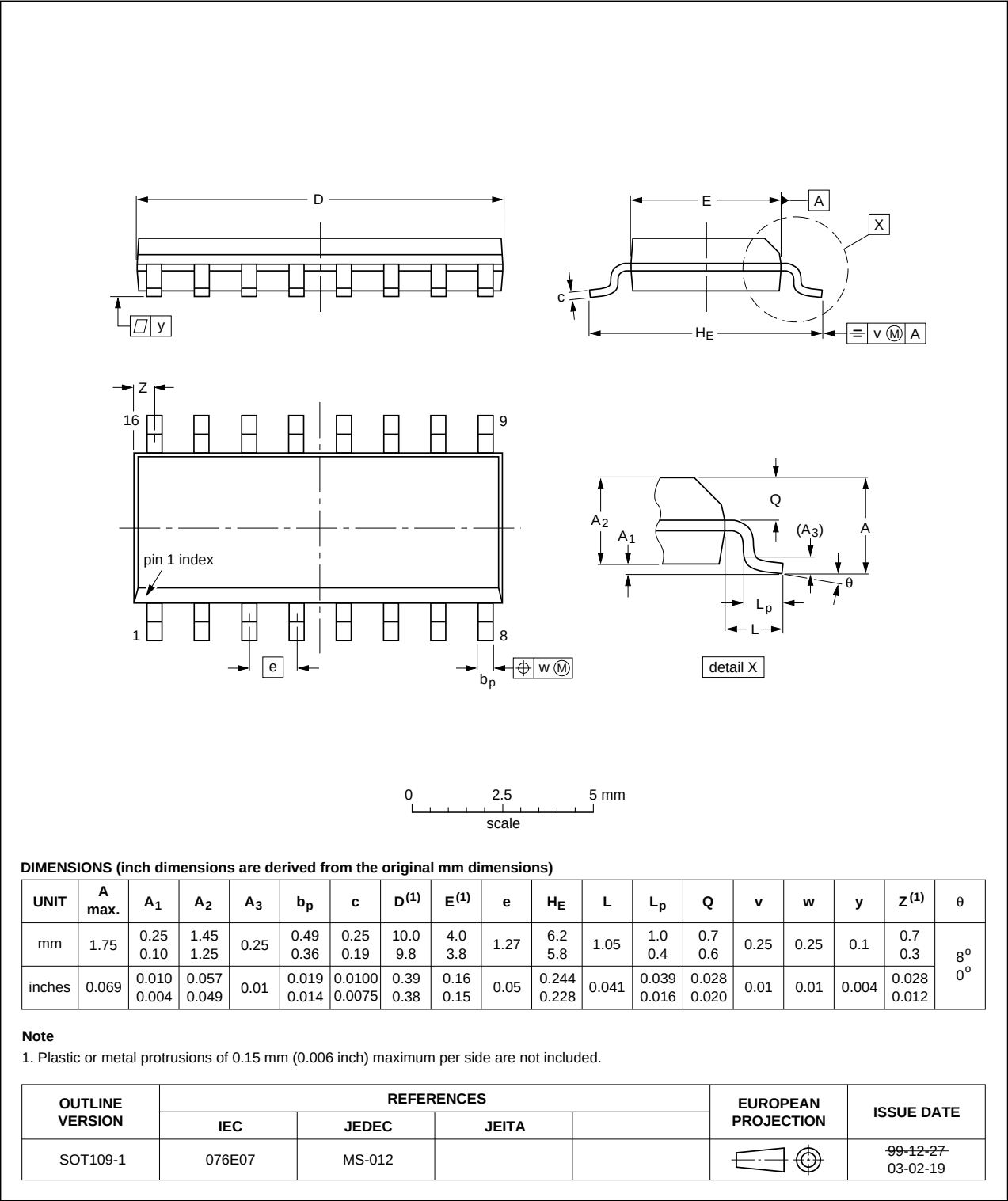


Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

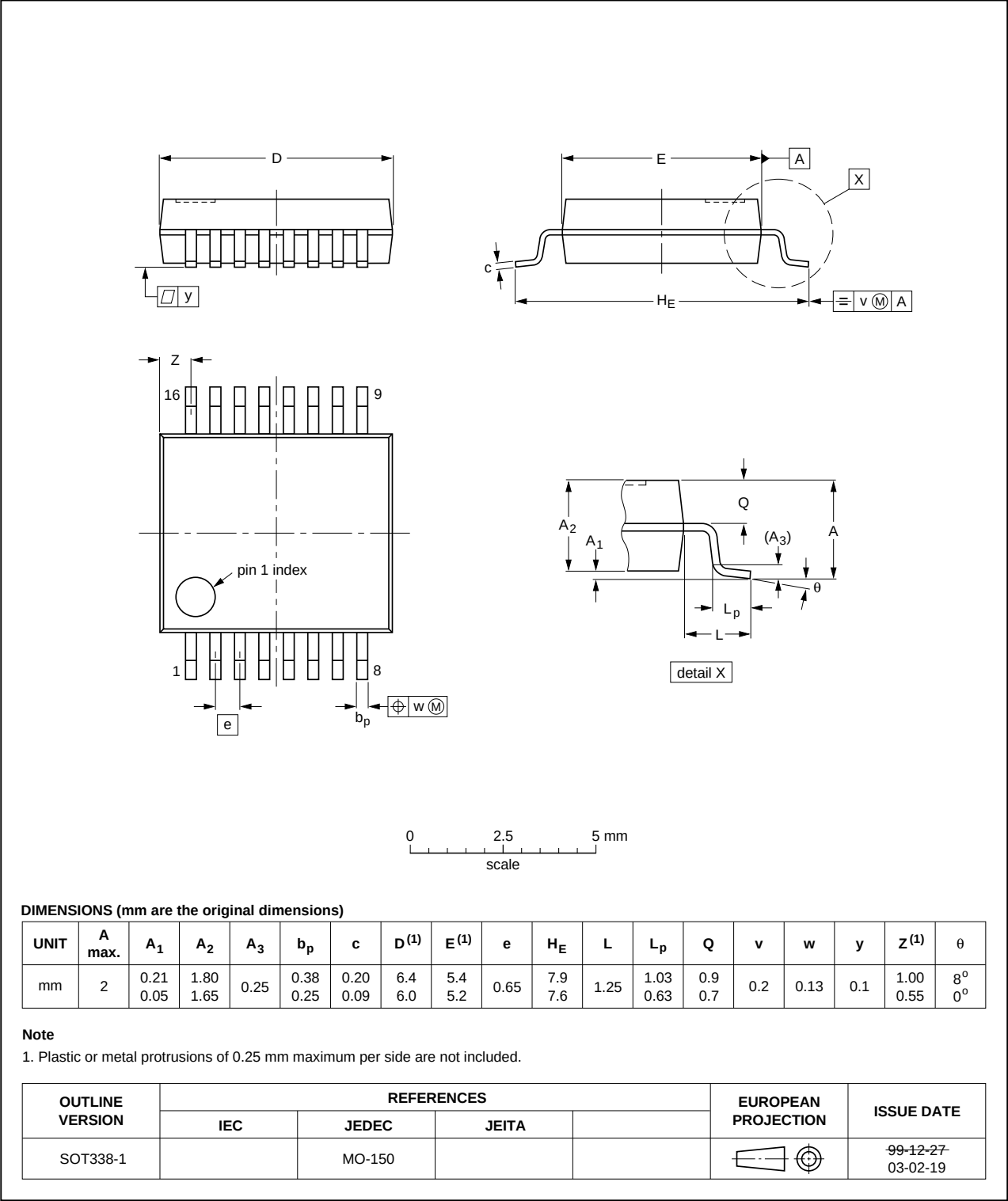


Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

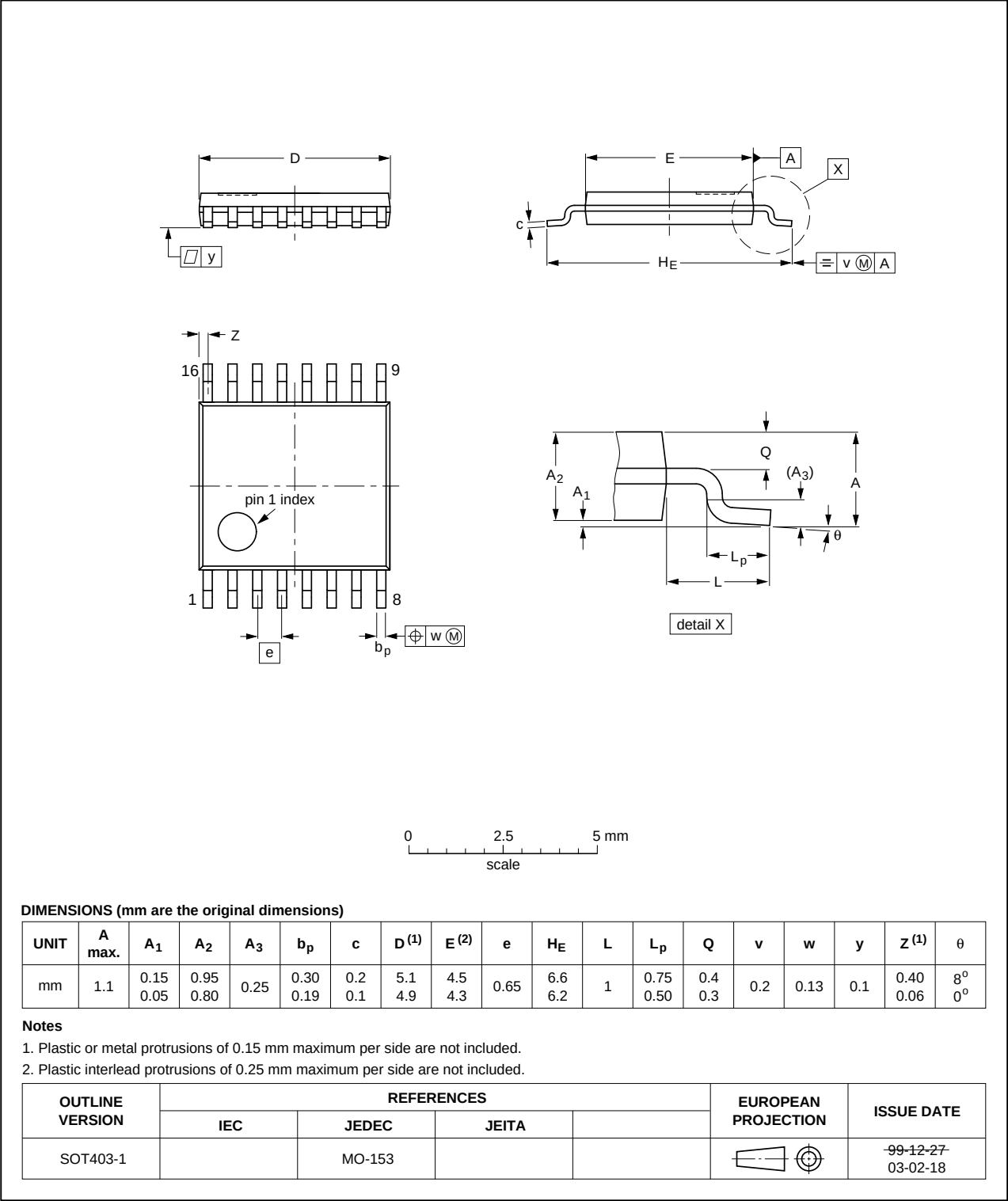


Fig 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

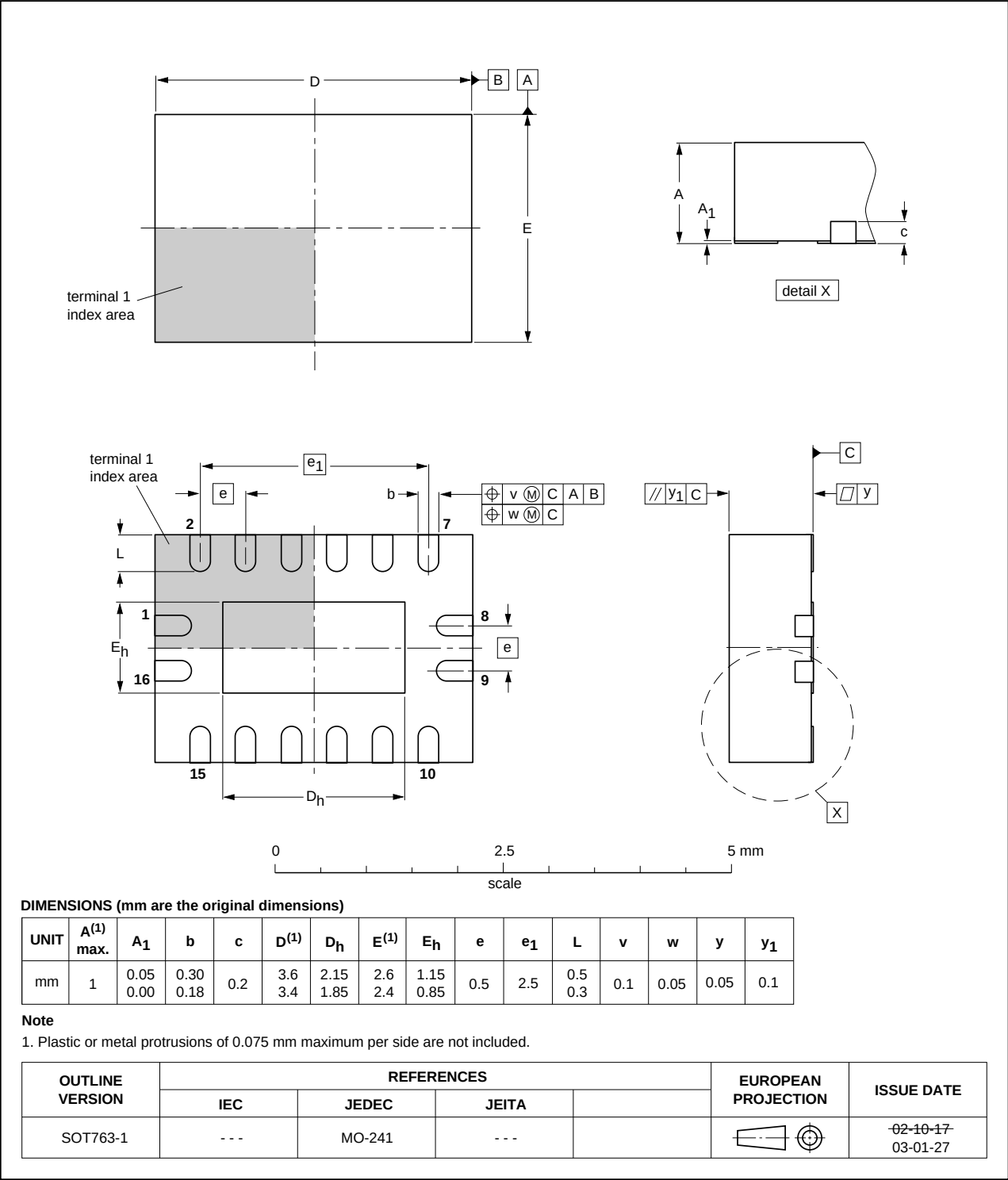


Fig 12. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC139 v.5	20111019	Product data sheet	-	74LVC139 v.4
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. Table 4, Table 5, Table 6, Table 7 and Table 8: values added for lower voltage ranges.			
74LVC139 v.4	040315	Product specification	-	74LVC139 v.3
74LVC139 v.3	030519	Product specification	-	74LVC139 v.2
74LVC139 v.2	980428	Product specification	-	74LVC139 v.1
74LVC139 v.1	-	-	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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