



**THE DATASHEET OF  
PH8230E,115**



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Kind regards,

Team Nexperia

## 1. Product profile

### 1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

### 1.2 Features and benefits

- Higher operating power due to low thermal resistance
- Low conduction losses due to low on-state resistance
- Simple gate drive required due to low gate charge

### 1.3 Applications

- DC-to-DC convertors
- Notebook computers
- Portable equipment
- Switched-mode power supplies

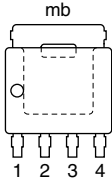
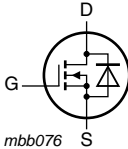
### 1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 150\text{ °C}$	-	-	30	V
$I_D$	drain current	$T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V};$ see <a href="#">Figure 1</a> and <a href="#">3</a>	-	-	67	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ see <a href="#">Figure 2</a>	-	-	62.5	W
<b>Dynamic characteristics</b>						
$Q_{GD}$	gate-drain charge	$V_{GS} = 5\text{ V}; I_D = 20\text{ A}; V_{DS} 10\text{ V};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 11</a>	-	5	-	nC
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 10\text{ A};$ $T_j = 25\text{ °C};$ see <a href="#">Figure 9</a> and <a href="#">10</a>	-	7.6	8.2	m $\Omega$

## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source		
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

**SOT669 (LFAK)**

## 3. Ordering information

Table 3. Ordering information

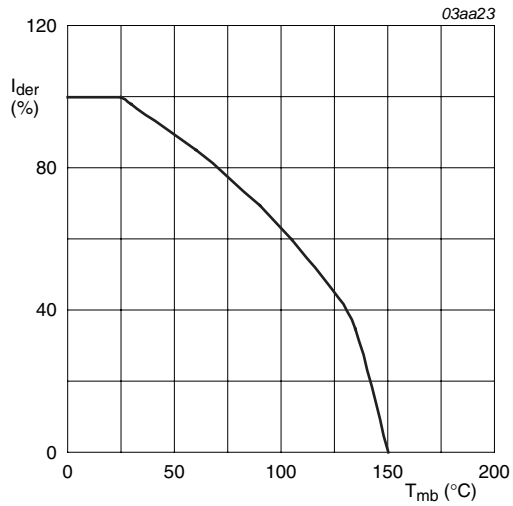
Type number	Package		Version
	Name	Description	
PH8230E	LFAK	plastic single-ended surface-mounted package (LFAK); 4 leads	SOT669

## 4. Limiting values

Table 4. Limiting values

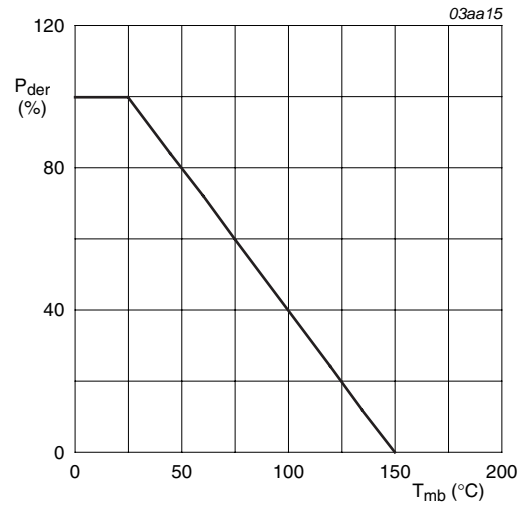
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	30	V
$V_{GS}$	gate-source voltage		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; see <a href="#">Figure 1</a>	-	42	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> and <a href="#">3</a>	-	67	A
$I_{DM}$	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 3</a>	-	268	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	62.5	W
$T_{stg}$	storage temperature		-55	150	°C
$T_j$	junction temperature		-55	150	°C
<b>Source-drain diode</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	52	A
$I_{SM}$	peak source current	$t_p \leq 10\text{ }\mu\text{s}$ ; pulsed; $T_{mb} = 25\text{ °C}$	-	150	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{GS} = 10\text{ V}$ ; $T_{j(\text{init})} = 25\text{ °C}$ ; $I_D = 33.9\text{ A}$ ; $V_{sup} = 30\text{ V}$ ; $t_p = 0.15\text{ ms}$ ; unclamped	-	115	mJ



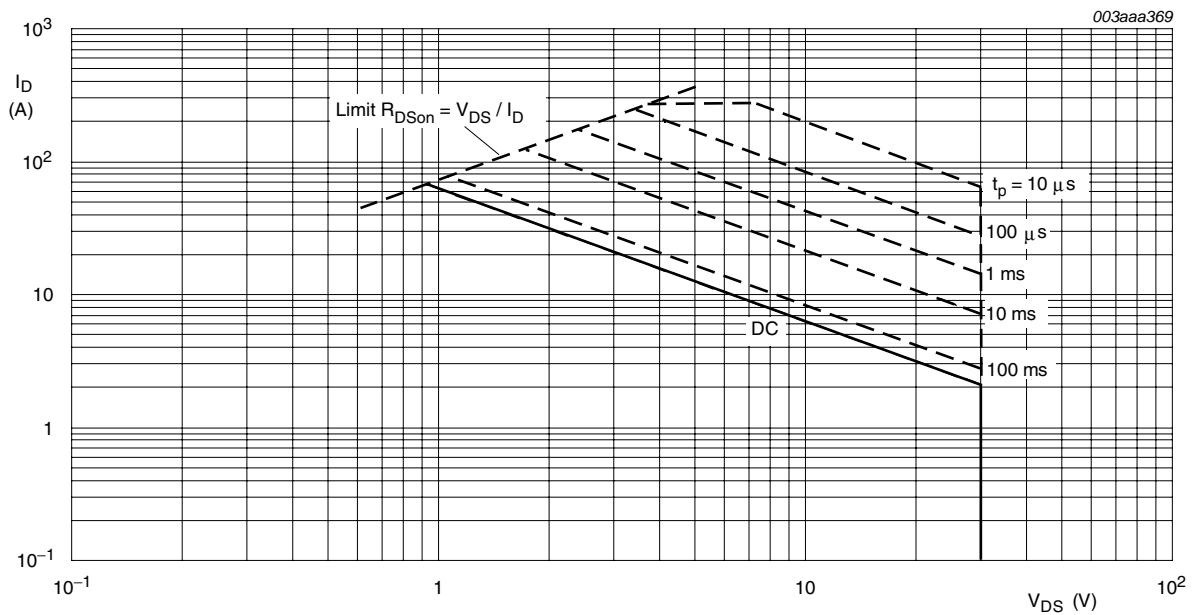
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



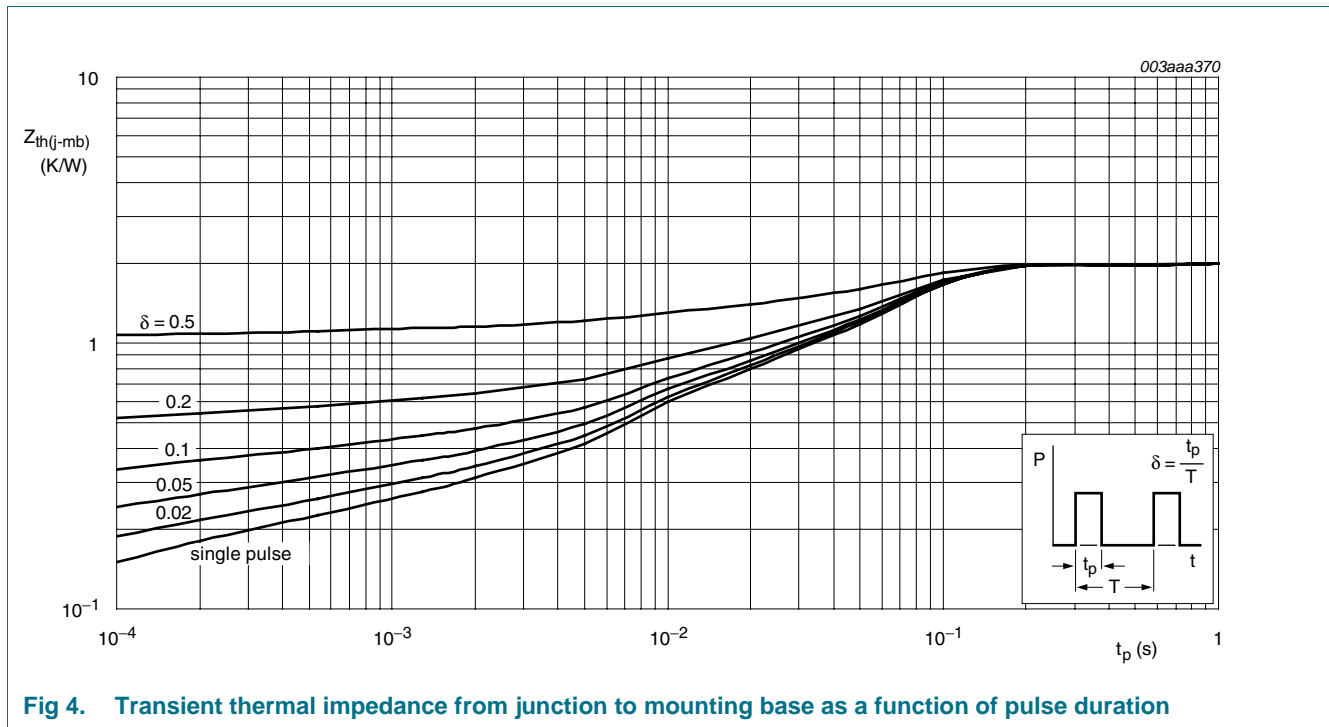
$T_{mb} = 25^\circ\text{C}; I_{DM}$  is single pulse;  $V_{GS} = 10\text{V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

### 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see <a href="#">Figure 4</a>	-	-	2	K/W



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 6. Characteristics

**Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	0.5	-	-	V
		$I_D = 1 \text{ mA}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 8</a>	1	1.7	2.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	0.06	1	$\mu A$
		$V_{DS} = 30 V$ ; $V_{GS} = 0 V$ ; $T_j = 150 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	20	100	nA
		$V_{GS} = -20 V$ ; $V_{DS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$	-	20	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 V$ ; $I_D = 10 A$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	7.6	8.2	m $\Omega$
		$V_{GS} = 10 V$ ; $I_D = 10 A$ ; $T_j = 150 \text{ }^\circ C$ ; see <a href="#">Figure 9</a> and <a href="#">10</a>	-	13	14	m $\Omega$
		$V_{GS} = 4.5 V$ ; $I_D = 10 A$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 10</a>	-	11	13.2	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 20 A$ ; $V_{DS} = 10 V$ ; $V_{GS} = 5 V$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	14	-	nC
$Q_{GS}$	gate-source charge		-	5.7	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 20 A$ ; $V_{DS} = 10 V$ ; $V_{GS} = 5 V$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 11</a>	-	5	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 10 V$ ; $V_{GS} = 0 V$ ; $f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 12</a>	-	1400	-	pF
$C_{oss}$	output capacitance		-	527	-	pF
$C_{rss}$	reverse transfer capacitance		-	235	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 10 V$ ; $R_L = 1.0 \Omega$ ; $V_{GS} = 4.5 V$ ; $R_{G(ext)} = 4.7 \Omega$ ; $T_j = 25 \text{ }^\circ C$ ; $I_D = 10 A$	-	28	-	ns
$t_r$	rise time		-	44	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
$t_f$	fall time		-	21	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 10 A$ ; $V_{GS} = 0 V$ ; $T_j = 25 \text{ }^\circ C$ ; see <a href="#">Figure 13</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 20 A$ ; $di_S/dt = -100 A/\mu s$ ; $V_{GS} = 0 V$ ; $V_{DS} = 20 V$ ; $T_j = 25 \text{ }^\circ C$	-	38	-	ns

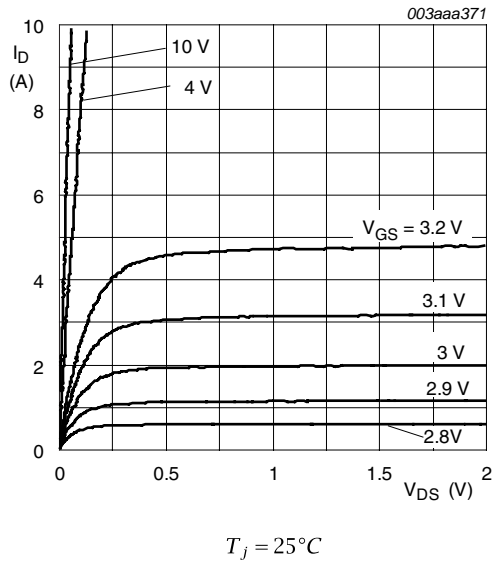


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

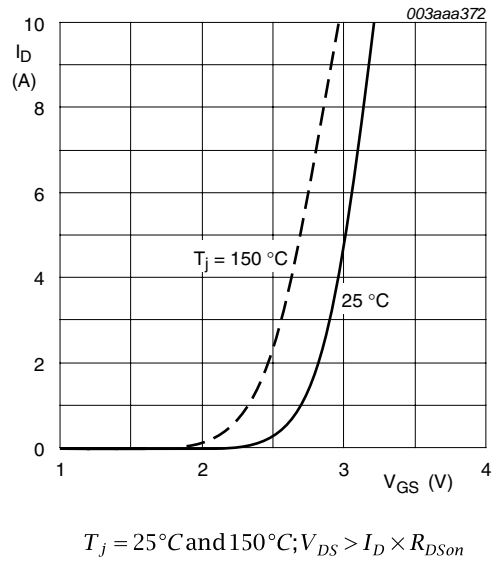


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

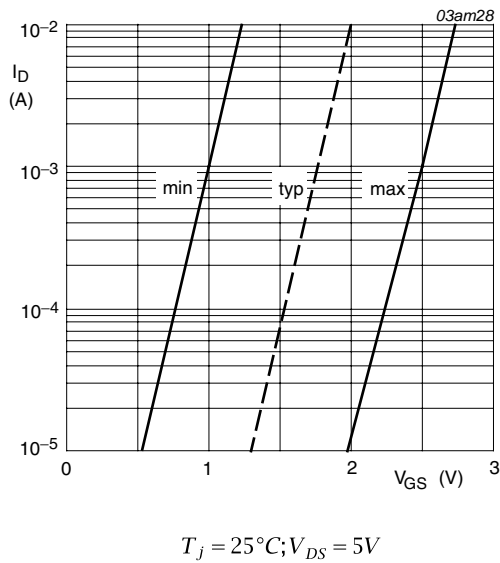


Fig 7. Sub-threshold drain current as a function of gate-source voltage

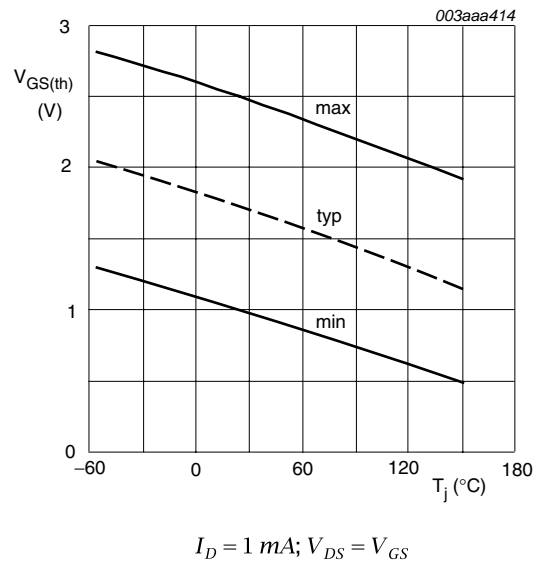
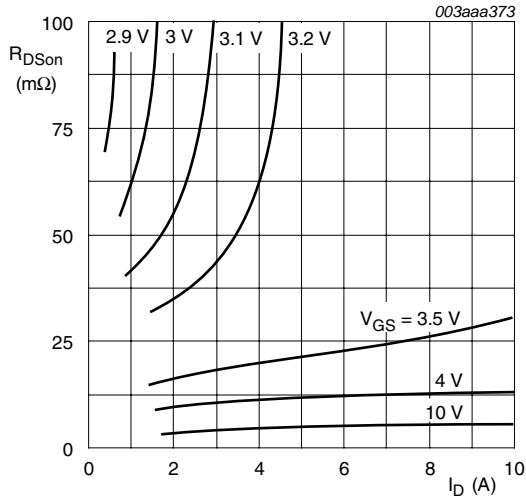
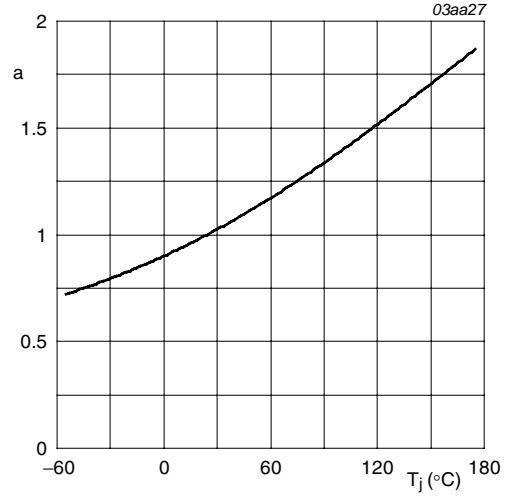


Fig 8. Gate-source threshold voltage as a function of junction temperature



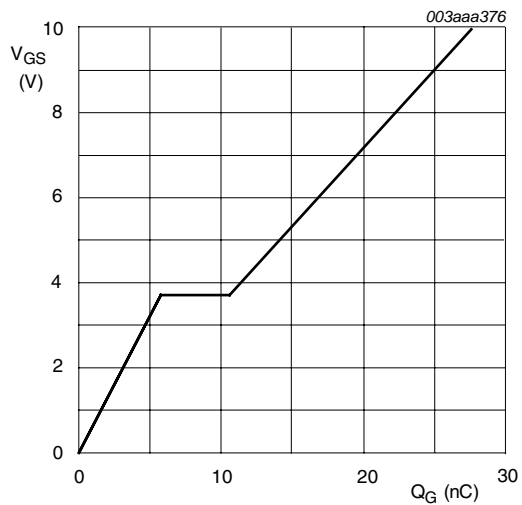
$T_j = 25^\circ C$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



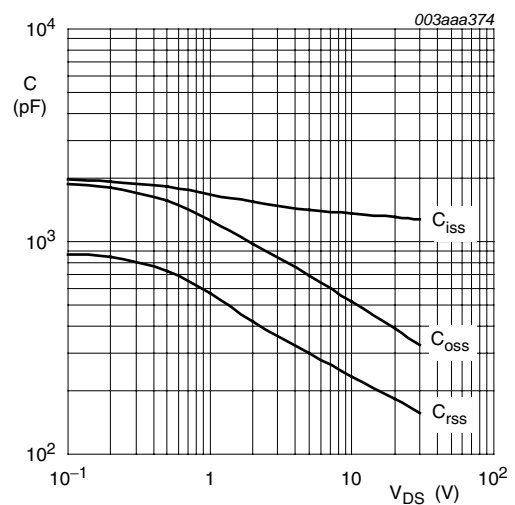
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



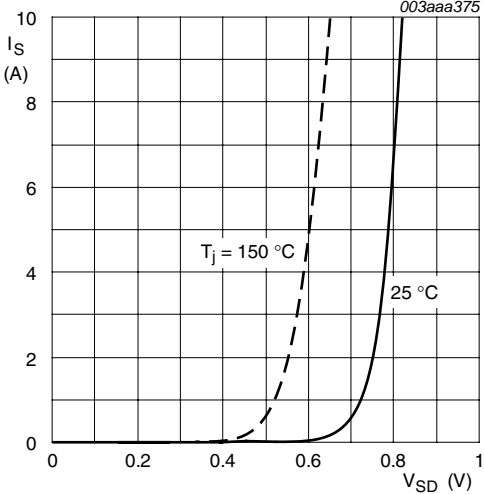
$I_D = 20A; V_{DS} = 10V$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0V; f = 1MHz$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (LFPAK); 4 leads

SOT669

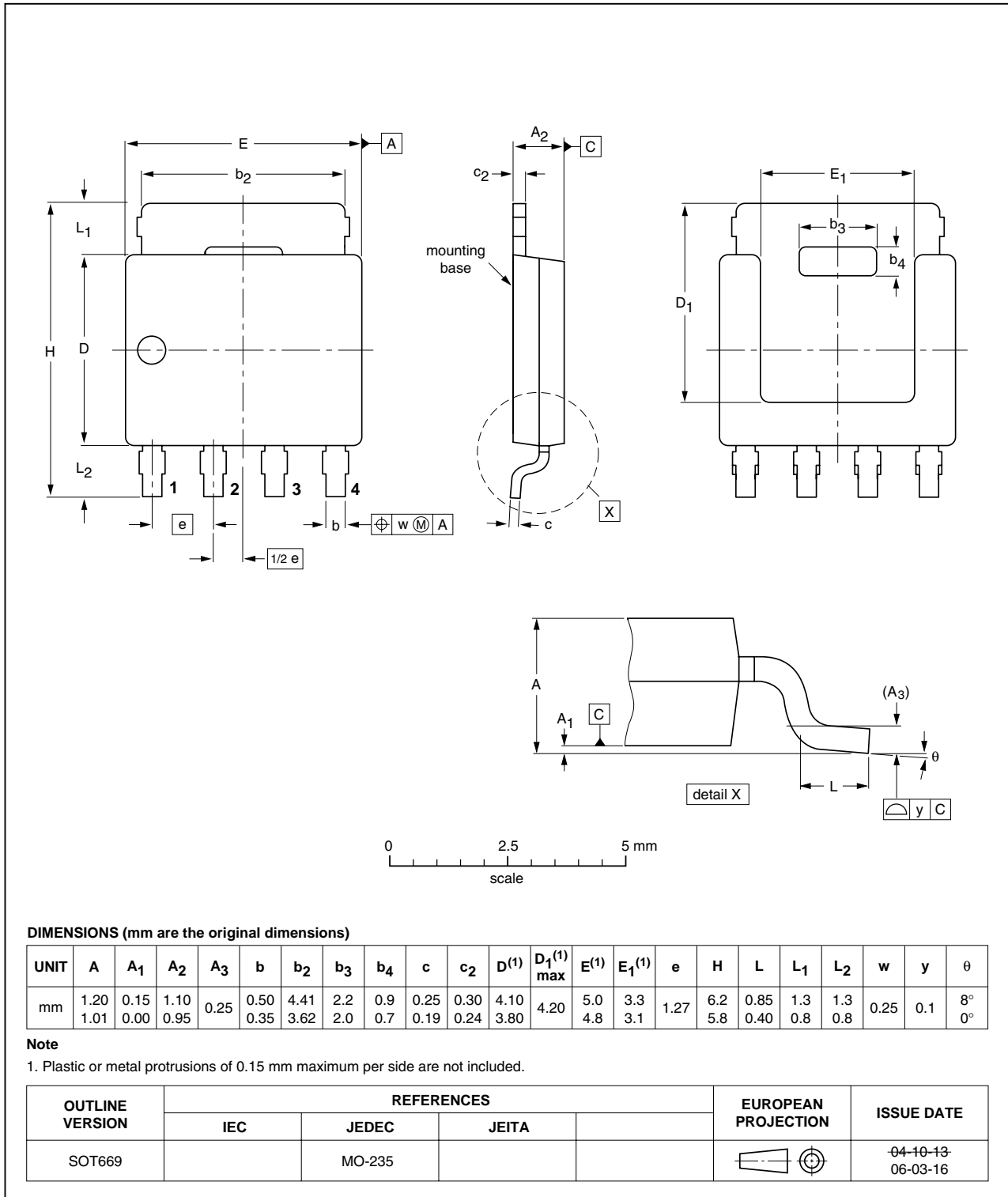


Fig 14. Package outline SOT669 (LFPAK)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PH8230E_4	20091117	Product data sheet	-	PH8230E-03
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>		
PH8230E-03	20040302	Product data	-	PH8230E-02
PH8230E-02	20030429	Product data	-	PH8230E-01
PH8230E-01	20030304	Preliminary data	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 11. Contents

<b>1</b>	<b>Product profile</b> . . . . .	<b>1</b>
1.1	General description . . . . .	1
1.2	Features and benefits . . . . .	1
1.3	Applications . . . . .	1
1.4	Quick reference data . . . . .	1
<b>2</b>	<b>Pinning information</b> . . . . .	<b>2</b>
<b>3</b>	<b>Ordering information</b> . . . . .	<b>2</b>
<b>4</b>	<b>Limiting values</b> . . . . .	<b>2</b>
<b>5</b>	<b>Thermal characteristics</b> . . . . .	<b>4</b>
<b>6</b>	<b>Characteristics</b> . . . . .	<b>5</b>
<b>7</b>	<b>Package outline</b> . . . . .	<b>9</b>
<b>8</b>	<b>Revision history</b> . . . . .	<b>10</b>
<b>9</b>	<b>Legal information</b> . . . . .	<b>11</b>
9.1	Data sheet status . . . . .	11
9.2	Definitions . . . . .	11
9.3	Disclaimers . . . . .	11
9.4	Trademarks . . . . .	11
<b>10</b>	<b>Contact information</b> . . . . .	<b>11</b>

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