THE DATASHEET OF

MC33565DR2

MC33565

Smart Voltage Regulator for Peripheral Card Applications

The MC33565 Low Drop Out Voltage Regulator is designed for computer peripheral card applications, allowing glitch−free transitions from “sleep” to “active” system modes. It has internal logic circuitry to detect whether there is a 5.0 V supply (“active” system mode) or an auxiliary 3.3 V supply (“sleep” system mode). A guaranteed 3.3 V regulated output voltage at 200 mA is always available even if the main 5.0 V supply drops out.

The regulated 3.3 V output voltage is provided by either an internal low dropout voltage regulator or an external P−channel MOSFET switch, depending on the system being in the “active” or “sleep” mode.

Features

- Glitch−Free Transition from “Sleep” to “Active” Mode
- Compatible with *Instantly Available* PC Systems
- Output Current up to 200 mA
- Output Regulated to 2% over Temperature
- Excellent Line and Load Regulation (0.4%)
- Prevents Reverse Current Flow during Sleep Mode
- Short Circuit Protection
- Pb−Free Packages are Available

Applications

- Computer
- Ethernet
- PCI/NIC Cards

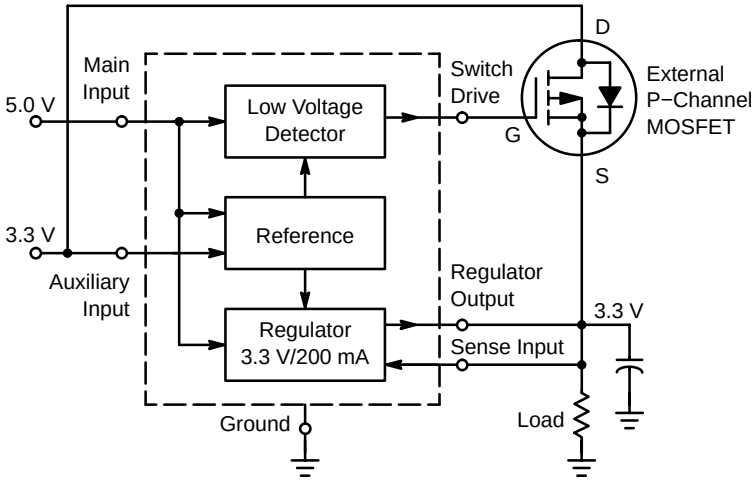


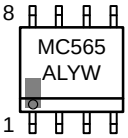
Figure 1. Simplified Block Diagram

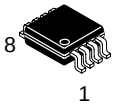
ON Semiconductor®

http://onsemi.com

MARKING DIAGRAMS

SOIC−8
D SUFFIX
CASE 751

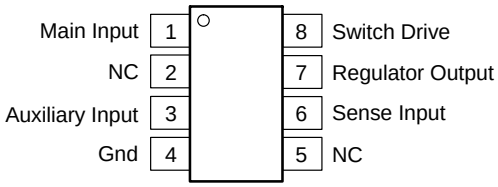




Micro8™
(MSOP−8)
DM SUFFIX
CASE 846A

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

PIN CONNECTIONS



Pins 2 and 5 are not internally connected

ORDERING INFORMATION

Device	Package	Shipping†
MC33565D	SOIC−8	98 Units / Rail
MC33565DR2	SOIC−8	2500 / Tape & Reel
MC33565DMR2	Micro8	4000 / Tape & Reel
MC33565DG	SOIC−8 (Pb−Free)	98 Units / Rail
MC33565DR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
MC33565DMR2G	Micro8 (Pb−Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

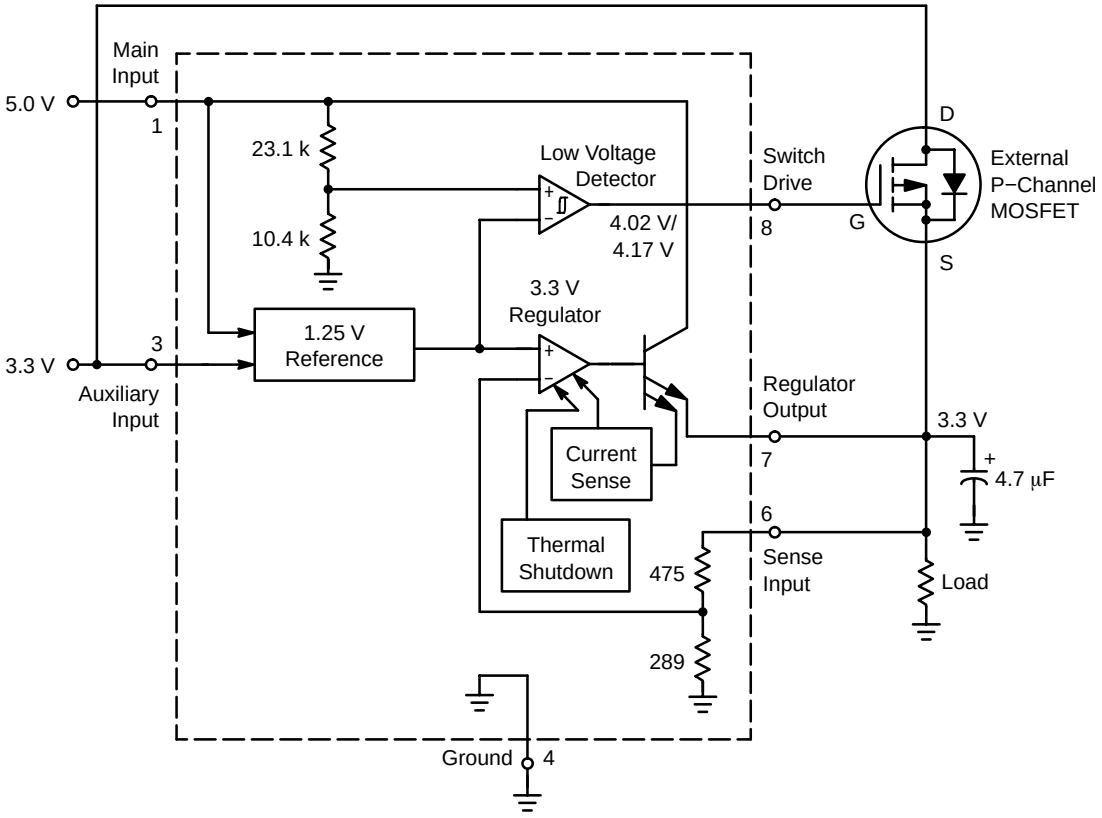


Figure 2. Functional Block Diagram

PIN ASSIGNMENTS AND FUNCTIONS

PIN #	FUNCTION	PIN DESCRIPTION
1	Main Input	This input connects to the system main power source, typically 5.0 V.
2, 5	NC	No connection. These pins are not internally connected.
3	Auxiliary Input	This input connects to the system auxiliary power source, typically 3.3 V.
4	Gnd	This is the regulator and control circuit power ground.
6	Sense Input	The sense input connects directly to the load allowing precise regulation.
7	Regulator Output	This output is precisely regulated at 3.3 V and is capable of up to 200 mA.
8	Switch Drive	This output is designed to drive the gate of an external P−channel MOSFET switch.

MAXIMUM RATINGS (Notes 1, 2)

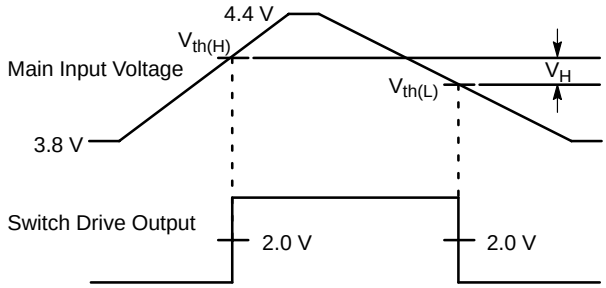
Rating	Symbol	Value	Unit
Main Input Voltage Range (Pin 1)	$V_{in(M)}$	−0.5 to +7.0	V
Auxiliary Input Voltage Range (Pin 3)	$V_{in(A)}$	−0.5 to +7.0	V
Thermal Resistance Junction to Air D Suffix, SOIC−8, Case 751 DM Suffix, MSOP−8, Case 846A	$R_{\theta JA}$	 146 172	°C/W
Operating Junction Temperature Range	T_J	−5.0 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C

ELECTRICAL CHARACTERISTICS ($V_{in(A)}$ = 3.3 V, $V_{in(M)}$ = 5.0 V, Pin 6 connected to Pin 7, $C_{pin6,7}$ = 4.7 μF, for typical values T_J = 25°C, for min/max values T_J = −5.0°C to 150°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
MAIN INPUT (Pin 1)					
Operating Voltage Range	$V_{in(M)}$	4.3	5.0	5.5	V
Quiescent Current (I_O = 0 mA)	$I_{Q(M)}$	−	8.0	10	mA
Output to Input Reverse Leakage Current ($V_{in(M)}$ = 0 V, V_{out} = 3.5 V, T_J = 25°C)	I_L	−	1.4	25	μA
AUXILIARY INPUT (Pin 3)					
Quiescent Current (I_O = 0 mA)	$I_{Q(A)}$	−	1.9	3.0	mA
REGULATOR OUTPUT (Pin 7)					
Output Voltage (I_O = 0 mA to 200 mA, Note 3) $V_{in(M)}$ = 4.3 V to 5.5 V T_A = 25°C T_J = −5.0°C to 150°C $V_{in(M)} = V_{th(L)}$ $V_{in(M)}$ = 7.0 V	V_{out}	 3.267 3.234 3.0 3.1	 3.3 3.3 − 3.3	 3.333 3.366 − 3.5	V
Line Regulation	Reg_{line}	−	1.5	13.2	mV
Load Regulation	Reg_{load}	−	1.9	13.2	mV
Short Circuit Current (T_J = 25°C, Note 3)	I_{SC}	230	750	800	mA
LOW VOLTAGE DETECTOR (Pins 1, 8)					
Input Threshold Voltage (Figure 3) Output Low State Transition, $V_{in(M)}$ Decreasing Output High State Transition, $V_{in(M)}$ Increasing Hysteresis	 $V_{th(L)}$ $V_{th(H)}$ V_H	 3.9 − 0.120	 4.02 4.17 0.150	 4.3 4.3 0.180	V
SWITCH DRIVE OUTPUT (Pin 8)					
Output Voltage Low State ($V_{in(M)}$ = 0 V, $V_{in(A)}$ = 3.3 V, I_{sink} = 200 μA) High State ($V_{in(M)}$ = 5.0 V, $V_{in(A)}$ = 0 V, I_{source} = 200 μA)	 $V_{O(L)}$ $V_{O(H)}$	 − 3.4	 0.044 4.15	 0.2 −	V
Peak Output Current (C_L = 1.2 nF) Sink Current ($V_{in(M)}$ = 3.9 V, V_O = 1.0 V) Source Current ($V_{in(M)}$ = 4.3 V, V_O = 2.3 V)	 $I_{sink(PK)}$ $I_{source(PK)}$	 15 15	 22 39	 − −	mA
Propagation Delay, Main Input to Switch Drive Output (Figure 4) C_L = 1.2 nF Switch Drive Output Fall ($V_{in(M)}$ Decreasing) Switch Drive Output Rise ($V_{in(M)}$ Increasing)	 t_{DL} t_{DH}	 − −	 0.65 1.4	 3.5 3.5	μs

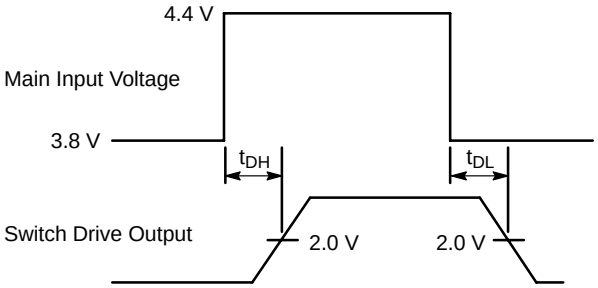
1. Maximum Ratings are those values beyond which damage to the device may occur.
2. This device series contains ESD protection and exceed the following tests:
   Human Body Model 2500 V per MIL STD 883, Method 3015.
   Machine Model Method 400 V.
3. Thermal shutdown activation can occur when the maximum operating junction temperature is exceeded.

TYPICAL CHARACTERISTICS



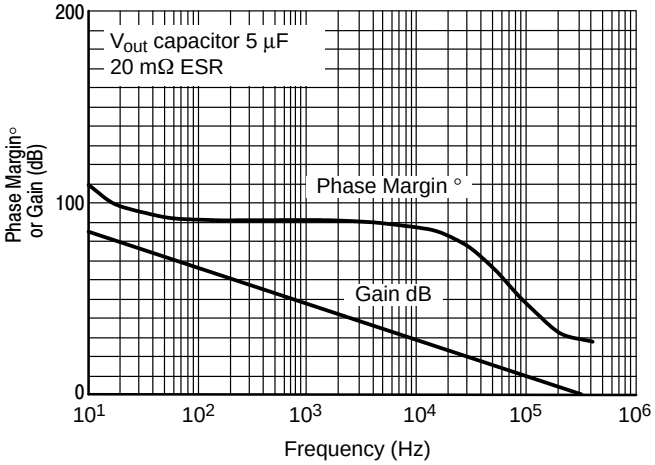
$V_{in(M)}$ rise and fall times (10% to 90%) to be ≥ 100 μs.

Figure 3. Low Voltage Detector Thresholds



$V_{in(M)}$ rise and fall times (10% to 90%) to be ≤ 100 ns.

Figure 4. Switch Drive to Main Input Timing Diagram



V_{out} capacitor ≥ 4.7 μF over operating temperature range. Maximum ESR permissible = 500 mΩ over operating temperature range.

Figure 5. Predicted Gain and Phase at Zero Load Current

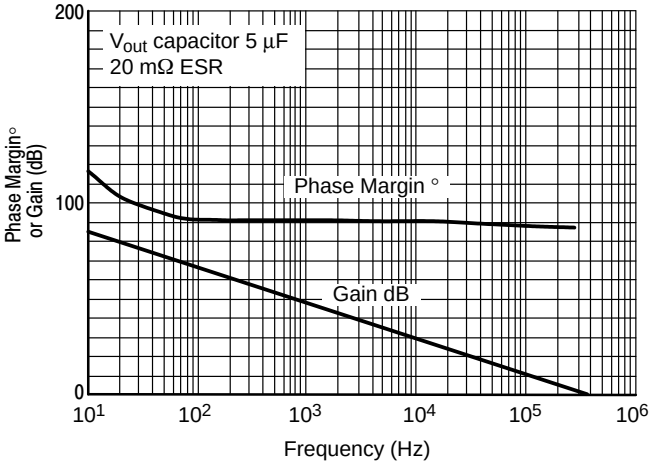


Figure 6. Predicted Gain and Phase at Full Load Current

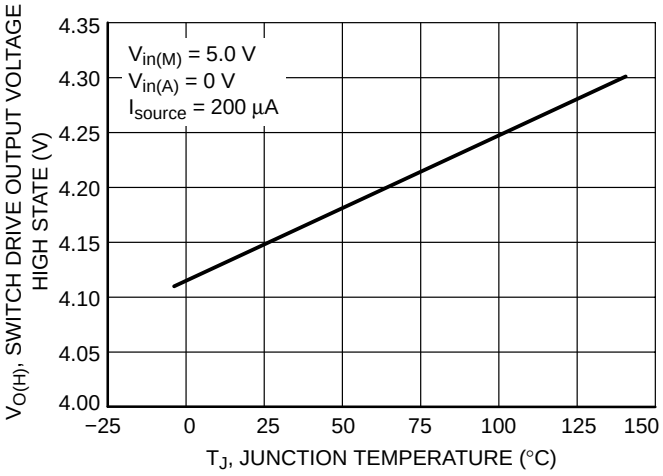


Figure 7. Switch Drive Output Voltage High State (external P−channel MOSFET turned off) vs. Junction Temperature

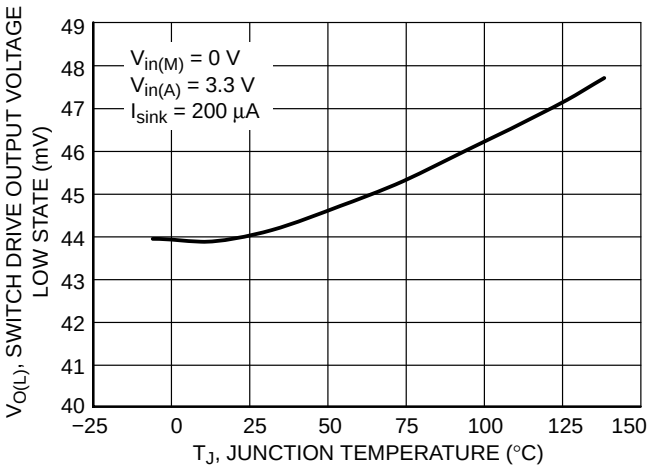


Figure 8. Switch Drive Output Voltage Low State (external P−channel MOSFET turned on) vs. Junction Temperature

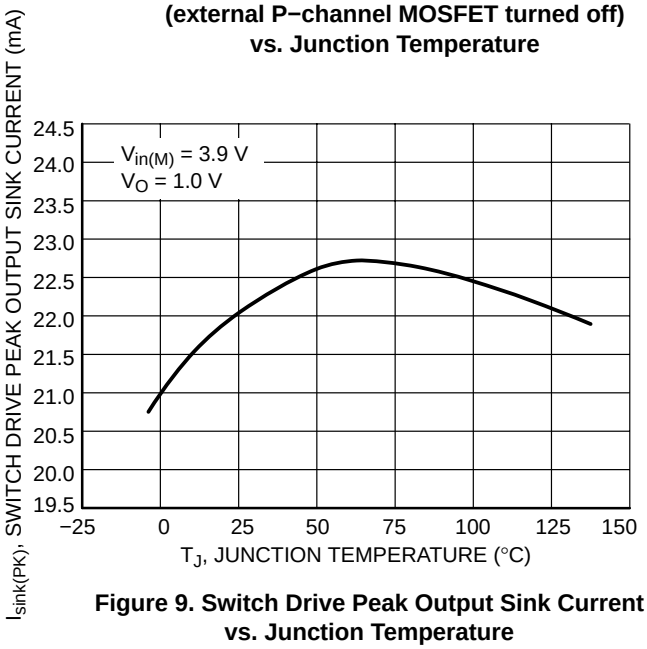


Figure 9. Switch Drive Peak Output Sink Current vs. Junction Temperature

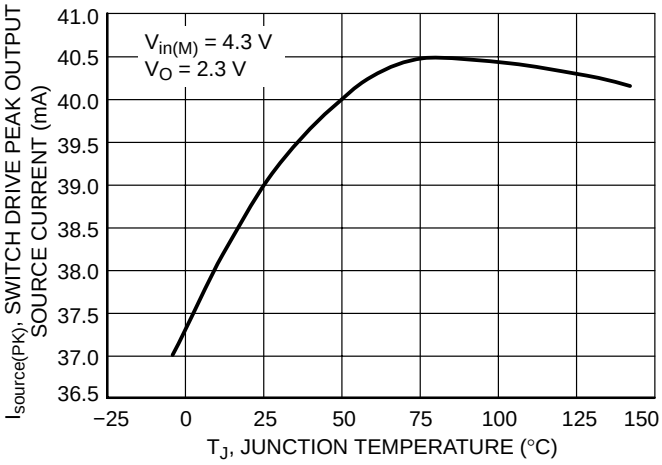


Figure 10. Switch Drive Peak Output Source Current vs. Junction Temperature

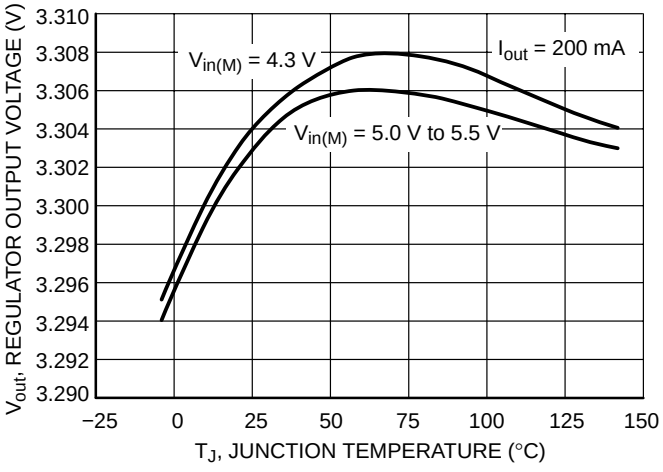


Figure 11. Regulator Output Voltage vs. Junction Temperature

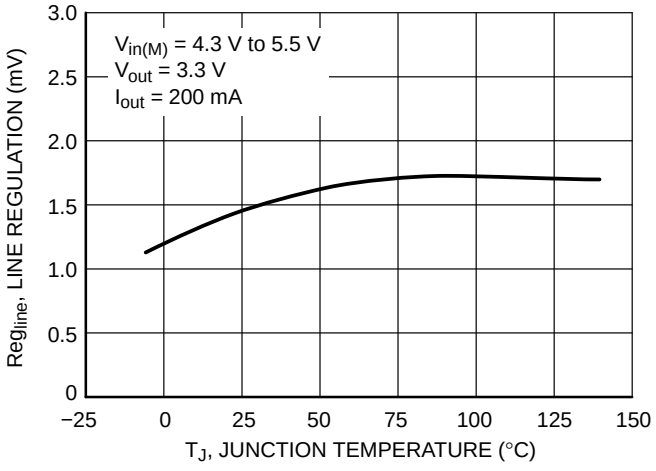


Figure 12. Line Regulation vs. Junction Temperature

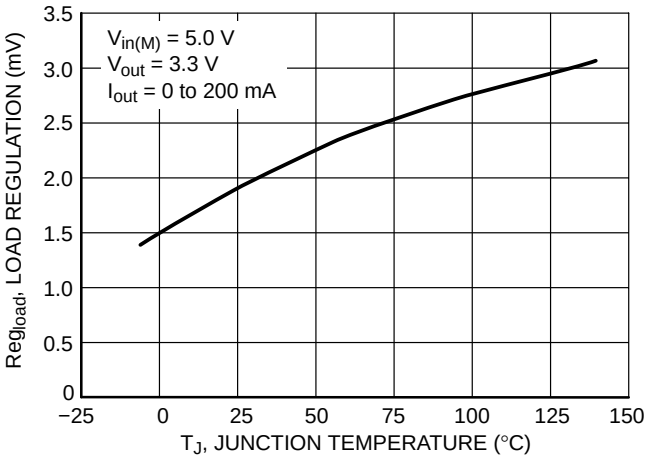


Figure 13. Load Regulation vs. Junction Temperature

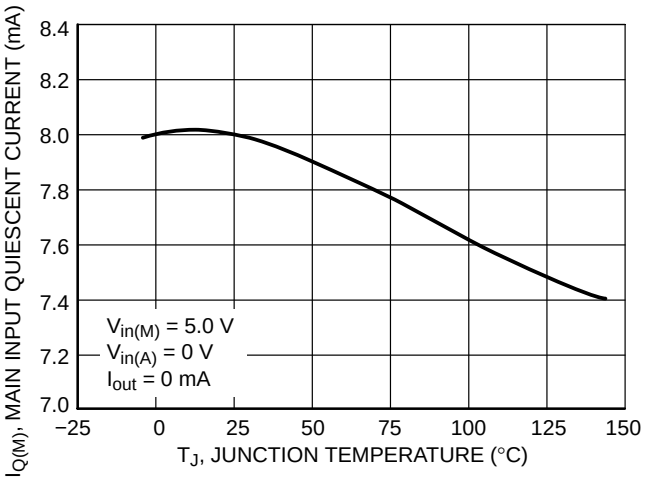


Figure 14. Main Input Quiescent Current vs. Junction Temperature

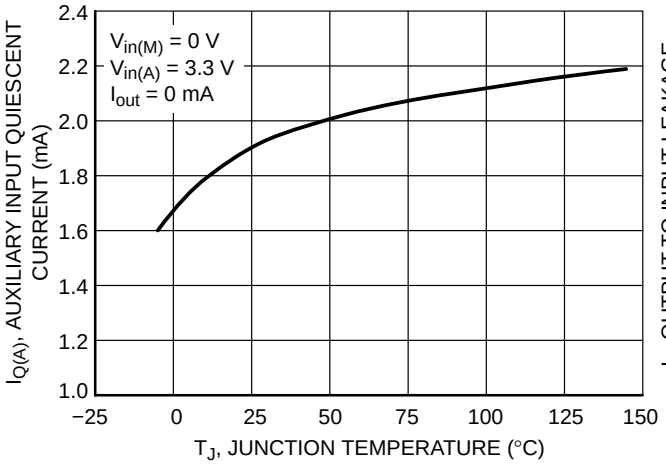


Figure 15. Auxiliary Input Quiescent Current vs. Junction Temperature

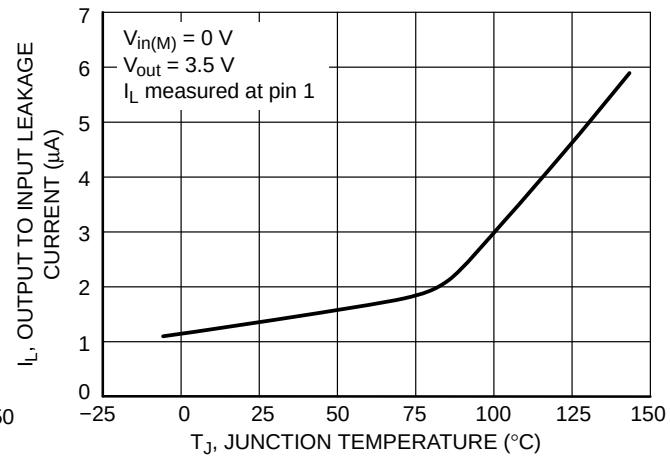


Figure 16. Output to Input Reverse Leakage Current vs. Junction Temperature

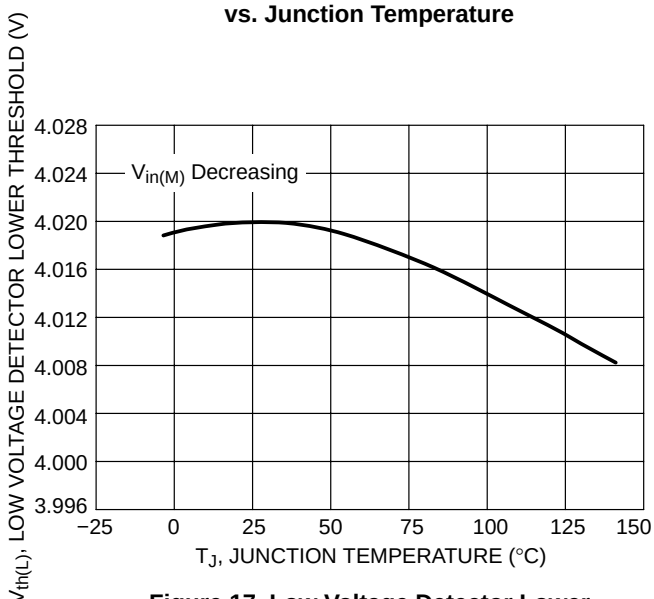


Figure 17. Low Voltage Detector Lower Threshold vs. Junction Temperature

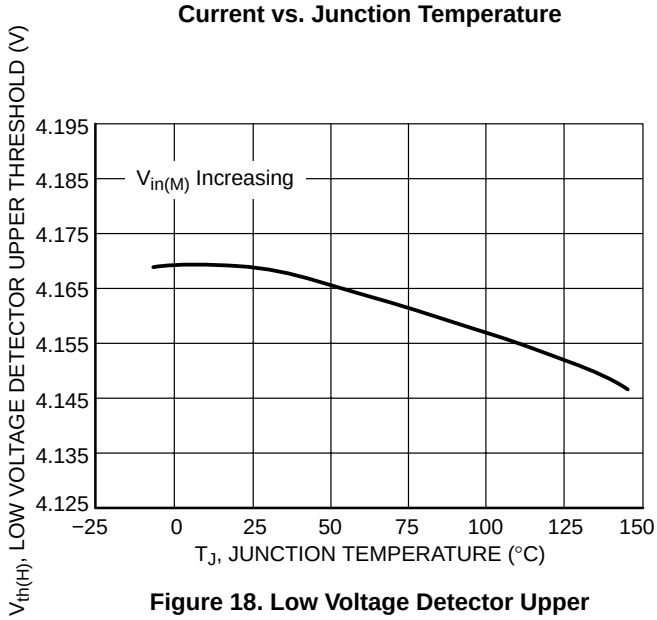


Figure 18. Low Voltage Detector Upper Threshold vs. Junction Temperature

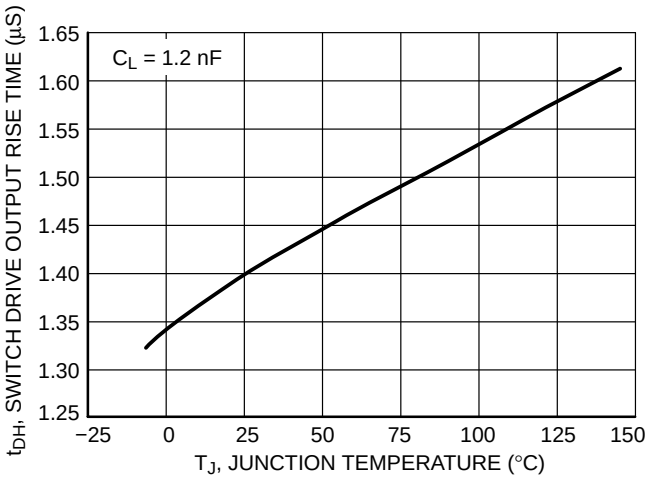


Figure 19. Switch Drive Output Rise Time vs. Junction Temperature

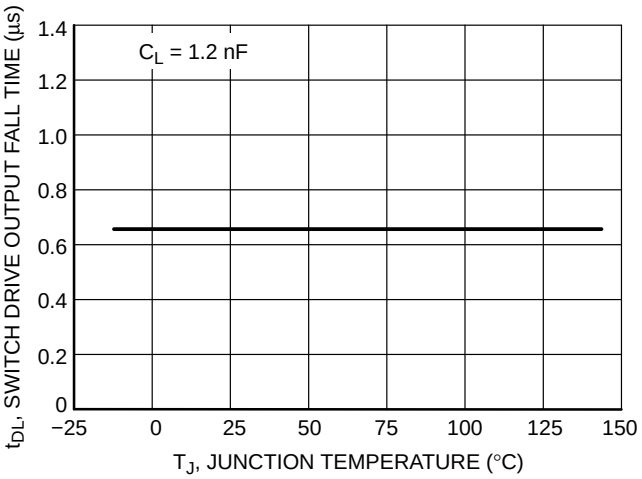
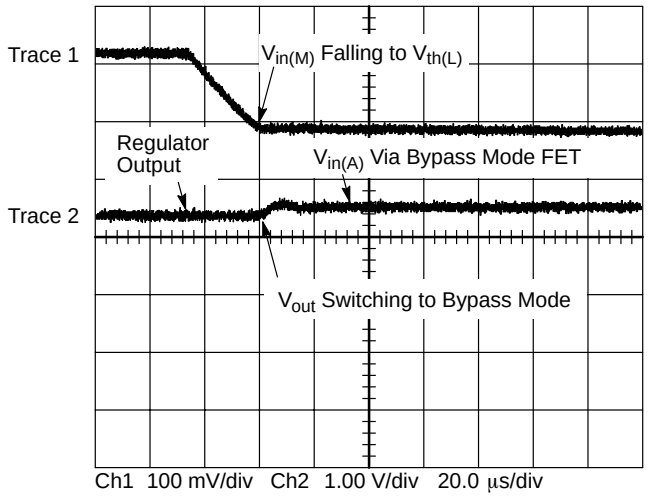


Figure 20. Switch Drive Output Fall Time vs. Junction Temperature



TRACE 1: $V_{in(M)}$ stepping from 5 V to $V_{th(L)}$
TRACE 2: V_{out} switching from regulator output to $V_{in(A)}$

Figure 21. Bypass Mode Transition

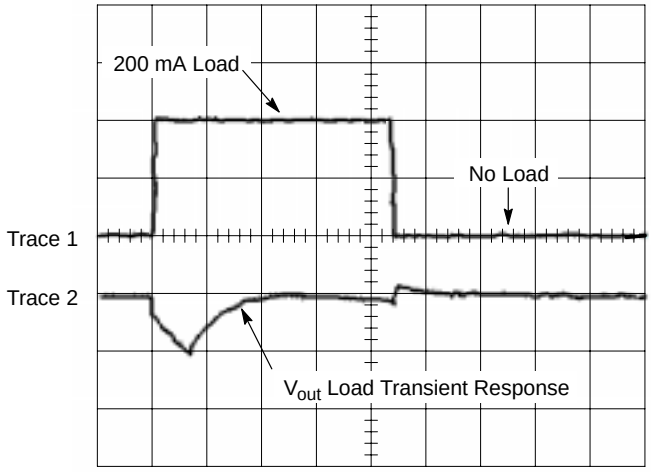


Figure 22. Load Transient Response

OPERATING DESCRIPTION

The MC33565 is designed for power managed computer applications such as peripheral card interface (PCI) and network interface cards (NIC) where glitch−free transitions between 3.3 V and 5.0 V supplies are necessary. In this type of application, the presence of a 5.0 V supply represents the “active” system mode, while the presence of 3.3 V represents the “sleep” system mode. The MC33565 complies with the *instantly available requirements* as specified by the Advanced Configuration and Power Interface (ACPI) standards set by Intel, Microsoft, and Toshiba. A regulated output voltage of 3.3 V is available even when the 5.0 V supply has been shut down and only the 3.3 V auxiliary supply is available.

The MC33565 has two supply inputs, the Main Input (typically 5.0 V) and an Auxiliary Input (typically 3.3 V). The MC33565 functions as a linear regulator while the Main Input is greater than its lower threshold voltage. Below this threshold, the internal regulator turns off and the 3.3 V output is supplied from the Auxiliary Input via the external P−channel MOSFET. The P−channel MOSFET gate is controlled by the Switch Drive Output.

Low Voltage Detector

Internal circuitry detects if the system is being powered from the Main or the Auxiliary Input supply. During normal operating conditions, the MC33565 is powered by the Main Input. A regulated output voltage of 3.3 V is provided by an internal low drop out 5.0 V to 3.3 V voltage regulator. While in this mode, the gate of the P−channel MOSFET is driven high, turning the MOSFET Switch OFF.

The internal Low Voltage Detector has typical upper and lower thresholds of 4.17 V and 4.02 V, respectively. The typical hysteresis voltage between the upper and lower thresholds is 150 mV, providing good noise immunity.

If the Main Input supply is not available or the supply voltage drops below the 4.02 V, the internal regulator turns OFF and the Switch Drive goes low. This enables the external MOSFET Switch, connecting the 3.3 V Auxiliary supply to the load allowing the load to remain powered even though the Main Input supply is not available. Once the Main Input supply voltage is above 4.17 V, the MOSFET Switch Drive goes high and the internal regulator is enabled.

The Low Voltage Detector logic is active throughout the entire range of the Main Input supply ramp up. The Switch Drive signal is never turned ON or OFF inappropriately during the Main Input ramp up. The output voltage is kept above 3.0 V while the load is biased from the Main Input supply.

Input Blocking

The internal regulator pass device (NPN transistor) ensures that no significant reverse current flows from V_{out} to the Main Supply or Gnd while the output is powered by the Auxiliary Supply. Reverse current is typically less than 6.0 μA over the entire operating temperature range.

P−Channel MOSFET Switch Polarity

The P−channel MOSFET drain should be connected to the Auxiliary Input, the source to the load and the gate to the Switch Drive Output. It is imperative that the polarity of the P−channel MOSFET is not reversed. If it is reversed, that is the drain connected to the load and the source connected to the Auxiliary supply, the body diode could be forward biased if the Auxiliary supply voltage is below V_{out}. Consequently, the linear regulator would not turn OFF and it would supply current to the Auxiliary supply rail.

External Compensation

Regulators are in nature feedback systems. As with any feedback system, loop stability needs to be evaluated to insure stability. The MC33565 requires an external compensation capacitor with a minimum value of 4.7 μF for stability. Increasing the capacitance will improve the overall load transient response. The equivalent series resistance (ESR) of the capacitor should be less than 0.5 Ω in order for the output voltage to be maintained within tight tolerance.

Sense

The Sense Input provides tight regulation of the output voltage while the Main supply is present even with varying load current. To take the most benefit of the Sense input, connect pin 6 as close as possible to the load. Use a separate trace to connect the source of the MOSFET Switch to the load as shown in Figure 23. This will help reduce interference or coupling in the Sense Input generated by the output current. The use of the Sense Input is required for correct device operation.

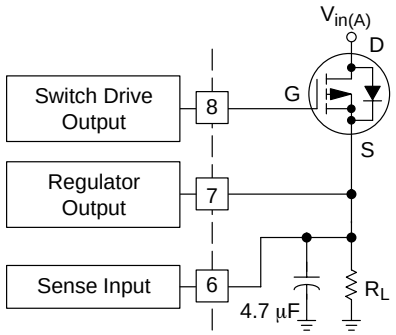


Figure 23. Voltage Regulation Using Sense Feature

Board Layout

It is recommended that the MC33565 is placed as close as possible to the MOSFET Switch and compensation capacitor. Use short traces to minimize extraneous signals from being induced in the Sense Input or Switch Drive Signals. Also, avoid routing the Sense Input close to the input and load current paths, as well as the Ground return path to prevent signal coupling.

The part list and board layout for a demonstration board using the MC33565 in an SOIC−8 package are available. The board operates with an input voltage between 4.3 V and

5.5 V and provides an output current up to 200 mA. The demonstration board layout (Silk Screen and Top Layers) are shown in Figures 26 and 27, respectively.

Current Limit and Thermal Shutdown

The MC33565 incorporates current limit and thermal shutdown to protect the device during fault conditions. If the device detects a current limit or short circuit condition, typically 730 mA, the device limits the drive to the internal regulator. Thermal shutdown protects the internal circuitry in the event that maximum junction temperature is exceeded. When activated, typically at 170°C, the output is disabled. There is no hysteresis built into the thermal limiting circuit. As a result, if the device is overheating, the output will appear to be oscillating. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended to be used as a substitute for proper heatsinking.**

Please consider that the thermal resistance values provided in the maximum ratings table will vary depending on pad size, adjacent components and air flow. If you are planning to operate the device close to its maximum junction temperature it is recommended that you measure the device temperature in your application to insure junction temperature is not exceeded.

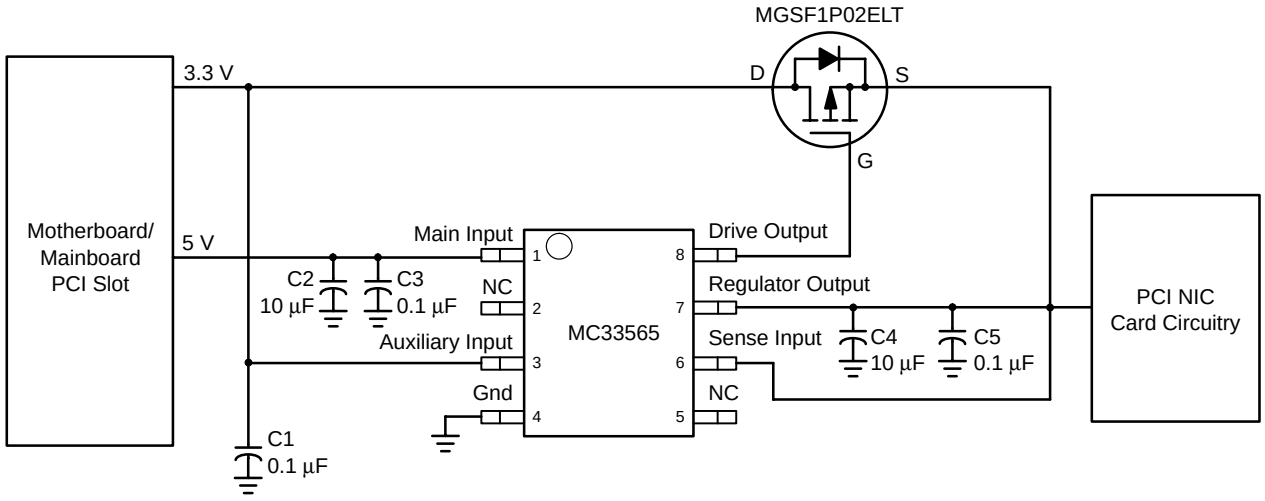


Figure 24. Application Board Schematic (See Figures 26 and 27)

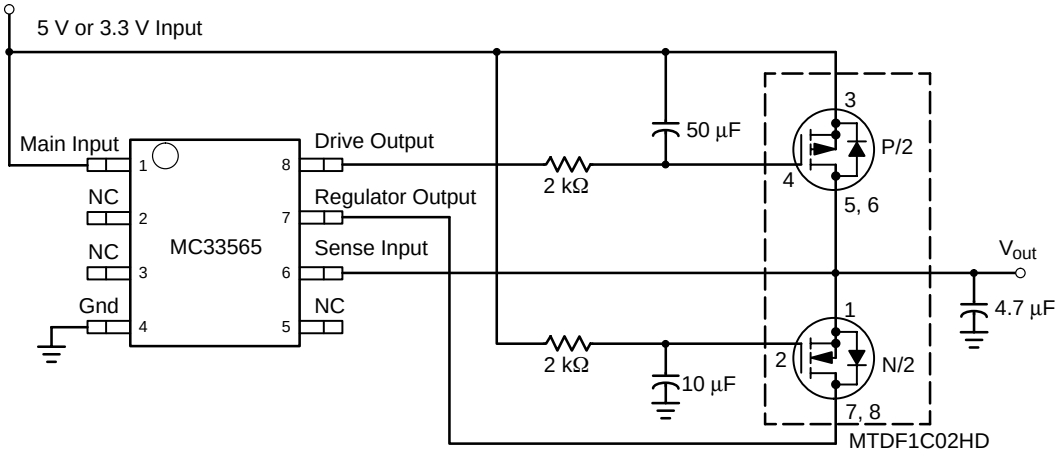


Figure 25. Alternative Application: 5.0 V or 3.3 V Card Input with Hot Swap Circuitry

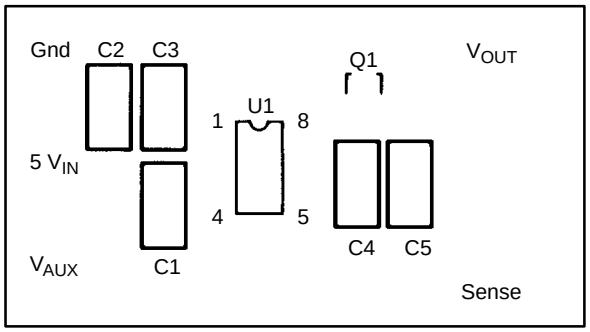


Figure 26. Demonstration Board Silk Screen Layer

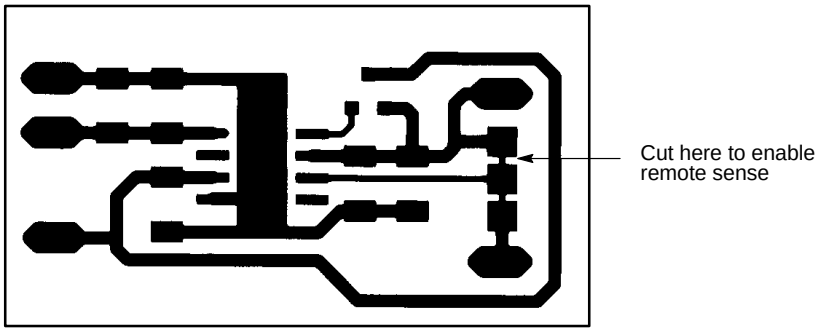


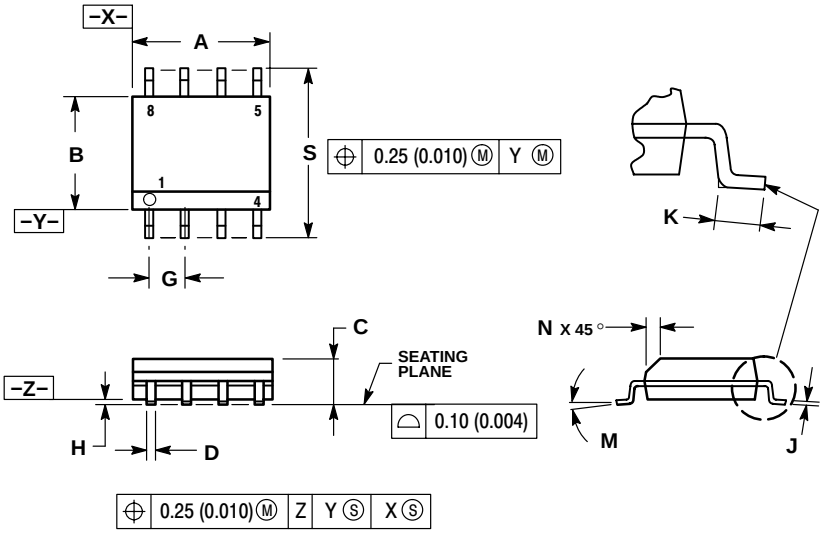
Figure 27. Demonstration Board Top Layer

PARTS LIST

Qty	Reference	Part/Description	Vendor	Notes
3	C1, C3, C5	0.1 μF Ceramic Capacitor	Various	−
2	C2, C4	10 μF Tantalum Capacitor	Various	−
1	U1	MC33565D	ON Semiconductor	(SOIC−8 Only)
1	Q1	MGSF1P02ELT	ON Semiconductor	P−Channel MOSFET

PACKAGE DIMENSIONS

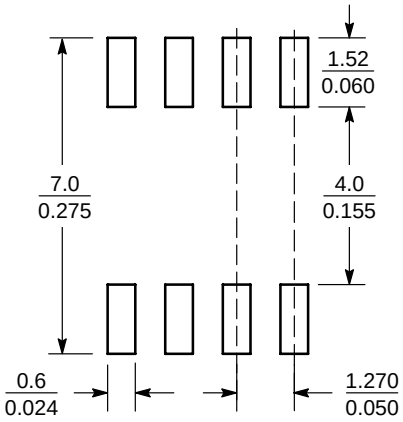
SOIC−8
D SUFFIX
CASE 751−07
ISSUE AE



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*

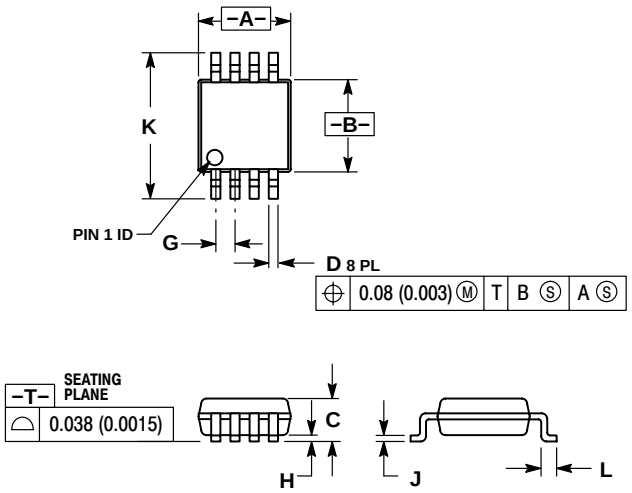


SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

Micro8
DM SUFFIX
CASE 846A−02
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. 846A−01 OBSOLETE, NEW STANDARD 846A−02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	---	1.10	---	0.043
D	0.25	0.40	0.010	0.016
G	0.65 BSC		0.026 BSC	
H	0.05	0.15	0.002	0.006
J	0.13	0.23	0.005	0.009
K	4.75	5.05	0.187	0.199
L	0.40	0.70	0.016	0.028

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