THE DATASHEET OF

AD8582AR

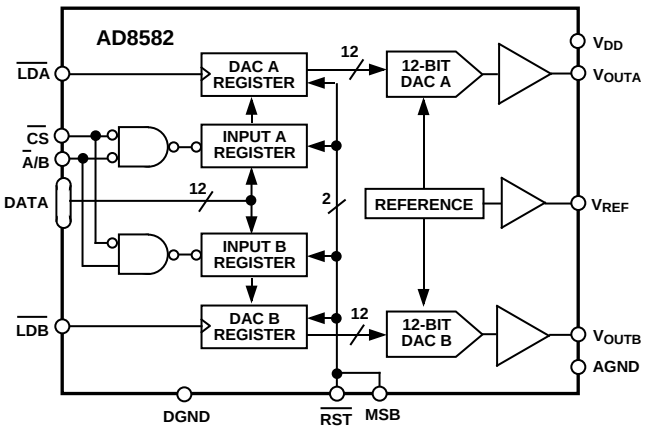
+5 Volt, Parallel Input Complete Dual 12-Bit DAC

AD8582

FEATURES
Complete Dual 12-Bit DAC
No External Components
Single +5 Volt Operation
1 mV/Bit with 4.095 V Full Scale
True Voltage Output, ±5 mA Drive
Very Low Power: 5 mW

APPLICATIONS
Digitally Controlled Calibration
Portable Equipment
Servo Controls
Process Control Equipment
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8582 is a complete, parallel input, dual 12-bit, voltage output DAC designed to operate from a single +5 volt supply. Built using a CBCMOS process, this monolithic DAC offers the user low cost, and ease-of-use in +5 volt only systems.

Included on the chip, in addition to the DACs, are a rail-to-rail amplifier, latch and reference. The reference (V_{REF}) is trimmed to 2.5 volts output, and the on-chip amplifier gains up the DAC output to 4.095 volts full scale. The user needs only supply a +5 volt supply.

The AD8582 is coded natural binary. The op amp output swings from 0 volt to +4.095 volts for a one-millivolt-per-bit resolution, and is capable of driving ±5 mA. Operation down to 4.3 V is possible with output load currents less than 1 mA.

The high speed parallel data interface connects to the fastest processors without wait states. The double-buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both LDA + LDB inputs will update both DAC outputs simultaneously. LDA and LDB can also be activated independently to immediately update their respective DAC registers. An address input decodes DAC A or DAC B when the chip select $\overline{CS}$ input is strobed. An asynchronous reset input sets the output to zero scale. The MSB bit can be used to establish a preset to midscale when the reset input is strobed.

The AD8582 is available in the 24-pin plastic DIP and the surface mount SOIC-24. Each part is fully specified for operation over –40°C to +85°C, and the full +5 V ± 5% power supply range.

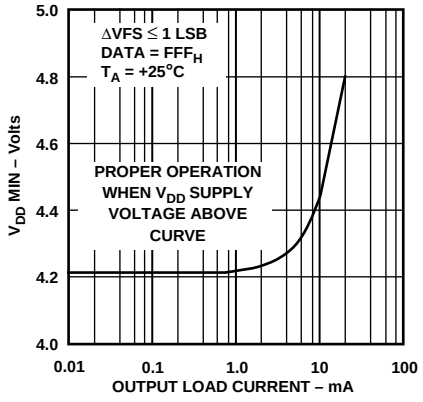


Figure 1. Minimum Supply Voltage vs. Load

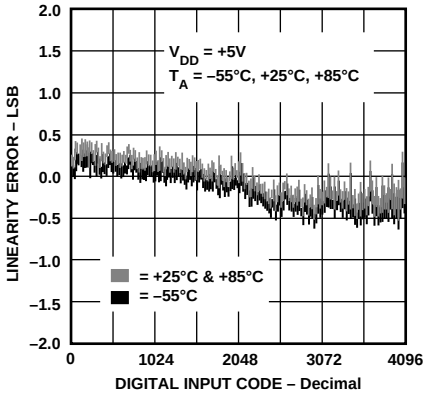


Figure 2. Linearity Error vs. Digital Code and Temperature

REV. 0

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AD8582–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_{DD} = +5.0 V ± 5%, R_L = No Load, –40°C ≤ T_A ≤ +85°C, unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Units
STATIC PERFORMANCE						
Resolution	N	Note 1	12			Bits
Relative Accuracy	INL		–2	±3/4	+2	LSB
Differential Nonlinearity	DNL	Monotonic	–1	±3/4	+1	LSB
Zero-Scale Error	V_{ZSE}	Data = 000_H		+0.2	+3	mV
Full-Scale Voltage	V_{FS}	Data = FFF_H,[2]	4.079	4.095	4.111	V
Full-Scale Tempco	TCV_{FS}	Notes 2 and 3		±16		ppm/°C
MATCHING PERFORMANCE						
Linearity Matching Error	$\Delta V_{FS}A/B$			±1		LSB
REFERENCE OUTPUT						
Output Voltage	V_{REF}		2.484	2.500	2.516	V
Output Source Current	I_{REF}	Note 4			–5	mA
Line Rejection	LN_{REJ}				0.08	%/V
Load Regulation	LD_{REG}	I_{REF} = 0 mA to 5 mA			0.1	%/mA
ANALOG OUTPUT						
Output Current	I_{OUT}	Data = 800_H			±5	mA
Load Regulation at Half Scale	LD_{REG}	R_L = 402 Ω to ∞, Data = 800_H		1	3	LSB
Capacitive Load	C_L	No Oscillation[3]		500		pF
DYNAMIC CHARACTERISTICS[3]						
Crosstalk	C_T			>64		dB
Voltage Output Settling Time[5]	t_S	To ±1 LSB of Final Value		16		µs
Digital Feedthrough	F_T	Signal Measured at DAC Output, While Changing Data ($\overline{LDA}$ = $\overline{LDB}$ = "1")		35		nV s
LOGIC INPUTS						
Logic Input Low Voltage	V_{IL}				0.8	V
Logic Input High Voltage	V_{IH}		2.4			V
Input Leakage Current	I_{IL}				10	µA
Input Capacitance	C_{IL}	Note 3			10	pF
TIMING SPECIFICATIONS[3, 6]						
Chip Select Pulse Width	t_{CSW}		30			ns
DAC Select Setup	t_{AS}		30			ns
DAC Select Hold	t_{AH}		0			ns
Data Setup	t_{DS}		30			ns
Data Hold	t_{DH}		10			ns
Load Setup	t_{LS}		20			ns
Load Hold	t_{LH}		10			ns
Load Pulse Width	t_{LDW}		20			ns
Reset Pulse Width	t_{RSW}		30			ns
SUPPLY CHARACTERISTICS						
Positive Supply Current	I_{DD}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		4	7	mA
		V_{IL} = 0 V, V_{DD} = +5 V		1	2	mA
Power Dissipation[7]	P_{DISS}	V_{IH} = 2.4 V, V_{IL} = 0.8 V		20	35	mW
		V_{IL} = 0 V, V_{DD} = +5 V		5	10	mW
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%		0.002	0.004	%/%

NOTES

[1]1 LSB = 1 mV for 0 V to +4.095 V output range.

[2]Includes internal voltage reference error.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Very little sink current is available at the V_{REF} pin. Use external buffer if setting up a virtual ground.

[5]Settling time is not guaranteed for the first six codes 0 through 5.

[6]All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of +5 V) and timed from a voltage level of 1.6 V.

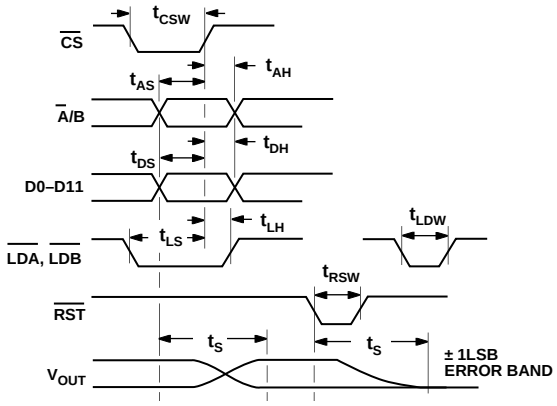
[7]Power dissipation is a calculated value $I_{DD} \times 5$ V.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to DGND & AGND . . . . . –0.3 V, +7 V
Logic Inputs to DGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND . . . . . –0.3 V, V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V, V_{DD}
I_{OUT} Short Circuit to GND . . . . . 50 mA
Package Power Dissipation . . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance, θ_{JA}
24-Pin Plastic DIP Package (N-24) . . . . . 62°C/W
24-Lead SOIC Package (SOL-24) . . . . . 73°C/W
Maximum Junction Temperature (T_J max) . . . . . 150°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



Timing Diagram

ORDERING INFORMATION*

Model	Temperature Range	Package Description	Package Option
AD8582AN	–40°C to +85°C	24-Pin Plastic DIP	N-24
AD8582AR	–40°C to +85°C	24-Lead SOIC	SOL-24
AD8582Chips	+25°C	Die	

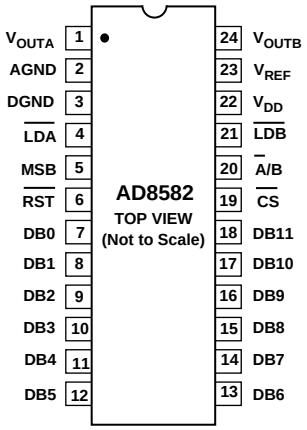
*For die specifications contact your local Analog Devices sales office. The AD8582 contains 1270 transistors.

PIN DESCRIPTION

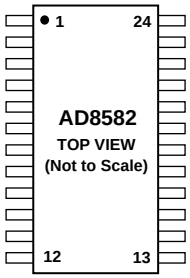
Pin No.	Name	Description
1, 24	V_{OUTA} V_{OUTB}	Voltage outputs from the DACs. Fixed output voltage range of 0 V to 4.095 V with 1 mV/LSB. An internal temperature stabilized reference maintains a fixed full-scale voltage independent of time, temperature and power supply variations.
2	AGND	Analog Ground. Ground reference for the internal bandgap reference voltage, the DAC, and the output buffer.
3	DGND	Digital ground for input logic.
4, 21	$\overline{LDA}$, $\overline{LDB}$	Load DAC register strobes. Transfers input register data to the DAC registers. Active low inputs, Level sensitive latch. May be connected together to double-buffer load DAC registers.
5	MSB	Digital Input: High presets DAC registers to half scale (800_H), Low clears DAC registers to zero (000_H) upon $\overline{RST}$ assertion.
6	$\overline{RST}$	Active low digital input that clears the DAC register to zero, setting the DAC to minimum scale when MSB pin = 0, or half-scale when MSB pin = 1.
7–18	$DB_{0–11}$	Twelve Binary Data Bit Inputs. DB11 is the MSB and DB0 is the LSB.
19	$\overline{CS}$	Chip Select. Active low input.
20	$\overline{A}$/B	Select DAC A = 0 or DAC B = 1.
22	V_{DD}	Positive Supply. Nominal value +5 V, ±5%.
23	V_{REF}	Nominal 2.5 V reference output voltage. This node must be buffered if required to drive external loads.

PIN CONFIGURATIONS

N-24
24-Pin Plastic DIP



SOL-24
24-Pin SOIC



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8582 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Table I. Control Logic Truth Table

$\overline{CS}$	$\overline{A}$/B	$\overline{LDA}$	$\overline{LDB}$	$\overline{RST}$	MSB	Input Register	DAC Register
L	L	H	H	H	X	Write to A	Latched
L	H	H	H	H	X	Write to B	Latched
L	L	L	H	H	X	Write to A	A Transparent
L	H	H	L	H	X	Write to B	B Transparent
H	X	L	L	H	X	Latched	A & B Transparent
H	X	^	^	H	X	Latched	Latched
X	X	X	X	L	L	Reset to Zero Scale	Reset to Zero Scale
X	X	X	X	L	H	Reset to Midscale	Reset to Midscale
H	X	X	X	^	X	Latch Reset Value	Latch Reset Value

^Denotes positive edge triggered.

OPERATION

The AD8582 is a complete, ready-to-use dual 12-bit digital-to-analog converter. Only one +5 V power supply is necessary for operation. It contains two voltage-switched, 12-bit, laser-trimmed digital-to-analog converters, a curvature-corrected bandgap reference, rail-to-rail output op amps, input registers, and DAC registers. The parallel data interface consists of twelve data bits, DB0–DB11, an address select pin $\overline{A}$/B, two load strobe pins ($\overline{LDA}$, $\overline{LDB}$) and an active low $\overline{CS}$ strobe. In addition an asynchronous $\overline{RST}$ pin will set all DAC register bits to zero causing the V_{OUT} to become zero volts, or to midscale for trimming applications when the MSB pin is programmed to Logic 1. This function is useful for power on reset or system failure recovery to a known state.

D/A CONVERTER SECTION

The internal DAC is a 12-bit voltage-mode device with an output that swings from AGND potential to the 2.5 volt internal bandgap voltage. It uses a laser trimmed R-2R ladder which is switched by N channel MOSFETs. The output voltage of the DAC has a constant resistance independent of digital input code. The DAC output (not available to the user) is internally connected to the rail-to-rail output op amp.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. This low power amplifier contains a differential PNP pair input stage which provides low offset voltage and low noise, as well as the ability to amplify the zero-scale DAC output voltages. The rail-to-rail amplifier is configured in a gain of 1.6384 (= 4.095 V/2.5 V) in order to set the 4.095 volt full-scale output (1 mV/LSB). See Figure 3 for an equivalent circuit schematic of the analog section.

The op amp has a 16 µs typical settling time to 0.01%. There are slight differences in settling time for negative slewing signals versus positive. See the oscilloscope photos in the Typical Performances section of this data sheet.

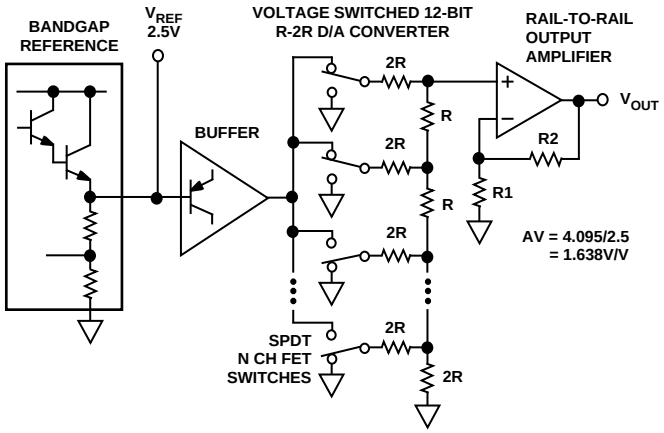


Figure 3. Equivalent Schematic of Analog Portion

OUTPUT SECTION

The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 4 shows an equivalent output schematic of the rail-to-rail amplifier with its N channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P channel pull-up device that can supply GND terminated loads, especially important at the –5% supply tolerance value of 4.75 volts.

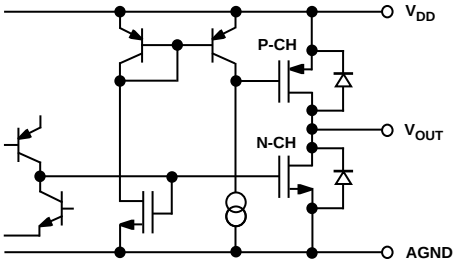


Figure 4. Equivalent Analog Output Circuit

Figures 5 and 6 in the typical performance characteristics section provide information on output swing performance near ground and full-scale as a function of load. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 500 pF capacitive load driving capability.

REFERENCE SECTION

The internal 2.5 V curvature-corrected bandgap voltage reference is laser trimmed for both initial accuracy and low temperature coefficient. The voltage generated by the reference is available at the V_{REF} pin. Since V_{REF} is not intended to drive external loads, it must be buffered. The equivalent emitter follower output circuit of the V_{REF} pin is shown in Figure 3.

Bypassing the V_{REF} pin will improve noise performance; however, bypassing is not required for proper operation. Figure 8 shows broadband noise performance.

POWER SUPPLY

The very low power consumption of the AD8582 is a direct result of a circuit design optimizing use of the CBCMOS process. By using the low power characteristics of the CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors good analog accuracy is achieved.

For power-consumption sensitive applications it is important to note that the internal power consumption of the AD8582 is strongly dependent on the actual logic-input voltage levels present on the DB0–DB11, $\overline{CS}$, $\overline{A}$/B, MSB, $\overline{LDA}$, $\overline{LDB}$ and $\overline{RST}$ pins. Since these inputs are standard CMOS logic structures they contribute static power dissipation dependent on the actual driving logic V_{OH} and V_{OL} voltage levels. The graph in Figure 9 shows the effect on total AD8582 supply current as a function of the actual value of input logic voltage. Consequently, for optimum dissipation use of CMOS logic versus TTL provides minimal dissipation in the static state. A V_{INL} = 0 V on the DB0–11 pins provides the lowest standby dissipation of 1 mA typical with a +5 V power supply.

As with any analog system, it is recommended that the AD8582 power supply be bypassed on the same PC card that contains the chip. Figure 10 shows the power supply rejection versus frequency performance. This should be taken into account when using higher frequency switched-mode power supplies with ripple frequencies of 100 kHz and higher.

One advantage of the rail-to-rail output amplifiers used in the AD8582 is the wide range of usable supply voltage. The part is fully specified and tested over temperature for operation from +4.75 V to +5.25 V. If reduced linearity and source current capability near full scale can be tolerated, operation of the AD8582 is possible down to +4.3 volts. The minimum operating supply voltage versus load current plot, in Figure 1, provides information for operation below V_{DD} = +4.75 V.

TIMING AND CONTROL

The input registers are level triggered and acquire data from the data bus during the time period when $\overline{CS}$ is low. The input register selected is determined by the $\overline{A}$/B select pin, see Table I. for a complete description. When $\overline{CS}$ goes high, the data is latched into the register and held until $\overline{CS}$ returns low. The minimum time required for the data to be present on the bus before $\overline{CS}$ returns high is called the data setup time (t_{DS}) as seen in Timing Diagram. The data hold time (t_{DH}) is the amount of time that the data has to remain on the bus after $\overline{CS}$ goes high. The high speed timing offered by the AD8582 provides for direct interface with no wait states in all but the fastest microprocessors.

The data from the input registers is transferred to the DAC registers by the active low $\overline{LDA}$ and $\overline{LDB}$ pins. If these inputs are tied together, a single logic input can perform a double buffer update of the DAC registers, which in turn simultaneously changes the analog output voltages to a new value. If the $\overline{LDA}$ and $\overline{LDB}$ pins are wired low, they become transparent. In this mode the input register data will directly control the output voltages. Refer to the Control Logic Truth Table for a complete description.

Unipolar Output Operation

This is the basic mode of operation for the AD8582. The AD8582 has been designed to drive loads as low as 820Ω in parallel with 500 pF. The code table for this operation is shown in Table II.

Table II. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
FFF	4095	+ 4.095
801	2049	+ 2.049
800	2048	+ 2.048
7FF	2047	+ 2.047
000	0	0

AD8582–Typical Performance Characteristics

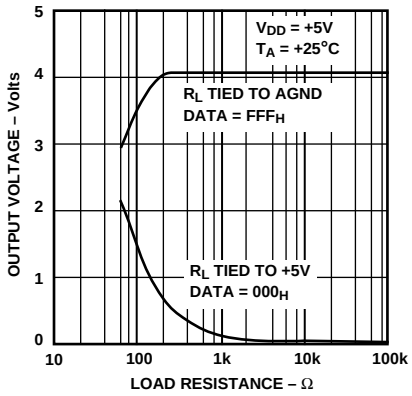


Figure 5. Output Swing vs. Load

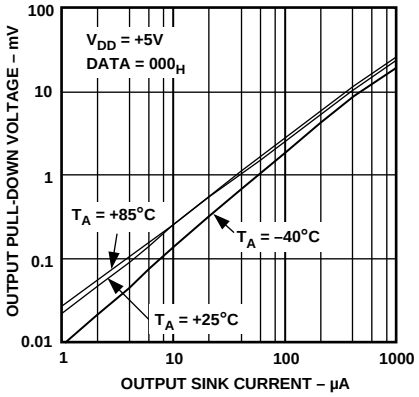


Figure 6. Pull-Down Voltage vs. Output Sink Current Capability

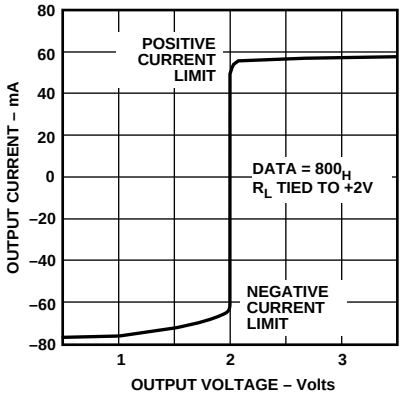


Figure 7. I_{OUT} vs. V_{OUT}

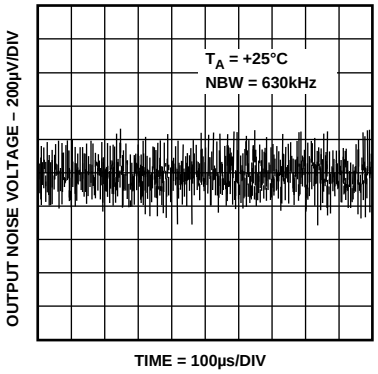


Figure 8. Broadband Noise

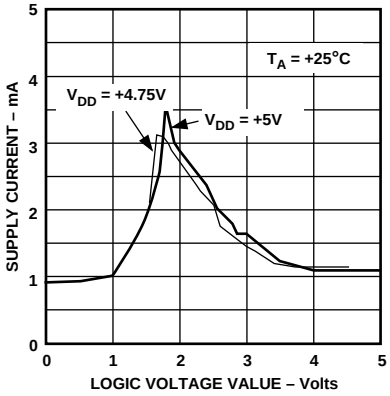


Figure 9. Supply Current vs. Logic Input Voltage

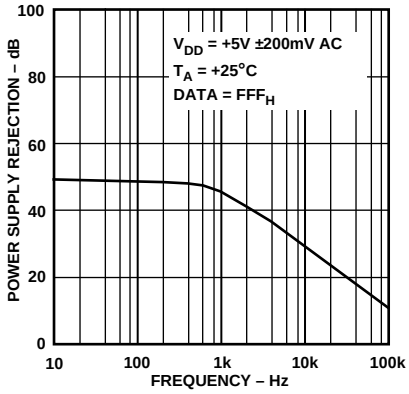


Figure 10. Power Supply Rejection vs. Frequency

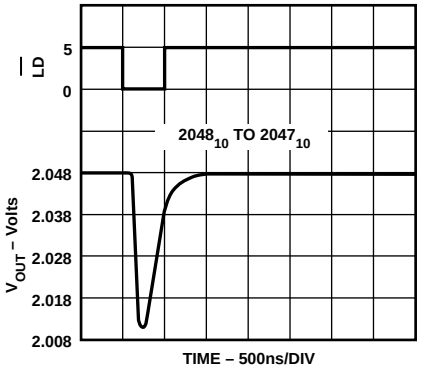


Figure 11. Midscale Transition Performance

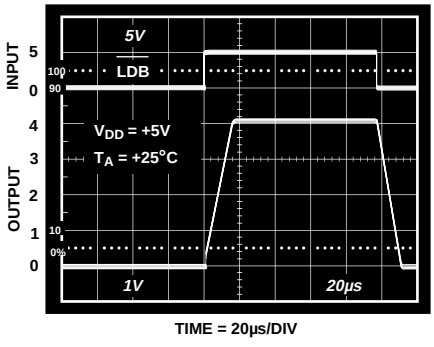


Figure 12. Large Signal Settling Time

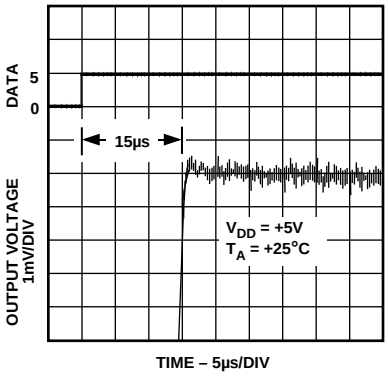


Figure 13. Output Voltage Rise Time Detail

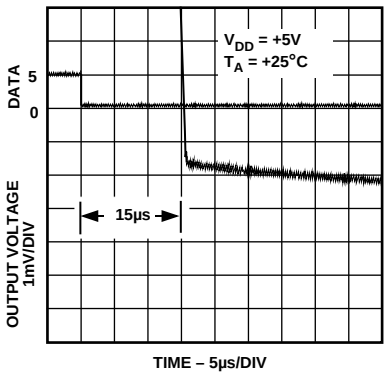


Figure 14. Output Voltage Fall Time Detail

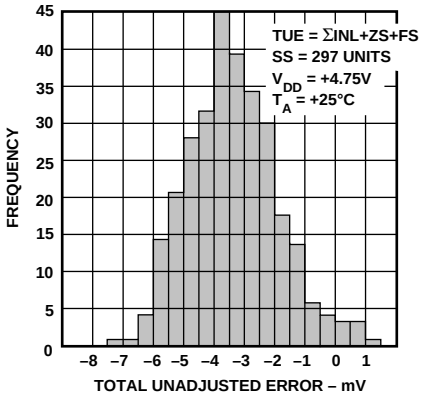


Figure 15. Total Unadjusted Error Histogram

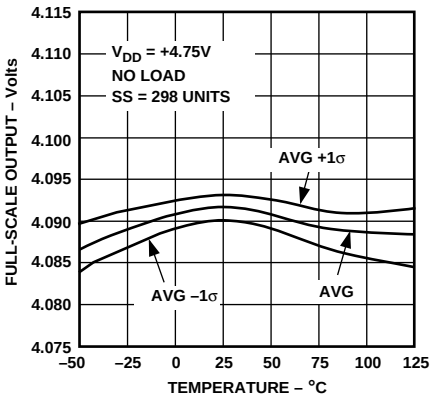


Figure 16. Full-Scale Voltage vs. Temperature

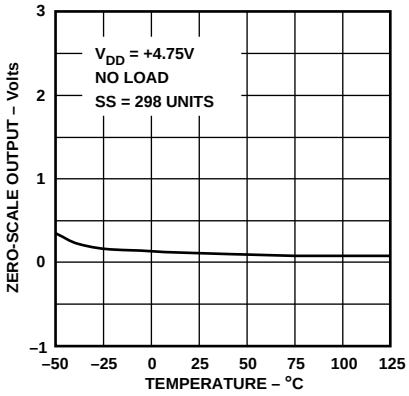


Figure 17. Zero-Scale Voltage vs. Temperature

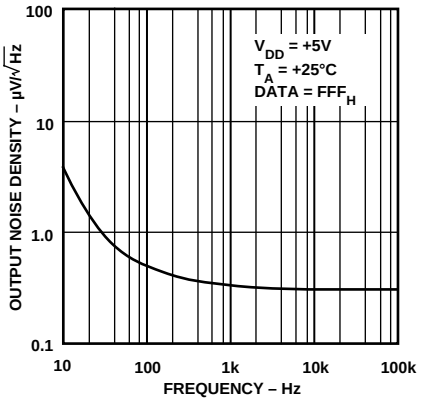


Figure 18. Output Voltage Noise Density vs. Frequency

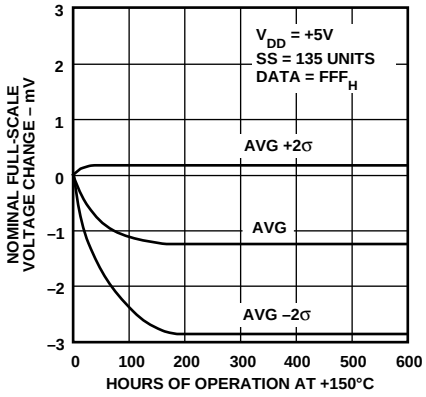


Figure 19. Long-Term Drift Accelerated by Burn-In

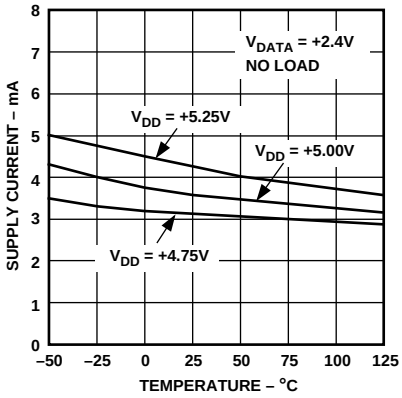


Figure 20. Supply Current vs. Temperature

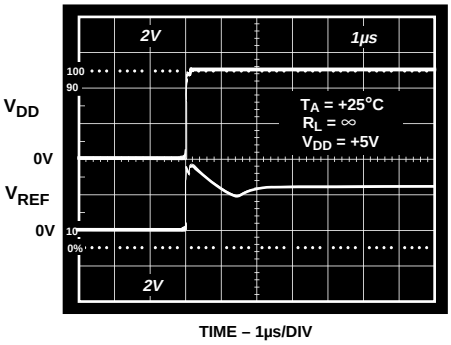


Figure 21. Reference Startup vs. Time

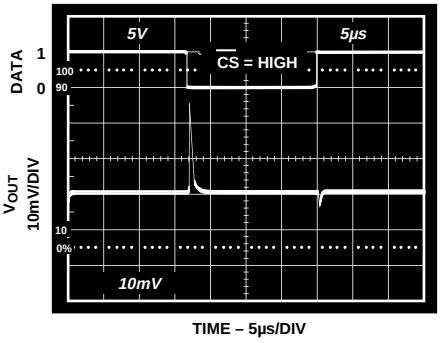


Figure 22. Digital Feedthrough vs. Time

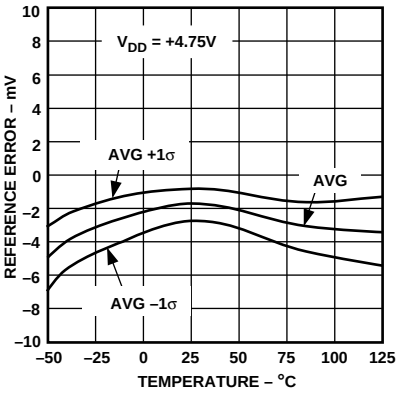


Figure 23. Reference Error vs. Temperature

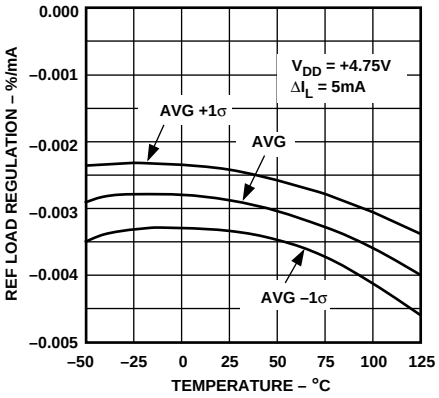


Figure 24. Reference Load Regulation vs. Temperature

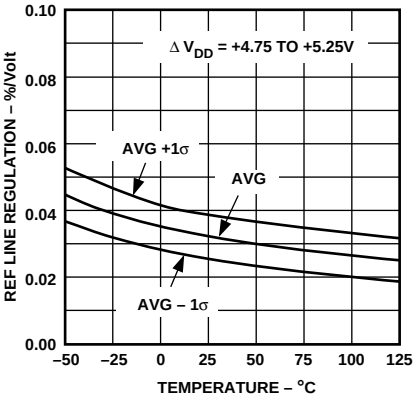


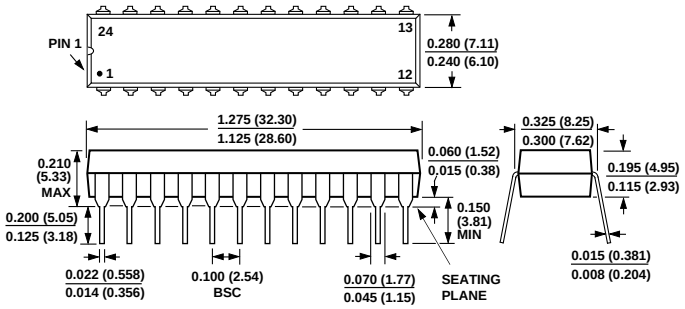
Figure 25. Reference Line Regulation vs. Temperature

C1869–18–12/93

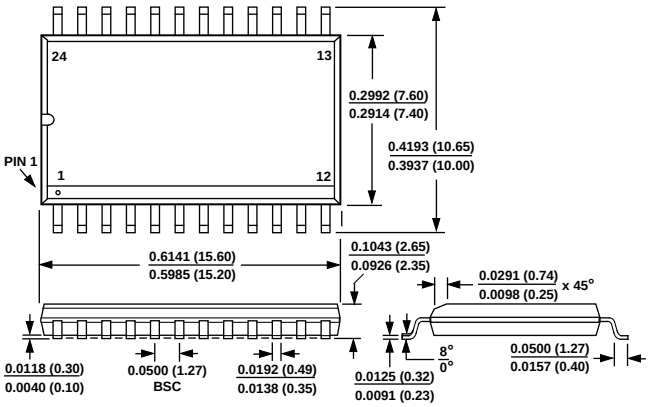
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

N-24
24-Pin Narrow Body Plastic DIP



SOL-24
24-Lead Wide Body SOIC



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