



THE DATASHEET OF PMN40ENEX





PMN40ENE

30 V, N-channel Trench MOSFET

24 May 2016

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Logic-level compatible
- Very fast switching
- Enhanced power dissipation capability of 1240 mW
- ElectroStatic Discharge (ESD) protection > 1 kV HBM

3. Applications

- LED driver
- Power management
- Low-side loadswitch
- Switching circuits

4. Quick reference data

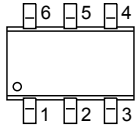
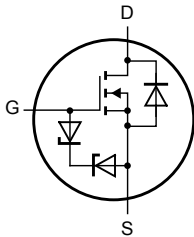
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	5.7	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 4.5\text{ A}; T_j = 25\text{ °C}$	-	30	38	m Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>TSOP6 (SOT457)</p>	 <p>017aaa255</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN40ENE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PMN40ENE	H4

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	30	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C; t ≤ 5 s	[1]	-	5.7	A
		V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	4.5	A
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	2.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	18	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	530	mW
			[1]	-	1.24	W
		T _{sp} = 25 °C		-	4.46	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	1.2	A

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

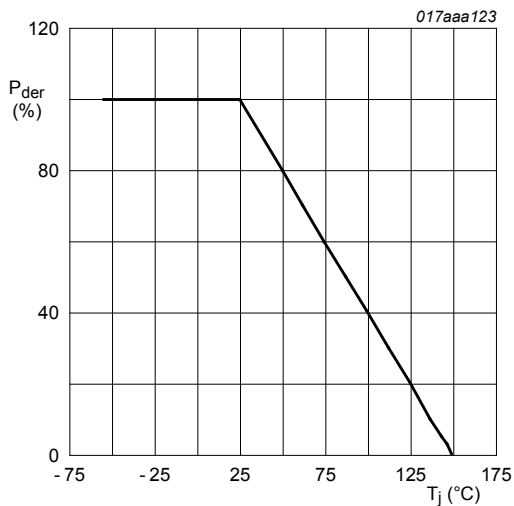


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100 \%$$

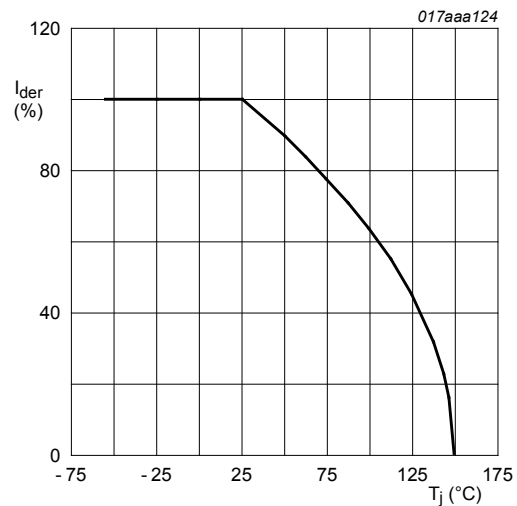
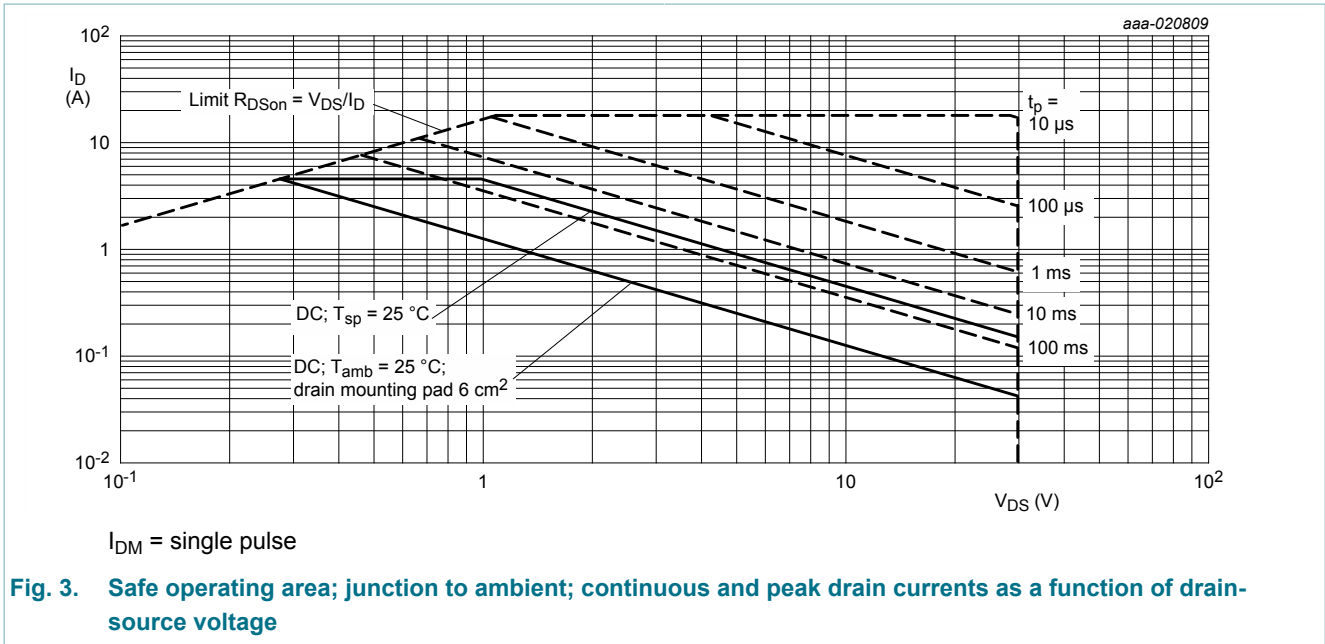


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100 \%$$

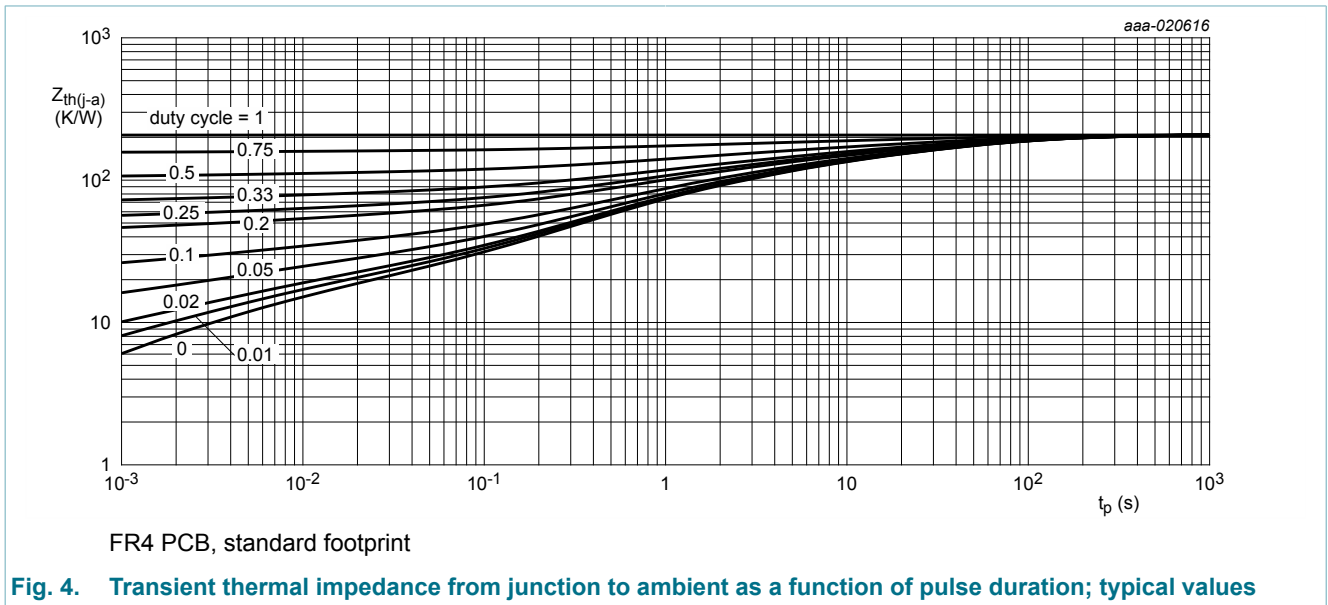


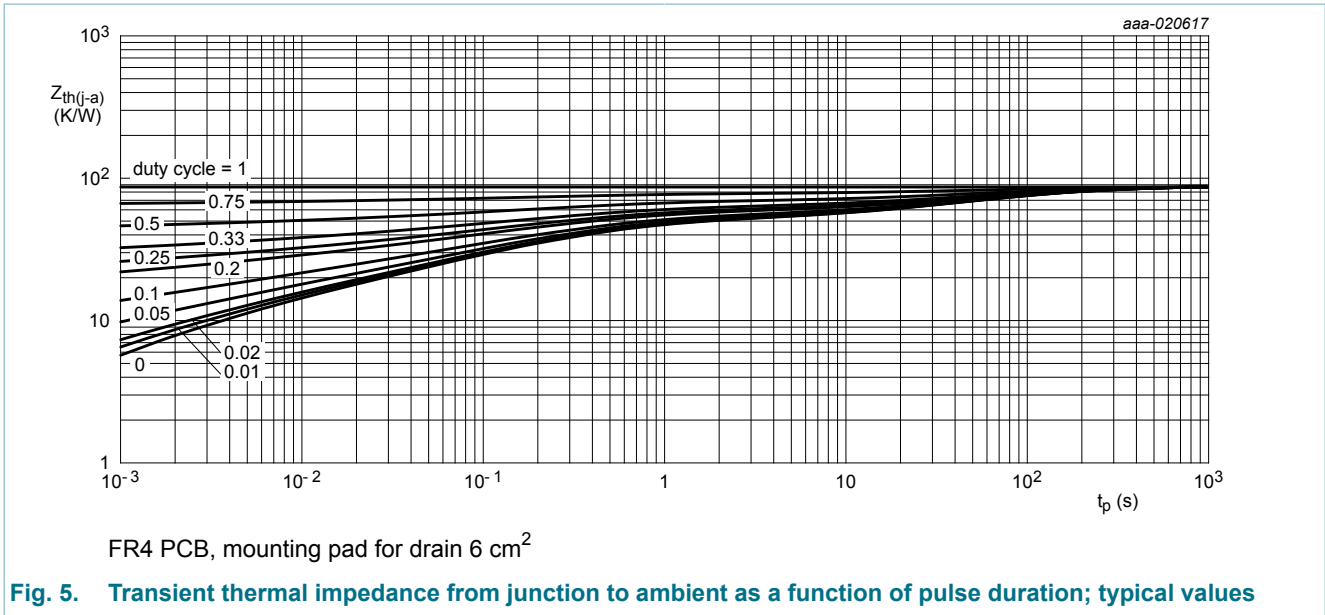
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	205	235	K/W
			[2]	-	88	101	K/W
		in free air; t ≤ 5 s	[2]	-	55	63	K/W
R _{th(j-sp)}	thermal resistance from junction to solder point			-	24	28	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².





10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	30	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	1	1.4	2	V
I_{DSS}	drain leakage current	$V_{DS} = 30 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 16 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -16 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	200	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 4.5 A$; $T_j = 25 \text{ }^\circ C$	-	30	38	m Ω
		$V_{GS} = 10 V$; $I_D = 4.5 A$; $T_j = 150 \text{ }^\circ C$	-	47	60	m Ω
		$V_{GS} = 4.5 V$; $I_D = 3.3 A$; $T_j = 25 \text{ }^\circ C$	-	44	70	m Ω
g_{fs}	forward transconductance	$V_{DS} = 10 V$; $I_D = 2 A$; $T_j = 25 \text{ }^\circ C$	-	10.7	-	S
R_G	gate resistance	$T_j = 25 \text{ }^\circ C$; $f = 1 \text{ MHz}$	-	0.5	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 V$; $I_D = 3.2 A$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$	-	5.6	11	nC
Q_{GS}	gate-source charge		-	0.76	-	nC
Q_{GD}	gate-drain charge		-	1.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 15 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	294	-	pF
C_{oss}	output capacitance		-	42	-	pF
C_{riss}	reverse transfer capacitance		-	33	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 V$; $I_D = 3.2 A$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$	-	4.6	-	ns
t_r	rise time		-	14.7	-	ns
$t_{d(off)}$	turn-off delay time		-	9.1	-	ns
t_f	fall time		-	3	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 1.2 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.8	1.2	V

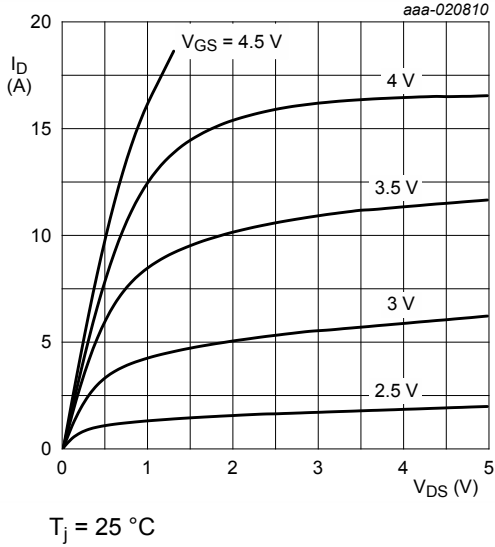


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

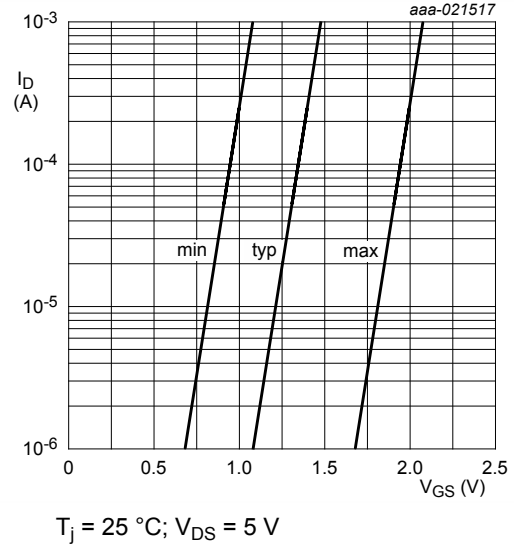


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

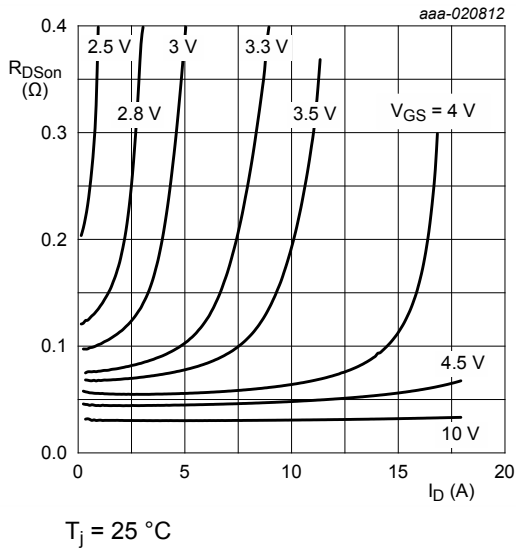


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

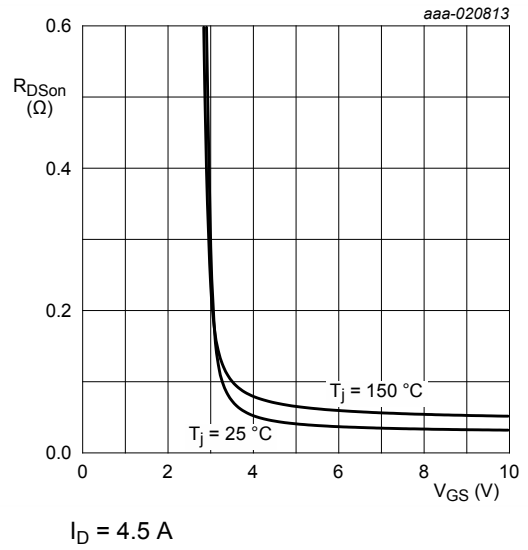
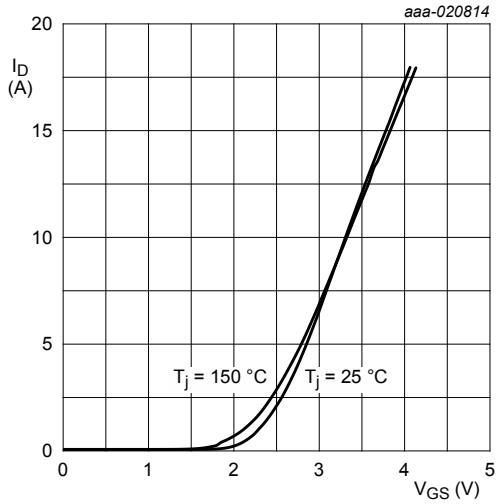


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

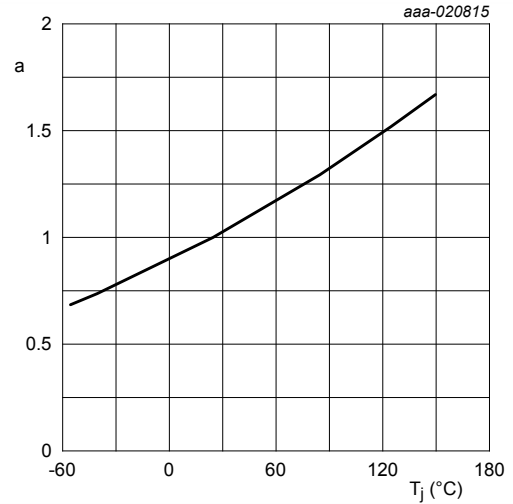
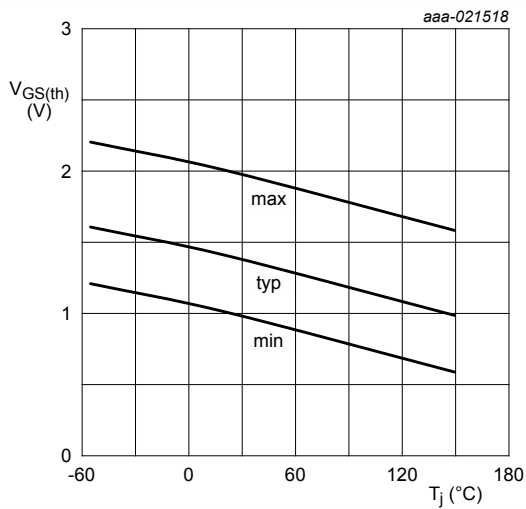


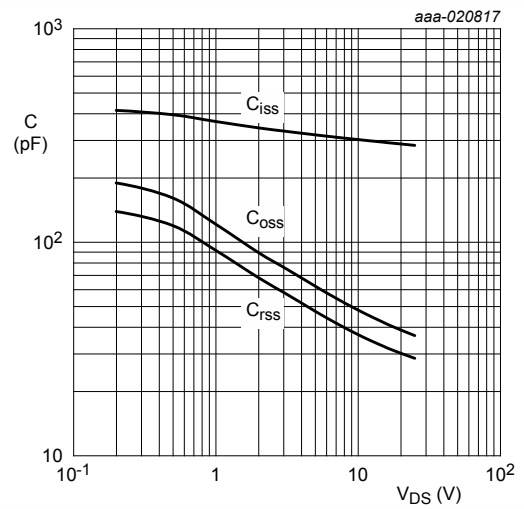
Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



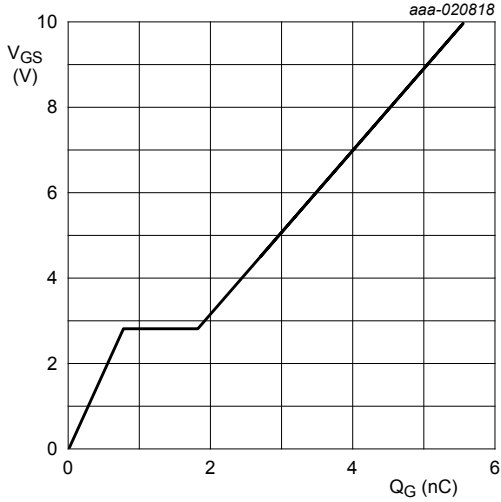
$$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 4.5$ A; $V_{DS} = 15$ V; $T_{amb} = 25$ °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

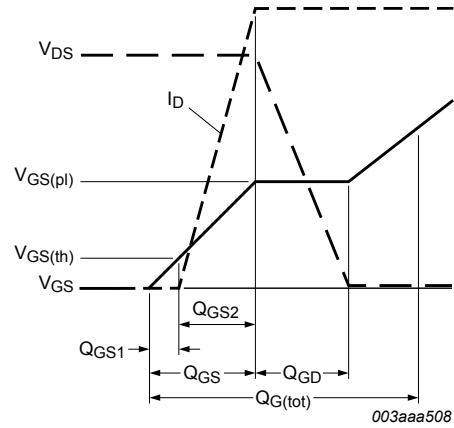
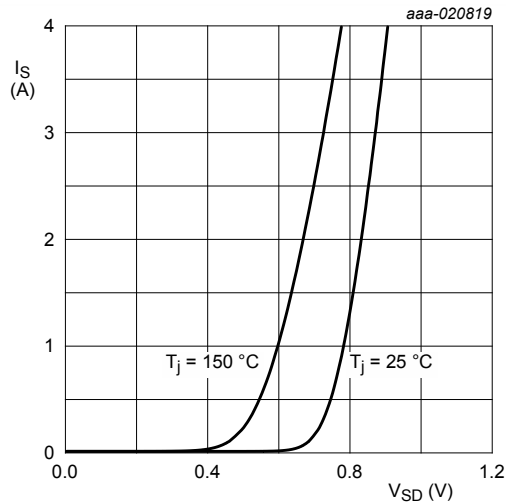


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

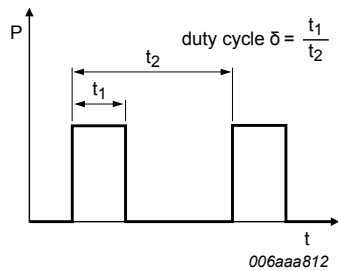


Fig. 17. Duty cycle definition

12. Package outline

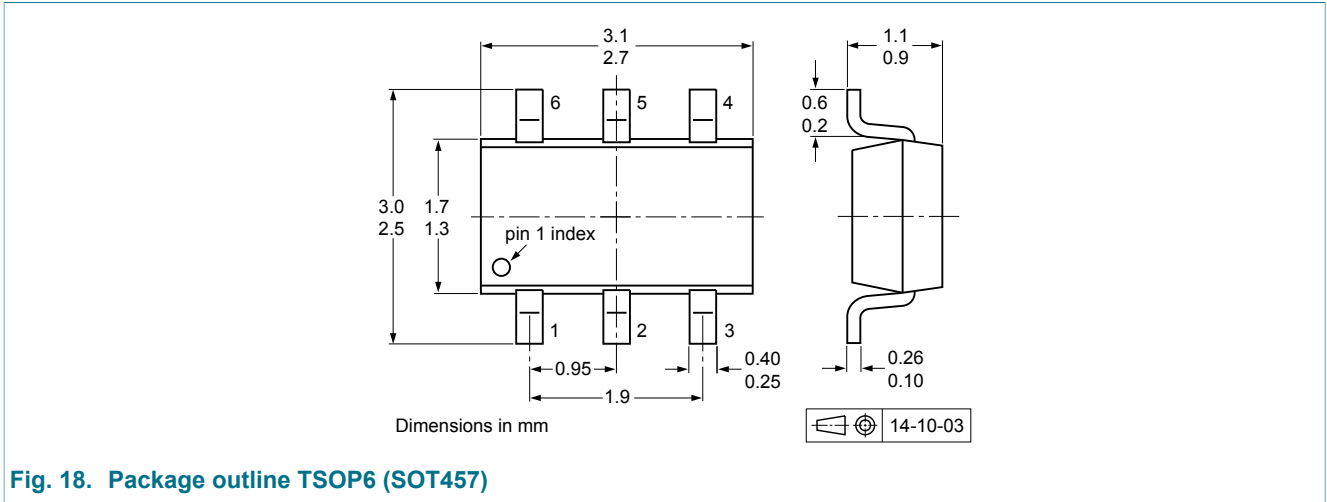


Fig. 18. Package outline TSOP6 (SOT457)

13. Soldering

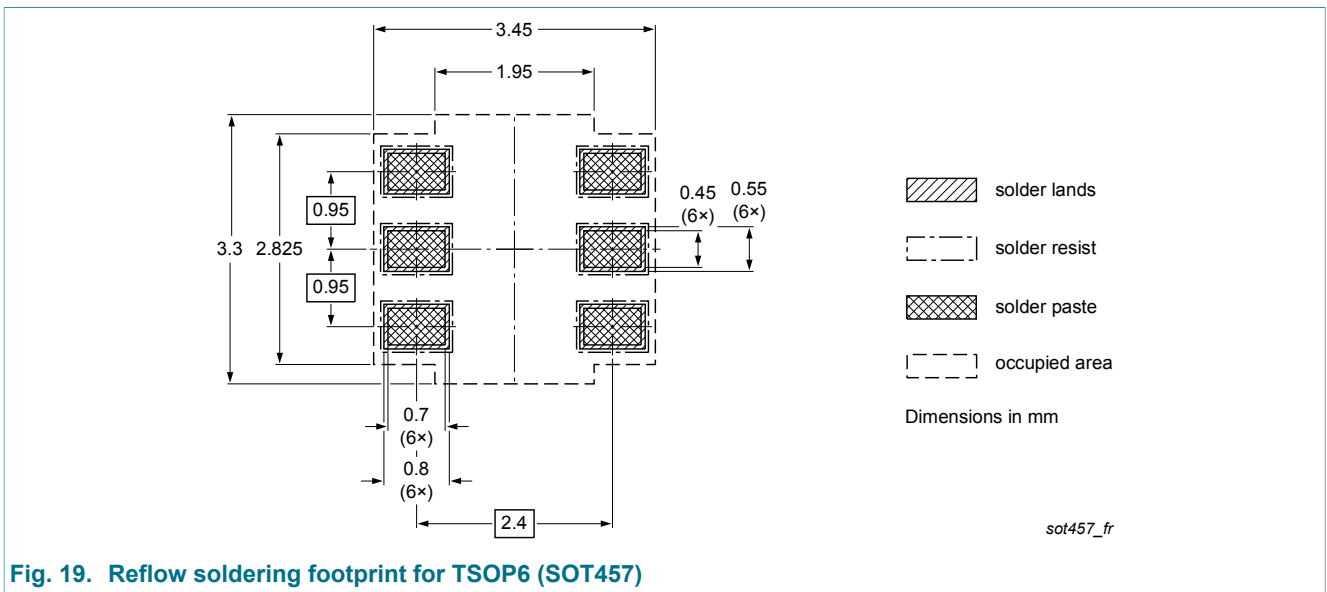


Fig. 19. Reflow soldering footprint for TSOP6 (SOT457)

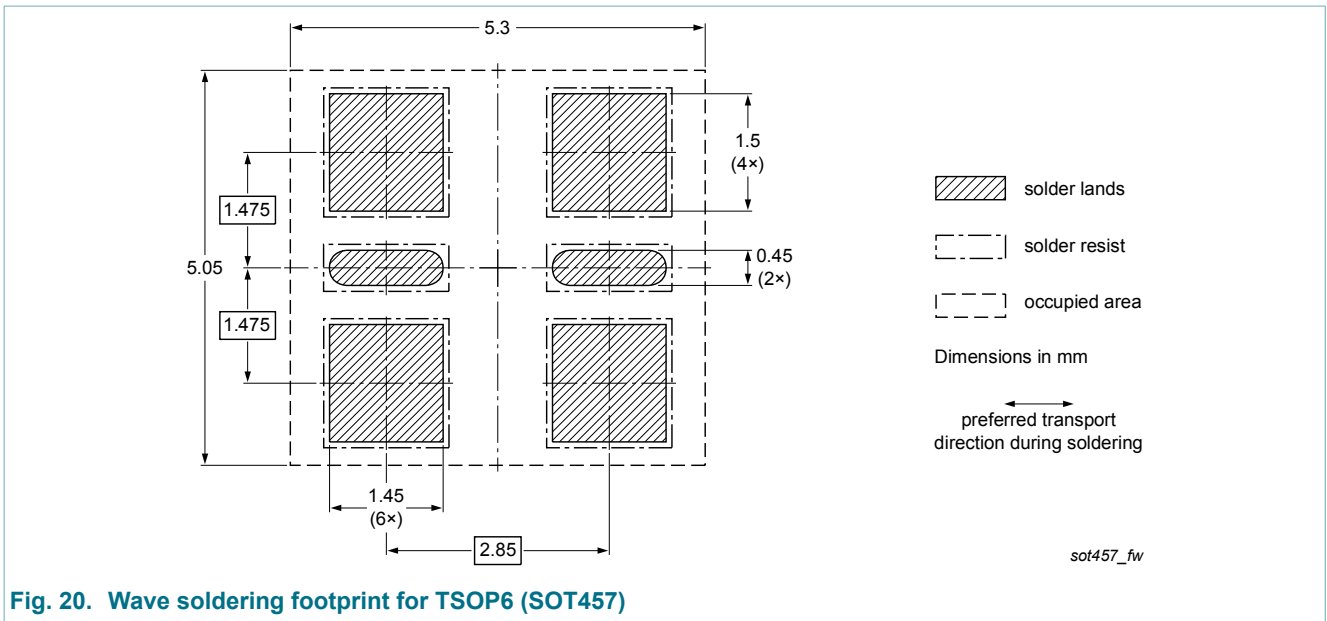


Fig. 20. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN40ENE v.1	20160526	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
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Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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