



**THE DATASHEET OF  
PDTA113EE,115**



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Kind regards,

Team Nexperia

# PDTA113E series

PNP resistor-equipped transistors; R1 = 1 k $\Omega$ , R2 = 1 k $\Omega$

Rev. 05 — 2 September 2009

Product data sheet

## 1. Product profile

### 1.1 General description

PNP Resistor-Equipped Transistors (RET).

Table 1. Product overview

Type number	Package			NPN complement
	NXP	JEITA	JEDEC	
PDTA113EE	SOT416	SC-75	-	PDTC113EE
PDTA113EK	SOT346	SC-59A	TO-236	PDTC113EK
PDTA113EM	SOT883	SC-101	-	PDTC113EM
PDTA113ES <sup>[1]</sup>	SOT54 (TO-92)	SC-43A	TO-92	PDTC113ES
PDTA113ET	SOT23	-	TO-236AB	PDTC113ET
PDTA113EU	SOT323	SC-70	-	PDTC113EU

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#))

### 1.2 Features

- Built-in bias resistors
- Reduces component count
- Simplifies circuit design
- Reduces pick and place costs

### 1.3 Applications

- General purpose switching and amplification
- Circuit drivers
- Inverter and interface circuits

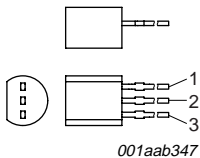
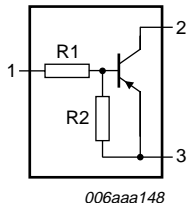
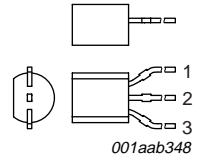
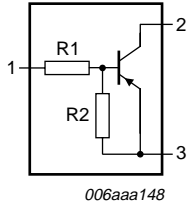
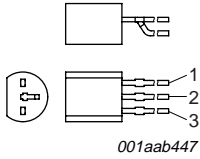
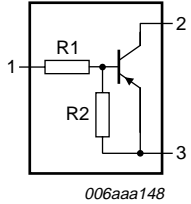
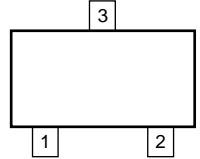
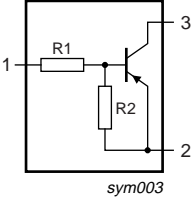
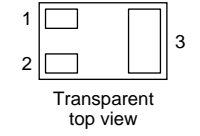
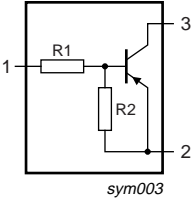
### 1.4 Quick reference data

Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CE0}$	collector-emitter voltage	open base	-	-	-50	V
$I_O$	output current (DC)		-	-	-100	mA
R1	bias resistor 1 (input)		0.7	1	1.3	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	

**2. Pinning information**

**Table 3. Pinning**

Pin	Description	Simplified outline	Symbol
<b>SOT54</b>			
1	input (base)	 <p>001aab347</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54A</b>			
1	input (base)	 <p>001aab348</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT54 variant</b>			
1	input (base)	 <p>001aab447</p>	 <p>006aaa148</p>
2	output (collector)		
3	GND (emitter)		
<b>SOT23, SOT323, SOT346, SOT416</b>			
1	input (base)	 <p>006aaa144</p>	 <p>sym003</p>
2	GND (emitter)		
3	output (collector)		
<b>SOT883</b>			
1	input (base)	 <p>Transparent top view</p>	 <p>sym003</p>
2	GND (emitter)		
3	output (collector)		

### 3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PDTA113EE	SC-75	plastic surface mounted package; 3 leads	SOT416
PDTA113EK	SC-59A	plastic surface mounted package; 3 leads	SOT346
PDTA113EM	SC-101	leadless ultra small plastic package; 3 solder lands; body 1.0 × 0.6 × 0.5 mm	SOT883
PDTA113ES <sup>[1]</sup>	SC-43A	plastic single-ended leaded (through hole) package; 3 leads	SOT54
PDTA113ET	-	plastic surface mounted package; 3 leads	SOT23
PDTA113EU	SC-70	plastic surface mounted package; 3 leads	SOT323

[1] Also available in SOT54A and SOT54 variant packages (see [Section 2](#) and [Section 9](#)).

### 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PDTA113EE	16
PDTA113EK	17
PDTA113EM	G4
PDTA113ES	TA113E
PDTA113ET	*15
PDTA113EU	*14

[1] \* = -: made in Hong Kong  
 \* = p: made in Hong Kong  
 \* = t: made in Malaysia  
 \* = W: made in China

## 5. Limiting values

**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CBO</sub>	collector-base voltage	open emitter	-	-50	V
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-50	V
V <sub>EBO</sub>	emitter-base voltage	open collector	-	-10	V
V <sub>I</sub>	input voltage				
	positive		-	+10	V
	negative		-	-10	V
I <sub>O</sub>	output current (DC)		-	-100	mA
I <sub>CM</sub>	peak collector current		-	-100	mA
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> ≤ 25 °C			
	SOT416		[1] -	150	mW
	SOT346		[1] -	250	mW
	SOT883		[2][3] -	250	mW
	SOT54		[1] -	500	mW
	SOT23		[1] -	250	mW
	SOT323		[1] -	200	mW
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>j</sub>	junction temperature		-	150	°C
T <sub>amb</sub>	ambient temperature		-65	+150	°C

[1] Refer to standard mounting conditions

[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60  $\mu$ m copper strip line.

## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air				
	SOT416		[1] -	-	833	K/W
	SOT346		[1] -	-	500	K/W
	SOT883		[2][3] -	-	500	K/W
	SOT54		[1] -	-	250	K/W
	SOT23		[1] -	-	500	K/W
	SOT323		[1] -	-	625	K/W

[1] Refer to standard mounting conditions.

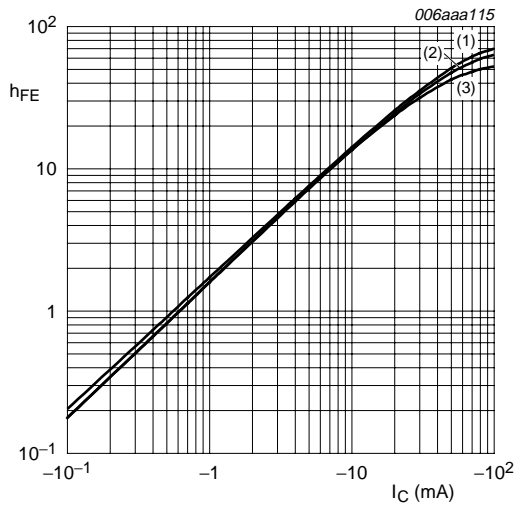
[2] Reflow soldering is the only recommended soldering method.

[3] Refer to SOT883 standard mounting conditions; FR4 printed-circuit board with 60  $\mu$ m copper strip line.

## 7. Characteristics

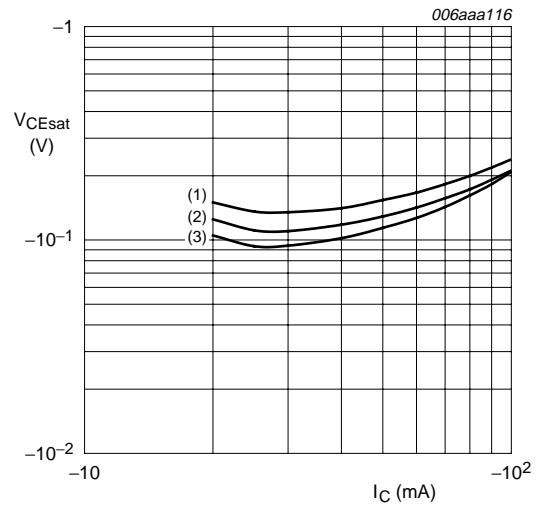
**Table 8. Characteristics**
*T<sub>amb</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I <sub>CBO</sub>	collector-base cut-off current	V <sub>CB</sub> = -50 V; I <sub>E</sub> = 0 A	-	-	-100	nA
I <sub>CEO</sub>	collector-emitter cut-off current	V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A	-	-	-1	$\mu$ A
		V <sub>CE</sub> = -30 V; I <sub>B</sub> = 0 A; T <sub>j</sub> = 150 °C	-	-	-50	$\mu$ A
I <sub>EBO</sub>	emitter-base cut-off current	V <sub>EB</sub> = -5 V; I <sub>C</sub> = 0 A	-	-	-4	mA
h <sub>FE</sub>	DC current gain	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -40 mA	30	-	-	
V <sub>CEsat</sub>	collector-emitter saturation voltage	I <sub>C</sub> = -30 mA; I <sub>B</sub> = -1.5 mA	-	-	-150	mV
V <sub>I(off)</sub>	off-state input voltage	V <sub>CE</sub> = -5 V; I <sub>C</sub> = -100 $\mu$ A	-	-1.3	-0.5	V
V <sub>I(on)</sub>	on-state input voltage	V <sub>CE</sub> = -300 mV; I <sub>C</sub> = -20 mA	-2	-1.7	-	V
R1	bias resistor 1 (input)		0.7	1	1.3	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	
C <sub>c</sub>	collector capacitance	V <sub>CB</sub> = -10 V; I <sub>E</sub> = i <sub>e</sub> = 0 A; f = 1 MHz	-	-	2	pF



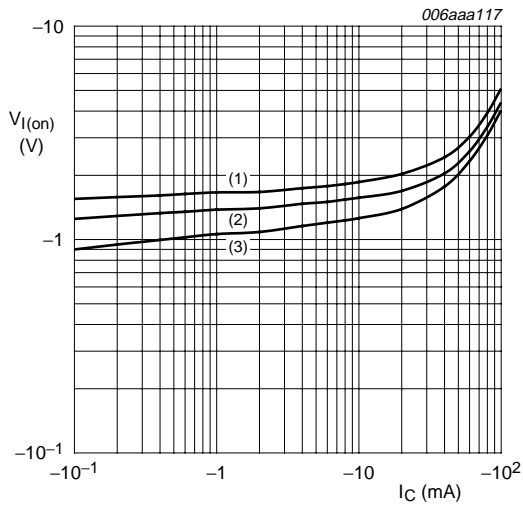
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 1. DC current gain as a function of collector current; typical values**



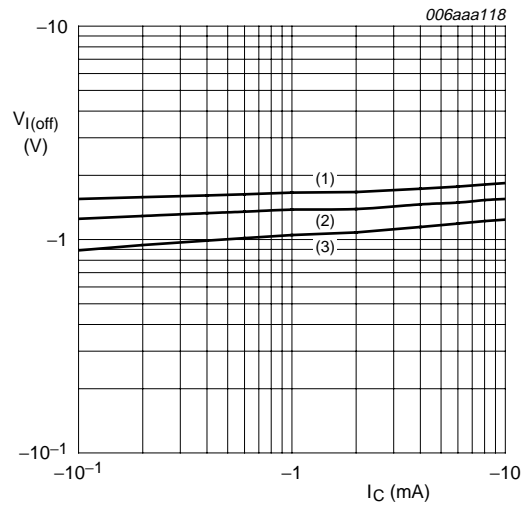
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 2. Collector-emitter saturation voltage as a function of collector current; typical values**



$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 3. On-state input voltage as a function of collector current; typical values**



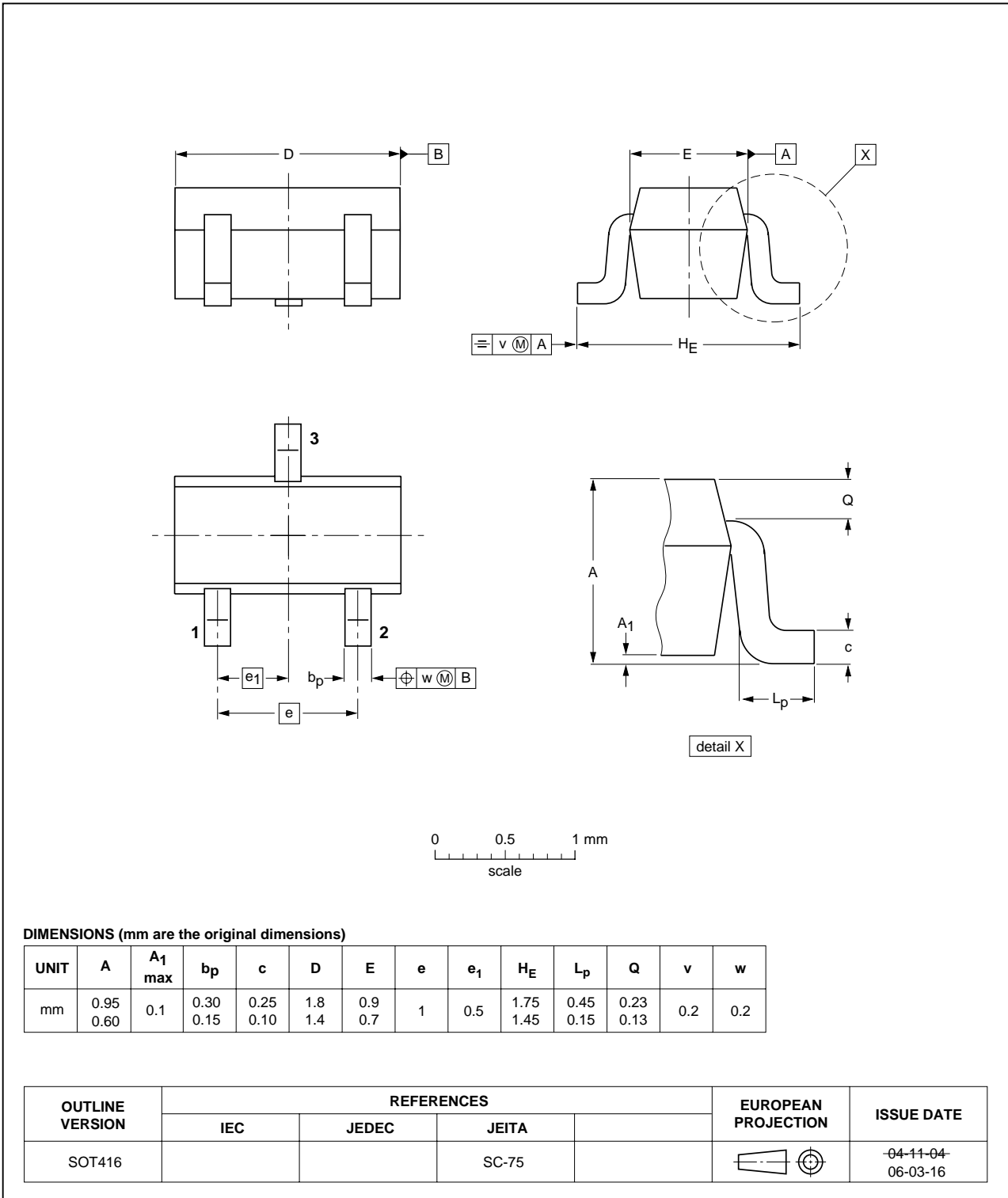
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 4. Off-state input voltage as a function of collector current; typical values**

**8. Package outline**

Plastic surface-mounted package; 3 leads

SOT416



**Fig 5. Package outline SOT416 (SC-75)**

Plastic surface-mounted package; 3 leads

SOT346

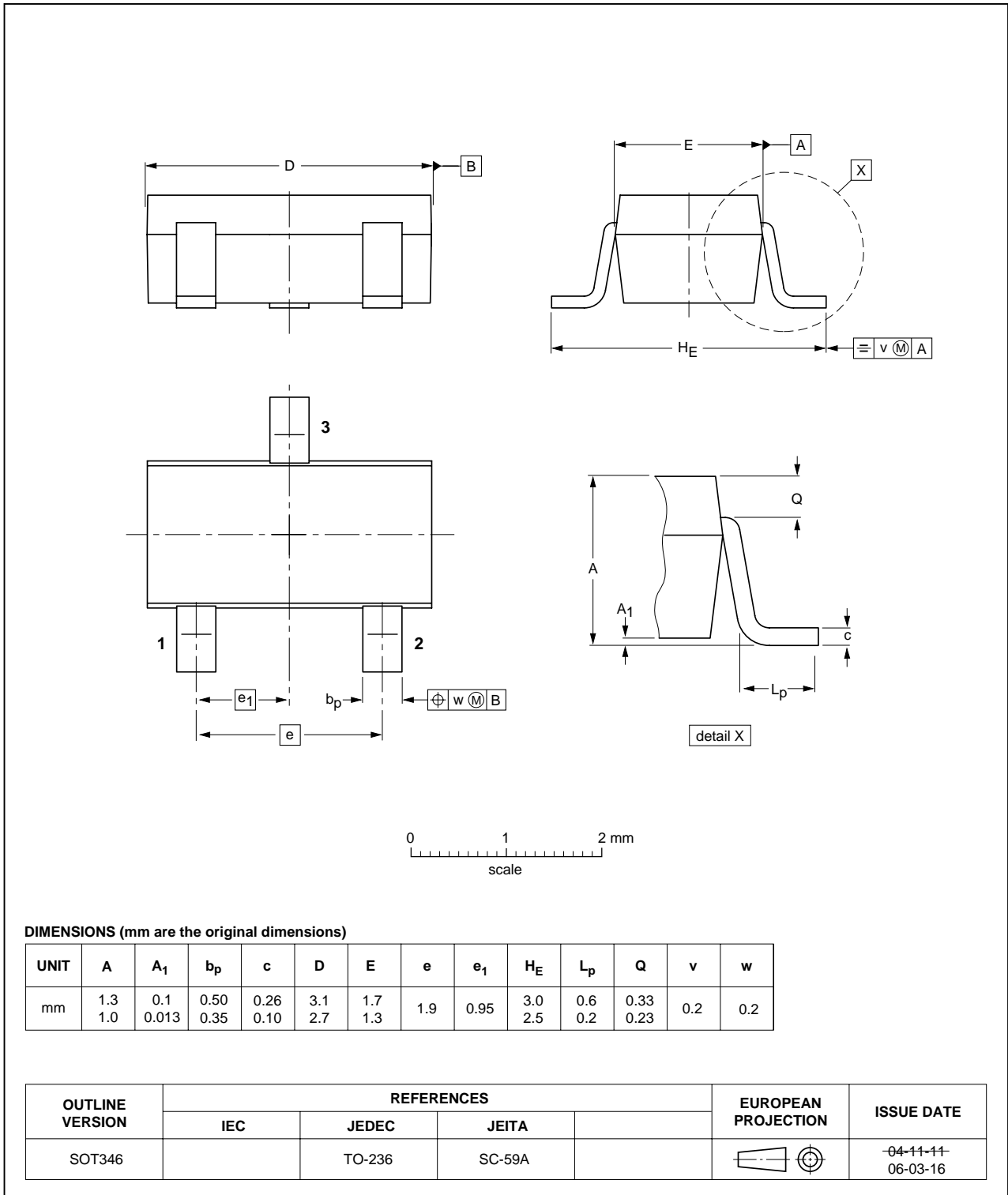


Fig 6. Package outline SOT346 (SC-59A/TO-236)

Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.5 mm

SOT883

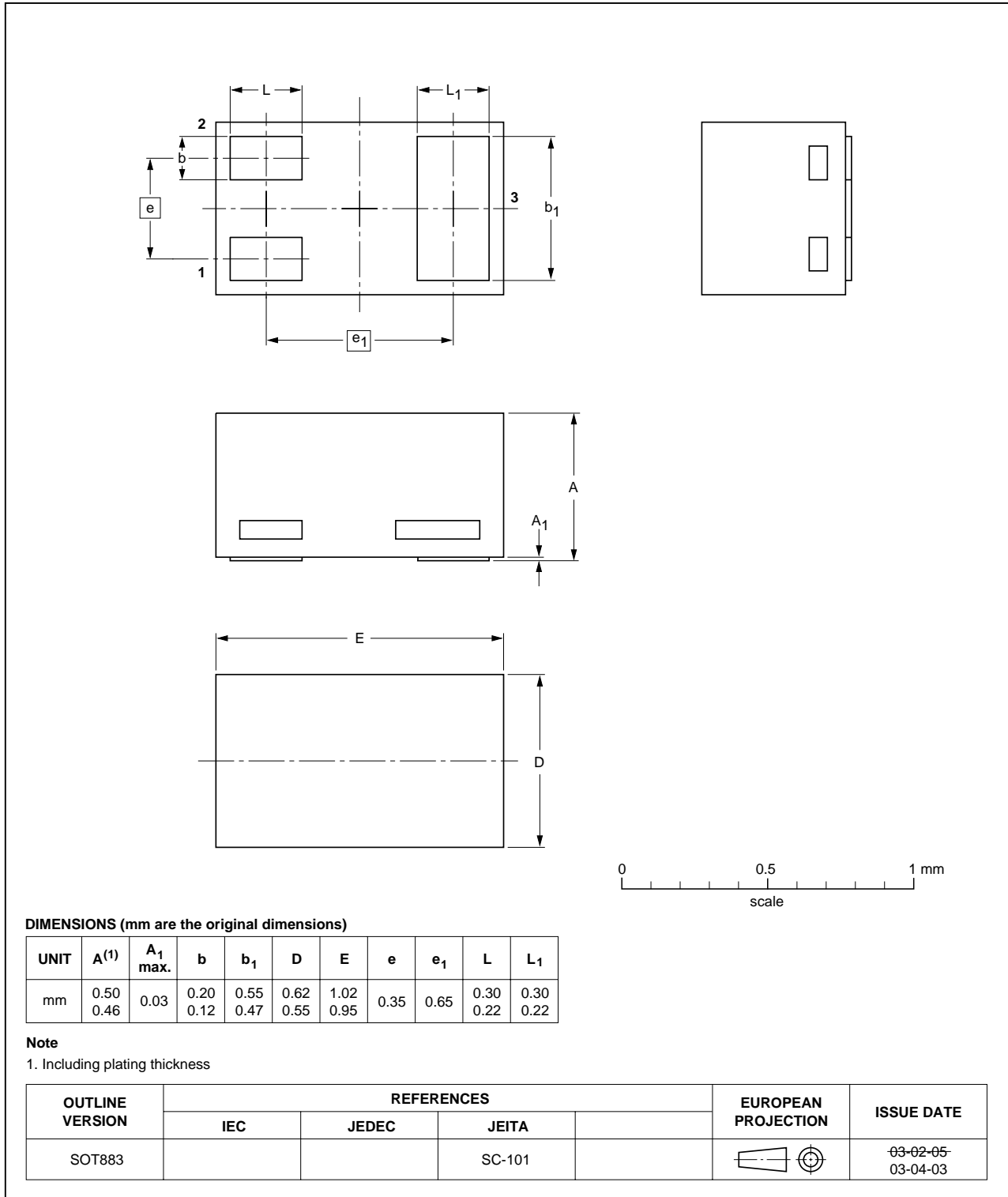


Fig 7. Package outline SOT883 (SC-101)

Plastic single-ended leaded (through hole) package; 3 leads

SOT54

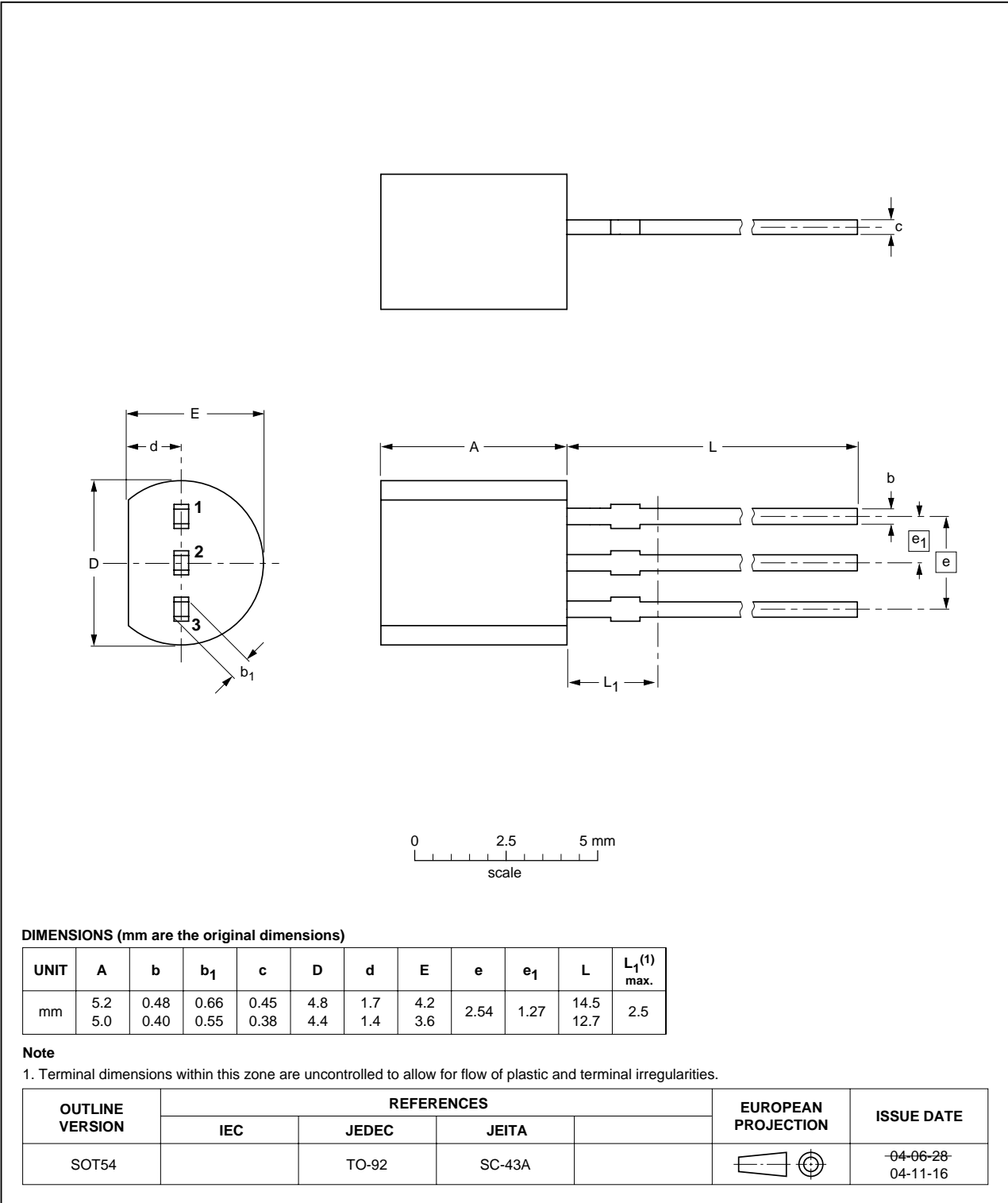


Fig 8. Package outline SOT54 (SC-43A/TO-92)

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)

SOT54A

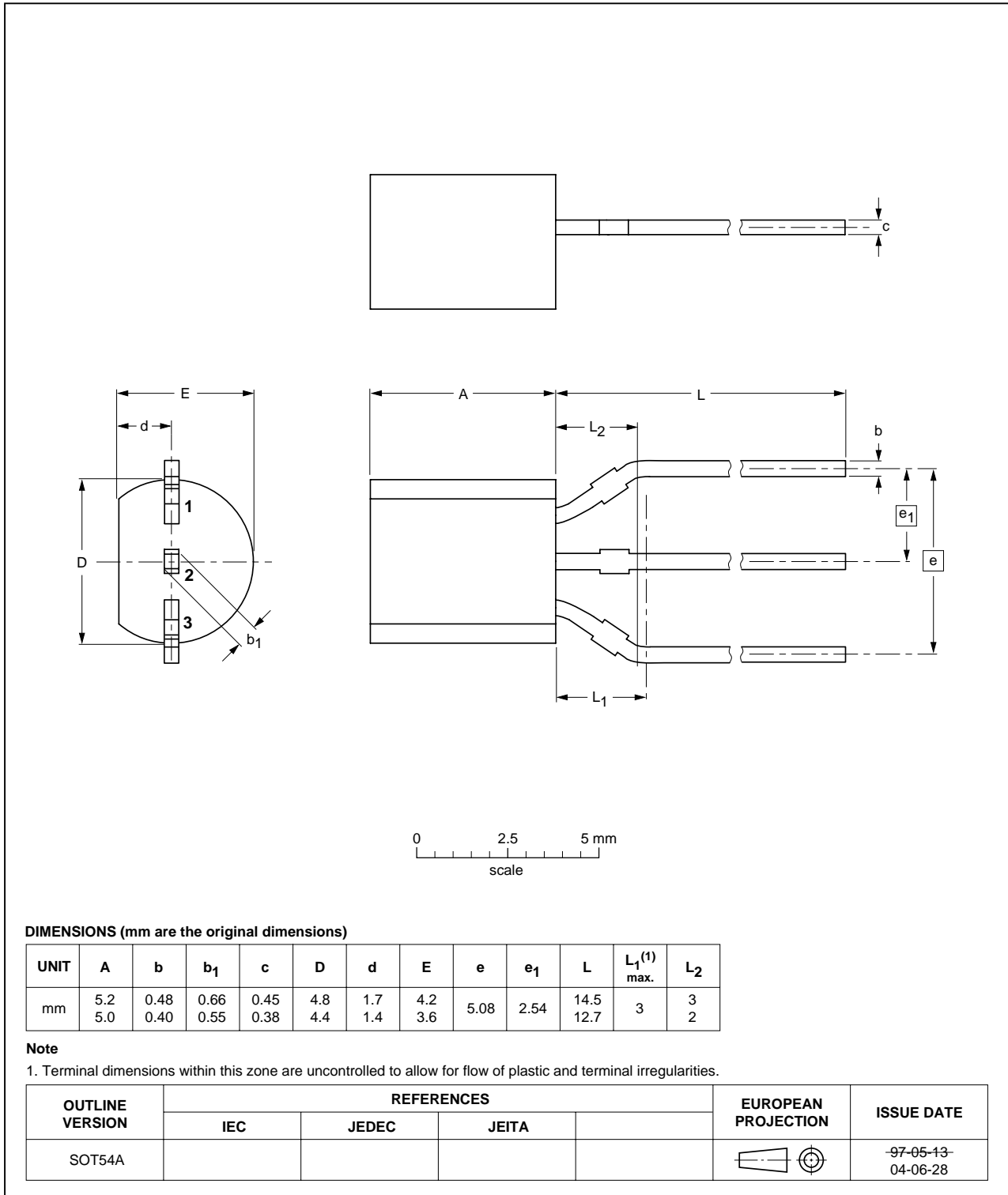


Fig 9. Package outline SOT54A

Plastic single-ended leaded (through hole) package; 3 leads (on-circle)

SOT54 variant

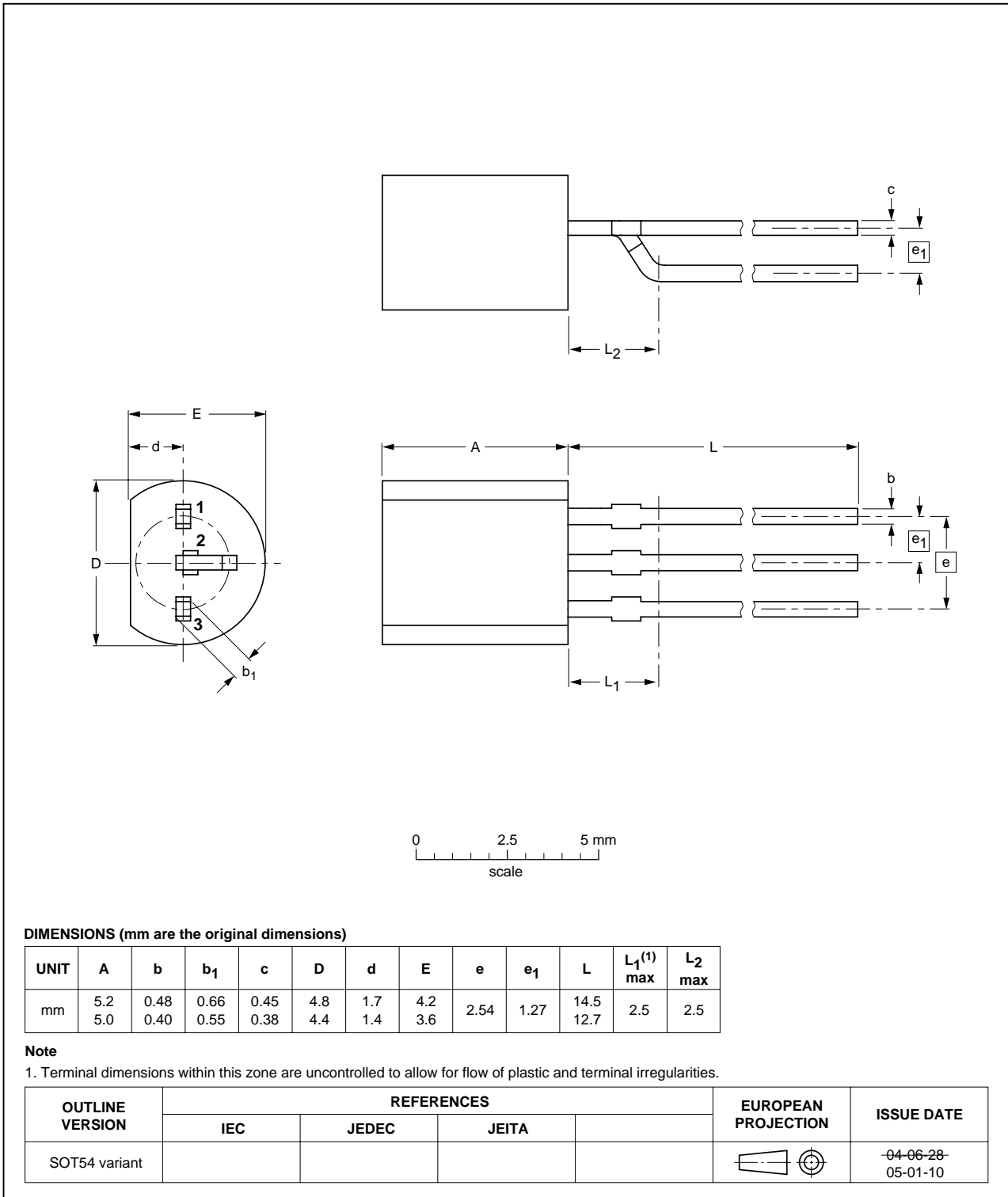


Fig 10. Package outline SOT54 variant

Plastic surface-mounted package; 3 leads

SOT23

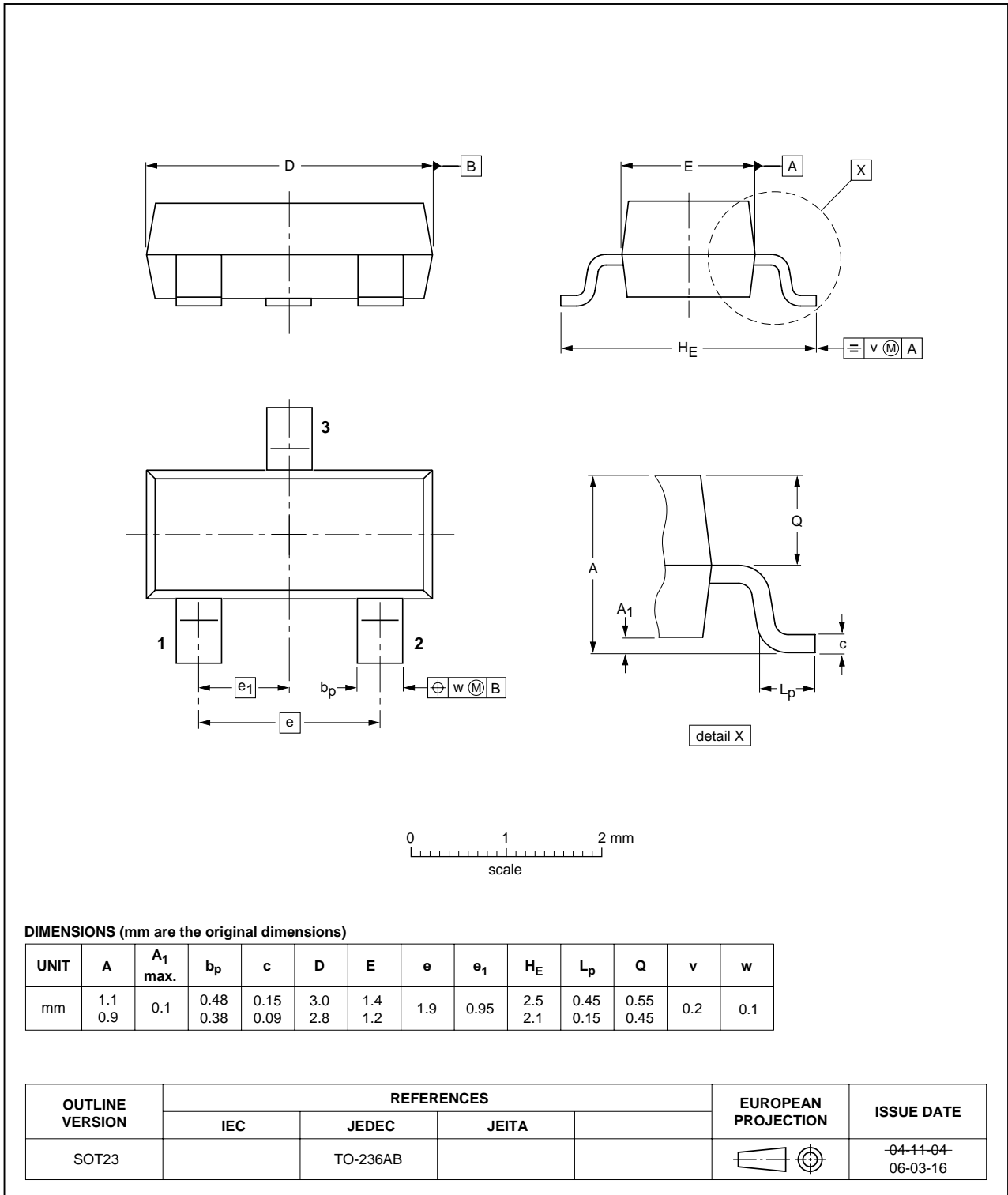


Fig 11. Package outline SOT23 (TO-236AB)

Plastic surface-mounted package; 3 leads

SOT323

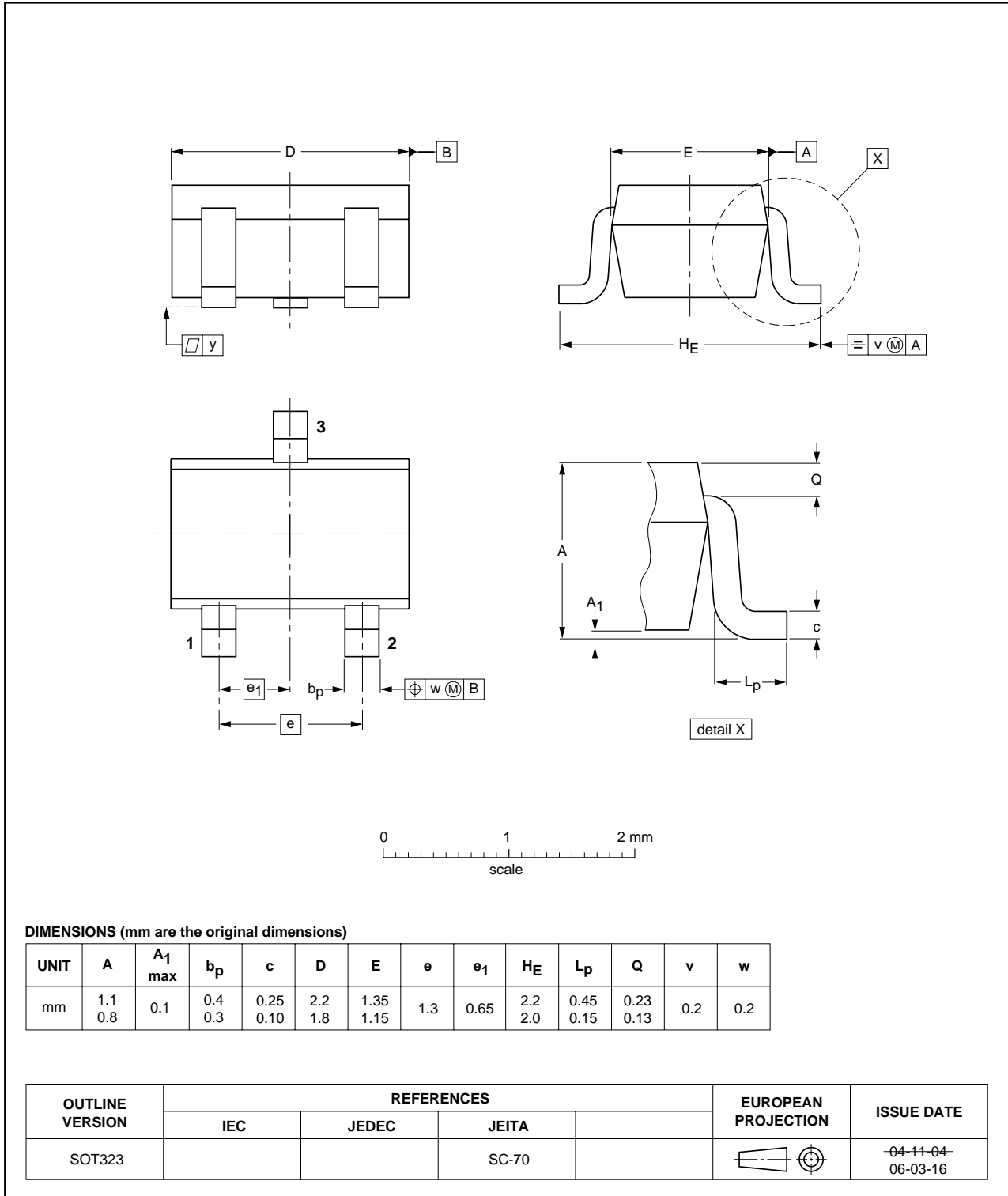


Fig 12. Package outline SOT323 (SC-70)

## 9. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code. [1]

Type number	Package	Description	Packing quantity		
			3000	5000	10000
PDTA113EE	SOT416	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113EK	SOT346	4 mm pitch, 8 mm tape and reel	-115	-	-135
PDTA113EM	SOT883	2 mm pitch, 8 mm tape and reel	-	-	-315
PDTA113ES	SOT54	bulk, straight leads	-	-412	-
	SOT54A	tape and reel, wide pitch	-	-	-116
	SOT54A	tape ammopack, wide patch	-	-	-126
	SOT54 variant	bulk, delta pinning	-	-112	-
PDTA113ET	SOT23	4 mm pitch, 8 mm tape and reel	-215	-	-235
PDTA113EU	SOT323	4 mm pitch, 8 mm tape and reel	-115	-	-135

[1] For further information and the availability of packing methods, see [Section 12](#).

## 10. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PDTA113E_SER_5	20090902	Product data sheet	-	PDTA113E_SER_4
Modifications:	<ul style="list-style-type: none"> <li>• This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content.</li> <li>• <a href="#">Figure 5 "Package outline SOT416 (SC-75)"</a> updated</li> <li>• <a href="#">Figure 6 "Package outline SOT346 (SC-59A/TO-236)"</a> updated</li> <li>• <a href="#">Figure 11 "Package outline SOT23 (TO-236AB)"</a> updated</li> <li>• <a href="#">Figure 12 "Package outline SOT323 (SC-70)"</a> updated</li> </ul>			
PDTA113E_SER_4	20050405	Product data sheet	-	PDTA113ET_3
PDTA113ET_3	20040720	Objective data sheet	-	PDTA113ET_2
PDTA113ET_2	20040415	Objective data sheet	-	PDTA113ET_1
PDTA113ET_1	20040316	Objective data sheet	-	-

## 11. Legal information

### 11.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 2 September 2009

Document identifier: PDTA113E\_SER\_5

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