THE DATASHEET OF

TPS659121YFFT

www.win-source.net 0086-755-83957316

TPS65912x PMU for Processor Power

1 Device Overview

1.1 Features

- Four Step-Down Converters:
  - V_{IN} Range From 2.7 V to 5.5 V
  - Power Save Mode at Light Load Current
  - Output Voltage Accuracy in PWM Mode ±2%
  - Typical 26-µA Quiescent Current per Converter
  - Dynamic Voltage Scaling
  - 100% Duty Cycle for Lowest Dropout
- Ten LDOs:
  - 8 General-Purpose LDOs
  - Output Voltage Range From 0.8 V to 3.3 V
  - 2 Low-Noise RF-LDOs
  - Output Voltage Range From 1.6 V to 3.3 V
  - 32-µA Quiescent Current
  - Preregulation Support by Separate Power Inputs
  - ECO Mode
  - V_{IN} Range of LDOs Respective to the Following Voltage Ranges:
    - 1.8 V to 3.6 V
    - 3.0 V to 5.5 V
- Three LED Outputs:
  - Internal Dimming Using I^2C
  - Multiplexed With GPIOs
  - Up to 20 mA per Current Sink
- Thermal Monitoring
  - High Temperature Warning
  - Thermal Shutdown
- Bypass Switch
  - Used With DCDC4 in Applications Powering an RF-PA
  - For Example, as Supply Switch for SD Cards
- Interface
  - I^2C Interface
  - Power I^2C Interface for Dynamic Voltage Scaling
  - SPI
- 32-kHz RC Oscillator
- Undervoltage Lockout and Battery Fault Comparator
- Long Button-Press Detection
- Flexible Power-Up and Power-Down Sequencing
- 3.6-mm × 3.6-mm DSBGA Package With 0.4-mm Pitch

1.2 Applications

- Data Cards
- Smart Phones
- Wireless Routers and Switches
- Tablets
- Industrial Applications
- LTE Modem
- GPS

1.3 Description

The TPS65912x device provides four configurable step-down converters with up to 2.5-A output current for memory, processor core, I/O, or preregulation of LDOs. The device also contains ten LDO regulators for external use. These LDOs can be supplied from either a battery or a preregulated supply. Power-up or power-down controller is configurable and can support any power-up or power-down sequences (OTP-based). The TPS65912x device integrates a 32-kHz RC oscillator to sequence all resources during power up or power down. All LDOs and DC-DC converters can be controlled by I^2C-SPI interface or basic ENABLE balls. In addition, an independent automatic voltage-scaling interface allows for transitioning DC-DC to a different voltage by I^2C or basic Roof/Floor Control. Three RGB LEDs with an advanced dimming feature are integrated inside the device. GPIO functionality is multiplexed with LED/ENABLE/SPI when not used. Each GPIO can be configured as part of the power-up sequence to control external resources. One SLEEP pin enables power mode control between active mode and preprogrammed sleep mode for power optimization. For system control, the TPS65912x device has one comparator for system state management. The TPS65912x device comes in a 9-pin × 9-pin DSBGA package (3.6 mm × 3.6 mm) with a 0.4-mm pitch.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE
TPS65912x	DSBGA (81)	3.6 mm × 3.6 mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information* section.

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the TPS65912x device.

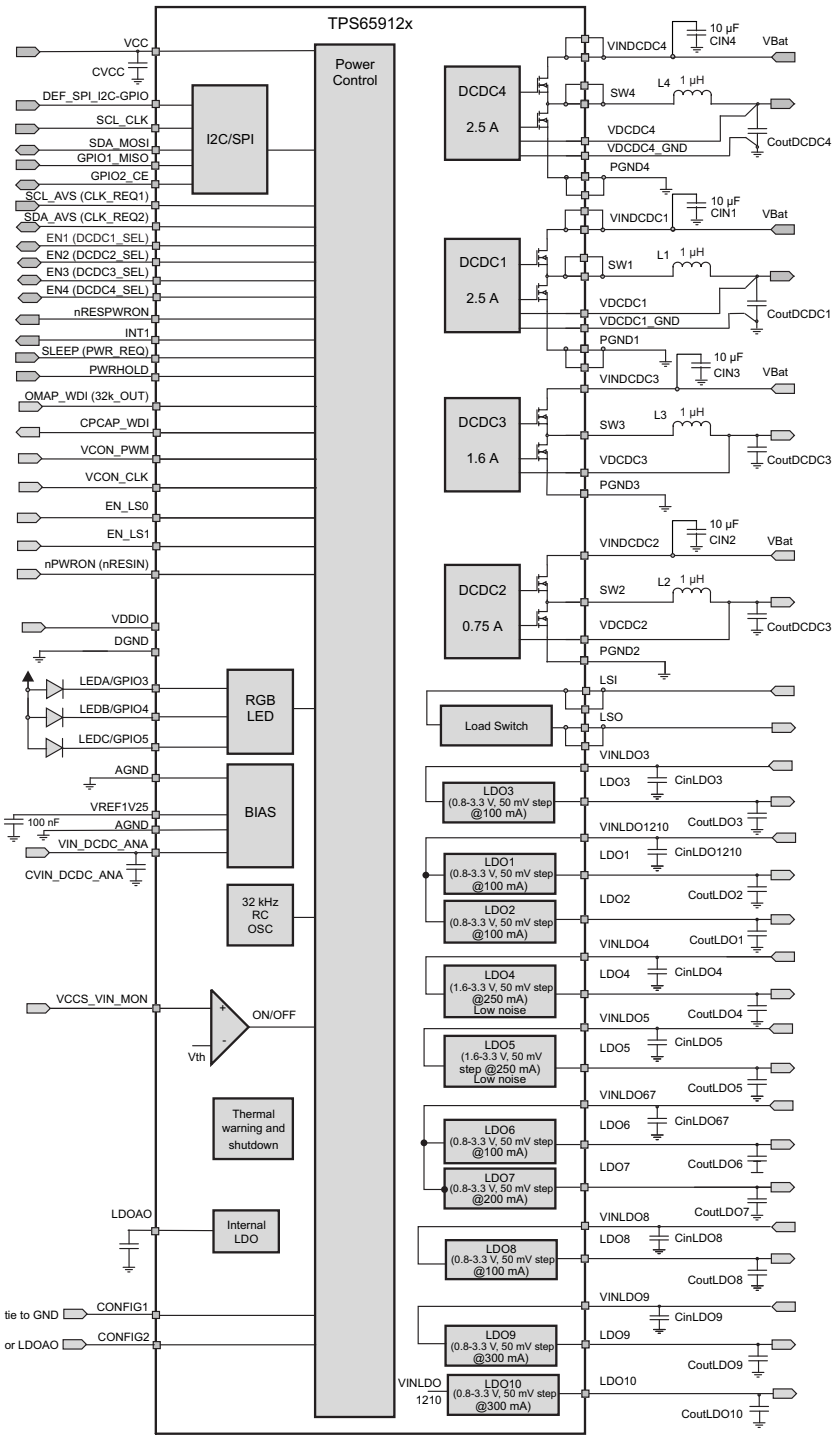

Figure 1-1. TPS65912x Block Diagram

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2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2015) to Revision C	Page
• Deleted the *Ordering Information* table	5
• Changed the TPS659122 default output voltage setting for CONFIG1=LOW for DCDC1_OP / DCDC1_AVS, DCDC3_OP / DCDC3_AVS, and DCDC4_OP / DCDC4_AVS in the *Default Settings for TPS659122* table	5
• Changed some bit values for TPS659122 for CONFIG1=LOW and TPS659122 for CONFIG1=HIGH in the ECEC and LDO register sections	63
• Added the *Application Information*, *Design Parameters*, external component list, and *Layout Example*	124
• Added the *Receiving Notification of Documentation Updates* section	137

Changes from Revision A (March 2015) to Revision B	Page
• Changed Applications section	1

Changes from Original (August 2012) to Revision A	Page
• Changed format of the data sheet to TI standard	1
• Added TPS659122 part number	1

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3 Default Settings

Table 3-1 lists the default output voltages for the DC-DC converters and the LDOs. For DCDC1 to DCDC4 and LDO1 to LDO4, there are two registers defining the output voltage. DCDCx_OP and LDOx_OP is used in active mode when CONFIG2=1. With CONFIG2=0, the status of the DCDCx_SEL pin is used to select between register _OP vs _AVS. With DCDCx_SEL=0, the _OP register defines the output voltage while _AVS sets the output voltage when DCDCx_SEL=1. LDO1 to LDO4 can be mapped to one of the DCDCx_SEL pins. See *Section 7.13* for register DEF_VOLT_MAPPING for details.

Table 3-1. Default Settings for TPS659121

Converter / LDO register	TPS659121 default output voltage setting for CONFIG1=LOW	TPS659121 default output voltage setting for CONFIG1=HIGH
DCDC1_OP / DCDC1_AVS	0.85 V / 0.90 V	0.85 V / 0.90 V
DCDC2_OP / DCDC2_AVS	1.8 V / 2.0 V	1.8 V / 2.0 V
DCDC3_OP / DCDC3_AVS	3.2 V / 2.7 V	3.2 V / 2.7 V
DCDC4_OP / DCDC4_AVS	0.5 V / 0.5 V	0.5 V / 0.5 V
LDO1_OP / LDO1_AVS	0.85 V / 0.90 V	0.85 V / 0.90 V
LDO2_OP / LDO2_AVS	0.85 V / 0.90 V	0.85 V / 0.90 V
LDO3_OP / LDO3_AVS	2.85 V / 1.20 V	2.85 V / 1.20 V
LDO4_OP / LDO4_AVS	1.8 V / 1.7 V	1.8 V / 1.7 V
LDO5	2.7 V	2.7 V
LDO6	1.8 V	1.8 V
LDO7	3.0 V	3.0 V
LDO8	3.1 V	3.1 V
LDO9	3.0 V	3.0 V
LDO10	1.8 V	1.8 V

Table 3-2. Default Settings for TPS659122

Converter / LDO register	TPS659122 default output voltage setting for CONFIG1=LOW	TPS659122 default output voltage setting for CONFIG1=HIGH
DCDC1_OP / DCDC1_AVS	1.1375 V/1.375 V	1.2 V / 1.1 V
DCDC2_OP / DCDC2_AVS	1.8 V / 1.8 V	1.8 V / 1.8 V
DCDC3_OP / DCDC3_AVS	1.1375 V/1.375 V	2.1 V / 2.0 V
DCDC4_OP / DCDC4_AVS	1.1375 V/1.375 V	3.3 V / 3.3 V
LDO1_OP / LDO1_AVS	1.7 V / 1.7 V	1.8 V / 3.0 V
LDO2_OP / LDO2_AVS	0.8 V / 0.8 V	3.0 V / 1.8 V
LDO3_OP / LDO3_AVS	0.8 V / 0.8 V	3.0 V / 3.0 V
LDO4_OP / LDO4_AVS	1.8 V / 1.8 V	1.85 V / 1.85 V
LDO5	1.8 V	1.85 V
LDO6	0.8 V	1.85 V
LDO7	1.8 V	1.85 V
LDO8	1.8 V	2.85 V
LDO9	3.3 V	1.85 V
LDO10	1.2 V	3.0 V

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4 Pin Configuration and Functions

Figure 4-1 shows the 81-Pin YFF Die-Size Ball-Grid Array pin assignments.

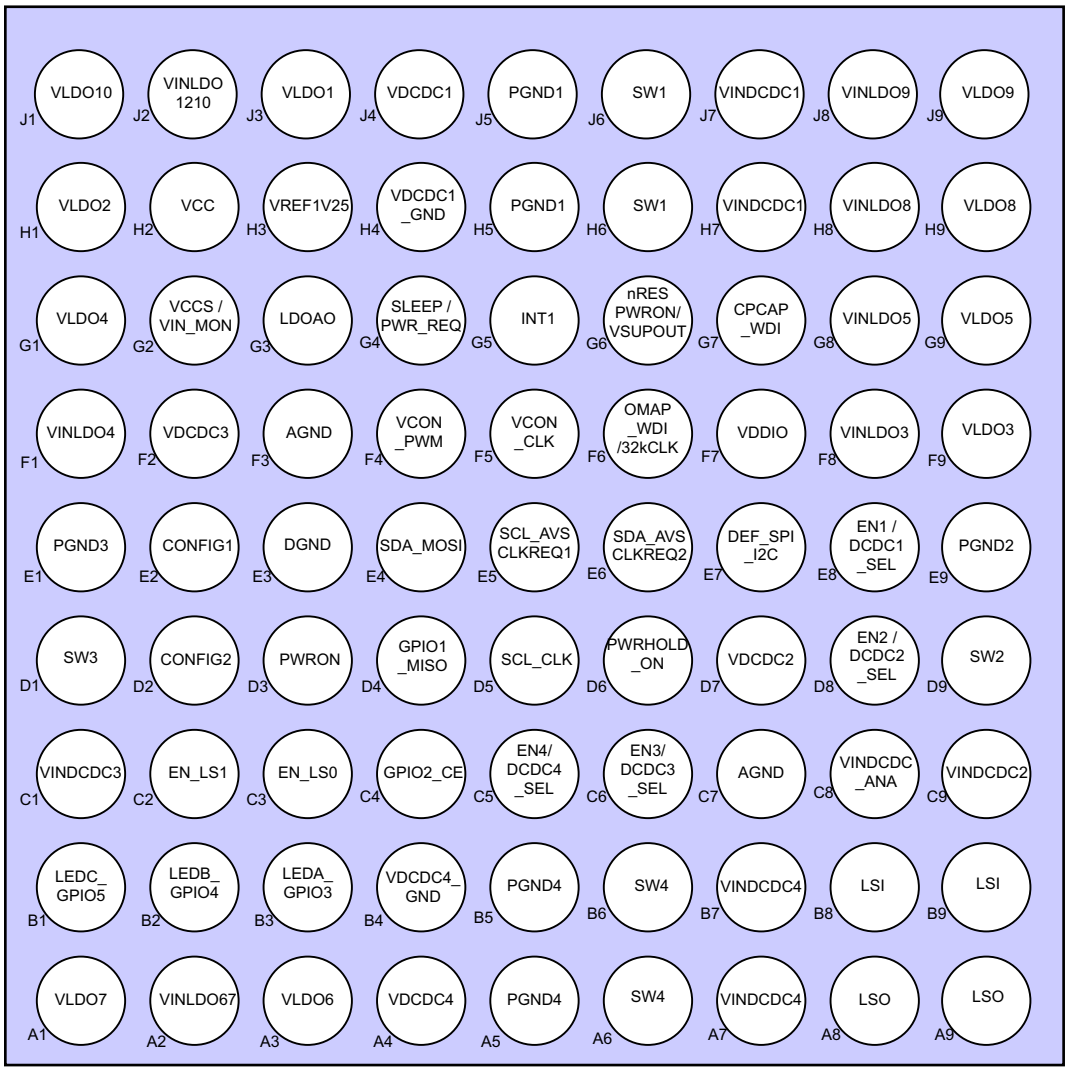

Figure 4-1. 81-Pin YFF DSBGA (Bottom View)

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4.1 Pin Functions

Pin Functions

TERMINAL			TYPE	DESCRIPTION
NAME	ALT NAME	NO.		
REFERENCE				
VREF1V25		H3	O	Internal reference voltage. Connect a 100-nF capacitor from this pin to GND. Do not load this pin externally.
AGND		F3, C7	–	Analog ground connection; connect to PGND on the PCB
DRIVERS / LIGHTING				
LEDA/GPIO3		B3	I/O	General-purpose I/O or LED driver output
LEDB/GPIO4		B2	I/O	General-purpose I/O or LED driver output
LEDC/GPIO5		B1	I/O	General-purpose I/O or LED driver output
STEP-DOWN CONVERTERS				
VINDCDC_ANA		C8	I	Analog supply input for DC-DC converters; must be connected to VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC4
VINDCDC1		H7, J7	I	Power input to DCDC1 converter; connect to VINDCDC2, VINDCDC3, VINDCDC4 and VINDCDC_ANA
VDCDC1		J4	I	Voltage sense (feedback) input "+" for DCDC1
VDCDC1_GND		H4	I	Voltage sense (feedback) input GND for DCDC1; tie to the GND plane or to AGND, alternatively tie to the GND-pad of the output capacitor
SW1		H6, J6	O	Switch node of DCDC1; connect output inductor
PGND1		H5, J5	–	Power GND connection for DCDC1 converter
VCON_PWM		F4	I	PWM period signal for dynamic voltage scaling on DCDC1
VCON_CLK		F5	I	Clock signal for dynamic voltage scaling on DCDC1
VINDCDC2		C9	I	Power input to DCDC2 converter; connect to VINDCDC1, VINDCDC3, VINDCDC4 and VINDCDC_ANA
VDCDC2		D7	I	Voltage sense (feedback) input for DCDC2
SW2		D9	O	Switch node of DCDC2; connect output inductor
PGND2		E9	–	Power GND connection for DCDC2 converter
VINDCDC3		C1	I	Power input to DCDC3 converter; connect to VINDCDC1, VINDCDC2, VINDCDC4 and VINDCDC_ANA
VDCDC3		F2	I	Voltage sense (feedback) input for DCDC3
SW3		D1	O	Switch node of DCDC3; connect output inductor
PGND3		E1	–	Power GND connection for DCDC3 converter
VINDCDC4		A7, B7	I	Power input to DCDC4 converter; connect to VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC_ANA
VDCDC4		A4	I	Voltage sense (feedback) input "+" for DCDC4
VDCDC4_GND		B4	I	Voltage sense (feedback) input GND for DCDC4; tie to the GND plane or to AGND, alternatively tie to the GND-pad of the output capacitor
SW4		A6, B6	O	Switch node of DCDC4; connect output inductor
PGND4		A5, B5	–	Power GND connection for DCDC4 converter
LOAD SWITCH				
LSI		B8, B9	I	Input of the load switch
LSO		A8, A9	O	Output of the load switch
EN_LS0		C3	I	Load switch enable pin; the status is copied to Bit [LOADSWITCH:ENABLE0] in state CONFIG
EN_LS1		C2	I	Load switch enable pin; the status is copied to Bit [LOADSWITCH:ENABLE1] in state CONFIG

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Pin Functions (continued)

TERMINAL			TYPE	DESCRIPTION
NAME	ALT NAME	NO.		
LOW DROPOUT REGULATORS				
VINLDO1210		J2	I	Power input for LDO1, LDO2 and LDO10
VINLDO3		F8	I	Power input for LDO3
VINLDO4		F1	I	Power input for LDO4
VINLDO5		G8	I	Power input for LDO5
VINLDO67		A2	I	Power input for LDO6 and LDO7
VINLDO8		H8	I	Power input for LDO8
VINLDO9		J8	I	Power input for LDO9
LDOAO		G3	O	"LDO always on" internal supply; connect buffer capacitor
VLDO1		J3	O	LDO1 output
VLDO2		H1	O	LDO2 output
VLDO3		F9	O	LDO3 output
VLDO4		G1	O	LDO4 output
VLDO5		G9	O	LDO5 output
VLDO6		A3	O	LDO6 output
VLDO7		A1	O	LDO7 output
VLDO8		H9	O	LDO8 output
VLDO9		J9	O	LDO9 output
VLDO10		J1	O	LDO10 output
STANDARD INTERFACE				
DEF_SPI_I2C-GPIO		E7	I	Digital input that defines whether SPI or I^2C and GPIOs is available on pins C4, D4, E4, D5: 0=SPI; 1=I2C and GPIO1 and GPIO2
SCL_SCK	SCK	D5	I	I^2C SCL for DEF_SPI_I2C=1 or SPI SCK for DEF_SPI_I2C=0
SDA_MOSI	MOSI	E4	I/O	I^2C SDA for DEF_SPI_I2C=1 or SPI MASTER OUT SLAVE IN (MOSI) for DEF_SPI_I2C=0
GPIO1_MISO	MISO	D4	I/O	GPIO1 for DEF_SPI_I2C=1 or SPI MASTER IN SLAVE OUT (MISO) for DEF_SPI_I2C=0
GPIO2_ CE	CE	C4	I/O	GPIO2 for DEF_SPI_I2C=1 or SPI CHIP ENABLE (CE) active HIGH for DEF_SPI_I2C=0
ENABLE / VOLTAGE SCALING				
EN1 / DCDC1_SEL(1)	DCDC1_SEL	E8	I	Enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 predefined values
EN2 / DCDC2_SEL(1)	DCDC2_SEL	D8	I	Enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 predefined values
EN3 / DCDC3_SEL(1)	DCDC3_SEL	C6	I	Enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 predefined values
EN4 / DCDC4_SEL(1)	DCDC4_SEL	C5	I	Enable pin or voltage scaling pin changing the output of a converter or a group of converters between 2 predefined values
SCL_AVS / CLK_REQ1(2)	CLK_REQ1	E5	I	Power I^2C for dynamic voltage scaling: clock pin or clock request signal1 used to enable and disable power resources
SDA_AVS / CLK_REQ2(2)	CLK_REQ2	E6	I/O	Power I^2C for dynamic voltage scaling; data pin or clock request signal2 used to enable and disable power resources
SLEEP / PWR_REQ(2)	PWR_REQ	G4	I	SLEEP mode input or CLK request input
nRESPWRON / VSUP_OUT	VSUP_OUT	G6	O	Reset output or output of voltage monitor
VCCS / VIN_MON	VIN_MON	G2	I	Voltage sense for input voltage monitor; output on pin VSUP_OUT
PWRHOLD_ON	ON	D6	I	POWERHOLD or ON; enable input
INT1		G5	O	Interrupt output

(1) DCDCx_SEL is selected by pulling pin CONFIG2 to GND; this also selects CLK_REQx and PWR_REQ as enable resources.
(2) CLK-REQ1, CLK_REQ2 and PWR_REQ is selected by puling pin CONFIG2 to GND.

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Pin Functions (continued)

TERMINAL			TYPE	DESCRIPTION
NAME	ALT NAME	NO.		
nPWRON	/RESIN (optional)	D3	I	Active low, debounced power-on input or power-request input to start power-up sequencing; alternatively active-low reset input to TPS65912x; debounced by 10 ms (OTP option); tie to LDOAO for a logic high if not used.
OMAP_WDI_32k_OUT		F6	I	Input from OMAP WDI pin to AND gate; alternatively 32-kHz RC oscillator output
CPCAP_WDI		G7	O	Push-pull output at VDDIO level of AND gate; connect to CPCAP WDI input
CONFIG1		E2	I	Selects predefined startup options and default voltages; chooses from two internal OTP settings; tie to GND or LDOAO
CONFIG2		D2	I	Selects predefined startup options; configures pins as DCDC1_SEL, DCDC2_SEL, DCDC3_SEL and DCDC4_SEL as well as CLK_REQ and PWR_REQ signals with CONFIG2 tied to GND. Tie to LDOAO for a logic high level.
VCC		H2	I	Digital supply input
VDDIO		F7	I	Supply voltage input for GPIOs and output stages that sets the HIGH level voltage (I/O voltage)
DGND		E3	–	Digital GND connection, tie to AGND and PGNDx on the PCB

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	All pins except A/PGND pins and pins listed below with respect to AGND	–0.3	6	V
	VLDO1, VLDO2, VLDO3, VLDO4, VLDO5, VLDO6, VLDO7,VLDO8, VLDO9, VLDO10, VINLDO1210, VINLDO3, EN1 (DCDC1_SEL), EN2 (DCDC2_SEL), EN3 (DCDC3_SEL), EN4 (DCDC4_SEL) SLEEP (PWR_REQ), CLK_REQ1, CLK_REQ2 VDDIO, CONFIG1, CONFIG2, DEF_SPI_I2C-GPIO, EN_LS0, EN_LS1, OMAP_WDI, CPCAP_WDI, VCON_CLK with respect to AGND	–0.3	3.6	
	Pin VDCDC1, VDCDC2, VDCDC3, VDCDC4 with respect to AGND	–0.3	3.8	
	Pins SDA_SDI, SCL_SCK, SDO_GPIO1, SCE_GPIO2, SDA_AVS, SCL_AVS, INT1, 32KCLKOUT,GPIO3 and GPIO4 and GPIO5 if defined as GPIOs with push-pull output (otherwise it is 6-V rated), NRESPWRON if nRESPWRON is push-pull output (otherwise it is 6-V rated) with respect to AGND	–0.3	VDDIO + 0.3	
	V_{CC}	VDDIO	6	
Current	All non power pins		5	mA
	Power pins (per pin)		2	A
Operating free-air temperature, T_A		–40	85	°C
Maximum junction temperature, T_J			125	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Section 5.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS001(1)	1000	V
		Charged device model (CDM), per JESD22-C101(2)	250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
DC-DC CONVERTERS					
VIN1, VIN2, VIN3, VIN4	Input voltage for step-down converter DCDC1, DCDC2, DCDC3, DCDC4	2.7		5.5	V
	Output voltage for step-down converter DCDC1, DCDC2, DCDC3 (1)	0.5		3.8	V
	Output voltage for step-down converter DCDC4 (1)	0.5		3.8	V
	Inductance at L2, L3	0.5	1.0	1.3	µH
	Inductance at L1, L4	0.5	1.0	1.3	µH
C_{IN1} , C_{IN4}	Input capacitance at VIN1 and VIN4 (on each pin)	10	22		µF
C_{IN2} , C_{IN3}	Input capacitance at VIN2 and VIN3 (on each pin)	4.7	10		µF
$C_{OUTDCDC1,2,3}$	Output capacitance at DCDC1, DCDC2 and DCDC3	4.7	10	22	µF
$C_{OUTDCDC4}$	Output capacitance at DCDC4	10	22	47	µF
LDOs					
VINLDO1210	Input voltage range for LDO1, LDO2 and LDO10	1.7		3.6	V
VINLDO4	Input voltage range for LDO4	1.9		5.5	V
VINLDO5	Input voltage range for LDO5	1.9		5.5	V
V_{LDO1}, V_{LDO2}, V_{LDO3}, V_{LDO6}, V_{LDO7}, V_{LDO8}, V_{LDO9}, V_{LDO10}	Output voltagefor general purpose (GP) LDOs (1)	0.8		3.3	V
V_{LDO4}, V_{LDO5},	Output voltage for RF-LDOs	1.6		3.3	V
$C_{INLDO1210}$ C_{INLDO3}, C_{INLDO4}, C_{INLDO5}, $C_{INLDO67}$ C_{INLDO8} C_{INLDO8}	Input capacitance on LDO supply pins	0.5			µF
$C_{outLDO4}$, $C_{outLDO5}$	Output capacitance on LDO4 and LDO5	2.2		10	µF
$C_{outLDO1}$, $C_{outLDO2}$ $C_{outLDO3}$ $C_{outLDO6}$ $C_{outLDO7}$ $C_{outLDO8}$	Output capacitance LDO1, LDO2, LDO3, LDO6, LDO7, LDO8 These LDOs are *capless*, the required capacitance can be placed at the load	0.5		10	µF
$C_{outLDO9}$ $C_{outLDO10}$	Output capacitance LDO9 and LDO10 These LDOs are *capless*, the required capacitance can be placed at the load	1		10	µF
$C_{outLDOAO}$	Output capacitance on LDOAO	0.5		10	µF
$C_{VIN_DCDC_ANA}$	Input capacitance on VIN_DCDC_ANA	100			nF
C_{VCC}	Input capacitance on VCC	100			nF
C_{VDDIO}	Input capacitance on VDDIO	100			nF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) The maximum output voltage of DCDC1 to DCDC4 and LDO1 to LDO4 can be reduced by a OTP setting to adopt the maximum voltage to the requirements (or maximum ratings) of the load powered. This allows to protect the processor from exceeding the maximum ratings for the core voltage. The value is set at TI upon customer request in nonvolatile memory (OTP).

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5.4 Thermal Characteristics

THERMAL METRIC(1)		TPS65912 YFF (DSBGA) 81 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	41.3	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	0.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.2	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

5.5 Electrical Characteristics – DCDC1, DCDC2, and DCDC3

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		2.3		5.5	V
V_{DCDC1} V_{DCDC2} V_{DCDC3}	DCDCx Output Voltage Range	Option1; in 12.5-mV steps; RANGE[1,0] = 00	0.5		1.2875	V
		Option2; in 12.5-mV steps; RANGE[1,0] = 01	0.7		1.4875	V
		Option3; in 25-mV steps; RANGE[1,0] = 10	0.5		2.075	V
		Option4; in 50-mV steps; RANGE[1,0] = 11	0.5		3.80	V
$I_{OUT(DCDCx)}$	Continuous Output Current	DCDC1 (VINDCDC1 ≥ 2.8 V)			2500	mA
		DCDC2 (VINDCDC2 ≥ 2.8 V)			750	
		DCDC3 (VINDCDC3 ≥ 2.8 V)			1200	
		DCDC3 for V_{IN}= 2.8 V to 4.5 V; VDCDC3(max) = 1.4875 V			1600	
I_Q	Quiescent Current	I_{LOAD} = 0 mA, DCDCx_MODE = 0, Device not switching; for DCDC1		26	55	µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 1, Device switching; for DCDC1		8		mA
		I_{LOAD} < 1 mA, Device not switching; ECO = **1** *AND* DCDCx_MODE = **0**, for DCDC1		9		µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 0, Device not switching, for DCDC2 or DCDC3		26	40	µA
		I_{LOAD} = 0 mA, DCDCx_MODE = 1, Device switching, for DCDC2 or DCDC3		8		mA
		I_{LOAD} < 1 mA, Device not switching; ECO = **1** *AND* DCDCx_MODE = **0**, for DCDC2 or DCDC3		3		µA
$V_{DCDC1/2/3}$	Accuracy	DCDCx_MODE = **1**, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C, ECO = **0**	–2%			
		DCDCx_MODE = 1, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = –40°C – 85°C, ECO = **0**	–2.5%			
		DCDCx_MODE = **0**, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C, ECO = **0**	–3%			
	ECO Mode Accuracy	V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = –40 – 85°C; ECO = **1** *AND* DCDCx_MODE = **0**	–5%		5%	
	Load Regulation	DCDCx_MODE = **1**, V_{IN} = 3.6 V; I_{LOAD} = 120 mA to 1080 mA; for DCDC1		0.01		%/A
		DCDCx_MODE = **1**, V_{IN} = 3.6 V; I_{LOAD} = 120 mA to 1080 mA; for DCDC3		0.01		
		DCDCx_MODE = **1**, V_{IN} = 3.6 V; I_{LOAD} = 50 mA to 450 mA; for DCDC2		0.01		
	Line Regulation	DCDCx_MODE = **1**, V_{IN} = 2.5 to 5.5 V, I_{LOAD} = 0 mA, for DCDC1		0.01		%/V
		DCDCx_MODE = **1**, V_{IN} = 2.5 to 5.5 V, I_{LOAD} = 0 mA, for DCDC2 or DCDC3		0.01		

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Electrical Characteristics – DCDC1, DCDC2, and DCDC3 *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
f_{SW}	Switching Frequency	DCDCx_MODE = **0**			3500	kHz
		DCDCx_MODE = **1**, V_{IN} = 3.6 V, V_{OUT} = 1.8 V		2800		kHz
$R_{DS(ON)}$	High-Side FET On-Resistance	for DCDC1 with VIN_DCDCx = 3.6 V, D = 100%		60	100	mΩ
		for DCDC2 and DCDC3 with VIN_DCDCx = 3.6 V, D = 100%		120	190	mΩ
$R_{DS(ON)}$	Low-Side FET On-Resistance	for DCDC1 with VIN_DCDCx = 3.6 V, D = 100%		60	100	mΩ
		for DCDC2 and DCDC3 with VIN_DCDCx = 3.6 V, D = 100%		100	160	mΩ
I_{LK_HS}	High-Side FET Leakage Current	T_J = 85°C; DCDC1; VINDCDC1 = 4.2 V			20	µA
		T_J = 85°C; DCDC2 or DCDC3; VINDCDC2 = VINDCDC3 = 4.2 V			3	
I_{LK_LS}	Low-Side FET Leakage Current	T_J = 85°C; DCDC1; VINDCDC1 = 4.2 V			20	µA
		T_J = 85°C; DCDC2 or DCDC3; VINDCDC2 = VINDCDC3 = 4.2 V			1	
I_{HS_LIMF}	High-Side Forward Current Limit	V_{IN} = 3.6 V; DCDC1	3200	4280	5300	mA
		V_{IN} = 3.6 V; DCDC2	1250	1667	2083	
		V_{IN} = 3.6 V; DCDC3	2100	2800	3500	
I_{LS_LIMF}	Low-Side Forward Current Limit	V_{IN} = 3.6 V; DCDC1	3200	4280	5300	mA
		V_{IN} = 3.6 V; DCDC2	1200	1600	2000	
		V_{IN} = 3.6 V; DCDC3	1875	2500	3125	
$t_{OFF(MIN)}$	Minimum HS FET Off Time	V_{IN} = 3.6 V		30		ns
	DCDC1 output voltage ripple	V_{IN} = 5 V; V_{OUT} = 0.95 V; I_o = 1.5 A; L = 1 µH, RSL = 50 mR; C_o = 10 µF		10		mVpp
	DCDC2 output voltage ripple	V_{IN} = 5 V; V_{OUT} = 2.0 V; I_o = 600 mA; L = 1 µH, RSL = 50 mR; C_o = 10 µF		10		mVpp
	DCDC3 output voltage ripple	V_{IN} = 5 V; V_{OUT} = 3.2 V; I_o = 600 mA; L = 1 µH, RSL = 50 mR; C_o = 10 µF		10		mVpp
	DCDC1 load transient response	V_{IN} = 5 V; V_{OUT} = 0.95 V; I_o = 1 mA to 2 A; L = 1 µH, RSL = 50 mR; C_o = 10 µF; dt = 100 ns		25		mV
	DCDC2 load transient response	V_{IN} = 5 V; V_{OUT} = 1.8 V; I_o = 1 mA to 400 mA; L = 1 µH, RSL = 50 mR; C_o = 10 µF; dt = 1 µs		50		mV
	DCDC3 load transient response	V_{IN} = 5 V; V_{OUT} = 3.2 V; I_o = 1 mA to 500 mA; L = 1 µH, RSL = 50 mR; C_o = 10 µF; dt = 1 µs		50		mV
V_{DCDCPG}	Power Good Threshold	VDCDCx falling	86%	90%	94%	
		VDCDCx rising			98%	
t_{DCDCPG}	Power Good Threshold Deglitch			1		ms
t_{Start}	Start-up time	Time to start switching, measured from end of I^2C command enabling converter	32	55	100	µs
t_{Ramp}	V_{OUT} Ramp UP time	Time to ramp from 5% to 95% of V_{OUT}	100	160	250	µs
$R_{Discharge}$	Discharge resistor		250	400	500	Ω
T_{pwm}	PWM clock period for VCON_CLK		30		300	ns
T_{su}	VCON set up time	VCON_PWM to rising edge of VCON_CLK			7	ns
T_{hd}	VCON hold time	VCON_PWM from rising edge of VCON_CLK			7	ns

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5.6 Electrical Characteristics – DCDC4

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range		2.3		5.5	V
V_{DCDC4}	DCDC4 Output Voltage Range	Option1; in 12.5-mV steps; RANGE[1,0] = 00	0.5		1.2875	V
		Option2; in 12.5-mV steps; RANGE[1,0] = 01	0.7		1.4875	
		Option3; in 25-mV steps; RANGE[1,0] = 10	0.5		2.075	
		Option4; in 50-mV steps; RANGE[1,0] = 11	0.5		3.80	
$I_{OUT(DCDC4)}$	Continuous Output Current	DCDC4 (VINDCDC4 ≥ 2.8 V)			2500	mA
I_Q	Quiescent Current	I_{LOAD} = 0 mA, DCDC4_MODE = 0, Device not switching		26	55	µA
		I_{LOAD} = 0 mA, DCDC4_MODE = 1, Device switching; EN_LS[1,0] = 00 or 01		8		mA
		I_{LOAD} < 1 mA, Device not switching; ECO = **1** *AND* DCDC4_MODE = **0**		9		µA
V_{DCDCx}	Accuracy	DCDC4_MODE = **1**, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C; EN_LS[1,0] = 00 or 01	–2%		2%	
		DCDC4_MODE = 1, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = –40°C – 85°C; EN_LS[1,0] = 00 or 01	–2.5%		2.5%	
		DCDC4_MODE = **0**, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = 25°C	–3%		3%	
		DCDC4_MODE = 0, V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = –40°C to 85°C	–3%		3%	
	ECO mode Accuracy	ECO = **1** *AND* DCDCx_MODE = **0** , V_{IN} = 3.6 V, I_{LOAD} = 0 mA, T_A = –40°C to 85°C	–5%		5%	
	Load Regulation	DCDC4_MODE = **1**, V_{IN} = 3.6 V; EN_LS[1,0] = 00 or 01; I_{LOAD} = 250 mA to 2250 mA		0.01		%/A
	Line Regulation	DCDC4_MODE = **1**, V_{IN} = 2.5 -5.5 V, I_{LOAD} = 0 mA; EN_LS[1,0] = 00 or 01		0.01		%/V
f_{SW}	Switching Frequency	DCDC4_MODE = **0**			3500	kHz
		DCDC4_MODE = **1**, V_{IN} = 3.6 V, V_{OUT} = 1.8 V, EN_LS[1,0] = 00 or 01		2800		kHz
$R_{DS(ON)}$	High-side MOSFET on-resistance	V_{IN_DCDC4} = 3.6 V, 100% duty cycle		60	100	mΩ
	Low-side MOSFET on-resistance	V_{IN_DCDC4} = 3.6 V, 0% duty cycle		60	100	mΩ
I_{LK_HS}	High-side leakage current	T_J = 85°C; VINDCDC4 = 4.2 V			20	µA
I_{LK_LS}	Low-side leakage current	T_J = 85°C; VINDCDC4 = 4.2 V			20	µA
I_{LIM}	High-side current limit	2.9 V ≤ V_{IN_DCDC4} ≤ 5.5 V	3000	4400	5000	mA
I_{LIM}	Low-side current limit	2.9 V ≤ V_{IN_DCDC4} ≤ 5.5 V	3000	3700	4300	mA
$t_{OFF(MIN)}$	Minimum HS FET Off Time	V_{IN} = 3.6 V		30		ns
	DCDC4 output voltage ripple	V_{IN} = 5 V; V_{OUT} = 3.4 V; I_o = 2 A; L = 1 µH, RSL = 50 mR; C_o = 10 µF		10		mVpp
	DCDC4 load transient response	V_{IN} = 5 V; V_{OUT} = 3.4 V; I_o = 1 mA to 2 A; L = 1 µH, RSL = 50 mR; C_o = 10 µF; dt = 10 µs		100		mV
V_{DCDCPG}	Power Good Threshold	VDCDC4 falling	86%	90%	94%	
		VDCDC1 rising			98%	
t_{DCDCPG}	Power Good deglitch time			1		ms
t_{Start}	Start-up time, (RAMP_TIME=0)	Time to start switching, measured from end of I^2C command enabling converter; DCDC4_CTRL:RAMP_TIME = 0	32	55	100	µs
	Start-up time, (RAMP_TIME=1)	Time to start switching, measured from end of I^2C command enabling converter; DCDC4_CTRL:RAMP_TIME = 1	4	7	14	µs

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Electrical Characteristics – DCDC4 *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Ramp}	V_{OUT} Ramp UP time (RAMP_TIME=0)	Time to ramp from 5% to 95% of V_{OUT} ; DCDC4_CTRL:RAMP_TIME = 0; V_{OUT} = 3.4 V	106	160	250	µs
	V_{OUT} Ramp UP time (RAMP_TIME=1)	Time to ramp from 5% to 95% of V_{OUT} ; DCDC4_CTRL:RAMP_TIME = 1; V_{OUT} = 3.4 V	25	40	66	µs
$R_{Discharge}$	Discharge resistor		250	400	500	Ω
Vbyp-on	Bypass mode turn-on duty cycle	For ENABLE[1,0]=10; turn on is based on the duty cycle of the PWM signal of DCDC4	90%	97.5%	99.5%	
Vbyp-off	Bypass mode turn-off output voltage threshold	For ENABLE[1,0]=10; turn off is based on output voltage above the nominal value	8%	12%	15%	

5.7 Electrical Characteristics – LDOs

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	LDO1	1.7		3.6	V
		LDO2	1.7		3.6	
		LDO3	1.7		3.6	
		LDO4	1.9		5.5	
		LDO5	1.9		5.5	
		LDO6	1.8		5.5	
		LDO7	1.8		5.5	
		LDO8	1.8		5.5	
		LDO9	1.8		5.5	
		LDO10	1.7		3.6	
V_{LDOx}	LDO Output Voltage for general-purpose LDOs (1)		0.8		3.3	V
	LDO Output Voltage for RF_LDOs		1.6		3.3	V
	LDO Voltage Accuracy	ECO = **0**	–2%		2.5%	
		ECO = **1**	–5%		5%	
$I_{OUT(LDOx)}$	LDO Continuous Output Current	LDO1	100			mA
		LDO2	100			
		LDO3	100			
		LDO4	250			
		LDO5	250			
		LDO6	100			
		LDO7	300			
		LDO8	100			
		LDO9	300			
		LDO10	300			
$I_{SHORT(LDOx)}$	LDO Current Limit	LDO1, LDO2, LDO3, LDO6, LDO8	100		420	mA
		LDO4, LDO5	250		650	
		LDO7	300		750	
		LDO9, LDO10	300		750	
		$I_{OUT(LDO1)}$ = 50 mA; VINLDO1 = 1.7 V			500	
		$I_{OUT(LDO2)}$ = 100 mA; VINLDO2 = 1.7 V			500	
		$I_{OUT(LDO3)}$ = 80 mA ; VINLDO3 = 1.5 V			200	

(1) LDO Output voltages are programmed separately

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Electrical Characteristics – LDOs *(continued)*

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
$V_{DO(LDOx)}$	Dropout Voltage (2)	$I_{OUT(LDO4)}$ = 200 mA; VINLDO4 = 2.0 V			200	mV
		$I_{OUT(LDO5)}$ = 200 mA; VINLDO5 = 3.0 V			300	
		$I_{OUT(LDO6)}$ = 100 mA; VINLDO6 = 3.2 V			200	
		$I_{OUT(LDO7)}$ = 200 mA; VINLDO7 = 3.2 V			200	
		$I_{OUT(LDO8)}$ = 100 mA; VINLDO8 = 2.9 V			200	
		$I_{OUT(LDO9)}$ = 300 mA (LDO9); VINLDO9 = 3.1 V			200	
		$I_{OUT(LDO10)}$ = 300 mA (LDO10); VINLDO10 = 2.0 V			200	
	Line Regulation	V_{IN} = V_{LDO} + 0.5 V and I_{LOAD} = 50 mA	–1%		1%	
	Load Regulation; ECO = **0**	LDO1, LDO2, LDO3, LDO6, LDO8: I_{LOAD} = 1 mA to 100 mA	–0.5%		0.5%	
		LDO5, LDO7: I_{LOAD} = 1 mA to 200 mA	–1%		1%	
		LDO4, LDO9, LDO10: I_{LOAD} = 1 mA to 300 mA	–1.5%		1.5%	
	Load Regulation; ECO = **1**	LDO1 to LDO10: I_{LOAD} = 0 mA to 1 mA	–5%		5%	
	Line Transient Response	dV/dt = ±0.5 V/µs	–50		50	mV
	Load Transient Response	dI/dt = 100 mA/µs; 10% to 90% load step	–110		110	mV
PSRR	Power Supply Rejection Ratio for LDO1 to LDO3 and LDO6 to LDO10	f = 10 Hz to 1 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} = 10 mA to 0.75 × $I_{LOAD(MAX)}$	47			dB
	Power Supply Rejection Ratio for LDO4 and LDO5	f = 10 Hz to 1 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} = 10 mA to 0.75 × $I_{LOAD(MAX)}$	63			
	Output voltage noise for LDO1 to LDO3 and LDO6 to LDO10	f = 10 Hz to 100 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} ≥ 10 mA		150		µVrms
		f = 10 Hz to 10 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} ≥ 10 mA		50		µVrms
	Output voltage noise for LDO4 and LDO5	f = 10 Hz to 100 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} ≥ 10 mA		30		µVrms
		f = 10 Hz to 10 kHz, V_{IN} – V_{OUT} ≥ 0.5 V, I_{LOAD} ≥ 10 mA		15		µVrms
I_q	Quiescent Current	ECO = **1**; I_{LOAD} ≤ 1 mA for LDO1, LDO2, LDO3, LDO6, LDO7, LDO8, LDO9, LDO10			8	µA
		ECO = **1**; I_{LOAD} ≤ 1 mA for LDO4, LDO5			16	
		ECO = **0**; I_{LOAD} ≤ 1 mA for LDO1, LDO2, LDO3, LDO6, LDO7, LDO8, LDO9, LDO10			32	
		ECO = **0**; I_{LOAD} ≤ 1 mA for LDO4, LDO5			40	
	ECO exit time	Minimum wait time before the full current can be drawn after ECO is set 0			50	µs
t_{Ramp}	V_{OUT} Ramp Up time	Time to ramp from 5% to 95% of V_{OUT} ; I_{OUT} = 100 mA			170	µs
V_{LDOPG}	PG Trigger	V_{LDOx} ≤ V_{TARGET} ; V_{LDOx} falling	87%	90.6%	94.5%	
		V_{LDOx} rising			98%	
t_{LDOPG}	Power Good deglitch time			1		ms
$R_{Discharge}$	Discharge resistance at LDO output	LDO disabled	200	325	450	Ω

(2) V_{DO} = V_{IN} – V_{OUT}, where V_{OUT} = $V_{OUT(NOM)}$ – 2%

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5.8 Electrical Characteristics – Digital Inputs, Digital Outputs

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{IL}	Low-Level Input Voltage		0	0.4	V
V_{IH}	High-Level Input Voltage	All pins except digital interfaces and configuration pins listed below	1.1	V_{CC}	V
		For CONFIG1, CONFIG2, DEF_SPI_I2C-GPIO, EN_LS0, EN_LS1, EN1 (DCDC1_SEL), EN2 (DCDC2_SEL), EN3 (DCDC3_SEL), EN4 (DCDC4_SEL), SLEEP (PWR_REQ), CPCAP_WDI, VCON_CLK, CLK_REQ1, CLK_REQ2	1.1	3.3	
		For SDA, SCL, SDA_AVS, SCL_AVS	0.7 × VDDIO	VDDIO	
		For MOSI	1.1	VDDIO	
V_{OL}	Low-Level Output Voltage	I_{OL}= 1 mA; except SDA, SCL, SDA_AVS, SCL_AVS	0	0.2	V
		I_{OL}= 3 mA; for SDA, SCL, SDA_AVS, SCL_AVS; for VDDIO = 1.8 V	0	0.2 × VDDIO	
		I_{OL}= 3 mA; for SDA, SCL, SDA_AVS, SCL_AVS; for 2 V < VDDIO ≤ 3.6 V	0	0.4	
V_{OH}	High-Level Output Voltage	For pins configured as push-pull output to VDDIO; I_{OH}= 1 mA	VDDIO – 0.2	VDDIO	V
		For pins configured as open-drain output		V_{CC}	
I_{OL}	Low-Level Output Current	Except SCL, SDA, AVS_SCL, AVS_SDA		1	mA
		For SCL, SDA, AVS_SCL, AVS_SDA		5	
I_{OH}	High-Level Output Current			1	mA
I_{LKG}	Input-Leakage Current	Input pins tied to V_{IL}or V_{IH}		0.5	µA

5.9 Electrical Characteristics – VMON Voltage Monitor, VDDIO, Undervoltage Lockout (UVLO), and LDOAO

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VMON	Voltage monitor threshold for VMON_SEL[1,0] = 00; rising voltage	–2%	3.1	+2%	V
	Voltage monitor threshold for VMON_SEL[1,0] = 01; rising voltage	–2%	2.9	+2%	V
	Voltage monitor threshold for VMON_SEL[1,0] = 10; rising voltage	–2%	2.8	+2%	V
	Voltage monitor threshold for VMON_SEL[1,0] = 11; rising voltage	–2%	2.7	+2%	V
VMON hysteresis	For falling voltage		250		mV
VDDIO voltage range	Voltage applied to VDDIO pin to set the high level voltage of push-pull output stages	1.63		3.6	V
VDDIO undervoltage lockout threshold		1.4		1.625	V
UVLO	Internal undervoltage lockout threshold (supply voltage rising)		2.5		V
	Internal UVLO threshold hysteresis		200		mV
VLDOAO	Output voltage for LDOAO (LDO always on)		2.5		V

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5.10 Electrical Characteristics – Load Switch

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage between LSI and LSO				5.5	V
LSI input current limit	ILIM[1,0] = **00**; V(LSI) = 2.7 V to 5.5 V	75	90	115	mA
	ILIM[1,0] = **00**; V(LSI) = 4.5 V to 5.5 V; T_A = –10°C to + 85°C	85	90	100	mA
	ILIM[1,0] = **01**; V(LSI) = 2.7 V to 5.5 V	450	485	520	mA
	ILIM[1,0] = **01**; V(LSI) = 4.5 V to 5.5 V; T_A = –10°C to + 85°C	460	485	500	mA
	ILIM[1,0] = **10**; V(LSI) = 2.7 V to 5.5 V	720	820	920	mA
	ILIM[1,0] = **10**; V(LSI) = 2.7 V to 5.5 V; T_A = –10°C to + 85°C	750	820	900	mA
	ILIM[1,0] = **11;** V(LSI) = 2.7 V to 5.5 V; not tested in production	2000	2500	3000	mA
Current limit response time			10		µs
Resistance from LSI to LSO	When switch closed and operated as load switch with ILIM[1,0] = 11		20	40	mΩ
Resistance from LSI to LSO	When switch closed and operated as load switch with ILIM[1,0] = 00 or 01 or 10			200	mΩ
Leakage current from LSI to LSO	When load switch is open			20	µA
Load switch over-voltage protection on the output (sensed at VDCDC4)	For EN_LS[1,0]= 10 or 11, when load switch is used as BYPASS switch		4.18		V

5.11 Electrical Characteristics – LED Drivers

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{SINK(LEDx)}$	LEDx output sink current	V(LEDA) = V(LEDB) = V(LEDC) = 0.25 V	2		20	mA
	Accuracy	Absolute accuracy	–8%		9.5%	
$V_{LO(LEDx)}$	Low level output voltage	Output low voltage at LEDx pins, 20 mA			0.25	V
$I_{LKG(LEDx)}$	Output off leakage current	Output voltage = 5 V, driver set to OFF			1	µA

5.12 Electrical Characteristics – Thermal Monitoring and Shutdown

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Hot-Die Temperature rising threshold	THERM_HDSEL[1:0]=00	113	117	136	°C
	THERM_HDSEL[1:0]=01	113	121		
	THERM_HDSEL[1:0]=10	113	125		
	THERM_HDSEL[1:0]=11	113	130	136	
Hot-Die Temperature hysteresis			10		°C
Thermal Shutdown temperature rising threshold		136	148	160	°C
Thermal Shutdown temperature hysteresis			10		°C
Ground current	Device in ACTIVE state, Temp = 27 °C, V_{CCS} = 3.8 V		6		µA

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5.13 Electrical Characteristics – 32-kHz RC Clock

T_A = –40°C to +85°C, typical values are at T_A = +25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CLK32KOUT rise and fall time	C_L = 35 pF			10	ns
Output-frequency low level output voltage	CK32KOUT output		32		kHz
Output-frequency accuracy	at 25°C	–20%	0%	+15%	
Output duty cycle		40%	50%	60%	
Settling time				150	µs

5.14 SPI Interface Timing Requirements

		MIN	MAX	UNIT
t_{cesu}	Chip select set up time	30		ns
t_{cehld}	Chip select hold time	30		ns
t_{ckper}	Clock cycle time	65		ns
t_{ckhigh}	Clock high typical pulse duration	20		ns
t_{cklow}	Clock low typical pulse duration	20		ns
t_{sisu}	Input data set up time, before clock active edge	5		ns
t_{sihld}	Input data hold time, after clock active edge	5		ns
t_{dr}	Data retention time		15	ns
t_{CE}	Time from CE going low to CE going high	65		ns
	Capacitive load on pin GPIO1_MISO		30	pF

5.15 I^2C Interface Timing Requirements(1)

			MIN	MAX	UNIT
$f_{(SCL)}$	SCL Clock Frequency	Standard mode		100	kHz
		Fast mode		400	kHz
		High-speed mode (write operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (read operation), C_B – 100 pF max		3.4	MHz
		High-speed mode (write operation), C_B – 400 pF max		1.7	MHz
		High-speed mode (read operation), C_B – 400 pF max		1.7	MHz
t_{BUF}	Bus Free Time Between a STOP and START Condition	Standard mode	4.7		µs
		Fast mode	1.3		µs
t_{HD}, t_{STA}	Hold Time (Repeated) START Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{LOW}	LOW Period of the SCL Clock	Standard mode	4.7		µs
		Fast mode	1.3		µs
		High-speed mode, C_B – 100 pF max	160		ns
		High-speed mode, C_B – 400 pF max	320		ns
t_{HIGH}	HIGH Period of the SCL Clock	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode, C_B – 100 pF max	60		ns
		High-speed mode, C_B – 400 pF max	120		ns

(1) Specified by design. Not tested in production.

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I²C Interface Timing Requirements[1] *(continued)*

			MIN	MAX	UNIT
t_{SU}, t_{STA}	Setup Time for a Repeated START Condition	Standard mode	4.7		µs
		Fast mode	600		ns
		High-speed mode	160		ns
t_{SU}, t_{DAT}	Data Setup Time	Standard mode	250		ns
		Fast mode	100		ns
		High-speed mode	10		ns
t_{HD}, t_{DAT}	Data Hold Time	Standard mode	0	3.45	µs
		Fast mode	0	0.9	µs
		High-speed mode, C_B – 100 pF max	0	70	ns
		High-speed mode, C_B – 400 pF max	0	150	ns
t_{RCL}	Rise Time of SCL Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RCL1}	Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge BIT	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FCL}	Fall Time of SCL Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	40	ns
		High-speed mode, C_B – 400 pF max	20	80	ns
t_{RDA}	Rise Time of SDA Signal	Standard mode	20 + 0.1 C_B	1000	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{FDA}	Fall Time of SDA Signal	Standard mode	20 + 0.1 C_B	300	ns
		Fast mode	20 + 0.1 C_B	300	ns
		High-speed mode, C_B – 100 pF max	10	80	ns
		High-speed mode, C_B – 400 pF max	20	160	ns
t_{SU}, t_{STO}	Setup Time for STOP Condition	Standard mode	4		µs
		Fast mode	600		ns
		High-speed mode	160		ns
C_B	Capacitive Load for SDA and SCL			400	pF

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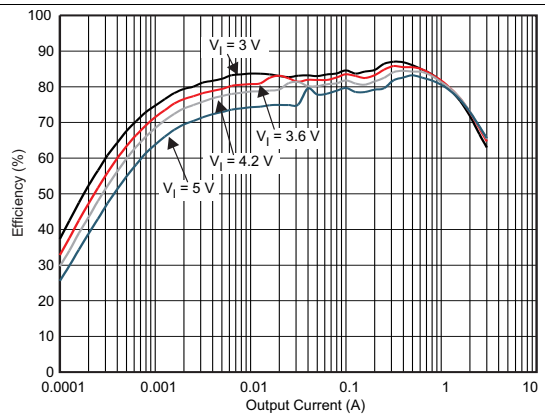
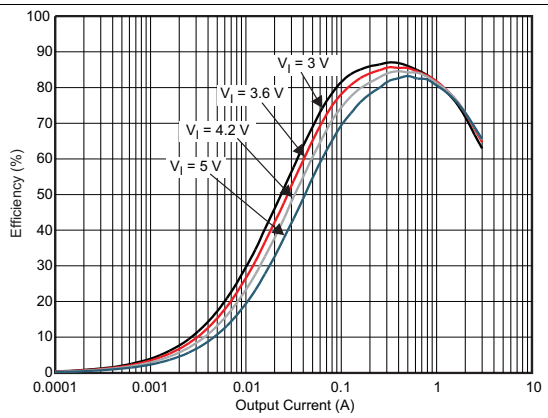
5.16 Typical Characteristics



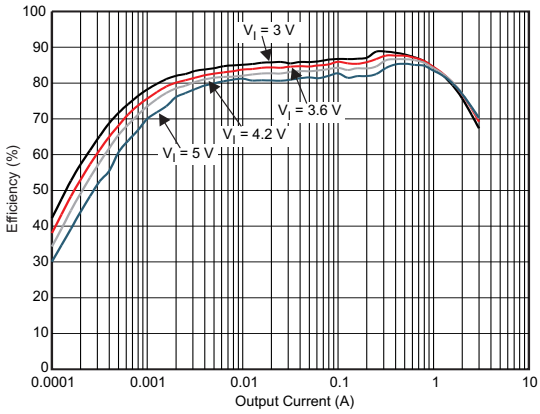
DCDC1 V_O = 0.9 V PFM Mode
DFE252012 25°C

Figure 5-1. DCDC1 Efficiency vs Output Current / PFM Mode



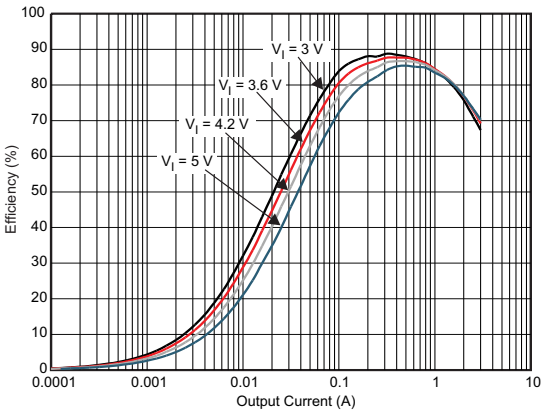
DCDC1 V_O = 0.9 V PFM Mode
DFE252012 25°C

Figure 5-2. DCDC1 Efficiency vs Output Current / PWM Mode



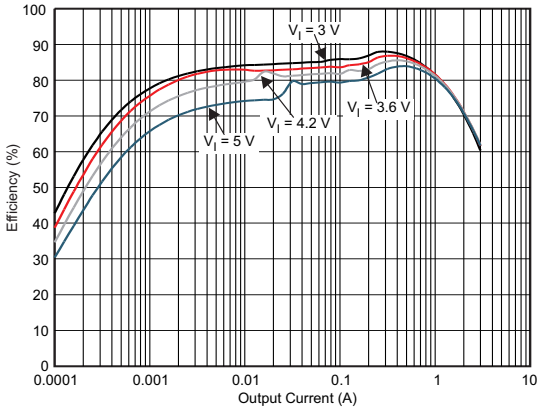
DCDC1 V_O = 1.1375 V PFM Mode
DFE252012 25°C

Figure 5-3. DCDC1 Efficiency vs Output Current / PFM Mode



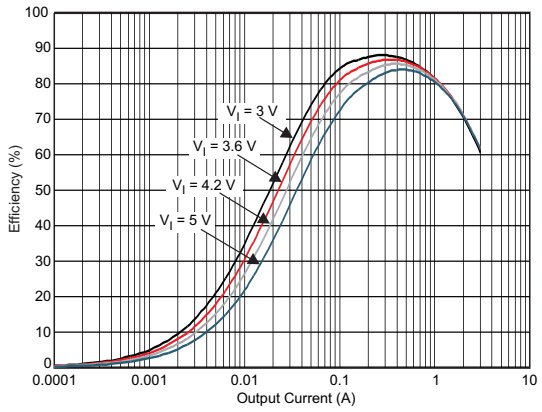
DCDC1 V_O = 1.1375 V PFM Mode
DFE252012 25°C

Figure 5-4. DCDC1 Efficiency vs Output Current / PWM Mode



DCDC1 V_O = 1.2 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-5. DCDC1 Efficiency vs Output Current / PFM Mode



DCDC1 V_O = 1.2 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-6. DCDC1 Efficiency vs Output Current / PWM Mode

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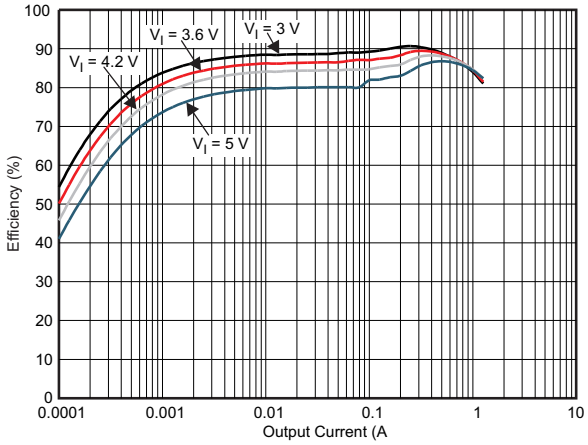
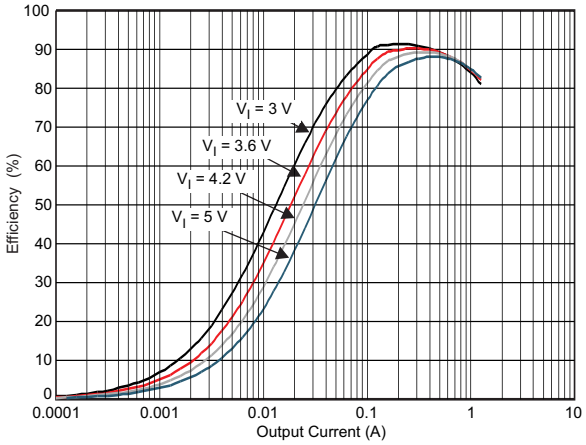
Typical Characteristics *(continued)*



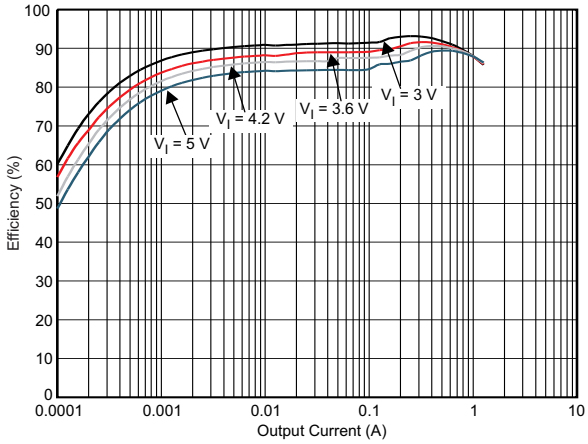
DCDC2 V_O = 1.8 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-7. DCDC2 Efficiency vs Output Current / PFM Mode



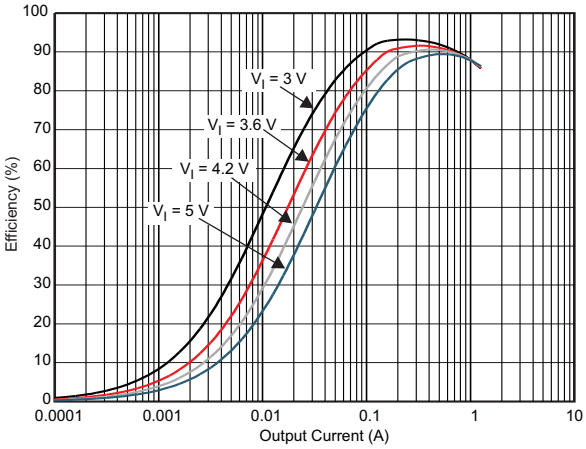
DCDC2 V_O = 1.8 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-8. DCDC2 Efficiency vs Output Current / PWM Mode



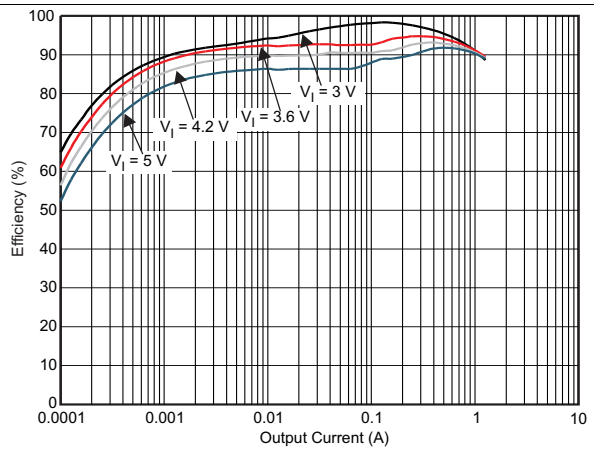
DCDC2 V_O = 2.25 V PFM Mode
VLS201612-1 µH 25°C

Figure 5-9. DCDC2 Efficiency vs Output Current / PFM Mode



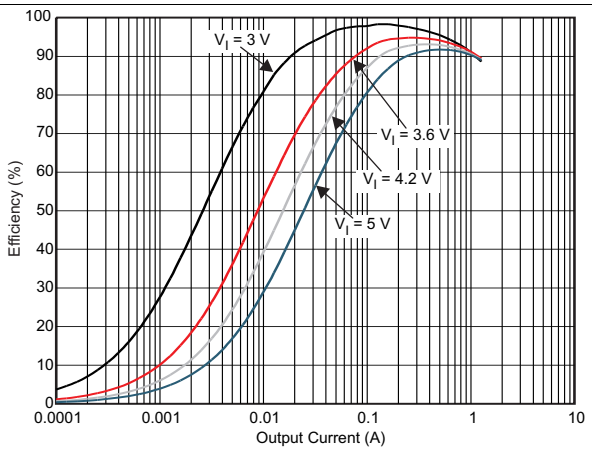
DCDC2 V_O = 2.25 V PFM Mode
VLS201612-1 µH 25°C

Figure 5-10. DCDC2 Efficiency vs Output Current / PFM Mode



DCDC2 V_O = 2.95 V PFM Mode
VLS201612-1 µH 25°C

Figure 5-11. DCDC2 Efficiency vs Output Current / PFM Mode



DCDC2 V_O = 2.95 V PFM Mode
VLS201612-1 µH 25°C

Figure 5-12. DCDC2 Efficiency vs Output Current / PWM Mode

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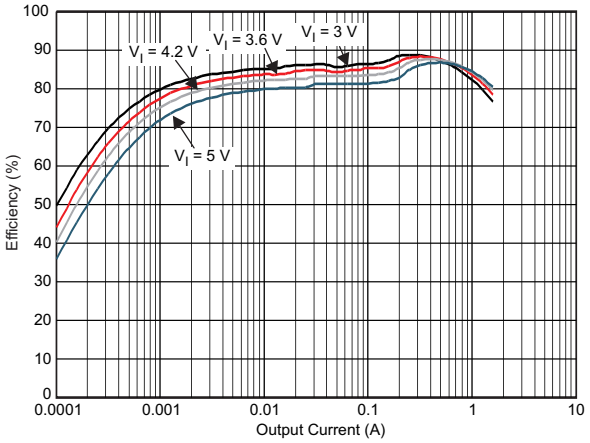
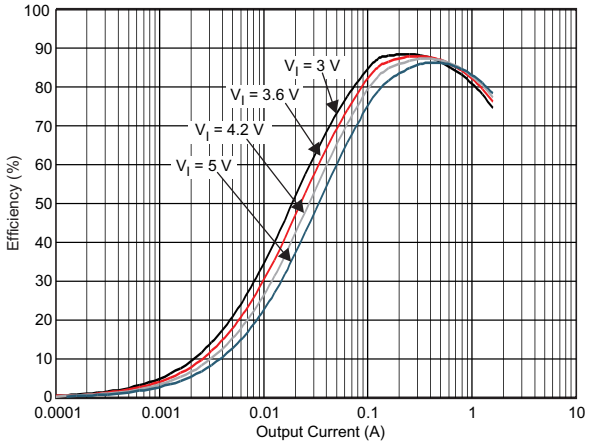
Typical Characteristics *(continued)*



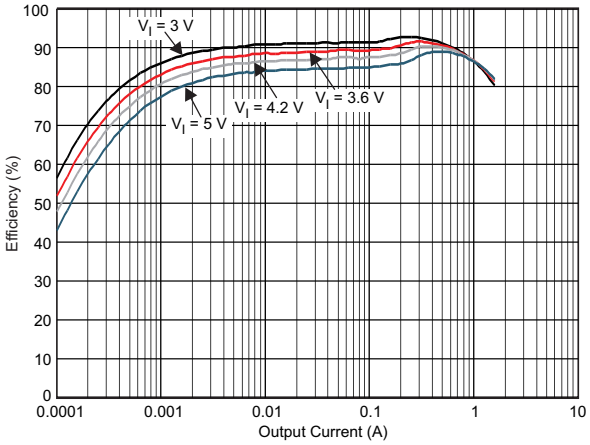
DCDC3 V_O = 1.1375 V PFM Mode
DEF252012-1 µH 25°C

Figure 5-13. DCDC3 Efficiency vs Output Current / PFM Mode



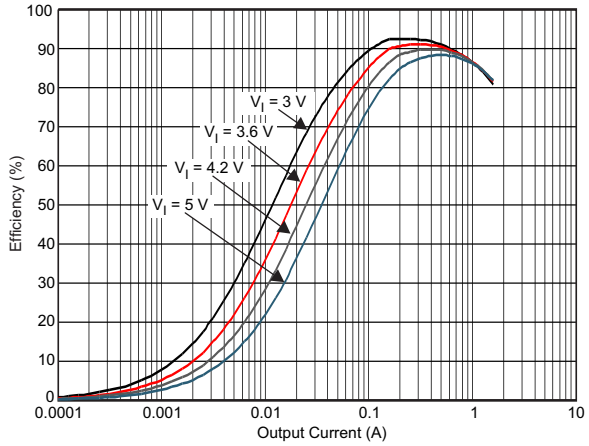
DCDC3 V_O = 1.1375 V PFM Mode
DEF252012-1 µH 25°C

Figure 5-14. DCDC3 Efficiency vs Output Current / PWM Mode



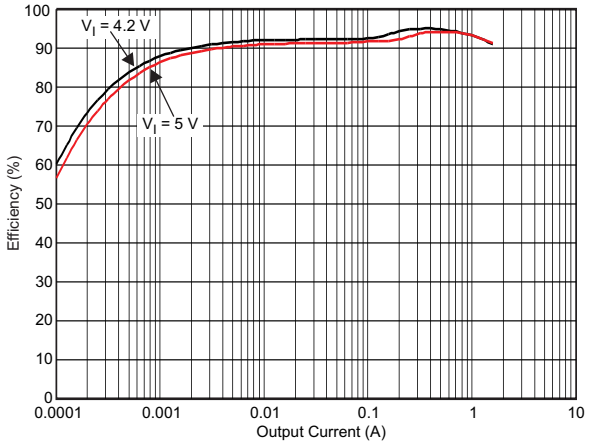
DCDC3 V_O = 2.1 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-15. DCDC3 Efficiency vs Output Current / PFM Mode



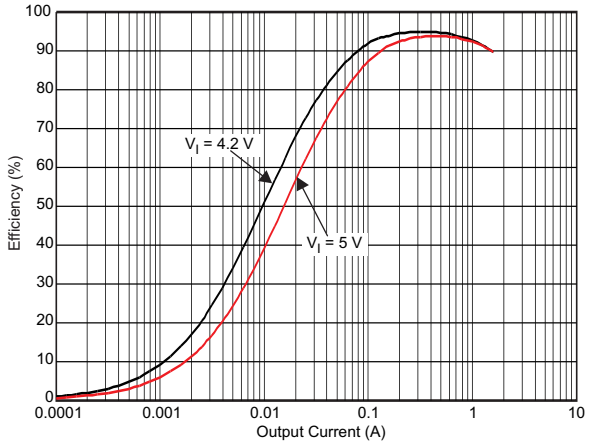
DCDC3 V_O = 2.1 V PFM Mode
LQM2NPN-1 µH 25°C

Figure 5-16. DCDC3 Efficiency vs Output Current / PWM Mode



DCDC3 V_O = 3.2 V PFM Mode
DEF25012-1 µH 25°C

Figure 5-17. DCDC3 Efficiency vs Output Current / PFM Mode



DCDC3 V_O = 3.2 V PFM Mode
DEF25012-1 µH 25°C

Figure 5-18. DCDC3 Efficiency vs Output Current / PWM Mode

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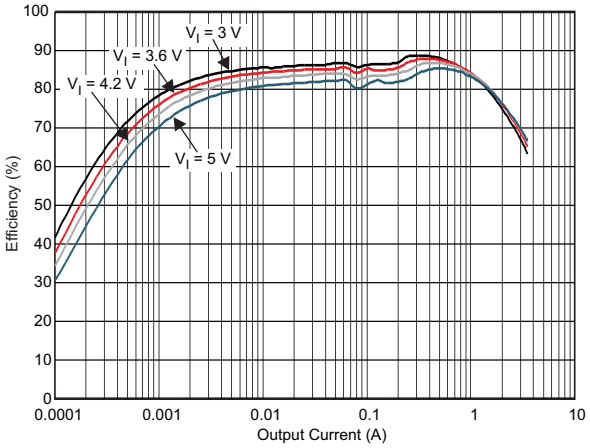
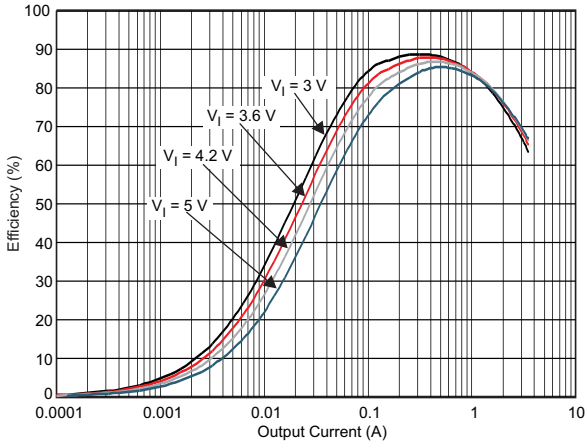
Typical Characteristics *(continued)*



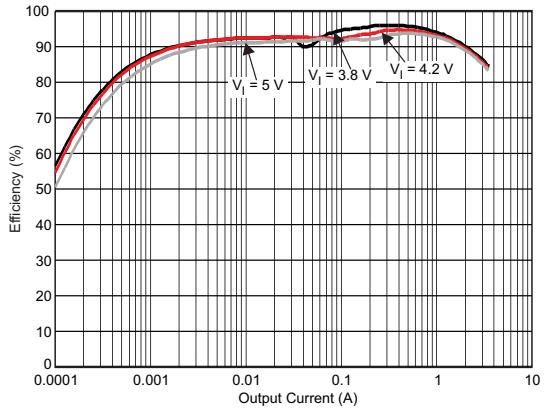
DCDC4 V_O = 1.1375 V PFM Mode
DEF25012-1 µH 25°C

Figure 5-19. DCDC4 Efficiency vs Output Current / PFM Mode



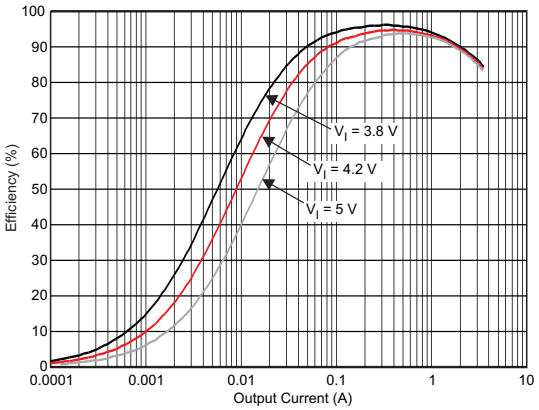
DCDC4 V_O = 1.1375 V PFM Mode
DEF322512-1 µH 25°C

Figure 5-20. DCDC4 Efficiency vs Output Current / PWM Mode



DCDC4 V_O = 3.3 V PFM Mode
DEF322512-1 µH 25°C

Figure 5-21. DCDC4 Efficiency vs Output Current / PFM Mode



DCDC4 V_O = 3.3 V PWM Mode
DEF322512-1 µH 25°C

Figure 5-22. DCDC4 Efficiency vs Output Current / PWM Mode

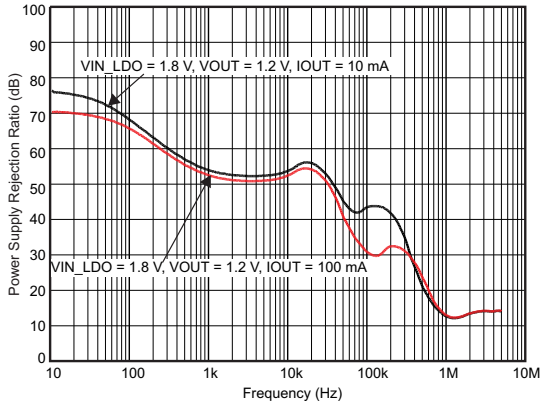
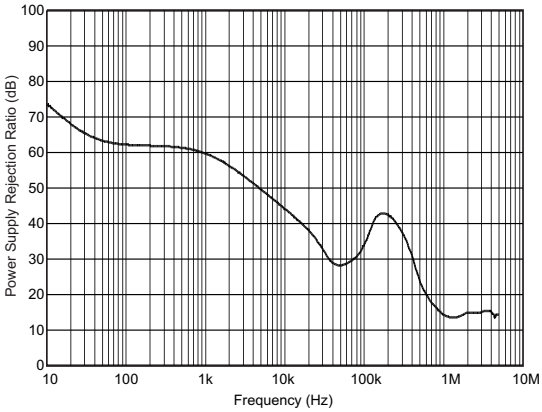


Figure 5-23. LDO1, LDO2, LDO3 PSRR vs Frequency



VIN _LDO = 3.2 V VOUT = 2.7 V
IOUT = 225 mA

Figure 5-24. LDO4 and LDO5 PSRR vs Frequency

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Typical Characteristics *(continued)*

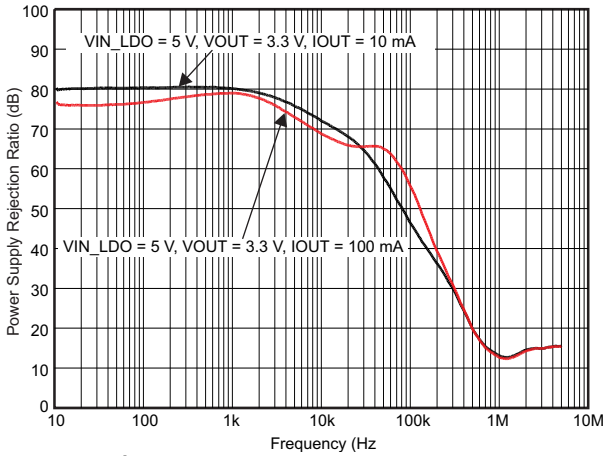


Figure 5-25. LDO4 PSRR vs Frequency

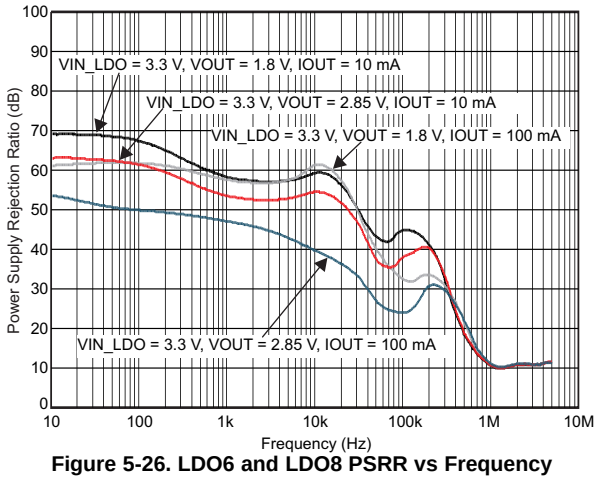


Figure 5-26. LDO6 and LDO8 PSRR vs Frequency

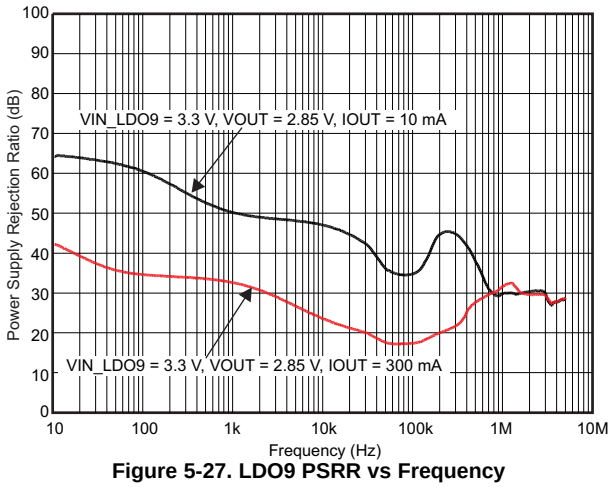


Figure 5-27. LDO9 PSRR vs Frequency

6 Parameter Measurement Information

6.1 I²C Timing Diagrams

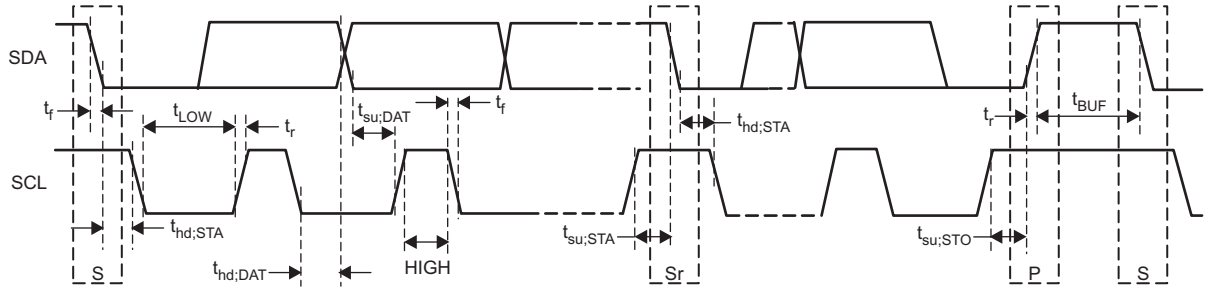
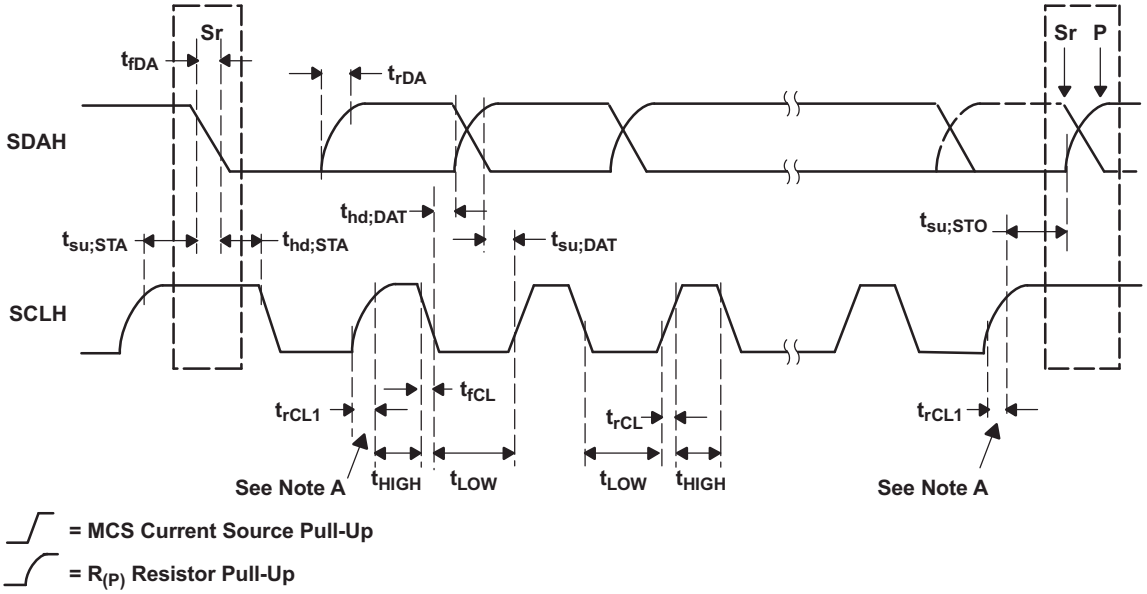


Figure 6-1. Serial Interface Timing Diagram for FS-Mode



A. First rising edge of the SCLH signal after Sr and after each acknowledge bit.

Figure 6-2. Serial Interface Timing Diagram for HS-Mode

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6.2 SPI Timing Diagram

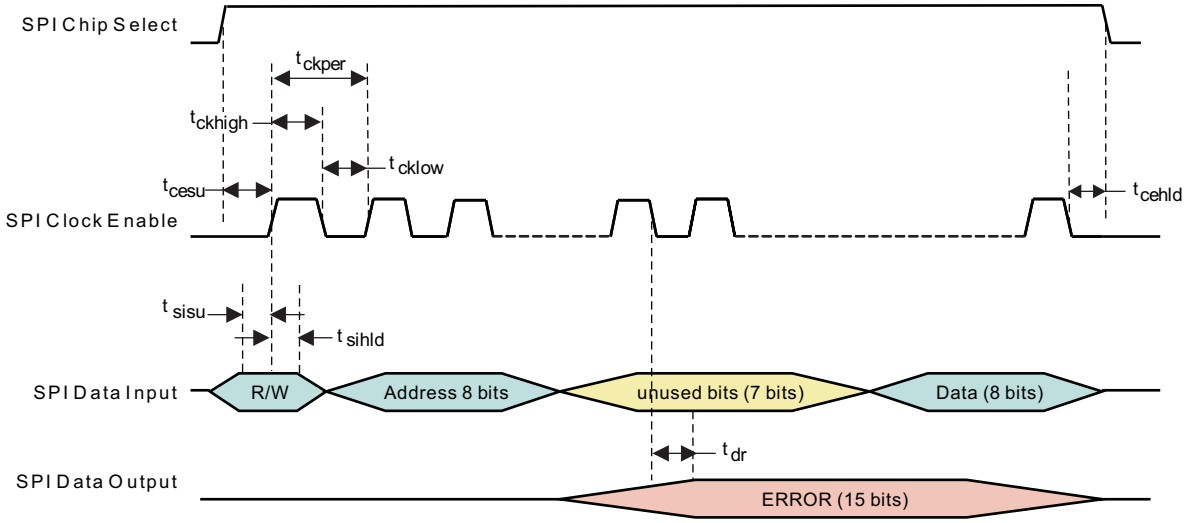

Figure 6-3. SPI Interface Timing

7 Detailed Description

7.1 Overview

The TPS65912x device is an integrated power-management integrated circuit (PMIC), available in an 81-pin, 0.4-mm pitch, 3.6-mm × 3.6-mm DSBGA package. It is designed for applications including data cards, smart phones, wireless routers and switchers, LTE modems, industrial applications, GPS, and tablets. It provides four configurable step-down converter rails, with a power save mode for light loads. The TPS65912x device also provides ten external LDO rails - eight general purpose LDOs and two low-noise RF-LDOs. It also comes with two I2C interface channels or one SPI interface channel, 5 GPIOs, 32-kHz RC oscillator, and programmable power sequencer and control for supporting different processors and applications. The four step-down converter rails are consisting of four high frequency switch mode converters with integrated FETs. They are capable of synchronizing to an external clock input and supports switching frequency between 2.8 MHz and 3.5 MHz. The DCDC4 rail also includes a bypass switch that can be used to turn on and off high current loads. In addition, the DCDC rails support dynamic voltage scaling with a dedicated I2C interface. The eight general LDOs support 0.8 V to 3.3 V output, while the two low-noise LDOs support 1.6 V to 3.3 V. All LDOs and step-down converters can be controlled by the SPI or I2C interface. The power-up and power-down controller is configurable and programmable through OTP. The TPS65912x device includes a 32-kHz RC oscillator to sequence all resources during power up and power down. Configurable GPIOs with multiplexed feature are available on the TPS65912x device. The GPIOs can be configured and used as enable signals for external resources, which can be included into the power-up and power-down sequence. The general-purpose (GP) sigma-delta analog-to-digital converter (ADC) with two external input channels included in this device can be used as thermal or voltage and current monitors. Lastly, there is a long button-press detection that allows startup of the device with the hold of a button.

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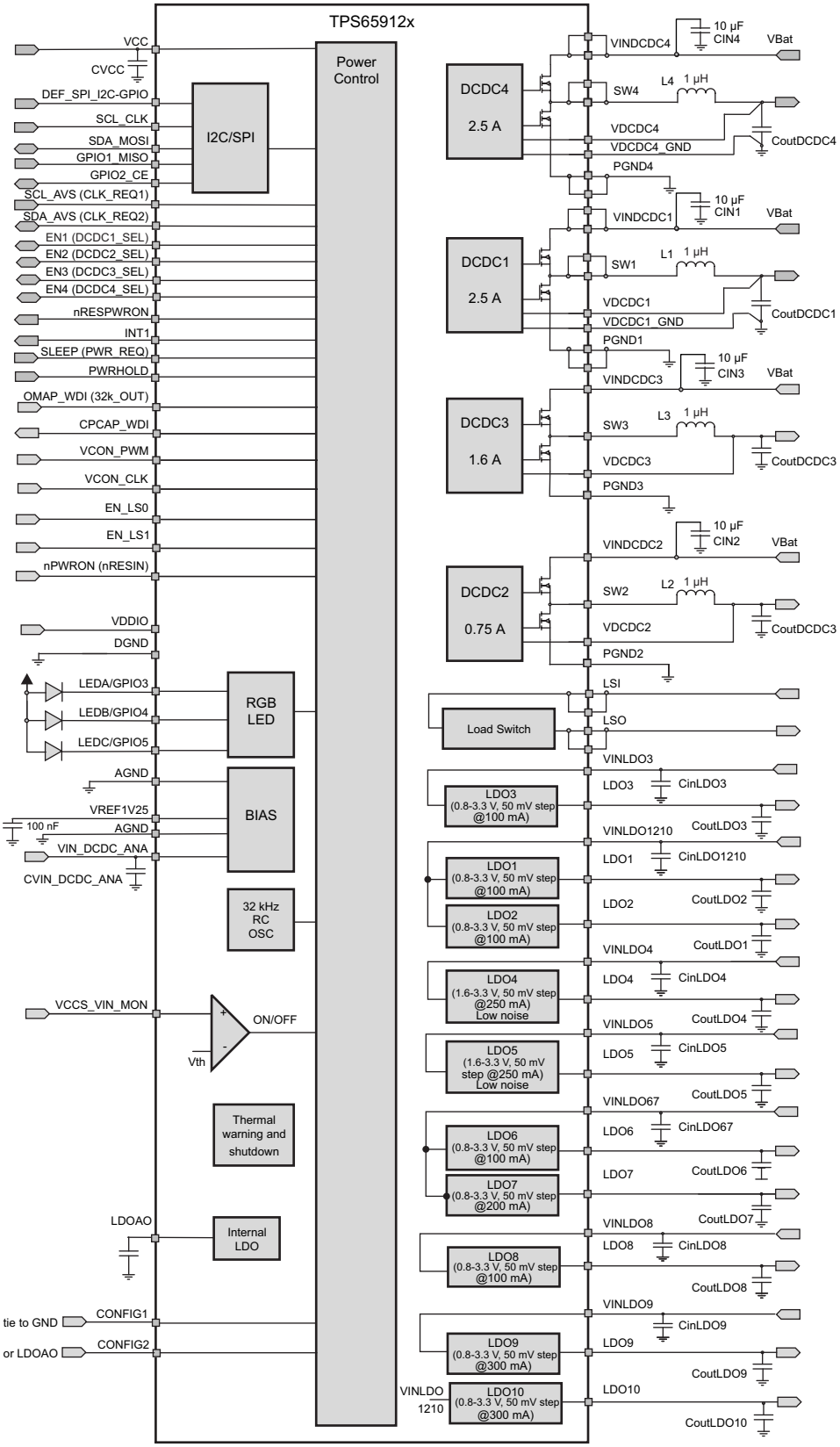
7.2 Functional Block Diagram



7.3 Linear Regulators

The power management core has 10 LDOs with various output voltage/current capabilities. Each LDO output voltage can be set independently through the communication bus (see *LDO Voltage Settings* table in *Section 7.28.2*) and the transition occurs immediately if the LDO is enabled.

7.3.1 Low Quiescent Current Mode (Eco-mode™)

Each LDO is equipped with a low quiescent current mode that can enabled or disabled separately. When the ECO bit is 1, the LDOx Eco-mode™ control scheme is enabled.

7.3.2 Output Discharge

Each LDO is equipped with an output discharge bit. When the bit is set to 1, the output of the LDO will be discharged to ground with the equivalent of a 300-Ω resistor. If the LDO is enabled, the discharge bit is ignored.

7.3.3 Thermal Shutdown

There is a global thermal shutdown protection for all step-down converters and LDOs. The thermal sensor will generate an early warning depending on the setting of register THRM_REG. If the temperature rises above the thermal shutdown threshold, the complete device is powered down to OFF state.

7.3.4 LDO Enable

The LDOs enable/disable is part of the flexible power-up and power-down state machine. Each LDO can be programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. Pins EN_1, EN_2, EN_3 and EN_4 as well as pins CLK_REQ1, CLK_REQ2 and PWR_REQ (SLEEP) can be mapped to any resource (LDOs, DC-DC converter, 32-kHz clock output or GPIO) to enable or disable it.

7.3.5 LDO Voltage Range

The output voltage range for the standard LDOs is 0.8 V to 3.3 V. For the RF-LDOs, LDO4 and LDO5, the output voltage range is 1.6 V to 3.3 V. The most significant bit for the voltage settings SEL[5] on LDO4 and LDO5 is ignored and is internally set to 1.

7.3.6 LDO Power Good Comparator

The output voltage of each LDO is supervised by an internal power good comparator. Its output is setting and clearing the PGOOD bits in registers PGOOD and PGOOD2. The power good bits are not valid if the LDO is enabled but the input voltage to the LDO is below 1 V.

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7.4 Step-Down Converters

The synchronous step-down converter used in the power management core includes a unique hysteric PWM controller scheme which enables switch frequencies over 3 MHz, excellent transient and AC load regulation as well as operation with tiny and cost competitive external components.

The controller topology supports forced PWM Mode as well as Power Save Mode operation. Power Save Mode operation reduces the quiescent current consumption and ensures high conversion efficiency at light loads by skipping switch pulses.

A significant advantage of this architecture compared to other hysteretic PWM controller topologies is its excellent DC and AC load regulation capability in combination with low output voltage ripple over the entire load range which makes this part well suited for audio and RF applications.

Once the output voltage falls below the threshold of the error comparator a switch pulse is initiated and the high side switch is turned on. It remains turned on until a minimum on time of T_{ONmin} expires and the output voltage trips the threshold of the error comparator or the inductor current reaches the high side switch current limit. Once the high side switch turns off, the low side switch rectifier is turned on and the inductor current ramps down until the high side switch turns on again or the inductor current reaches zero.

7.4.1 PWM/PFM Mode

In forced PWM Mode, the device avoids pulse skipping and allows easy filtering of the switch noise by external filter components. PWM mode is forced by setting bit DCDCx_MODE = 1. If this bit is not set, the DCDC outputs will switch to a low current PFM mode when there is light load and sufficient headroom between the DCDCx input and output rails.

7.4.2 Low Quiescent Current Mode

Each step-down converter may be individually controlled to enter a low quiescent current mode. This mode is entered when the ECO bit is **1**. In ECO mode, the quiescent current is reduced and the output voltage is supervised by a comparator while most part of the control is disabled to save power. ECO mode should only be enabled when a converter has less than 2 mA of load current. In addition, the ECO mode should be disabled prior to a load transient step to allow the converter to respond in a timely manner to the excess current draw. Setting the step-down converter into PWM mode by DCDCx_MODE = **1** disables ECO mode independently from the setting of bit ECO.

7.4.3 Output Voltage Monitoring

Internal power good comparators monitors the switching regulator outputs and detect when the output voltage is below 90% of the programmed value. This information is used by the power management core to generate interrupts depending on specific I^2C register settings. See the Interrupt Controller section for additional details. An individual power good comparator of the switching regulator will be blanked when the regulator is disabled or when the voltage of the regulator is transitioning from one set point to another.

7.4.4 Output Discharge

Each switching regulator is equipped with an output discharge enable bit. When the bit is set to 1, the output of the regulator will be discharged to ground with the equivalent of a 400-Ω resistor. If the enable bit of the regulator is set, the discharge bit is ignored.

7.4.5 Thermal Shutdown

There is a global thermal shutdown protection for all step-down converters and LDOs. The thermal sensor will generate an early warning depending on the setting of register THRM_REG. If the temperature rises above the thermal shutdown threshold, the complete device is powered down to OFF state.

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7.4.6 Step-Down Converter ENABLE

The step-down converter enable/disable is part of the flexible power-up and power-down state machine. Each converter can be programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. Pins EN_1, EN_2, EN_3 and EN_4 as well as pins CLK_REQ1, CLK_REQ2 and PWR_REQ (SLEEP) can be mapped to any resource (LDOs, DC-DC converter, 32 kHz clock output or GPIO) to enable or disable it.

7.4.7 Step-Down converter SOFT START

The step-down converters in TPS65912x have an internal soft-start circuit that controls the ramp up of the output voltage. The output voltage ramps up from 5% to 95% of its nominal value within a time defined in *Section 5*. This limits the inrush current in the converter during start up and prevents possible input voltage drops when a battery or high impedance power source is used. The soft-start circuit is enabled after the start-up time t_{Start} has expired. For DCDC4, there is an option to set two different values for the start up and ramp time. For applications that require a fast response, set DCDC4_CTRL:RAMP_TIME = 1.

During soft start, the output voltage ramp up is controlled as shown in Figure 7-1.

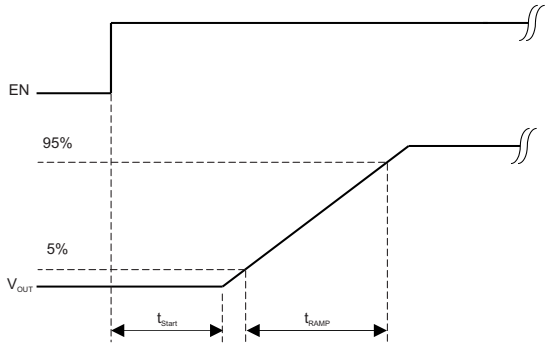

Figure 7-1. Soft Start

The step-down converter enable/disable is part of the flexible power-up and power-down state machine. Each converter can be programmed such that it is powered up automatically in one of the 15 time slots after a power-on condition occurs or is controlled by a dedicated pin. Pins EN_1, EN_2, EN_3 and EN_4 as well as pins CLK_REQ1, CLK_REQ2 and PWR_REQ (SLEEP) can be mapped to any resource (LDOs, DC-DC converter, 32 kHz clock output or GPIO) to enable or disable it.

7.5 GPIOs

There are 5 GPIOs in TPS65912x. GPIO1 and GPIO2 are shared with the SPI interface, so they are not available if SPI is used. GPIO3, GPIO4 and GPIO5 are for general purpose use and are shared with the LED driver. GPIO1 and GPIO2 input and output stages are similar to GPIO3 however, they do not contain the LED current sink. If the output stage is programmed to push-pull, it pulls to the high-voltage set by VDDIO. With VDDIO being below the VDDIO undervoltage lockout, the high-side driver is disabled and the output is set to open drain.

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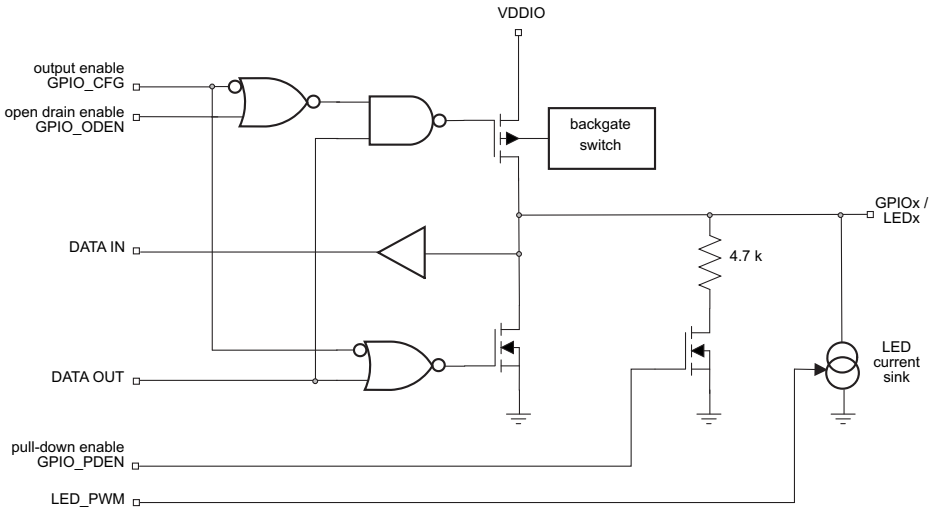

Figure 7-2. GPIO Block for GPIO3, GPIO4, and GPIO5

7.6 Power State Machine

The embedded power controller (EPC) manages the state of the device and controls the power up sequence.

The EPC will support the following states:

The transitions for the state machine are shown figure below

NO SUPPLY The main battery supply voltage is not high enough to power the LDOAO (LDO always ON) regulator. A global reset is asserted in this case. Everything on the device is off.

CONFIG This state is entered either from NO SUPPLY state automatically or from ACTIVE or SLEEP when TPS65912x is configured accordingly by Bit LOAD-OTP in [DEVCTRL:Bit6]. When CONFIG is entered, all registers are set to their default value; nRESPWRON is asserted.

OFF LDOAO is on and internal logic is active. All power supplies are in off-state. Device can detect and execute power-up sequence. nRESPWRON is asserted.

ACTIVE Device POWER ON enable conditions are met and regulated power supplies are ON or can be enabled with full current capability. Reset is released; interfaces are active.

SLEEP Device SLEEP enable conditions are met and selected regulated power supplies are in low-power/OFF mode.

7.7 Transition Conditions

- Device POWER ON enable conditions:
  - nPWRON signal low level
  - Or PWRHOLD signal high level
  - Or Pwr_hold_reg control bit set to 1 (default inactive)
  - Or interrupt flag active (default INT1 low) will generate a POWER ON enable condition during a fixed delay (During this delay it is expected processor to main acknowledge power by writing in Pwr_Hold reg or setting Power Hold pin to 1). Interrupt sources Generate wake up only if they are not Mask (OTP/Register dependant)
- Device POWER ON disable conditions:
  - nPWRON signal low level during more than the Long Press delay: PWON_LP_DELAY (can be disable though register programming). The interrupt corresponding to this condition is the PWRON_LP_IT in INT_STS_REG register.
  - Or Die temperature has reached the thermal shutdown threshold (THERM_TS=1)
  - Or DEV_OFF_RST control bit set to 1

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- Device SLEEP enable condition:
  - SLEEP signal low level (Default, or high level depending of the programmed polarity)
  - AND DEV_SLP control bit set to 1
  - AND interrupt flag inactive (default INT1 high): no none masked interrupt pending
- Device has three different reset scenarios:
  - Full reset: all digital of device is reset
    - Caused by POR (Power On Reset) when VCCS < UVLO
  - General reset:
    - Caused by turn-off event with LOAD-OTP=1
    - Turn-off event by PWON_LP_OFF_RST bit set to 1
    - Optionally for TPS65912x1 by pin PWRON pulled low for longer than 100 ms

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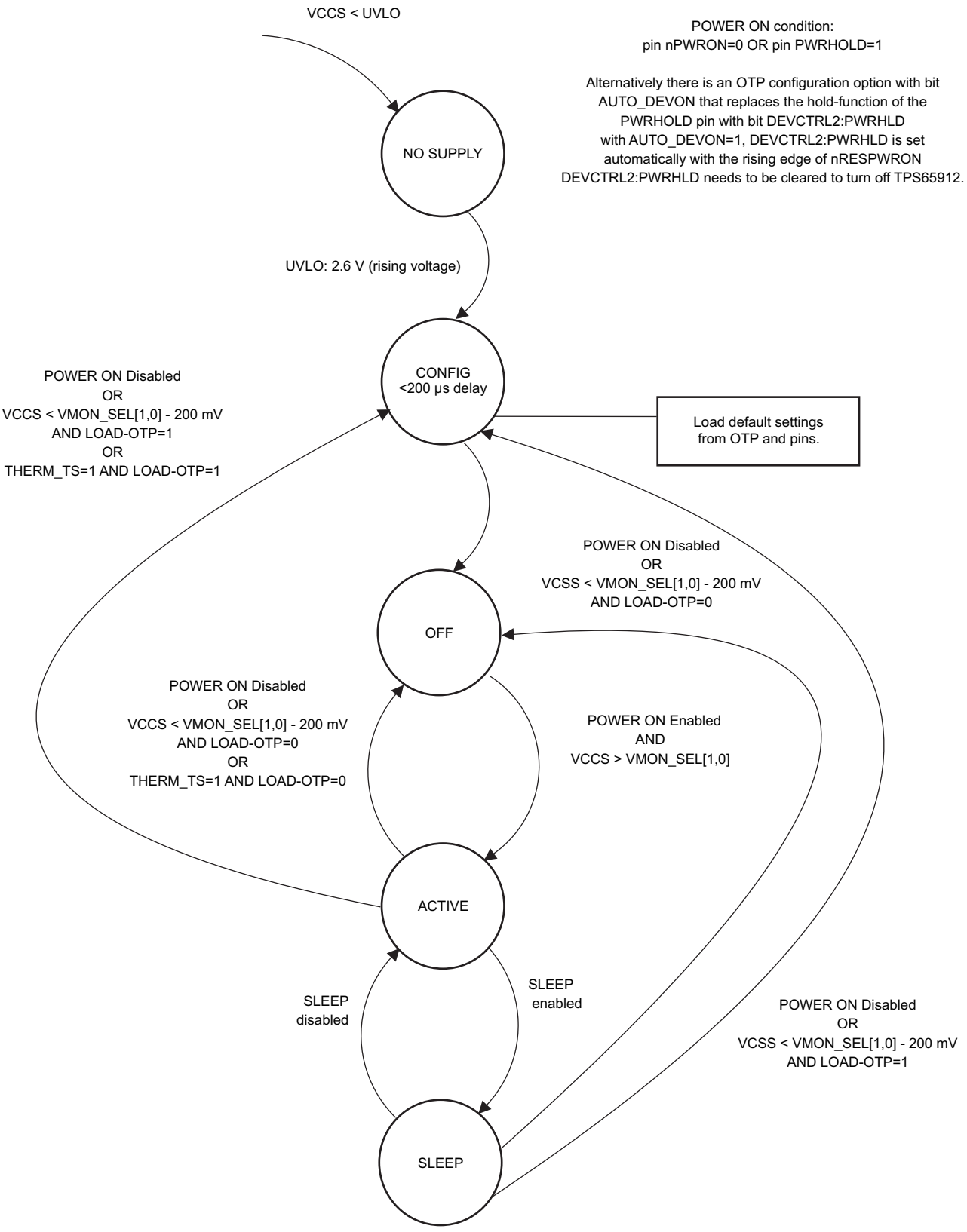

Figure 7-3. Embedded Power Control State Machine

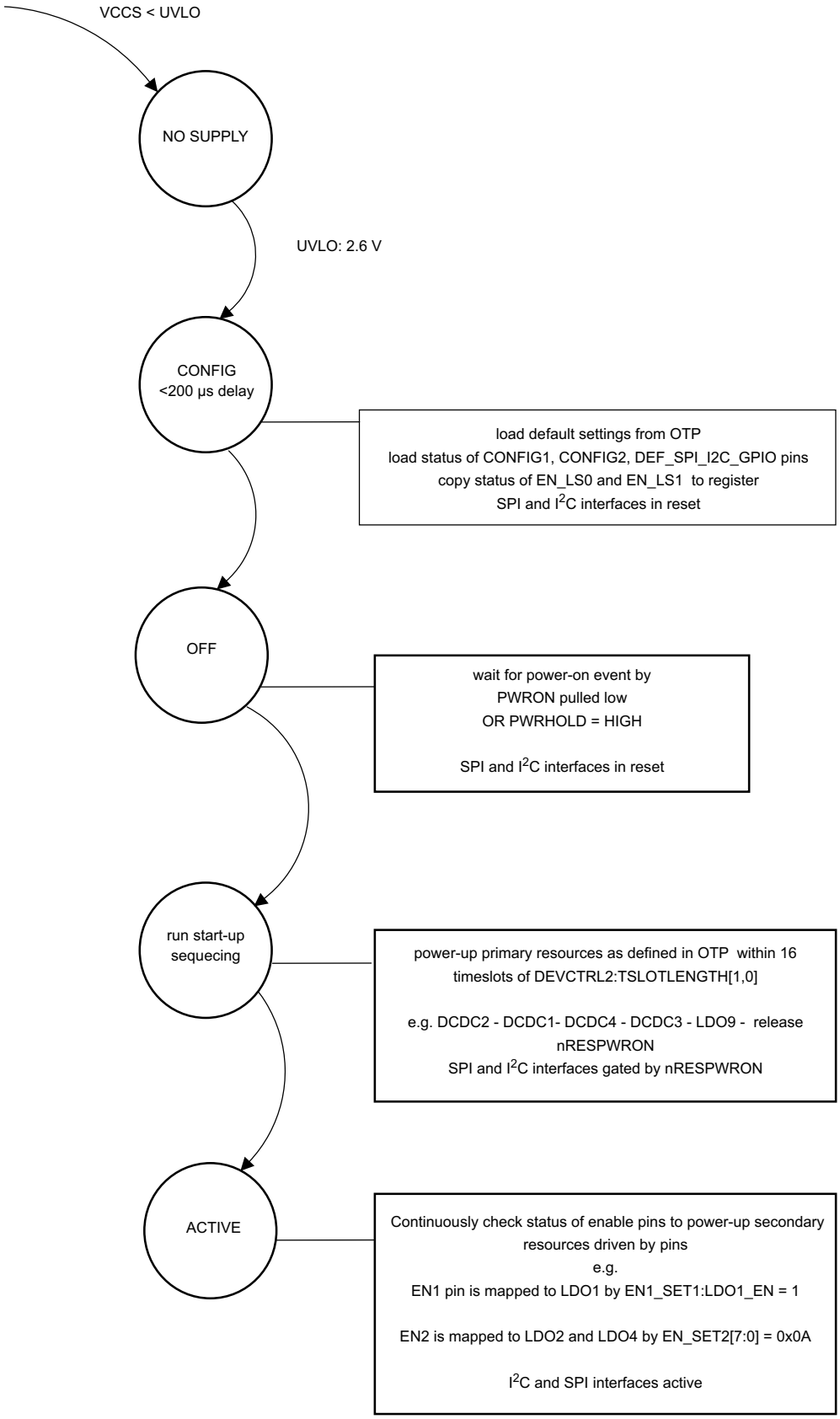

Figure 7-4. STARTUP Flow for CONFIG2=1

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Figure 7-4 is valid for CONFIG2=1. With CONFIG2=1, pins EN1, EN2, EN3 and EN4 are used as enable pins to enable one or several resources. Registers EN1_SET1 and EN1_SET2 define which converters or LDOs are controlled by pin EN1. Pins EN2, EN3, and EN4 are handled similarly.

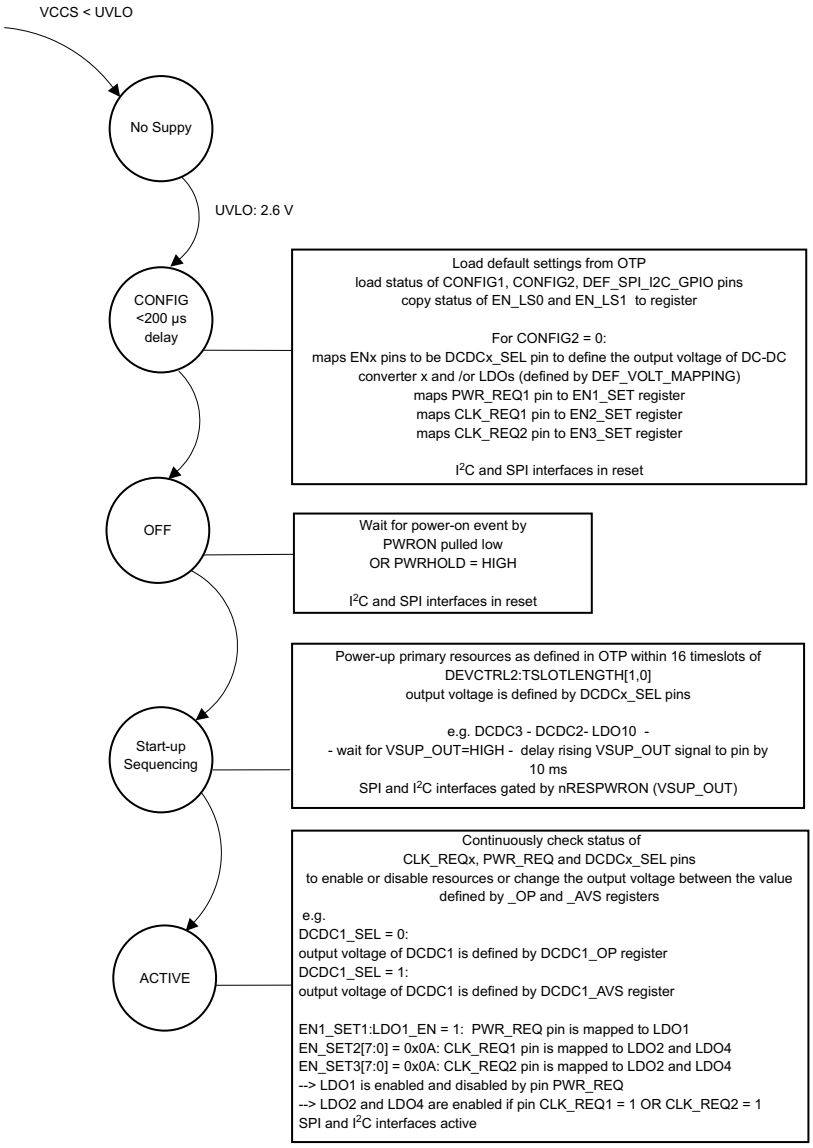

Figure 7-5. STARTUP Flow for CONFIG2=0

Figure 7-5 is valid for CONFIG2=0. With CONFIG2=0, pins EN1, EN2, EN3 and EN4 are re-mapped to be DCDCx_SEL pins, defining which register is used to set the output voltage on a specific DC-DC converter. For example, DCDC1_SEL=0 sets the output voltage of DCDC1 to what is defined by register DCDC1_OP while DCDC1_SEL=1 sets the voltage defined by DCDC1_AVS. The DCDC2 voltage is defined by DCDC2_SEL and so forth.

LDO1 to LDO4 can be mapped to DCDCx_SEL pins. Register DEF_VOLT_MAPPING defines what LDO is controlled by what DCDCx_SEL pin.

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In addition to this, CONFIG2=0 also re-maps pins SCL_AVS, SDA_AVS and SLEEP to be CLK_REQ1, CLK_REQ2 and PWR_REQ pins. The functionality is actually similar to the ENx pins.

Register EN1_SET1 and EN1_SET2 define what resource is controlled by PWR_REQ, EN2_SETx define the resource controlled by CLK_REQ1 and EN3_SETx defines the resources for CLK_REQ2.

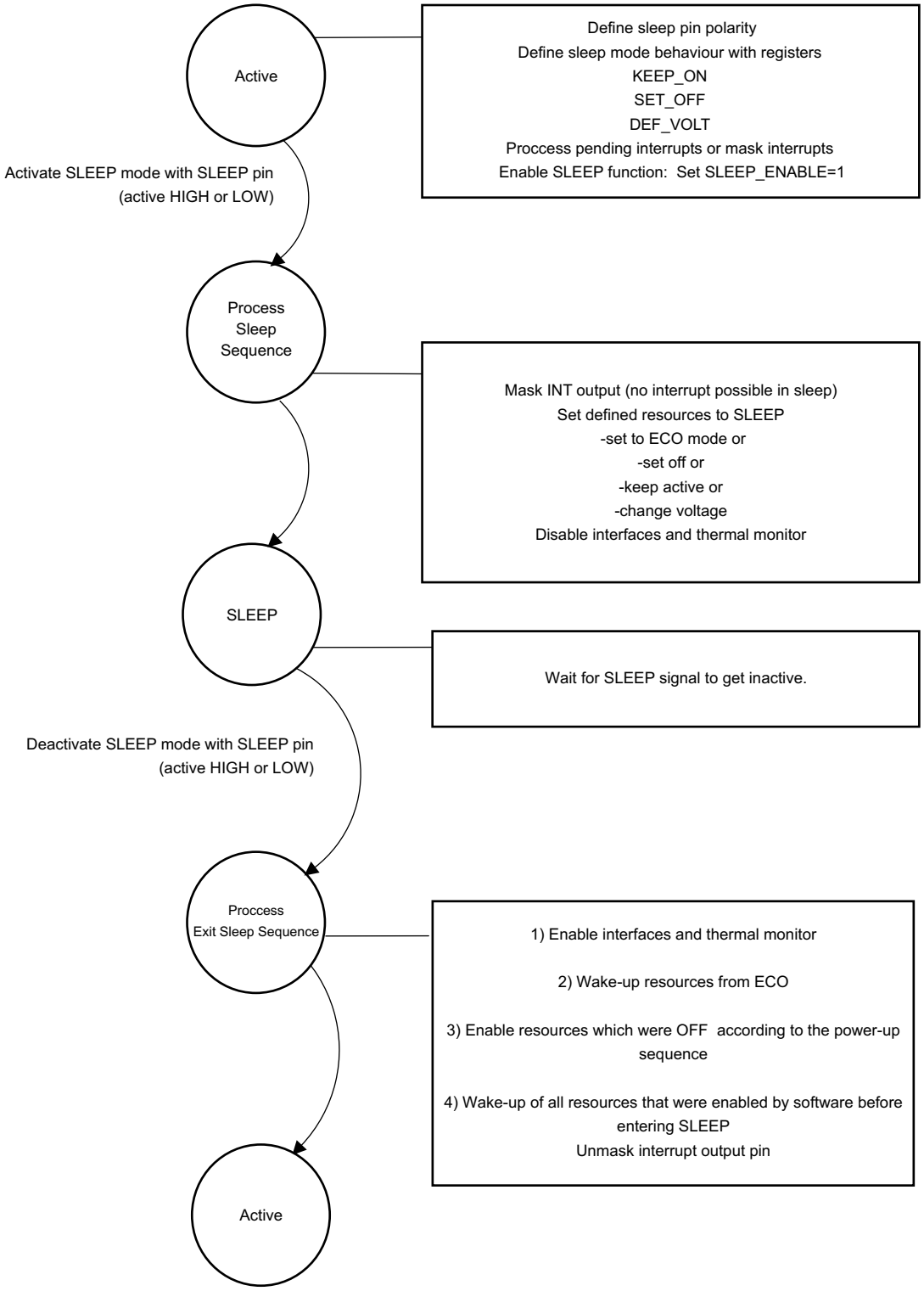

Figure 7-6. SLEEP Flow

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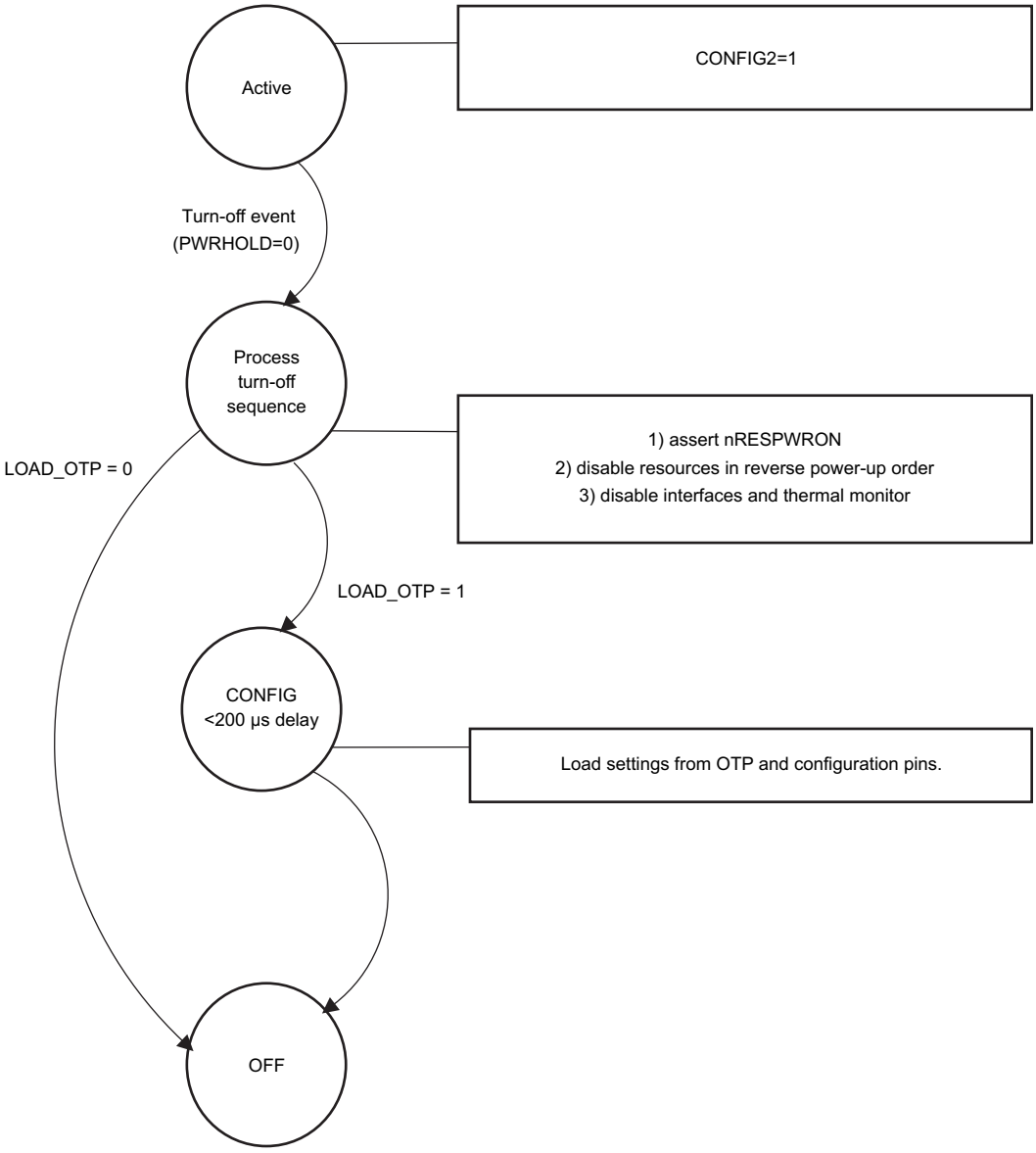

Figure 7-7. SHUTDOWN Flow for CONFIG2=1

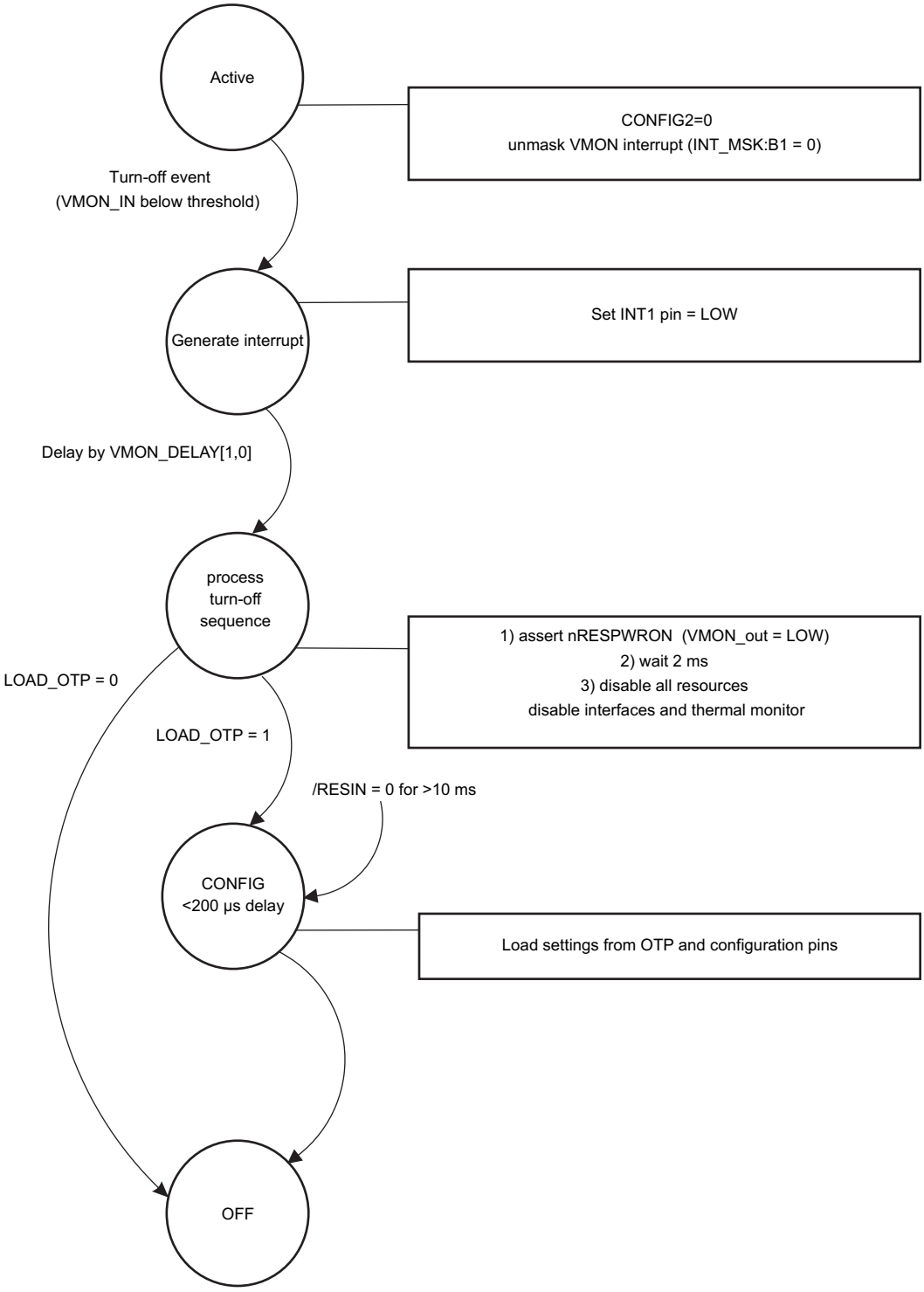

Figure 7-8. SHUTDOWN Flow for CONFIG2=0

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7.8 Implementation of Internal Power-Up and Power-Down Sequencing

The TPS65912x allows to internally enable resources during power up (going to ON state) and power down (going to OFF state) and for entering and exit of SLEEP mode. The internal power sequencing is defined in OTP memory programmed at TI. The sequencing allows to enable resources in 15 time slots during power-up and power-down. A resource can be associated to any of these 15 time slots that will be processed in the opposite direction during power down. There are 4 settings programmable for the delay, effective for all 15 time slots:

- TSLOT_LENGTH[1,0] = 00: 30 µs
- TSLOT_LENGTH[1,0] = 01: 200 µs
- TSLOT_LENGTH[1,0] = 10: 500 µs
- TSLOT_LENGTH[1,0] = 11: 2 ms

Resources may include:

- Step-down converters
- LDOs
- 32-kHz clock outputs
- nRESPWRON output

Resources that are not part of the automatic sequencing may be configured such that they are enabled by external pins or by their enable Bit in the register set. Resources that are enabled automatically should not be assigned to an external enable pin. A "break point" can be defined that stops power-up sequencing and continues upon the status of the voltage monitor. This allows to hold power-up until the voltage of the voltage monitors exceeds a certain limit.

As shown in Figure 7-9, resources can be mapped to any of the time slots with none, one or multiple resources for any time slot.

NOTE

Figure 7-9 is an example of the programmability of the sequencing and does not match the settings for TPS659120 or TPS659121 as these are shown in the sequencing diagrams already.

For SLEEP entry and SLEEP exit, only three time slots are used with a 120-µs delay between time slots.

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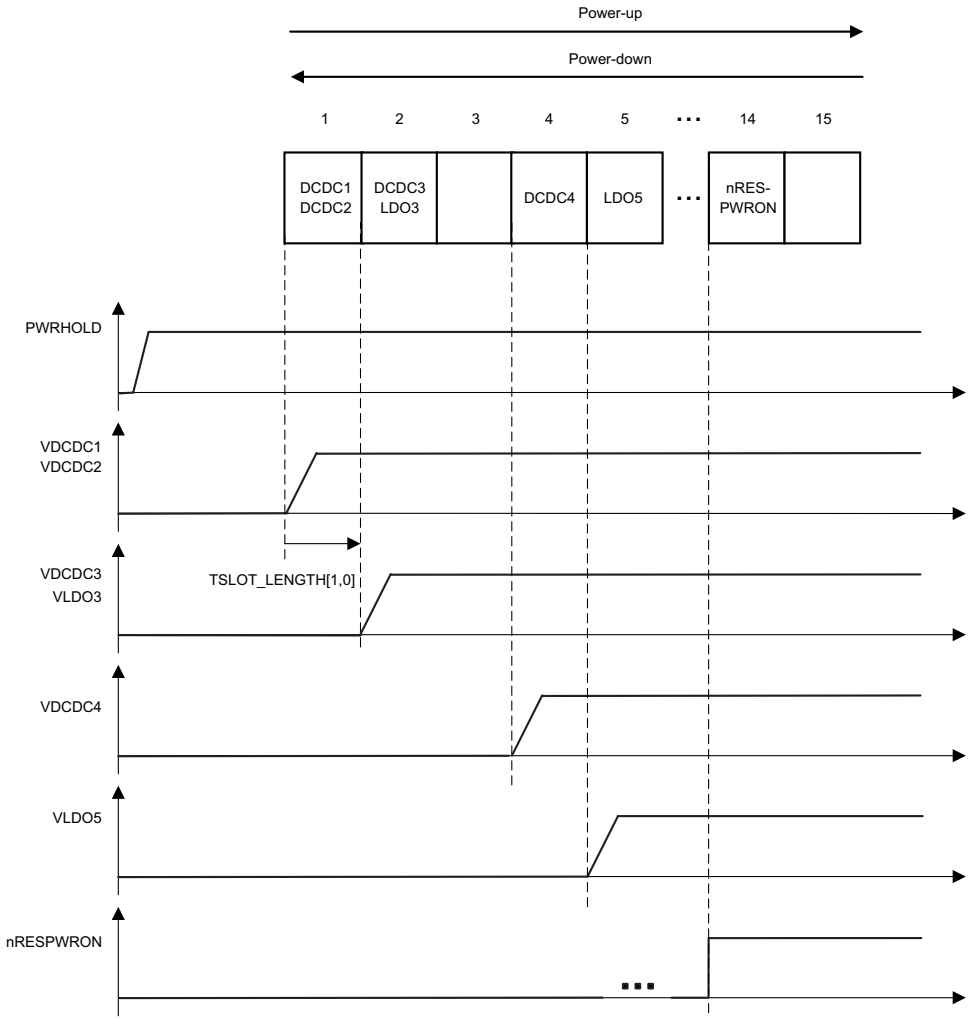

Figure 7-9. Internal Power-Up Example

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7.9 EN1, EN2, EN3, EN4, Resources Control

ENx control signal can turn ON/OFF Resources based on register setting. It is possible to assigned several resources to one ENx control signal. It is possible to assigned resource to several ENx (active control will be dominant). ENx configuration is done by OTP; however, it is possible to change this setting after power up inside ENx_SETx registers. ENx is effective only in Active or SLEEP mode. See for further details at Section 7.11 on how the pin status on ENx is interpreted.

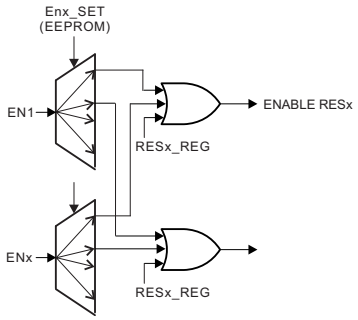

Figure 7-10. ENx Architecture

7.10 SLEEP State Control

The sleep control input on pin SLEEP is used to move the IC into Sleep state where resource behavior (DC-DC, LDOs, 32-kHz clock output, and thermal monitor) are defined in registers called SET_OFF, KEEP_ON and DEF_VOLT.

7.11 Registers SET_OFF, KEEP_ON and DEF_VOLT Used in SLEEP State; CONFIG2 = 1

Registers SET_OFF; KEEP_ON and DEF_VOLT are used to define the behavior of a resource in SLEEP state. SLEEP state is entered based on the signal at pin SLEEP if enabled by bit DEVCTRL2:SLEEP_ENABLE. The polarity of an active sleep signal can be changed using bit DEVCTRL2:SLEEP_POL.

DCDC1 to DCDC4 and LDO1 to LDO4 allow to change the output voltage depending on ACTIVE state vs SLEEP state. See the following for programming of SET_OFF, KEEP_ON and DEF_VOLT:

- Keep resource enabled in SLEEP state: SET_OFF=x , KEEP_ON=1
- Turn resource off in SLEEP state: SET_OFF=1 , KEEP_ON=0
- Set resource to ECO mode in SLEEP state: SET_OFF=0, KEEP_ON=0
- Change the output voltage of a resource when in SLEEP state:
  - DEF_VOLT=0: voltage defined by _OP register
  - DEF_VOLT=1: voltage defined by _AVS register

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7.12 Registers SET_OFF, KEEP_ON and DEF_VOLT Used for Resources Assigned to an External Enable Pin; CONFIG2 = 1

As described in Section 7.8, a resource can be assigned to an enable pin. In this case SLEEP state has no effect on such a resource but its behavior is defined by the state of the enable pin. Registers SET_OFF, KEEP_ON and DEF_VOLT are re-mapped and used to define how a resource is acting when the enable pin is set low or is set high. The definition for an high signal on ENx is similar to an ACTIVE state while a low signal on ENx equals the behavior in SLEEP state. See the following for a detailed description:

- Enable resource when ENx pin is set high: SET_OFF=x , KEEP_ON=x
- Disable resource when ENx pin is set low: SET_OFF=1 , KEEP_ON=0
- Set resource to ECO when ENx pin is set low: SET_OFF=0, KEEP_ON=0
- Change the output voltage of a resource when pin ENx is set low:
  - DEF_VOLT=0: voltage defined by _OP register
  - DEF_VOLT=1: voltage defined by _AVS register

7.13 Registers SET_OFF, KEEP_ON and DEF_VOLT for Resources Assigned to Pins PWR_REQ, CLK_REQ1 and CLK_REQ2; CONFIG2 = 0

With the CONFIG2 pin tied to GND, pins ENx are used as voltage select pins DCDCx_SEL for the DC-DC converters and for LDOs assigned to these pins by register DEF_VOLT_MAPPING. There pins are only used to switch the output voltage between two values as defined in registers _OP and _AVS.

- DCDCx_SEL=0: _OP registers are used to define the output voltage
- DCDCx_SEL=1: _AVS registers are used to define the output voltage

The basic function of enabling or disabling resources is re-mapped to pins PWR_REQ, CLK_REQ1 and CLK_REQ2. The pin function is managed by registers ENx_SETx in the following list. Register EN4_SETx is not used and should be set 0x00.

- PWR_REQ: EN1_SETx
- CLK_REQ1: EN2_SETx
- CLK_REQ2: EN3_SETx

7.14 Voltage Scaling Interface Control Using _OP and _AVS Registers with I^2C or SPI Interface

A dedicated I^2C_AVS interface is available for voltage scaling functionality. It works in three different modes.

- I^2C voltage scaling interface where voltage target can be setup in DCDCx_OP registers.
- AVSx pin called DCDCx_SEL can be used as roof or floor configuration where the DC-DC voltage switches between the value defined in the DCDCx_OP register and the DCDCx_AVS register.

The slew rate of VDDX voltage supply reaching a new programmed value is programmable though the VDDx_REG register.

Both I^2C interfaces are compliant with HS-I^2C specification (100 kbits/s, 400 kbits/s, or 3.4 Mbits/s)

CONFIG1=0: OTP option A is selected

CONFIG1=1: OTP option B is selected

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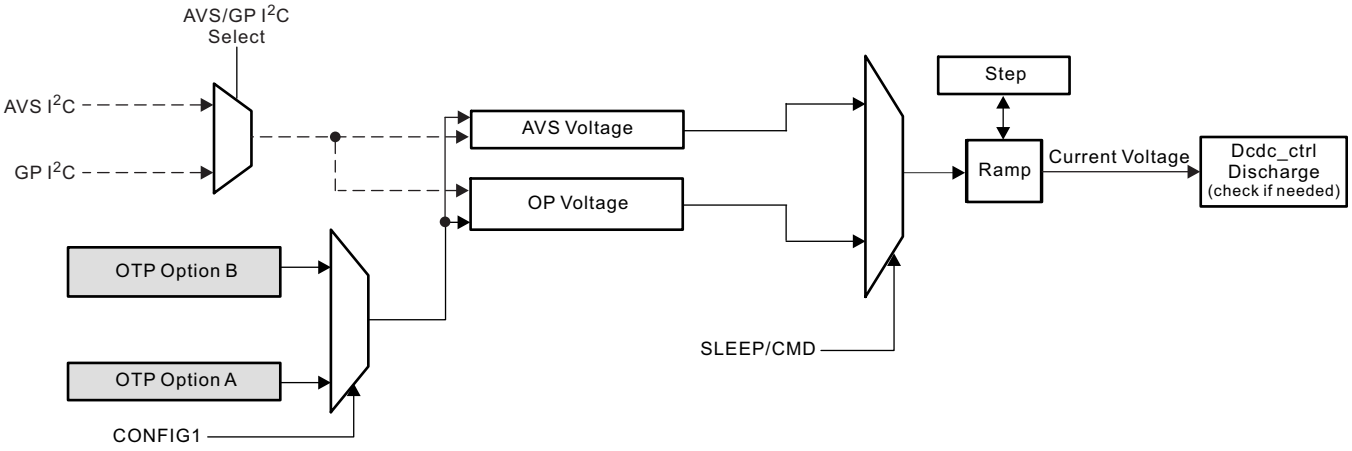

Figure 7-11. DC-DC Voltage Scaling Architecture

7.15 Voltage Scaling Using the VCON Decoder on Pins VCON_PWM and VCON_CLK

Output voltage control for DCDC1 defaults to internal registers DCDC1_OP and DCDC1_AVS or DCDC_SEL pins for CONFIG2=0. With DCDC1_CTRL:VCON_ENABLE = 1, voltage scaling is set to VCON.

When enabled, VCON decodes the VCON_PWM from VCON_CLK. It validates the generated output voltage does not exceed 1.1 V when 25-mV step size is selected. For PWM ratios 0/32 to 7/32, the output voltage will clip to 1.1 V. Four ranges can be selected by setting the VCON_RANGE[1:0] bits in register DCDC1_CTRL. The range bits towards the converters will be adjusted according to the VCON_RANGE bits.

The VCON_CLK and VCON_PWM signal need to be active and one complete frame received by TPS65912x before it is enabled with DCDC1_CTRL:VCON_ENABLE. Once DCDC1_CTRL:VCON_ENABLE is set to 0, the voltage setting is reverted back to register DCDC1_AVS or DCDC1_OP depending on the DCDC1_SEL pin. The range bits are fed through as set in the DCDC1_LIMIT register. For VCON mode, no DVS, MAX voltage comparison nor RANGE information is checked within the VCON DECODER block (but in the digital core as described in the data sheet).

For TPS659121(A) only: VCON is automatically disabled by internally clearing DCDC1_CTRL:VCON_ENABLE once the PWR_REQ pin goes LOW. It not automatically turn on but will have to be enabled in software again after PWR_REQ was set HIGH.

The function calculates the desired converter voltage based on the in incoming PWM information. The max CLK frequency is 30 MHz. The period of the PWM signal is 1/32 of VCON_CLK. The decoding follows Equation 1.

$$V_{OUT}\ (mV) = V_{RANGE}\ (mV) - D\ (int) \times (25\ mV \text{ or } 12.5\ mV) \quad (1)$$

where

- V_{OUT} is the resulting converter voltage in mV (6-bit bus)
- V_{RANGE} is the selected voltage RANGE from VCON_RANGE[1:0] bits
- D is the time VCON_PWM is high within 32 clock cycles of VCON_CLK

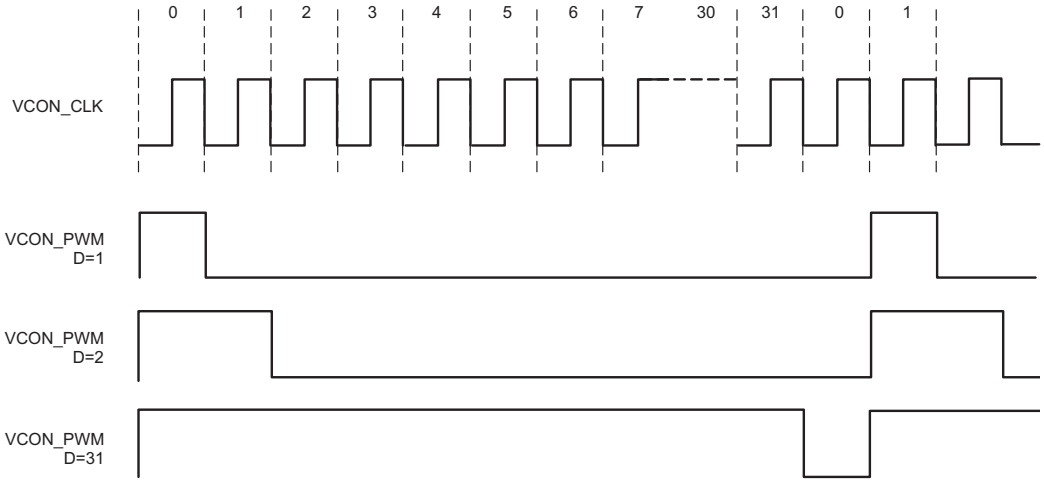

Figure 7-12. VCON Voltage Scaling Architecture

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7.16 Configuration Pins CONFIG1, CONFIG2 and DEF_SPI_I2C-GPIO

The TPS65912x contains two banks of OTP memory that define the default settings programmed. CONFIG1 selects between these two banks of memory. The logic level at pin CONFIG1 in state CONFIG determines which of the OTP banks is used and its content is copied to the user registers to set all OTP configurable options like default voltages and power-up timing.

CONFIG2 is used to remap functions to pins. For CONFIG2=1, pins EN1 to EN4 as well as SCL_AVS, SDA_AVS and SLEEP are active. With CONFIG2=0, these pins are used as DCDCx_SEL and CLK_REQ1, CLK_REQ2 and PWR_REQ pins.

CONFIG2=1; DEFAULT PIN USAGE	DEFAULT FUNCTION	CONFIG2=0; ALTERNATE PIN USAGE	ALTERNATE FUNCTION
EN1	enable pin for a set of DC-DC converters and LDOs defined by register EN1_SET1 and EN1_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN1=0	DCDC1_SEL	DCDC1_SEL=1: output voltage is defined by DCDC1_AVS register DCDC1_SEL=0: output voltage is defined by DCDC1_OP register
EN2	enable pin for a set of DC-DC converters and LDOs defined by register EN2_SET1 and EN2_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN2=0	DCDC2_SEL	DCDC2_SEL=1: output voltage is defined by DCDC2_AVS register DCDC2_SEL=0: output voltage is defined by DCDC2_OP register
EN3	enable pin for a set of DC-DC converters and LDOs defined by register EN3_SET1 and EN3_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN3=0	DCDC3_SEL	DCDC3_SEL=1: output voltage is defined by DCDC3_AVS register DCDC3_SEL=0: output voltage is defined by DCDC3_OP register
EN4	enable pin for a set of DC-DC converters and LDOs defined by register EN4_SET1 and EN4_SET2 for resources that are mapped to a pin, SET_OFFx, KEEP_ONx and DEF_VOLT define behavior for the case when EN4=0	DCDC4_SEL	DCDC4_SEL=1: output voltage is defined by DCDC4_AVS register DCDC4_SEL=0: output voltage is defined by DCDC4_OP register
SLEEP	SLEEP pin inactive (polarity is defined with Bit SLEEP_POL): TPS65912x is not in SLEEP state SLEEP pin active: TPS65912x is in SLEEP state; registers SET_OFFx, KEEP_ONx and DEF_VOLT define behavior with SLEEP active	PWR_REQ	enable pin for a set of DC-DC converters and LDOs defined by register EN1_SET1 and EN1_SET2
SCL_AVS	clock input of the voltage scaling (AVS) I^2C interface	CLK_REQ1	enable pin for a set of DC-DC converters and LDOs defined by register EN2_SET1 and EN2_SET2
SDA_AVS	data input/output of the voltage scaling (AVS) I^2C interface	CLK_REQ2	enable pin for a set of DC-DC converters and LDOs defined by register EN3_SET1 and EN3_SET2

DEF_SPI_I2C-GPIO defines whether the SPI interface or the I^2C interface is used as the standard communication interface. DEF_SPI_I2C-GPIO =0 defines SPI as the standard interface associated to pins SCL_SCK, SDA_MOSI, GPIO1_MISO and GPIO2_CE. CONFIG1, CONFIG2 and DEF_SPI_I2C-GPIO should be tied to GND for a low level and to LDOAO for a logic high level.

Pins CONFIG1, CONFIG2 and DEF_SPI_I2C-GPIO should not be switched in operation but hardwired to a logic low level (GND) or a logic high level by connecting them to the LDOAO voltage.

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7.17 VDDIO Voltage for Push-Pull Output Stages

There is a number of outputs that can either be configured as a push-pull output or are push-pull outputs only. Any pin with a push-pull output stage will generate its output high level by the voltage applied to pin VDDIO. The input voltage range on VDDIO is 1.6 V to 3.3 V with an undervoltage lockout below 1.6 V. With a VDDIO voltage below the undervoltage lockout threshold, the high side driver of the push-pull output stages are disabled and the output default back to open drain. Pins affected are listed below:

- nRESPWRON push-pull or open drain defined by DEVCTRL:Bit3
- INT1 push-pull or open drain defined by DEVCTRL2:Bit6
- VSUP_OUT same pin with nRESPWRON, definition by DEVCTRL:Bit3
- GPIO1, GPIO2: push-pull only
- GPIO3, GPIO4, GPIO5: push-pull or open drain managed by GPIOx registers
- 32-kHz CLKOUT: alternative function to OMAP_WDI (input); switched to output by CONFIG2=0, switched to input with CONFIG2=1; push-pull only if output with CONFIG2=0: CPCAP_WDI is set to 0 with CONFIG2=1: CPCAP_WDI is the output of the AND gate

7.18 Digital Signal Summary

- SLEEP:
  - When all SLEEP condition are met (no pending interrupt, Sleep Ball low, Sleep register set to 1), The IC is transitioning to SLEEP which impact LDO/DC-DC behavior based on settings defined in registers SET_OFF, KEEP_ON and DEF_VOLT. An interrupt or a SLEEP pin level change will cause a transition back to ACTIVE state. This input signal is level sensitive and no debouncing is applied. SLEEP is configurable and is disabled by default, so at power up its status will be ignored. In a user register it can be enabled and its active level changed between active HIGH or active LOW using bits SLEEP_POL and SLEEP_ENABLE in register DEVCTRL2.
- PWRHOLD:
  - PWRHOLD pin can be used as ON/OFF signal input (when nPWRON and Interrupt not used). It can also be used as acknowledge (Maintain Power) of power-up sequence trigger by interrupt or press of nPWRON. This input signal is level sensitive and no debouncing is applied. Rising and/or falling edge of PWRHOLD is highlighted through an associated interrupt if interrupt is unmasked.
- NRESPWRON/VSUP_OUT:
  - NRESPWRON signal is used as the reset to the processor and is in VDDIO domain. It is held low until the ACTIVE state is reached. See Section 7.19, Section 7.20 to get detailed timing.
  - VSUP_OUT is the output of the voltage monitor that can alternatively be used as a reset to a processor or included in the power-up sequencing such that it hold power up until its output is HIGH or the device power down when LOW.
- 32KCLKOUT:
  - This signal is the output of the 32K RC oscillator, which can be enabled or not during the power-on sequence. It can be enabled and disabled by register bit, during ACTIVE state of the device.
- nPWRON:
  - The nPWRON input is connected to an external button. A debounced falling edge on this signal causes a OFF to ACTIVE state transition of the device. If the device is in ACTIVE/SLEEP mode then a low level on this signal generates an interrupt. If the nPWRON signal is low for more than the PWON_TO_OFF_DELAY delay and the corresponding interrupt is not acknowledged by the external processor in TBDs then the device will go to OFF state.

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- INT1:
  - INT1 signal (active low) warns the host processor of any event that occurred on the TPS65912x device. The host processor can then poll the interrupt from the interrupt status register via I^2C to identify the interrupt source. A low level indicates an active interrupt, highlighted in the INT_STSx registers. Interrupt flag active will generate a POWER ON enable condition pulse of length TDOINT1 only when the device is in OFF state (when NRESPWRON signal is low). The POWER ON enable condition pulse will occur only if the interrupt status bit is initially low (no previous interrupt pending in the status register). Interrupt status register must be cleared first to allow device POWER OFF during the TDOINT1 pulse duration. Any of the interrupt sources can be masked programming INT_MSKx registers. The default setting is masking all interrupts. When an interrupt is masked, its corresponding interrupt status bit is still updated, but the INT1 flag is not activated. Interrupt source masking can be used to mask a device switch-on event. The INT output can be programmed as push-pull or open drain output stage with either active LOW or active HIGH output defined by two OTP settings.
- GPIO1, GPIO2, GPIO3, GPIO4, GPIO5:
  - GPIO functionality are muxed with LED and SPI interface. It can be used for event detection or control of external resources during power up.
- VCCS_VIN_MON:
  - This is the input for the internal undervoltage lockout monitor. The block provides a selectable low battery warning as well as a undervoltage shutdown.
- VCON_CLK; VCON_PWM:
  - Clock and data input for voltage scaling of DCDC1. The feature is enabled by TBD Bit. When enabled, voltage scaling through DCDC1_OP and DCDC1_AVS registers is blocked.
- CLK, MOSI, MISO,CE:
  - Clock chip enable and master in slave out (MISO) and master out slave in MOSI pins for the SPI interface. The pins are shared with the standard I^2C interface SCL and SDA and GPIO1 and GPIO2
- DEF_SPI_I2C-GPIO:
  - Defines whether multifunction pins are used for the SPI interface or for the I^2C interface and GPIOs. For DEF_SPI_I2C-GPIO = 0, the function is assigned to the SPI interface on pins CLK, MOSI, MISO, CE. For DEF_SPI_I2C-GPIO = 1, the function is assigned to the I^2C interface and GPIOs on pins SCL, SDA, GPIO1 and GPIO2.
- SCL_AVS, SDA_AVS:
  - Power I^2C interface, typically used for DVS on the step-down converters. There is a Bit on each step-down converter to switch the voltage scaling registers from the standard I^2C interface or SPI interface to the power-I^2C interface. When switched to power-I^2C, the register is blocked for access through the standard interface.

7.19 TPS659121 On/Off Operation With E450, E500

7.19.1 TPS659121 Power Up From Battery or 5-V USB Supply; CONFIG1=LOW

PWRHOLD is tied to the supply voltage so TPS65912x starts its power-up sequencing once the input voltage is above the UVLO threshold. After DCDC2, DCDC3 and LDO10 are powered, further power up is pending the status of the voltage monitor based on the VIN_MON voltage. Once the voltage is above the threshold, VSUP_OUT goes high and power-up sequencing continues. DCDC1 and LDO1 are controlled by the status of their enable pin PWR_REQ. CLK_REQ1 and CLK_REQ2 are logically OR´d to enable LDO4 and LDO5.

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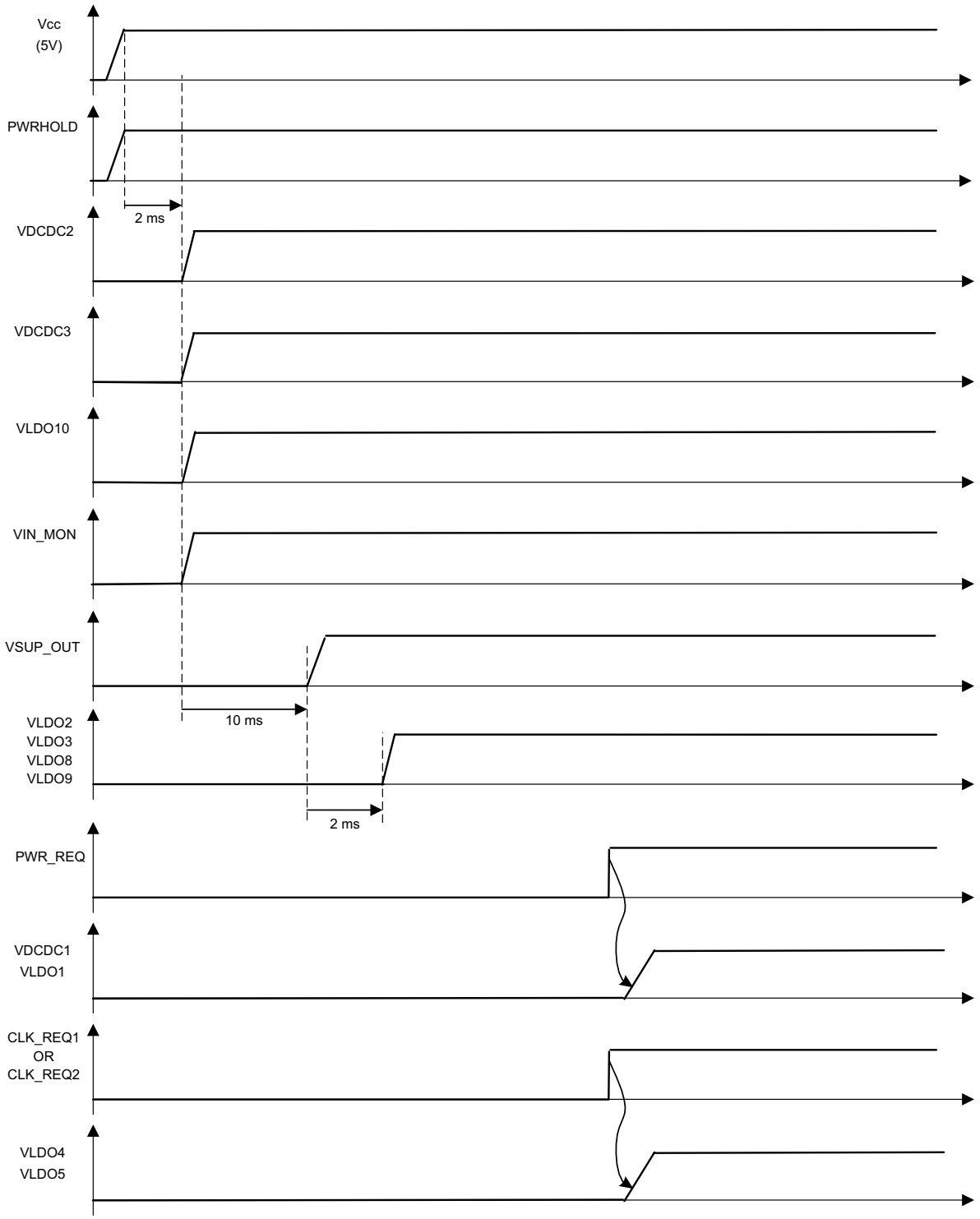

Figure 7-13. TPS659121 Battery or 5 V-USB Power-Up With CONFIG1=LOW

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7.19.2 TPS659121 Power Up From 3.3-V Host Supply; CONFIG1=LOW

PWRHOLD and VIN_MON are directly tied to the supply input of 3.3 V. TPS65912x will power up DCDC2 and LDO10 first and wait for VSUP_OUT going high to continue with LDO2, LDO3, LDO8, and LDO9. PWR_REQ and CLK_REQ pins are used to directly control DCDC1 and LDO1 or LDO4 and LDO5, respectively similar to the 5-V USB power up.

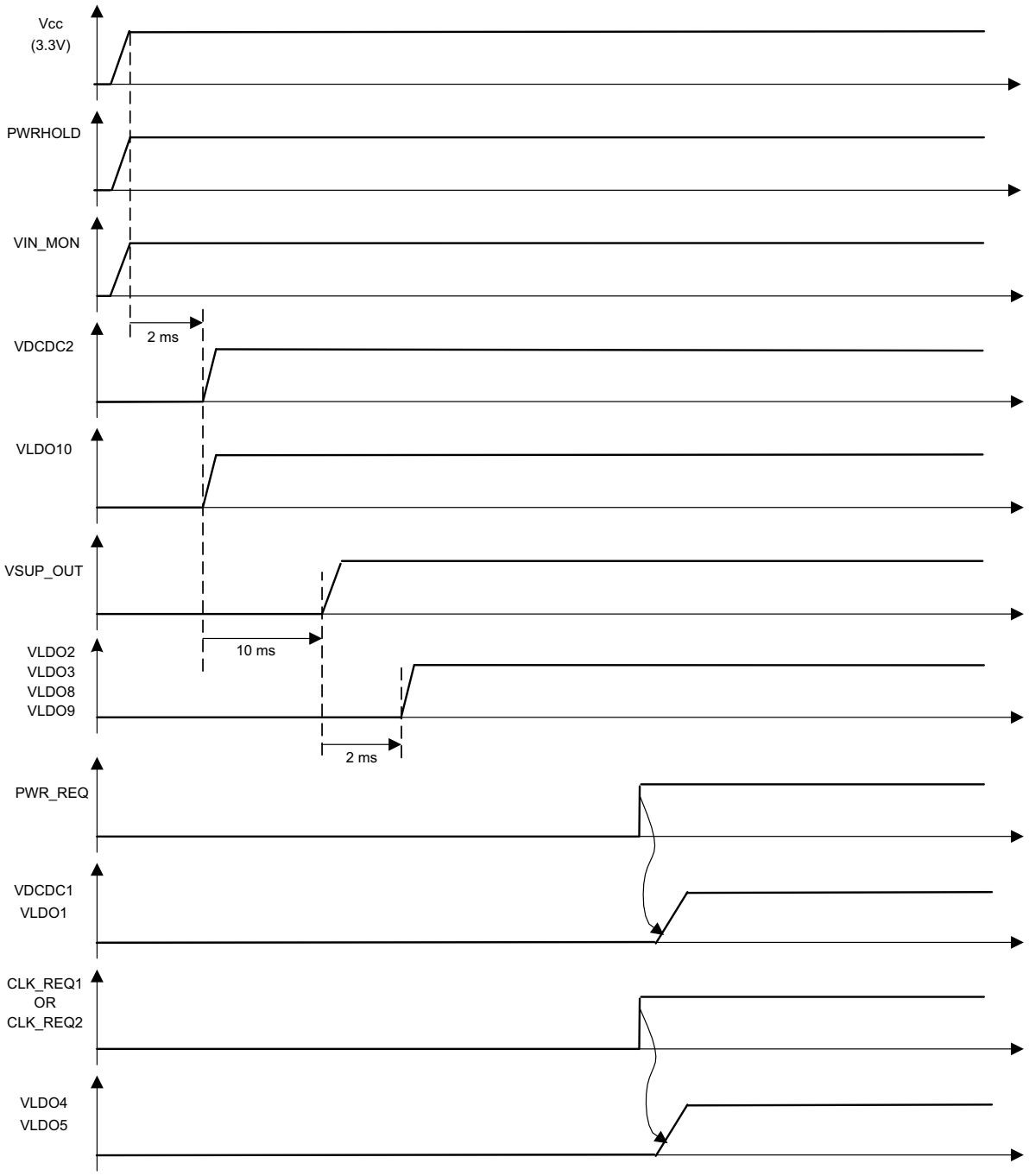

Figure 7-14. TPS659121 3.3-V Host Power Up With CONFIG1=LOW

7.20 TPS659122 On/Off Operation for CONFIG1=HIGH

TPS659122 with CONFIG1=HIGH addresses a chip set with a start-up sequencing as defined in the following. See the default voltage table given under , Figure 7-15, Figure 7-16, and Figure 7-17.

7.20.1 TPS659122 Power Up With CONFIG1=HIGH

PWRHOLD is tied to the supply voltage, so TPS659122 starts its power-up sequencing once the input voltage is above the UVLO threshold. After the DC-DC converters and LDOs have started, the nRESPWRON signal is released and TPS659122 is ready to respond to commands over its digital interfaces. Pin CLK_REQ1 is used to enable / disable LDO1 while CLK_REQ2 controls the enable function for LDO3. DCDC4 is enabled during the automatic power-up sequence along with DCDC2. After nRESPWRON is released high, enable control for DCDC4 is given to pin SLEEP, so pulling the SLEEP pin low will disable DCDC4 after the power-up cycle is completed and nRespwron has been released.

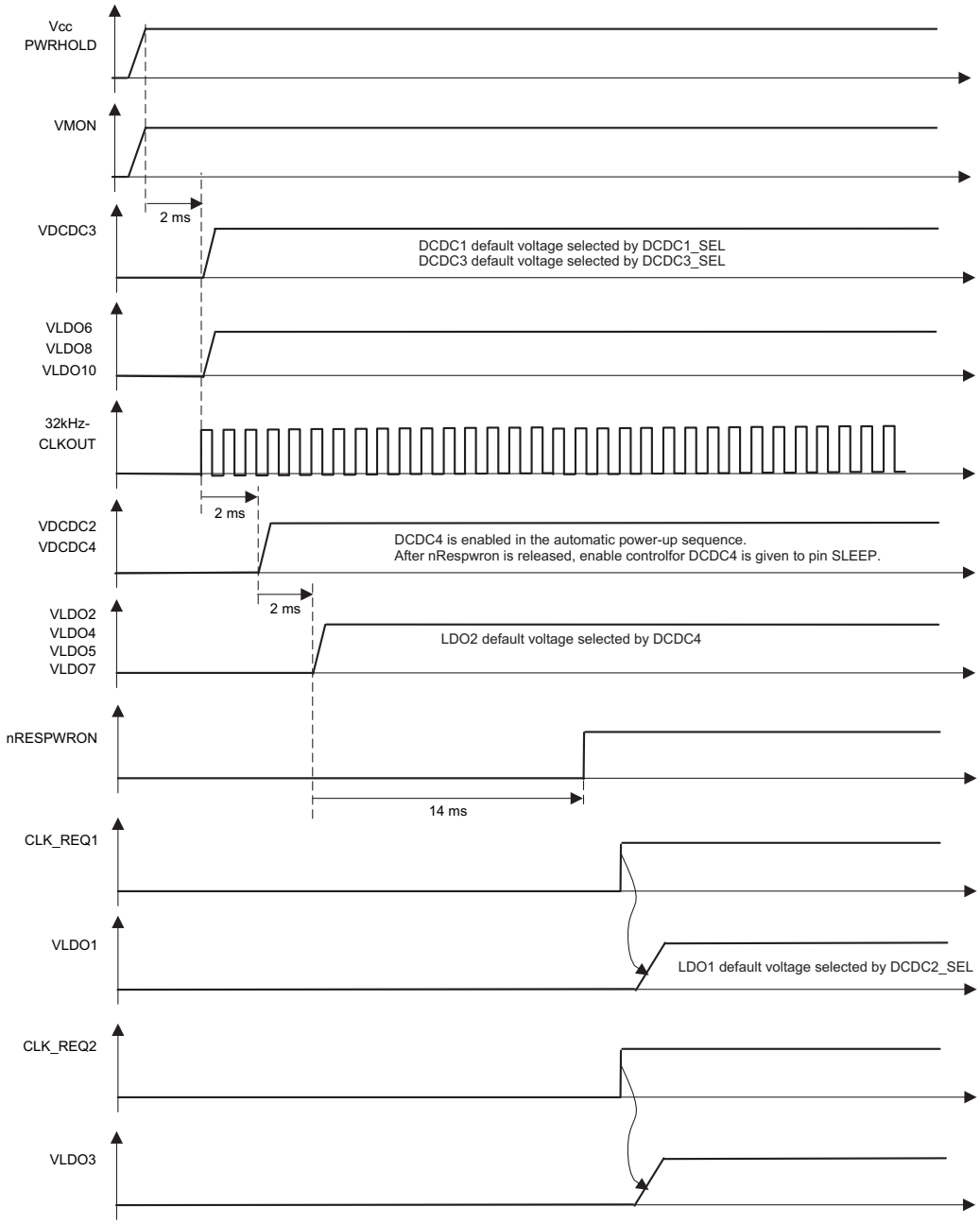

Figure 7-15. TPS659122 Power Up With CONFIG1=HIGH

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7.20.2 TPS659121, TPS659122 Power-Off Sequence With CONFIG1=HIGH

Once the voltage at the input to the voltage monitor on pin VI_MON drops below the threshold, an interrupt at pin INT1 is generated by pulling INT1=LOW. After a programmable delay of VMON_DELAY[1,0] of up to 250 µs, VSUP_OUT goes LOW which triggers the shutdown cycle after another 2-ms delay. During shutdown, all converters and LDOs are disabled at the same time.

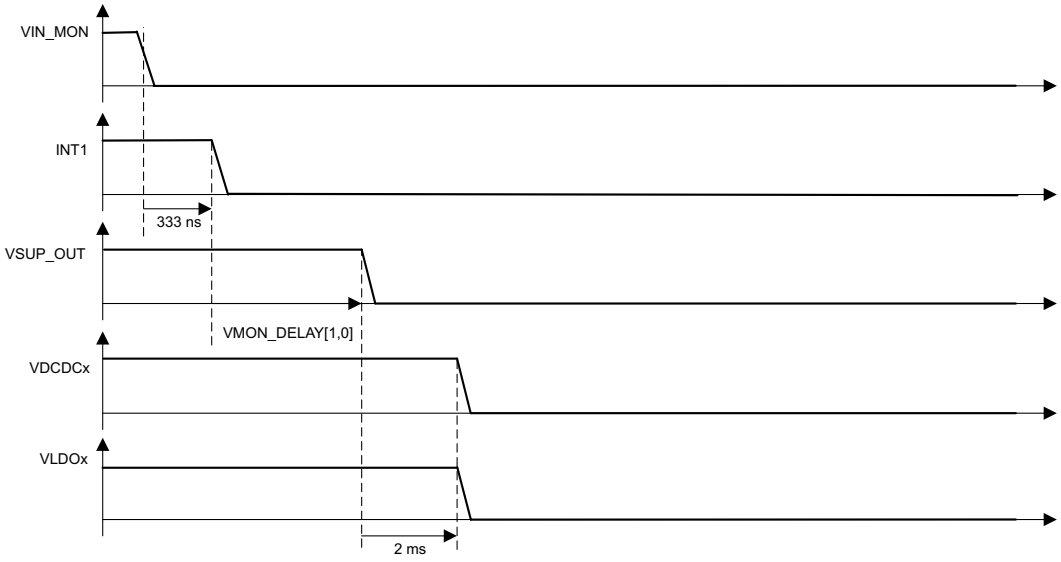

Figure 7-16. TPS659121, TPS659122 Power Cut With CONFIG1=HIGH

7.21 TPS659122 On/Off Operation for CONFIG1=LOW

TPS659122 with CONFIG1=LOW addresses a different chipset and, therefore, has default voltage settings and start-up sequencing defined differently compared to CONFIG1=HIGH. See the default voltage table given under and Figure 7-17.

7.21.1 TPS659122 Power Up With CONFIG1=LOW

PWRHOLD is tied to the supply voltage, so TPS659122 starts its power-up sequencing once the input voltage is above the UVLO threshold. After the DC-DC converters and LDOs have started, the nRESPWRON signal is released and TPS659122 is ready to respond to commands over its digital interfaces.

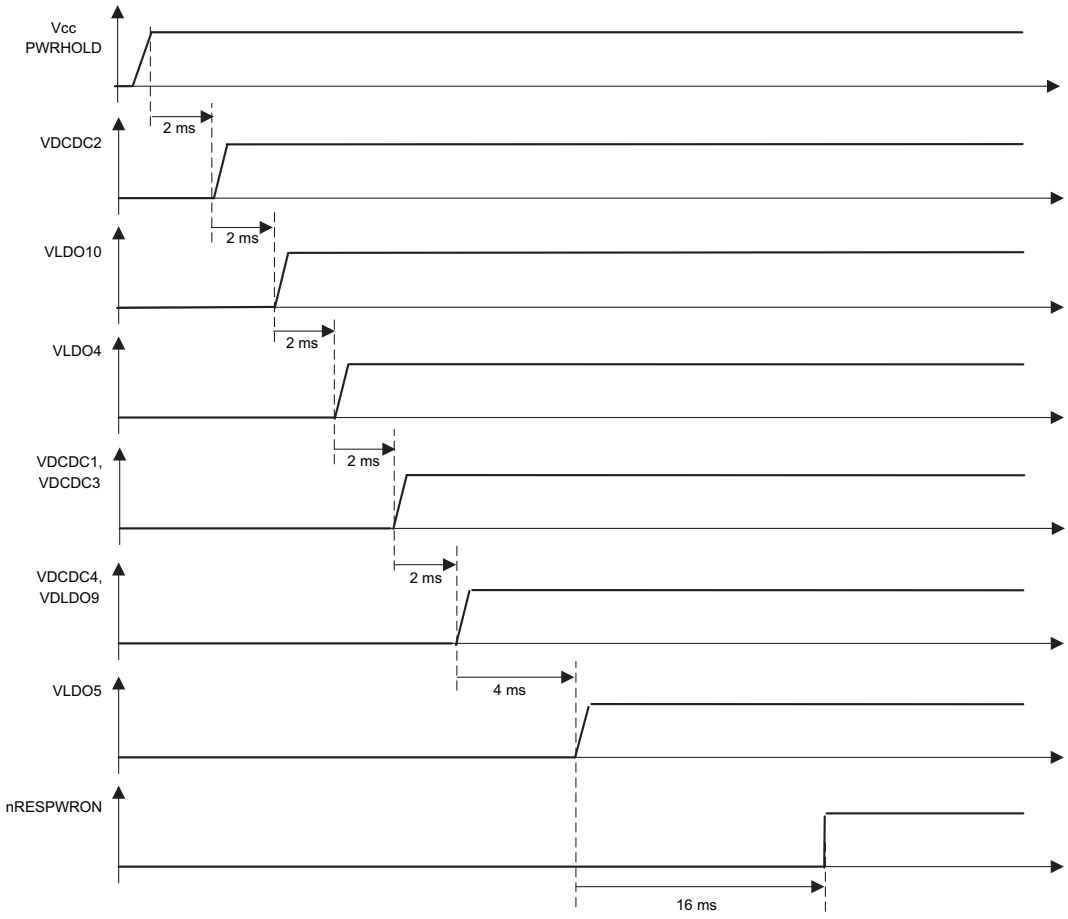

Figure 7-17. TPS659122 Power Up With CONFIG1=LOW

7.21.2 TPS659122 Power-Off Sequence With CONFIG1=LOW

When PWRHOLD goes LOW, all resources will power down at the same time.

7.22 Interfaces

There are three interfaces in the TPS65912x device. A high-speed I^2C interface that has access to all register, a SPI interface that can optionally be used to access all registers and a high-speed power I^2C interface that can be used to dynamically change the output voltage of the DC-DC converters. The power I^2C interface only has access to the voltage scaling registers of the DC-DC converters. If it is activated by a selection bit, the registers it is using are blocked for the general-purpose I^2C or SPI interface. All interfaces are active in ACTIVE state only; in all other states, the interfaces are held in a reset and cannot be used to access TPS65912x.

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7.23 Serial Peripheral Interface

The serial peripheral interface (SPI) uses 4 signals: A chip enable SPI_CE, the clock from the bus master SPI_CLK, an input port SPI_MOSI (Master In Slave Out), and an output port SPI_MISO (Master Out Slave In). The read/write Bit is followed by a 8-bit register address followed by 7 bits of unused bits followed by the data bits. The MISO output is set to high impedance when TPS65912x is not addressed by setting CE = LOW; thus allowing multiple slaves on the SPI bus.

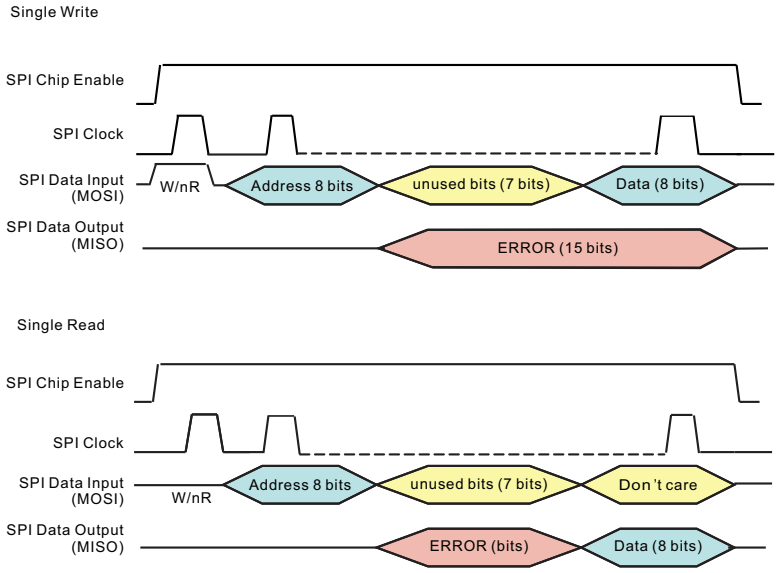

Figure 7-18. SPI READ and WRITE Protocol

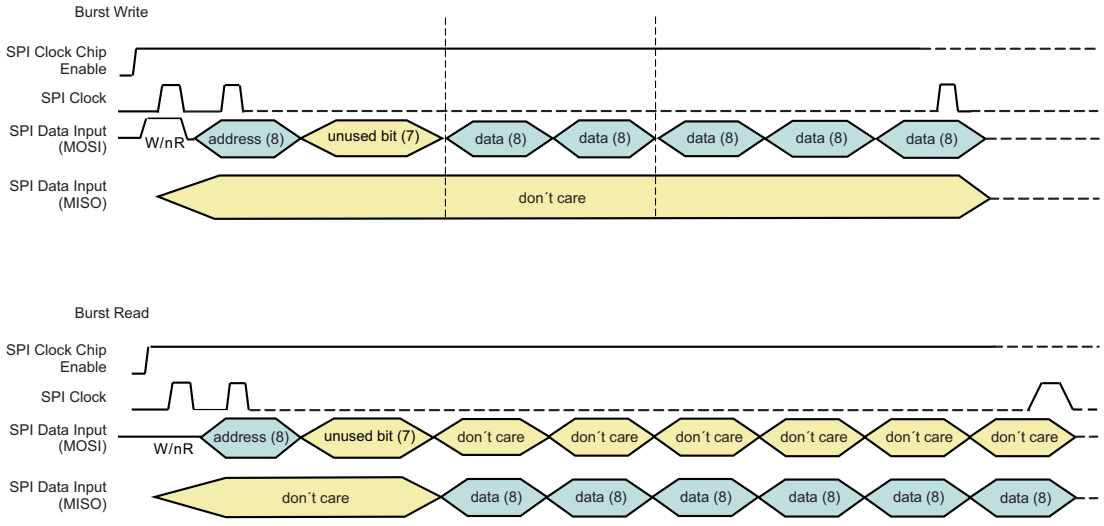

Figure 7-19. SPI BURST READ and BURST WRITE Protocol

7.24 I²C Interface

I²C is a 2-wire serial interface developed by NXP® (formerly Philips Semiconductor) (see I²C-Bus Specification and user manual). The bus consists of a data line (SDA) and a clock line (SCL) with pullup structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I²C compatible devices connect to the I²C bus through open-drain I/O pins, SDA and SCL. A master device, usually a microcontroller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The TPS65912x works as a slave and supports the following data transfer modes, as defined in the I²C-Bus Specification: standard mode (100 kbps), fast mode (400 kbps), and high-speed mode (up to 3.4 Mbps in write mode). The interface adds flexibility to the power supply solution, enabling most functions to be programmed to new values depending on the instantaneous application requirements. Register contents are loaded when voltage is applied to TPS65912x higher than the undervoltage lockout level (UVLO) of 2.4 V. Once the device is in ACTIVE state and is turned off, Bit LOAD-OTP [DEVCONTROL:Bit6] forces a reload of the registers when LOAD-OTP = 1 (default). With LOAD-OTP = 0, register content is not changed unless the supply voltage drops below the UVLO threshold. The I²C interface is running from an internal oscillator that is automatically enabled when there is an access to the interface.

The data transfer protocol for standard and fast modes is exactly the same, therefore, they are referred to as F/S-mode in this document. The protocol for high-speed mode is different from the F/S mode, and it is referred to as HS mode. The TPS65912x supports 7-bit addressing; 10-bit addressing and general call address are not supported.

7.24.1 I²C Implementation

There are two I²C interfaces on TPS65912x. One for general purpose use referred to as general purpose or standard I²C interface and one that is exclusively used for voltage scaling on the DC-DC converters referred to as AVS- or power-I²C interface.

The TPS65912x has a 7-bit address with the LSB factory programmable.

The device address for the STANDARD-I²C interface is set to *0101101*.

The device address for the AVS-I²C interface is set to *0010011*.

Other default addresses are available upon request. Contact TI about different settings.

7.24.2 F/S-Mode Protocol

The master initiates data transfer by generating a start condition. The start condition is when a high-to-low transition occurs on the SDA line while SCL is high, see Figure 7-20. All I²C-compatible devices should recognize a start condition.

The master then generates the SCL pulses, and transmits the 7-bit address and the read/write direction bit R/W on the SDA line. During all transmissions, the master ensures that data is valid. A valid data condition requires the SDA line to be stable during the entire high period of the clock pulse, see Figure 7-21. All devices recognize the address sent by the master and compare it to their internal fixed addresses. Only the slave device with a matching address generates an *acknowledge*, see Figure 7-22, by pulling the SDA line low during the entire high period of the ninth SCL cycle. Upon detecting this acknowledge, the master knows that the communication link with a slave has been established.

The master generates further SCL cycles to either transmit data to the slave (R/W bit = 0) or receive data from the slave (R/W bit = 1). In either case, the receiver must acknowledge the data sent by the transmitter. An acknowledge signal can either be generated by the master or by the slave, depending on which one is the receiver. Valid 9-bit data sequences consisting of 8-bit data and 1-bit acknowledge can continue as long as necessary.

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To signal the end of the data transfer, the master generates a stop condition by pulling the SDA line from low to high while the SCL line is high, see Figure 7-20. This releases the bus and stops the communication link with the addressed slave. All I^2C-compatible devices must recognize the stop condition. Upon the receipt of a stop condition, all devices know that the bus is released, and they wait for a start condition followed by a matching address

Attempting to read data from register addresses not listed in this section results in a readout of FFh.

7.24.3 H/S-Mode Protocol

When the bus is idle, both SDA and SCL lines are pulled high by the pullup devices.

The master generates a start condition followed by a valid serial byte containing HS master code 00001XXX. This transmission is made in F/S mode at no more than 400 Kbps. No device is allowed to acknowledge the HS master code, but all devices must recognize it and switch their internal setting to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. A stop condition ends the HS mode and switches all the internal settings of the slave devices to support the F/S mode. Instead of using a stop condition, repeated start conditions are used to secure the bus in HS mode.

Attempting to read data from register addresses not listed in this section results in a readout of FFh.

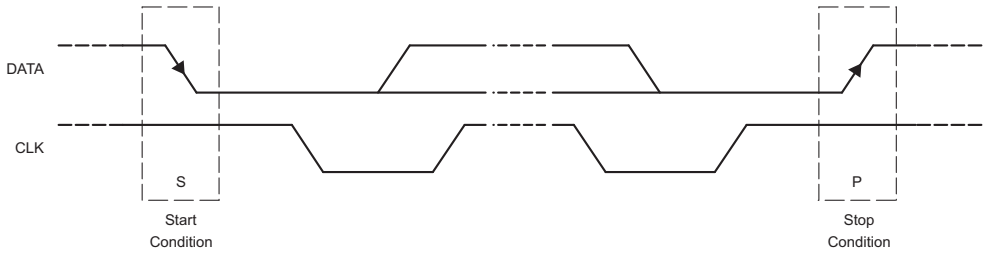

Figure 7-20. START and STOP Conditions

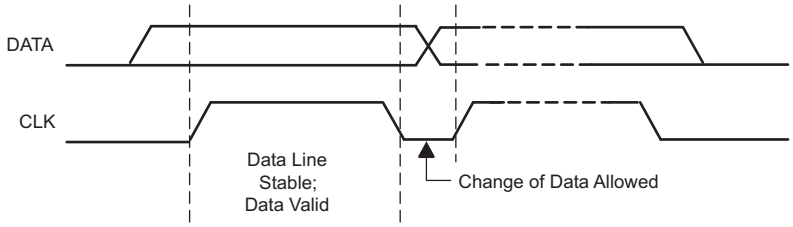

Figure 7-21. Bit Transfer on the Serial Interface

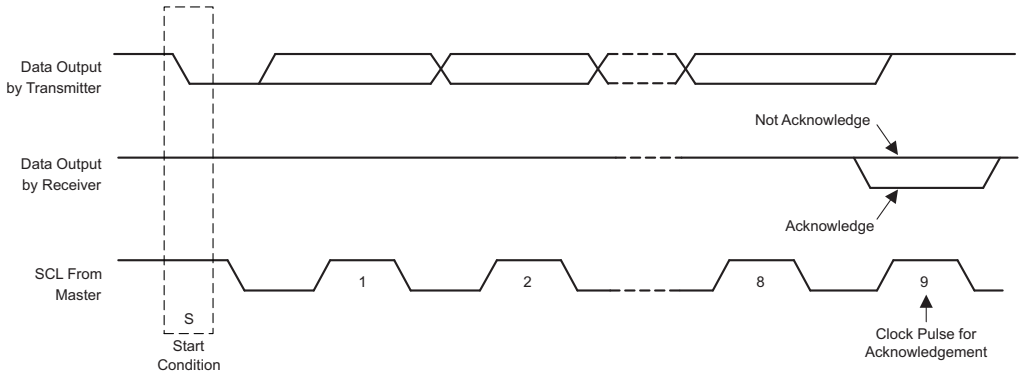

Figure 7-22. Acknowledge on the I²C Bus

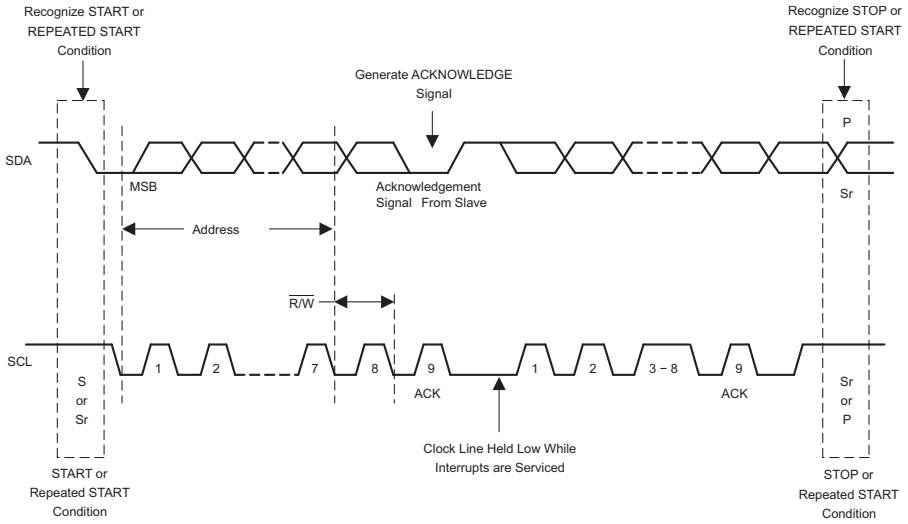

Figure 7-23. Bus Protocol

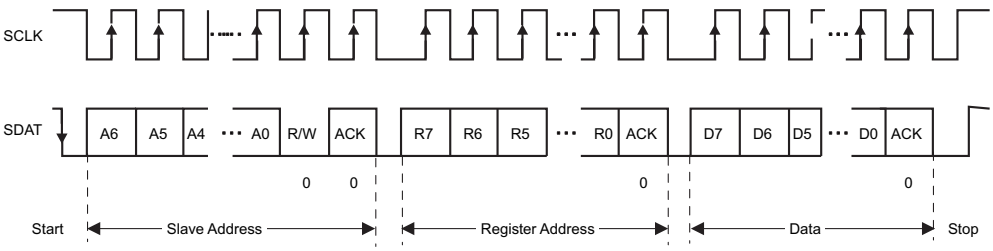

Figure 7-24. I²C Interface WRITE to TPS65912x; F/S mode

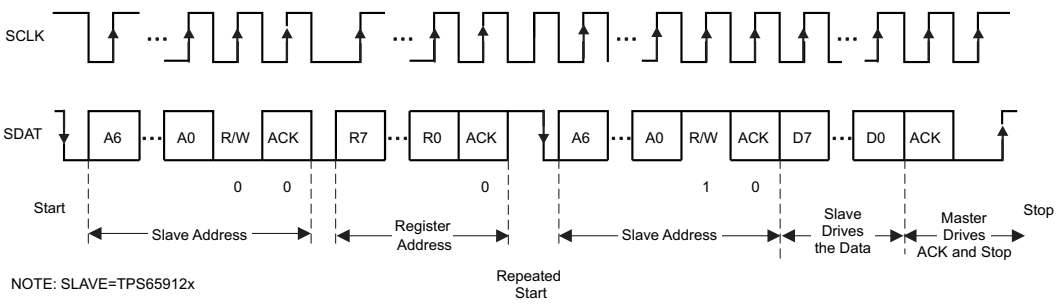

Figure 7-25. I²C Interface READ from TPS65912x; F/S mode

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7.25 Thermal Monitoring and Shutdown

Two thermal-protection modules monitor the junction temperature of the device versus two thresholds:

- Hot-Die temperature threshold
- Thermal Shutdown temperature thresholds

When the Hot-Die temperature threshold is reached, an interrupt is sent to SW to close the non-critical running tasks.

The output of both thermal protection modules is logically OR'd. When the Thermal Shutdown temperature threshold is reached the TPS65912x device is set under reset and a transition to OFF state is initiated. Then the POWER ON enable conditions of the device will not be taken into consideration until the die temperature has decreased below the Hot-Die threshold. An hysteresis is applied to the Hot-Die and shutdown threshold, when detecting a falling edge of temperature, and both detection are debounced in order to avoid any parasitic detection. The TPS65912x device allows to program four hot-die temperature thresholds in order to increase the flexibility of the system.

By default, the thermal protection is enabled in ACTIVE state, but It can be disabled through programming the THERM_REG register. The thermal protection is automatically enabled during an OFF to ACTIVE state transition and will be kept enabled in OFF state after a switch-off sequence caused by a thermal shutdown event. Transition to OFF-state sequence caused by a thermal shutdown event will be highlighted in the INT_STS_REG status register. Recovery from this OFF state is initiated (switch-on sequence) when the die temperature falls below the Hot-Die temperature threshold.

Hot-Die and thermal shutdown temperature threshold detections state can be monitored or masked by reading or programming the THERM_REG register. Hot-Die interrupt can be masked by programming the INT_MSK_REG register.

7.26 Load Switch

The load switch on TPS65912x can be used as the following:

- Bypass switch for DCDC4
- Current limited switch if TPS65912x is used in USB powered applications
- A switch to turn on and off high current loads like SD cards

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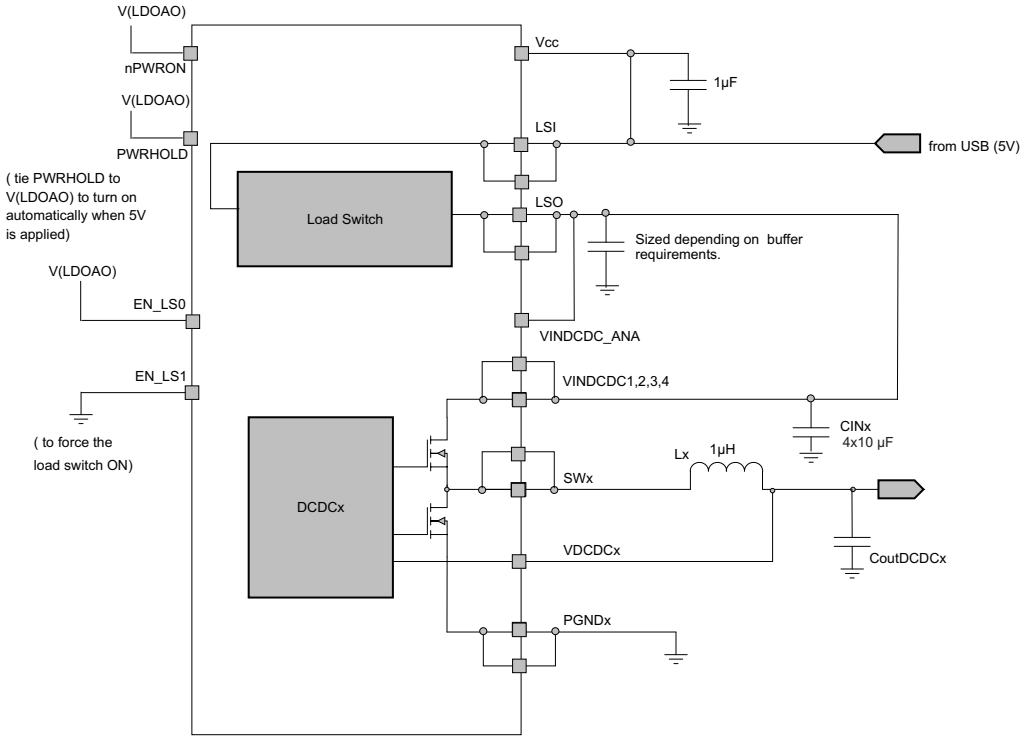

Figure 7-26. Load Switch Connected as USB Input Current Limited Switch

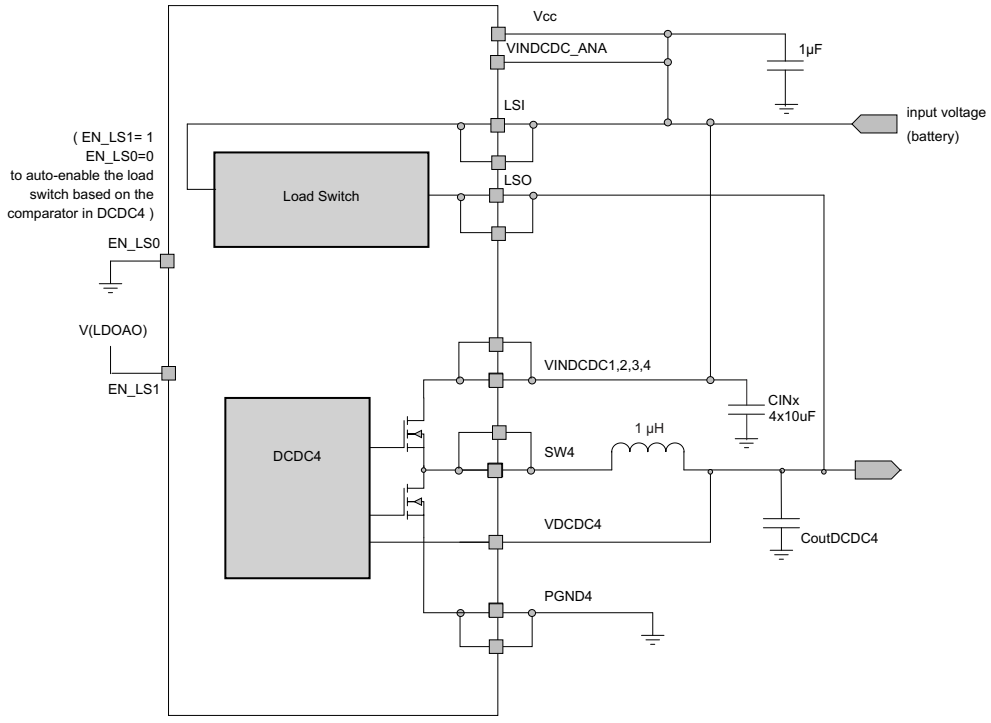

Figure 7-27. Load Switch Connected as BYPASS Switch for DCDC4

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There is a register called LOADSWITCH associated to the load switch function allowing it to be used as a bypass switch on DCDC4 or as a current limited switch. There are 4 programmable current limits between 90 mA (typically) and 2.5 A with the default current defined by an OTP setting. The enable bits are mapped to external pins called EN_LS0 and EN_LS1. The status of the pins will be copied to the register in state CONFIG, so the usage of the load switch can be externally predefined. In ACTIVE state (or SLEEP), the functionality of the load switch is controlled by the ENABLE0 and ENABLE1 bits only to turn the load switch ON, turn it off or assign it to a comparator as a bypass switch for DCDC4. When the enable function is set to the comparator, it is auto-enabled based on the voltage differential V_{in} to V_{out} on the step-down converter, DCDC4.

In case the load switch is used as a bypass switch for DCDC4, there are two additional features. The following features are enabled with LOADSWITCH:ENBALE[1,0] = 10 or 11:

- Forced PWM mode of DCDC4 is blocked if the bypass switch is closed
- The bypass switch is opened automatically when there is a overvoltage condition; LOADSWITCH:ENBALE[1,0] is automatically set "00" in an over-voltage event so the switch is opened

In applications where the load switch is used as an USB input current limited switch or as a load switch on the output of a DC-DC converter to LDO, the above features must be disabled. This is the case when the load switch is enabled with LOADSWITCH:ENBALE[1,0] = 01.

See the LOADSWITCH register in *Section 7.28.2* for further details.

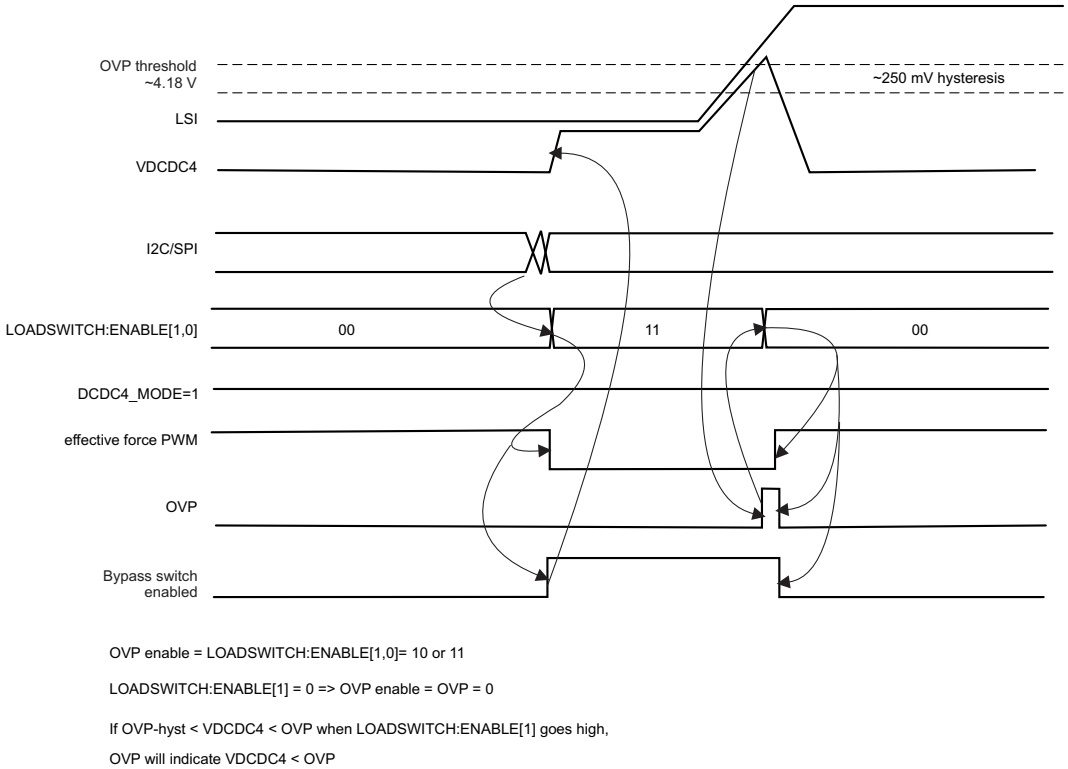

Figure 7-28. Load Switch Timing for LOADSWITCH:ENABLE[1,0] = 10 or 11

7.27 LED Driver

GPIO3, GPIO4, and GPIO5 can alternatively be configured to drive LEDs by setting Bit GPIO_SEL = 1 in register GPIOx. This will switch the output stage to a current sink controlled by the LED control registers LEDx_CTRLx, LED_RAMP_UP_TIME, LED_RAMP_DOWN_TIME and LED_SEQ_EN. LEDs are enabled in the LED_SEQ_EN register. The LED current sink is PWMd with the duty cycle defined LEDx_CTRL7:LEDx_PWM[4,0]. All 3 GPIOs should either be assigned as a LED driver or as a standard GPIO.

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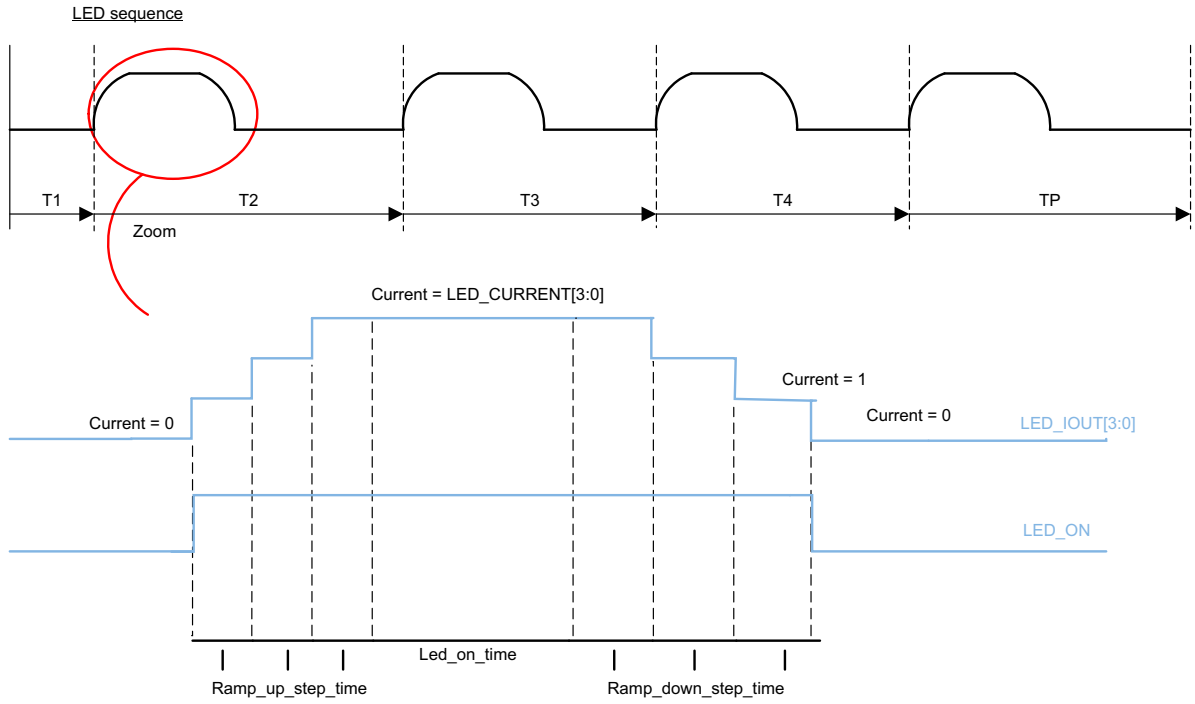
To turn on LEDA with a constant current of 10 mA:

- Set the GPIO as a LED current sink output: GPIOA:GPIO_SEL = 1
- Set the constant current to 10 mA: LEDA_CTRL1:LEDA_CURRENT[3,0] = 0b0100
- Set the PWM duty cycle to 100%: LEDA_CTRL7:LEDA_PWM[4,0] = 0b11111
- Enable the LEDA current sink: LED_SEQ_EN:LEDA_EN = 1

In addition to just turn on and turn off an LED, the LED driver allows to set LED sequence to perform a flash sequence in hardware by enabling the flash sequencer by Bit LEDx_SEQ_EN for each of the three LEDs.



T1, T2, T3, T4 : 0, 1 ...127 x 64 ms => reg ledx_t1, ledx_t2 ….

Tp : 0, 1 …127 x 64 ms=> reg ledx_tp

Ramp step time : 0, 1 … 31 x 8 ms=> reg led_ramp_up_time, led_ramp_down_time

Figure 7-29. LED Sequencer

The LED driver allows to set a dc current in the range from 2 mA to 20 mA for each LED. In addition to this, there is a LED flash sequence programmable defined by T1, T2, T3, T4, and TP. Within these time slots the LED can be turned on defined by LEDx_ON_TIME with a defined ramp-up slope set with register LED_RAMP_UP and ramp-down slope. The slopes are set to the same value for all three LEDs but other parameters are programmable independently. Figure 7-29 shows an LED flash cycle. The ramp enable bits define whether the current immediately steps to its defined value (LEDx_CURRENT[3,0]) or ramps with a certain slope.

- During a sequence if LEDx_RAMP_EN=0, current immediately goes to LEDx_I[3:0]
- During a sequence if LEDx_RAMP_EN=1, current steps up and down to LEDx_I[3:0] with a certain slope

In addition, the LED current is pulse-width modulated with a duty cycle defined in register LEDx_CTRL7.

For the LED driver to operate properly, the time for RAMP-UP + LED_ON + RAMP_DOWN must be smaller than the sequence Tn (with n = 1, 2, 3, 4, P).

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7.28 Memory

7.28.1 Register Format

The TPS65912x family consists of several devices. All of them allow to select between two different default configurations stored in OTP memory. The memory bank used, is selected by either setting pin CONFIG1 to a logic LOW or a logic HIGH level. For the complete family there are four different default configurations possible that are given in the register set. Registers that allow different default settings based on the family member and CONFIG1 setting contain separate lines showing their default. Some registers are not configurable in their default settings. For these registers, only one line is shown. The enable bits of resources that are powered up in the automatic power-up sequence are set during this automatic sequence. The status after power up is therefore different from their reset state defined in OTP.

The format in the registers is as given in Table 7-1. A separate *Bit Field Description* table lists the bit names and bit descriptions for each register address.

Table 7-1. REGISTER NAME(1); Register Address

7	6	5	4	3	2	1	0
Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name	Bit Name
Default settings for TPS659121 for CONFIG1=LOW							
Default settings for TPS659121 for CONFIG1=HIGH							
Default settings for TPS659122 for CONFIG1=LOW							
Default settings for TPS659122 for CONFIG1=HIGH							
OTP = default state is configurable at TI							
R = read or R/W = read/write capability for each Bit							

(1) Register reset on Power On Reset (POR)

7.28.2 Register Descriptions

7.28.2.1 DCDC Registers

Table 7-2. DCDC Register Memory Map

Offset	Register Name	Section
00h	DCDC1_CTRL	DCDC1_CTRL (00h)
01h	DCDC2_CTRL	DCDC2_CTRL (01h)
02h	DCDC3_CTRL	DCDC3_CTRL (02h)
03h	DCDC4_CTRL	DCDC4_CTRL (03h)
04h	DCDC1_OP	DCDC1_OP (04h)
05h	DCDC1_AVS	DCDC1_AVS (05h)
06h	DCDC1_LIMIT	DCDC1_LIMIT (06h)
07h	DCDC2_OP	DCDC2_OP (07h)
08h	DCDC2_AVS	DCDC2_AVS (08h)
09h	DCDC2_LIMIT	DCDC2_LIMIT (09h)
0Ah	DCDC3_OP	DCDC3_OP (0Ah)
0Bh	DCDC3_AVS	DCDC3_AVS (0Bh)
0Ch	DCDC3_LIMIT	DCDC3_LIMIT (0Ch)
0Dh	DCDC4_OP	DCDC4_OP (0Dh)
0Eh	DCDC4_AVS	DCDC4_AVS (0Eh)
0Fh	DCDC4_LIMIT	DCDC4_LIMIT (0Fh)

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7.28.2.1.1 DCDC1_CTRL (00h)

Figure 7-30. DCDC1_CTRL(1); Register Address: 00h

7	6	5	4	3	2	1	0
VCON_ENABLE	VCON_RANGE[1]	VCON_RANGE[0]	TSTEP[2]	TSTEP[1]	TSTEP[0]	DCDC1_MODE	RSVD
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
0	0	1	0	0	0	0	0
0	0	0	0	0	0	0	0
OTP	OTP	OTP				OTP	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-3. Bit Field Descriptions

Field	Description
VCON_ENABLE	**0** voltage scaling is done by I^2C registers or DCDCx_SEL pins (if configured) **1** voltage scaling is done by the VCON pins VCON_PWM and VCON_CLK; voltage table is automatically forced to RANGE[1,0]=00; register content in voltage scaling register is ignored
VCON_RANGE[1,0]	**00** sets output voltage range for VCON operation: 500 mV to 1100 mV with 25 mV steps; 24 steps **01** sets output voltage range for VCON operation: 700 mV to 1100 mV with 12.5 mV steps; 32 steps **10** sets output voltage range for VCON operation: 600 mV to 1000 mV with 12.5 mV steps; 32 steps **11** sets output voltage range for VCON operation: 500 mV to 900 mV with 12.5 mV steps; 32 steps
TSTEP[2:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 7-7
DCDC1_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM
RSVD	Unused bit, should be written to **0**

7.28.2.1.2 DCDC2_CTRL (01h)

Figure 7-31. DCDC2_CTRL(1); Register Address: 01h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	TSTEP[2]	TSTEP[1]	TSTEP[0]	DCDC2_MODE	RSVD
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
						OTP	
R	R	R	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-4. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
TSTEP[2:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 7-7
DCDC2_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM

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7.28.2.1.3 DCDC3_CTRL (02h)

Figure 7-32. DCDC3_CTRL[1]; Register Address: 02h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	TSTEP[2]	TSTEP[1]	TSTEP[0]	DCDC3_MODE	RSVD
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
						OTP	
R	R	R	R/W	R/W	R/W	R/W	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-5. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
TSTEP[2:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 7-7
DCDC3_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM
RSVD	Unused bit, should be written to **0**

7.28.2.1.4 DCDC4_CTRL (03h)

Figure 7-33. DCDC4_CTRL[1]; Register Address: 03h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	TSTEP[2]	TSTEP[1]	TSTEP[0]	DCDC4_MODE	RAMP_TIME
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1
						OTP	OTP
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-6. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
TSTEP[2:0]	Time step: when changing the output voltage, the new value is reached through successive voltage steps (if not bypassed). The equivalent programmable slew rate of the output voltage is shown in Table 7-7
DCDC4_MODE	**0** Enable Automatic PWM/PFM mode switching **1** Force PWM
RAMP_TIME[1]	**0** ramp time for initial start up is 200-µs minimum **1** ramp time for initial start up is 60-µs maximum

(1) See the SPARE register at address 0x63 for additional options for DCDC4 in Rev 1.1 of silicon

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Table 7-7. DCDCx TSTEP Settings

TSTEP[2:0]	Slew Rate (mV/µs)
000	30
001	12.5
010	9.4
011	7.5
100	6.25
101	4.7
110	3.12
111	2.5

7.28.2.1.5 DCDC1_OP (04h)

Figure 7-34. DCDC1_OP(1); Register Address: 04h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	1	1	1	0	0
0	0	0	1	1	1	0	0
0	0	1	0	0	0	1	1
0	0	1	1	1	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-8. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
SELREG	**0** V_{DCDC1} Voltage selected by DCDC1_OP register; if pin CONFIG2 is set to LOW enabling the DCDC1_SEL functionality, this Bit should be kept at 0 to allow the DCDC1_SEL pin to take control of whether DCDC1_OP or DCDC1_AVS is used to set the output voltage **1** V_{DCDC1} selected by DCDC1_AVS register
SEL[5:0]	DCDC1 Output Voltage Selection based on RANGE[1:0] in DCDC1 register selections shown in Table 7-21 through Table 7-24. The register is set to its default voltage with PWR_REQ=LOW.

7.28.2.1.6 DCDC1_AVS (05h)

Figure 7-35. DCDC1_AVS(1); Register Address: 05h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	0	0	0	0	0
0	0	1	0	0	0	0	0
(1)	0	1	0	0	0	1	1
(1)	0	1	1	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-9. Bit Field Descriptions

Field	Description
ENABLE	**0** DCDC1 Disabled **1** DCDC1 Enabled **(1)** DCDC1 Enabled during automatic power-up sequence
ECO	**0** normal mode **1** ECO mode if bit DCDC1_MODE is set to 0
RSVD	Unused bit, should be written to **0**
SEL[5:0]	DCDC1 Output Voltage Selection based on RANGE[1:0] in DCDC1 register selections shown in Table 7-21 through Table 7-24. The register is set to its default voltage with PWR_REQ=LOW.

7.28.2.1.7 DCDC1_LIMIT (06h)

Figure 7-36. DCDC1_LIMIT(1); Register Address: 06h

7	6	5	4	3	2	1	0
RANGE[1]	RANGE[0]	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
0	0	1	1	0	0	0	0
0	0	1	1	0	0	0	0
0	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-10. Bit Field Descriptions

Field	Description
RANGE[1:0]	Selects the output range. See Table 7-20 for further information.
MAX_SEL[5:0]	Defines the maximum value the output voltage in DCDC1_AVS or DCDC1_OP can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If MAX_SEL is set to any other value than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked; contact TI for setting of the max limit in DCDC1_LIMIT in OTP memory.

7.28.2.1.8 DCDC2_OP (07h)

Figure 7-37. DCDC2_OP(1); Register Address: 07h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	0	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	0	1	0	0
0	0	1	1	0	1	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-11. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
SELREG	**0** V_{DCDC2} Voltage selected by DCDC2_OP reg; if pin CONFIG2 is set to LOW enabling the DCDC2_SEL functionality, this Bit should be kept at 0 to allow the DCDC2_SEL pin to take control of whether DCDC2_OP or DCDC2_AVS is used to set the output voltage **1** V_{DCDC2} selected by DCDC2_AVS register

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Table 7-11. Bit Field Descriptions (continued)

Field	Description
SEL[5:0]	DCDC2 Output Voltage Selection based on RANGE[1:0] in DCDC2 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.9 DCDC2_AVS (08h)

Figure 7-38. DCDC2_AVS(1); Register Address: 08h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	1	1	1	0	0
(1)	0	1	1	1	1	0	0
(1)	0	1	1	0	1	0	0
(1)	0	1	1	0	1	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-12. Bit Field Descriptions

Field	Description
ENABLE	**0** DCDC2 Disabled **1** DCDC2 Enabled **(1)** DCDC2 Enabled during automatic power-up sequence
ECO	**0** normal mode **1** ECO mode if bit DCDC2_MODE is set to 0
RSVD	Unused bit, should be written to **0**
SEL[5:0]	DCDC2 Output Voltage Selection based on RANGE[1:0] in DCDC2 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.10 DCDC2_LIMIT (09h)

Figure 7-39. DCDC2_LIMIT(1); Register Address: 09h

7	6	5	4	3	2	1	0
RANGE[1]	RANGE[0]	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
1	0	1	1	1	1	1	1
1	0	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-13. Bit Field Descriptions

Field	Description
RANGE[1:0]	Selects the output range. See Table 7-20 for further information.
MAX_SEL[5:0]	Defines the maximum value the output voltage in DCDC2_AVS or DCDC2_OP can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If MAX_SEL is set to any other value than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked; contact TI for setting of the max limit in DCDC2_LIMIT in OTP memory.

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7.28.2.1.11 DCDC3_OP (0Ah)

Figure 7-40. DCDC3_OP(1); Register Address: 0Ah

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	0	1	1	0
0	0	1	1	0	1	1	0
0	0	1	0	0	0	1	1
0	0	1	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-14. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
SELREG	**0** V_{DCDC3} Voltage selected by DCDC3_OP reg; if pin CONFIG2 is set to LOW enabling the DCDC3_SEL functionality, this Bit should be kept at 0 to allow the DCDC3_SEL pin to take control of whether DCDC3_OP or DCDC3_AVS is used to set the output voltage **1** V_{DCDC3} selected by DCDC3_AVS register
SEL[5:0]	DCDC3 Output Voltage Selection based on RANGE[1:0] in DCDC3 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.12 DCDC3_AVS (0Bh)

Figure 7-41. DCDC3_AVS(1); Register Address: 0Bh

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	0	1	1	0	0
(1)	0	1	0	1	1	0	0
(1)	0	1	0	0	0	1	1
(1)	0	0	1	1	1	1	0
		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-15. Bit Field Descriptions

Field	Description
ENABLE	**0** DCDC3 Disabled **1** DCDC3 Enabled **(1)** DCDC3 Enabled during automatic power-up sequence
ECO	**0** normal mode **1** ECO mode if bit DCDC3_MODE is set to 0
RSVD	Unused bit, should be written to **0**
SEL[5:0]	DCDC3 Output Voltage Selection based on RANGE[1:0] in DCDC3 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.13 DCDC3_LIMIT (0Ch)

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Figure 7-42. DCDC3_LIMIT(1); Register Address: 0Ch

7	6	5	4	3	2	1	0
RANGE[1]	RANGE[0]	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-16. Bit Field Descriptions

Field	Description
RANGE[1:0]	Selects the output range. See Table 7-20 for further information.
MAX_SEL[5:0]	Defines the maximum value the output voltage in DCDC3_AVS or DCDC3_OP can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If MAX_SEL is set to any other value than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked; contact TI for setting of the max limit in DCDC3_LIMIT.

7.28.2.1.14 DCDC4_OP (0Dh)

Figure 7-43. DCDC4_OP(1); Register Address: 0Dh

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	1
0	0	1	1	1	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-17. Bit Field Descriptions

Field	Description
RSVD	Unused bit, should be written to **0**
SELREG	**0** V_{DCDC4} Voltage selected by DCDC4_OP reg; if pin CONFIG2 is set to LOW enabling the DCDC4_SEL functionality, this Bit should be kept at 0 to allow the DCDC4_SEL pin to take control of whether DCDC4_OP or DCDC4_AVS is used to set the output voltage **1** V_{DCDC4} selected by DCDC4_AVS register
SEL[5:0]	DCDC4 Output Voltage Selection based on RANGE[1:0] in DCDC4 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.15 DCDC4_AVS (0Eh)

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Figure 7-44. DCDC4_AVS(1); Register Address: 0Eh

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
(1)	0	1	0	0	0	1	1
(1)	0	1	1	1	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-18. Bit Field Descriptions

Field	Description
ENABLE	**0** DCDC4 Disabled **1** DCDC4 Enabled **(1)** DCDC4 Enabled during automatic power-up sequence
ECO	**0** normal mode **1** ECO mode if bit DCDC4_MODE is set to 0
SEL[5:0]	DCDC4 Output Voltage Selection based on RANGE[1:0] in DCDC4 register selections shown in Table 7-21 through Table 7-24.

7.28.2.1.16 DCDC4_LIMIT (0Fh)

Figure 7-45. DCDC4_LIMIT(1); Register Address: 0Fh

7	6	5	4	3	2	1	0
RANGE[1]	RANGE[0]	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-19. Bit Field Descriptions

Field	Description
RANGE[1:0]	Selects the output range. See Table 7-20 for further information.
MAX_SEL[5:0]	Defines the maximum value the output voltage in DCDC4_AVS or DCDC4_OP can be programmed to; values exceeding MAX_SEL will be replaced by the value defined in MAX_SEL. If MAX_SEL is set to any other value than 0x3F or 0x00, the RANGE bits and the MAX_SEL bits are locked; contact TI for setting of the max limit in DCDC4_LIMIT.

7.28.2.1.17 V_{DCDCx} Range Settings

Table 7-20. V_{DCDCx} Range Settings

RANGE[1:0]	Output Voltage Range
00	0.5 V to 1.2875 V in 12.5 mV steps (See Table 7-21)
01	0.7 V to 1.4875 V in 12.5 mV steps (See Table 7-22)
10	0.5 V to 2.075 V in 25 mV steps (See Table 7-23)
11	0.5 V to 3.8 V in 50 mV steps (See Table 7-24)

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7.28.2.1.18 DCDCx Voltage Settings

Table 7-21. DCDCx Voltage Settings (RANGE[1:0] = 2'b00)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.5000	100000	0.9000
000001	0.5125	100001	0.9125
000010	0.5250	100010	0.9250
000011	0.5375	100011	0.9375
000100	0.5500	100100	0.9500
000101	0.5625	100101	0.9625
000110	0.5750	100110	0.9750
000111	0.5875	100111	0.9875
001000	0.6000	101000	1.0000
001001	0.6125	101001	1.0125
001010	0.6250	101010	1.025
001011	0.6375	101011	1.0375
001100	0.6500	101100	1.0500
001101	0.6625	101101	1.0625
001110	0.6750	101110	1.0750
001111	0.6875	101111	1.0875
010000	0.7000	110000	1.1000
010001	0.7125	110001	1.1125
010010	0.725	110010	1.1250
010011	0.7375	110011	1.1375
010100	0.7500	110100	1.1500
010101	0.7625	110101	1.1625
010110	0.7750	110110	1.1750
010111	0.7875	110111	1.1875
011000	0.8000	111000	1.2000
011001	0.8125	111001	1.2125
011010	0.8250	111010	1.2250
011011	0.8375	111011	1.2375
011100	0.8500	111100	1.2500
011101	0.8625	111101	1.2625
011110	0.8750	111110	1.2750
011111	0.8875	111111	1.2875

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Table 7-22. DCDCx Voltage Settings (RANGE[1:0] = 2'b01)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.7000	100000	1.1000
000001	0.7125	100001	1.1125
000010	0.7250	100010	1.1250
000011	0.7375	100011	1.1375
000100	0.7500	100100	1.1500
000101	0.7625	100101	1.1625
000110	0.7750	100110	1.1750
000111	0.7875	100111	1.1875
001000	0.8000	101000	1.2000
001001	0.8125	101001	1.2125
001010	0.8250	101010	1.225
001011	0.8375	101011	1.2375
001100	0.8500	101100	1.2500
001101	0.8625	101101	1.2625
001110	0.8750	101110	1.2750
001111	0.8875	101111	1.2875
010000	0.9000	110000	1.3000
010001	0.9125	110001	1.3125
010010	0.925	110010	1.3250
010011	0.9375	110011	1.3375
010100	0.9500	110100	1.3500
010101	0.9625	110101	1.3625
010110	0.9750	110110	1.3750
010111	0.9875	110111	1.3875
011000	1.0000	111000	1.4000
011001	1.0125	111001	1.4125
011010	1.0250	111010	1.4250
011011	1.0375	111011	1.4375
011100	1.0500	111100	1.4500
011101	1.0625	111101	1.4625
011110	1.0750	111110	1.4750
011111	1.0875	111111	1.4875

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Table 7-23. DCDCx Voltage Settings (RANGE[1:0] = 2'b10)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.500	100000	1.300
000001	0.525	100001	1.325
000010	0.550	100010	1.350
000011	0.575	100011	1.375
000100	0.600	100100	1.400
000101	0.625	100101	1.425
000110	0.650	100110	1.450
000111	0.675	100111	1.475
001000	0.700	101000	1.500
001001	0.725	101001	1.525
001010	0.750	101010	1.550
001011	0.775	101011	1.575
001100	0.800	101100	1.600
001101	0.825	101101	1.625
001110	0.850	101110	1.650
001111	0.875	101111	1.675
010000	0.900	110000	1.700
010001	0.925	110001	1.725
010010	0.950	110010	1.750
010011	0.975	110011	1.775
010100	1.000	110100	1.800
010101	1.025	110101	1.825
010110	1.050	110110	1.850
010111	1.075	110111	1.875
011000	1.100	111000	1.900
011001	1.125	111001	1.925
011010	1.150	111010	1.950
011011	1.175	111011	1.975
011100	1.200	111100	2.000
011101	1.225	111101	2.025
011110	1.250	111110	2.050
011111	1.275	111111	2.075

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Table 7-24. DCDCx Voltage Settings (RANGE[1:0] = 2'b11)

SEL(DCDCx)[5:0]	VDCDCx (V)	SEL(DCDCx)[5:0]	VDCDCx (V)
000000	0.50	100000	2.10
000001	0.55	100001	2.15
000010	0.60	100010	2.20
000011	0.65	100011	2.25
000100	0.70	100100	2.30
000101	0.75	100101	2.35
000110	0.80	100110	2.40
000111	0.85	100111	2.45
001000	0.90	101000	2.50
001001	0.95	101001	2.55
001010	1.00	101010	2.60
001011	1.05	101011	2.65
001100	1.10	101100	2.70
001101	1.15	101101	2.75
001110	1.20	101110	2.80
001111	1.25	101111	2.85
010000	1.30	110000	2.90
010001	1.35	110001	2.95
010010	1.40	110010	3.00
010011	1.45	110011	3.05
010100	1.50	110100	3.10
010101	1.55	110101	3.15
010110	1.60	110110	3.20
010111	1.65	110111	3.25
011000	1.70	111000	3.30
011001	1.75	111001	3.35
011010	1.80	111010	3.40
011011	1.85	111011	3.45
011100	1.90	111100	3.50
011101	1.95	111101	3.55
011110	2.00	111110	3.60
011111	2.05	111111	3.80

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7.28.2.2 LDO Registers

Table 7-25. LDO Register Memory Map

Offset	Register Name	Section
10h	LDO1_OP	LDO1_OP (10h)
11h	LDO1_AVS	LDO1_AVS (11h)
12h	LDO1_LIMIT	LDO1_LIMIT (12h)
13h	LDO2_OP	LDO2_OP (13h)
14h	LDO2_AVS	LDO2_AVS (14h)
15h	LDO2_LIMIT	LDO2_LIMIT (15h)
16h	LDO3_OP	LDO3_OP (16h)
17h	LDO3_AVS	LDO3_AVS (17h)
18h	LDO3_LIMIT	LDO3_LIMIT (18h)
19h	LDO4_OP	LDO4_OP (19h)
1Ah	LDO4_AVS	LDO4_AVS (1Ah)
1Bh	LDO4_LIMIT	LDO4_LIMIT (1Bh)
1Ch	LDO5	LDO5 (1Ch)
1Dh	LDO6	LDO6 (1Dh)
1Eh	LDO7	LDO7 (1Eh)
1Fh	LDO8	LDO8 (1Fh)
20h	LDO9	LDO9 (20h)
21h	LDO10	LDO10 (21h)

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7.28.2.2.1 LDO1_OP (10h)

Figure 7-46. LDO1_OP(1); Register Address: 10h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
0	0	1	0	0	0	1	0
0	0	1	0	0	1	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-26. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
SELREG	**0** LDO1 Voltage selected by LDO1_OP register **1** LDO1 Voltage selected by LDO1_AVS register
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.2 LDO1_AVS (11h)

Figure 7-47. LDO1_AVS(1); Register Address: 11h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0
(1)	0	1	0	0	0	1	0
0	0	1	1	1	1	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-27. Register Description

Field	Description
ENABLE	**0** LDO1 Disabled **1** LDO1 Enabled **(1)** LDO1 Enabled during automatic power-up sequence
ECO	**0** LDO1 is in normal mode; Bit is ignored when SLEEP is active **1** LDO1 is in power save mode; Bit is ignored when SLEEP is active
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.3 LDO1_LIMIT (12h)

Figure 7-48. LDO1_LIMIT(1); Register Address: 12h

7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	1
0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-28. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
MAX_SEL[5:0]	Defines the maximum value the output voltage can be programmed to for LDO1_OP and LDO1_AVS. Values exceeding this limit are ignored. Supply Voltage - setting shown in Table 7-44. If MAX_SEL is set to any other value than 0x00 or 0x3F, the register is set to read only; contact Ti for a default setting in OTP memory if needed.

7.28.2.2.4 LDO2_OP (13h)

Figure 7-49. LDO2_OP(1); Register Address: 13h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-29. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
SELREG	**0** LDO2 Voltage selected by LDO2_OP register **1** LDO2 Voltage selected by LDO2_AVS register
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.5 LDO2_AVS (14h)

Figure 7-50. LDO2_AVS(1); Register Address: 14h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	0	0	0	1	0	0
(1)	0	0	0	0	1	0	0
(1)	0	0	0	0	0	0	0
(1)	0	1	0	0	1	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-30. Register Description

Field	Description
ENABLE	**0** LDO2 Disabled **1** LDO2 Enabled **(1)** LDO2 Enabled during automatic power-up sequence
ECO	**0** LDO2 is in normal mode **1** LDO2 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.6 LDO2_LIMIT (15h)

Figure 7-51. LDO2_LIMIT(1); Register Address: 15h

7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	1
0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

(1) Register reset on Power On Reset (POR)

Table 7-31. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
MAX_SEL[5:0]	Defines the maximum value the output voltage can be programmed to for LDO2_OP and LDO2_AVS. Values exceeding this limit are ignored. Supply Voltage - setting shown in Table 7-44. If MAX_SEL is set to any other value than 0x00 or 0x3F, the register is set to read only; contact Ti for a default setting in OTP memory if needed.

7.28.2.2.7 LDO3_OP (16h)

Figure 7-52. LDO3_OP(1); Register Address: 16h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	1	0	0	1
0	0	1	1	1	0	0	1
0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-32. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
SELREG	**0** LDO2 Voltage selected by LDO2_OP register **1** LDO2 Voltage selected by LDO2_AVS register
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.8 LDO3_AVS (17h)

Figure 7-53. LDO3_AVS(1); Register Address: 17h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	0	1	0	0	0	0
(1)	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0
0	0	1	1	1	1	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-33. Register Description

Field	Description
ENABLE	**0** LDO3 Disabled **1** LDO3 Enabled **(1)** LDO3 Enabled during automatic power-up sequence
ECO	**0** LDO3 is in normal mode **1** LDO3 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44

7.28.2.2.9 LDO3_LIMIT (18h)

Figure 7-54. LDO3_LIMIT(1); Register Address: 18h

7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
0	0	1	1	1	1	0	0
0	0	1	1	1	1	0	0
0	0	1	1	1	1	1	1
0	0	1	1	1	1	1	1
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-34. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
MAX_SEL[5:0]	defines the maximum value the output voltage can be programmed to for LDO3. Values exceeding this limit are ignored. Supply Voltage - setting shown in Table 7-44 If MAX_SEL is set to any other value than 0x00 or 0x3F, the register is set to read only; contact Ti for a default setting in OTP memory if needed.

7.28.2.2.10 LDO4_OP (19h)

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Figure 7-55. LDO4_OP(1); Register Address: 19h

7	6	5	4	3	2	1	0
RSVD	SELREG	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1 (internally fixed)	0	0	1	0	0
0	0	1 (internally fixed)	0	0	1	0	0
0	0	1 (internally fixed)	0	0	1	0	0
0	0	1 (internally fixed)	0	0	1	0	1
		OTP	OTP	OTP	OTP	OTP	OTP
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-35. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
SELREG	**0** LDO4 Voltage selected by LDO4_OP register **1** LDO4 Voltage selected by LDO4_AVS register
SEL[5:0]	Supply Voltage - setting shown in Table 7-45; SEL[5] is internaly set to 1 on LDO4 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

7.28.2.2.11 LDO4_AVS (1Ah)

Figure 7-56. LDO4_AVS(1); Register Address: 1Ah

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1 (internally fixed)	0	0	0	1	0
0	0	1 (internally fixed)	0	0	0	1	0
(1)	0	1 (internally fixed)	0	0	1	0	0
(1)	0	1 (internally fixed)	0	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-36. Register Description

Field	Description
ENABLE	**0** LDO4 Disabled **1** LDO4 Enabled **(1)** LDO4 Enabled during automatic power-up sequence
ECO	**0** LDO4 is in normal mode **1** LDO4 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-45; SEL[5] is internaly set to 1 on LDO4 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

7.28.2.2.12 LDO4_LIMIT (1Bh)

Figure 7-57. LDO4_LIMIT(1); Register Address: 1Bh

7	6	5	4	3	2	1	0
RSVD	RSVD	MAX_SEL[5]	MAX_SEL[4]	MAX_SEL[3]	MAX_SEL[2]	MAX_SEL[1]	MAX_SEL[0]
0	0	1 (internally fixed)	0	1	0	0	0
0	0	1 (internally fixed)	0	1	0	0	0
0	0	1 (internally fixed)	1	1	1	1	1
0	0	1 (internally fixed)	1	1	1	1	1
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-37. Register Description

Field	Description
RSVD	Unused Bit; should be written to 0
MAX_SEL[5:0]	Defines the maximum value the output voltage can be programmed to for LDO4_OP and LDO4_AVS. Values exceeding this limit are ignored. Supply Voltage - setting shown in Table 7-45. If MAX_SEL is set to any other value than 0x00 or 0x3F, the register is set to read only; contact Ti for a default setting in OTP memory if needed.

7.28.2.2.13 LDO5 (1Ch)

Figure 7-58. LDO5(1); Register Address: 1Ch

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1 (internally fixed)	1	0	1	1	0
0	0	1 (internally fixed)	1	0	1	1	0
0	0	1 (internally fixed)	0	0	1	0	0
(1)	0	1 (internally fixed)	0	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

(1) Register reset on Power On Reset (POR)

Table 7-38. Register Description

Field	Description
ENABLE	**0** LDO5 Disabled **1** LDO5 Enabled **(1)** LDO5 Enabled during automatic power-up sequence
ECO	**0** LDO5 is in normal mode **1** LDO5 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-45; SEL[5] is internaly set to 1 on LDO5 to reflect the programmable output voltage range from 1.6 V to 3.3 V.

7.28.2.2.14 LDO6 (1Dh)

Figure 7-59. LDO6(1); Register Address: 1Dh

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	0	0	1	0	0
0	0	1	0	0	1	0	0
(1)	0	0	0	0	0	0	0
(1)	0	1	0	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-39. Register Description

Field	Description
ENABLE	**0** LDO6 Disabled **1** LDO6 Enabled **(1)** LDO6 Enabled during automatic power-up sequence
ECO	**0** LDO6 is in normal mode **1** LDO6 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44.

7.28.2.2.15 LDO7 (1Eh)

Figure 7-60. LDO7(1); Register Address: 1Eh

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
0	0	1	1	1	1	0	0
0	0	1	1	1	1	0	0
0	0	1	0	0	1	0	0
(1)	0	1	0	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-40. Register Description

Field	Description
ENABLE	**0** LDO7 Disabled **1** LDO7 Enabled **(1)** LDO7 Enabled during automatic power-up sequence
ECO	**0** LDO7 is in normal mode **1** LDO7 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44.

7.28.2.2.16 LDO8 (1Fh)

Figure 7-61. LDO8(1); Register Address: 1Fh

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	1	1	1	0	1
(1)	0	1	1	1	1	0	1
0	0	1	0	0	1	0	0
(1)	0	1	1	1	0	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-41. Register Description

Field	Description
ENABLE	**0** LDO8 Disabled **1** LDO8 Enabled **(1)** LDO8 Enabled during automatic power-up sequence
ECO	**0** LDO8 is in normal mode **1** LDO8 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44.

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7.28.2.2.17 LDO9 (20h)

Figure 7-62. LDO9(1); Register Address: 20h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	1	1	1	0	0
(1)	0	1	1	1	1	0	0
(1)	0	1	1	1	1	1	1
(1)	0	1	0	0	1	0	1
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-42. Register Description

Field	Description
ENABLE	**0** LDO9 Disabled **1** LDO9 Enabled **(1)** LDO9 Enabled during automatic power-up sequence
ECO	**0** LDO9 is in normal mode **1** LDO9 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44.

7.28.2.2.18 LDO10 (21h)

Figure 7-63. LDO10(1); Register Address: 21h

7	6	5	4	3	2	1	0
ENABLE	ECO	SEL[5]	SEL[4]	SEL[3]	SEL[2]	SEL[1]	SEL[0]
(1)	0	1	0	0	1	0	0
(1)	0	1	0	0	1	0	0
0	0	0	1	0	0	0	0
(1)	0	1	1	1	1	0	0
OTP		OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-43. Register Description

Field	Description
ENABLE	**0** LDO10 Disabled **1** LDO10 Enabled **(1)** LDO10 Enabled during automatic power-up sequence
ECO	**0** LDO10 is in normal mode **1** LDO10 is in power save mode
SEL[5:0]	Supply Voltage - setting shown in Table 7-44.

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7.28.2.3 LDO Voltage Settings

Table 7-44. LDO Voltage Settings; Except LDO4 and LDO5

SEL[5:0]	LDOx Output (V)	SEL[5:0]	LDOx Output (V)
000000	0.800	100000	1.600
000001	0.825	100001	1.650
000010	0.850	100010	1.700
000011	0.875	100011	1.750
000100	0.900	100100	1.800
000101	0.925	100101	1.850
000110	0.950	100110	1.900
000111	0.975	100111	1.950
001000	1.000	101000	2.000
001001	1.025	101001	2.050
001010	1.050	101010	2.100
001011	1.075	101011	2.150
001100	1.100	101100	2.200
001101	1.125	101101	2.250
001110	1.150	101110	2.300
001111	1.175	101111	2.350
010000	1.200	110000	2.400
010001	1.225	110001	2.450
010010	1.250	110010	2.500
010011	1.275	110011	2.550
010100	1.300	110100	2.600
010101	1.325	110101	2.650
010110	1.350	110110	2.700
010111	1.375	110111	2.750
011000	1.400	111000	2.800
011001	1.425	111001	2.850
011010	1.450	111010	2.900
011011	1.475	111011	2.950
011100	1.500	111100	3.000
011101	1.525	111101	3.100
011110	1.550	111110	3.200
011111	1.575	111111	3.300

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Table 7-45. LDO Voltage Settings for LDO4 and LDO5

SEL[5:0]	LDOx Output (V)
100000	1.600
100001	1.650
100010	1.700
100011	1.750
100100	1.800
100101	1.850
100110	1.900
100111	1.950
101000	2.000
101001	2.050
101010	2.100
101011	2.150
101100	2.200
101101	2.250
101110	2.300
101111	2.350
110000	2.400
110001	2.450
110010	2.500
110011	2.550
110100	2.600
110101	2.650
110110	2.700
110111	2.750
111000	2.800
111001	2.850
111010	2.900
111011	2.950
111100	3.000
111101	3.100
111110	3.200
111111	3.300

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7.28.2.4 DEVCTRL Registers

Table 7-46. DEVCTRL Register Memory Map

Offset	Register Name	Section
22h	THRM_REG	THRM_REG (22h)
23h	CLK32KOUT	CLK32KOUT (23h)
24h	DEVCTRL	DEVCTRL (24h)
25h	DEVCTRL2	DEVCTRL2 (25h)
26h	I2C_SPI_CFG	I2C_SPI_CFG (26h)
27h	KEEP_ON1	KEEP_ON1 (27h)
28h	KEEP_ON2	KEEP_ON2 (28h)
29h	SET_OFF1	SET_OFF1 (29h)
2Ah	SET_OFF2	SET_OFF2 (2Ah)
(2Bh)	DEF_VOLT	DEF_VOLT (2Bh)
	LDO SLEEP MODE BEHAVIOR	LDO Sleep Mode Behavior
2Ch	DEF_VOLT_MAPPING	DEF_VOLT_MAPPING (2Ch)
2Dh	DISCHARGE1	DISCHARGE1 (2Dh)
2Eh	DISCHARGE2	DISCHARGE2 (2Eh)
2Fh	EN1_SET1	EN1_SET1 (2Fh)
30h	EN1_SET2	EN1_SET2 (30h)
31h	EN2_SET1	EN2_SET1 (31h)
32h	EN2_SET2	EN2_SET2 (32h)
33h	EN3_SET1	EN3_SET1 (33h)
34h	EN3_SET2	EN3_SET2 (34h)
35h	EN4_SET1	EN4_SET1 (35h)
36h	EN4_SET2	EN4_SET2 (36h)
37h	PGOOD	PGOOD (37h)
38h	PGOOD2	PGOOD2 (38h)
39h	INT_STS	INT_STS (39h)
3Ah	INT_MSK	INT_MSK (3Ah)
3Bh	INT_STS2	INT_STS2 (3Bh)
3Ch	INT_MSK2	INT_MSK2 (3Ch)
3Dh	INT_STS3	INT_STS3 (3Dh)
3Eh	INT_MSK3	INT_MSK3 (3Eh)
3Fh	INT_STS4	INT_STS4 (3Fh)
40h	INT_MSK4	INT_MSK4 (40h)
41h	GPIO1	GPIO1 (41h)
42h	GPIO2	GPIO2 (42h)
43h	GPIO3	GPIO3 (43h)
44h	GPIO4	GPIO4 (44h)
45h	GPIO5	GPIO5 (45h)
46h	VMON	VMON (46h)
47h	LEDA_CTRL1	LEDA_CTRL1 (47h)
48h	LEDA_CTRL2	LEDA_CTRL2 (48h)
49h	LEDA_CTRL3	LEDA_CTRL3 (49h)
4Ah	LEDA_CTRL4	LEDA_CTRL4 (4Ah)
4Bh	LEDA_CTRL5	LEDA_CTRL5 (4Bh)
4Ch	LEDA_CTRL6	LEDA_CTRL6 (4Ch)

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Table 7-46. DEVCTRL Register Memory Map (continued)

Offset	Register Name	Section
4Dh	LEDA_CTRL7	LEDA_CTRL7 (4Dh)
4Eh	LEDA_CTRL8	LEDA_CTRL8 (4Eh)
4Fh	LEDB_CTRL1	LEDB_CTRL1 (4Fh)
50h	LEDB_CTRL2	LEDB_CTRL2 (50h)
51h	LEDB_CTRL3	LEDB_CTRL3 (51h)
52h	LEDB_CTRL4	LEDB_CTRL4 (52h)
53h	LEDB_CTRL5	LEDB_CTRL5 (53h)
54h	LEDB_CTRL6	LEDB_CTRL6 (54h)
55h	LEDB_CTRL7	LEDB_CTRL7 (55h)
56h	LEDB_CTRL8	LEDB_CTRL8 (56h)
57h	LEDC_CTRL1	LEDC_CTRL1 (57h)
58h	LEDC_CTRL2	LEDC_CTRL2 (58h)
59h	LEDC_CTRL3	LEDC_CTRL3 (59h)
5Ah	LED_CTRL4	LED_CTRL4 (5Ah)
5Bh	LEDC_CTRL5	LEDC_CTRL5 (5Bh)
5Ch	LEDC_CTRL6	LEDC_CTRL6 (5Ch)
5Dh	LEDC_CTRL7	LEDC_CTRL7 (5Dh)
5Eh	LEDC_CTRL8	LEDC_CTRL8 (5Eh)
5Fh	LED_RAMP_UP_TIME	LED_RAMP_UP_TIME (5Fh)
60h	LED_RAMP_DOWN_TIME	LED_RAMP_DOWN_TIME (60h)
61h	LED_SEQ_EN	LED_SEQ_EN (61h)
	LEDx DC Current	LEDx DC Current
62h	LOADSWITCH	LOADSWITCH (62h)
63h	SPARE	SPARE (63h)
64h	VERNUM	VERNUM (64h)

7.28.2.4.1 THRM_REG (22h)

Figure 7-64. THRM_REG(1) ; Register Address: 22h

7	6	5	4	3	2	1	0
RSVD	RSVD	THERM_HD	THERM_TS	THERM_ HDSEL[1]	THERM_ HDSEL[0]	RSVD	THERM_EN
0	0	0	0	1	1	0	1
0	0	0	0	1	1	0	1
0	0	0	0	1	1	0	1
0	0	0	0	1	1	0	1
R	R	R	R	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-47. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
THERM_HD	**0** Hot die threshold is not reached **1** Hot threshold is reached
THERM_TS	**0** Thermal shutdown detector output - indicates thermal shutdown not reached (typically 150°C) **1** Thermal shutdown detector output - indicates thermal shutdown reached

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Table 7-47. Bit Field Descriptions (continued)

Field	Description
THERM_HDSEL	**00** Temperature selection for hot die detector: T = 117°C **01** Temperature selection for hot die detector: T = 121°C **10** Temperature selection for hot die detector: T = 125°C **11** Temperature selection for hot die detector: T = 130°C
THERM_EN	**0** Thermal shutdown module is disabled **1** Thermal shutdown module is enabled

7.28.2.4.2 CLK32KOUT (23h)

Figure 7-65. CLK32KOUT(1) ; Register Address: 23h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	CLK32KOUT_EN
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	(1)
R	R	R	R	R	R	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-48. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
CLK32KOUT_EN	**0** 32K CLK disabled **1** 32K CLK enabled **(1)** 32K CLK enabled during automatic power-up sequence

7.28.2.4.3 DEVCTRL (24h)

Figure 7-66. DEVCTRL(1) ; Register Address: 24h

7	6	5	4	3	2	1	0
PWR_OFF_SEQ	LOAD-OTP	LOCK_LDO9	RSVD	nRESPWRON_ OUTPUT	PWRHLD	DEV_SLP	DEV_OFF
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	0	1	0	0	0
0	1	0	0	0	0	0	0
OTP	OTP	OTP		OTP	OTP		
R/W	R/W	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-49. Bit Field Descriptions

Field	Description
PWR_OFF_SEQ	**0** All resources disabled at the same time **1** Power-off will be sequential, reverse of power-on sequence (first resource to power on will be the last to power off)
LOAD-OTP	**0** register contents are kept in OFF state **1** register default values are re-loaded from OTP when in OFF state
LOCK_LDO9	**0** LDO9 Bits are allowed to be changed **1** LDO9 Bits are locked; LDO9 is enabled in the startup sequence and disabled in OFF state; no further control allowed
RSVD	Unused bit read returns **0**
nRESPWRON_OUTPUT	**0** nRESPWRON output is open drain **1** nRESPWRON output is push-pull to VDDIO

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Table 7-49. Bit Field Descriptions (continued)

Field	Description
PWRHLD	**0** Cleared in OFF mode. **1** Write '1' will maintain the device on (ACTIVE or SLEEP device state) (if DEV_OFF=0 and DEV_OFF_RST=0).
DEV_SLP	**0** Write '0' will start an SLEEP to ACTIVE device state transition (wake-up event) (if DEV_OFF=0 and DEV_OFF_RST=0). This bit is cleared in OFF state. **1** Write '1' allows SLEEP device state (if DEV_OFF=0 and DEV_OFF_RST=0)
DEV_OFF	**0** This bit is cleared in OFF state. **1** Write '1' will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event).

7.28.2.4.4 DEVCTRL2 (25h)

Figure 7-67. DEVCTRL2(1) ; Register Address: 25h

7	6	5	4	3	2	1	0
SLEEP_ENABLE	INT_OUTPUT	TSLOT_ LENGTH[1]	TSLOT_ LENGTH[0]	SLEEP_POL	PWON_LP_OFF	PWON_LP_ OFF_RST	INT_POL
0	1	1	1	0	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	1	1	0
0	1	1	1	0	0	0	0
	OTP	OTP	OTP		OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-50. Bit Field Descriptions

Field	Description
SLEEP_ENABLE	**0** SLEEP signal is ignored; default for power-up **1** SLEEP is active and the input signal active state defined by SLEEP_POL
INT_OUTPUT	**0** interrupt output is open drain **1** interrupt output is push-pull to VDDIO
TSLOT_LENGTH[1,0]	Time slot duration programming; selects length of the timeslots for startup or shutdown timing **00** 30 µs **01** 200 µs **10** 500 µs **11** 2 ms
SLEEP_POL	**0** SLEEP signal active high **1** SLEEP signal active low
PWON_LP_OFF(1)	**0** No effect **1** Allows device turn-off after a nPWRON Long Press (signal low). After nPWRON=low for 4 s, an interrupt is generated and after 5 s, TPS65912 is set to OFF state
PWON_LP_OFF_RST(2)	**0** No effect **1** Allows device turn-off after a nPWRON Long Press (signal low). After nPWRON=low for 4s, an interrupt is generated and after 5 s, TPS65912 is set to OFF state; registers are loaded with their default values; priority over PWON_LP_OFF
INT_POL	**0** INT1 interrupt pad polarity control signal is active low **1** Is active high

(1) For TPS659121 with nPWRON configured as a active low reset input (nRESIN), the status of PWON_LP_OFF and PWON_LP_OFF_RST is DON´T CARE
(2) For TPS659121 with nPWRON configured as a active low reset input (nRESIN), the status of PWON_LP_OFF and PWON_LP_OFF_RST is DON´T CARE

7.28.2.4.5 I2C_SPI_CFG (26h)

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Figure 7-68. I2C_SPI_CFG(1) ; Register Address: 26h

7	6	5	4	3	2	1	0
I2CAVS_ID_SEL1	I2CAVS_ID_SEL0	I2CGP_ID_SEL1	I2CGP_ID_SEL0	DCDC4_AVS	DCDC3_AVS	DCDC2_AVS	DCDC1_AVS
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-51. Bit Field Descriptions

Field	Description
I2CAVS_ID_SEL[1,0]	**00** device address for the AVS-I2C interface is: 0010010 **01** device address for the AVS-I2C interface is: 0010011 **10** device address for the AVS-I2C interface is: 0010100 **11** device address for the AVS-I2C interface is: 0010101
I2CGP_ID_SEL1[1,0]	**00** device address for the standard-I2C interface is: 0101101 **01** device address for the standard-I2C interface is: 0101110 **10** device address for the standard-I2C interface is: 0101111 **11** device address for the standard-I2C interface is: 0110000
DCDC4_AVS	**0** DCDC4_OP and DCDC4_AVS registers are assigned to the standard interface **1** DCDC4_OP and DCDC4_AVS registera are assigned to the AVS- interface
DCDC3_AVS	**0** DCDC3_OP and DCDC3_AVS registers are assigned to the standard interface **1** DCDC3_OP and DCDC3_AVS registers are assigned to the AVS- interface
DCDC2_AVS	**0** DCDC2_OP and DCDC2_AVS registers are assigned to the standard interface **1** DCDC2_OP and DCDC2_AVS registers are assigned to the AVS- interface
DCDC1_AVS	**0** DCDC1_OP and DCDC1_AVS registers are assigned to the standard interface **1** DCDC1_OP and DCDC1_AVS registers are assigned to the AVS- interface

7.28.2.4.6 KEEP_ON1 (27h)

Figure 7-69. KEEP_ON1(1) ; Register Address: 27h(2)

7	6	5	4	3	2	1	0
LDO8_KEEPON	LDO7_KEEPON	LDO6_KEEPON	LDO5_KEEPON	LDO4_KEEPON	LDO3_KEEPON	LDO2_KEEPON	LDO1_KEEPON
1	1	1	0	0	1	1	0
1	1	1	0	0	1	1	0
0	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) Settings shown in Table 7-57

Table 7-52. Bit Field Descriptions

Field	Description
LDO8_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO7_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO6_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO5_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP

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Table 7-52. Bit Field Descriptions (continued)

Field	Description
LDO4_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO3_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO2_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO1_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP

7.28.2.4.7 KEEP_ON2 (28h)

Figure 7-70. KEEP_ON2(1) ; Register Address: 28h(2)

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_ KEEPON	DCDC3_ KEEPON	DCDC2_ KEEPON	DCDC1_ KEEPON	LDO10_ KEEPON	LDO9_ KEEPON
0	0	1	1	1	0	1	1
0	0	1	1	1	0	1	1
0	0	0	1	0	0	1	0
0	0	0	1	1	1	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) Settings shown in Table 7-57

Table 7-53. Bit Field Descriptions

Field	Description
DCDC4_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
DCDC3_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
DCDC2_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
DCDC1_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO10_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP
LDO9_KEEPON	**0** set in ECO mode in SLEEP **1** keep active in SLEEP

7.28.2.4.8 SET_OFF1 (29h)

Figure 7-71. SET_OFF1(1) ; Register Address: 29h(2)

7	6	5	4	3	2	1	0
LDO8_SET_OFF	LDO7_SET_OFF	LDO6_SET_OFF	LDO5_SET_OFF	LDO4_SET_OFF	LDO3_SET_OFF	LDO2_SET_OFF	LDO1_SET_OFF
0	0	0	1	1	0	0	1
0	0	0	1	1	0	0	1
0	0	0	1	1	0	1	0
0	0	0	0	0	1	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) Settings shown in Table 7-57

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Table 7-54. Bit Field Descriptions

Field	Description
LDO8_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO7_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO6_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO5_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO4_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO3_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO2_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO1_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0

7.28.2.4.9 SET_OFF2 (2Ah)

Figure 7-72. SET_OFF2(1) ; Register Address: 2Ah(2)

7	6	5	4	3	2	1	0
THERM_ KEEP_ON	CLK32KOUT_ KEEPON	DCDC4_ SET_OFF	DCDC3_ SET_OFF	DCDC2_ SET_OFF	DCDC1_ SET_OFF	LDO10_ SET_OFF	LDO9_ SET_OFF
0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0
0	1	0	0	0	0	0	0
0	0	1	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) Settings shown in Table 7-57

Table 7-55. Bit Field Descriptions

Field	Description
THERM_KEEP_ON	**0** enabled in SLEEP **1** set off in SLEEP
CLK32KOUT_KEEPON	**0** enabled in SLEEP **1** set off in SLEEP
DCDC4_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
DCDC3_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
DCDC2_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
DCDC1_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO10_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0
LDO9_SET_OFF	**0** defined by KEEP_ON register **1** set off in SLEEP if KEEP_ON bit set to 0

7.28.2.4.10 DEF_VOLT (2Bh)

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Figure 7-73. DEF_VOLT(1) ; Register Address: 2Bh(2)

7	6	5	4	3	2	1	0
LDO4_DEF_VOLT	LDO3_DEF_VOLT	LDO2_DEF_VOLT	LDO1_DEF_VOLT	DCDC4_DEF_VOLT	DCDC3_DEF_VOLT	DCDC2_DEF_VOLT	DCDC1_DEF_VOLT
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) Settings shown in Table 7-57

Table 7-56. Bit Field Descriptions

Field	Description
LDO4_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
LDO3_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
LDO2_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
LDO1_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
DCDC4_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
DCDC3_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
DCDC2_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register
DCDC1_DEF_VOLT	**0** output voltage defined by _OP register **1** output voltage defined by _AVS register

7.28.2.4.11 LDO Sleep Mode Behavior

Table 7-57. LDO SLEEP MODE BEHAVIOR

CONFIG BITS	LDO IS SET TO ECO MODE	LDO STAYS ACTIVE	LDO IS SET TO OFF
DEF_VOLT	0 = voltage defined by _OP register	0 = voltage defined by _OP register	0 = voltage defined by _OP register
	1 = voltage defined by _AVS register	1 = voltage defined by _AVS register	1 = voltage defined by _AVS register
KEEP ON	0	1	0
SET OFF	0	x	1

7.28.2.4.12 DEF_VOLT_MAPPING (2Ch)

Figure 7-74. DEF_VOLT_MAPPING(1) ; Register Address: 2Ch

7	6	5	4	3	2	1	0
LDO4_VOLT_ MAPPING[1]	LDO4_VOLT_ MAPPING[0]	LDO3_VOLT_ MAPPING[1]	LDO3_VOLT_ MAPPING[0]	LDO2_VOLT_ MAPPING[1]	LDO2_VOLT_ MAPPING[0]	LDO1_VOLT_ MAPPING[1]	LDO1_VOLT_ MAPPING[0]
0	1	0	1	0	0	0	0
0	1	0	1	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	1	1	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-58. Bit Field Descriptions

Field	Description
LDO4_VOLT MAPPING[1,0]	maps a DCDCx_SEL pin to the voltage scaling function to select either LDO4_OP or LDO4_AVS as the register defining the output voltage for LDO4 **00** = DEF_VOLT Bit set and cleared by status of DCDC1_SEL pin **01** = DEF_VOLT Bit set and cleared by status of DCDC2_SEL pin **10** = DEF_VOLT Bit set and cleared by status of DCDC3_SEL pin **11** = DEF_VOLT Bit set and cleared by status of DCDC4_SEL pin
LDO3_VOLT MAPPING[1,0]	maps a DCDCx_SEL pin to the voltage scaling function to select either LDO3_OP or LDO3_AVS as the register defining the output voltage for LDO3 **00** = DEF_VOLT Bit set and cleared by status of DCDC1_SEL pin **01** = DEF_VOLT Bit set and cleared by status of DCDC2_SEL pin **10** = DEF_VOLT Bit set and cleared by status of DCDC3_SEL pin **11** = DEF_VOLT Bit set and cleared by status of DCDC4_SEL pin
LDO2_VOLT MAPPING[1,0]	maps a DCDCx_SEL pin to the voltage scaling function to select either LDO2_OP or LDO2_AVS as the register defining the output voltage for LDO2 **00** = DEF_VOLT Bit set and cleared by status of DCDC1_SEL pin **01** = DEF_VOLT Bit set and cleared by status of DCDC2_SEL pin **10** = DEF_VOLT Bit set and cleared by status of DCDC3_SEL pin **11** = DEF_VOLT Bit set and cleared by status of DCDC4_SEL pin
LDO1_VOLT MAPPING[1,0]	maps a DCDCx_SEL pin to the voltage scaling function to select either LDO1_OP or LDO1_AVS as the register defining the output voltage for LDO1 **00** = DEF_VOLT Bit set and cleared by status of DCDC1_SEL pinv **01** = DEF_VOLT Bit set and cleared by status of DCDC2_SEL pin **10** = DEF_VOLT Bit set and cleared by status of DCDC3_SEL pin **11** = DEF_VOLT Bit set and cleared by status of DCDC4_SEL pin

7.28.2.4.13 DISCHARGE1 (2Dh)

Figure 7-75. DISCHARGE1(1) ; Register Address: 2Dh

7	6	5	4	3	2	1	0
LDO8_ DISCHARGE	LDO7_ DISCHARGE	LDO6_ DISCHARGE	LDO5_ DISCHARGE	LDO4_ DISCHARGE	LDO3_ DISCHARGE	LDO2_ DISCHARGE	LDO1_ DISCHARGE
0	1	1	0	0	0	0	0
0	1	1	0	0	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-59. Bit Field Descriptions

Field	Description
LDO8_DISCHARGE	**0** LDO8 output is not discharged when disabled **1** LDO8 output is discharged when disabled
LDO7_DISCHARGE	**0** LDO7 output is not discharged when disabled **1** LDO7 output is discharged when disabled
LDO6_DISCHARGE	**0** LDO6 output is not discharged when disabled **1** LDO6 output is discharged when disabled
LDO5_DISCHARGE	**0** LDO5 output is not discharged when disabled **1** LDO5 output is discharged when disabled
LDO4_DISCHARGE	**0** LDO4 output is not discharged when disabled **1** LDO4 output is discharged when disabled
LDO3_DISCHARGE	**0** LDO3 output is not discharged when disabled **1** LDO3 output is discharged when disabled
LDO2_DISCHARGE	**0** LDO2 output is not discharged when disabled **1** LDO2 output is discharged when disabled
LDO1_DISCHARGE	**0** LDO1 output is not discharged when disabled **1** LDO1 output is discharged when disabled

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7.28.2.4.14 DISCHARGE2 (2Eh)

Figure 7-76. DISCHARGE2(1) ; Register Address: 2Eh

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_ DISCHARGE	DCDC3_ DISCHARGE	DCDC2_ DISCHARGE	DCDC1_ DISCHARGE	LDO10_ DISCHARGE	LDO9_ DISCHARGE
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1
0	0	0	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-60. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
DCDC4_DISCHARGE	**0** DCDC4 output is not discharged when disabled **1** DCDC4 output is discharged when disabled
DCDC3_DISCHARGE	**0** DCDC3 output is not discharged when disabled **1** DCDC3 output is discharged when disabled
DCDC2_DISCHARGE	**0** DCDC2 output is not discharged when disabled **1** DCDC2 output is discharged when disabled
DCDC1_DISCHARGE	**0** DCDC1 output is not discharged when disabled **1** DCDC1 output is discharged when disabled
LDO10_DISCHARGE	**0** LDO10 output is not discharged when disabled **1** LDO10 output is discharged when disabled
LDO9_DISCHARGE	**0** LDO9 output is not discharged when disabled **1** LDO9 output is discharged when disabled

7.28.2.4.15 EN1_SET1 (2Fh)

Figure 7-77. EN1_SET1(1) ; Register Address: 2Fh

7	6	5	4	3	2	1	0
LDO8_EN1	LDO7_EN1	LDO6_EN1	LDO5_EN1	LDO4_EN1	LDO3_EN1	LDO2_EN1	LDO1_EN1
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-61. Bit Field Descriptions

Field	Description
LDO8_EN1	**0** EN1 pin has no effect on LDO8 enable **1** EN1 pin is controlling LDO8
LDO7_EN1	**0** EN1 pin has no effect on LDO7 enable **1** EN1 pin is controlling LDO7
LDO6_EN1	**0** EN1 pin has no effect on LDO6 enable **1** EN1 pin is controlling LDO6
LDO5_EN1	**0** EN1 pin has no effect on LDO5 enable **1** EN1 pin is controlling LDO5

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Table 7-61. Bit Field Descriptions (continued)

Field	Description
LDO4_EN1	**0** EN1 pin has no effect on LDO4 enable **1** EN1 pin is controlling LDO4
LDO3_EN1	**0** EN1 pin has no effect on LDO3 enable **1** EN1 pin is controlling LDO3
LDO2_EN1	**0** EN1 pin has no effect on LDO2 enable **1** EN1 pin is controlling LDO2
LDO1_EN1	**0** EN1 pin has no effect on LDO1 enable **1** EN1 pin is controlling LDO1

7.28.2.4.16 EN1_SET2 (30h)

Figure 7-78. EN1_SET2(1) ; Register Address: 30h

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_EN1	DCDC3_EN1	DCDC2_EN1	DCDC1_EN1	LDO10_EN1	LDO9_EN1
0	0	0	0	0	1	0	0
0	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-62. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
DCDC4_EN1	**0** EN1 pin has no effect on DCDC4 enable **1** EN1 pin is controlling DCDC4
DCDC3_EN1	**0** EN1 pin has no effect on DCDC3 enable **1** EN1 pin is controlling DCDC3
DCDC2_EN1	**0** EN1 pin has no effect on DCDC2 enable **1** EN1 pin is controlling DCDC2
DCDC1_EN1	**0** EN1 pin has no effect on DCDC1 enable **1** EN1 pin is controlling DCDC1
LDO10_EN1	**0** EN1 pin has no effect on LDO10 enable **1** EN1 pin is controlling LDO10
LDO9_EN1	**0** EN1 pin has no effect on LDO9 enable **1** EN1 pin is controlling LDO9

7.28.2.4.17 EN2_SET1 (31h)

Figure 7-79. EN2_SET1(1) ; Register Address: 31h

7	6	5	4	3	2	1	0
LDO8_EN2	LDO7_EN2	LDO6_EN2	LDO5_EN2	LDO4_EN2	LDO3_EN2	LDO2_EN2	LDO1_EN2
0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-63. Bit Field Descriptions

Field	Description
LDO8_EN2	**0** EN2 pin has no effect on LDO8 enable **1** EN2 pin is controlling LDO8
LDO7_EN2	**0** EN2 pin has no effect on LDO7 enable **1** EN2 pin is controlling LDO7
LDO6_EN2	**0** EN2 pin has no effect on LDO6 enable **1** EN2 pin is controlling LDO6
LDO5_EN2	**0** EN2 pin has no effect on LDO5 enable **1** EN2 pin is controlling LDO5
LDO4_EN2	**0** EN2 pin has no effect on LDO4 enable **1** EN2 pin is controlling LDO4
LDO3_EN2	**0** EN2 pin has no effect on LDO3 enable **1** EN2 pin is controlling LDO3
LDO2_EN2	**0** EN2 pin has no effect on LDO2 enable **1** EN2 pin is controlling LDO2
LDO1_EN2	**0** EN2 pin has no effect on LDO1 enable **1** EN2 pin is controlling LDO1

7.28.2.4.18 EN2_SET2 (32h)

Figure 7-80. EN2_SET2(1) ; Register Address: 32h

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_EN2	DCDC3_EN2	DCDC2_EN2	DCDC1_EN2	LDO10_EN2	LDO9_EN2
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-64. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
DCDC4_EN2	**0** EN2 pin has no effect on DCDC4 enable **1** EN2 pin is controlling DCDC4
DCDC3_EN2	**0** EN2 pin has no effect on DCDC3 enable **1** EN2 pin is controlling DCDC3
DCDC2_EN2	**0** EN2 pin has no effect on DCDC2 enable **1** EN2 pin is controlling DCDC2
DCDC1_EN2	**0** EN2 pin has no effect on DCDC1 enable **1** EN2 pin is controlling DCDC1
LDO10_EN2	**0** EN2 pin has no effect on LDO10 enable **1** EN2 pin is controlling LDO10
LDO9_EN2	**0** EN2 pin has no effect on LDO9 enable **1** EN2 pin is controlling LDO9

7.28.2.4.19 EN3_SET1 (33h)

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Figure 7-81. EN3_SET1(1) ; Register Address: 33h

7	6	5	4	3	2	1	0
LDO8_EN3	LDO7_EN3	LDO6_EN3	LDO5_EN3	LDO4_EN3	LDO3_EN3	LDO2_EN3	LDO1_EN3
0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	0	0	1	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-65. Bit Field Descriptions

Field	Description
LDO8_EN3	**0** EN3 pin has no effect on LDO8 enable **1** EN3 pin is controlling LDO8
LDO7_EN3	**0** EN3 pin has no effect on LDO7 enable **1** EN3 pin is controlling LDO7
LDO6_EN3	**0** EN3 pin has no effect on LDO6 enable **1** EN3 pin is controlling LDO6
LDO5_EN3	**0** EN3 pin has no effect on LDO5 enable **1** EN3 pin is controlling LDO5
LDO4_EN3	**0** EN3 pin has no effect on LDO4 enable **1** EN3 pin is controlling LDO4
LDO3_EN3	**0** EN3 pin has no effect on LDO3 enable **1** EN3 pin is controlling LDO3
LDO2_EN3	**0** EN3 pin has no effect on LDO2 enable **1** EN3 pin is controlling LDO2
LDO1_EN3	**0** EN3 pin has no effect on LDO1 enable **1** EN3 pin is controlling LDO1

7.28.2.4.20 EN3_SET2 (34h)

Figure 7-82. EN3_SET2(1) ; Register Address: 34h

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_EN3	DCDC3_EN3	DCDC2_EN3	DCDC1_EN3	LDO10_EN3	LDO9_EN3
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-66. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
DCDC4_EN3	**0** EN3 pin has no effect on DCDC4 enable **1** EN3 pin is controlling DCDC4
DCDC3_EN3	**0** EN3 pin has no effect on DCDC3 enable **1** EN3 pin is controlling DCDC3
DCDC2_EN3	**0** EN3 pin has no effect on DCDC2 enable **1** EN3 pin is controlling DCDC2
DCDC1_EN3	**0** EN3 pin has no effect on DCDC1 enable **1** EN3 pin is controlling DCDC1

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Table 7-66. Bit Field Descriptions (continued)

Field	Description
LDO10_EN3	**0** EN3 pin has no effect on LDO10 enable **1** EN3 pin is controlling LDO10
LDO9_EN3	**0** EN3 pin has no effect on LDO9 enable **1** EN3 pin is controlling LDO9

7.28.2.4.21 EN4_SET1 (35h)

Figure 7-83. EN4_SET1(1) ; Register Address: 35h

7	6	5	4	3	2	1	0
LDO8_EN4	LDO7_EN4	LDO6_EN4	LDO5_EN4	LDO4_EN4	LDO3_EN4	LDO2_EN4	LDO1_EN4
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-67. Bit Field Descriptions

Field	Description
LDO8_EN4	**0** EN4 pin has no effect on LDO8 enable **1** EN4 pin is controlling LDO8
LDO7_EN4	**0** EN4 pin has no effect on LDO7 enable **1** EN4 pin is controlling LDO7
LDO6_EN4	**0** EN4 pin has no effect on LDO6 enable **1** EN4 pin is controlling LDO6
LDO5_EN4	**0** EN4 pin has no effect on LDO5 enable **1** EN4 pin is controlling LDO5
LDO4_EN4	**0** EN4 pin has no effect on LDO4 enable **1** EN4 pin is controlling LDO4
LDO3_EN4	**0** EN4 pin has no effect on LDO3 enable **1** EN4 pin is controlling LDO3
LDO2_EN4	**0** EN4 pin has no effect on LDO2 enable **1** EN4 pin is controlling LDO2
LDO1_EN4	**0** EN4 pin has no effect on LDO1 enable **1** EN4 pin is controlling LDO1

7.28.2.4.22 EN4_SET2 (36h)

Figure 7-84. EN4_SET2(1) ; Register Address: 36h

7	6	5	4	3	2	1	0
RSVD	RSVD	DCDC4_EN4	DCDC3_EN4	DCDC2_EN4	DCDC1_EN4	LDO10_EN4	LDO9_EN4
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	0
		OTP	OTP	OTP	OTP	OTP	OTP
R	R	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-68. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
DCDC4_EN4	**0** EN4 pin has no effect on DCDC4 enable **1** EN4 pin is controlling DCDC4
DCDC3_EN4	**0** EN4 pin has no effect on DCDC3 enable **1** EN4 pin is controlling DCDC3
DCDC2_EN4	**0** EN4 pin has no effect on DCDC2 enable **1** EN4 pin is controlling DCDC2
DCDC1_EN4	**0** EN4 pin has no effect on DCDC1 enable **1** EN4 pin is controlling DCDC1
LDO10_EN4	**0** EN4 pin has no effect on LDO10 enable **1** EN4 pin is controlling LDO10
LDO9_EN4	**0** EN4 pin has no effect on LDO9 enable **1** EN4 pin is controlling LDO9

7.28.2.4.23 PGOOD (37h)

Figure 7-85. PGOOD(1) ; Register Address: 37h(2)

7	6	5	4	3	2	1	0
PGOOD_LDO4	PGOOD_LDO3	PGOOD_LDO2	PGOOD_LDO1	PGOOD_DCDC4	PGOOD_DCDC3	PGOOD_DCDC2	PGOOD_DCDC1
-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) The PGOOD_LDOx Bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V.

Table 7-69. Bit Field Descriptions

Field	Description
PGOOD_LDOx	the Bit is set or cleared by the power-good comparator in the LDO converter block **0** LDOx output voltage is below its target regulation voltage or disabled **1** LDOx output voltage is in regulation
PGOOD_DCDCx	the Bit is set or cleared by the power-good comparator in the DC-DC converter block **0** DCDCx output voltage is below its target regulation voltage or disabled **1** DCDCx output voltage is in regulation

7.28.2.4.24 PGOOD2 (38h)

Figure 7-86. PGOOD2(1) ; Register Address: 38h(2)

7	6	5	4	3	2	1	0
RSVD	RSVD	PGOOD_LDO10	PGOOD_LDO9	PGOOD_LDO8	PGOOD_LDO7	PGOOD_LDO6	PGOOD_LDO5
0	0	-	-	-	-	-	-
0	0	-	-	-	-	-	-
0	0	-	-	-	-	-	-
0	0	-	-	-	-	-	-
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) The PGOOD_LDOx Bit is not valid if the LDO is enabled but the supply voltage to the LDO is below 1 V.

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Table 7-70. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
PGOOD_LDOx	the Bit is set or cleared by the power-good comparator in the LDO converter block **0** LDOx output voltage is below its target regulation voltage or disabled **1** LDOx output voltage is in regulation

7.28.2.4.25 INT_STS (39h)

Figure 7-87. INT_STS(1) ; Register Address: 39h

7	6	5	4	3	2	1	0
GPIO1_F_IT	GPIO1_R_IT	HOTDIE_IT	PWRHOLD_R_IT	PWRON_LP_IT	PWRON_IT	VMON_IT	PWRHOLD_F_IT
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-71. Bit Field Descriptions

Field	Description
GPIO1_F_IT	**0** no falling edge occurred **1** GPIO1 falling edge detection interrupt status; write 1 to clear the interrupt flag
GPIO1_R_IT	**0** no rising edge occurred **1** GPIO1 rising edge detection interrupt status; write 1 to clear the interrupt flag
HOTDIE_IT	**0** no hot die event occurred **1** Hot die event interrupt status; write 1 to clear the interrupt flag
PWRHOLD_R_IT	**0** no rising edge on PWRHOLD detected **1** Rising PWRHOLD event interrupt status; write 1 to clear the interrupt flag
PWRON_LP_IT	**0** no nPWRON Long Press Key detected **1** nPWRON Long Press event interrupt status; write 1 to clear the interrupt flag
PWRON_IT	**0** no nPWRON event detected **1** nPWRON event interrupt status; write 1 to clear the interrupt flag
VMON_IT	**0** no VMON event detected **1** falling edge detection for VMON; voltage at VMON is below the VMON_SEL[1,0] threshold; no delay; write 1 to clear the interrupt flag
PWRHOLD_F_IT	**0** no PWRHOLD event detected **1** Falling PWRHOLD event interrupt status; write 1 to clear the interrupt flag

7.28.2.4.26 INT_MSK (3Ah)

Figure 7-88. INT_MSK(1) ; Register Address: 3Ah

7	6	5	4	3	2	1	0
GPIO1_F_ IT_MSK	GPIO1_R_ IT_MSK	HOTDIE_ IT_MSK	PWRHOLD_R_ IT_MSK	PWRON_LP_ IT_MSK	PWRON_ IT_MSK	VMON_ IT_MSK	PWRHOLD_F_ IT_MSK
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-72. Bit Field Descriptions

Field	Description
GPIO1_F_IT_MSK	**0** interrupt not masked **1** GPIO1 falling edge detection interrupt masked
GPIO1_R_IT_MSK	**0** interrupt not masked **1** GPIO1 rising edge detection interrupt masked
HOTDIE_IT_MSK	**0** interrupt not masked **1** Hot die event interrupt masked
PWRHOLD_R_IT_MSK	**0** interrupt not masked **1** Rising PWRHOLD event interrupt masked
PWRON_LP_IT_MSK	**0** interrupt not masked **1** nPWRON Long Press event interrupt masked
PWRON_IT_MSK	**0** interrupt not masked **1** nPWRON event interrupt masked
VMON_IT_MSK	**0** interrupt not masked **1** VMON event interrupt masked.
PWRHOLD_F_IT_MSK	**0** interrupt not masked **1** PWRHOLD falling edge event interrupt masked

7.28.2.4.27 INT_STS2 (3Bh)

Figure 7-89. INT_STS2(1) ; Register Address: 3Bh

7	6	5	4	3	2	1	0
GPIO5_F_IT	GPIO5_R_IT	GPIO4_F_IT	GPIO4_R_IT	GPIO3_F_IT	GPIO3_R_IT	GPIO2_F_IT	GPIO2_R_IT
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-73. Bit Field Descriptions

Field	Description
GPIO5_F_IT	**0** no falling edge occurred **1** GPIO5 falling edge detection interrupt status; write 1 to clear the interrupt flag
GPIO5_R_IT	**0** no rising edge occurred **1** GPIO5 rising edge detection interrupt status; write 1 to clear the interrupt flag
GPIO4_F_IT	**0** no falling edge occurred **1** GPIO4 falling edge detection interrupt status; write 1 to clear the interrupt flag
GPIO4_R_IT	**0** no rising edge occurred **1** GPIO4 rising edge detection interrupt status; write 1 to clear the interrupt flag
GPIO3_F_IT	**0** no falling edge occurred **1** GPIO3 falling edge detection interrupt status; write 1 to clear the interrupt flag
GPIO3_R_IT	**0** no rising edge occurred **1** GPIO3 rising edge detection interrupt status; write 1 to clear the interrupt flag
GPIO2_F_IT	**0** no falling edge occurred **1** GPIO2 falling edge detection interrupt status; write 1 to clear the interrupt flag
GPIO2_R_IT	**0** no rising edge occurred **1** GPIO2 rising edge detection interrupt status; write 1 to clear the interrupt flag

7.28.2.4.28 INT_MSK2 (3Ch)

Figure 7-90. INT_MSK2(1) ; Register Address: 3Ch

7	6	5	4	3	2	1	0
GPIO5_F_IT_MSK	GPIO5_R_IT_MSK	GPIO4_F_IT_MSK	GPIO4_R_IT_MSK	GPIO3_F_IT_MSK	GPIO3_R_IT_MSK	GPIO2_F_IT_MSK	GPIO2_R_IT_MSK
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-74. Bit Field Descriptions

Field	Description
GPIO5_F_IT_MSK	**0** interrupt not masked **1** GPIO5 falling edge detection interrupt masked
GPIO5_R_IT_MSK	**0** interrupt not masked **1** GPIO5 rising edge detection interrupt masked
GPIO4_F_IT_MSK	**0** interrupt not masked **1** GPIO4 falling edge detection interrupt masked
GPIO4_R_IT_MSK	**0** interrupt not masked **1** GPIO4 rising edge detection interrupt masked
GPIO3_F_IT_MSK	**0** interrupt not masked **1** GPIO3 falling edge detection interrupt masked
GPIO3_R_IT_MSK	**0** interrupt not masked **1** GPIO3 rising edge detection interrupt masked
GPIO2_F_IT_MSK	**0** interrupt not masked **1** GPIO2 falling edge detection interrupt masked
GPIO2_R_IT_MSK	**0** interrupt not masked **1** GPIO2 rising edge detection interrupt masked

7.28.2.4.29 INT_STS3 (3Dh)

Figure 7-91. INT_STS3(1) ; Register Address: 3Dh

7	6	5	4	3	2	1	0
PGOOD_LDO4_IT	PGOOD_LDO3_IT	PGOOD_LDO2_IT	PGOOD_LDO1_IT	PGOOD_DCDC4_IT	PGOOD_DCDC3_IT	PGOOD_DCDC2_IT	PGOOD_DCDC1_IT
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-75. Bit Field Descriptions

Field	Description
PGOOD_LDO4_IT	**0** no status change occurred **1** PGOOD_LDO4 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled; write 1 to clear the interrupt flag
PGOOD_LDO3_IT	**0** no status change occurred **1** PGOOD_LDO3 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled; write 1 to clear the interrupt flag
PGOOD_LDO2_IT	**0** no status change occurred **1** PGOOD_LDO2 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled; write 1 to clear the interrupt flag

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Table 7-75. Bit Field Descriptions (continued)

Field	Description
PGOOD_LDO1_IT	**0** no status change occurred **1** PGOOD_LDO1 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled; write 1 to clear the interrupt flag
PGOOD_DCDC4_IT	**0** no status change occurred **1** PGOOD_DCDC4 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the converter is disabled; write 1 to clear the interrupt flag
PGOOD_DCDC3_IT	**0** no status change occurred **1** PGOOD_DCDC3 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the converter is disabled; write 1 to clear the interrupt flag
PGOOD_DCDC2_IT	**0** no status change occurred **1** PGOOD_DCDC2 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the converter is disabled; write 1 to clear the interrupt flag
PGOOD_DCDC1_IT	**0** no status change occurred **1** PGOOD_DCDC1 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the converter is disabled; write 1 to clear the interrupt flag

7.28.2.4.30 INT_MSK3 (3Eh)

Figure 7-92. INT_MSK3(1) ; Register Address: 3Eh

7	6	5	4	3	2	1	0
PGOOD_LDO4_IT_MSK	PGOOD_LDO3_IT_MSK	PGOOD_LDO2_IT_MSK	PGOOD_LDO1_IT_MSK	PGOOD_DCDC4_IT_MSK	PGOOD_DCDC3_IT_MSK	PGOOD_DCDC2_IT_MSK	PGOOD_DCDC1_IT_MSK
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-76. Bit Field Descriptions

Field	Description
PGOOD_LDO4_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO4 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_LDO3_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO3 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_LDO2_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO2 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_LDO1_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO1 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_DCDC4_IT_MSK	**0** interrupt not masked **1** PGOOD_DCDC4 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_DCDC3_IT_MSK	**0** interrupt not masked **1** PGOOD_DCDC3 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_DCDC2_IT_MSK	**0** interrupt not masked **1** PGOOD_DCDC2 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled
PGOOD_DCDC1_IT_MSK	**0** interrupt not masked **1** PGOOD_DCDC1 falling edge detection interrupt status; masked by ENABLE, therefore not triggered if the output voltage drops when the LDO is disabled

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7.28.2.4.31 INT_STS4 (3Fh)

Figure 7-93. INT_STS4(1) ; Register Address: 3Fh

7	6	5	4	3	2	1	0
RSVD	RSVD	PGOOD_LDO10_IT	PGOOD_LDO9_IT	PGOOD_LDO8_IT	PGOOD_LDO7_IT	PGOOD_LDO6_IT	PGOOD_LDO5_IT
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-77. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
PGOOD_LDO10_IT	**0** no status change occurred **1** PGOOD_LDO10 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag
PGOOD_LDO9_IT	**0** no status change occurred **1** PGOOD_LDO9 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag
PGOOD_LDO8_IT	**0** no status change occurred **1** PGOOD_LDO8 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag
PGOOD_LDO7_IT	**0** no status change occurred **1** PGOOD_LDO7 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag
PGOOD_LDO6_IT	**0** no status change occurred **1** PGOOD_LDO6 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag
PGOOD_LDO5_IT	**0** no status change occurred **1** PGOOD_LDO5 falling or rising edge detection interrupt status; write 1 to clear the interrupt flag

7.28.2.4.32 INT_MSK4 (40h)

Figure 7-94. INT_MSK4(1) ; Register Address: 40h

7	6	5	4	3	2	1	0
RSVD	RSVD	PGOOD_LDO10_IT_MSK	PGOOD_LDO9_IT_MSK	PGOOD_LDO8_IT_MSK	PGOOD_LDO7_IT_MSK	PGOOD_LDO6_IT_MSK	PGOOD_LDO5_IT_MSK
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-78. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
PGOOD_LDO10_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO10 falling or rising edge detection interrupt masked
PGOOD_LDO9_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO9 falling or rising edge detection interrupt masked
PGOOD_LDO8_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO8 falling or rising edge detection interrupt masked
PGOOD_LDO7_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO7 falling or rising edge detection interrupt masked
PGOOD_LDO6_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO6 falling or rising edge detection interrupt masked

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Table 7-78. Bit Field Descriptions (continued)

Field	Description
PGOOD_LDO5_IT_MSK	**0** interrupt not masked **1** PGOOD_LDO5 falling or rising edge detection interrupt masked

7.28.2.4.33 GPIO1 (41h)

Figure 7-95. GPIO1(1) ; Register Address: 41h

7	6	5	4	3	2	1	0
GPIO_SLEEP	RSVD	RSVD	GPIO_DEB	RSVD	GPIO_CFG	GPIO_STS	GPIO_SET
0	0	0	0	0	0	x	0
0	0	0	0	0	0	x	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
OTP	-	-	OTP	-	OTP	-	OTP
R/W	R	R	R/W	R	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-79. Bit Field Descriptions

Field	Description
GPIO_SLEEP	**0** No impact, keep as in active mode **1** When in SLEEP and GPIO in output mode, force output low
RSVD	Unused bit read returns **0**
GPIO_DEB	**0** GPIO input debouncing time is 94 µs **1** GPIO input debouncing time is 156 µs
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

7.28.2.4.34 GPIO2 (42h)

Figure 7-96. GPIO2(1) ; Register Address: 42h

7	6	5	4	3	2	1	0
GPIO_SLEEP	RSVD	RSVD	GPIO_DEB	RSVD	GPIO_CFG	GPIO_STS	GPIO_SET
0	0	0	0	0	0	x	0
0	0	0	0	0	0	x	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
OTP	-	-	OTP	-	OTP	-	OTP
R/W	R	R	R/W	R	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-80. Bit Field Descriptions

Field	Description
GPIO_SLEEP	**0** No impact, keep as in active mode **1** When in SLEEP and GPIO in output mode, force output low
RSVD	Unused bit read returns **0**
GPIO_DEB	**0** GPIO input debouncing time is 94 µs **1** GPIO input debouncing time is 156 µs

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Table 7-80. Bit Field Descriptions (continued)

Field	Description
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

7.28.2.4.35 GPIO3 (43h)

Figure 7-97. GPIO3(1) ; Register Address: 43h

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
0	0	0	0	0	0	x	0
0	0	0	0	0	0	x	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
OTP	OTP	OTP	OTP	OTP	OTP	-	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-81. Bit Field Descriptions

Field	Description
GPIO_SLEEP	**0** No impact, keep as in active mode **1** When in SLEEP and GPIO in output mode, force output low
GPIO_SEL	**0** GPIO_SET to be available at GPIO when configured as output **1** LEDA out to be available at GPIO when configured as output
GPIO_ODEN	**0** Push-pull output mode, GPIO assigned to power-up sequence **1** Open drain output mode
GPIO_DEB	**0** GPIO input debouncing time is 94us **1** GPIO input debouncing time is 156us
GPIO_PDEN	**0** GPIO pad pulldown control - pulldown is disabled **1** GPIO pad pulldown control - pulldown is enabled
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

7.28.2.4.36 GPIO4 (44h)

Figure 7-98. GPIO4(1) ; Register Address: 44h

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
0	0	0	0	0	0	x	0
0	0	0	0	0	0	x	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
OTP	OTP	OTP	OTP	OTP	OTP	-	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-82. Bit Field Descriptions

Field	Description
GPIO_SLEEP	**0** No impact, keep as in active mode **1** When in SLEEP and GPIO in output mode, force output low
GPIO_SEL	**0** GPIO_SET to be available at GPIO when configured as output **1** LEDB out to be available at GPIO when configured as output
GPIO_ODEN	**0** Push-pull output mode, GPIO assigned to power-up sequence **1** Open drain output mode
GPIO_DEB	**0** GPIO input debouncing time is 94 µs **1** GPIO input debouncing time is 156 µs
GPIO_PDEN	**0** GPIO pad pulldown control - pulldown is disabled **1** GPIO pad pulldown control - pulldown is enabled
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

7.28.2.4.37 GPIO5 (45h)

Figure 7-99. GPIO5(1) ; Register Address: 45h

7	6	5	4	3	2	1	0
GPIO_SLEEP	GPIO_SEL	GPIO_ODEN	GPIO_DEB	GPIO_PDEN	GPIO_CFG	GPIO_STS	GPIO_SET
0	0	0	0	0	0	x	0
0	0	0	0	0	0	x	0
0	0	0	0	0	0	1	0
0	0	0	0	0	0	1	0
OTP	OTP	OTP	OTP	OTP	OTP	-	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-83. Bit Field Descriptions

Field	Description
GPIO_SLEEP	**0** No impact, keep as in active mode **1** When in SLEEP and GPIO in output mode, force output low
GPIO_SEL	**0** GPIO_SET to be available at GPIO when configured as output **1** LEDC out to be available at GPIO when configured as output
GPIO_ODEN	**0** Push-pull output mode, GPIO assigned to power-up sequence **1** Open drain output mode
GPIO_DEB	**0** GPIO input debouncing time is 94 µs **1** GPIO input debouncing time is 156 µs
GPIO_PDEN	**0** GPIO pad pulldown control - pulldown is disabled **1** GPIO pad pulldown control - pulldown is enabled
GPIO_CFG	**0** Configuration of the GPIO pad direction - the pad is configured as an input **1** The GPIO pad is configured as an output, GPIO assigned to power-up sequence
GPIO_STS	**0** Status of the GPIO pad **1** Status of the GPIO pad
GPIO_SET	**0** Value set to logic 1'b0 on the GPIO output when configured in output mode **1** Value set to logic 1'b1 on the GPIO output when configured in output mode

7.28.2.4.38 VMON (46h)

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Figure 7-100. VMON(1) ; Register Address: 46h

7	6	5	4	3	2	1	0
RSVD	VMON_DELAY[1]	VMON_DELAY[0]	VSUP_MASK	RSVD	VSUP_OUT	VMON_SEL[1]	VMON_SEL[0]
0	1	0	1	0	x	0	1
0	1	0	1	0	x	0	1
0	1	0	1	0	x	0	0
0	1	0	1	0	x	1	1
	OTP	OTP	OTP			OTP	OTP
R	R/W	R/W	R/W	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-84. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
VMON_DELAY[1:0]	delays the output signal at VSUP_OUT for a falling input voltage on the VMON_IN pin to allow an interrupt to be generated before VSUP_OUT goes low **00** no falling edge delay **01** 50 µs falling edge delay **10** 100 µs falling edge delay **11** 250 µs falling edge delay
VSUP_MASK	**0** The output of the voltage monitor is not used as a switch-off event **1** The output of the voltage monitor is used as a switch-off event
VSUP_OUT	status output of the voltage monitor: **0** The voltage at pin VCCS_VIN_MON is below the VMON threshold **1** The voltage at pin VCCS_VIN_MON is above the VMON threshold
VMON_SEL[1:0]	Battery voltage comparator threshold: **00** VMON threshold is 3.1 V (rising voltage) **01** VMON threshold is 2.9 V (rising voltage) **10** VMON threshold is 2.8 V (rising voltage) **11** VMON threshold is 2.7 V (rising voltage)

7.28.2.4.39 LEDA_CTRL1 (47h)

Figure 7-101. LEDA_CTRL1(1) ; Register Address: 47h

7	6	5	4	3	2	1	0
RSVD	RSVD	LEDA_RAMP_ENABLE	RSVD	LEDA_CURRENT[3]	LEDA_CURRENT[2]	LEDA_CURRENT[1]	LEDA_CURRENT[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R/W	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-85. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_RAMP_ENABLE	**0** no ramp **1** ramp enabled
LEDA_CURRENT[3:0]	LEDA dc current. See Table 7-112

7.28.2.4.40 LEDA_CTRL2 (48h)

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Figure 7-102. LEDA_CTRL2(1) ; Register Address: 48h

7	6	5	4	3	2	1	0
RSVD	LEDA_T1[6]	LEDA_T1[5]	LEDA_T1[4]	LEDA_T1[3]	LEDA_T1[2]	LEDA_T1[1]	LEDA_T1[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-86. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_T1[6:0]	LEDA T1 sequence length = LEDA_T1[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.41 LEDA_CTRL3 (49h)

Figure 7-103. LEDA_CTRL3(1) ; Register Address: 49h

7	6	5	4	3	2	1	0
RSVD	LEDA_T2[6]	LEDA_T2[5]	LEDA_T2[4]	LEDA_T2[3]	LEDA_T2[2]	LEDA_T2[1]	LEDA_T2[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-87. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_T2[6:0]	LEDA T2 sequence length = LEDA_T2[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.42 LEDA_CTRL4 (4Ah)

Figure 7-104. LEDA_CTRL4(1); Register Address: 4Ah

7	6	5	4	3	2	1	0
RSVD	LEDA_T3[6]	LEDA_T3[5]	LEDA_T3[4]	LEDA_T3[3]	LEDA_T3[2]	LEDA_T3[1]	LEDA_T3[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-88. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_T3[6:0]	LEDA T3 sequence length = LEDA_T3[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.43 LEDA_CTRL5 (4Bh)

Figure 7-105. LEDA_CTRL5(1); Register Address: 4Bh

7	6	5	4	3	2	1	0
RSVD	LEDA_T4[6]	LEDA_T4[5]	LEDA_T4[4]	LEDA_T4[3]	LEDA_T4[2]	LEDA_T4[1]	LEDA_T4[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-89. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_T4[6:0]	LEDA T4 sequence length = LEDA_T4[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.44 LEDA_CTRL6 (4Ch)

Figure 7-106. LEDA_CTRL6(1); Register Address: 4Ch

7	6	5	4	3	2	1	0
RSVD	LEDA_TP[6]	LEDA_TP[5]	LEDA_TP[4]	LEDA_TP[3]	LEDA_TP[2]	LEDA_TP[1]	LEDA_TP[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-90. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_TP[6:0]	LEDA TP sequence length = LEDA_TP[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.45 LEDA_CTRL7 (4Dh)

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Figure 7-107. LEDA_CTRL7(1); Register Address: 4Dh

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDA_PWM[4]	LEDA_PWM[3]	LEDA_PWM[2]	LEDA_PWM[1]	LEDA_PWM[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-91. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_PWM[6:0]	LEDA_ON duty-cycle: ([LEDA_PWM] +1) × 1 / 32 x 8 ms period 00000 = 1 / 2 x 8 ms (LEDA_ON is high for 250 µs, low for 7.75 ms) 11111 = 32 / 32 x 8 ms (LEDA_ON is always high)

7.28.2.4.46 LEDA_CTRL8 (4Eh)

Figure 7-108. LEDA_CTRL8(1); Register Address: 4Eh

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDA_ON_TIME[4]	LEDA_ON_TIME[3]	LEDA_ON_TIME[2]	LEDA_ON_TIME[1]	LEDA_ON_TIME[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-92. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_ON_TIME[4:0]	LEDA ON-TIME: LEDA_ON_TME[4:0] x 64 ms 00000 = 0 x 64 ms 11111 = 31 x 64 ms

7.28.2.4.47 LEDB_CTRL1 (4Fh)

Figure 7-109. LEDB_CTRL1(1); Register Address: 4Fh

7	6	5	4	3	2	1	0
RSVD	RSVD	LEDB_RAMP_ ENABLE	RSVD	LEDB_CURRENT[3]	LEDB_CURRENT[2]	LEDB_CURRENT[1]	LEDB_CURRENT[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R/W	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-93. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_RAMP_ENABLE	**0** no ramp **1** ramp enabled
LEDBA_CURRENT[3:0]	LEDB dc current. See Table 7-112

7.28.2.4.48 LEDB_CTRL2 (50h)

Figure 7-110. LEDB_CTRL2(1); Register Address: 50h

7	6	5	4	3	2	1	0
RSVD	LEDB_T1[6]	LEDB_T1[5]	LEDB_T1[4]	LEDB_T1[3]	LEDB_T1[2]	LEDB_T1[1]	LEDB_T1[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-94. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_T1[6:0]	LEDB T1 sequence length = LEDB_T1[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.49 LEDB_CTRL3 (51h)

Figure 7-111. LEDB_CTRL3(1); Register Address: 51h

7	6	5	4	3	2	1	0
RSVD	LEDB_T2[6]	LEDB_T2[5]	LEDB_T2[4]	LEDB_T2[3]	LEDB_T2[2]	LEDB_T2[1]	LEDB_T2[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-95. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_T2[6:0]	LEDB T2 sequence length = LEDB_T2[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.50 LEDB_CTRL4 (52h)

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Figure 7-112. LEDB_CTRL4(1); Register Address: 52h

7	6	5	4	3	2	1	0
RSVD	LEDB_T3[6]	LEDB_T3[5]	LEDB_T3[4]	LEDB_T3[3]	LEDB_T3[2]	LEDB_T3[1]	LEDB_T3[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-96. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_T3[6:0]	LEDB T3 sequence length = LEDB_T3[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.51 LEDB_CTRL5 (53h)

Figure 7-113. LEDB_CTRL5(1); Register Address: 53h

7	6	5	4	3	2	1	0
RSVD	LEDB_T4[6]	LEDB_T4[5]	LEDB_T4[4]	LEDB_T4[3]	LEDB_T4[2]	LEDB_T4[1]	LEDB_T4[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-97. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_T4[6:0]	LEDB T4 sequence length = LEDB_T4[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.52 LEDB_CTRL6 (54h)

Figure 7-114. LEDB_CTRL6(1); Register Address: 54h

7	6	5	4	3	2	1	0
RSVD	LEDB_TP[6]	LEDB_TP[5]	LEDB_TP[4]	LEDB_TP[3]	LEDB_TP[2]	LEDB_TP[1]	LEDB_TP[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-98. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_TP[6:0]	LEDB TP sequence length = LEDB_TP[6:0] x 64ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.53 LEDB_CTRL7 (55h)

Figure 7-115. LEDB_CTRL7(1); Register Address: 55h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDB_PWM[4]	LEDB_PWM[3]	LEDB_PWM[2]	LEDB_PWM[1]	LEDB_PWM[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-99. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_PWM[6:0]	LEDB_ON duty-cycle: ([LEDB_PWM] +1) x 1 / 32 x 8 ms period 00000 = 1 / 32 x 8 ms (LEDB_ON is high for 250 µs, low for 7.75 ms) 11111 = 32 / 32 x 8 ms (LEDB_ON is always high)

7.28.2.4.54 LEDB_CTRL8 (56h)

Figure 7-116. LEDB_CTRL8(1); Register Address: 56h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDB_ON_TIME[4]	LEDB_ON_TIME[3]	LEDB_ON_TIME[2]	LEDB_ON_TIME[1]	LEDB_ON_TIME[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-100. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDB_ON_TIME[4:0]	LEDB ON-TIME: LEDB_ON_TME[4:0] x 64 ms 00000 = 0 x 64 ms 11111 = 31 x 64 ms

7.28.2.4.55 LEDC_CTRL1 (57h)

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Figure 7-117. LEDC_CTRL1(1) ; Register Address: 57h

7	6	5	4	3	2	1	0
RSVD	RSVD	LEDC_RAMP_ENABLE	RSVD	LEDC_CURRENT[3]	LEDC_CURRENT[2]	LEDC_CURRENT[1]	LEDC_CURRENT[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R/W	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-101. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_RAMP_ENABLE	**0** no ramp **1** ramp enabled
LEDCA_CURRENT[3:0]	LEDC dc current. See Table 7-112

7.28.2.4.56 LEDC_CTRL2 (58h)

Figure 7-118. LEDC_CTRL2(1) ; Register Address: 58h

7	6	5	4	3	2	1	0
RSVD	LEDC_T1[6]	LEDC_T1[5]	LEDC_T1[4]	LEDC_T1[3]	LEDC_T1[2]	LEDC_T1[1]	LEDC_T1[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-102. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_T1[6:0]	LEDC T1 sequence length = LEDC_T1[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.57 LEDC_CTRL3 (59h)

Figure 7-119. LEDC_CTRL3(1) ; Register Address: 59h

7	6	5	4	3	2	1	0
RSVD	LEDC_T2[6]	LEDC_T2[5]	LEDC_T2[4]	LEDC_T2[3]	LEDC_T2[2]	LEDC_T2[1]	LEDC_T2[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-103. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_T2[6:0]	LEDC T2 sequence length = LEDC_T2[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.58 LED_CTRL4 (5Ah)

Figure 7-120. LED_CTRL4(1) ; Register Address: 5Ah

7	6	5	4	3	2	1	0
RSVD	LEDC_T3[6]	LEDC_T3[5]	LEDC_T3[4]	LEDC_T3[3]	LEDC_T3[2]	LEDC_T3[1]	LEDC_T3[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-104. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_T3[6:0]	LEDC T3 sequence length = LEDC_T3[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.59 LEDC_CTRL5 (5Bh)

Figure 7-121. LEDC_CTRL5(1) ; Register Address: 5Bh

7	6	5	4	3	2	1	0
RSVD	LEDC_T4[6]	LEDC_T4[5]	LEDC_T4[4]	LEDC_T4[3]	LEDC_T4[2]	LEDC_T4[1]	LEDC_T4[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-105. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_T4[6:0]	LEDC T4 sequence length = LEDC_T4[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.60 LEDC_CTRL6 (5Ch)

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Figure 7-122. LEDC_CTRL6(1) ; Register Address: 5Ch

7	6	5	4	3	2	1	0
RSVD	LEDC_TP[6]	LEDC_TP[5]	LEDC_TP[4]	LEDC_TP[3]	LEDC_TP[2]	LEDC_TP[1]	LEDC_TP[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-106. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_TP[6:0]	LEDC TP sequence length = LEDC_TP[6:0] x 64 ms 0000000 = 0 x 64 ms 1111111 = 127 x 64 ms

7.28.2.4.61 LEDC_CTRL7 (5Dh)

Figure 7-123. LEDC_CTRL7(1) ; Register Address: 5Dh

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDC_PWM[4]	LEDC_PWM[3]	LEDC_PWM[2]	LEDC_PWM[1]	LEDC_PWM[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-107. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_PWM[6:0]	LEDC_ON duty-cycle: ([LEDC_PWM] +1) x 1 / 32 x 8 ms period 00000 = 1 / 32 x 8 ms (LEDC_ON is high for 250 µs, low for 7.75 ms) 11111 = 32 / 32 x 8 ms (LEDC_ON is always high)

7.28.2.4.62 LEDC_CTRL8 (5Eh)

Figure 7-124. LEDC_CTRL8(1) ; Register Address: 5Eh

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LEDC_ON_TIME[4]	LEDC_ON_TIME[3]	LEDC_ON_TIME[2]	LEDC_ON_TIME[1]	LEDC_ON_TIME[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

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Table 7-108. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDC_ON_TIME[4:0]	LEDC ON-TIME: LEDC_ON_TME[4:0] x 64 ms 00000 = 0 x 64 ms 11111 = 31 x 64 ms

7.28.2.4.63 LED_RAMP_UP_TIME (5Fh)

Figure 7-125. LED_RAMP_UP_TIME(1) ; Register Address: 5Fh

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LED_RAMP_UP[4]	LED_RAMP_UP[3]	LED_RAMP_UP[2]	LED_RAMP_UP[1]	LED_RAMP_UP[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-109. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LED_RAMP_UP[4:0]	LED ramp up time for LEDA, LEDB and LEDC: LED_RAMP_UP[4:0] x 8 ms 00000 = 0 x 8 ms 11111 = 31 x 8 ms

7.28.2.4.64 LED_RAMP_DOWN_TIME (60h)

Figure 7-126. LED_RAMP_DOWN_TIME(1) ; Register Address: 60h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	LED_RAMP_ DOWN[4]	LED_RAMP_ DOWN[3]	LED_RAMP_ DOWN[2]	LED_RAMP_ DOWN[1]	LED_RAMP_ DOWN[0]
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R	R	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-110. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LED_RAMP_DOWN[4:0]	LED ramp down time for LEDA, LEDB and LEDC: LED_RAMP_DOWN[4:0] x 8 ms 00000 = 0 x 8 ms 11111 = 31 x 8 ms

7.28.2.4.65 LED_SEQ_EN (61h)

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Figure 7-127. LED_SEQ_EN(1) ; Register Address: 61h

7	6	5	4	3	2	1	0
RSVD	LEDA_EN	LEDB_EN	LEDC_EN	RSVD	LEDA_SEQ_EN	LEDB_SEQ_EN	LEDC_SEQ_EN
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
R	R/W	R/W	R/W	R	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-111. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
LEDA_EN	**0** LEDA is disabled **1** LEDA is enabled
LEDB_EN	**0** LEDB is disabled **1** LEDB is enabled
LEDC_EN	**0** LEDC is disabled **1** LEDC is enabled
LEDA_SEQ_EN	**0** LEDA sequencer is disabled **1** LEDA sequencer is enabled
LEDB_SEQ_EN	**0** LEDB sequencer is disabled **1** LEDB sequencer is enabled
LEDC_SEQ_EN	**0** LEDC sequencer is disabled **1** LEDC sequencer is enabled

7.28.2.4.66 LEDx DC Current

Table 7-112. LEDx DC Current

LEDx_CURRENT[3:0]	LED CURRENT / mA
0000	2
0001	4
0010	6
0011	8
0100	10
0101	12
0110	14
0111	16
1000	18
1001	20
1010 to 1111	20

7.28.2.4.67 LOADSWITCH (62h)

Figure 7-128. LOADSWITCH(1) ; Register Address: 62h

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	ILIM[1]	ILIM[0]	ENABLE[1]	ENABLE[0]
0	0	0	0	0	1	x	x
0	0	0	0	0	1	x	x
0	0	0	0	1	0	x	x
0	0	0	0	1	1	x	x
				OTP	OTP	pin EN_LS1	pin EN_LS0
R	R	R	R	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-113. Bit Field Descriptions

Field	Description
RSVD	Unused bit read returns **0**
ENABLE[1,0]	**00:** load switch is OFF **01:** load switch is forced ON **10:** load switch in bypass switch operation: It is automatically enabled by comparators in DCDC4; forced PWM mode of DCDC4 is blocked and the bypass switch is disabled (ENABLE[1,0] is set = "00") if the voltage on pin VDCDC4 exceeds typically 4.18 V **11:** load switch in bypass switch operation: Switch is forced ON; forced PWM mode of DCDC4 is blocked and the bypass switch is disabled (ENABLE[1,0] is set = "00") if the voltage on pin VDCDC4 exceeds typically 4.18 V
ILIM[1,0]	**00:** current limit is 100mA maximum **01:** current limit is 500 mA maximum **10:** current limit is 750 mA ±10% **11:** current limit is 2.5 A ±20%

7.28.2.4.68 SPARE (63h)

Figure 7-129. SPARE(1) ; Register Address: 63h(2) (3)

7	6	5	4	3	2	1	0
SPARE	SPARE	SPARE	SPARE	9MHZ OSC OFF	DCDC4_ SEL DELAY	DCDC4_ IMMEDIATE	CLK32k_ OD_EN
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -*n* = value after reset

(1) Register reset on Power On Reset (POR)
(2) **Register Bits B0 and B1 defined in the SPARE register are new functions available in Rev 1.1 of silicon from July 2011**
(3) **Register Bits B2 and B3 defined in the SPARE register are new functions available in Rev 1.4 of silicon from May 2012**

Table 7-114. Bit Field Descriptions

Field	Description
SPARE	Unused bit read returns **0**
CLK32k_OD_EN	**0** 32K clock output is configured as a push-pull output to VDDIO **1** 32K clock output is configured as an open drain output
DCDC4_IMMEDIATE	**0** a voltage change in registers DCDC4_OP or DCDC4_AVS is done with the slew rate defined in DCDC4_CTRL:TSTEP[2:0] **1** a voltage change in registers DCDC4_OP or DCDC4_AVS is done immediately without limiting it by the slew rate control
DCDC4_SEL DELAY	**0** DELAY is 0.5...1.5 x 1 / 32 kHz for a falling output voltage (default for all revisions) **1** NO DELAY on DCDC4_SEL; this option is only available in Rev 1.4

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Table 7-114. Bit Field Descriptions (continued)

Field	Description
9 MHz OSC OFF	**0** 9 MHz oscillator continuously enabled in ON state - available for Rev 1.4 and higher; please leave this bit at 0 on all versions other than TPS659121 **1** 9 MHz oscillator is disabled based on PWR_REQ and CLK_REQ1 pins as listed below: PWR_REQ=0, CLK_REQ1=0 oscillator OFF PWR_REQ=0, CLK_REQ1=1 oscillator ON PWR_REQ=1, CLK_REQ1=0 oscillator ON PWR_REQ=1, CLK_REQ1=1 oscillator ON

7.28.2.4.69 VERNUM (64h)

Figure 7-130. VERNUM(1) ; Register Address: 64h

7	6	5	4	3	2	1	0
VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM	VERNUM
0	0	0	0	0	1	0	1
0	0	0	1	0	1	0	1
0	0	0	0	0	0	1	1
0	0	0	0	0	0	1	1
OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; *-n* = value after reset

(1) Register reset on Power On Reset (POR)

Table 7-115. Bit Field Descriptions

Field	Description
VERNUM	Value depending on silicon revision 0x00 - Revision 1.0 0x01 - Revision 1.1 0x02 - Revision 1.2 0x03 - Revision 1.3 0x04 - Revision 1.4 0x05 - Revision 1.5

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8 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65912 device is an integrated power-management integrated circuit (PMIC) that comes in an 81-pin, 0.4-mm pitch, DSBGA package. This device was designed for personal electronic, industrial, and communication applications and is dedicated to designs powered from a 5-V input supply that require multiple power rails. The device provides four step-down converters along with an interface to control ten external LDO regulators. The device can support a variety of different processors and applications. The step-down converters can also support dynamic voltage scaling through a dedicated I2C interface to provide optimum power savings. In addition to the power resources, the device contains an embedded power controller (EPC) to manage the power sequencing requirements of systems. The power sequencing is programmable through OTP. The device also contains five configurable GPIOs, a real-time clock module, and three LED outputs. The following sections provide the typical application use-case with the recommended external components and layout guidelines.

8.2 Typical Application

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8.2.1 DC-DC Converters

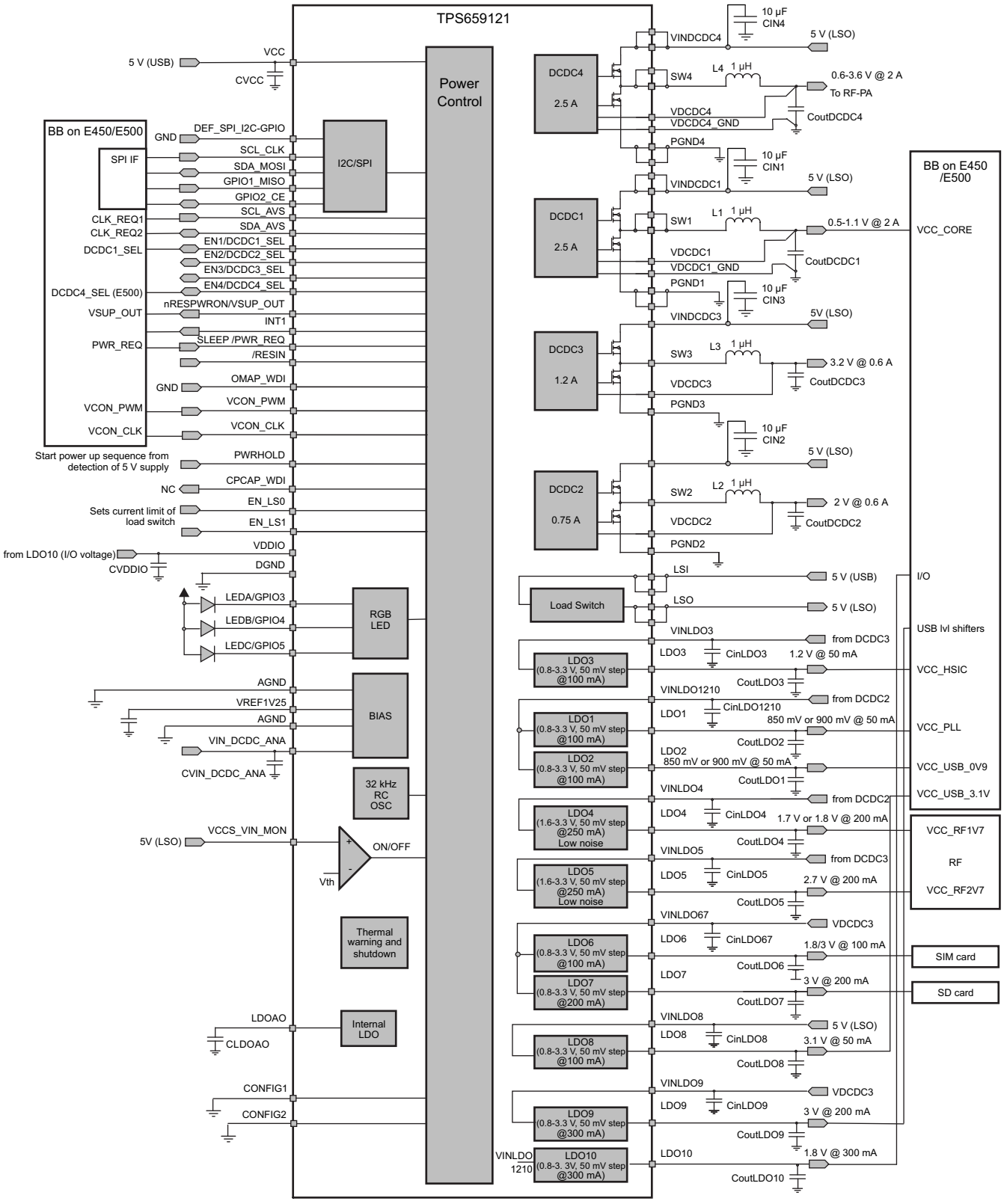

Figure 8-1. 5-V USB Host Connections for E450 and E500 Platforms

8.2.1.1 Design Requirements

For a typical application shown in Figure 8-1, Table 8-1 lists the key design parameters of the power resources.

Table 8-1. Design Parameters

DESIGN PARAMETER	VALUE
Supply voltage	2.7 V to 5.5 V
Switching frequency	Up to 3.5 MHz
DCDC1 voltage	1.1 V
DCDC1 current	Up to 2.5 A
DCDC2 voltage	2.0 V
DCDC2 current	Up to 0.75 A
DCDC3 voltage	3.2 V
DCDC3 current	Up to 1.6 A
DCDC4 voltage	3.6 V
DCDC4 current	Up to 2.5 A
LDO1 voltage	850 mV or 900 mV
LDO1 current	Up to 100 mA
LDO2 voltage	850 mV or 900 mV
LDO2 current	Up to 100 mA
LDO3 voltage	1.2 V
LDO3 current	Up to 100 mA
LDO4 voltage	1.7 V or 1.8 V
LDO4 current	Up to 250 mA
LDO5 voltage	2.7 V
LDO5 current	Up to 250 mA
LDO6 voltage	1.8 V or 3.0 V
LDO6 current	Up to 100 mA
LDO7 voltage	3.0 V
LDO7 current	Up to 200 mA
LDO8 voltage	3.1 V
LDO8 current	Up to 100 mA
LDO9 voltage	3.0 V
LDO9 current	Up to 300 mA
LDO10 voltage	1.8 V
LDO10 current	Up to 300 mA

8.2.1.2 Detailed Design Procedure

Table 8-2 lists the recommended external components.

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Table 8-2. Recommended External Components

REFERENCE COMPONENTS	COMPONENT(1)	MANUFACTURER	PART NUMBER	VALUE	EIA SIZE CODE(2)	SIZE (mm)	MASS PRODUCTION(3)
INPUT POWER SUPPLIES EXTERNAL COMPONENTS							
CVCC, CVIN_DCDC_ANA, LDOAO	Power input capacitors	Murata	GRM188R71A225KE15	2.2 µF, 10V	0603	1.6 × 0.8 × 0.8	Available(4)
CVDDIO	I/O input capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available(4)
RGB LED EXTERNAL COMPONENTS							
LEDA	Yellow LED	Lite On	LTST-C190YKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (4)
LEDB	Green LED	Lite On	LTST-C190GKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (4)
LEDC	Red LED	Lite On	LTST-C190CKT	20mA, 2.1 V	0603	1.6 × 0.8 × 0.8	Available (4)
DCDC EXTERNAL COMPONENTS							
CIN1, CIN2, CIN3, CIN4	Input capacitor	Murata	GRM188R60J106ME47	10 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available (4)
CoutDCDC1, CoutDCDC4	Output capacitor	Murata	GCM32ER70J476KE19 (Two capacitors per rail)	10 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available (4)
CoutDCDC2, CoutDCDC3	Output capacitor	Murata	GRM188R60J106ME47	10 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available (4)
L1, L2, L3, L4	Inductor	Toko	1239AS-H-1R0N=P2	1 µH		2 × 2.5	Available(4)
LDO EXTERNAL COMPONENTS							
CinLDO1210, CinLDO3, CinLDO67, CinLDO8, CinLDO9	Input capacitor	Murata	GRM188R71A225KE15	2.2 µF, 10V	0603	1.6 × 0.8 × 0.8	Available(4)
CinLDO4, CinLDO5	Input capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available(4)
CoutLDO3, CoutLDO1, CoutLDO2, CoutLDO6, CoutLDO7, CoutLDO8, CoutLDO9, CoutLDO10	Output capacitor	Murata	GRM188R71A225KE15	2.2 µF, 10V	0603	1.6 × 0.8 × 0.8	Available(4)
CoutLDO4, CoutLDO5	Output capacitor	Murata	GRM188R60J475KE19	4.7 µF, 6.3V	0603	1.6 × 0.8 × 0.8	Available(4)

(1) Component minimum and maximum tolerance values are specified in the electrical parameters section of each IP.
(2) The PACK column describes the external component package type.
(3) This column refers to the criteria.
(4) Component used on the validation boards.

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8.2.1.2.1 Output Filter Design (Inductor and Output Capacitor)

8.2.1.2.1.1 Inductor Selection

The step-down converters are designed to operate with small external components such as 1-µH output inductors. The values given under the recommended operating conditions include tolerances and saturation effects and must not be violated for stable operation. The selected inductor must be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 2 can be used to calculate the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 2. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \quad (2)$$

where

- ΔI_L = Peak-to-peak inductor ripple current
- L = Inductor value
- f = Switching frequency

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \quad (3)$$

where

- I_{Lmax} = Maximum inductor current

The highest inductor current will occur at maximum V_{in}.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Refer to Table 8-3 and the typical applications for possible inductors.

Table 8-3. Tested Inductors

INDUCTOR TYPE	NOMINAL INDUCTANCE	SUPPLIER
DFE252012	1 µH	Toko
DFE322510	1 µH	Toko
DFE322512	1 µH	Toko
VLS201612ET-1R0	1 µH	TDK
SPM3012T-1R0	1 µH	TDK

8.2.1.2.1.2 Output Capacitor Selection

The control scheme of the DC-DC converters allow the use of small ceramic capacitors with a typical value as given in the recommended operating conditions, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended.

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If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as shown in Equation 4.

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (4)$$

At nominal load current, the inductive converters operate in PWM mode and the overall output-voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor. See Equation 5.

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (5)$$

Where the highest output voltage ripple occurs at the highest input voltage, V_{in}.

At light load currents, the converters operate in Power Save Mode and the output voltage ripple is dependent on the value of the output capacitor. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

8.2.1.2.1.3 Input Capacitor Selection / Input Voltage

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input-voltage spikes. The converters need a ceramic input capacitor of 10 µF. The input capacitor can be increased without any limit for better input voltage filtering. Ceramic capacitors suffer from the so-called *dc bias effect*. A dc voltage applied at a ceramic capacitor will change the effective capacitance to a value lower than the nominal value. Curves about that behavior are available at the capacitor manufacturers and need to be considered when using the capacitors in applications where a dc voltage is applied and a minimum capacitance must be maintained for proper functionality of the circuit. The values given in the *Recommended operating Conditions* for TPS65912x are for the capacitance. The actual capacitor used may have a larger nominal value that drops with the voltage applied to what is recommended. The capacitance drop depends on the voltage applied, so for a higher voltage; for example, the output voltage of a DC-DC converter or LDO, this must be considered when choosing a proper capacitor.

The input voltage for the step-down converters must be connected to pin VINDCDC1, VINDCDC2, VINDCDC3 and VINDCDC4. These pins need to be tied together with VIN_DCDC_ANA to the power source. VCC must be tied to the highest voltage in the system. If the load switch is used as switch on the output, VCC must be tied to the input voltage of VINDCDx and VIN_DCDC_ANA. If the load switch is used as a current limited switch on the input, VCC must be connected to pin LSI while LSO is connected to VINDCDCx and VINDCDC_ANA. The four step-down converters must not be supplied from different input voltages.

8.2.1.2.1.4 Output Capacitor Table

The DC-DC converters are designed for an output capacitance as listed under the *Recommended Operating Conditions*. A ceramic capacitor, such as X5R or X7R type, is required at the output. Table 8-4 lists capacitors used for TPS65912x.

Table 8-4. Possible Capacitors

Value	Size	Vendor	Material and Rating
47 µF / 6.3 V	0805	Murata GRM21BR60J476ME15	Ceramic X5R
22 µF / 6.3 V	0805	Murata GRM21BR60J226M	Ceramic X5R
10 µF / 10 V	0603	Murata GRM188R61A106ME69	Ceramic X5R

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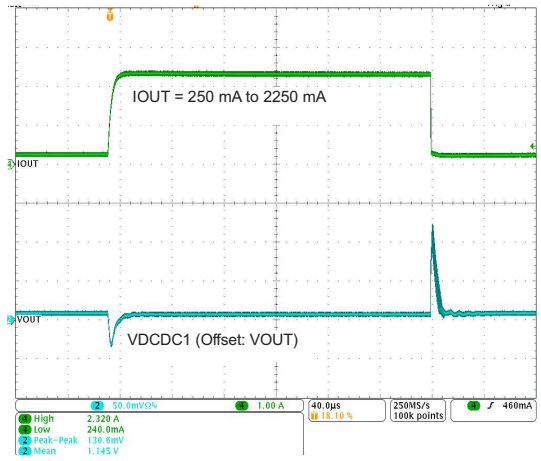
Table 8-4. Possible Capacitors (continued)

Value	Size	Vendor	Material and Rating
4.7 µF / 6.3 V	0603	Murata GRM188R60J475KE19	Ceramic X5R
4.7 µF / 6.3 V	0402	Murata GRM155R60J475ME87	Ceramic X5R

8.2.1.2.1.5 Voltage Change on DCDC1 to DCDC4

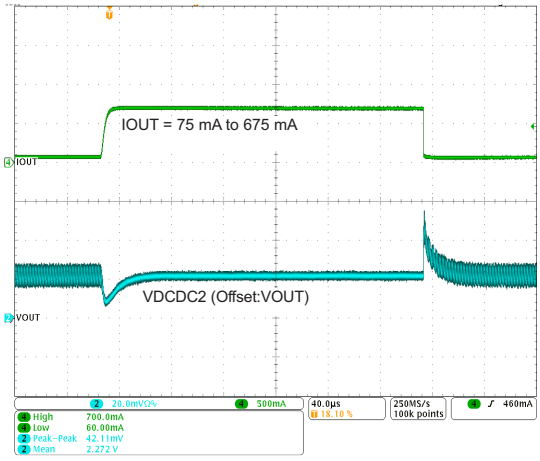
The output voltage of the DC-DC converters can be changed during operation by either the digital interfaces or by toggling the DCDCx_SEL pin or by entering SLEEP state if configured such.

8.2.1.3 Application Curves



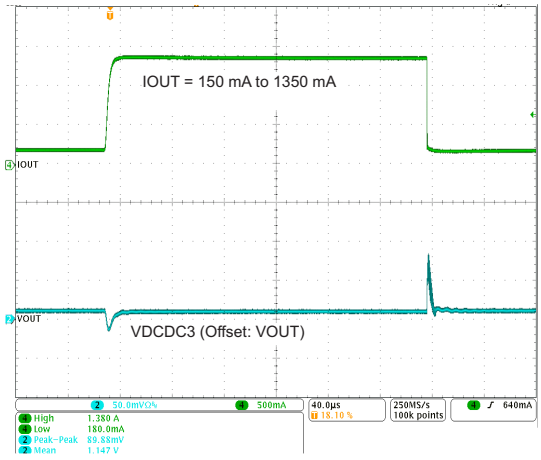
V_{IN} = 3.6 V V_O = 1.1375 V

Figure 8-2. Load Transient Response DCDC1



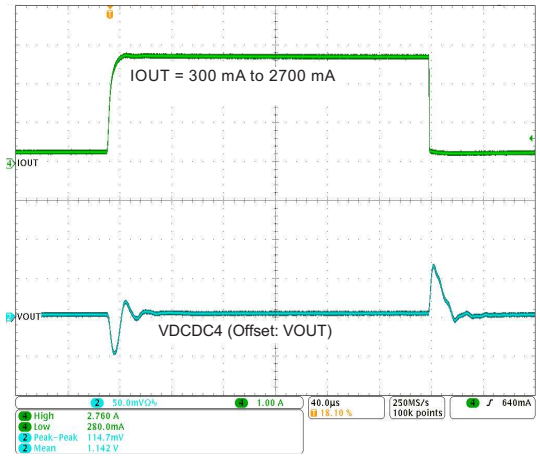
V_{IN} = 3.6 V V_O = 2.25 V

Figure 8-3. Load Transient Response DCDC2



V_{IN} = 3.6 V V_O = 1.1375 V

Figure 8-4. Load Transient Response DCDC3



V_{IN} = 3.6 V V_O = 1.1375 V

Figure 8-5. Load Transient Response DCDC4

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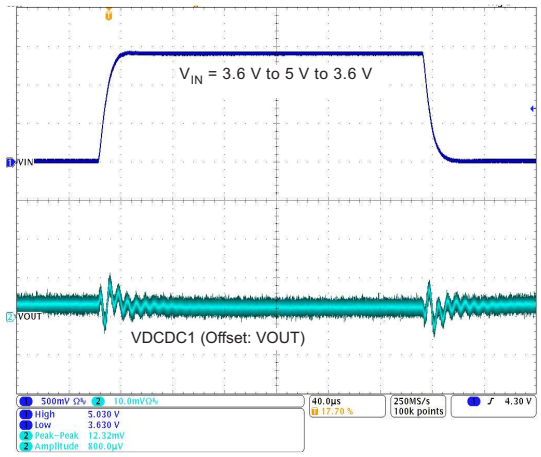
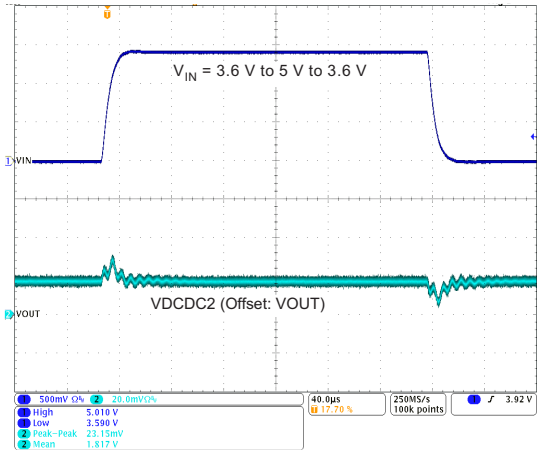


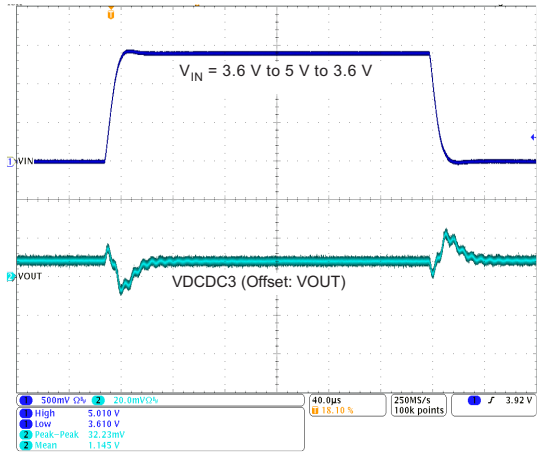
V_O = 1.1375 V I_O = 2500 mA

Figure 8-6. Line Transient Response DCDC1



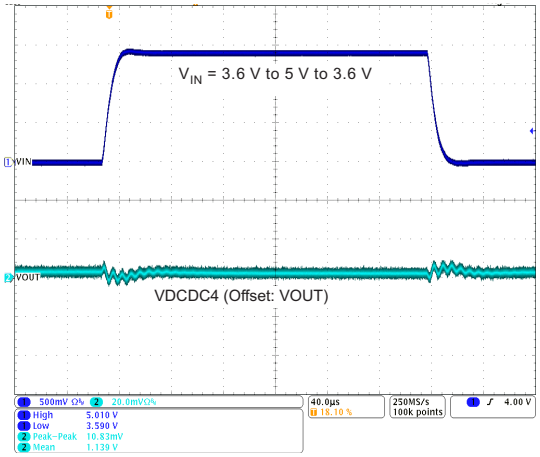
V_O = 1.8 V I_O = 750 mA

Figure 8-7. Line Transient Response DCDC2



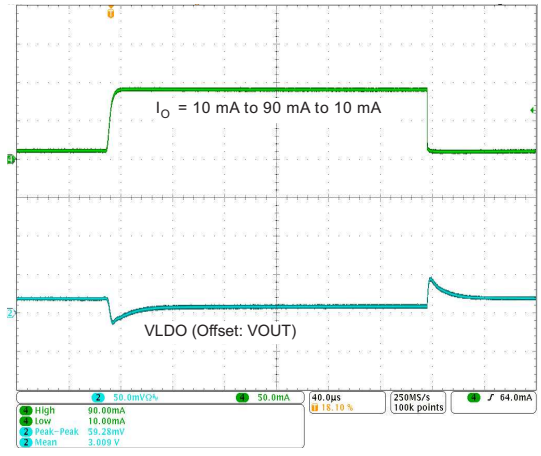
V_O = 1.1375 V I_O = 1500 mA

Figure 8-8. Line Transient Response DCDC3



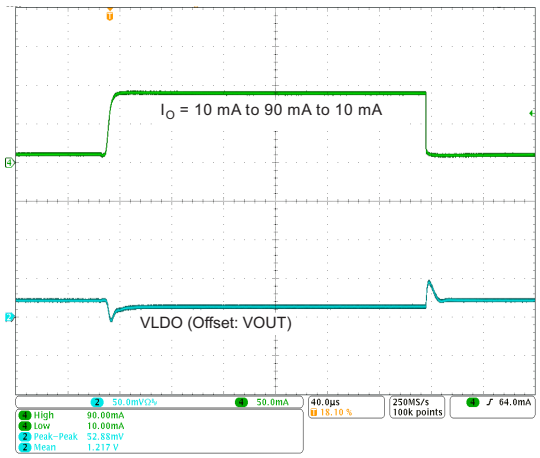
V_O = 1.1375 V I_O = 3000 mA

Figure 8-9. Line Transient Response DCDC4



V_{IN} = 3.3 V V_O = 3.0 V

Figure 8-10. Load Transient Response LDO1, LDO2, LDO3



V_{IN} = 1.8 V V_O = 1.2 V

Figure 8-11. Load Transient Response LDO1, LDO2, LDO3

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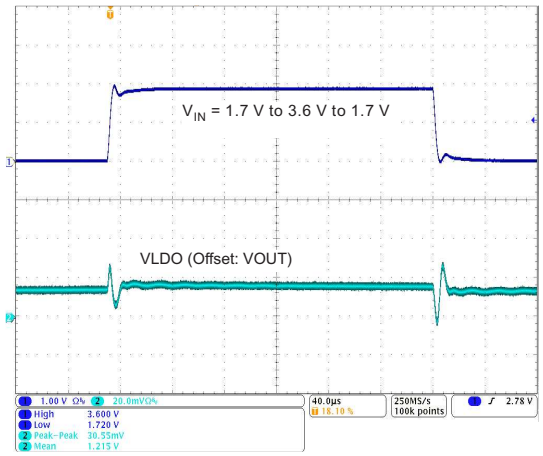
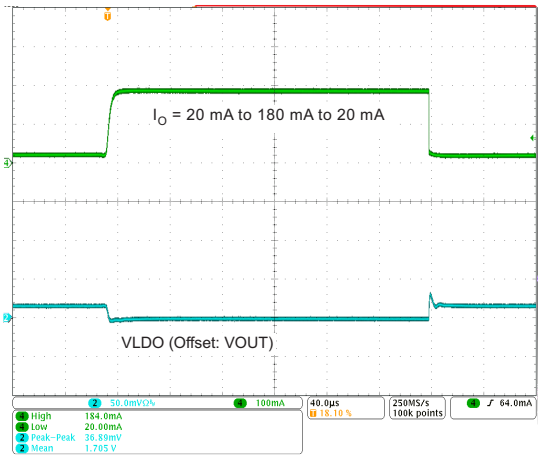


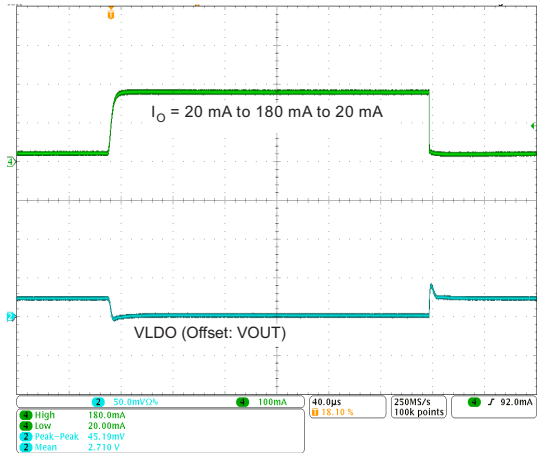
I_O = 100 mA V_O = 1.2 V

Figure 8-12. Line Transient Response LDO1, LDO2, LDO3



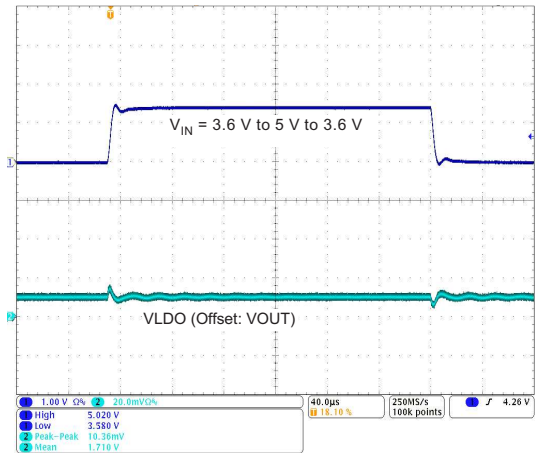
V_{IN} = 2.0 V V_O = 1.7 V

Figure 8-13. Load Transient Response LDO4, LDO5



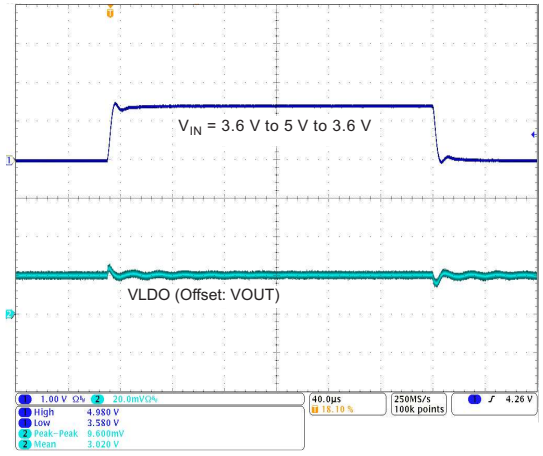
V_{IN} = 3.2 V V_O = 2.7 V

Figure 8-14. Load Transient Response LDO4, LDO5



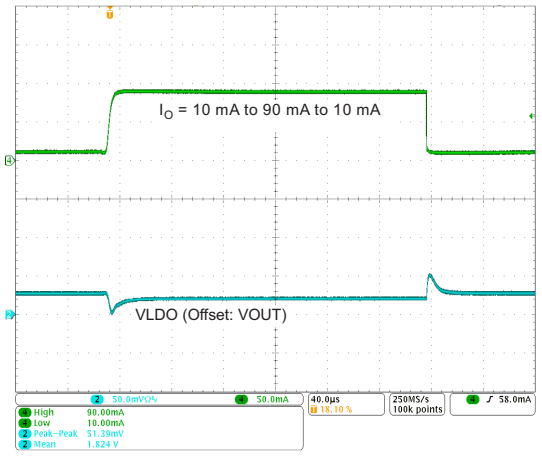
I_O = 100 mA V_O = 1.7 V

Figure 8-15. Line Transient Response LDO4, LDO5



I_O = 100 mA V_O = 3.0 V

Figure 8-16. Line Transient Response LDO4, LDO5



V_{IN} = 3.3 V V_O = 1.8 V

Figure 8-17. Load Transient Response LDO6, LDO8

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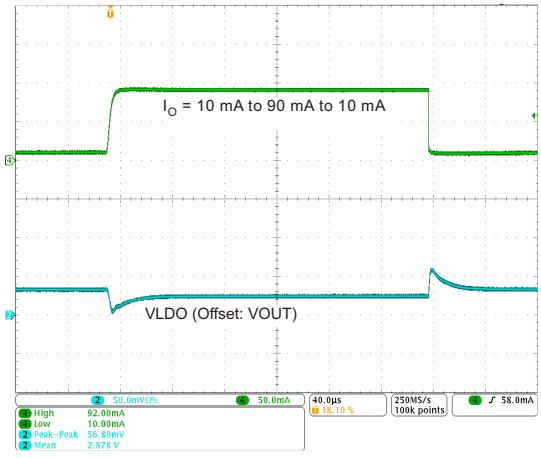
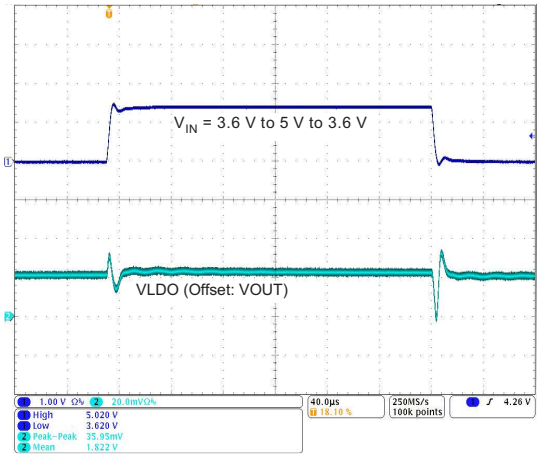


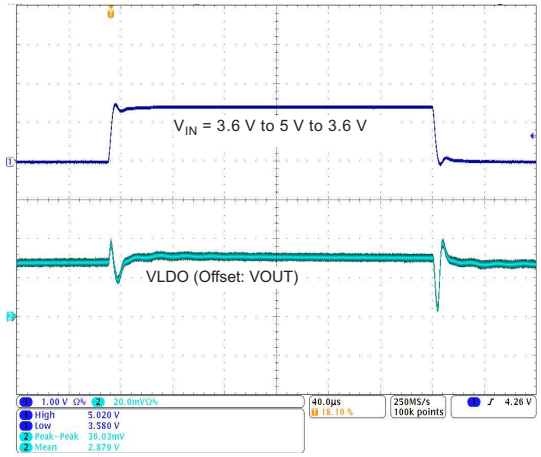
V_{IN} = 3.3 V V_O = 2.85 V

Figure 8-18. Load Transient Response LDO6, LDO8



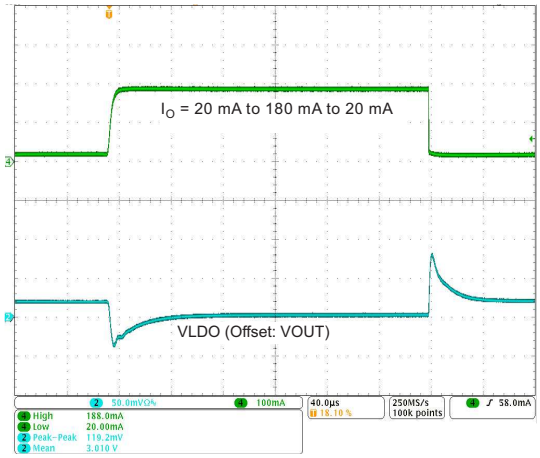
I_O = 100 mA V_O = 1.8 V

Figure 8-19. Line Transient Response LDO6, LDO8



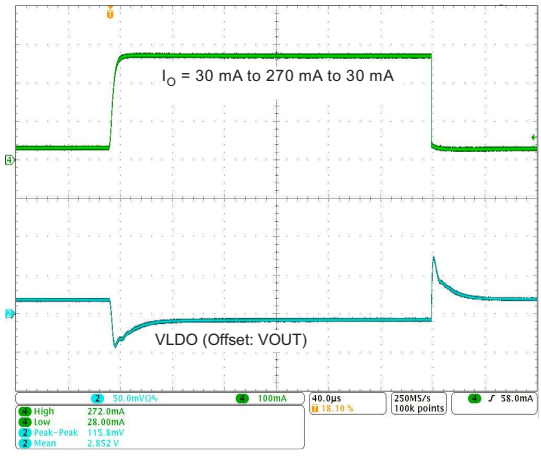
I_O = 100 mA V_O = 2.85 V

Figure 8-20. Line Transient Response LDO6, LDO8



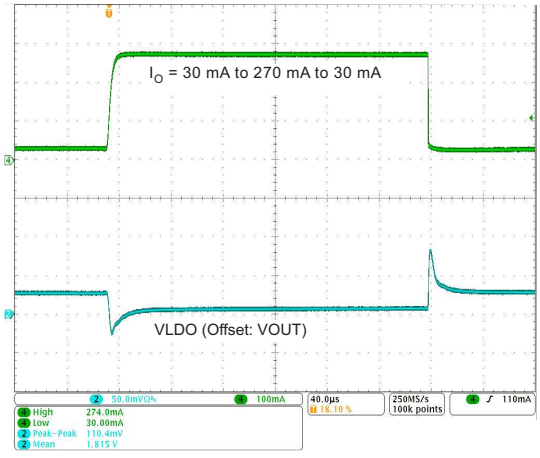
V_{IN} = 3.2 V V_O = 3.0 V

Figure 8-21. Load Transient Response LDO7



V_{IN} = 3.3 V V_O = 2.85 V

Figure 8-22. Load Transient Response LDO9



V_{IN} = 3.3 V V_O = 1.8 V

Figure 8-23. Load Transient Response LDO10

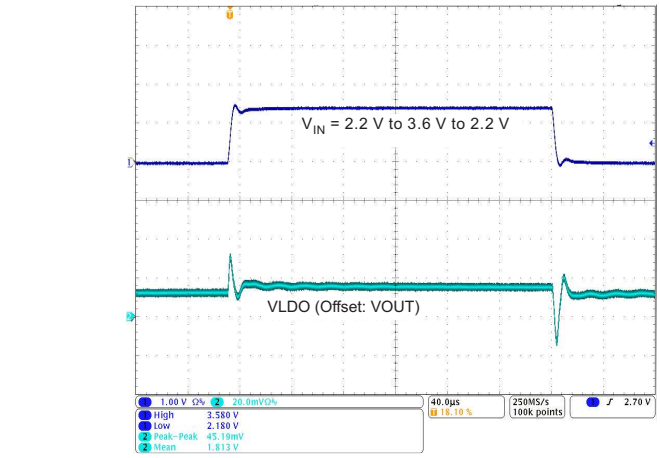


Figure 8-24. Line Transient Response LDO10

8.2.1.4 Layout

8.2.1.4.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design. Proper function of the device demands careful attention to PCB layout. Care must be taken in board layout to get the specified performance. If the layout is not carefully done, the regulators may show poor line and/or load regulation and stability issues, as well as EMI problems. It is critical to provide a low-impedance ground path. Therefore, use wide and short traces for the main current paths. The input capacitors must be placed as close as possible to the IC pins as well as the inductor and output capacitor.

Keep the common path to the GND pins, which returns the small signal components, and the high current of the output capacitors as short as possible to avoid ground noise. The VDCDCx trace should be connected right to the output capacitor and routed away from noisy components and traces (for example, the L1, L2, L3, and L4 traces).

The most critical connections are:

- PGNDx
- VDCDCx (positive output voltage sense connection)
- VDCDCx_GND (ground-sense connection)
- AGND
- VINDCDCx, VINDCDC_ANA, VCC

The PGNDx pins are the ground connections of the power stages, so they will carry high dc- and ac- peak currents. A low impedance connection to the GND-plane is needed, which must be independent from other pins in order not to couple noise into other pins. No other pins must be connected to PGNDx pins.

The VDCDCx pins are the positive-sense connections for the feedback loop. The connection must be made directly to the positive terminal of the pad of the output capacitor. Do not tie the pin to the pad of the output inductor or anywhere in between inductor and capacitor. It is also a good practice to shield the connection by GND traces or a GND-plane.

VDCDCx_GND is a sense connection for GND and is only available for DCDC1 and DCDC4. The connection can either be made to the GND pad of the output capacitor (preferred) or to the GND-plane directly if there is a solid connection of the GND-plane to the output capacitor. The pin must not be connected to the PGNDx pins as this will couple switching noise into the feedback loop.

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The AGND (analog ground) pin is the main GND connection for internal analog circuitry. A proper connection must be made to a GND plane directly by a via. AGND and DGND (located next to each other) may be connected and a via each be used to the GND-plane.

VINDCDCx, VINDCD_ANA and VCC are supply-voltage-input terminals and need to be properly bypassed by their input capacitors. The CAPACITANCE needed is given in the Section 5.3. As ceramic capacitors will change their capacitance based on the voltage applied, temperature and age, the influence of these parameters need to be considered when choosing the value of a capacitor. The input capacitors are ideally placed on the same layer as the IC, so the connection can be made short and directly on the same layer with multiple vias used from the GND terminal to the GND-plane.

For details about the layout for TPS659121 and TPS659122, see the EVM user's guide, which can be found in the product folder on ti.com.

8.2.1.4.2 Layout Example

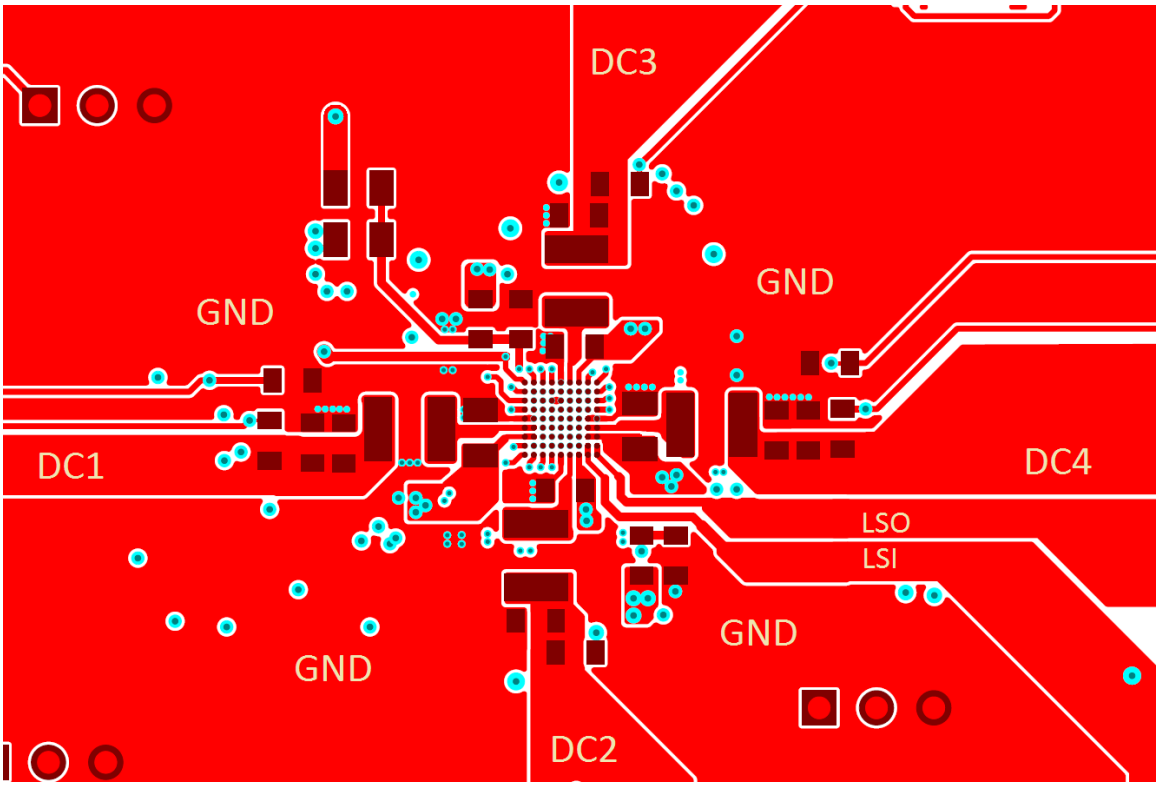

Figure 8-25. Layout Example

8.3 Power Supply Recommendations

The TPS65912 device is designed to work with an analog supply voltage range from 2.7 V to 5.5 V. The input supply should be well regulated and connected to the VCC pin, as well as the DCDC and LDO input pins. If the input supply is located more than a few inches from the TPS65912 device, additional capacitance may be required in addition to the recommended input capacitors at the VCC pin and the DCDC and LDO input pins.

9 Device and Documentation Support

9.1 Device Support

9.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

The following products support development of the TPS659121 and TPS659122 device applications:

Software Development Tools: Code Composer Studio™ Integrated Development Environment (IDE): including Editor C/C++/Assembly Code Generation, and Debug plus additional development tools Scalable, Real-Time Foundation Software (DSP/BIOS™), which provides the basic run-time target software needed to support any TPS659121 and TPS659122 device application.

Hardware Development Tools: Extended Development System (XDS™) Emulator

For a complete listing of development-support tools for the TPS659121 and TPS659122 platform, visit the Texas Instruments website at www.ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TPS659121 and TPS659122).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

X and P devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TPS659121 and TPS659122 devices in the YFF package types, see the Package Option Addendum of this document, the TI website (www.ti.com), or contact your TI sales representative.

9.2 Documentation Support

9.2.1 Related Documentation

For related documentation see the following:
Texas Instruments, *TPS65912xEVM-081 User's Guide*

9.3 Receiving Notification of Documentation Updates

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To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community The TI engineer-to-engineer (E2E) community was created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.5 Trademarks

Eco-mode, Code Composer Studio, DSP/BIOS, XDS, E2E are trademarks of Texas Instruments.
NXP is a registered trademark of NXP Semiconductors.
All other trademarks are the property of their respective owners.

9.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS659121YFFR	ACTIVE	DSBGA	YFF	81	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659121	Samples
TPS659121YFFT	ACTIVE	DSBGA	YFF	81	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659121	Samples
TPS659122YFFR	ACTIVE	DSBGA	YFF	81	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659122	Samples
TPS659122YFFT	ACTIVE	DSBGA	YFF	81	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659122	Samples
TPS659127YFFR	ACTIVE	DSBGA	YFF	81	1500	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659127	Samples
TPS659127YFFT	ACTIVE	DSBGA	YFF	81	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS659127	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

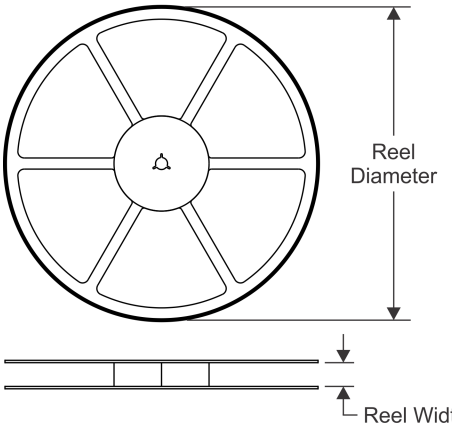
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

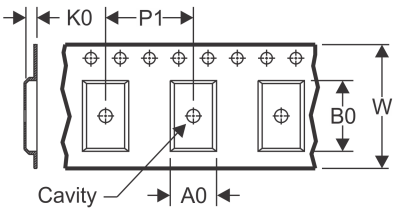
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

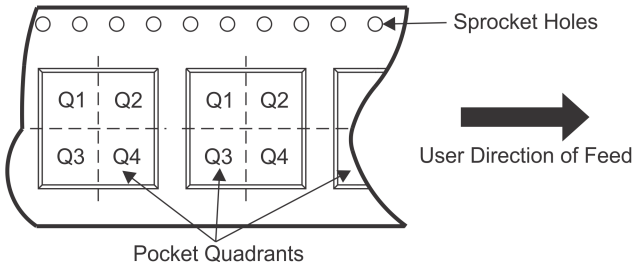


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

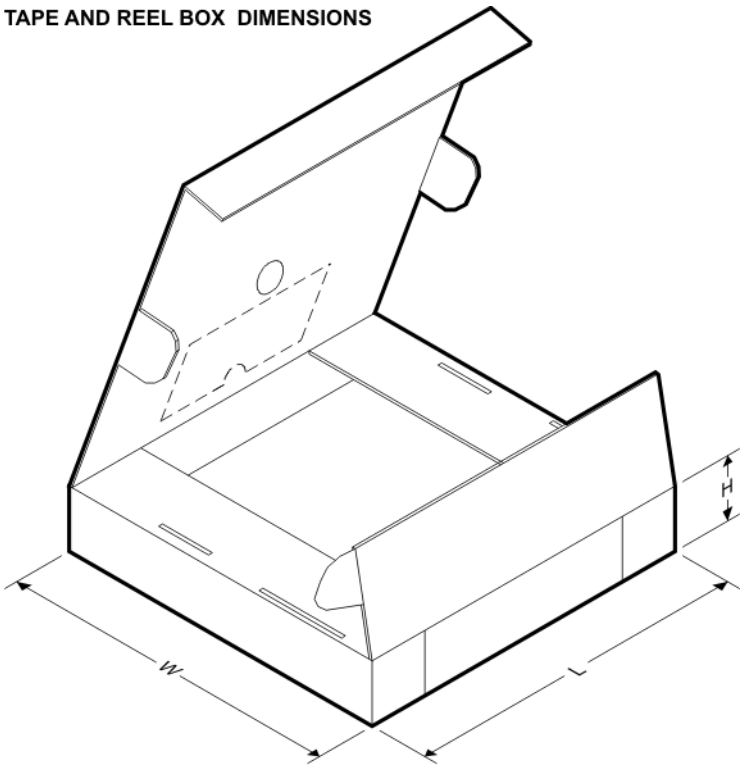
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS659121YFFR	DSBGA	YFF	81	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659121YFFT	DSBGA	YFF	81	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659122YFFR	DSBGA	YFF	81	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659122YFFT	DSBGA	YFF	81	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659127YFFR	DSBGA	YFF	81	1500	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1
TPS659127YFFT	DSBGA	YFF	81	250	180.0	12.4	3.79	3.79	0.71	8.0	12.0	Q1

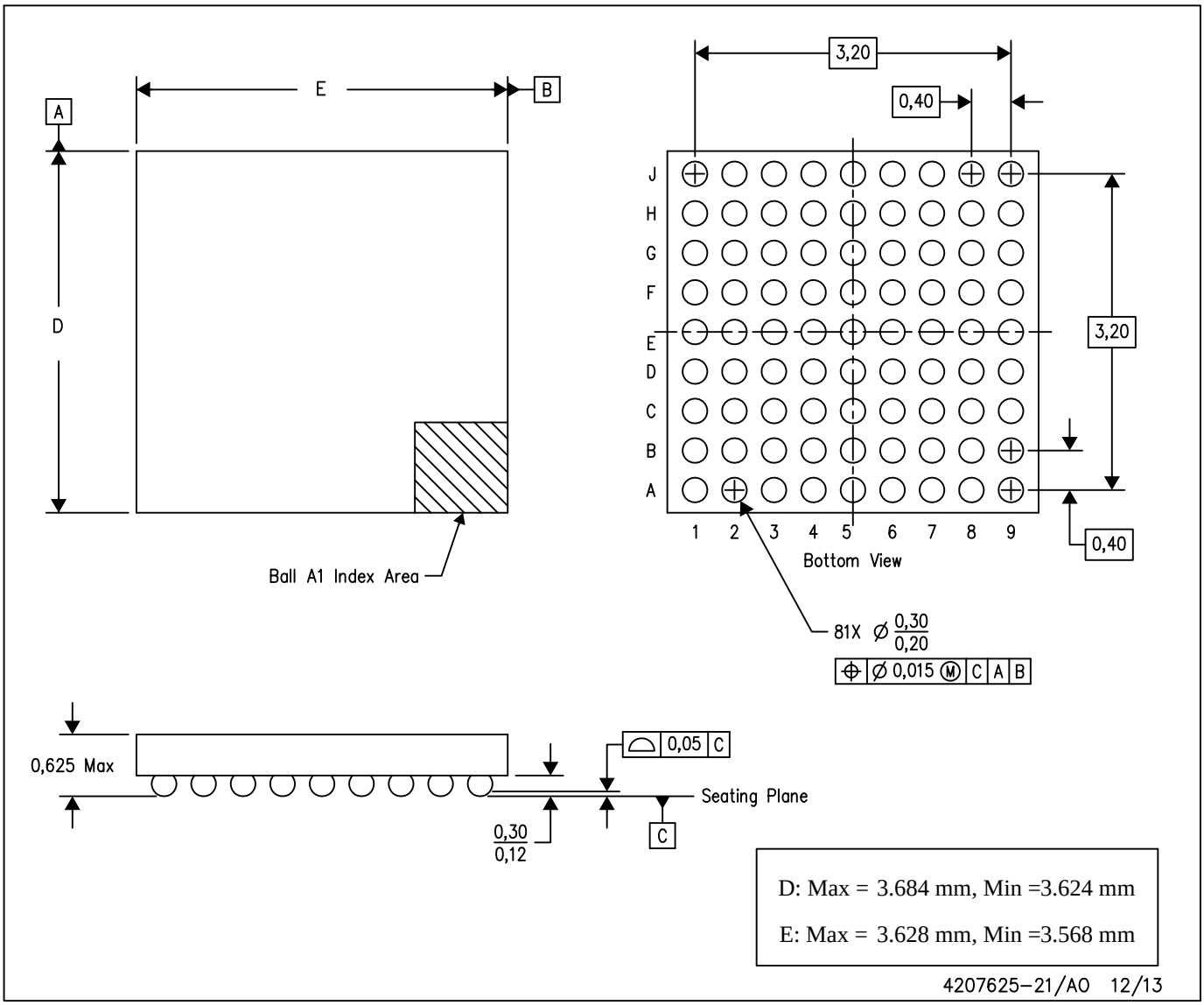
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS659121YFFR	DSBGA	YFF	81	1500	182.0	182.0	20.0
TPS659121YFFT	DSBGA	YFF	81	250	182.0	182.0	20.0
TPS659122YFFR	DSBGA	YFF	81	1500	182.0	182.0	20.0
TPS659122YFFT	DSBGA	YFF	81	250	182.0	182.0	20.0
TPS659127YFFR	DSBGA	YFF	81	1500	182.0	182.0	20.0
TPS659127YFFT	DSBGA	YFF	81	250	182.0	182.0	20.0

YFF (R–XBGA–N81) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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