THE DATASHEET OF

AD9225ARSRL

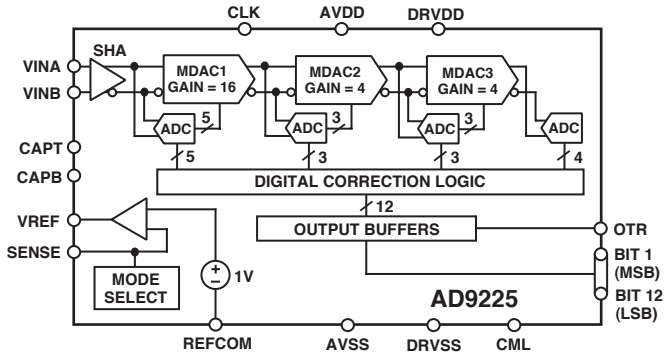
Complete 12-Bit, 25 MSPS Monolithic A/D Converter

AD9225

FEATURES

Monolithic 12-Bit, 25 MSPS ADC
Low Power Dissipation: 280 mW
Single 5 V Supply
No Missing Codes Guaranteed
Differential Nonlinearity Error: ±0.4 LSB
Complete On-Chip Sample-and-Hold Amplifier and Voltage Reference
Signal-to-Noise and Distortion Ratio: 71 dB
Spurious-Free Dynamic Range: –85 dB
Out-of-Range Indicator
Straight Binary Output Data
28-Lead SOIC
28-Lead SSOP
Compatible with 3 V Logic

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9225 is a monolithic, single-supply, 12-bit, 25 MSPS analog-to-digital converter with an on-chip, high performance sample-and-hold amplifier and voltage reference. The AD9225 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 25 MSPS data rates, and guarantees no missing codes over the full operating temperature range.

The AD9225 combines a low cost, high speed CMOS process and a novel architecture to achieve the resolution and speed of existing bipolar implementations at a fraction of the power consumption and cost.

The input of the AD9225 allows for easy interfacing to both imaging and communications systems. With the device's truly differential input structure, the user can select a variety of input ranges and offsets, including single-ended applications. The dynamic performance is excellent.

The sample-and-hold amplifier (SHA) is well suited for both multiplexed systems that switch full-scale voltage levels in successive channels and sampling single-channel inputs at frequencies up to and well beyond the Nyquist rate.

The AD9225's wideband input, combined with the power and cost savings over previously available monolithics, suits applications in communications, imaging, and medical ultrasound.

The AD9225 has an on-board programmable reference. An external reference can also be chosen to suit the dc accuracy and temperature drift requirements of an application.

A single clock input is used to control all internal conversion cycles. The digital output data is presented in straight binary output format. An out-of-range signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

PRODUCT HIGHLIGHTS

The AD9225 is fabricated on a very cost effective CMOS process. High speed precision analog circuits are combined with high density logic circuits.

The AD9225 offers a complete, single-chip sampling, 12-bit, 25 MSPS analog-to-digital conversion function in 28-lead SOIC and SSOP packages.

Low Power—The AD9225 at 280 mW consumes a fraction of the power presently available in monolithic solutions.

On-Board Sample-and-Hold Amplifier (SHA)—The versatile SHA input can be configured for either single-ended or differential inputs.

Out-of-Range (OTR)—The OTR output bit indicates when the input signal is beyond the AD9225's input range.

Single Supply—The AD9225 uses a single 5 V power supply, simplifying system power supply design. It also features a separate digital driven supply line to accommodate 3 V and 5 V logic families.

Pin Compatibility—The AD9225 is pin compatible with the AD9220, AD9221, AD9223, and AD9224 ADCs.

Rev. C

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax:781/461-3113
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AD9225–SPECIFICATIONS

DC SPECIFICATIONS

(AVDD = 5 V, DRVDD = 5 V, f_{SAMPLE} = 25 MSPS, VREF = 2.0 V, VINB = 2.5 V dc, T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	12			Bits
MAX CONVERSION RATE	25			MHz
INPUT REFERRED NOISE				
VREF = 1.0 V		0.35		LSB rms
VREF = 2.0 V		0.17		LSB rms
ACCURACY				
Integral Nonlinearity (INL)		±1.0	±2.5	LSB
Differential Nonlinearity (DNL)		±0.4	±1.0	LSB
No Missing Codes		12		Bits Guaranteed
Zero Error (@ 25°C)		±0.3	±0.6	% FSR
Gain Error (@ 25°C)[1]		±0.5	±2.2	% FSR
Gain Error (@ 25°C)[2]		±0.4	±1.7	% FSR
TEMPERATURE DRIFT				
Zero Error		±2		ppm/°C
Gain Error[1]		±26		ppm/°C
Gain Error[2]		±0.4		ppm/°C
POWER SUPPLY REJECTION				
AVDD (+5 V ± 0.25 V)		±0.1	±0.35	% FSR
ANALOG INPUT				
Input Span		2		V p-p
		4		V p-p
Input (VINA or VINB) Range		0		V
		AVDD		V
Input Capacitance		10		pF
INTERNAL VOLTAGE REFERENCE				
Output Voltage (1 V Mode)		1.0		V
Output Voltage Tolerance (1 V Mode)		±5	±17	mV
Output Voltage (2.0 V Mode)		2.0		V
Output Voltage Tolerance (2.0 V Mode)		±10	±35	mV
Output Current (Available for External Loads)		1.0		mA
Load Regulation[3]		1.0	3.4	mV
REFERENCE INPUT RESISTANCE		8		kΩ
POWER SUPPLIES				
Supply Voltages				
AVDD	4.75	5	5.25	V (±5% AVDD Operating)
DRVDD	2.85		5.25	V (±5% DRVDD Operating)
Supply Currents				
IAVDD		65	72.5	mA
IDRVDD		2.0	4.0	mA
POWER CONSUMPTION				
External Reference		280	310	mW (VREF = 1 V)
		335	373	mW (VREF = 2 V)
Internal Reference		290		mW (VREF = 1 V)
		345		mW (VREF = 2 V)

NOTES

[1]Includes internal voltage reference error.

[2]Excludes internal voltage reference error.

[3]Load regulation with 1 mA load current (in addition to that required by the AD9225).

Specifications subject to change without notice.

AC SPECIFICATIONS

(AVDD = 5 V, DRVDD = 5 V, f_{SAMPLE} = 25 MSPS, VREF = 2.0 V, T_{MIN} to T_{MAX}, Differential Input unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
SIGNAL-TO-NOISE AND DISTORTION RATIO (S/N+D)				
f_{INPUT} = 2.5 MHz	67.4	70.7		dB
f_{INPUT} = 10 MHz	66.7	69.6		dB
SIGNAL-TO-NOISE RATIO (SNR)				
f_{INPUT} = 2.5 MHz	69.0	71		dB
f_{INPUT} = 10 MHz	68.2	70		dB
TOTAL HARMONIC DISTORTION (THD)				
f_{INPUT} = 2.5 MHz		–82	–72	dB
f_{INPUT} = 10 MHz		–81	–71.5	dB
SPURIOUS FREE DYNAMIC RANGE				
f_{INPUT} = 2.5 MHz	73	–85		dB
f_{INPUT} = 10 MHz	72.5	–83		dB
Full Power Bandwidth		105		MHz
Small Signal Bandwidth		105		MHz
Aperture Delay		1		ns
Aperture Jitter		1		ps rms
Acquisition to Full-Scale Step		10		ns

Specifications subject to change without notice.

DIGITAL SPECIFICATIONS

(AVDD = 5 V, DRVDD = 5 V, unless otherwise noted.)

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS					
High Level Input Voltage	V_{IH}	3.5			V
Low Level Input Voltage	V_{IL}			1.0	V
High Level Input Current (V_{IN} = DRVDD)	I_{IH}	–10		+10	μA
Low Level Input Current (V_{IN} = 0 V)	I_{IL}	–10		+10	μA
Input Capacitance	C_{IN}		5		pF
LOGIC OUTPUTS					
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	4.5			V
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.4			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}			0.4	V
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}			0.1	V
Output Capacitance	C_{OUT}		5		pF
LOGIC OUTPUTS (with DRVDD = 3 V)					
High Level Output Voltage (I_{OH} = 50 μA)	V_{OH}	2.95			V
High Level Output Voltage (I_{OH} = 0.5 mA)	V_{OH}	2.80			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	V_{OL}			0.4	V
Low Level Output Voltage (I_{OL} = 50 μA)	V_{OL}			0.05	V

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

(T_{MIN} to T_{MAX} with AVDD = 5 V, DRVDD = 5 V, C_L = 20 pF)

Parameter	Symbol	Min	Typ	Max	Unit
Clock Period*	t_C	40			ns
CLOCK Pulse Width High	t_{CH}	18			ns
CLOCK Pulse Width Low	t_{CL}	18			ns
Output Delay	t_{OD}	13			ns
Pipeline Delay (Latency)			3		Clock Cycles

*The clock period may be extended to 1 ms without degradation in specified performance @ 25°C.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Pin Name	With Respect to	Min	Max	Unit
AVDD	AVSS	–0.3	+6.5	V
DRVDD	DRVSS	–0.3	+6.5	V
AVSS	DRVSS	–0.3	+0.3	V
AVDD	DRVDD	–6.5	+6.5	V
REFCOM	AVSS	–0.3	+0.3	V
CLK	AVSS	–0.3	AVDD + 0.3	V
Digital Outputs	DRVSS	–0.3	DRVDD + 0.3	V
VINA, VINB	AVSS	–0.3	AVDD + 0.3	V
VREF	AVSS	–0.3	AVDD + 0.3	V
SENSE	AVSS	–0.3	AVDD + 0.3	V
CAPB, CAPT	AVSS	–0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		–65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

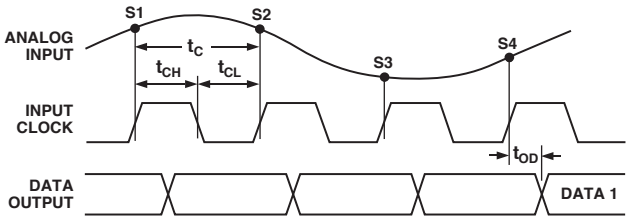
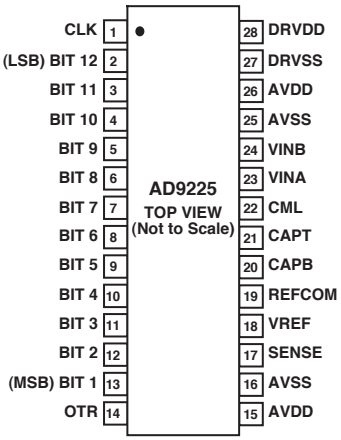


Figure 1. Timing Diagram

PIN CONFIGURATION
28-Lead SOIC and SSOP



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9225 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin Number	Mnemonic	Description
1	CLK	Clock Input Pin
2	BIT 12	Least Significant Data Bit (LSB)
3–12	BIT 11–2	Data Output Bit
13	BIT 1	Most Significant Data Bit (MSB)
14	OTR	Out of Range
15, 26	AVDD	5 V Analog Supply
16, 25	AVSS	Analog Ground
17	SENSE	Reference Select
18	VREF	Input Span Select (Reference I/O)
19	REFCOM	Reference Common (AVSS)
20	CAPB	Noise Reduction Pin
21	CAPT	Noise Reduction Pin
22	CML	Common-Mode Level (Midsupply)
23	VINA	Analog Input Pin (+)
24	VINB	Analog Input Pin (–)
27	DRVSS	Digital Output Driver Ground
28	DRVDD	3 V to 5 V Digital Output Driver Supply

TERMINOLOGY

Integral Nonlinearity (INL)
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs 1/2 LSB before the first code transition. Positive full scale is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes, respectively, must be present over all operating ranges.

Zero Error
The major carry transition should occur for an analog value 1/2 LSB below VINA = VINB. Zero error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value 1/2 LSB above negative full scale. The last transition should occur at an analog value 1 1/2 LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Aperture Jitter
Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the ADC.

Aperture Delay
Aperture delay is a measure of the sample-and-hold amplifier (SHA) performance and is measured from the rising edge of the clock input to when the input signal is held for conversion.

Signal-to-Noise and Distortion Ratio (S/N+D, SINAD)
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Effective Number of Bits (ENOB)
For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula,

$$N = (SINAD - 1.76)/6.02$$

it is possible to get a measure of performance expressed as N, the effective number of bits.

The effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

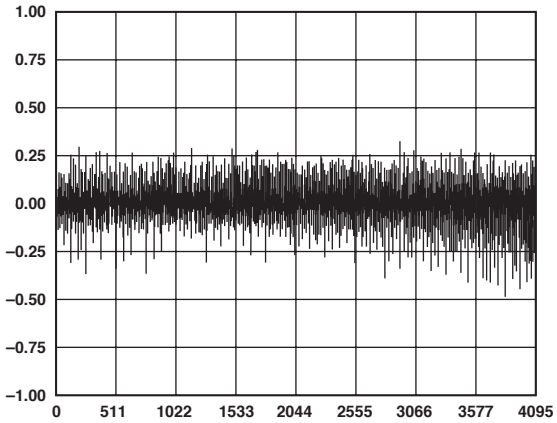
Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in decibels.

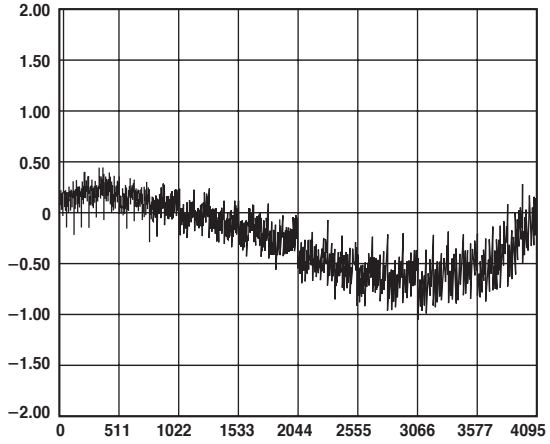
Spurious-Free Dynamic Range (SFDR)
SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

AD9225–Typical Performance Characteristics

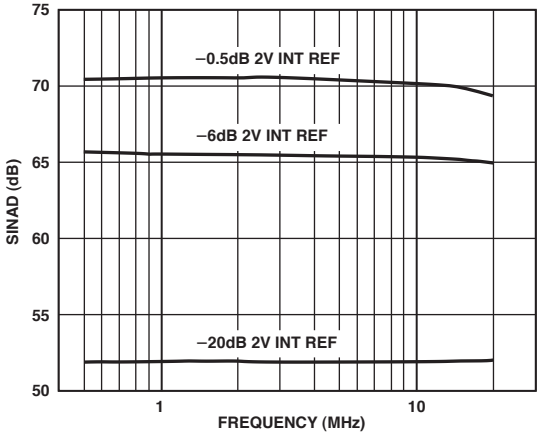
(AVDD, DRVDD = 5 V, f_S = 25 MHz (50% Duty Cycle), unless otherwise noted.)



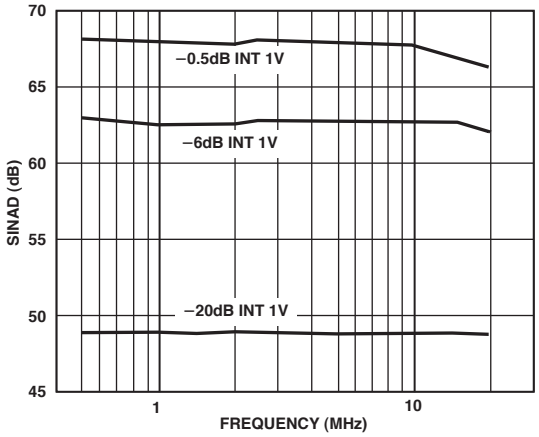
TPC 1. Typical DNL



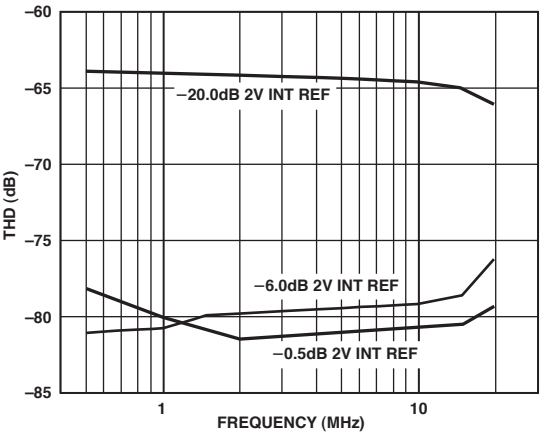
TPC 4. Typical INL



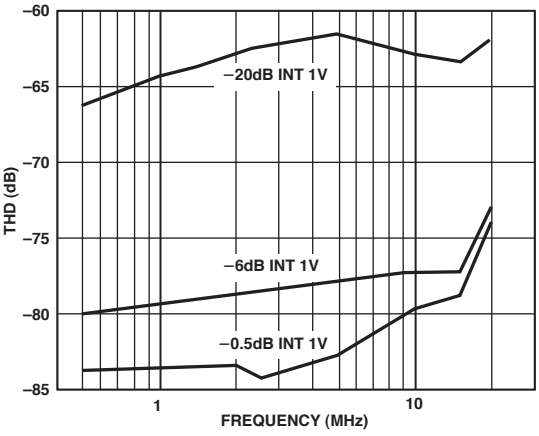
TPC 2. SINAD vs. Input Frequency (Input Span = 4.0 V p-p, V_{CM} = 2.5 V Differential Input)



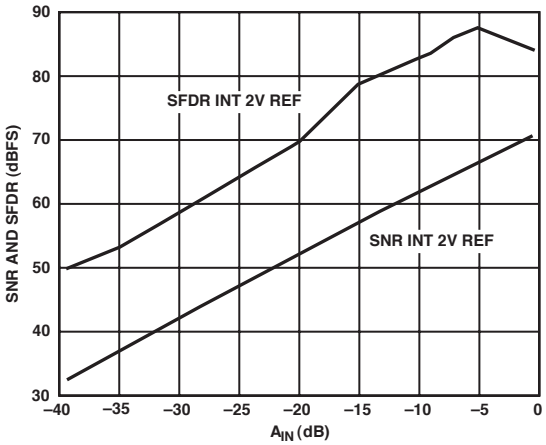
TPC 5. SINAD vs. Input Frequency (Input Span = 2 V p-p V_{CM} = 2.5 V Differential Input)



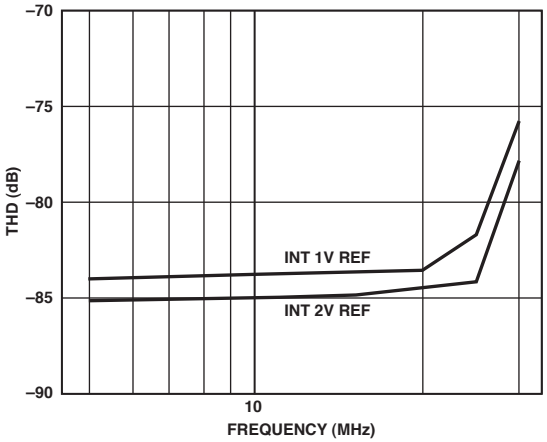
TPC 3. THD vs. Input Frequency (Input Span = 4.0 V p-p, V_{CM} = 2.5 V Differential Input)



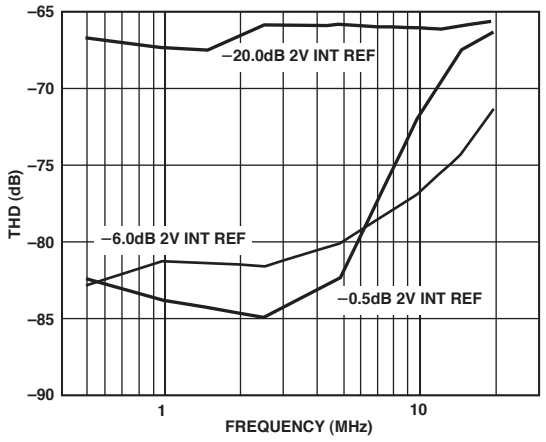
TPC 6. THD vs. Input Frequency (Input Span = 2 V p-p, V_{CM} = 2.5 V Differential Input)



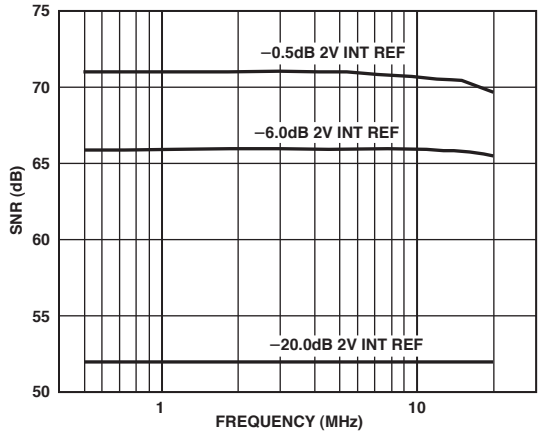
TPC 7. SNR/SFDR vs. A_{IN} (Input Amplitude) (f_{IN} = 12.5 MHz, Input Span = 4.0 V p-p, V_{CM} = 2.5 V Differential Input)



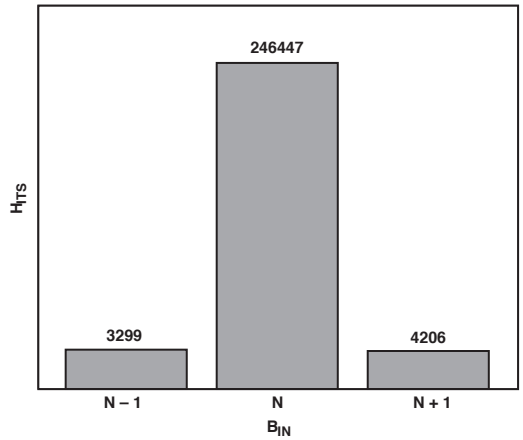
TPC 10. THD vs. Sample Rate, (A_{IN} = –0.5 dB, V_{CM} = 2.5 V, Input Span = 4.0 V p-p Differential Input)



TPC 8. THD vs. Input Frequency (Input Span = 4.0 V p-p, V_{CM} = 2.5 V Single-Ended Input)



TPC 11. SNR vs. Input Frequency (Input Span = 4.0 V p-p, V_{CM} = 2.5 V Single-Ended Input)



TPC 9. Grounded-Input Histogram (Input Span = 40 V p-p)

INTRODUCTION

The AD9225 is a high performance, complete single-supply 12-bit ADC. The analog input range of the AD9225 is highly flexible, allowing for both single-ended or differential inputs of varying amplitudes that can be ac-coupled or dc-coupled.

The AD9225 utilizes a four-stage pipeline architecture with a wideband input sample-and-hold amplifier (SHA) implemented on a cost-effective CMOS process. Each stage of the pipeline, excluding the last stage, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier amplifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The pipeline architecture allows a greater throughput rate at the expense of pipeline delay or latency. This means that while the converter is capable of capturing a new input sample every clock cycle, it actually takes three clock cycles for the conversion to be fully processed and appear at the output. This latency is not a concern in most applications. The digital output, together with the out-of-range indicator (OTR), is latched into an output buffer to drive the output pins. The output drivers of the AD9225 can be configured to interface with 5 V or 3.3 V logic families.

The AD9225 uses both edges of the clock in its internal timing circuitry (see Figure 1 and Specifications tables for exact timing requirements). The ADC samples the analog input on the rising edge of the clock input. During the clock low time (between the falling edge and rising edge of the clock), the input SHA is in the sample mode; during the clock high time it is in hold mode. System disturbances just prior to the rising edge of the clock and/or excessive clock jitter may cause the input SHA to acquire the wrong value, and should be minimized.

ANALOG INPUT AND REFERENCE OVERVIEW

Figure 2 is a simplified model of the AD9225. It highlights the relationship between the analog inputs, VINA and VINB, and the reference voltage, VREF. Like the voltage applied to the top of the resistor ladder in a flash ADC, the value VREF defines the maximum input voltage to the ADC core. The minimum input voltage to the ADC core is automatically defined to be –VREF.

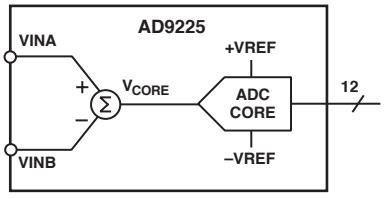


Figure 2. Equivalent Functional Input Circuit

The addition of a differential input structure gives the user an additional level of flexibility that is not possible with traditional flash converters. The input stage allows the user to easily configure the inputs for either single-ended operation or differential operation. The A/D converter's input structure allows the dc offset of the input signal to be varied independently of the input span of the converter. Specifically, the input to the ADC core is the difference of the voltages applied at the *VINA* and *VINB* input pins. Therefore, the equation

$$VCORE = VINA - VINB \quad (1)$$

defines the output of the differential input stage and provides the input to the ADC core.

The voltage, *VCORE*, must satisfy the condition

$$-VREF \le VCORE \le VREF \quad (2)$$

where *VREF* is the voltage at the *VREF* pin.

While an infinite combination of *VINA* and *VINB* inputs exist that satisfy Equation 2, there is an additional limitation placed on the inputs by the power supply voltages of the AD9225. The power supplies bound the valid operating range for *VINA* and *VINB*. The condition

$$AVSS - 0.3\ V < VINA < AVDD + 0.3\ V \quad (3)$$

$$AVSS - 0.3\ V < VINB < AVDD + 0.3\ V$$

where *AVSS* is nominally 0 V and *AVDD* is nominally 5 V, defines this requirement. The range of valid inputs for *VINA* and *VINB* is any combination that satisfies both Equations 2 and 3.

For additional information showing the relationships among VINA, VINB, VREF, and the digital output of the AD9225, see Table IV.

Refer to Table I and Table II at the end of this section for a summary of the various analog input and reference configurations.

ANALOG INPUT OPERATION

Figure 3 shows the equivalent analog input of the AD9225, which consists of a differential sample-and-hold amplifier. The differential input structure of the SHA is highly flexible, allowing the devices to be easily configured for either a differential or single-ended input. The dc offset, or common-mode voltage, of the input(s) can be set to accommodate either single-supply or dual-supply systems. Also, note that the analog inputs, VINA and VINB, are interchangeable, with the exception that reversing the inputs to the VINA and VINB pins results in a polarity inversion.

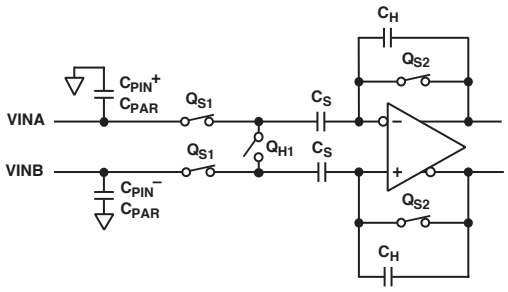


Figure 3. Simplified Input Circuit

The AD9225 has a wide input range. The input peaks may be moved to AVDD or AVSS before performance is compromised. This allows for much greater flexibility when selecting single-ended drive schemes. Op amps and ac coupling clamps can be set to available reference levels rather than be dictated according to what the ADC needs.

Due to the high degree of symmetry within the SHA topology, a significant improvement in distortion performance for differential input signals with frequencies up to and beyond Nyquist can be realized. This inherent symmetry provides excellent cancellation of both common-mode distortion and noise. Also, the required input signal voltage span is reduced by a half, which further reduces the degree of R_{ON} modulation and its effects on distortion.

The optimum noise and dc linearity performance for either differential or single-ended inputs is achieved with the largest input signal voltage span (i.e., 4 V input span) and matched input impedance for VINA and VINB. Only a slight degradation in dc linearity performance exists between the 2 V and 4 V input spans.

Referring to Figure 3, the differential SHA is implemented using a switched capacitor topology. Its input impedance and its switching effects on the input drive source should be considered in order to maximize the converter's performance. The combination of the pin capacitance, C_{PIN}, parasitic capacitance, C_{PAR}, and the sampling capacitance, C_S, is typically less than 5 pF. When the SHA goes into track mode, the input source must charge or discharge the voltage stored on C_S to the new input voltage. This action of charging and discharging C_S, averaged over a period of time and for a given sampling frequency, f_S, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period (i.e., $T = 1/f_S$), the input impedance is dynamic and therefore certain precautions on the input drive source should be observed.

The resistive component to the input impedance can be computed by calculating the average charge that gets drawn by C_H from the input drive source. It can be shown that if C_S is allowed to fully charge up to the input voltage before switches Q_{S1} are opened, then the average current into the input would be the same as it would if there were a resistor of $1/(C_S f_S)$ Ohms connected between the inputs. This means that the input impedance is inversely proportional to the converter's sample rate. Since C_S is only 5 pF, this resistive component is typically much larger than that of the drive source (i.e., 8 kΩ at f_S = 25 MSPS).

The SHA's input impedance over a sampling period appears as a dynamic input impedance to the input drive source. When the SHA goes into the track mode, the input source ideally should provide the charging current through R_{ON} of switch Q_{S1} in an exponential manner. The requirement of exponential charging means that the most common input source, an op amp, must exhibit a source impedance that is both low and resistive up to and beyond the sampling frequency.

The output impedance of an op amp can be modeled with a series inductor and resistor. When a capacitive load is switched onto the output of the op amp, the output will momentarily drop due to its effective output impedance. As the output recovers, ringing may occur. To remedy the situation, a series resistor can be inserted between the op amp and the SHA input as shown in Figure 4. The series resistance helps isolate the op amp from the switched capacitor load.

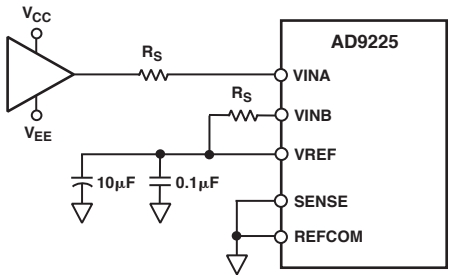


Figure 4. Series Resistor Isolates Switched Capacitor SHA Input from Op Amp. Matching Resistors Improve SNR Performance.

The optimum size of this resistor is dependent on several factors, which include the ADC sampling rate, the selected op amp, and the particular application. In most applications, a 30 Ω to 100 Ω resistor is sufficient. However, some applications may require a larger resistor value to reduce the noise bandwidth or possibly to limit the fault current in an overvoltage condition. Other applications may require a larger resistor value as part of an antialiasing filter. In any case, since the THD performance is dependent on the series resistance and the above mentioned factors, optimizing this resistor value for a given application is encouraged.

The source impedance driving VINA and VINB should be matched. Failure to provide that matching will result in degradation of the AD9225's superb SNR, THD, and SFDR.

For noise sensitive applications, the very high bandwidth of the AD9225 may be detrimental. The addition of a series resistor and/or shunt capacitor can help limit the wideband noise at the ADC's input by forming a low-pass filter. Note, however, that the combination of this series resistance with the equivalent input capacitance of the AD9225 should be evaluated for those time domain applications that are sensitive to the input signal's absolute settling time. In applications where harmonic distortion is not a primary concern, the series resistance may be selected in combination with the SHA's nominal 10 pF of input capacitance to set the filter's 3 dB cutoff frequency.

A better method of reducing the noise bandwidth, while possibly establishing a real pole for an antialiasing filter, is to add some additional shunt capacitance between the input (i.e., VINA and/or VINB) and analog ground. Since this additional shunt capacitance combines with the equivalent input capacitance of the AD9225, a lower series resistance can be selected to establish the filter's cutoff frequency while not degrading the distortion performance of the device. The shunt capacitance also acts like a charge reservoir, sinking or sourcing the additional charge required by the hold capacitor, C_H, and further reducing current transients seen at the op amp's output.

The effect of this increased capacitive load on the op amp driving the AD9225 should be evaluated. To optimize performance when noise is the primary consideration, increase the shunt capacitance as much as the transient response of the input signal will allow. Increasing the capacitance too much may adversely affect the op amp's settling time, frequency response, and distortion performance.

REFERENCE OPERATION

The AD9225 contains an on-board band gap reference that provides a pin strappable option to generate either a 1 V or 2 V output. With the addition of two external resistors, the user can generate reference voltages other than 1 V and 2 V. Another alternative is to use an external reference for designs requiring enhanced accuracy and/or drift performance. See Table II for a summary of the pin strapping options for the AD9225 reference configurations.

Figure 5 shows a simplified model of the internal voltage reference of the AD9225. A pin strappable reference amplifier buffers a 1 V fixed reference. The output from the reference amplifier, A1, appears on the VREF pin. The voltage on the VREF pin determines the full-scale input span of the ADC. This input span equals

$$Full\text{-}Scale\ Input\ Span = 2 \times VREF$$

The voltage appearing at the VREF pin as well as the state of the internal reference amplifier, A1, are determined by the voltage appearing at the SENSE pin. The logic circuitry contains two comparators that monitor the voltage at the SENSE pin. The comparator with the lowest set point (approximately 0.3 V) controls the position of the switch within the feedback path of A1. If the SENSE pin is tied to AVSS (AGND), the switch is connected to the internal resistor network thus providing a VREF of 2.0 V. If the SENSE pin is tied to the VREF pin via a short or resistor, the switch will connect to the SENSE pin. This short will provide a VREF of 1.0 V. An external resistor network will provide an alternative VREF between 1.0 V and 2.0 V. The other comparator controls internal circuitry that will disable the reference amplifier if the SENSE pin is tied AVDD. Disabling the reference amplifier allows the VREF pin to be driven by an external voltage reference.

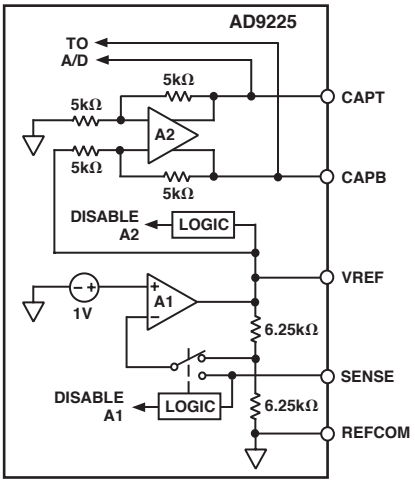


Figure 5. Equivalent Reference Circuit

The actual reference voltages used by the internal circuitry of the AD9225 appears on the CAPT and CAPB pins. For proper operation when using the internal or an external reference, it is necessary to add a capacitor network to decouple these pins. Figure 6 shows the recommended decoupling network. This capacitive network performs the following three functions: (1) along with the reference amplifier, A2, it provides a low source impedance over a large frequency range to drive the ADC internal circuitry, (2) it provides the necessary compensation for A2, and (3) it bandlimits the noise contribution from the reference. The turn-on time of the reference voltage appearing between CAPT and CAPB is approximately 15 ms and should be evaluated in any power-down mode of operation.

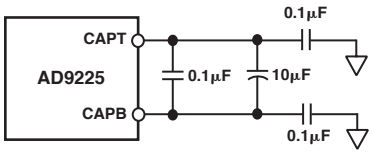


Figure 6. Recommended CAPT/CAPB Decoupling Network

The ADC's input span may be varied dynamically by changing the differential reference voltage appearing across CAPT and CAPB symmetrically around 2.5 V (i.e., midsupply). To change the reference at speeds beyond the capabilities of A2, it will be necessary to drive CAPT and CAPB with two high speed, low noise amplifiers. In this case, both internal amplifiers (i.e., A1 and A2) must be disabled by connecting SENSE to AVDD, connecting VREF to AVSS and removing the capacitive decoupling network. The external voltages applied to CAPT and CAPB must be 2.0 V + Input Span/4 and 2.0 V – Input Span/4, respectively, in which the input span can be varied between 2 V and 4 V. Note that those samples within the pipeline ADC during any reference transition will be corrupted and should be discarded.

DRIVING THE ANALOG INPUTS

The AD9225 has a highly flexible input structure allowing it to interface with single ended or differential input interface circuitry. The applications shown in this section and the Reference Configurations section along with the information presented in the Input and Reference Overview give examples of single-ended and differential operation. Refer to Tables I and II for a list of the different possible input and reference configurations and their associated figures in the data sheet.

The optimum mode of operation, analog input range, and associated interface circuitry will be determined by the particular applications performance requirements as well as power supply options. For example, a dc-coupled single-ended input would be appropriate for most data acquisition and imaging applications. Many communication applications, which require a dc-coupled input for proper demodulation, can take advantage of the excellent single-ended distortion performance of the AD9225. The input span should be configured so the system's performance objectives and the headroom requirements of the driving op amp are simultaneously met.

Table I. Analog Input Configuration Summary

Input Connection	Coupling	Input Span (V)	Input Range (V) VINA*	Input Range (V) VINB*	Figure No.	Comments
Single-Ended	DC	2	0 to 2	1	8, 9	Best for stepped input response applications; requires ±5 V op amp.
		2 × VREF	0 to 2 × VREF	VREF	8, 9	Same as above but with improved noise performance due to increase in dynamic range. Headroom/settling time requirements of ±5 V op amp should be evaluated.
		4	0 to 4	2.0	8, 9	Optimum noise performance, excellent THD performance, often requires low distortion op amp with VCC > +5 V due to its headroom issues.
		2 × VREF	2.0 – VREF to 2.0 + VREF	2.0	21	Optimum THD performance with VREF = 1. Single-supply operation (i.e., +5 V) for many op amps.
Single-Ended	AC	2 or 2 × VREF	0 to 1 or 0 to 2 × VREF	1 or VREF	10, 11	
		4	0.5 to 4.5	2.0	11	Optimum noise performance, excellent THD performance; ability to use ±5 V op amp.
		2 × VREF	2.0 – VREF to 2.0 + VREF	2.0	10	Flexible input range, optimum THD performance with VREF = 1. Ability to use either +5 V or ±5 V op amp.
Differential (via Transformer) or Amplifier	AC/DC	2	2 to 3	3 to 2	12, 13	Optimum full-scale THD and SFDR performance well beyond the ADC's Nyquist frequency. Preferred mode for undersampling applications.
		2 × VREF	2.0 – VREF/2 to 2.0 + VREF/2	2.0 + VREF/2 to 2.0 – VREF/2	12, 13	Same as above with the exception that full-scale THD and SFDR performance can be traded off for better noise performance.
		4.0	1.5 to 3.5	3.5 to 1.5	12, 13	Optimum noise performance.

*VINA and VINB can be interchanged if signal inversion is required.

Table II. Reference Configuration Summary

Reference Operating Mode	Input Span (VINA–VINB) (V p-p)	Required VREF (V)	Connect	To
Internal	2	1	SENSE	VREF
Internal	4	2	SENSE	REFCOM
Internal	2 ≤ SPAN ≤ 4 and SPAN = 2 × VREF	1 ≤ VREF ≤ 2.0 and VREF = (1 + R1/R2)	R1 R2	VREF and SENSE SENSE and REFCOM
External (Nondynamic)	2 ≤ SPAN ≤ 4	1 ≤ VREF ≤ 2.0	SENSE VREF	AVDD External Reference
External (Dynamic)	2 ≤ SPAN ≤ 4	CAPT and CAPB Externally Driven	SENSE VREF External Reference External Reference	AVDD AVSS CAPT CAPB

Differential modes of operation (ac-coupled or dc-coupled input) provide the best THD and SFDR performance over a wide frequency range. Differential operation should be considered for the most demanding spectral based applications (e.g., direct IF-to-digital conversion). See Figures 12 and 13 and the Differential Mode of Operation section. Differential input characterization was performed for this data sheet using the configuration shown in Figure 13.

Single-ended operation requires that VINA be ac-coupled or dc-coupled to the input signal source while VINB of the AD9225 be biased to the appropriate voltage corresponding to a midscale code transition. Note that signal inversion may be easily accomplished by transposing VINA and VINB. Most of the single-ended specifications for the AD9225 are characterized using Figure 21 circuitry with input spans of 4 V and 2 V as well as VINB = 2.5 V.

Differential operation requires that VINA and VINB be simultaneously driven with two equal signals that are in and out of phase versions of the input signal. Differential operation of the AD9225 offers the following benefits: (1) Signal swings are smaller and, therefore, linearity requirements placed on the input signal source may be easier to achieve, (2) Signal swings are smaller and therefore may allow the use of op amps which may otherwise have been constrained by headroom limitations, (3) Differential operation minimizes even-order harmonic products, and (4) Differential operation offers noise immunity based on the device's common-mode rejection.

As is typical of most IC devices, exceeding the supply limits will turn on internal parasitic diodes resulting in transient currents within the device. Figure 7 shows a simple means of clamping an ac-coupled or dc-coupled single-ended input with the addition of two series resistors and two diodes. An optional capacitor is shown for ac-coupled applications. Note that a larger series resistor could be used to limit the fault current through D1 and D2 but should be evaluated since it can cause a degradation in overall performance. A similar clamping circuit could also be used for each input if a differential input signal is being applied. The diodes might cause nonlinearities in the signal. Careful evaluation should be performed on the diodes used.

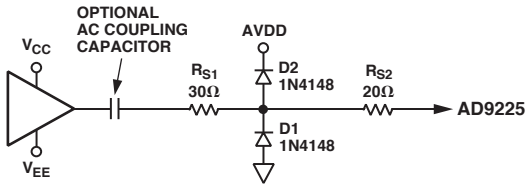


Figure 7. Simple Clamping Circuit

SINGLE-ENDED MODE OF OPERATION

The AD9225 can be configured for single-ended operation using dc-coupling or ac-coupling. In either case, the input of the ADC must be driven from an operational amplifier that will not degrade the ADC's performance. Because the ADC operates from a single supply, it will be necessary to level shift ground based bipolar signals to comply with its input requirements. Both dc and ac coupling provide this necessary function, but each method results in different interface issues that may influence the system design and performance.

Single-ended operation is often limited by the availability of driving op amps. Very low distortion op amps that provide great performance out to the Nyquist frequency of the converter are hard to find. Compounding the problem, for dc-coupled, single-ended applications, is the inability of many high performance amplifiers to maintain low distortions as their outputs approach their positive output voltage limit (i.e., 1 dB compression point). For this reason, it is recommended that applications requiring high performance dc coupling use the single-ended-to-differential circuit shown in Figure 12.

DC COUPLING AND INTERFACE ISSUES

Many applications require the analog input signal to be dc-coupled to the AD9225. An operational amplifier can be configured to rescale and level shift the input signal so that it is compatible with the selected input range of the ADC. The input range to the ADC should be selected on the basis of system performance objectives, as well as the analog power supply availability since this will place certain constraints on the op amp selection.

Many of the new high performance op amps are specified for only ±5 V operation and have limited input/output swing capabilities. The selected input range of the AD9225 should be considered with the headroom requirements of the particular op amp to prevent clipping of the signal. Since the output of a dual supply amplifier can swing below –0.3 V, clamping its output should be considered in some applications.

In some applications, it may be advantageous to use an op amp specified for single-supply +5 V operation since it will inherently limit its output swing to within the power supply rails. Amplifiers like the AD8041 and AD8011 are useful for this purpose but their low bandwidths will limit the AD9225's performance. High performance amplifiers, such as the AD9631, AD9632, AD8056, or AD8055, allow the AD9225 to be configured for larger input spans which will improve the ADC's noise performance.

Op amp circuits using a noninverting and inverting topology are discussed in the next section. Although not shown, the noninverting and inverting topologies can be easily configured as part of an antialiasing filter by using a Sallen-Key or multiple-feedback topology. An additional R-C network can be inserted between the op amp output and the AD9225 input to provide a filter pole.

Simple Op Amp Buffer

In the simplest case, the input signal to the AD9225 will already be biased at levels in accordance with the selected input range. It is simply necessary to provide an adequately low source impedance for the VINA and VINB analog pins of the ADC. Figure 8 shows the recommended configuration a single-ended drive using an op amp. In this case, the op amp is shown in a noninverting unity gain configuration driving the VINA pin. The internal reference drives the VINB pin. Note that the addition of a small series resistor of 30 Ω to 50 Ω connected to VINA and VINB will be beneficial in nearly all cases. Refer to the Analog Input Operation section on a discussion on resistor selection. Figure 8 shows the proper connection for a 0 V to 4 V input range. Alternative single-ended ranges of 0 V to 2 × VREF can also be realized with the proper configuration of VREF (refer to the Using the Internal Reference section). Headroom limitations of the op amp must always be considered.

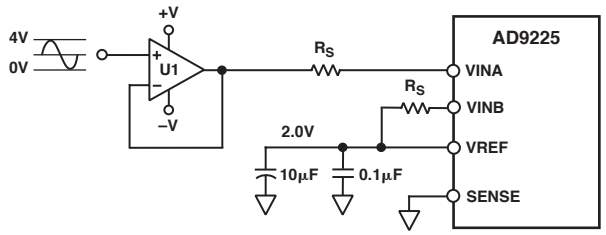


Figure 8. Single-Ended AD9225 Op Amp Drive Circuit

Op Amp with DC Level Shifting

Figure 9 shows a dc-coupled level shifting circuit employing an op amp, A1, to sum the input signal with the desired dc set. Configuring the op amp in the inverting mode with the given resistor values results in an ac signal gain of –1. If the signal inversion is undesirable, interchange the VINA and VINB connections to re-establish the original signal polarity. The dc voltage at VREF sets the common-mode voltage of the AD9225. For example, when VREF = 2.0 V, the input level from the op amp will also be centered around 2.0 V. The use of ratio matched, thin-film resistor networks will minimize gain and offset errors. Also, an optional pull-up resistor, RP, may be used to reduce the output load on VREF to less than its 1 mA maximum.

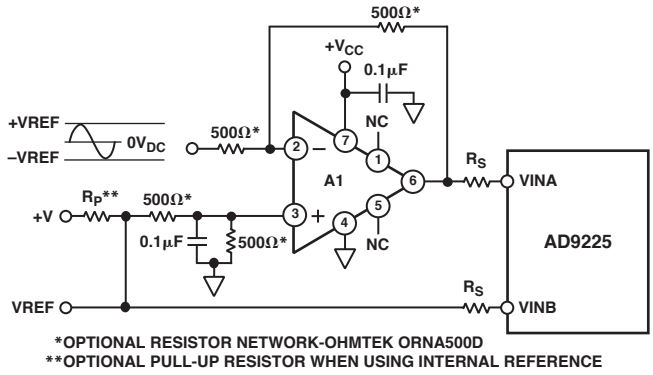


Figure 9. Single-Ended Input with DC-Coupled Level Shift

AC COUPLING AND INTERFACE ISSUES

For applications where ac coupling is appropriate, the op amp output can be easily level-shifted via a coupling capacitor. This has the advantage of allowing the op amp common-mode level to be symmetrically biased to its midsupply level (i.e., $(V_{CC} + V_{EE})/2$). Op amps that operate symmetrically with respect to their power supplies typically provide the best ac performance as well as greatest input/output span. Various high speed/performance amplifiers which are restricted to +5 V/–5 V operation and/or specified for +5 V single-supply operation can be easily configured for the 4 V or 2 V input span of the AD9225. Note that differential transformer coupling, which is another form of ac coupling, should be considered for optimum ac performance.

Simple AC Interface

Figure 10 shows a typical example of an ac-coupled, single-ended configuration. The bias voltage shifts the bipolar, ground-referenced input signal to approximately AVDD/2. The value for C1 and C2 will depend on the size of the resistor, R. The capacitors, C1 and C2, are a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. The combination of the capacitor and the resistor form a high-pass filter with a high-pass –3 dB frequency determined by the equation

$$f_{-3\,dB} = 1/(2 \times \pi \times R \times (C1 + C2))$$

The low impedance VREF voltage source biases both the VINB input and provides the bias voltage for the VINA input. Figure 10 shows the VREF configured for 2.0 V thus the input range of the ADC is 0 V to 4 V. Other input ranges could be selected by changing VREF.

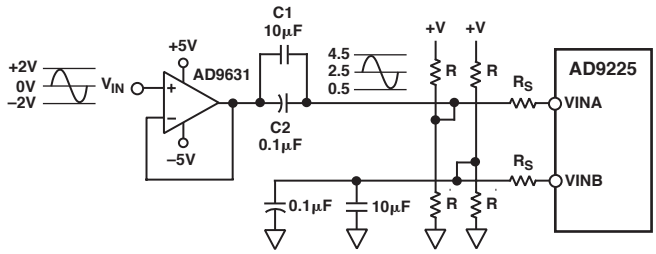


Figure 10. AC-Coupled Input

Alternative AC Interface

Figure 11 shows a flexible ac-coupled circuit that can be configured for different input spans. Since the common-mode voltage of VINA and VINB are biased to midsupply independent of VREF, VREF can be pin strapped or reconfigured to achieve input spans between 2 V and 4 V p-p. The AD9225's CMRR along with the symmetrical coupling R-C networks will reject both power supply variations and noise. The resistors, R, establish the common-mode voltage. They may have a high value (e.g., 5 kΩ) to minimize power consumption and establish a low cutoff frequency. The capacitors, C1 and C2, are typically a 0.1 µF ceramic and 10 µF tantalum capacitor in parallel to achieve a low cutoff frequency while maintaining a low impedance over a wide frequency range. R_S isolates the buffer amplifier from the ADC input. The optimum performance is achieved when VINA and VINB are driven via symmetrical networks. The $f_{-3\,dB}$ point can be approximated by the equation

$$f_{-3\,dB} = \frac{1}{2\,\pi \times 6K + (C1 + C2)}$$

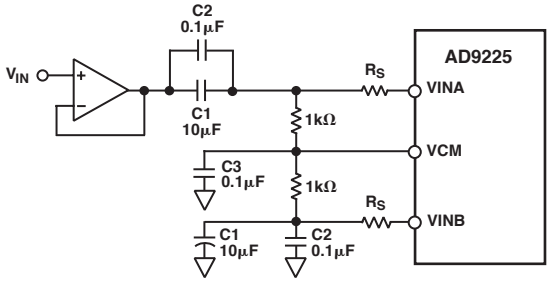


Figure 11. AC-Coupled Input-Flexible Input Span, V_{CM} = 2.5 V

OP AMP SELECTION GUIDE

Op amp selection for the AD9225 is highly dependent on the particular application. In general, the performance requirements of any given application can be characterized by either time domain or frequency domain parameters. In either case, one should carefully select an op amp that preserves the performance of the ADC. This task becomes challenging when the AD9225's high performance capabilities are coupled with other extraneous system level requirements such as power consumption and cost.

The ability to select the optimal op amp may be further complicated by either limited power supply availability and/or limited acceptable supplies for a desired op amp. Newer, high performance op amps typically have input and output range limitations in accordance with their lower supply voltages. As a result, some op amps will be more appropriate in systems where ac coupling is allowable. When dc coupling is required, op amps without headroom constraints such as rail-to-rail op amps or the ones where larger supplies can be used should be considered. The following section describes some op amps currently available from Analog Devices, Inc. The system designer is always encouraged to contact the factory or local sales office to be updated on Analog Devices' latest amplifier product offerings. Highlights of the areas where the op amps excel and where they may limit the performance of the AD9225 is also included.

AD8055: $f_{-3\ dB}$ = 300 MHz.
Low cost. Best used for driving single-ended ac-coupled configuration.
Limit: THD is compromised when output is not swinging about 0 V.

AD8056: Dual Version of above amp.
Perfect for single-ended to differential configuration (see Figure 12). Harmonics cancel each other in differential drive, making this amplifier highly recommended for a single-ended input signal source. Handles input signals past the 20 MHz Nyquist frequency.

AD9631: $f_{-3\ dB}$ = 250 MHz.
Moderate cost.
Good for single-ended drive applications when signal is anywhere between 0 V and 3 V.
Limits: THD is compromised above 8 MHz.

DIFFERENTIAL MODE OF OPERATION

Since not all applications have a signal preconditioned for differential operation, there is often a need to perform a single-ended-to-differential conversion. In systems that do not need to be dc-coupled, an RF transformer with a center tap is the best method to generate differential inputs for the AD9225. It provides all the benefits of operating the ADC in the differential mode without contributing additional noise or distortion. An RF transformer also has the added benefit of providing electrical isolation between the signal source and the ADC.

An improvement in THD and SFDR performance can be realized by operating the AD9225 in the differential mode. The performance enhancement between the differential and single-ended mode is most noteworthy as the input frequency approaches and goes beyond the Nyquist frequency (i.e., $f_{IN} > f_S/2$).

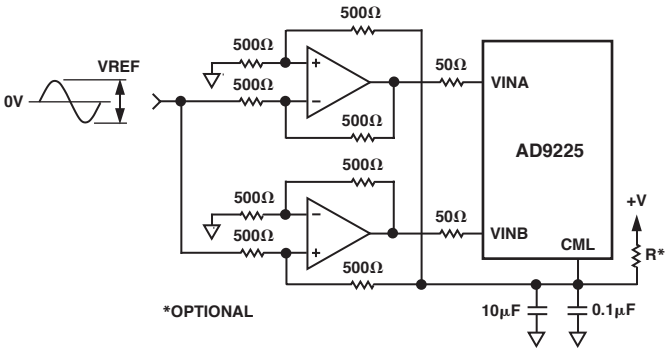


Figure 12. Direct Coupled Drive Circuit with AD8056 Dual Op Amp

The circuit shown in Figure 12 is an ideal method of applying a differential dc drive to the AD9225. We have used this configuration to drive the AD9225 from 2 V to 4 V spans at frequencies approaching Nyquist with performance numbers matching those listed in the Specifications tables (gathered through a transformer). The dc input is shifted to a dc point swinging symmetrically about the reference voltage. The optional resistor will provide additional current if more reference drive is required.

The driver circuit shown in Figure 12 is optimized for dc coupling applications requiring optimum distortion performance. This differential op amp driver circuit is configured to convert and level shift a 2 V p-p single-ended, ground referenced signal to a 4 V p-p differential signal centered at the VREF level of the ADC. The circuit is based on two op amps that are configured as matched unity gain difference amplifiers. The single-ended input signal is applied to opposing inputs of the difference amplifiers, thus providing differential drive. The common-mode offset voltage is applied to the noninverting resistor leg of each difference amplifier providing the required offset voltage. The common-mode offset can be varied over a wide span without any serious degradation in distortion performance as shown in Figures 14 and 15, thus providing some flexibility in improving output compression distortion from some ±5 V op amps with limited positive voltage swing.

To protect the AD9225 from an undervoltage fault condition from op amps specified for ±5 V operation, two diodes to AGND can be inserted between each op amp output and the AD9225 inputs. The AD9225 will inherently be protected against any overvoltage condition if the op amps share the same positive power supply (i.e., AVDD) as the AD9225. Note that the gain accuracy and common-mode rejection of each difference amplifier in this driver circuit can be enhanced by using a matched thin-film resistor network (i.e., Ohmtek ORNA5000F) for the op amps. Recall that the AD9225's small signal bandwidth is 105 MHz and therefore, any noise falling within the baseband bandwidth of the AD9225 will degrade its overall noise performance.

The noise performance of each unity gain differential driver circuit is limited by its inherent noise gain of 2. For unity gain op amps ONLY, the noise gain can be reduced from 2 to 1 beyond the input signals passband by adding a shunt capacitor, C_F, across each op amp's feedback resistor. This will essentially establish a low-pass filter, which reduces the noise gain to 1 beyond the filter's $f_{-3\ dB}$ while simultaneously bandlimiting the input signal to $f_{-3\ dB}$. Note that the pole established by this filter can also be used as the real pole of an antialiasing filter.

Figure 13 shows the schematic of the suggested transformer circuit. The circuit uses a minicircuits RF transformer, model #T4-1T, which has an impedance ratio of 4 (turns ratio of 2). The schematic assumes that the signal source has a 50 Ω source impedance. The 1:4 impedance ratio requires the 200 Ω secondary termination for optimum power transfer and VSWR. The center tap of the transformer provides a convenient means of level-shifting the input signal to a desired common-mode voltage.

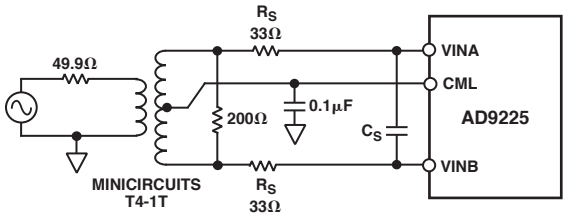


Figure 13. Transformer Coupled Input

The configuration in Figure 13 was used to gather the differential data on the Specifications tables.

Transformers with other turns ratios may also be selected to optimize the performance of a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. For example, selecting a transformer with a higher impedance ratio (e.g., Minicircuits T16-6T with a 1:16 impedance ratio) effectively steps up the signal level further reducing the driving requirements of the signal source.

Referring to Figure 13, a series resistors, R_S, and shunt capacitor, C_S, were inserted between the AD9225 and the secondary of the transformer. The value of 33 Ω was selected to specifically optimize both the THD and SNR performance of the ADC. R_S and C_S help provide a low-pass filter to block high frequency noise.

The AD9225 can be easily configured for either a 2 V p-p input span or a 4.0 V p-p input span by setting the internal reference (see Table II). Other input spans can be realized with two external gain setting resistors as shown in Figure 19. Figures 14 and 15 demonstrate how both spans of the AD9225 achieve the high degree of linearity and SFDR over a wide range of amplitudes required by the most demanding communication applications.

Figures 14 and 15 demonstrate the flexibility of common-mode voltage (transformer center tap) with respect to THD.

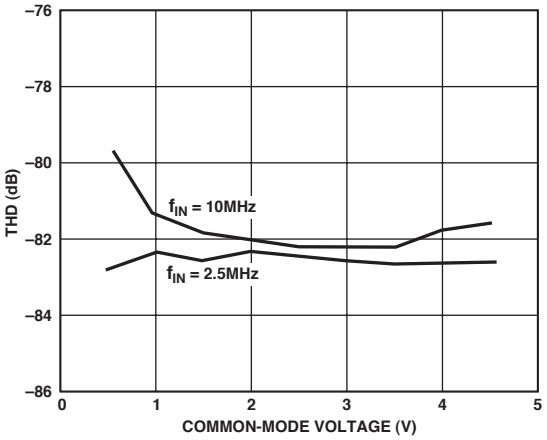


Figure 14. Common-Mode Voltage vs. THD (A_{IN} = 2 V Differential)

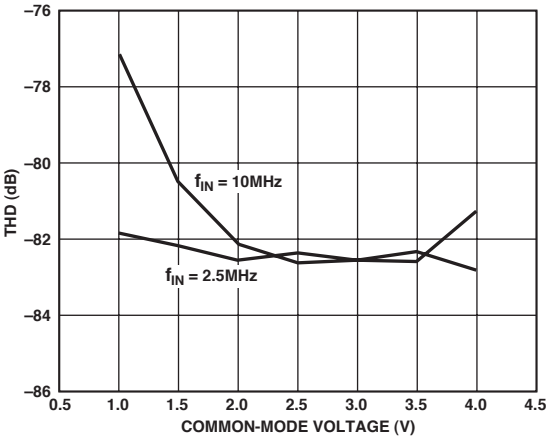


Figure 15. Common-Mode Voltage vs. THD (A_{IN} = 4 V Differential)

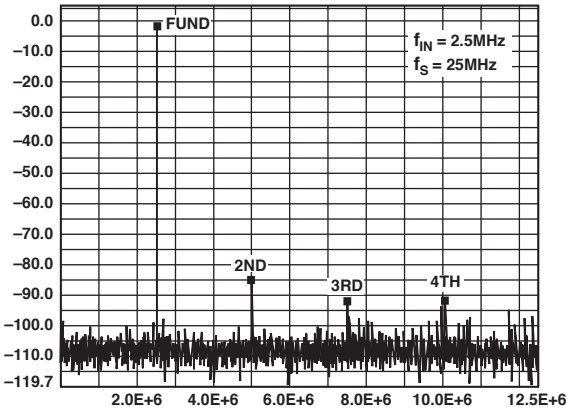


Figure 16. Single-Tone Frequency Domain Plot Common-Mode Voltage = 2.5 V (A_{IN} = 4 V Differential)

REFERENCE CONFIGURATIONS

The figures associated with this section on internal and external reference operation do not show recommended matching series resistors for VINA and VINB for the purpose of simplicity. Refer to the Driving the Analog Inputs and Introduction sections for a discussion of this topic. The figures do not show the decoupling network associated with the CAPT and CAPB pins. Refer to the Reference Operation section for a discussion of the internal reference circuitry and the recommended decoupling network shown in Figure 16.

USING THE INTERNAL REFERENCE

Single-Ended Input with 0 to 2 3 VREF Range

Figure 16 shows how to connect the AD9225 for a 0 V to 2 V or 0 V to 4 V input range via pin strapping the SENSE pin. An intermediate input range of 0 to 2 × VREF can be established using the resistor programmable configuration in Figure 19.

In either case, both the midscale voltage and input span are directly dependent on the value of VREF. More specifically, the midscale voltage is equal to VREF while the input span is equal to 2 × VREF. Thus, the valid input range extends from 0 to 2 × VREF. When VINA is ≤ 0 V, the digital output will be 0x000; when VINA is ≥ 2 × VREF, the digital output will be 0xFFF.

Shorting the VREF pin directly to the SENSE pin places the internal reference amplifier in unity-gain mode and the resulting VREF output is 1 V. Therefore, the valid input range is 0 V to 2 V. However, shorting the SENSE pin directly to the REFCOM pin configures the internal reference amplifier for a gain of 2.0 and the resulting VREF output is 2.0 V. Therefore, the valid input range becomes 0 V to 4 V. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

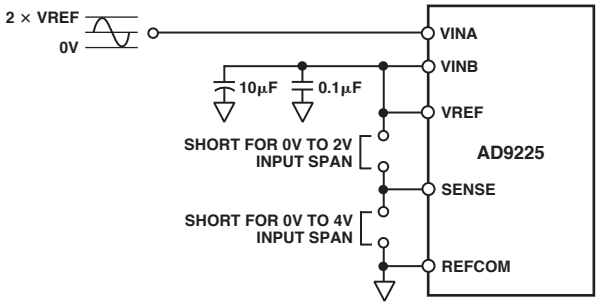


Figure 17. Internal Reference—2 V p-p Input Span, V_{CM} = 1 V, or 4 V p-p Input Span

Figure 18 shows the single-ended configuration that gives good dynamic performance (SINAD, SFDR). To optimize dynamic specifications, center the common-mode voltage of the analog input at approximately by 2.5 V by connecting VINB to a low impedance 2.5 V source. As described above, shorting the VREF pin directly to the SENSE pin results in a 1 V reference voltage and a 2 V p-p input span. The valid range for input signals is 1.5 V to 3.5 V. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low-inductance 0.1 µF ceramic capacitor.

This reference configuration could also be used for a differential input in which VINA and VINB are driven via a transformer as shown in Figure 13. In this case, the common-mode voltage, VCM , is set at midsupply by connecting the transformer's center tap to CML of the AD9225. VREF can be configured for 1.0 V or 2.0 V by connecting SENSE to either VREF or REFCOM, respectively. Note that the valid input range for each of the differential inputs is one half of the single-ended input and thus becomes VCM – VREF/2 to VCM + VREF/2.

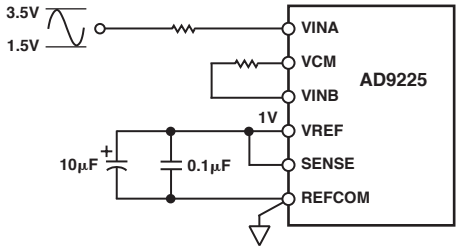


Figure 18. Internal Reference—2 V p-p Input Span, V_{CM} = 2.5 V

Resistor Programmable Reference

Figure 19 shows an example of how to generate a reference voltage other than 1.0 V or 2.0 V with the addition of two external resistors and a bypass capacitor. Use the equation

$$VREF = 1\ V \times (1 + R1/R2)$$

to determine appropriate values for R1 and R2. These resistors should be in the 2 kΩ to 100 kΩ range. For the example shown, R1 equals 2.5 kΩ and R2 equals 5 kΩ. From the equation above, the resultant reference voltage on the VREF pin is 1.5 V. This sets the input span to be 3 V p-p. To assure stability, place a 0.1 µF ceramic capacitor in parallel with R1.

The midscale voltage can be set to VREF by connecting VINB to VREF to provide an input span of 0 to 2 × VREF. Alternatively, the midscale voltage can be set to 2.5 V by connecting VINB to a low impedance 2.5 V source. For the example shown, the valid input single-ended range for VINA is 1 V to 4 V since VINB is set to an external, low impedance 2.5 V source. The VREF pin should be bypassed to the REFCOM pin with a 10 µF tantalum capacitor in parallel with a low inductance 0.1 µF ceramic capacitor.

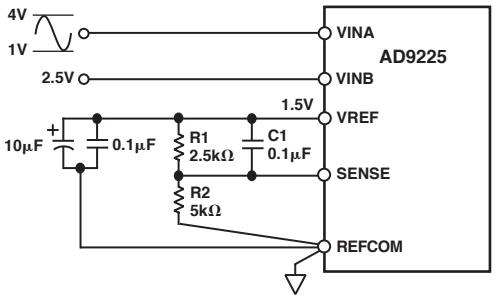


Figure 19. Resistor Programmable Reference 3 V p-p Input Span, V_{CM} = 2.5 V

USING AN EXTERNAL REFERENCE

Using an external reference may enhance the dc performance of the AD9225 by improving drift and accuracy. Figures 20 and 21 show examples of how to use an external reference with the ADC. Table III is a list of suitable voltage references from Analog Devices. To use an external reference, the user must disable the internal reference amplifier and drive the VREF pin. Connecting the SENSE pin to AVDD disables the internal reference amplifier.

Table III. Suitable Voltage References

	Output Voltage	Drift (ppm/°C)	Initial Accuracy % (max)	Operating Current
Internal	1.00	26	1.4	1 mA
AD589	1.235	10–100	1.2–2.8	50 μA
AD1580	1.225	50–100	0.08–0.8	50 μA
REF191	2.048	5–25	0.1–0.5	45 μA
Internal	2.0	26	1.4	1 mA

The AD9225 contains an internal reference buffer, A2 (see Figure 5), that simplifies the drive requirements of an external reference. The external reference must be able to drive about 5 kΩ (±20%) load. Note that the bandwidth of the reference buffer is deliberately left small to minimize the reference noise contribution. As a result, it is not possible to change the reference voltage rapidly in this mode.

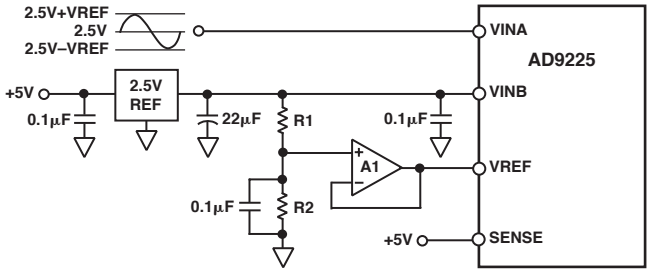


Figure 20. External Reference

Variable Input Span with V_{CM} = 2.5 V

Figure 20 shows an example of the AD9225 configured for an input span of 2 × VREF centered at 2.5 V. An external 2.5 V reference drives the VINB pin thus setting the common-mode voltage at 2.5 V. The input span can be independently set by a voltage divider consisting of R1 and R2, which generates the VREF signal. A1 buffers this resistor network and drives VREF. Choose this op amp based on accuracy requirements. It is essential that a minimum of a 10 μF capacitor in parallel with a 0.1 μF low inductance ceramic capacitor decouple A1's output to ground.

Single-Ended Input with 0 to 2 × VREF Range

Figure 21 shows an example of an external reference driving both VINB and VREF. In this case, both the common-mode voltage and input span are directly dependent on the value of VREF. More specifically, the common-mode voltage is equal to VREF while the input span is equal to 2 × VREF. The valid input range extends from 0 to 2 × VREF. For example, if the REF191, a 2.048 V external reference was selected, the valid input range extends from 0 to 4.096 V. In this case, 1 LSB of the AD9225 corresponds to 1 mV. It is essential that a minimum of a 10 μF capacitor in parallel with a 0.1 μF low inductance ceramic capacitor decouple the reference output to ground.

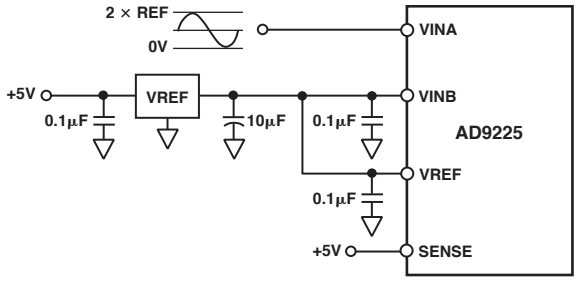


Figure 21. Input Range = 0 V to 2× VREF

DIGITAL INPUTS AND OUTPUTS

Digital Outputs

The AD9225 output data is presented in positive true straight binary for all input ranges. Table IV indicates the output data formats for various input ranges regardless of the selected input range. A twos complement output data format can be created by inverting the MSB.

Table IV. Output Data Format

Input (V)	Condition (V)	Digital Output	OTR
VINA–VINB	< – VREF	0000 0000 0000	1
VINA–VINB	= – VREF	0000 0000 0000	0
VINA–VINB	= 0	1000 0000 0000	0
VINA–VINB	= + VREF – 1 LSB	1111 1111 1111	0
VINA–VINB	≥ + VREF	1111 1111 1111	1

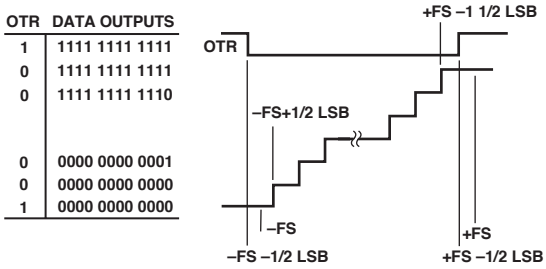


Figure 22. Output Data Format

Out-Of-Range (OTR)

An out-of-range condition exists when the analog input voltage is beyond the input range of the converter. OTR is a digital output that is updated along with the data output corresponding to the particular sampled analog input voltage. OTR has the same pipeline delay (latency) as the digital data. It is low when the analog input voltage is within the analog input range. It is high when the analog input voltage exceeds the input range as shown in Figure 23. OTR will remain high until the analog input returns within the input range and another conversion is completed. By logical ANDing OTR with the MSB and its complement, overrange high or underrange low conditions can be detected. Table V is a truth table for the overrange circuit in Figure 24 which uses NAND gates. Systems requiring programmable gain conditioning of the AD9225 input signal can immediately detect an out-of-range condition, eliminating gain selection iterations. OTR can also be used for digital offset and gain calibration.

Table V. Out-of-Range Truth Table

OTR	MSB	Analog Input Is
0	0	In Range
0	1	In Range
1	0	Underrange
1	1	Overrange

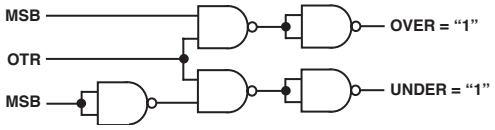


Figure 23. Overrange or Underrange Logic

Digital Output Driver Considerations (DRVDD)

The AD9225 output drivers can be configured to interface with 5 V or 3.3 V logic families by setting DRVDD to 5 V or 3.3 V, respectively. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause glitches on the supplies and may affect SINAD performance. Applications requiring the ADC to drive large capacitive loads or large fanout may require additional decoupling capacitors on DRVDD. In extreme cases, external buffers or latches may be required.

Clock Input and Considerations

The AD9225 internal timing uses the two edges of the clock input to generate a variety of internal timing signals. The clock input must meet or exceed the minimum specified pulse width high and low (t_{CH} and t_{CL}) specifications for the given ADC as defined in the Switching Specifications table to meet the rated performance specifications. For example, the clock input to the AD9225 operating at 25 MSPS may have a duty cycle between 45% to 55% to meet this timing requirement since the minimum specified t_{CH} and t_{CL} is 18 ns. For low clock rates, the duty cycle may deviate from this range to the extent that both t_{CH} and t_{CL} are satisfied.

All high speed high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{IN}) due to only aperture jitter (t_A) can be calculated with the following equation:

$$SNR = 20 \log_{10}\left[\frac{1}{2\pi f_{IN} t_A}\right]$$

In the equation, the rms aperture jitter, t_A, represents the root-sum square of all the jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

Clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9225. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter crystal controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other method), it should be retimed by the original clock at the last step.

The clock input is referred to as the analog supply. Its logic threshold is AVDD/2. If the clock is being generated by 3 V logic, it will have to be level shifted into 5 V CMOS logic levels. This can also be accomplished by ac coupling and level-shifting the clock signal.

The AD9225 has a clock tolerance of 5% at 25 MHz. One way to obtain a 50% duty cycle clock is to divide down a clock of higher frequency, as shown in Figure 24. This configuration will also decrease the jitter of the source clock.

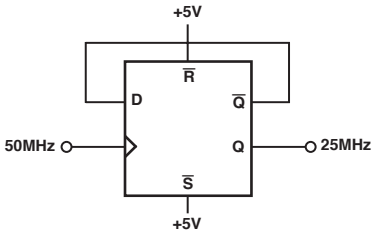


Figure 24. Divide-by-Two Clock Circuit

In this case, a 50 MHz clock is divided by two to produce the 25 MHz clock input for the AD9225. In this configuration, the duty cycle of the 50 MHz clock is irrelevant.

The input circuitry for the CLOCK pin is designed to accommodate CMOS inputs. The quality of the logic input, particularly the rising edge, is critical in realizing the best possible jitter performance of the part; the faster the rising edge, the better the jitter performance.

As a result, careful selection of the logic family for the clock driver, as well as the fanout and capacitive load on the clock line, is important. Jitter-induced errors become more predominant at higher frequency and large amplitude inputs, where the input slew rate is greatest.

Most of the power dissipated by the AD9225 is from the analog power supplies. However, lower clock speeds will reduce digital current. Figure 25 shows the relationship between power and clock rate.

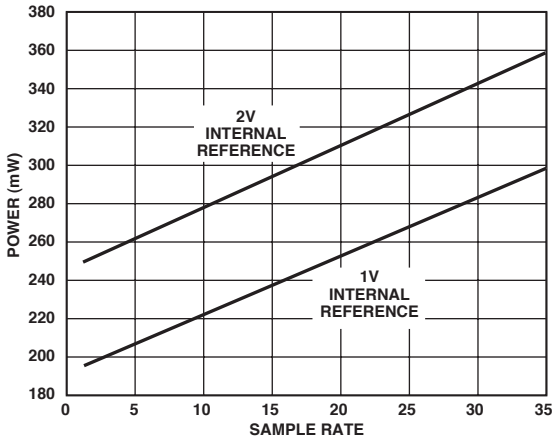


Figure 25. Power Consumption vs. Clock Rate

Direct IF Down Conversion Using the AD9225

Sampling IF signals above an ADC's baseband region (i.e., dc to $f_S/2$) is becoming increasingly popular in communication applications. This process is often referred to as direct IF down conversion or undersampling. There are several potential benefits in using the ADC to alias (i.e., or mix) down a narrowband or wideband IF signal. First and foremost is the elimination of a complete mixer stage with its associated baseband amplifiers and filters, reducing cost and power dissipation. Second is the ability to apply various DSP techniques to perform such functions as filtering, channel selection, quadrature demodulation, data reduction,

and detection, among other things. See Application Note AN-302 on using this technique in digital receivers.

In direct IF down conversion applications, one exploits the inherent sampling process of an ADC in which an IF signal lying outside the baseband region can be aliased back into the baseband region in a similar manner that a mixer will down-convert an IF signal. Similar to the mixer topology, an image rejection filter is required to limit other potential interferring signals from also aliasing back into the ADC's baseband region. A trade-off exists between the complexity of this image rejection filter and the ADC's sample rate as well as dynamic range.

The AD9225 is well suited for various IF sampling applications. The AD9225's low distortion input SHA has a full-power bandwidth extending beyond 130 MHz thus encompassing many popular IF frequencies. A DNL of ±0.4 LSB (typ) combined with low thermal input referred noise allows the AD9225 in the 2 V span to provide 69 dB of SNR for a baseband input sine wave. Its low aperture jitter of 0.8 ps rms ensures minimum SNR degradation at higher IF frequencies. In fact, the AD9225 is capable of still maintaining 68 dB of SNR at an IF of 71 MHz with a 2 V input span. Although the AD9225 can yield a 1 dB to 2 dB improvement in SNR when configured for the larger 4 V span, the 2 V span achieves the optimum full-scale distortion performance at these higher input frequencies. The 2 V span reduces only the performance requirements of the input driver circuitry (i.e., IP3) and thus may also be more attractive from a system implementation perspective.

Figure 26 shows a simplified schematic of the AD9225 configured in an IF sampling application. To reduce the complexity of the digital demodulator in many quadrature demodulation applications, the IF frequency and/or sample rate are strategically selected such that the band-limited IF signal aliases back into the center of the ADC's baseband region (i.e., $f_S/4$). This demodulation technique typically reduces the complexity of the post digital demodulator ASIC that follows the ADC.

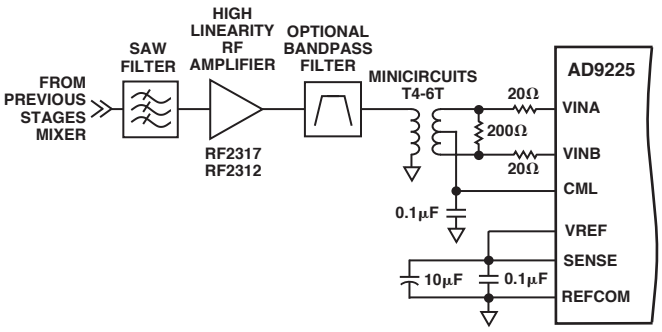


Figure 26. Example of AD9225 IF Sampling Circuit

To maximize its distortion performance, the AD9225 is configured in the differential mode with a 2 V span using a transformer. The center tap of the transformer is biased at midsupply via the CML output of the AD9225. Preceding the AD9225 and transformer is an optional band-pass filter as well as a gain stage. A low Q passive band-pass filter can be inserted to reduce the out-of-band distortion and noise that lies within the AD9225's 130 MHz bandwidth. A large gain stage(s) is often required to compensate for the high insertion losses of a SAW filter used for channel selection and image rejection. The gain stage will also provide adequate isolation for the SAW filter from the charge kickback currents associated with the AD9225's switched capacitor input stage.

The distortion and noise performance of an ADC at the given IF frequency is of particular concern when evaluating an ADC for a narrowband IF sampling application. Both single-tone and dual-tone SFDR versus amplitude are very useful in assessing an ADC's dynamic and static nonlinearities. SNR versus amplitude performance at the given IF is useful in assessing the ADC's noise performance and noise contribution due to aperture jitter. In any application, one is advised to test several units of the same device under the same conditions to evaluate the given applications sensitivity to that particular device.

Figures 27 to 30 combine the dual-tone SFDR as well as single-tone SFDR and SNR performances at IF frequencies of 35 MHz, 45 MHz, 70 MHz, and 85 MHz. Note that the SFDR versus amplitude data is referenced to dBFS while the single-tone SNR data is referenced to dBc. The performance characteristics in these figures are representative of the AD9225 without any preceding gain stage. The AD9225 was operated in the differential mode (via transformer) with a 2 V span and a sample rate between 28 MSPS and 36 MSPS. The analog supply (AVDD) and the digital supply (DRVDD) were set to 5 V and 3.3. V, respectively.

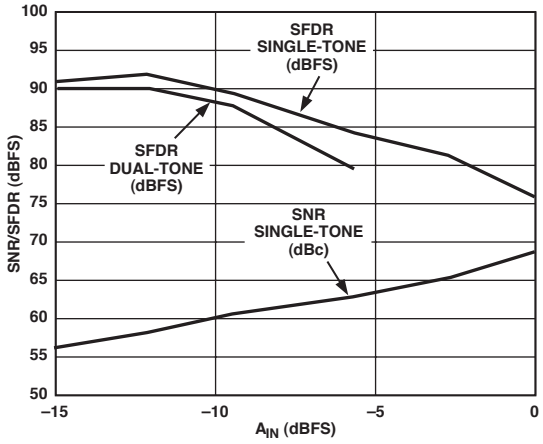


Figure 27. IF Undersampling at 35 MHz (F_1 = 34.63 MHz, F_2 = 35.43 MHz, CLOCK = 20 MHz)

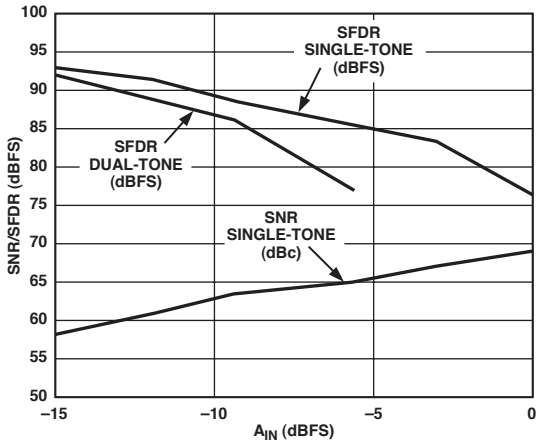


Figure 28. IF Undersampling at 45 MHz (F_1 = 44.81 MHz, F_2 = 45.23 MHz, CLOCK = 20 MHz)

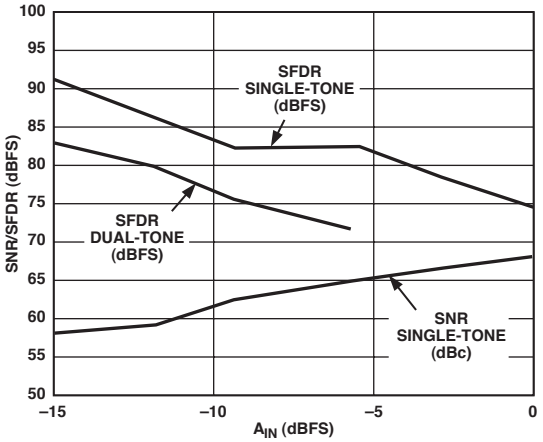


Figure 29. IF Undersampling at 70 MHz (F_1 = 69.50 MHz, F_2 = 70.11 MHz, CLOCK = 25 MHz)

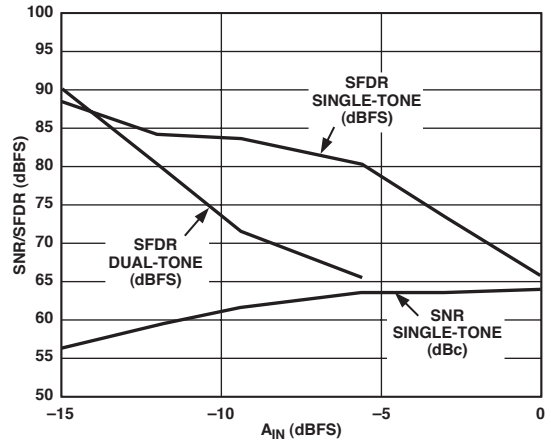


Figure 30. IF Undersampling at 85 MHz (F_1 = 84.81 MHz, F_2 = 85.23 MHz, CLOCK = 20 MHz)

GROUNDING AND DECOUPLING

Analog and Digital Grounding

Proper grounding is essential in any high speed, high resolution system. Multilayer printed circuit boards (PCBs) are recommended to provide optimal grounding and power schemes. The use of ground and power planes offers distinct advantages:

- The minimization of the loop area encompassed by a signal and its return path.
- The minimization of the impedance associated with ground and power paths.
- The inherent distributed capacitor formed by the power plane, PCB insulation and ground plane.

These characteristics result in both a reduction of electromagnetic interference (EMI) and an overall improvement in performance.

It is important to design a layout that prevents noise from coupling onto the input signal. Digital signals should not be run in parallel with input signal traces and should be routed away from the input circuitry. While the AD9225 features separate analog and driver ground pins, it should be treated as an analog component. The AVSS and DRVSS pins must be joined together directly under the AD9225. A solid ground plane under the ADC is acceptable if the power and ground return currents are carefully managed. Alternatively, the ground plane under the ADC may contain serrations to steer currents in predictable directions where cross coupling between analog and digital would otherwise be unavoidable. The AD9225/AD9225EB ground layout, shown in Figure 38, depicts the serrated type of arrangement.

The board is built primarily over a common ground plane. It has a slit to route currents near the clock driver. Figure 31 illustrates a general scheme of ground and power implementation, in and around the AD9225.

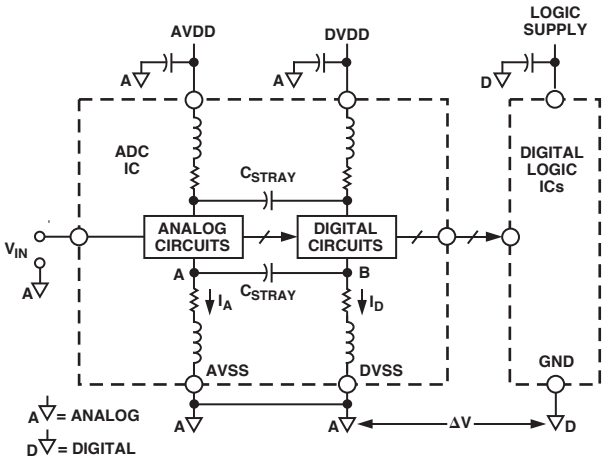


Figure 31. Ground and Power Consideration

Analog and Digital Driver Supply Decoupling

The AD9225 features separate analog and driver supply and ground pins, helping to minimize digital corruption of sensitive analog signals. In general, AVDD, the analog supply, should be decoupled to AVSS, the analog common, as close to the chip as physically possible. Figure 32 shows the recommended decoupling for the analog supplies; 0.1 µF ceramic chip and 10 µF tantalum capacitors should provide adequately low impedance over a wide frequency range. Note that the AVDD and AVSS pins are co-located on the AD9225 to simplify the layout of the decoupling capacitors and provide the shortest possible PCB trace lengths. The AD9225/AD9225EB power plane layout, shown in Figure 39 depicts a typical arrangement using a multilayer PCB.

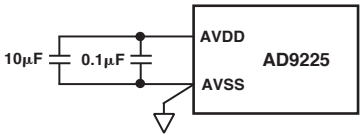


Figure 32. Analog Supply Decoupling

The CML is an internal analog bias point used internally by the AD9225. This pin must be decoupled with at least a 0.1 µF capacitor as shown in Figure 33. The dc level of CML is approximately AVDD/2. This voltage should be buffered if it is to be used for any external biasing.

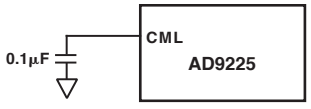


Figure 33. CML Decoupling

The digital activity on the AD9225 chip falls into two general categories: correction logic and output drivers. The internal correction logic draws relatively small surges of current, mainly during the clock transitions. The output drivers draw large current impulses while the output bits are changing. The size and duration of these currents are a function of the load on the output bits; large capacitive loads are to be avoided. Note that the internal correction logic of the AD9225 is referenced to AVDD while the output drivers are referenced to DRVDD.

The decoupling shown in Figure 34, a 0.1 µF ceramic chip capacitor and a 10 µF tantalum capacitor, are appropriate for a reasonable capacitive load on the digital outputs (typically 20 pF on each pin). Applications involving greater digital loads should consider increasing the digital decoupling proportionally, and/or using external buffers/latches.

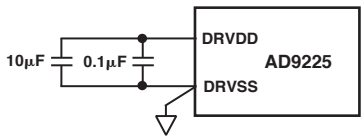


Figure 34. Digital Supply Decoupling

A complete decoupling scheme will also include large tantalum or electrolytic capacitors on the PCB to reduce low frequency ripple to negligible levels. Refer to the AD9225/AD9225EB schematic and layouts in Figures 35 to 41 for more information regarding the placement of decoupling capacitors.

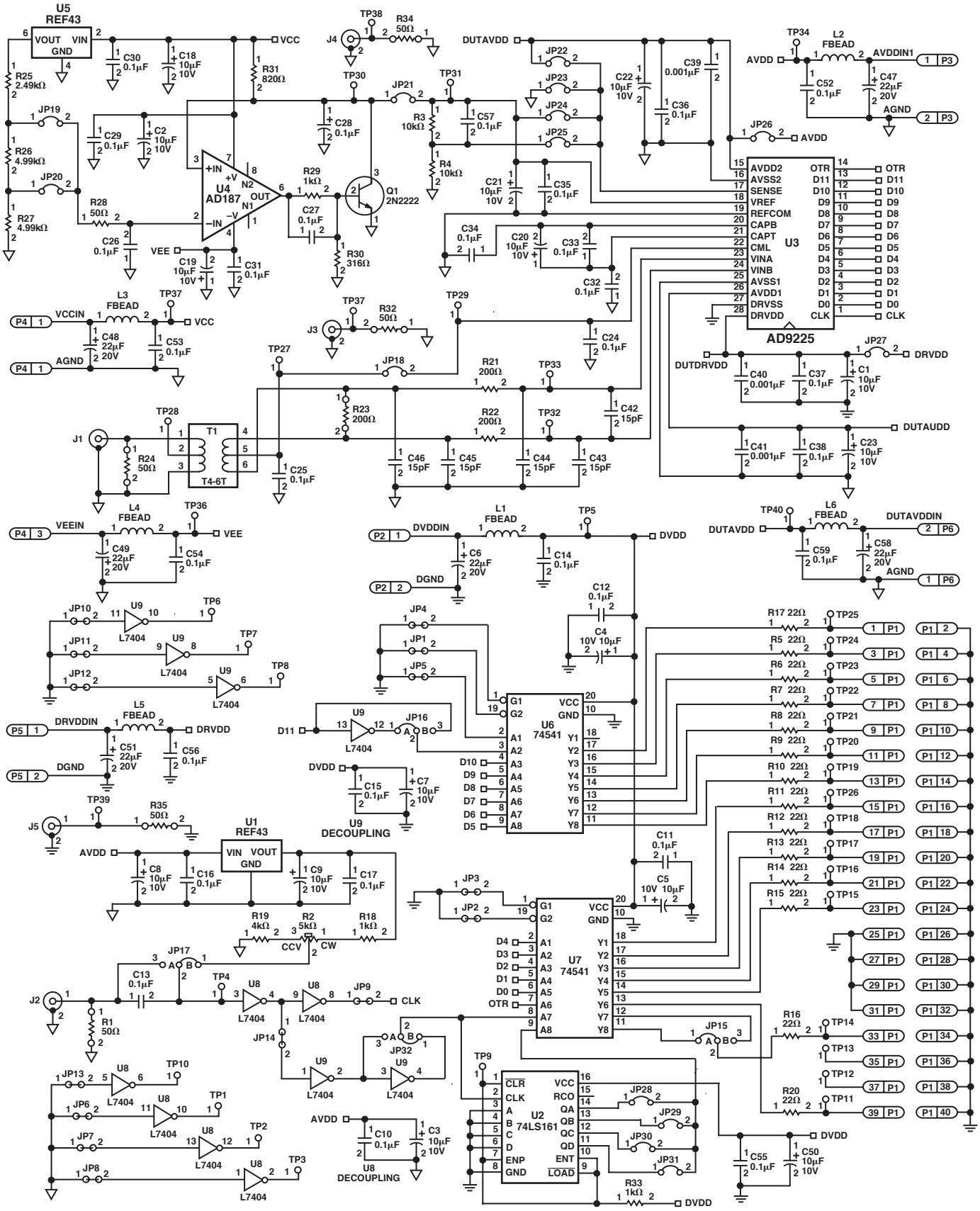


Figure 35. Evaluation Board Schematic

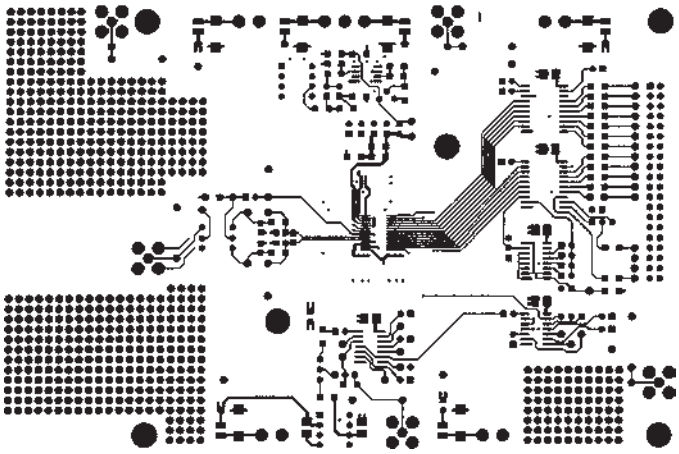


Figure 36. Evaluation Board Component Side Layout (Not to Scale)

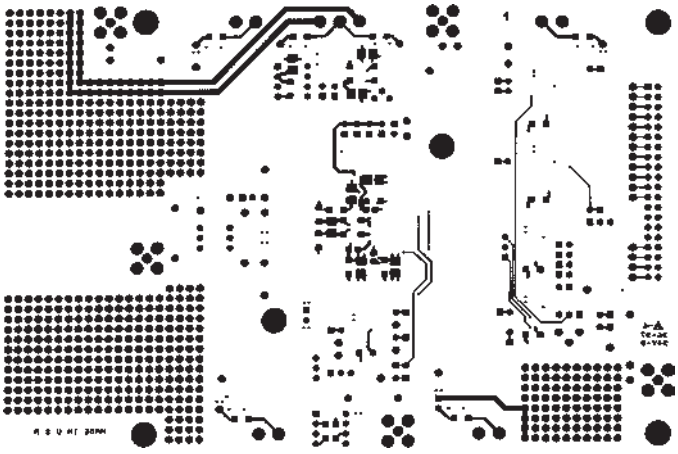


Figure 39. Evaluation Board Solder Side Layout (Not to Scale)

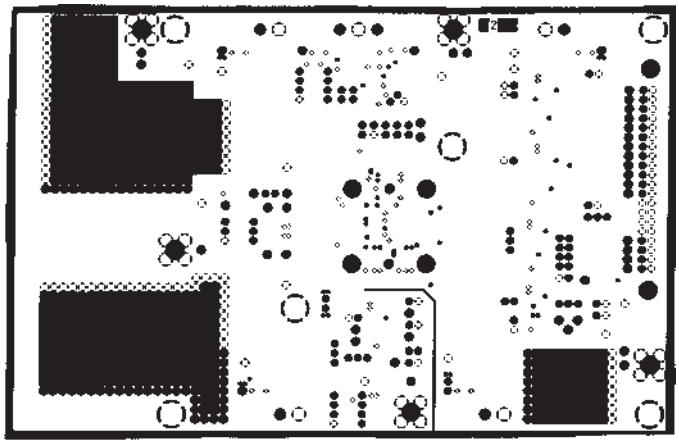


Figure 37. Evaluation Board Ground Plane Layout (Not to Scale)

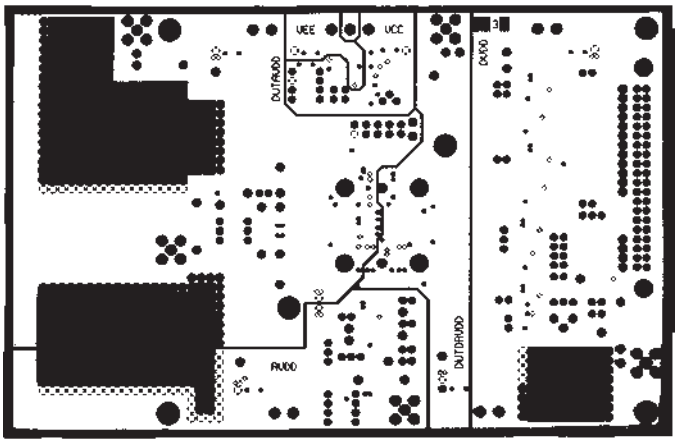


Figure 40. Evaluation Board Power Plane Layout

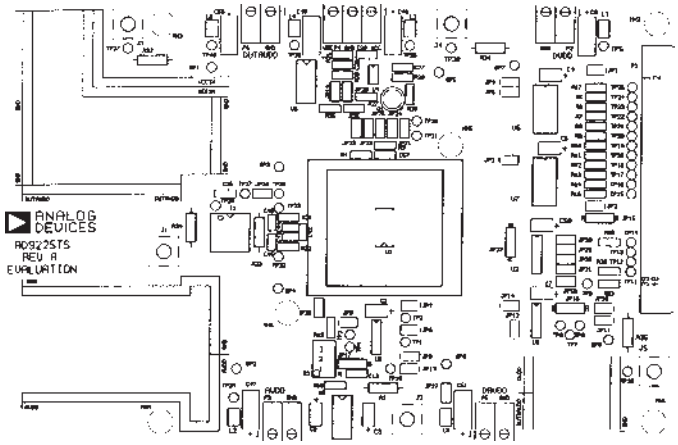


Figure 38. Evaluation Board Component Side Silkscreen (Not to Scale)

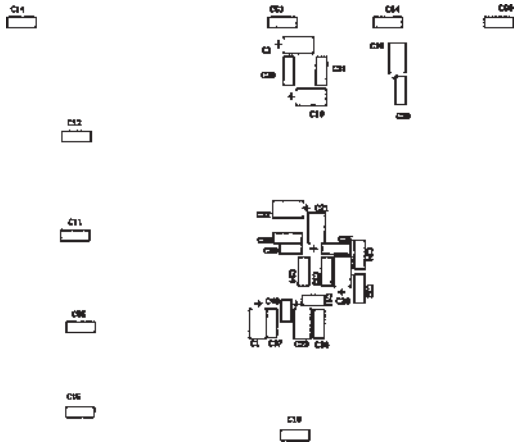


Figure 41. Evaluation Board Solder Side Silkscreen (Not to Scale)

OUTLINE DIMENSIONS

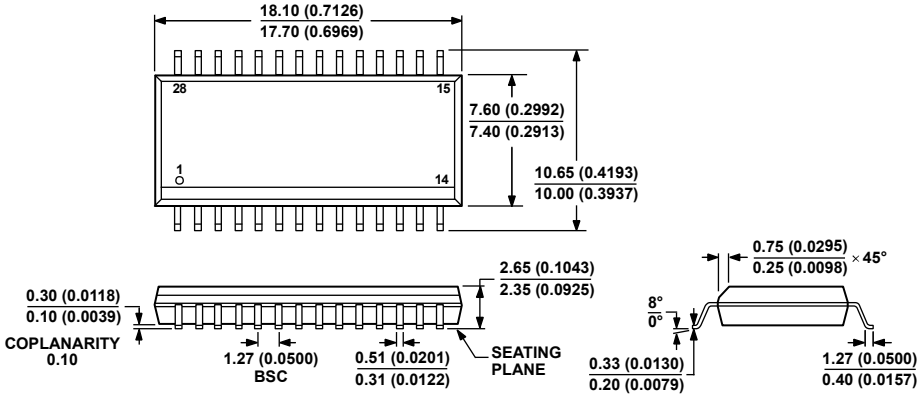


Figure 1. 28-Lead Standard Small Outline Package [SOIC_W]
Wide Body (RW-28)
Dimensions shown in millimeters and (inches)

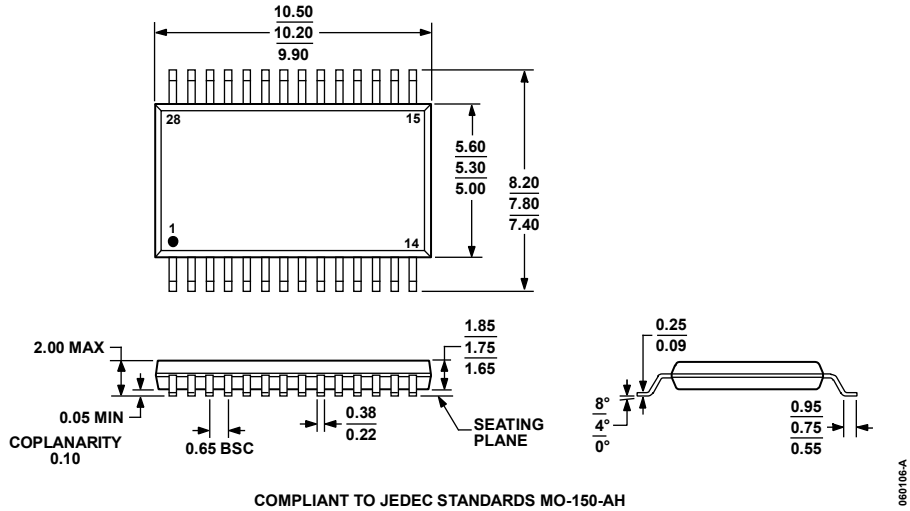


Figure 2. 28-Lead Shrink Small Outline Package [SSOP]
(RS-28)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9225AR	−40°C to +85°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
AD9225ARS	−40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD9225ARSRL	−40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD9225ARZ	−40°C to +85°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
AD9225ARZRL	−40°C to +85°C	28-Lead Standard Small Outline Package [SOIC_W]	RW-28
AD9225ARSZ	−40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28
AD9225ARSZRL	−40°C to +85°C	28-Lead Shrink Small Outline Package [SSOP]	RS-28

[1] Z = RoHS Compliant Part.

REVISION HISTORY

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8/03—REV. A to REV. B

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