THE DATASHEET OF

AD9235BCPZ-65

www.win-source.net 0086-755-83957316

12-Bit, 20/40/65 MSPS 3 V A/D Converter

Data Sheet

AD9235

FEATURES

Single 3 V supply operation (2.7 V to 3.6 V)
SNR = 70 dBc to Nyquist at 65 MSPS
SFDR = 85 dBc to Nyquist at 65 MSPS
Low power: 300 mW at 65 MSPS
Differential input with 500 MHz bandwidth
On-chip reference and SHA
DNL = ±0.4 LSB
Flexible analog input: 1 V p-p to 2 V p-p range
Offset binary or twos complement data format
Clock duty cycle stabilizer

APPLICATIONS

Ultrasound equipment
IF sampling in communications receivers
IS-95, CDMA-One, IMT-2000
Battery-powered instruments
Hand-held scopemeters
Low cost digital oscilloscopes

FUNCTIONAL BLOCK DIAGRAM

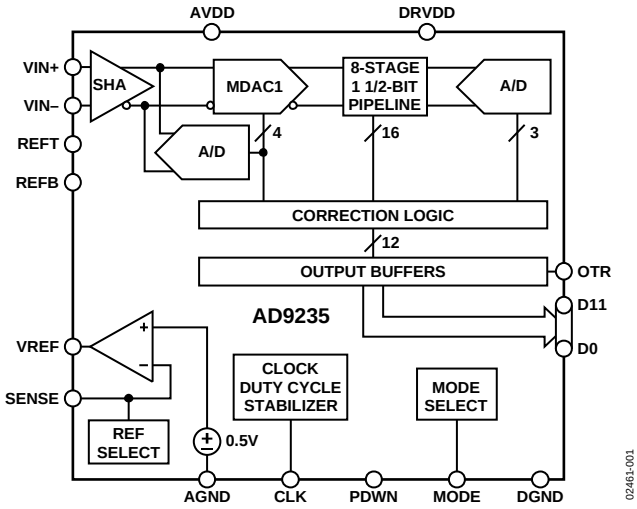

Figure 1.

GENERAL DESCRIPTION

The AD9235 is a family of monolithic, single 3 V supply, 12-bit, 20/40/65 MSPS analog-to-digital converters (ADCs). This family features a high performance sample-and-hold amplifier (SHA) and voltage reference. The AD9235 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy at 20/40/65 MSPS data rates and guarantee no missing codes over the full operating temperature range.

The wide bandwidth, truly differential SHA allows a variety of user-selectable input ranges and offsets including single-ended applications. It is suitable for multiplexed systems that switch full-scale voltage levels in successive channels and for sampling single-channel inputs at frequencies well beyond the Nyquist rate. Combined with power and cost savings over previously available ADCs, the AD9235 is suitable for applications in communications, imaging, and medical ultrasound.

A single-ended clock input is used to control all internal conversion cycles. A duty cycle stabilizer (DCS) compensates for wide variations in the clock duty cycle while maintaining excellent overall ADC performance. The digital output data is presented in straight binary or twos complement formats. An out-of-range (OTR) signal indicates an overflow condition that can be used with the most significant bit to determine low or high overflow.

Fabricated on an advanced CMOS process, the AD9235 is available in a 28-lead TSSOP and a 32-lead LFCSP and is specified over the industrial temperature range (–40°C to +85°C).

PRODUCT HIGHLIGHTS

1. The AD9235 operates from a single 3 V power supply and features a separate digital output driver supply to accommodate 2.5 V and 3.3 V logic families.
2. Operating at 65 MSPS, the AD9235 consumes a low 300 mW.
3. The patented SHA input maintains excellent performance for input frequencies up to 100 MHz and can be configured for single-ended or differential operation.
4. The AD9235 pinout is similar to the AD9214-65, a 10-bit, 65 MSPS ADC. This allows a simplified upgrade path from 10 bits to 12 bits for 65 MSPS systems.
5. The clock DCS maintains overall ADC performance over a wide range of clock pulse widths.
6. The OTR output bit indicates when the signal is beyond the selected input range.

Rev. D
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REVISION HISTORY

10/12—Rev. C to Rev. D

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Updated Outline Dimensions (Changed CP-32-2 to CP-32-7) ... 36
Changes to Ordering Guide ... 37

10/04—Data Sheet changed from Rev. B to Rev. C

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5/03—Data Sheet changed from Rev. A to Rev. B

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8/02—Data Sheet changed from Rev. 0 to Rev. A

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SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	Temp	Test Level	AD9235BRU/BCP-20			AD9235BRU/BCP-40			AD9235BRU/BCP-65			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
RESOLUTION	Full	VI	12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	VI		±0.30	±1.20		±0.50	±1.20		±0.50	±1.20	% FSR
Gain Error[1]	Full	VI		±0.30	±2.40		±0.50	±2.50		±0.50	±2.60	% FSR
Differential Nonlinearity (DNL)[2]	Full	IV		±0.35	±0.65		±0.35	±0.75		±0.40	±0.80	LSB
	25°C	I		±0.35			±0.35			±0.35		LSB
Integral Nonlinearity (INL)[2]	Full	IV		±0.45	±0.80		±0.50	±0.90		±0.70	±1.30	LSB
	25°C	I		±0.40			±0.40			±0.45		LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±2			±2			±3		ppm/°C
Gain Error	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5	±35		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
VREF = 0.5 V	25°C	V		0.54			0.54			0.54		LSB rms
VREF = 1.0 V	25°C	V		0.27			0.27			0.27		LSB rms
ANALOG INPUT												
Input Span, VREF = 0.5 V	Full	IV		1			1			1		V p-p
Input Span, VREF = 1.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	V		30			55			100		mA
IDRVDD[2]	Full	V		2			5			7		mA
PSRR	Full	V		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		90			165			300		mW
Sine Wave Input[2]	Full	VI		95	110		180	205		320	350	mW
Standby Power[5]	Full	V		1.0			1.0			1.0		mW

[1] Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2] Measured at maximum clock rate, f_{IN} = 2.4 MHz, full-scale sine wave, with approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AGND. Refer to Figure 5 for the equivalent analog input structure.
[4] Measured with dc input at maximum clock rate.
[5] Standby power is measured with a dc input, the CLK pin inactive (i.e., set to AVDD or AGND).

DIGITAL SPECIFICATIONS

Table 2.

Parameter	Temp	Test Level	AD9235BRU/BCP-20 Min	AD9235BRU/BCP-20 Typ	AD9235BRU/BCP-20 Max	AD9235BRU/BCP-40 Min	AD9235BRU/BCP-40 Typ	AD9235BRU/BCP-40 Max	AD9235BRU/BCP-65 Min	AD9235BRU/BCP-65 Typ	AD9235BRU/BCP-65 Max	Unit
LOGIC INPUTS												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Input Capacitance	Full	V		2			2			2		pF
LOGIC OUTPUTS[1]												
DRVDD = 3.3 V												
High-Level Output Voltage (IOH = 50 µA)	Full	IV	3.29			3.29			3.29			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	3.25			3.25			3.25			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)	Full	IV			0.05			0.05			0.05	V
DRVDD = 2.5 V												
High-Level Output Voltage (IOH = 50 µA)	Full	IV	2.49			2.49			2.49			V
High-Level Output Voltage (IOH = 0.5 mA)	Full	IV	2.45			2.45			2.45			V
Low-Level Output Voltage (IOL = 1.6 mA)	Full	IV			0.2			0.2			0.2	V
Low-Level Output Voltage (IOL = 50 µA)	Full	IV			0.05			0.05			0.05	V

[1] Output voltage levels measured with 5 pF load on each output.

SWITCHING SPECIFICATIONS

Table 3.

Parameter	Temp	Test Level	AD9235BRU/BCP-20 Min	AD9235BRU/BCP-20 Typ	AD9235BRU/BCP-20 Max	AD9235BRU/BCP-40 Min	AD9235BRU/BCP-40 Typ	AD9235BRU/BCP-40 Max	AD9235BRU/BCP-65 Min	AD9235BRU/BCP-65 Typ	AD9235BRU/BCP-65 Max	Unit
CLOCK INPUT PARAMETERS												
Maximum Conversion Rate	Full	VI	20			40			65			MSPS
Minimum Conversion Rate	Full	V			1			1			1	MSPS
CLK Period	Full	V	50.0			25.0			15.4			ns
CLK Pulse-Width High[1]	Full	V	15.0			8.8			6.2			ns
CLK Pulse-Width Low[1]	Full	V	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETERS												
Output Delay[2] (t_{PD})	Full	V		3.5			3.5			3.5		ns
Pipeline Delay (Latency)	Full	V		7			7			7		Cycles
Aperture Delay (t_A)	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty Jitter (t_J)	Full	V		0.5			0.5			0.5		ps rms
Wake-Up Time[3]	Full	V		3.0			3.0			3.0		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		1			1			2		Cycles

[1] For the AD9235-65 model only, with duty cycle stabilizer enabled. DCS function not applicable for -20 and -40 models.
[2] Output delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load on each output.
[3] Wake-up time is dependent on value of decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

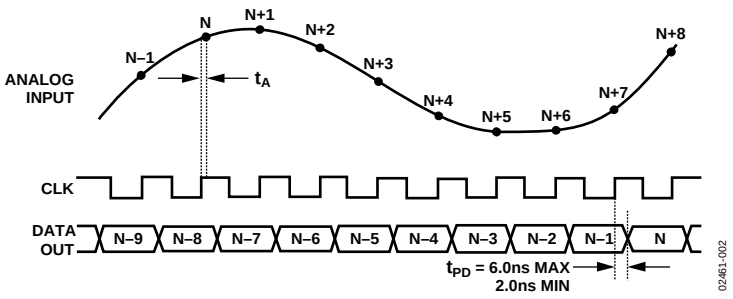


Figure 2. Timing Diagram

AC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, 2 V p-p differential input, A_{IN} = –0.5 dBFS, 1.0 V internal reference, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

			AD9235BRU/BCP-20			AD9235BRU/BCP-40			AD9235BRU/BCP-65			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO												
f_{INPUT} = 2.4 MHz	25°C	V		70.8			70.6			70.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV	70.0	70.4								dBc
	25°C	I		70.6								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.9	70.3					dBc
	25°C	I					70.4					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.7	69.7		dBc
	25°C	I								70.1		dBc
f_{INPUT} = 100 MHz	25°C	V		68.7			68.5			68.3		dBc
SIGNAL-TO-NOISE RATIO AND DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		70.6			70.5			70.4		dBc
f_{INPUT} = 9.7 MHz	Full	IV	69.9	70.3								dBc
	25°C	I		70.5								dBc
f_{INPUT} = 19.6 MHz	Full	IV				69.7	70.2					dBc
	25°C	I					70.3					dBc
f_{INPUT} = 32.5 MHz	Full	IV							68.3	69.5		dBc
	25°C	I								69.9		dBc
f_{INPUT} = 100 MHz	25°C	V		68.6			68.3			67.8		dBc
TOTAL HARMONIC DISTORTION												
f_{INPUT} = 2.4 MHz	25°C	V		–88.0			–89.0			–87.5		dBc
f_{INPUT} = 9.7 MHz	Full	IV		–86.0	–79.0							dBc
	25°C	I		–87.4								dBc
f_{INPUT} = 19.6 MHz	Full	IV					–85.5	–79.0				dBc
	25°C	I					–86.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV								–81.8	–74.0	dBc
	25°C	I								–82.0		dBc
f_{INPUT} = 100 MHz	25°C	V		–84.0			–82.5			–78.0		dBc
WORST HARMONIC (SECOND OR THIRD)												
f_{INPUT} = 9.7 MHz	Full	IV		–90.0	–80.0							dBc
f_{INPUT} = 19.6 MHz	Full	IV					–90.0	–80.0				dBc
f_{INPUT} = 32.5 MHz	Full	IV								–83.5	–74.0	dBc

Parameter	Temp	Test Level	AD9235BRU/BCP-20 Min	AD9235BRU/BCP-20 Typ	AD9235BRU/BCP-20 Max	AD9235BRU/BCP-40 Min	AD9235BRU/BCP-40 Typ	AD9235BRU/BCP-40 Max	AD9235BRU/BCP-65 Min	AD9235BRU/BCP-65 Typ	AD9235BRU/BCP-65 Max	Unit
SPURIOUS-FREE DYNAMIC RANGE												
f_{INPUT} = 2.4 MHz	25°C	V		92.0			92.0			92.0		dBc
f_{INPUT} = 9.7 MHz	Full	IV	80.0	88.5								dBc
	25°C	I		91.0								dBc
f_{INPUT} = 19.6 MHz	Full	IV				80.0	89.0					dBc
	25°C	I					90.0					dBc
f_{INPUT} = 32.5 MHz	Full	IV							74.0	83.0		dBc
	25°C	I								85.0		dBc
f_{INPUT} = 100 MHz	25°C	V		84.0			85.0			80.5		dBc

ABSOLUTE MAXIMUM RATINGS

Table 5.

Pin Name	With Respect to	Min	Max	Unit
ELECTRICAL				
AVDD	AGND	–0.3	+3.9	V
DRVDD	DGND	–0.3	+3.9	V
AGND	DGND	–0.3	+0.3	V
AVDD	DRVDD	–3.9	+3.9	V
Digital Outputs	DGND	–0.3	DRVDD + 0.3	V
CLK, MODE	AGND	–0.3	AVDD + 0.3	V
VIN+, VIN–	AGND	–0.3	AVDD + 0.3	V
VREF	AGND	–0.3	AVDD + 0.3	V
SENSE	AGND	–0.3	AVDD + 0.3	V
REFB, REFT	AGND	–0.3	AVDD + 0.3	V
PDWN	AGND	–0.3	AVDD + 0.3	V
ENVIRONMENTAL[1]				
Operating Temperature		–40	+85	°C
Junction Temperature			150	°C
Lead Temperature (10 sec)			300	°C
Storage Temperature		–65	+150	°C

[1] Typical thermal impedances (28-lead TSSOP), θ_{JA} = 67.7°C/W; (32-lead LFCSP), θ_{JA} = 32.5°C/W, θ_{JC} = 32.71°C/W. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-1.

Absolute maximum ratings are limiting values to be applied individually and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Levels	Description
I	100% production tested.
II	100% production tested at 25°C and sample tested at specified temperatures.
III	Sample tested only.
IV	Parameter is guaranteed by design and characterization testing.
V	Parameter is a typical value only.
VI	100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

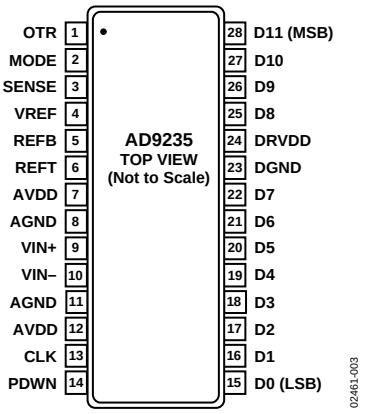


Figure 3. 28-Lead TSSOP Pin Configuration

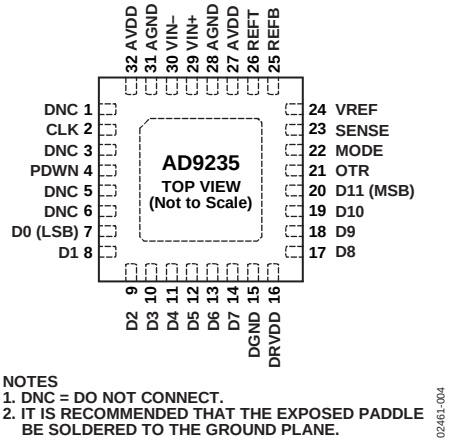


Figure 4. 32-Lead LFCSP Pin Configuration

Table 6. Pin Function Descriptions

Pin No. 28-Lead TSSOP	Pin No. 32-Lead LFCSP	Mnemonic	Description
1	21	OTR	Out-of-Range Indicator.
2	22	MODE	Data Format and Clock Duty Cycle Stabilizer (DCS) Mode Selection.
3	23	SENSE	Reference Mode Selection.
4	24	VREF	Voltage Reference Input/Output.
5	25	REFB	Differential Reference (–).
6	26	REFT	Differential Reference (+).
7, 12	27, 32	AVDD	Analog Power Supply.
8, 11	28, 31	AGND	Analog Ground.
9	29	VIN+	Analog Input Pin (+).
10	30	VIN–	Analog Input Pin (–).
13	2	CLK	Clock Input Pin.
14	4	PDWN	Power-Down Function Selection (Active High).
15 to 22, 25 to 28	7 to 14, 17 to 20	D0 (LSB) to D11 (MSB)	Data Output Bits.
23	15	DGND	Digital Output Ground.
24	16	DRVDD	Digital Output Driver Supply. Must be decoupled to DGND with a minimum. 0.1 µF capacitor. Recommended decoupling is 0.1 µF in parallel with 10 µF.
	1, 3, 5, 6	DNC	Do Not Connect.
	EP	EPAD	Exposed Pad. It is recommended that the exposed paddle be soldered to the ground plane. There is an increased reliability of the solder joints and maximum thermal capability of the package is achieved with exposed paddle soldered to the customer board.

DEFINITIONS OF SPECIFICATIONS

Analog Bandwidth (Full Power Bandwidth)
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay (t_A)
The delay between the 50% point of the rising edge of the clock and the instant at which the analog input is sampled.

Aperture Jitter (t_J)
The sample-to-sample variation in aperture delay.

Integral Nonlinearity (INL)
The deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1 ½ LSBs beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4096 codes must be present over all operating ranges.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1 ½ LSB below the positive full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for offset error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection Ratio
The change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)[1]
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal.

Signal-to-Noise and Distortion (SINAD)[1]
The ratio of the rms signal amplitude (set 0.5 dB below full scale) to the rms value of the sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc.

Effective Number of Bits (ENOB)
The ENOB for a device for sine wave inputs at a given input frequency can be calculated directly from its measured *SINAD* using the following formula

$$N = (SINAD - 1.76)/6.02$$

Signal-to-Noise Ratio (SNR)[1]
The ratio of the rms signal amplitude (set at 0.5 dB below full scale) to the rms value of the sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc.

Spurious-Free Dynamic Range (SFDR)[1]
The difference in dB between the rms amplitude of the input signal and the peak spurious signal.

Two-Tone SFDR[1]
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Clock Pulse Width and Duty Cycle
Pulse-width high is the minimum amount of time that the clock pulse should be left in the Logic 1 state to achieve rated performance. Pulse-width low is the minimum time the clock pulse should be left in the low state. At a given clock rate, these specifications define an acceptable clock duty cycle.

Minimum Conversion Rate
The clock rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The clock rate at which parametric testing is performed.

Output Propagation Delay (t_{PD})
The delay between the clock logic threshold and the time when all bits are within valid logic levels.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transition from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

[1] AC specifications may be reported in dBc (degrades as signal levels are lowered) or in dBFS (always related back to converter full scale).

EQUIVALENT CIRCUITS

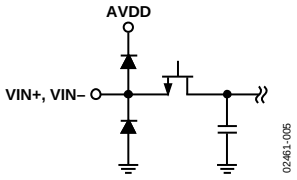


Figure 5. Equivalent Analog Input Circuit

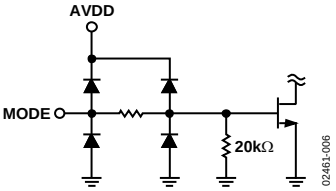


Figure 6. Equivalent MODE Input Circuit

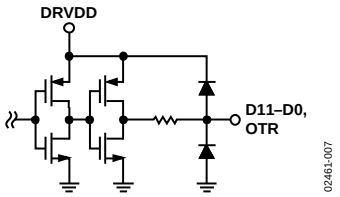


Figure 7. Equivalent Digital Output Circuit

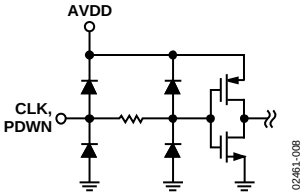


Figure 8. Equivalent Digital Input Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 3.0 V, DRVDD = 2.5 V, f_{SAMPLE} = 65 MSPS with DCS disabled, T_A = 25°C, 2 V differential input, A_{IN} = −0.5 dBFS, VREF = 1.0 V, unless otherwise noted.

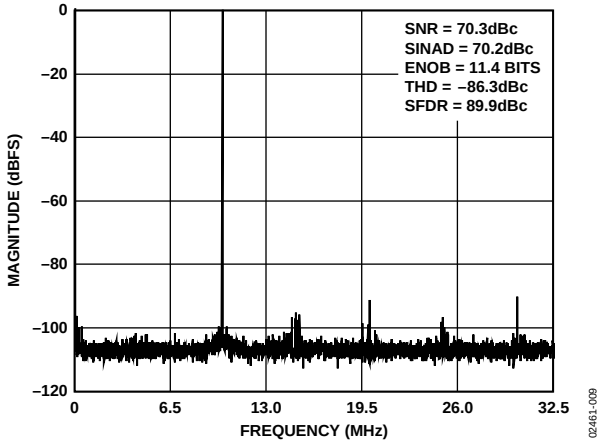


Figure 9. Single Tone 8K FFT with f_{IN} = 10 MHz

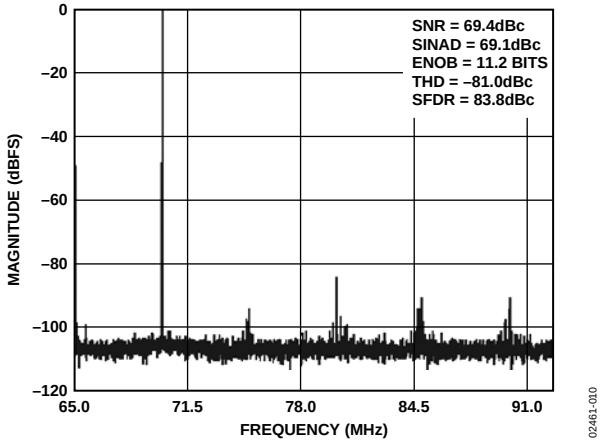


Figure 10. Single Tone 8K FFT with f_{IN} = 70 MHz

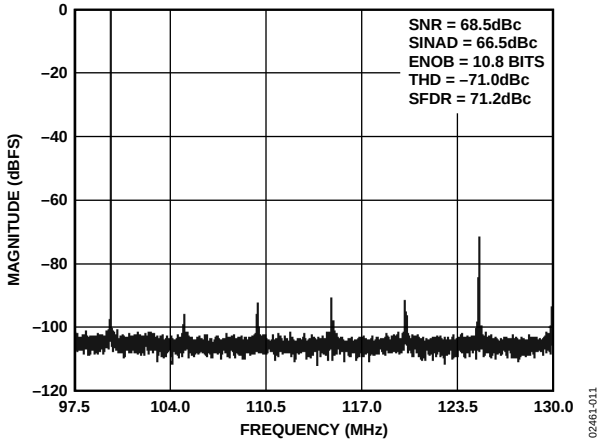


Figure 11. Single Tone 8K FFT with f_{IN} = 100 MHz

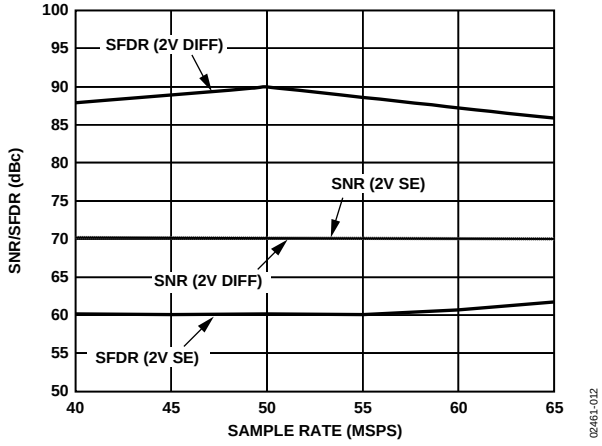


Figure 12. AD9235-65: Single Tone SNR/SFDR vs. f_{CLK} with f_{IN} = Nyquist (32.5 MHz)

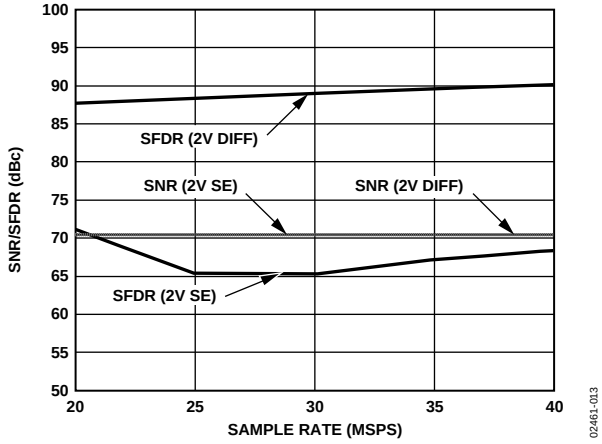


Figure 13. AD9235-40: Single Tone SNR/SFDR vs. f_{CLK} with f_{IN} = Nyquist (20 MHz)

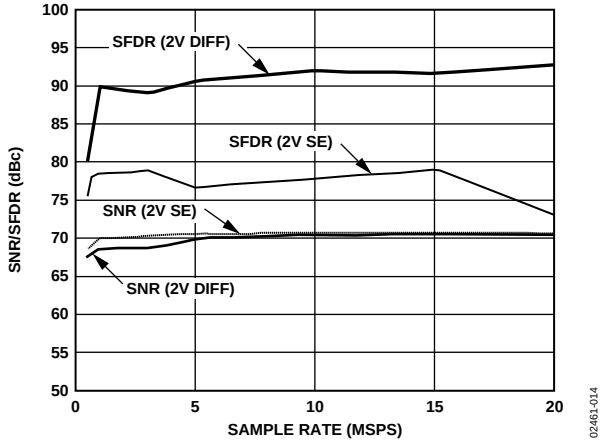


Figure 14. AD9235-20: Single Tone SNR/SFDR vs. f_{CLK} with f_{IN} = Nyquist (10 MHz)

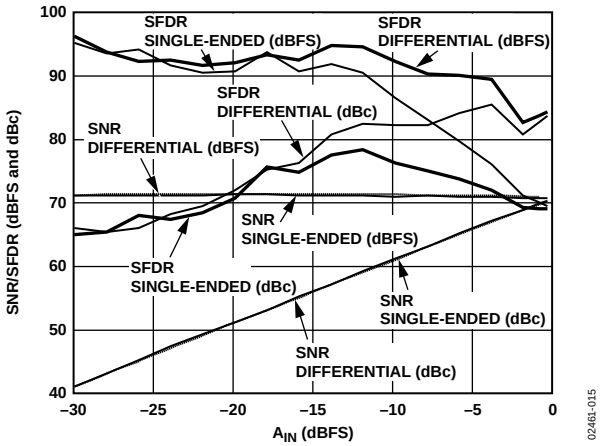


Figure 15. AD9235-65: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (32.5 MHz)

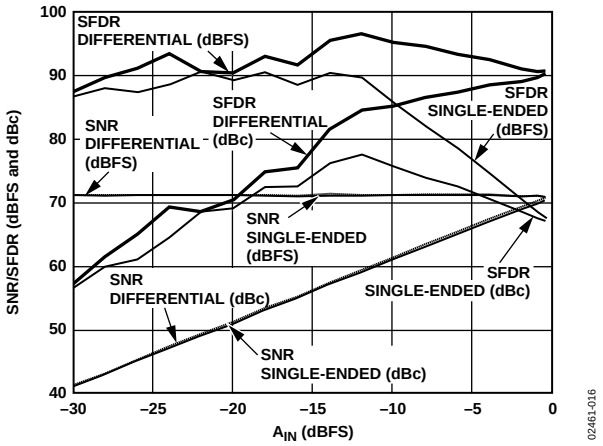


Figure 16. AD9235-40: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (20 MHz)

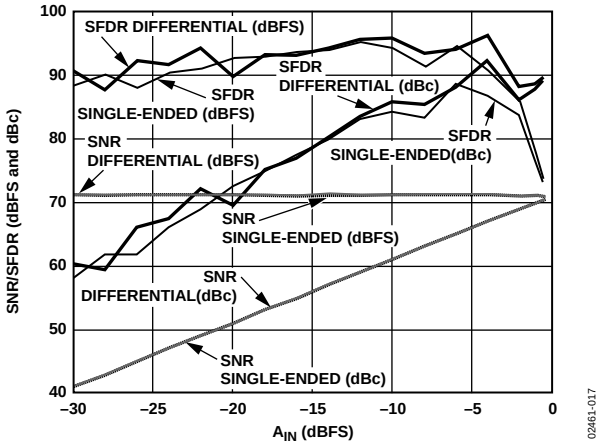


Figure 17. AD9235-20: Single Tone SNR/SFDR vs. A_{IN} with f_{IN} = Nyquist (10 MHz)

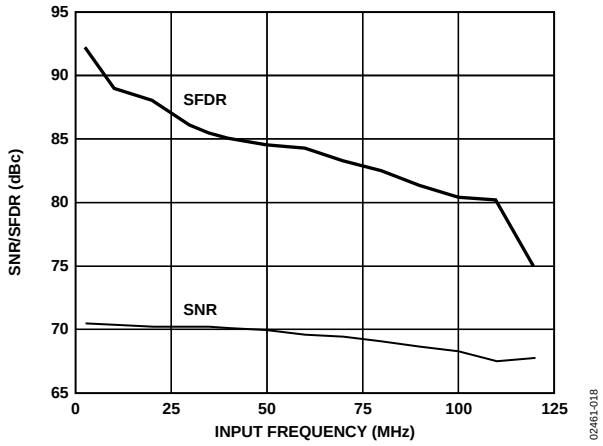


Figure 18. AD9235-65: SNR/SFDR vs. f_{IN}

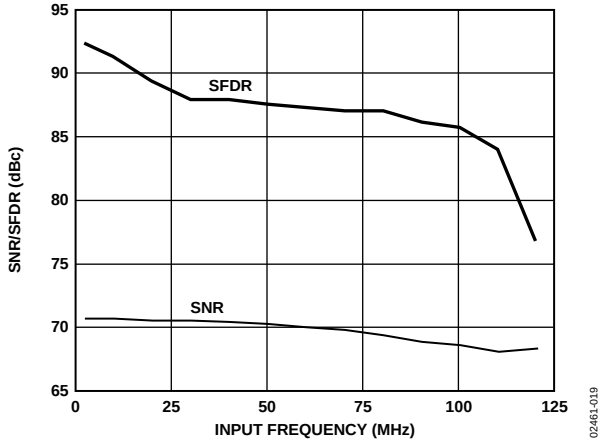


Figure 19. AD9235-40: SNR/SFDR vs. f_{IN}

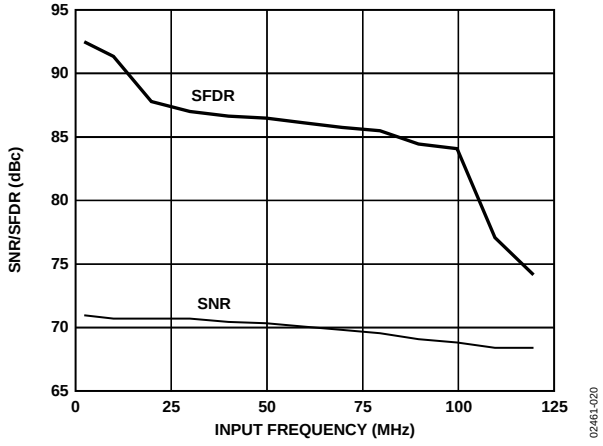


Figure 20. AD9235-20: SNR/SFDR vs. f_{IN}

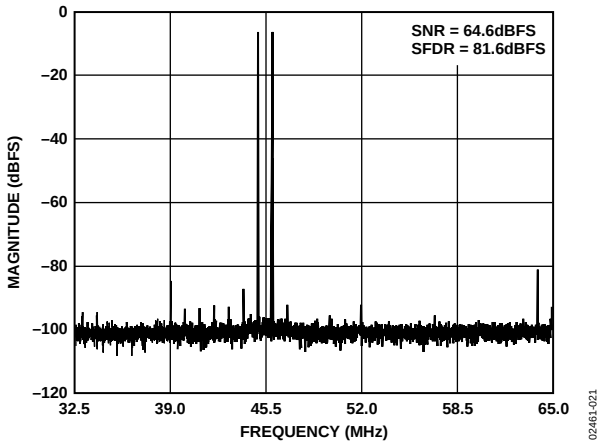


Figure 21. Dual Tone 8K FFT with f_{IN1} = 45 MHz and f_{IN2} = 46 MHz

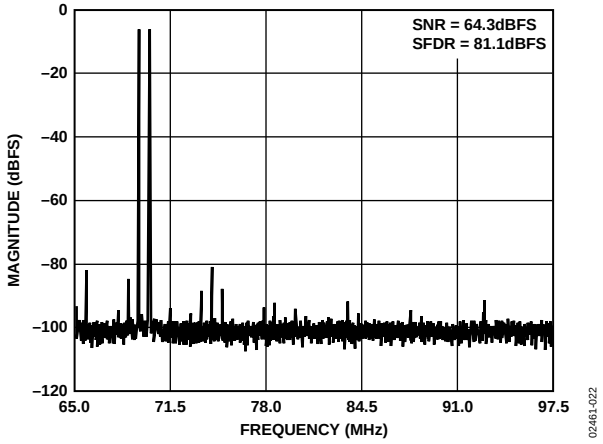


Figure 22. Dual Tone 8K FFT with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz

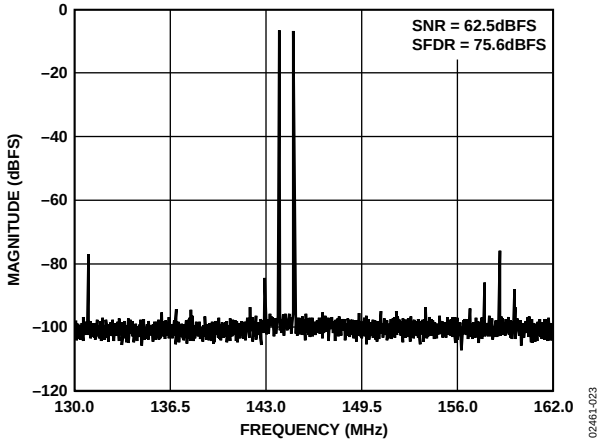


Figure 23. Dual Tone 8K FFT with f_{IN1} = 144 MHz and f_{IN2} = 145 MHz

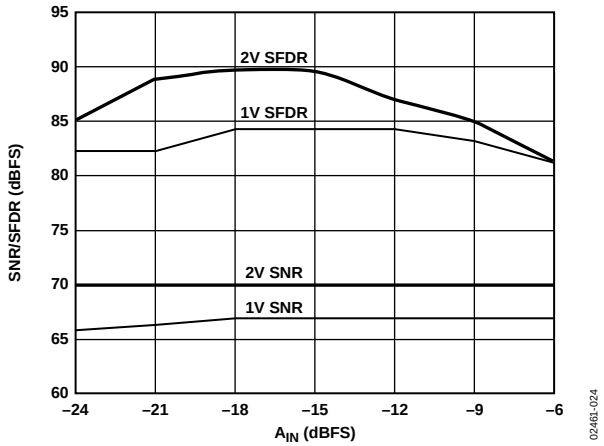


Figure 24. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 45 MHz and f_{IN2} = 46 MHz

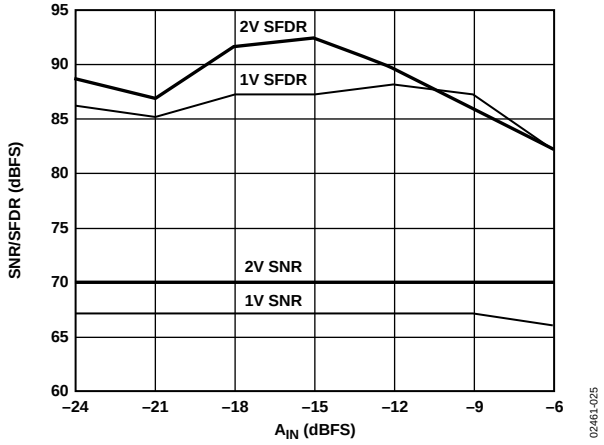


Figure 25. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 69 MHz and f_{IN2} = 70 MHz

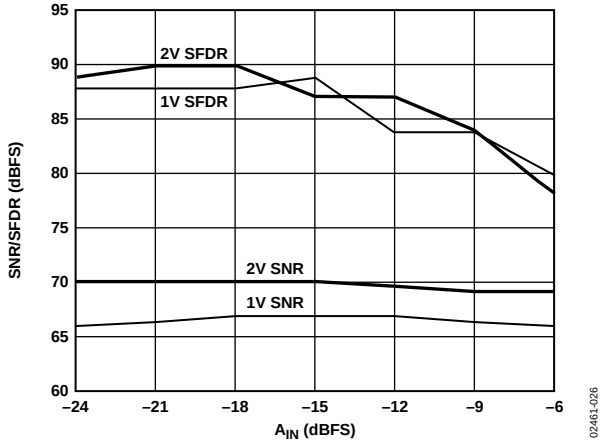


Figure 26. Dual Tone SNR/SFDR vs. A_{IN} with f_{IN1} = 144 MHz and f_{IN2} = 145 MHz

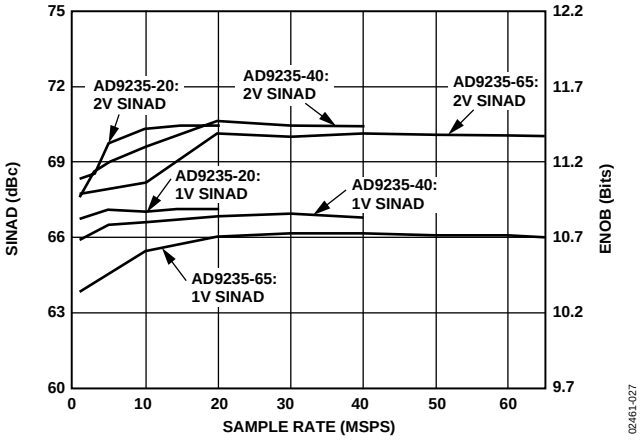


Figure 27. SINAD vs. f_{CLK} with f_{IN} = Nyquist

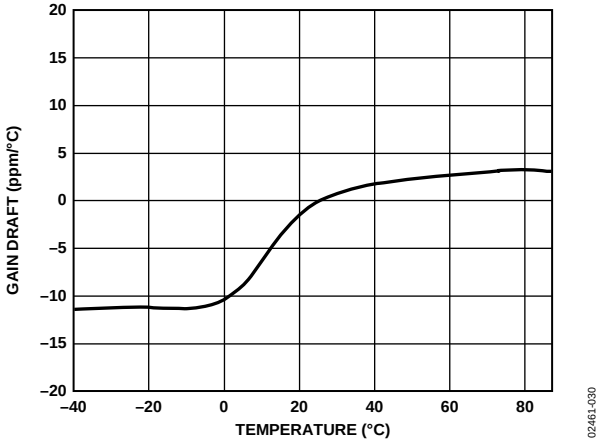


Figure 30. A/D Gain vs. Temperature Using an External Reference

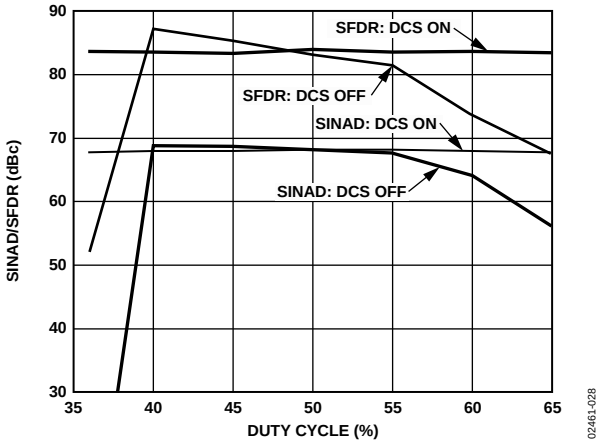


Figure 28. SINAD/SFDR vs. Clock Duty Cycle

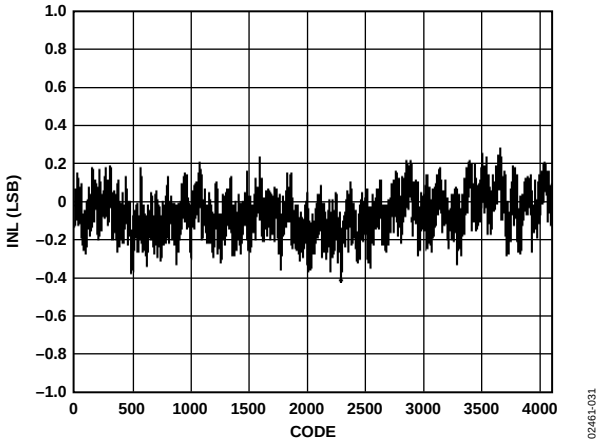


Figure 31. Typical INL

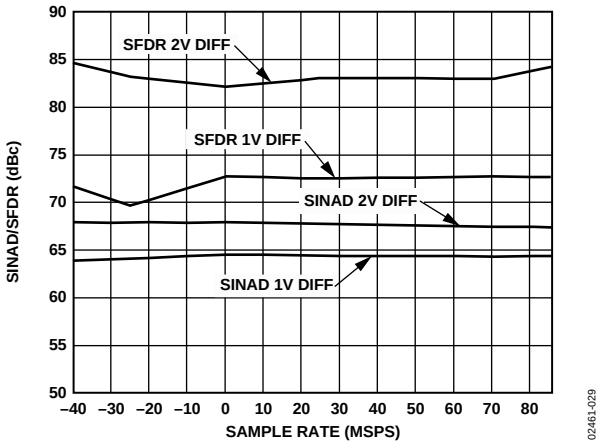


Figure 29. SINAD/SFDR vs. Temperature with f_{IN} = 32.5 MHz

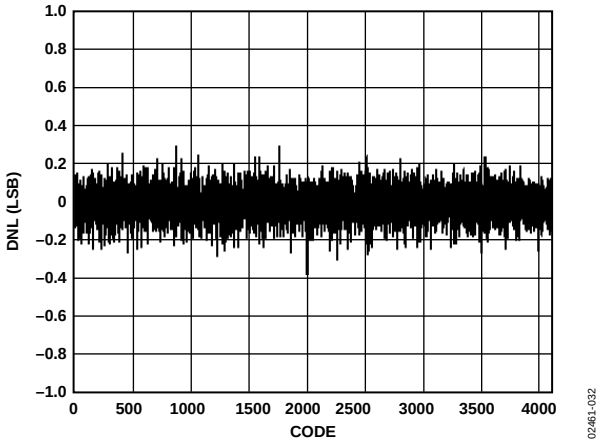


Figure 32. Typical DNL

APPLYING THE AD9235

THEORY OF OPERATION

The AD9235 architecture consists of a front end SHA followed by a pipelined switched capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage followed by eight 1.5-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined into a final 12-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor DAC and interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT

The analog input to the AD9235 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal. The SHA input can support a wide common-mode range and maintain excellent performance, as shown in Figure 34. An input common-mode voltage of midsupply minimizes signal-dependent errors and provides optimum performance.

Referring to Figure 33, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC's input; therefore, the precise values are dependent upon the application. In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they would limit the input bandwidth.

For best dynamic performance, the source impedances driving VIN+ and VIN– should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

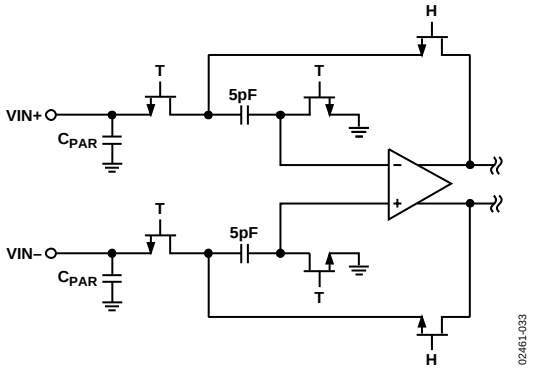


Figure 33. Switched-Capacitor SHA Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as:

$$REFT = ½(AVDD + VREF)$$

$$REFB = ½(AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

It can be seen from the equations above that the REFT and REFB voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

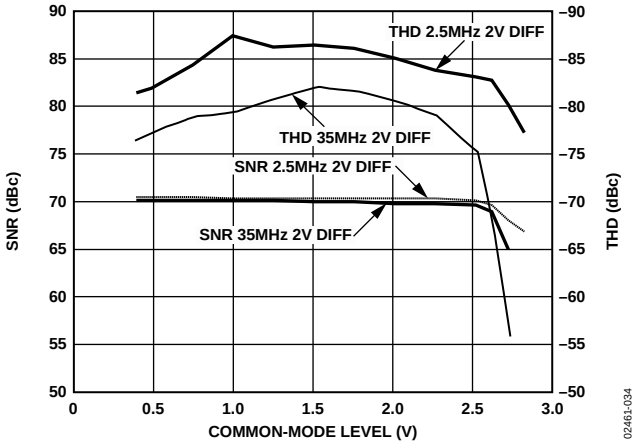


Figure 34. AD9235-65: SNR, THD vs. Common-Mode Level

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V, or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the AD9235 set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as:

$$VCM_{MIN} = VREF/2$$

$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD9235 to accommodate ground-referenced inputs.

Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN–. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VIN+ while a 1 V reference is applied to VIN–. The AD9235 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies and in the lower speed grade models (AD9235-40 and AD9235-20).

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9235 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

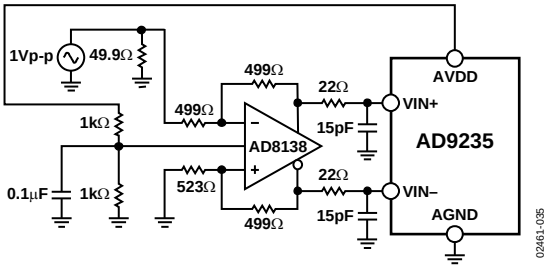


Figure 35. Differential Input Configuration Using the AD8138

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9235. This is especially true in IF undersampling applications where frequencies in the 70 MHz to 100 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 36.

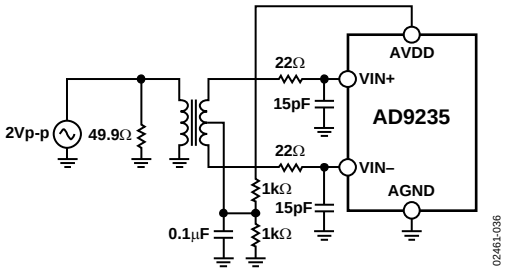


Figure 36. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is degradation in SFDR and in distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance. Figure 37 details a typical single-ended input configuration.

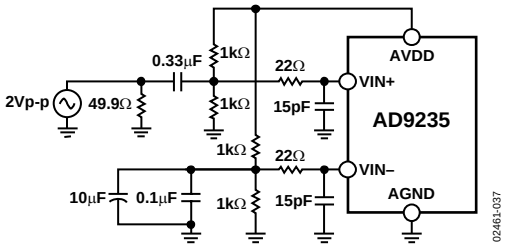


Figure 37. Single-Ended Input Configuration

CLOCK INPUT CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals, and as a result, may be sensitive to clock duty cycle. Commonly a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics. The AD9235 contains a clock duty cycle stabilizer (DCS) that retimes the nonsampling edge, providing an internal clock signal with a nominal 50% duty cycle. This allows a wide range of clock input duty cycles without affecting the performance of the AD9235. As shown in Figure 30, noise and distortion performance are nearly flat over a 30% range of duty cycle.

The duty cycle stabilizer uses a delay-locked loop (DLL) to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 100 clock cycles to allow the DLL to acquire and lock to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated by

$$SNR\ Degradation = -20 \times \log_{10}[2\pi \times f_{INPUT} \times t_J]$$

In the equation, the rms aperture jitter, t_J, represents the root-sum square of all jitter sources, which include the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9235. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 38, the power dissipated by the AD9235 is proportional to its sample rate. The digital power dissipation does not vary substantially between the three speed grades because it is determined primarily by the strength of the digital drivers and the load on each output bit. The maximum DRVDD current can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits, 12 in the case of the AD9235. This maximum current occurs when every output bit switches on every clock cycle, i.e., a full-scale square wave at the Nyquist frequency, $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the encode rate and the characteristics of the analog input signal.

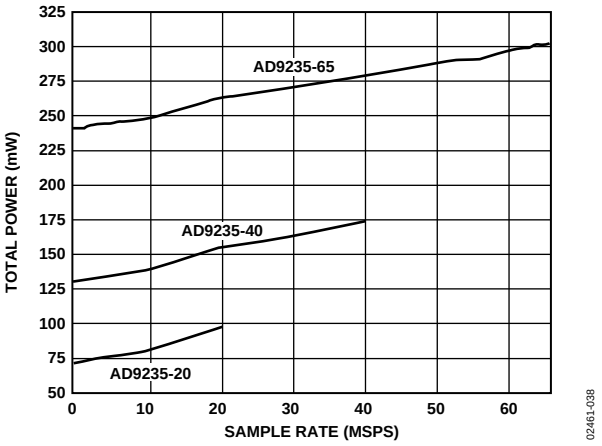


Figure 38. Total Power vs. Sample Rate with f_{IN} = 10 MHz

For the AD9235-20 speed grade, the digital power consumption can represent as much as 10% of the total dissipation. Digital power consumption can be minimized by reducing the capacitive load presented to the output drivers. The data in Figure 38 was taken with a 5 pF load on each output driver.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases linearly with the clock frequency.

By asserting the PDWN pin high, the AD9235 is placed in standby mode. In this state, the ADC typically dissipates 1 mW if the CLK and analog inputs are static. During standby, the output drivers are placed in a high impedance state. Reasserting the PDWN pin low returns the AD9235 into its normal operational mode.

Low power dissipation in standby mode is achieved by shutting down the reference, reference buffer, and biasing networks. The decoupling capacitors on REFT and REFB are discharged when entering standby mode and then must be recharged when returning to normal operation. As a result, the wake-up time is related to the time spent in standby mode, and shorter standby cycles result in proportionally shorter wake-up times. With the recommended 0.1 µF and 10 µF decoupling capacitors on REFT and REFB, it takes approximately 1 sec to fully discharge the reference buffer decoupling capacitors and 3 ms to restore full operation.

Table 7. Reference Configuration Summary

Selected Mode	SENSE Voltage	Internal Switch Position	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	N/A	2 × External Reference
Internal Fixed Reference	VREF	SENSE	0.5	1.0
Programmable Reference	0.2 V to VREF	SENSE	0.5 × (1 + R2/R1)	2 × VREF (See Figure 40)
Internal Fixed Reference	AGND to 0.2 V	Internal Divider	1.0	2.0

DIGITAL OUTPUTS

The AD9235 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

As detailed in Table 8, the data format can be selected for either offset binary or twos complement.

Timing

The AD9235 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9235; these transients can detract from the converter's dynamic performance.

The lowest typical conversion rate of the AD9235 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9235. The input range can be adjusted by varying the reference voltage applied to the AD9235, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly.

If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

Internal Reference Connection

A comparator within the AD9235 detects the potential at the SENSE pin and configures the reference into one of four possible states, which are summarized in Table 7. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 39), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected as shown in Figure 40, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times (1 + R2/R1)$$

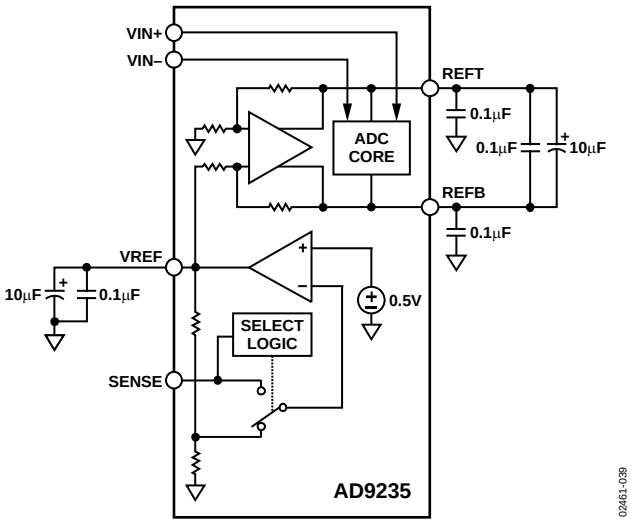


Figure 39. Internal Reference Configuration

In all reference configurations, REFT and REFB drive the A/D conversion core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

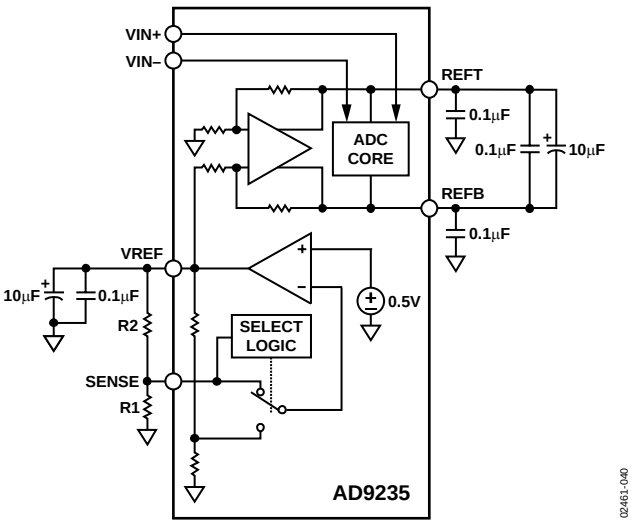


Figure 40. Programmable Reference Configuration

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 41 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes.

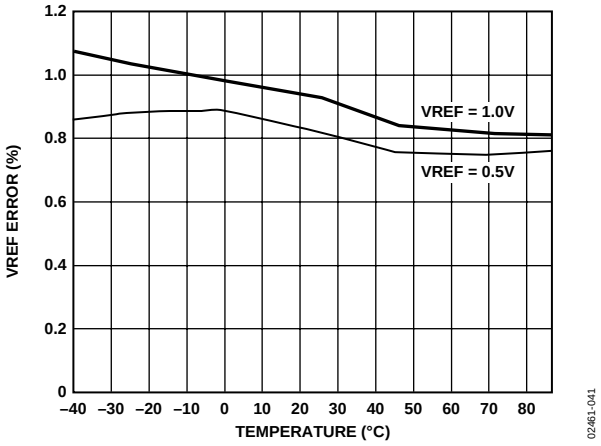


Figure 41. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V.

If the internal reference of the AD9235 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 42 depicts how the internal reference voltage is affected by loading.

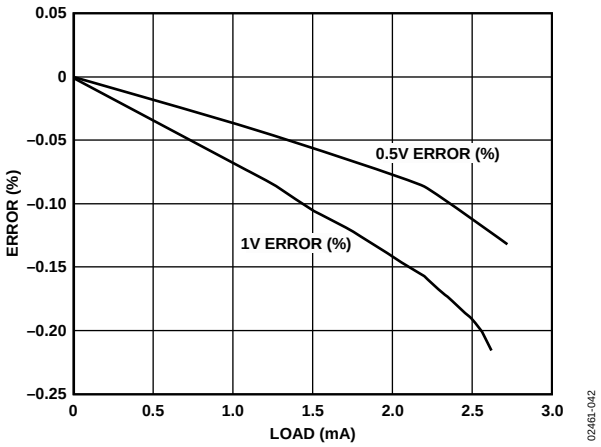


Figure 42. VREF Accuracy vs. Load

OPERATIONAL MODE SELECTION

As discussed earlier, the AD9235 can output data in either offset binary or twos complement format. There is also a provision for enabling or disabling the clock DCS. The MODE pin is a multilevel input that controls the data format and DCS state. The input threshold values and corresponding mode selections are outlined in Table 8.

Table 8. Mode Selection

MODE Voltage	Data Format	Duty Cycle Stabilizer
AVDD	Twos Complement	Disabled
2/3 AVDD	Twos Complement	Enabled
1/3 AVDD	Offset Binary	Enabled
AGND (Default)	Offset Binary	Disabled

The MODE pin is internally pulled down to AGND by a 20 kΩ resistor.

TSSOP EVALUATION BOARD

The AD9235 evaluation board provides the support circuitry required to operate the ADC in its various modes and configurations. The converter can be driven differentially, through an AD8138 driver or a transformer, or single-ended. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics). Figure 43 shows the typical bench characterization setup used to evaluate the ac performance of the AD9235. It is critical that signal sources with very low phase noise (<1 ps rms jitter) be used to realize the ultimate performance of the converter. Proper filtering of the input signal, to remove harmonics and lower the integrated noise at the input, is also necessary to achieve the specified noise performance.

The AUXCLK input should be selected in applications requiring the lowest jitter and SNR performance, i.e., IF undersampling characterization. It allows the user to apply a clock input signal that is 4× the target sample rate of the AD9235. A low-jitter, differential divide-by-4 counter, the MC100LVEL33D, provides a 1× clock output that is subsequently returned back to the CLK input via JP9. For example, a 260 MHz signal (sinusoid) is divided down to a 65 MHz signal for clocking the ADC. Note that R1 must be removed with the AUXCLK interface. Lower jitter is often achieved with this interface since many RF signal generators display improved phase noise at higher output frequencies and the slew rate of the sinusoidal output signal is 4× that of a 1× signal of equal amplitude.

Complete schematics and layout plots follow and demonstrate the proper routing and grounding techniques that should be applied at the system level.

LFCSP EVALUATION BOARD

The typical bench setup used to evaluate the ac performance of the AD9235 is similar to the TSSOP Evaluation Board connections (refer to the schematics for connection details). The AD9235 can be driven single-ended or differentially through a transformer. Separate power pins are provided to isolate the DUT from the support circuitry. Each input configuration can be selected by proper connection of various jumpers (refer to the schematics).

An alternative differential analog input path using an AD8351 op amp is included in the layout but is not populated in production. Designers interested in evaluating the op amp with the ADC should remove C15, R12, and R3 and populate the op amp circuit. The passive network between the AD8351 outputs and the AD9235 allows the user to optimize the frequency response of the op amp for the application.

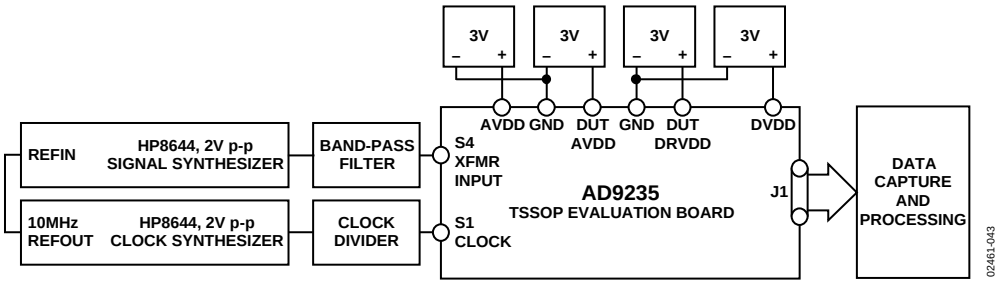


Figure 43. TSSOP Evaluation Board Connections

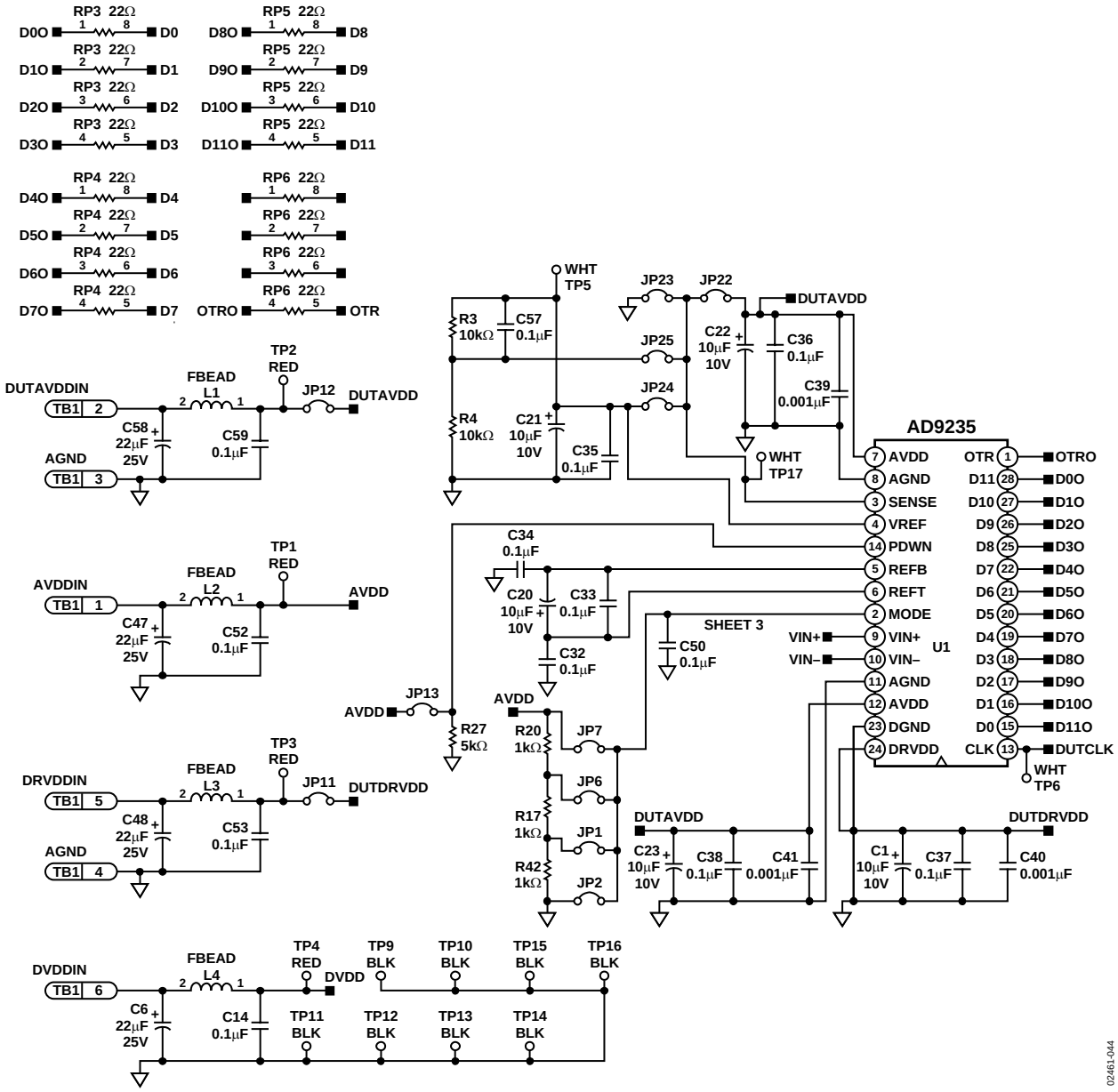


Figure 44. TSSOP Evaluation Board Schematic, DUT

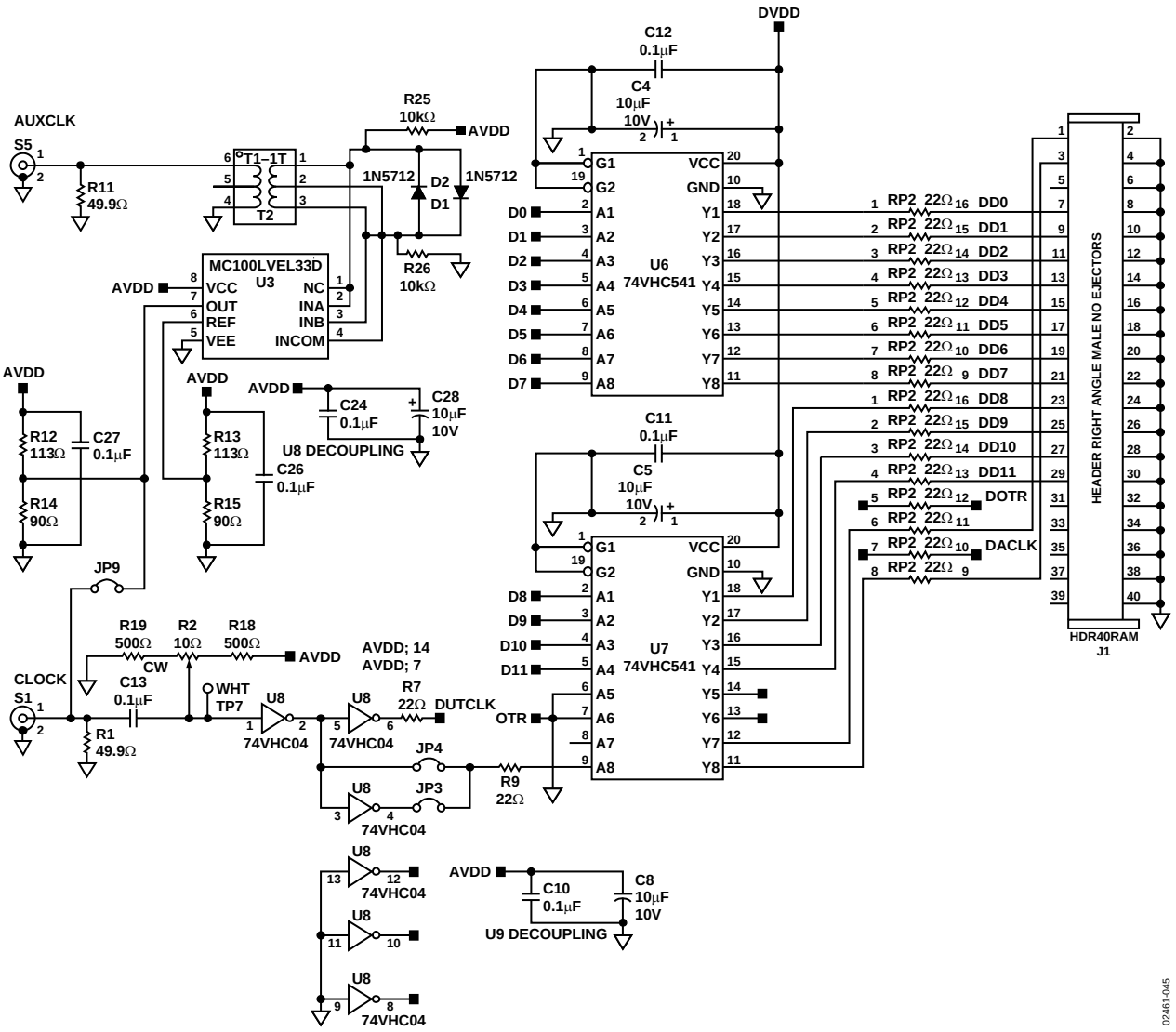


Figure 45. TSSOP Evaluation Board Schematic, Clock Inputs and Output Buffering

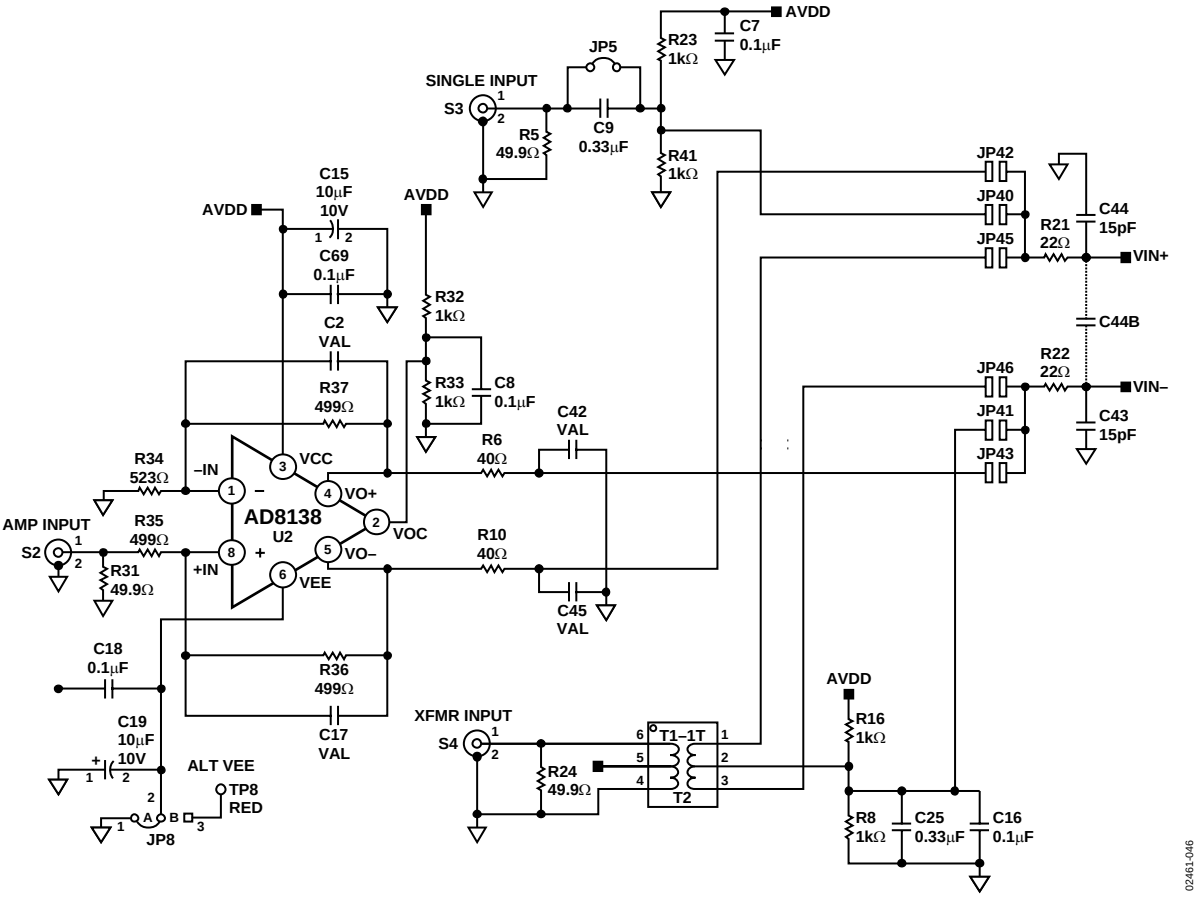


Figure 46. TSSOP Evaluation Board Schematic, Analog Inputs

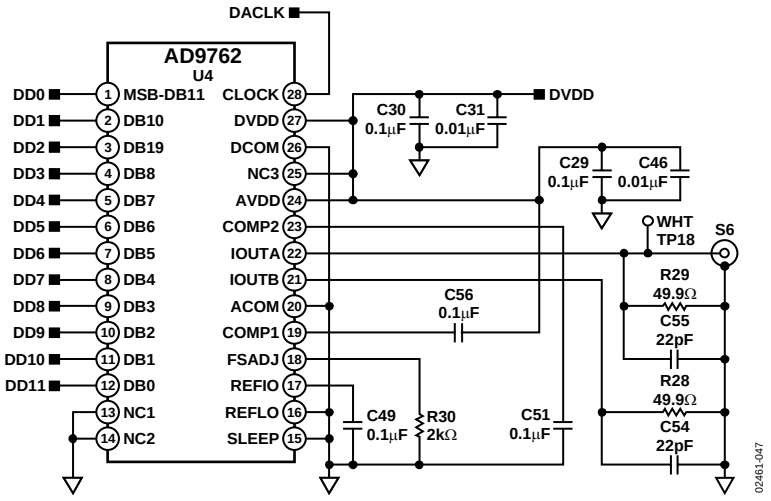


Figure 47. TSSOP Evaluation Board Schematic, Optional DAC

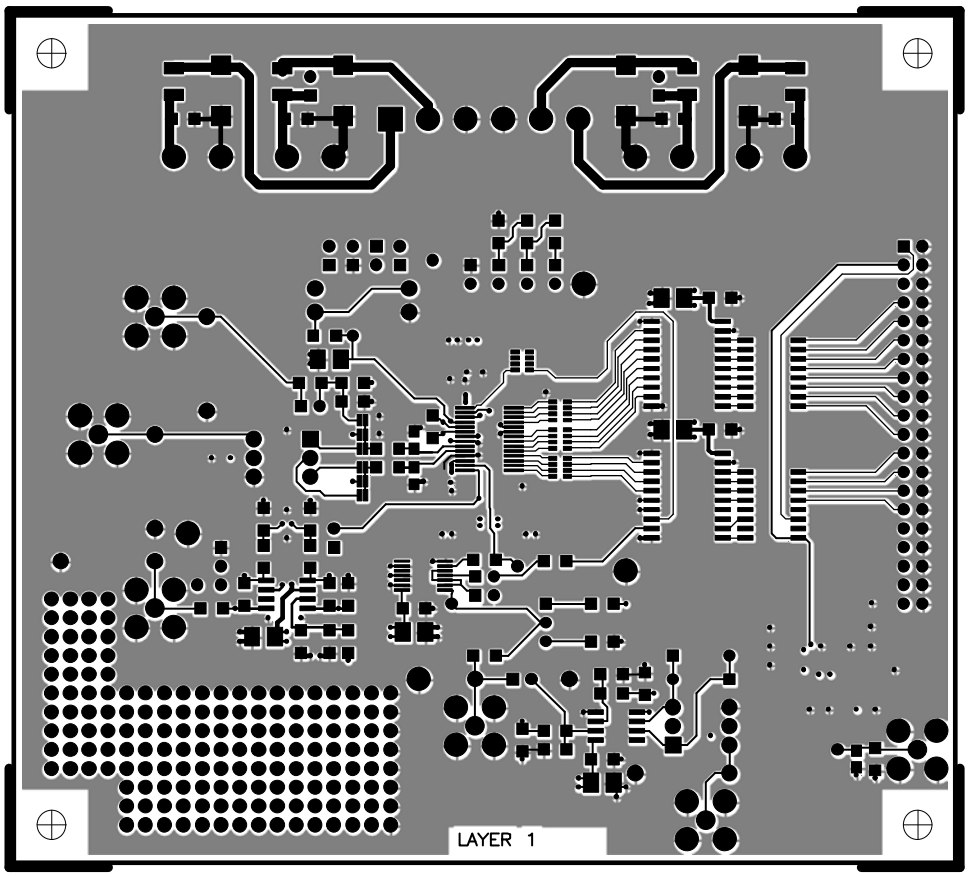


Figure 48. TSSOP Evaluation Board Layout, Primary Side

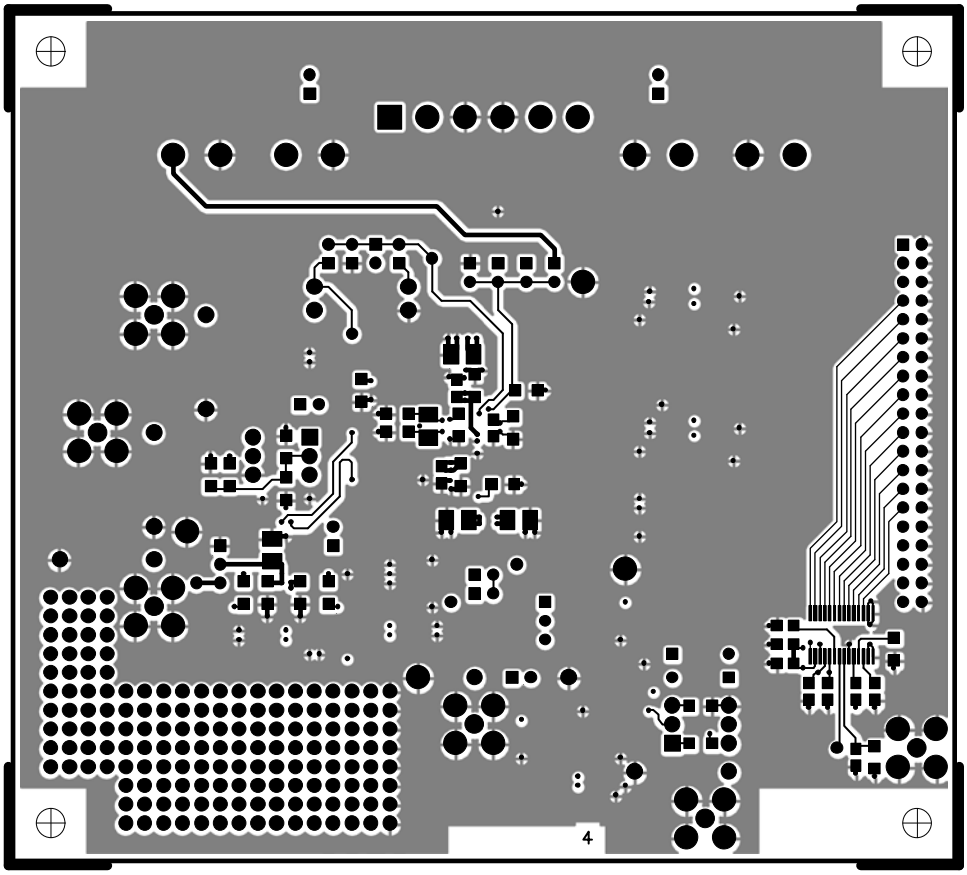


Figure 49. TSSOP Evaluation Board Layout, Secondary Side

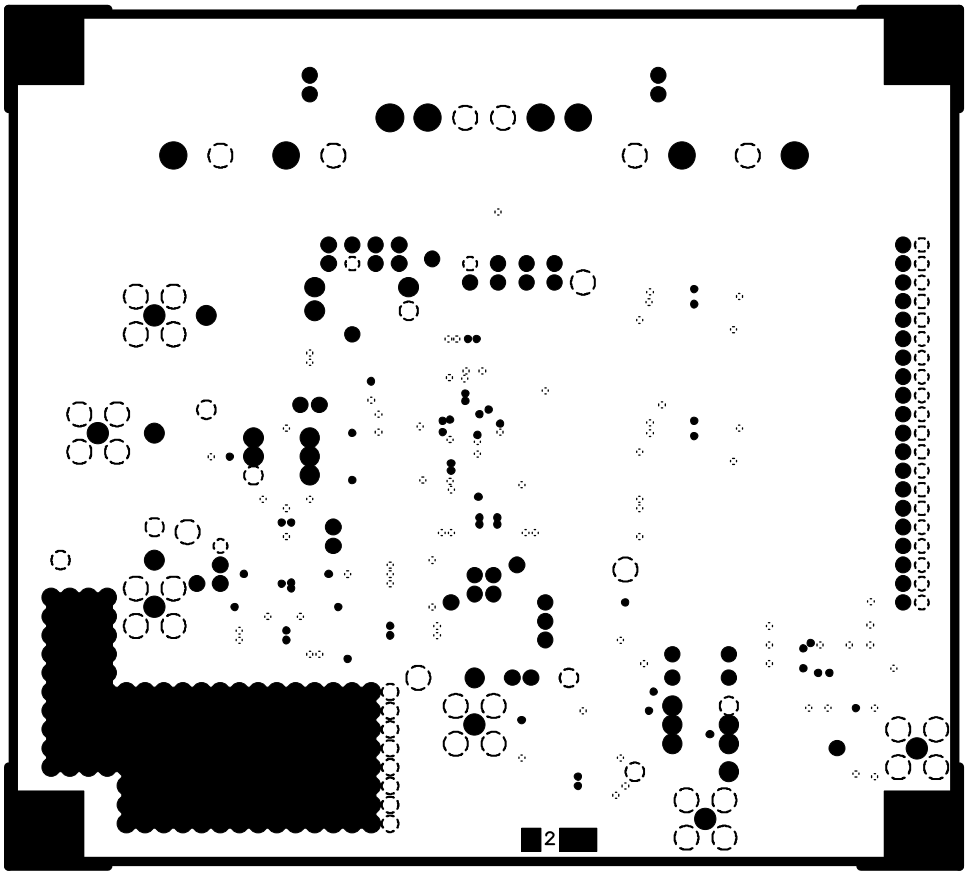


Figure 50. TSSOP Evaluation Board Layout, Ground Plane

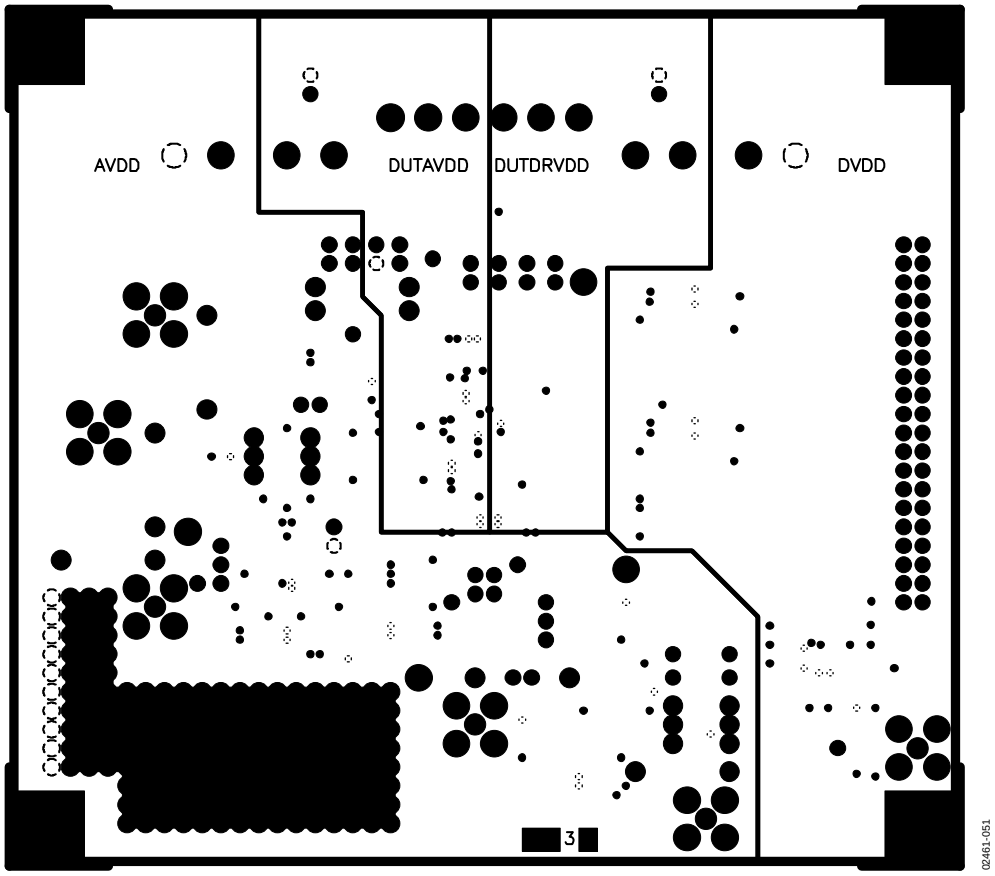


Figure 51. TSSOP Evaluation Board Power Plane

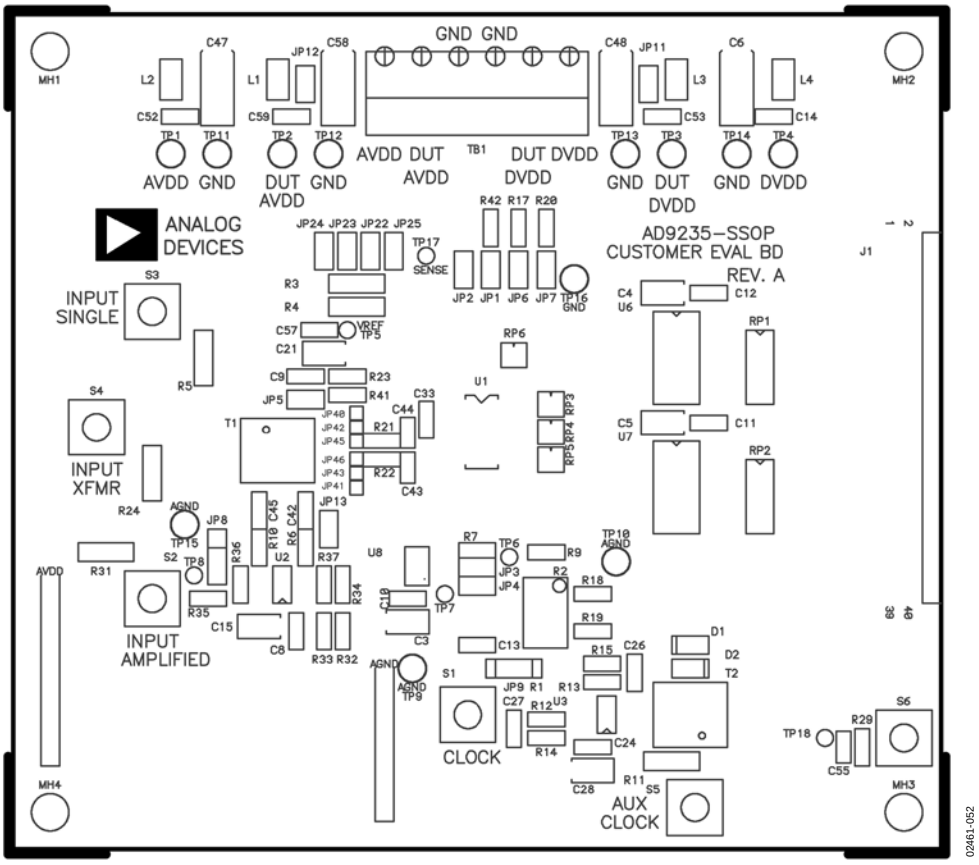


Figure 52. TSSOP Evaluation Board Layout, Primary Silkscreen

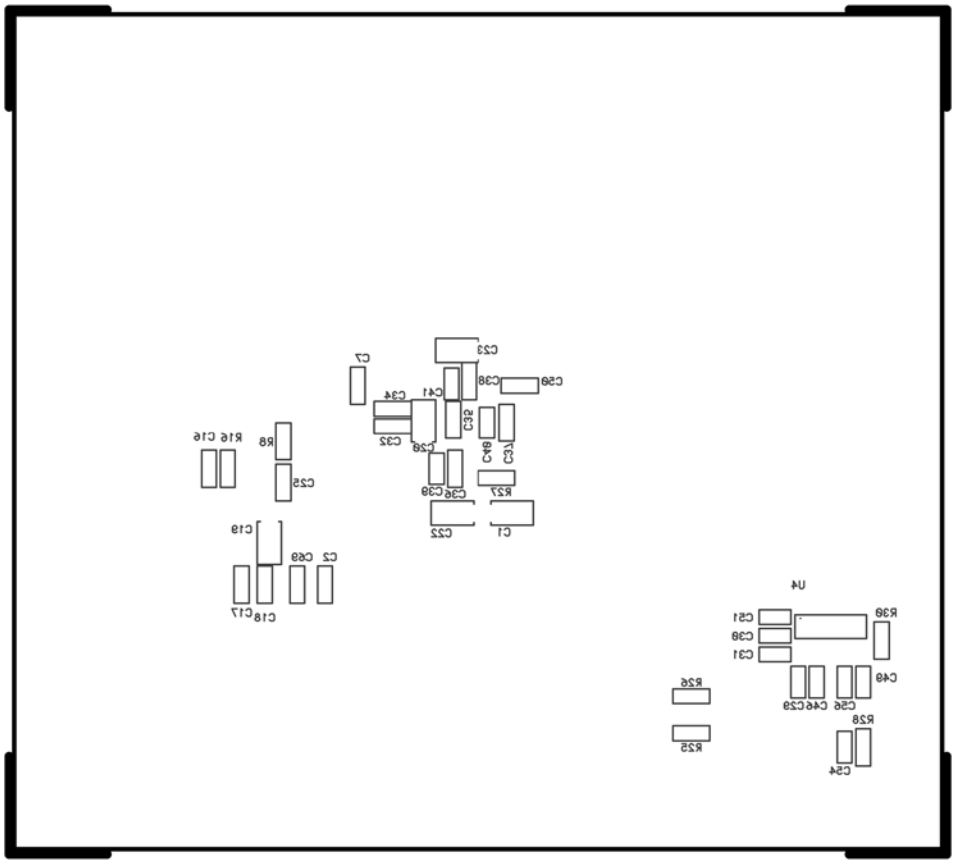
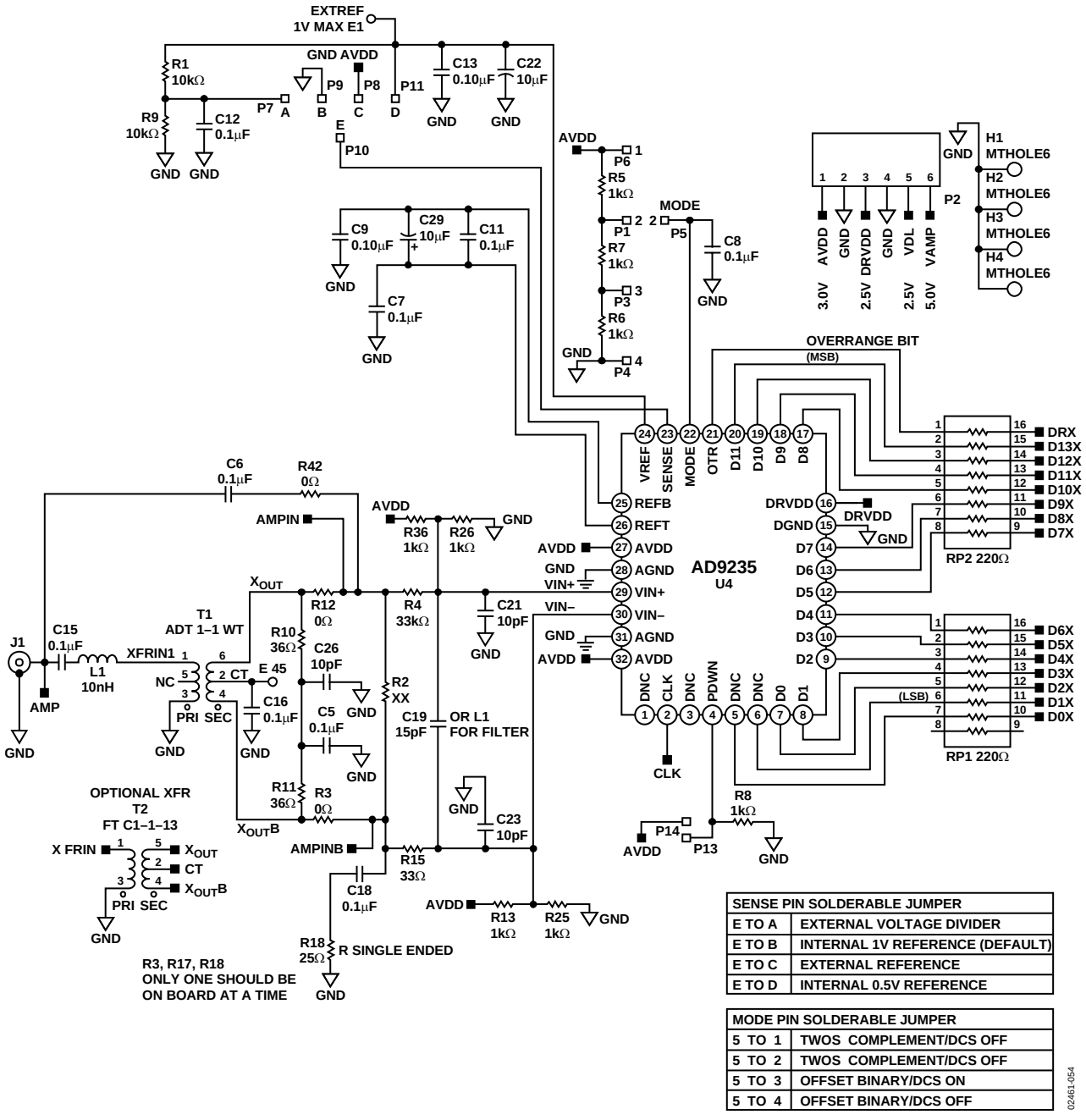


Figure 53. TSSOP Evaluation Board Layout, Secondary Silkscreen



SENSE PIN SOLDERABLE JUMPER	
E TO A	EXTERNAL VOLTAGE DIVIDER
E TO B	INTERNAL 1V REFERENCE (DEFAULT)
E TO C	EXTERNAL REFERENCE
E TO D	INTERNAL 0.5V REFERENCE

MODE PIN SOLDERABLE JUMPER	
5 TO 1	TWOS COMPLEMENT/DCS OFF
5 TO 2	TWOS COMPLEMENT/DCS OFF
5 TO 3	OFFSET BINARY/DCS ON
5 TO 4	OFFSET BINARY/DCS OFF

02461-054

Figure 54. LFCSP Evaluation Board Schematic, Analog Inputs and DUT

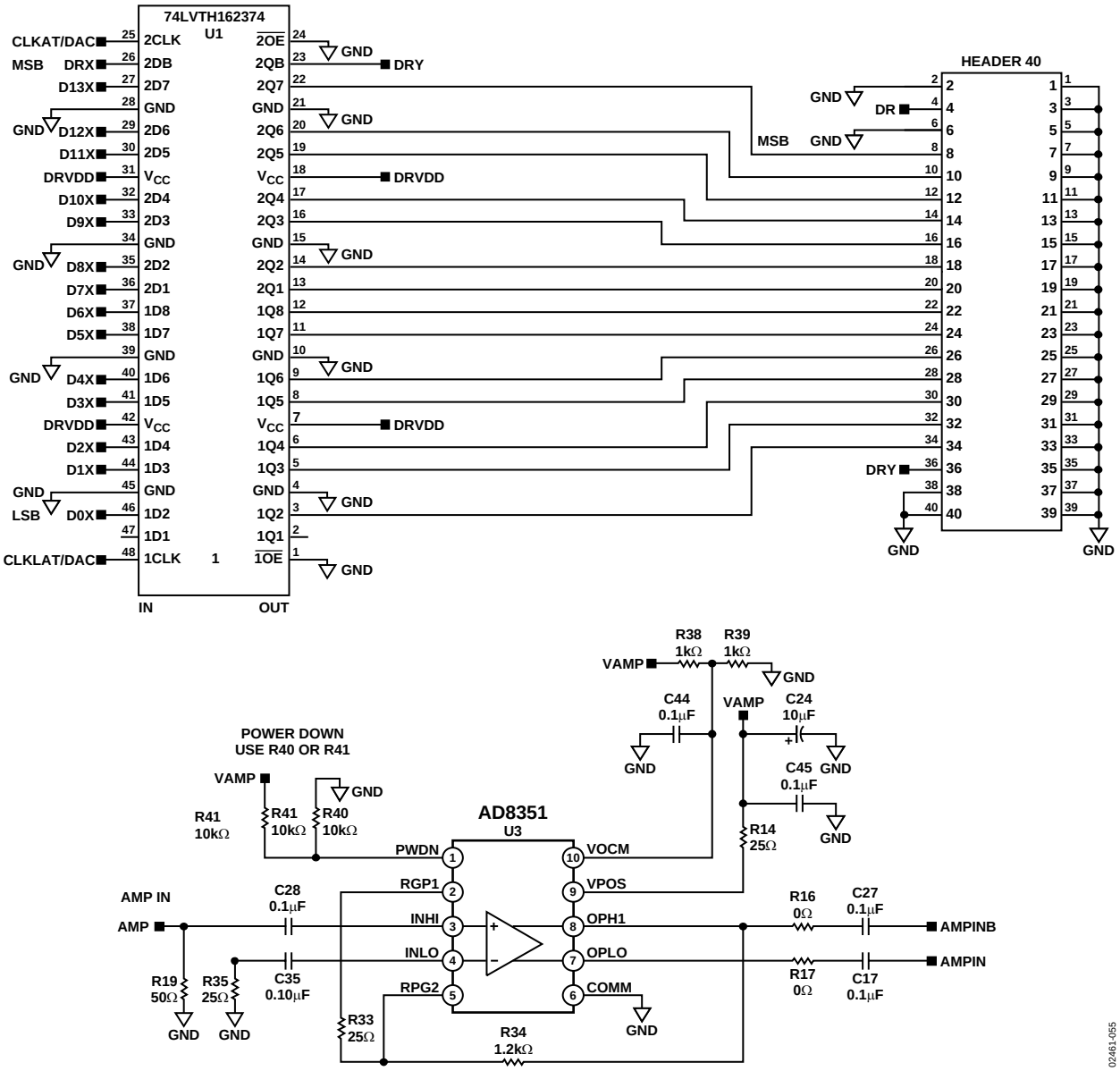


Figure 55. LFCSP Evaluation Board Schematic, Digital Path

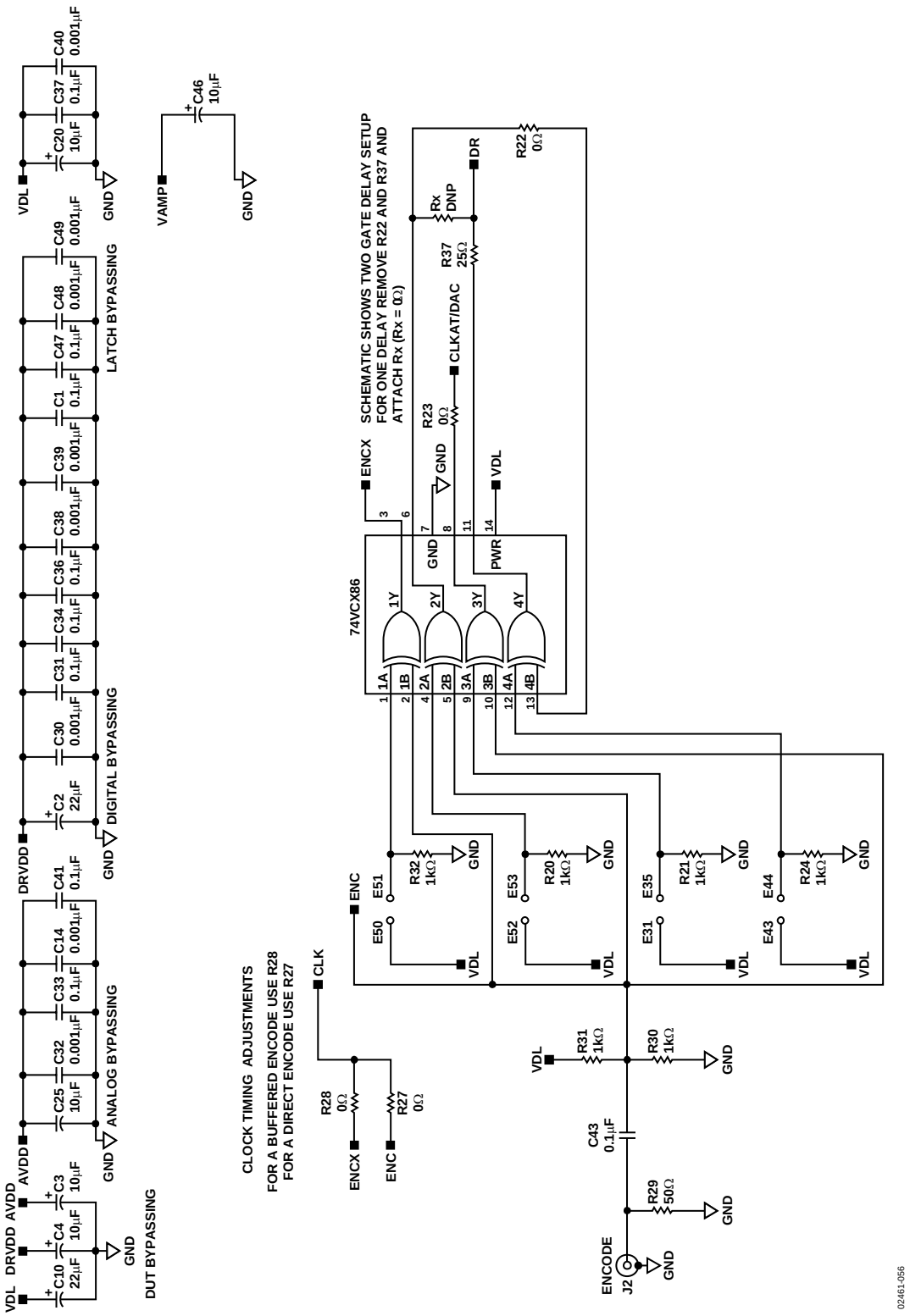


Figure 56. LFCSP Evaluation Board Schematic, Clock Input

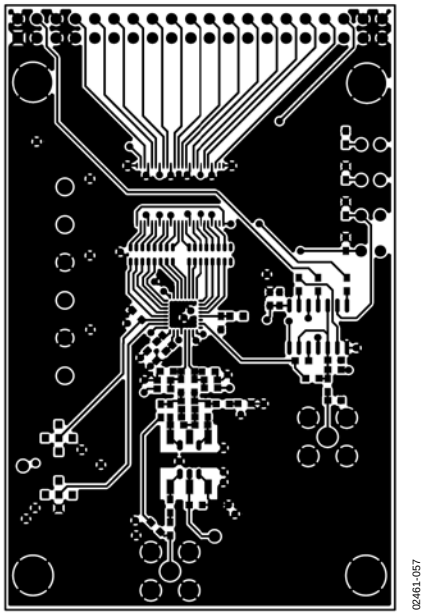


Figure 57. LFCSP Evaluation Board Layout, Primary Side

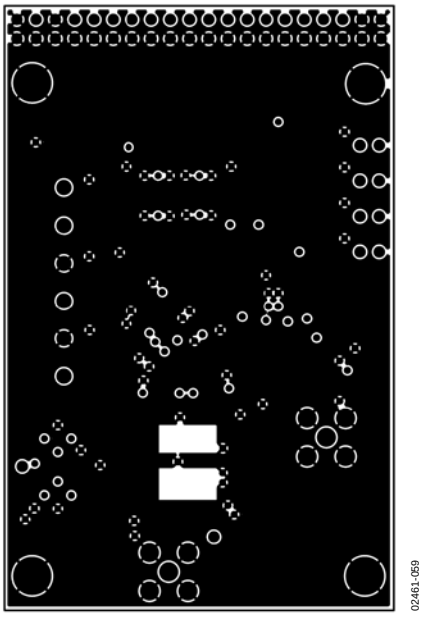


Figure 59. LFCSP Evaluation Board Layout, Ground Plane

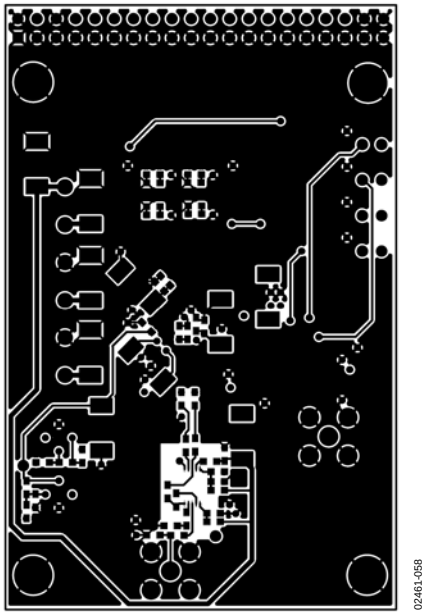


Figure 58. LFCSP Evaluation Board Layout, Secondary Side

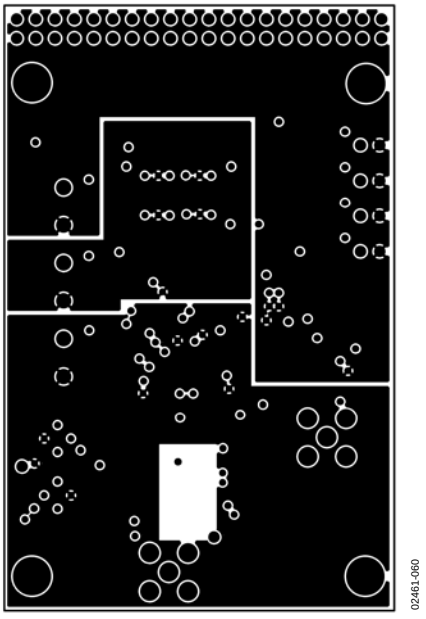


Figure 60. LFCSP Evaluation Board Layout, Power Plane

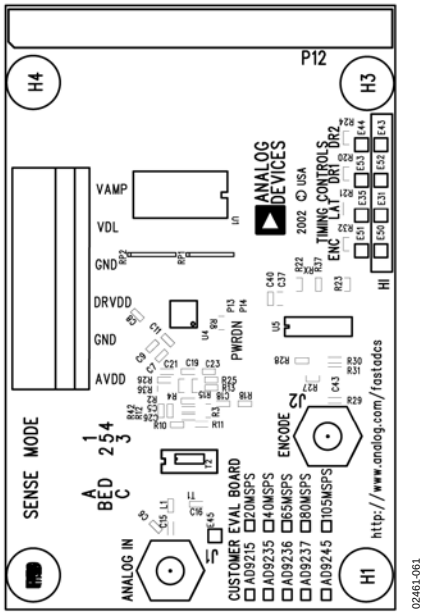


Figure 61. LFCSP Evaluation Board Layout, Primary Silkscreen

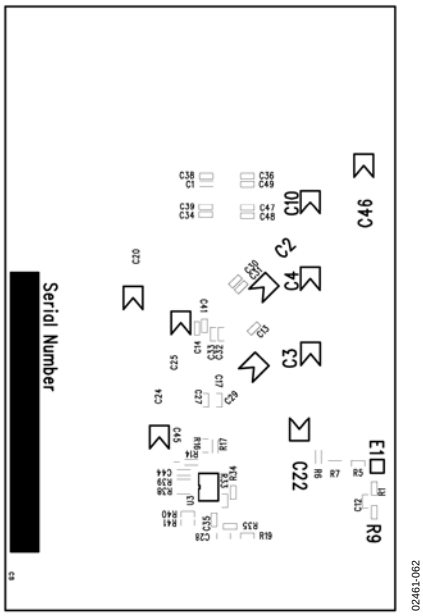


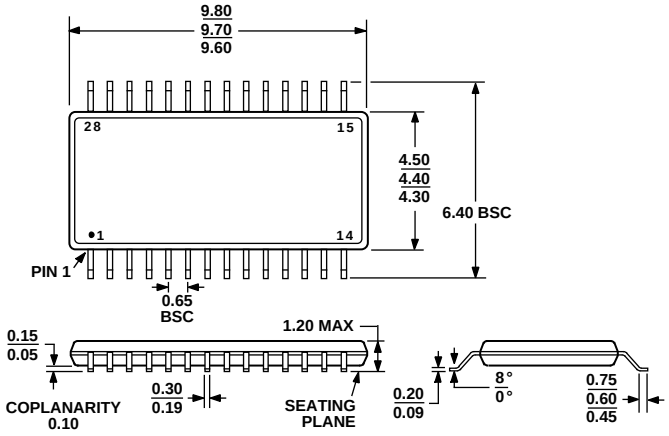
Figure 62. LFCSP Evaluation Board Layout, Secondary Silkscreen

Table 9. LFCSP Evaluation Board Bill of Materials (BOM)

Item	Qty.	Omit[1]	Reference Designator	Device	Package	Value	Recommended Vendor/ Part Number	Supplied by ADI
1	18		C1, C5, C7, C8, C9, C11, C12, C13, C15, C16, C31, C33, C34, C36, C37, C41, C43, C47	Chip Capacitor	0603	0.1 µF		
		8	C6, C18, C27, C17, C28, C35, C45, C44					
2	8		C2, C3, C4, C10, C20, C22, C25, C29	Tantalum Capacitor	TAJD	10 µF		
		2	C46, C24					
3	8		C14, C30, C32, C38, C39, C40, C48, C49	Chip Capacitor	0603	0.001 µF		
4	3		C19, C21, C23	Chip Capacitor	0603	10 pF		
5	1		C26	Chip Capacitor	0603	10 pF		
6	9		E31, E35, E43, E44, E50, E51, E52, E53	Header	EHOLE		Jumper Blocks	
		2	E1, E45					
7	2		J1, J2	SMA Connector/50 Ω	SMA			
8		1	L1	Inductor	0603	10 nH	Coilcraft/ 0603CS-10NXGBU	
9	1		P2	Terminal Block	TB6		Wieland/25.602.2653.0, z5-530-0625-0	
10	1		P12	Header Dual 20-Pin RT Angle	HEADER40		Digi-Key S2131-20-ND	
11	5		R3, R12, R23, R28, RX	Chip Resistor	0603	0 Ω		
		6	R37, R22, R42, R16, R17, R27					
12	2		R4, R15	Chip Resistor	0603	33 Ω		
13	14		R5, R6, R7, R8, R13, R20, R21, R24, R25, R26, R30, R31, R32, R36	Chip Resistor	0603	1 k Ω		
14	2		R10, R11	Chip Resistor	0603	36 Ω		
15	1		R29	Chip Resistor	0603	50 Ω		
		1	R19					
16	2		RP1, RP2	Resistor Pack	R_742	220 Ω	Digi-Key CTS/742C163220JTR	
17	1		T1	ADT1-1WT	AWT1-1T		Mini-Circuits	
18	1		U1	74LVTH162374 CMOS Register	TSSOP-48			
19	1		U4	AD9235BCP ADC (DUT)	LFCSP-32		Analog Devices, Inc.	X
20	1		U5	74VCX86M	SOIC-14		Fairchild	
21	1		PCB	AD92XXBCP/PCB	PCB		Analog Devices, Inc.	X
22		1	U3	AD8351 Op Amp	MSOP-8		Analog Devices, Inc.	X
23		1	T2	MACOM Transformer	ETC1-1-13	1-1 TX	M/A-COM/ETC1-1-13	
24		5	R9, R1, R2, R38, R39	Chip Resistor	0603	SELECT		
25		3	R18, R14, R35	Chip Resistor	0603	25 Ω		
26		2	R40, R41	Chip Resistor	0603	10 k Ω		
27		1	R34	Chip Resistor		1.2 k Ω		
28		1	R33	Chip Resistor		100 Ω		
Total	82	34						

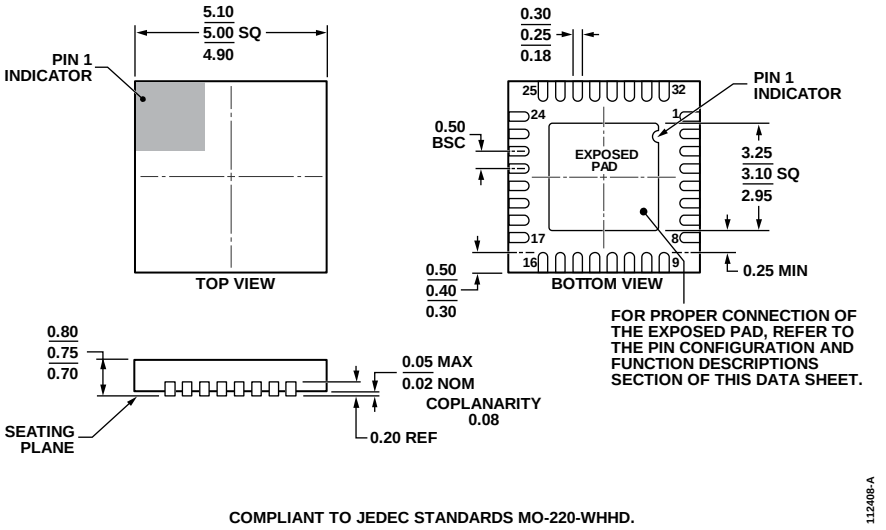
[1] These items are included in the PCB design but are omitted at assembly.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 63. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 64. 32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
5 × 5 mm Body, Very Very Thin Quad
(CP-32-7)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	Package Description	Package Option
AD9235BRU-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRURL7-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZ-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZRL7-20	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRU-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRURL7-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZ-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZRL7-40	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRU-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRURL7-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZ-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BRUZRL7-65	–40°C to +85°C	28-Lead Thin Shrink Small Outline Package (TSSOP)	RU-28
AD9235BCPZ-20	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9235BCPZRL7-20	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9235BCPZ-40	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9235BCPZRL7-40	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9235BCPZ-65	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7
AD9235BCPZRL7-65	–40°C to +85°C	32-Lead Lead Frame Chip Scale Package (LFCSP_WQ)	CP-32-7

[1] Z = RoHS Compliant Part.
[2] It is recommended that the exposed paddle be soldered to the ground plane. There is an increased reliability of the solder joints and maximum thermal capability of the package is achieved with exposed paddle soldered to the customer board.

NOTES

NOTES

NOTES

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D02461-0-10/12(D)

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- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management