THE DATASHEET OF

AD9238BSTZ-20

www.win-source.net 0086-755-83957316

12-Bit, 20 MSPS/40 MSPS/65 MSPS Dual A/D Converter

AD9238

FEATURES

Integrated dual 12-bit ADC
Single 3 V supply operation (2.7 V to 3.6 V)
SNR = 70 dB (to Nyquist, AD9238-65)
SFDR = 80.5 dBc (to Nyquist, AD9238-65)
Low power: 300 mW/channel at 65 MSPS
Differential input with 500 MHz, 3 dB bandwidth
Exceptional crosstalk immunity > 85 dB
Flexible analog input: 1 V p-p to 2 V p-p range
Offset binary or twos complement data format
Clock duty cycle stabilizer
Output datamux option

APPLICATIONS

Ultrasound equipment
Direct conversion or IF sampling receivers
WB-CDMA, CDMA2000, WiMAX
Battery-powered instruments
Hand-held scopemeters
Low cost, digital oscilloscopes

GENERAL DESCRIPTION

The AD9238 is a dual, 3 V, 12-bit, 20 MSPS/40 MSPS/65 MSPS analog-to-digital converter (ADC). It features dual high performance sample-and-hold amplifiers (SHAs) and an integrated voltage reference. The AD9238 uses a multistage differential pipelined architecture with output error correction logic to provide 12-bit accuracy and to guarantee no missing codes over the full operating temperature range at up to 65 MSPS data rates. The wide bandwidth, differential SHA allows for a variety of user-selectable input ranges and offsets, including single-ended applications. It is suitable for various applications, including multiplexed systems that switch full-scale voltage levels in successive channels and for sampling inputs at frequencies well beyond the Nyquist rate.

Dual single-ended clock inputs are used to control all internal conversion cycles. A duty cycle stabilizer is available and can compensate for wide variations in the clock duty cycle, allowing the converter to maintain excellent performance. The digital output data is presented in either straight binary or twos complement format. Out-of-range signals indicate an overflow condition, which can be used with the most significant bit to determine low or high overflow.

FUNCTIONAL BLOCK DIAGRAM

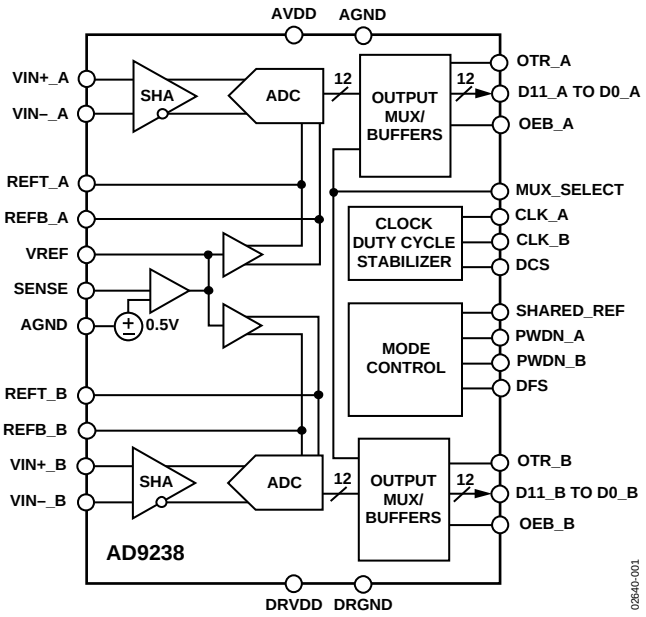

Figure 1.

Fabricated on an advanced CMOS process, the AD9238 is available in a Pb-free, space saving, 64-lead LQFP or LFCSP and is specified over the industrial temperature range (−40°C to +85°C).

PRODUCT HIGHLIGHTS

1. Pin-compatible with the AD9248, 14-bit 20MSPS/ 40 MSPS/65 MSPS ADC.
2. Speed grade options of 20 MSPS, 40 MSPS, and 65 MSPS allow flexibility between power, cost, and performance to suit an application.
3. Low power consumption: AD9238-65: 65 MSPS = 600 mW, AD9238-40: 40 MSPS = 330 mW, and AD9238-20: 20 MSPS = 180 mW.
4. Typical channel isolation of 85 dB @ f_{IN} = 10 MHz.
5. The clock duty cycle stabilizer (AD9238-20/AD9238-40/ AD9238-65) maintains performance over a wide range of clock duty cycles.
6. Multiplexed data output option enables single-port operation from either Data Port A or Data Port B.

Rev. C
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REVISION HISTORY

11/10—Rev. B to Rev. C

Changes to Absolute Maximum Ratings Section 7
Added Figure 4; Renumbered Sequentially 8
Changes to Analog Input Section 16
Deleted Note 1 from Dual ADC LFCSP PCB Section 34
Changes to Outline Dimensions 45

4/05—Rev. A to Rev. B

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2/03—Revision 0: Initial Version

SPECIFICATIONS

DC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 1.

		Test	AD9238BST/BCP-20			AD9238BST/BCP-40			AD9238BST/BCP-65			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	VI	12			12			12			Bits
ACCURACY												
No Missing Codes Guaranteed	Full	VI	12			12			12			Bits
Offset Error	Full	VI		±0.30	±1.2		±0.50	±1.1		±0.50	±1.1	% FSR
Gain Error[1]	Full	IV		±0.30	±2.2		±0.50	±2.4		±0.50	±2.5	% FSR
Differential Nonlinearity (DNL)[2]	Full	V		±0.35			±0.35			±0.35		LSB
	25°C	I		±0.35	±0.9		±0.35	±0.8		±0.35	±1.0	LSB
Integral Nonlinearity (INL)[2]	Full	V		±0.45			±0.60			±0.70		LSB
	25°C	I		±0.40	±1.4		±0.50	±1.4		±0.55	±1.75	LSB
TEMPERATURE DRIFT												
Offset Error	Full	V		±4			±4			±6		µV/°C
Gain Error	Full	V		±12			±12			±12		ppm/°C
INTERNAL VOLTAGE REFERENCE												
Output Voltage Error (1 V Mode)	Full	VI		±5	±35		±5	±35		±5	±35	mV
Load Regulation @ 1.0 mA	Full	V		0.8			0.8			0.8		mV
Output Voltage Error (0.5 V Mode)	Full	V		±2.5			±2.5			±2.5		mV
Load Regulation @ 0.5 mA	Full	V		0.1			0.1			0.1		mV
INPUT REFERRED NOISE												
Input Span = 1 V	25°C	V		0.54			0.54			0.54		LSB rms
Input Span = 2.0 V	25°C	V		0.27			0.27			0.27		LSB rms
ANALOG INPUT												
Input Span = 1.0 V	Full	IV		1			1			1		V p-p
Input Span = 2.0 V	Full	IV		2			2			2		V p-p
Input Capacitance[3]	Full	V		7			7			7		pF
REFERENCE INPUT RESISTANCE	Full	V		7			7			7		kΩ
POWER SUPPLIES												
Supply Voltages												
AVDD	Full	IV	2.7	3.0	3.6	2.7	3.0	3.6	2.7	3.0	3.6	V
DRVDD	Full	IV	2.25	3.0	3.6	2.25	3.0	3.6	2.25	3.0	3.6	V
Supply Current												
IAVDD[2]	Full	V		60			110			200		mA
IDRVDD[2]	Full	V		4			10			14		mA
PSRR	Full	V		±0.01			±0.01			±0.01		% FSR
POWER CONSUMPTION												
DC Input[4]	Full	V		180			330			600		mW
Sine Wave Input[2]	Full	VI		190	212		360	397		640	698	mW
Standby Power[5]	Full	V		2.0			2.0			2.0		mW
MATCHING CHARACTERISTICS												
Offset Error	25°C	V		±0.1			±0.1			±0.1		% FSR
Gain Error	25°C	V		±0.05			±0.05			±0.05		% FSR

[1] Gain error and gain temperature coefficient are based on the ADC only (with a fixed 1.0 V external reference).
[2] Measured at maximum clock rate with a low frequency sine wave input and approximately 5 pF loading on each output bit.
[3] Input capacitance refers to the effective capacitance between one differential input pin and AVSS. Refer to Figure 29 for the equivalent analog input structure.
[4] Measured with dc input at maximum clock rate.
[5] Standby power is measured with the CLK_A and CLK_B pins inactive (that is, set to AVDD or AGND).

AC SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 2.

		Test	AD9238BST/BCP-20			AD9238BST/BCP-40			AD9238BST/BCP-65			
Parameter	**Temp**	**Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)												
f_{INPUT} = 2.4 MHz	25°C	V		70.4			70.4			70.3		dB
f_{INPUT} = 9.7 MHz	Full	V		70.2								dB
	25°C	IV	69.7	70.4								dB
f_{INPUT} = 19.6 MHz	Full	V					70.1					dB
	25°C	IV				69.7	70.3					dB
f_{INPUT} = 32.5 MHz	Full	V								69.3		dB
	25°C	IV							68.7	70.0		dB
f_{INPUT} = 100 MHz	25°C	V		68.7			68.3			67.6		dB
SIGNAL-TO-NOISE AND DISTORTION RATIO (SINAD)												
f_{INPUT} = 2.4 MHz	25°C	V		70.2			70.2			70.1		dB
f_{INPUT} = 9.7 MHz	Full	V		70.1								dB
	25°C	IV	69.3	70.2								dB
f_{INPUT} = 19.6 MHz	Full	V					69.9					dB
	25°C	IV				69.4	70.1					dB
f_{INPUT} = 32.5 MHz	Full	V								68.9		dB
	25°C	IV							68.1	69.1		dB
f_{INPUT} = 100 MHz	25°C	V		67.9			67.9			66.6		dB
EFFECTIVE NUMBER OF BITS (ENOB)												
f_{INPUT} = 2.4 MHz	25°C	V		11.5			11.5			11.4		Bits
f_{INPUT} = 9.7 MHz	Full	V		11.4								Bits
	25°C	IV	11.3	11.5								Bits
f_{INPUT} = 19.6 MHz	Full	V					11.4					Bits
	25°C	IV				11.3	11.4					Bits
f_{INPUT} = 32.5 MHz	Full	V								11.2		Bits
	25°C	IV							11.1	11.3		Bits
f_{INPUT} = 100 MHz	25°C	V		11.1			11.1			10.9		Bits
WORST HARMONIC (SECOND or THIRD)												
f_{INPUT} = 9.7 MHz	Full	V		−84.0								dBc
f_{INPUT} = 19.6 MHz	Full	V					−85.0					dBc
f_{INPUT} = 35 MHz	Full	V								−80.0		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)												
f_{INPUT} = 2.4 MHz	25°C	V		86.0			86.0			86.0		dBc
f_{INPUT} = 9.7 MHz	Full	V		84.0								dBc
	25°C	I	76.1	86.0								dBc
f_{INPUT} = 19.6 MHz	Full	V					85.0					dBc
	25°C	I				76.7	86.0					dBc
f_{INPUT} = 32.5 MHz	Full	V								80.0		dBc
	25°C	I							72.5	80.5		dBc
f_{INPUT} = 100 MHz	25°C	V								75.0		dBc
CROSSTALK	Full	V		−85.0			−85.0			−85.0		dB

DIGITAL SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 3.

Parameter	Temp	Test Level	AD9238BST/BCP-20 Min	Typ	Max	AD9238BST/BCP-40 Min	Typ	Max	AD9238BST/BCP-65 Min	Typ	Max	Unit
LOGIC INPUTS												
High Level Input Voltage	Full	IV	2.0			2.0			2.0			V
Low Level Input Voltage	Full	IV			0.8			0.8			0.8	V
High Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Low Level Input Current	Full	IV	−10		+10	−10		+10	−10		+10	µA
Input Capacitance	Full	IV		2			2			2		pF
LOGIC OUTPUTS[1]												
High Level Output Voltage	Full	IV	DRVDD – 0.05			DRVDD – 0.05			DRVDD – 0.05			V
Low Level Output Voltage	Full	IV			0.05			0.05			0.05	V

[1] Output voltage levels measured with capacitive load only on each output.

SWITCHING SPECIFICATIONS

AVDD = 3 V, DRVDD = 2.5 V, maximum sample rate, CLK_A = CLK_B; A_{IN} = −0.5 dBFS differential input, 1.0 V internal reference, T_{MIN} to T_{MAX}, DCS enabled, unless otherwise noted.

Table 4.

Parameter	Temp	Test Level	AD9238BST/BCP-20 Min	Typ	Max	AD9238BST/BCP-40 Min	Typ	Max	AD9238BST/BCP-65 Min	Typ	Max	Unit
SWITCHING PERFORMANCE												
Maximum Conversion Rate	Full	VI	20			40			65			MSPS
Minimum Conversion Rate	Full	V			1			1			1	MSPS
CLK Period	Full	V	50.0			25.0			15.4			ns
CLK Pulse-Width High[1]	Full	V	15.0			8.8			6.2			ns
CLK Pulse-Width Low[1]	Full	V	15.0			8.8			6.2			ns
DATA OUTPUT PARAMETER												
Output Delay[2] (t_{PD})	Full	VI	2	3.5	6	2	3.5	6	2	3.5	6	ns
Pipeline Delay (Latency)	Full	V		7			7			7		Cycles
Aperture Delay (t_A)	Full	V		1.0			1.0			1.0		ns
Aperture Uncertainty (t_J)	Full	V		0.5			0.5			0.5		ps rms
Wake-Up Time[3]	Full	V		2.5			2.5			2.5		ms
OUT-OF-RANGE RECOVERY TIME	Full	V		2			2			2		Cycles

[1] The AD9238-65 model has a duty cycle stabilizer circuit that, when enabled, corrects for a wide range of duty cycles (see Figure 24).
[2] Output delay is measured from clock 50% transition to data 50% transition, with a 5 pF load on each output.
[3] Wake-up time is dependent on the value of the decoupling capacitors; typical values shown with 0.1 µF and 10 µF capacitors on REFT and REFB.

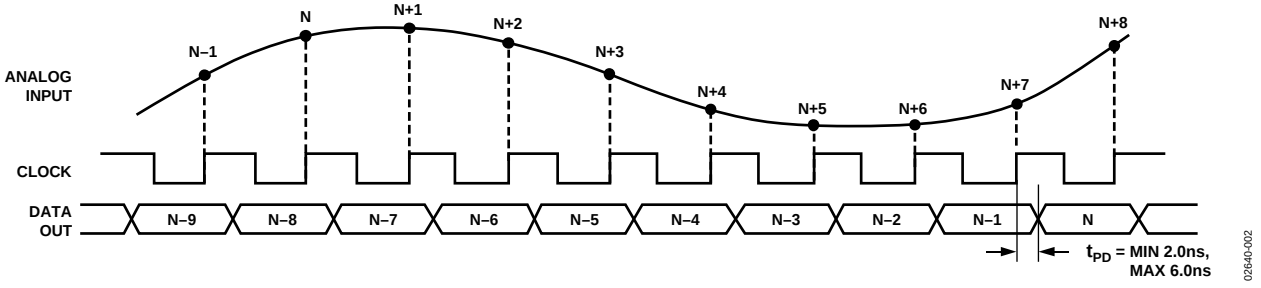


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

Table 5.

Parameter	Rating
ELECTRICAL	
AVDD to AGND	−0.3 V to +3.9 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +3.9 V
Digital Outputs to DRGND	−0.3 V to DRVDD + 0.3 V
OEB, DFS, CLK, DCS, MUX_SELECT, SHARED_REF to AGND	−0.3 V to AVDD + 0.3 V
VINA, VINB to AGND	−0.3 V to AVDD + 0.3 V
VREF to AGND	−0.3 V to AVDD + 0.3 V
SENSE to AGND	−0.3 V to AVDD + 0.3 V
REFB, REFT to AGND	−0.3 V to AVDD + 0.3 V
PDWN to AGND	−0.3 V to AVDD + 0.3 V
ENVIRONMENTAL[1]	
Operating Temperature	−40°C to +85°C
Junction Temperature	150°C
Lead Temperature (10 sec)	300°C
Storage Temperature	−65°C to +150°C

[1] Typical thermal impedances: 64-lead LQFP, θ_{JA} = 54°C/W; 64-lead LFCSP, θ_{JA} = 26.4°C/W with heat slug soldered to ground plane. These measurements were taken on a 4-layer board in still air, in accordance with EIA/JESD51-7.

EXPLANATION OF TEST LEVELS

I 100% production tested.

II 100% production tested at 25°C and sample tested at specified temperatures.

III Sample tested only.

IV Parameter is guaranteed by design and characterization testing.

V Parameter is a typical value only.

VI 100% production tested at 25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

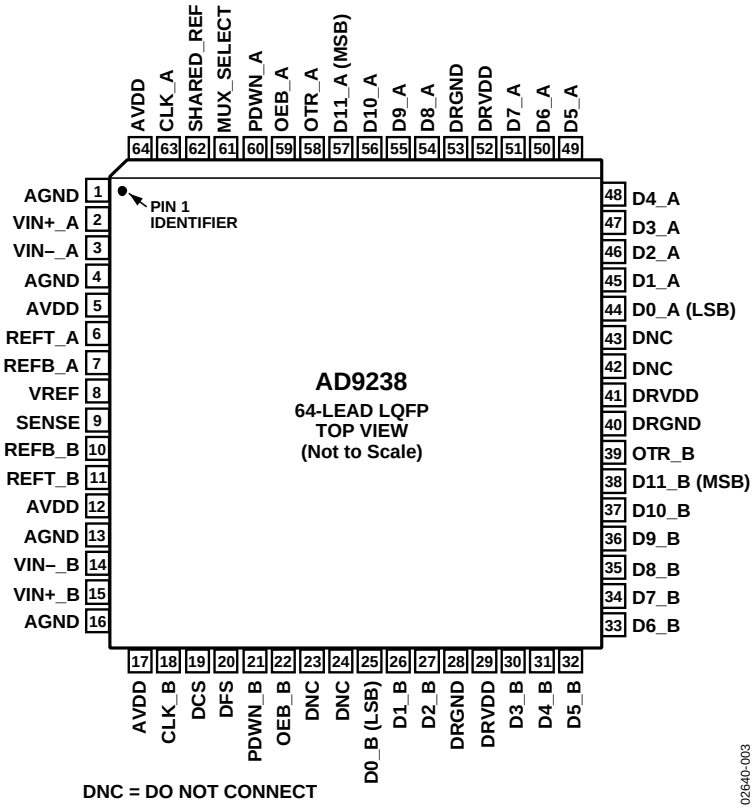
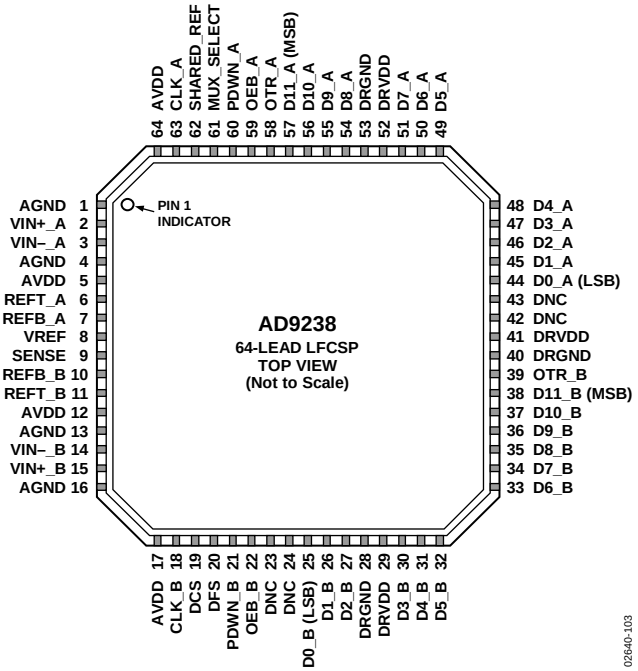


Figure 3. 64-Lead LQFP Pin Configuration



NOTES
1. THERE IS AN EXPOSED PAD THAT MUST CONNECT TO AGND.
2. DNC = DO NOT CONNECT.

Figure 4. 64-Lead LFCSP Pin Configuration

Table 6. 64-Lead LQFP and 64-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 13, 16	AGND	Analog Ground.
2	VIN+_A	Analog Input Pin (+) for Channel A.
3	VIN−_A	Analog Input Pin (−) for Channel A.
5, 12, 17, 64	AVDD	Analog Power Supply.
6	REFT_A	Differential Reference (+) for Channel A.
7	REFB_A	Differential Reference (−) for Channel A.
8	VREF	Voltage Reference Input/Output.
9	SENSE	Reference Mode Selection.
10	REFB_B	Differential Reference (−) for Channel B.
11	REFT_B	Differential Reference (+) for Channel B.
14	VIN−_B	Analog Input Pin (−) for Channel B.
15	VIN+_B	Analog Input Pin (+) for Channel B.
18	CLK_B	Clock Input Pin for Channel B.
19	DCS	Enable Duty Cycle Stabilizer (DCS) Mode (Tie High to Enable).
20	DFS	Data Output Format Select Bit (Low for Offset Binary, High for Twos Complement).
21	PDWN_B	Power-Down Function Selection for Channel B: Logic 0 enables Channel B. Logic 1 powers down Channel B. (Outputs static, not High-Z.)
22	OEB_B	Output Enable Bit for Channel B: Logic 0 enables Data Bus B. Logic 1 sets outputs to High-Z.
23, 24, 42, 43	DNC	Do Not Connect Pins. Should be left floating.
25 to 27, 30 to 38	D0_B (LSB) to D11_B (MSB)	Channel B Data Output Bits.
28, 40, 53	DRGND	Digital Output Ground.
29, 41, 52	DRVDD	Digital Output Driver Supply. Must be decoupled to DRGND with a minimum 0.1 µF capacitor. Recommended decoupling is 0.1 µF capacitor in parallel with 10 µF.
39	OTR_B	Out-of-Range Indicator for Channel B.
44 to 51, 54 to 57	D0_A (LSB) to D11_A (MSB)	Channel A Data Output Bits.
58	OTR_A	Out-of-Range Indicator for Channel A.
59	OEB_A	Output Enable Bit for Channel A: Logic 0 enables Data Bus A. Logic 1 sets outputs to High-Z.
60	PDWN_A	Power-Down Function Selection for Channel A: Logic 0 enables Channel A. Logic 1 powers down Channel A. (Outputs static, not High-Z.)
61	MUX_SELECT	Data Multiplexed Mode. (See Data Format section for how to enable; high setting disables output data multiplexed mode).
62	SHARED_REF	Shared Reference Control Bit (Low for Independent Reference Mode, High for Shared Reference Mode).
63	CLK_A	Clock Input Pin for Channel A.
	EP	For the 64-Lead LFCSP only, there is an exposed pad that must connect to AGND.

TERMINOLOGY

Aperture Delay
SHA performance measured from the rising edge of the clock input to when the input signal is held for conversion.

Aperture Jitter
The variation in aperture delay for successive samples, which is manifested as noise on the input to the ADC.

Integral Nonlinearity (INL)
Deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Guaranteed no missing codes to 12-bit resolution indicates that all 4,096 codes must be present over all operating ranges.

Offset Error
The major carry transition should occur for an analog value ½ LSB below VIN+ = VIN−. Offset error is defined as the deviation of the actual transition from that point.

Gain Error
The first code transition should occur at an analog value ½ LSB above negative full scale. The last transition should occur at an analog value 1½ LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Temperature Drift
The temperature drift for zero error and gain error specifies the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection
The specification shows the maximum change in full scale from the value with the supply at the minimum limit to the value with the supply at its maximum limit.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal, expressed as a percentage or in decibels relative to the peak carrier signal (dBc).

Signal-to-Noise and Distortion (SINAD) Ratio
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for SINAD is expressed in dB.

Effective Number of Bits (ENOB)
Using the following formula

$$ENOB = (SINAD - 1.76)/6.02$$

ENOB for a device for sine wave inputs at a given input frequency can be calculated directly from its measured *SINAD*.

Signal-to-Noise Ratio (SNR)
The ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding the first six harmonics and dc. The value for SNR is expressed in dB.

Spurious-Free Dynamic Range (SFDR)
The difference in dB between the rms amplitude of the input signal and the peak spurious signal, which may or may not be a harmonic.

Nyquist Sampling
When the frequency components of the analog input are below the Nyquist frequency ($f_{CLOCK}/2$), this is often referred to as Nyquist sampling.

IF Sampling
Due to the effects of aliasing, an ADC is not limited to Nyquist sampling. Higher sampled frequencies are aliased down into the first Nyquist zone (DC – $f_{CLOCK}/2$) on the output of the ADC. The bandwidth of the sampled signal should not overlap Nyquist zones and alias onto itself. Nyquist sampling performance is limited by the bandwidth of the input SHA and clock jitter (jitter adds more noise at higher input frequencies).

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product.

Out-of-Range Recovery Time
The time it takes for the ADC to reacquire the analog input after a transient from 10% above positive full scale to 10% above negative full scale, or from 10% below negative full scale to 10% below positive full scale.

Crosstalk
Coupling onto one channel being driven by a (−0.5 dBFS) signal when the adjacent interfering channel is driven by a full-scale signal. Measurement includes all spurs resulting from both direct coupling and mixing components.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD, DRVDD = 3.0 V, T = 25°C, A_{IN} differential drive, full scale = 2 V, unless otherwise noted.

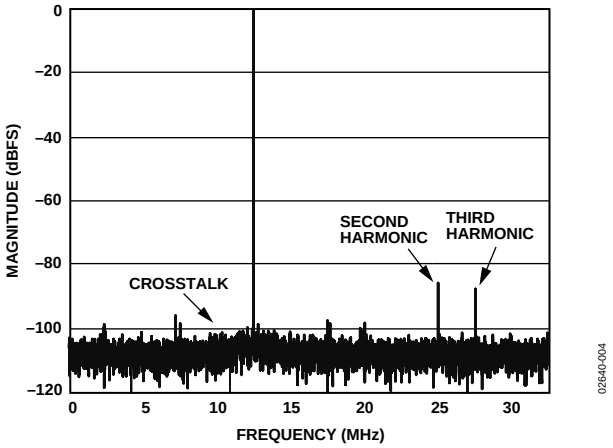


Figure 5. Single-Tone FFT of Channel A Digitizing f_{IN} = 12.5 MHz While Channel B Is Digitizing f_{IN} = 10 MHz

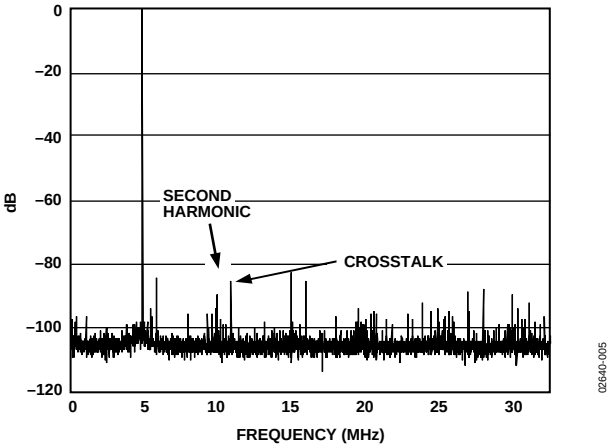


Figure 6. Single-Tone FFT of Channel A Digitizing f_{IN} = 70 MHz While Channel B Is Digitizing f_{IN} = 76 MHz

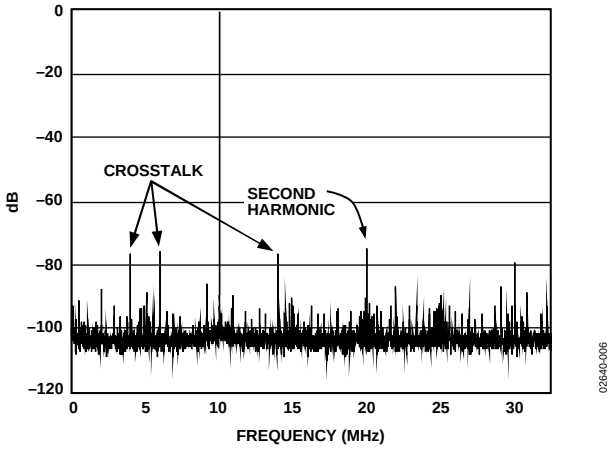


Figure 7. Single-Tone FFT of Channel A Digitizing f_{IN} = 120 MHz While Channel B is Digitizing f_{IN} = 126 MHz

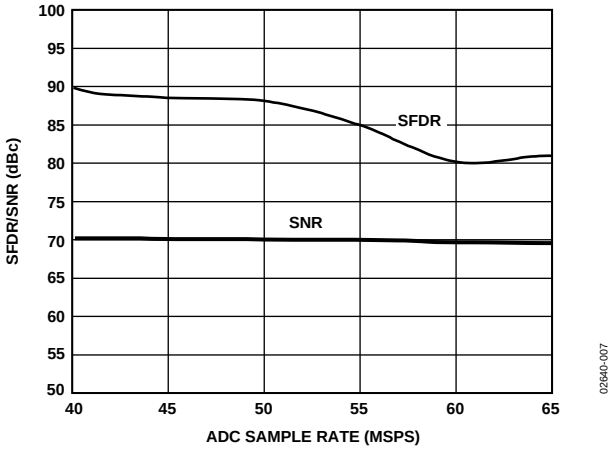


Figure 8. AD9238-65 Single-Tone SNR/SFDR vs. FS with f_{IN} = 32.5 MHz

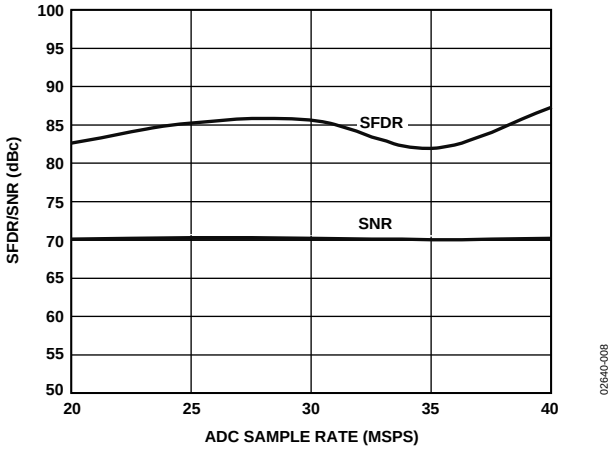


Figure 9. AD9238-40 Single-Tone SNR/SFDR vs. FS with f_{IN} = 20 MHz

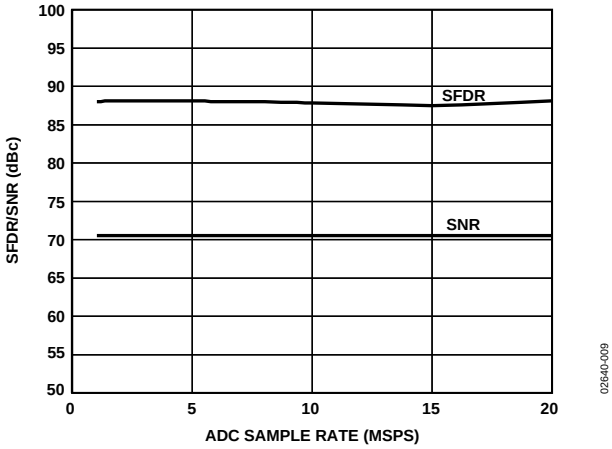


Figure 10. AD9238-20 Single-Tone SNR/SFDR vs. FS with f_{IN} = 10 MHz

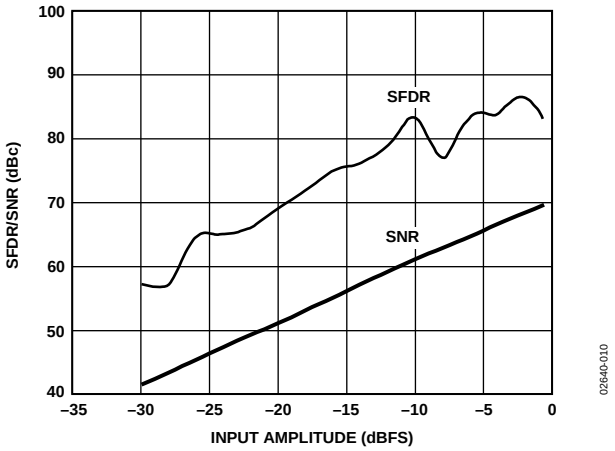


Figure 11. AD9238-65 Single-Tone SNR/SFDR vs. AIN with f_{IN} = 32.5 MHz

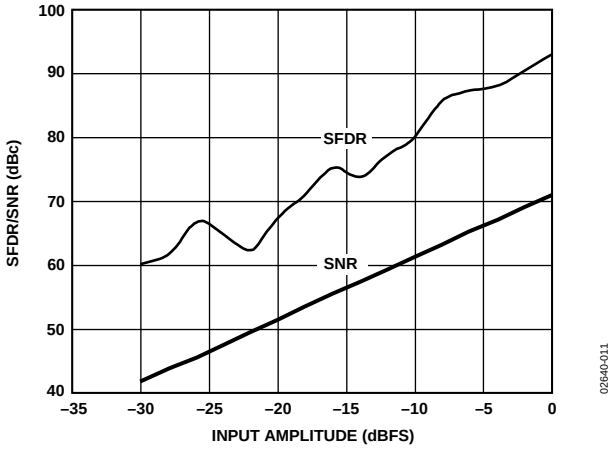


Figure 12. AD9238-40 Single-Tone SNR/SFDR vs. AIN with f_{IN} = 20 MHz

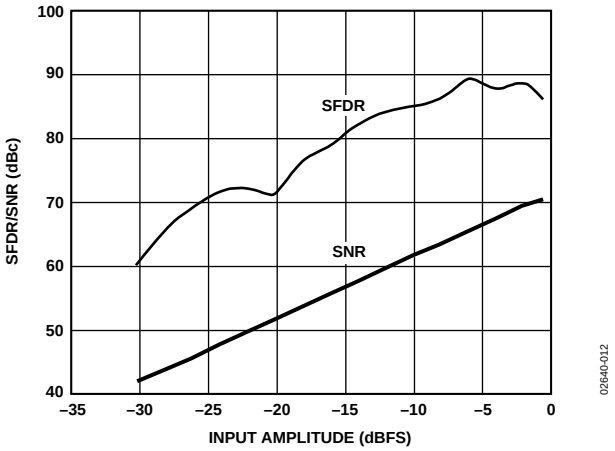


Figure 13. AD9238-20 Single-Tone SNR/SFDR vs. AIN with f_{IN} = 10 MHz

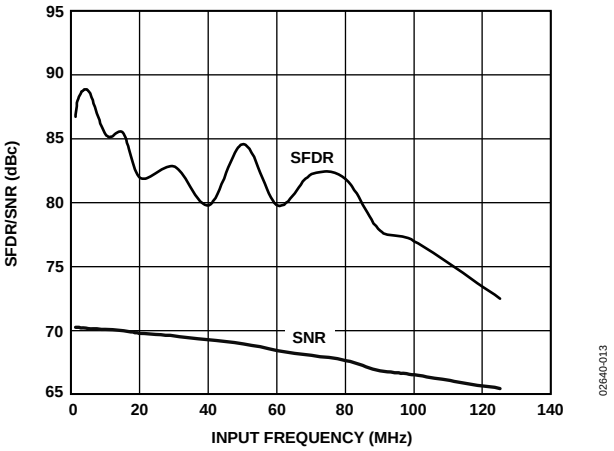


Figure 14. AD9238-65 Single-Tone SNR/SFDR vs. f_{IN}

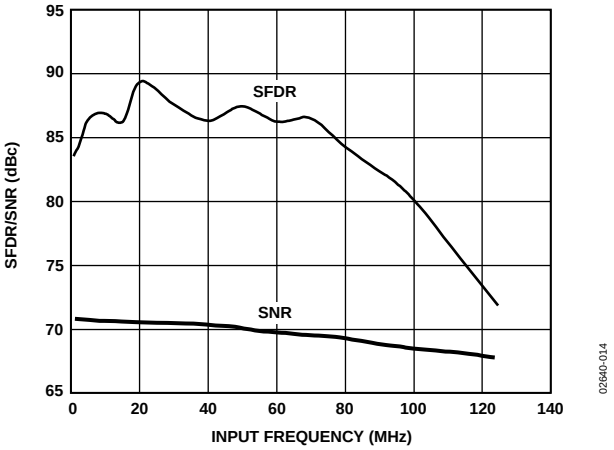


Figure 15. AD9238-40 Single-Tone SNR/SFDR vs. f_{IN}

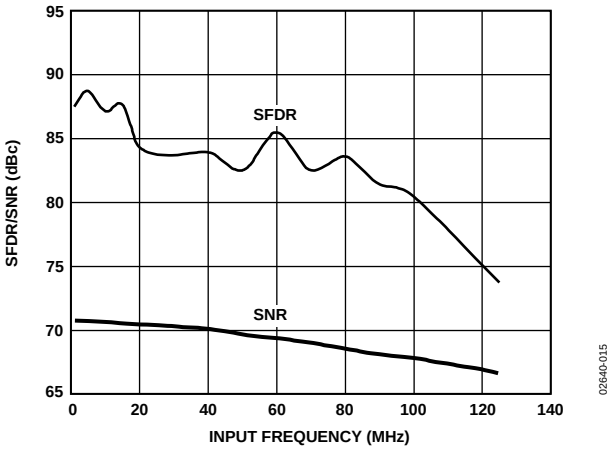


Figure 16. AD9238-20 Single-Tone SNR/SFDR vs. f_{IN}

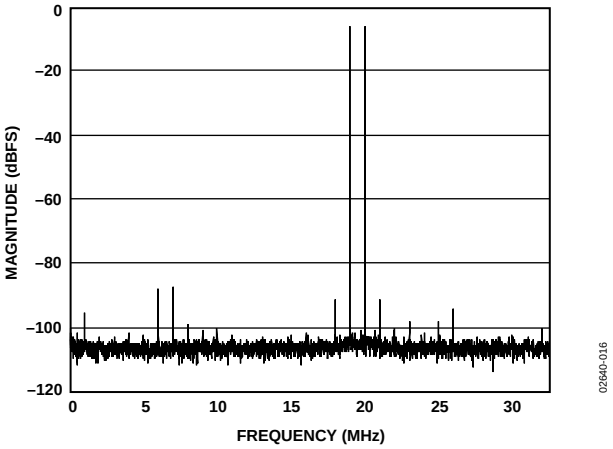


Figure 17. Dual-Tone FFT with $f_{IN}1 = 45$ MHz and $f_{IN}2 = 46$ MHz

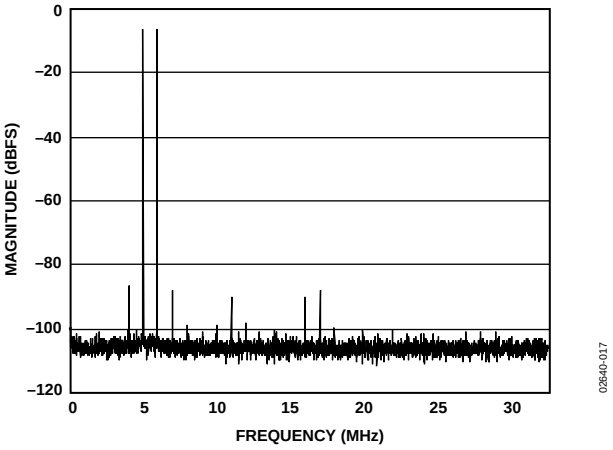


Figure 18. Dual-Tone FFT with $f_{IN}1 = 70$ MHz and $f_{IN}2 = 71$ MHz

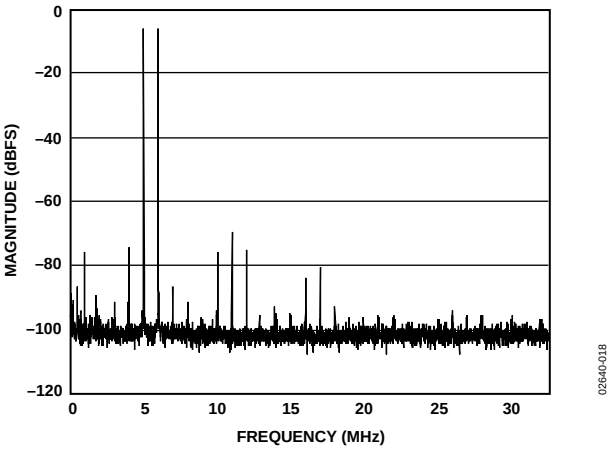


Figure 19. Dual-Tone FFT with $f_{IN}1 = 200$ MHz and $f_{IN}2 = 201$ MHz

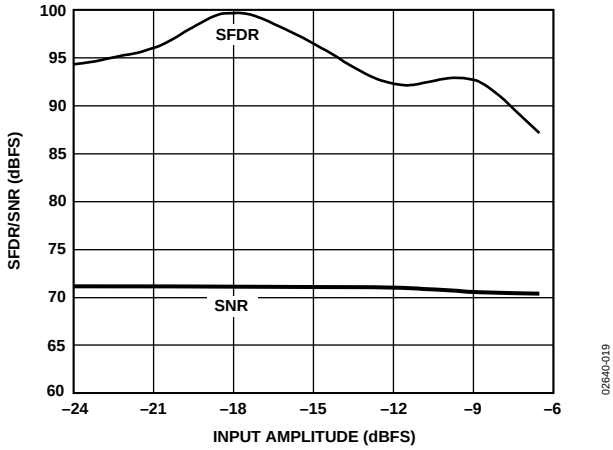


Figure 20. Dual-Tone SNR/SFDR vs. AIN with $f_{IN}1 = 45$ MHz and $f_{IN}2 = 46$ MHz

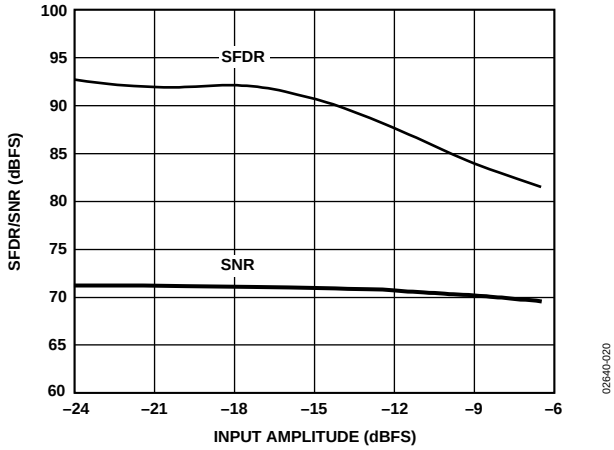


Figure 21. Dual-Tone SNR/SFDR vs. AIN with $f_{IN}1 = 70$ MHz and $f_{IN}2 = 71$ MHz

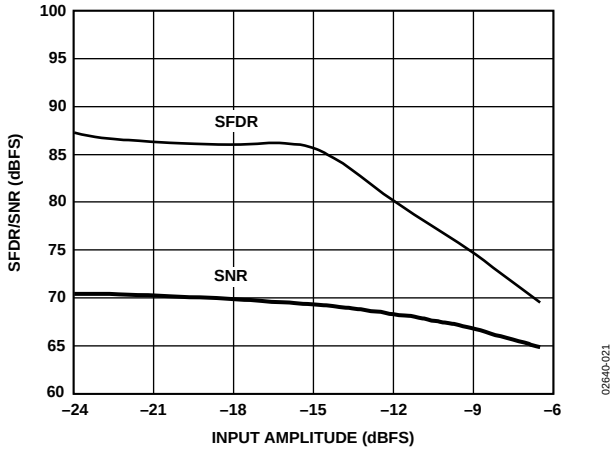


Figure 22. Dual-Tone SNR/SFDR vs. AIN with $f_{IN}1 = 200$ MHz and $f_{IN}2 = 201$ MHz

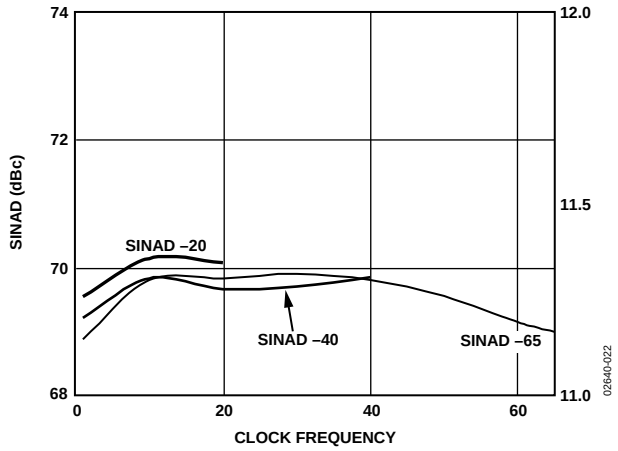


Figure 23. SINAD vs. FS with Nyquist Input

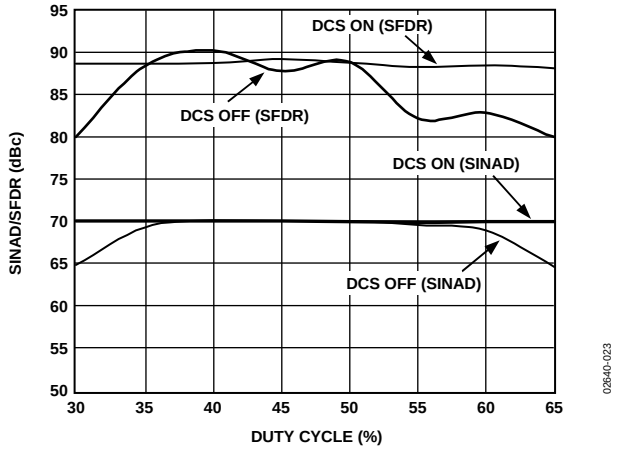


Figure 24. SINAD/SFDR vs. Clock Duty Cycle

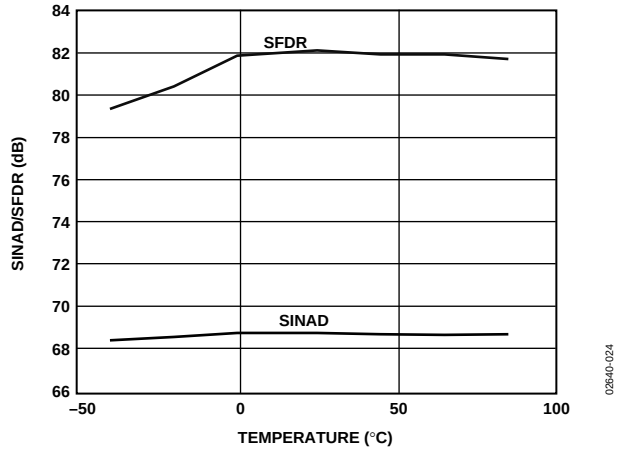


Figure 25. SINAD/SFDR vs. Temperature with f_{IN} = 32.5 MHz

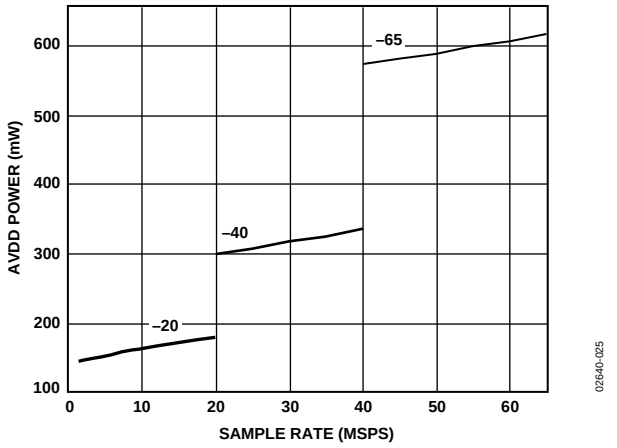


Figure 26. Analog Power Consumption vs. FS

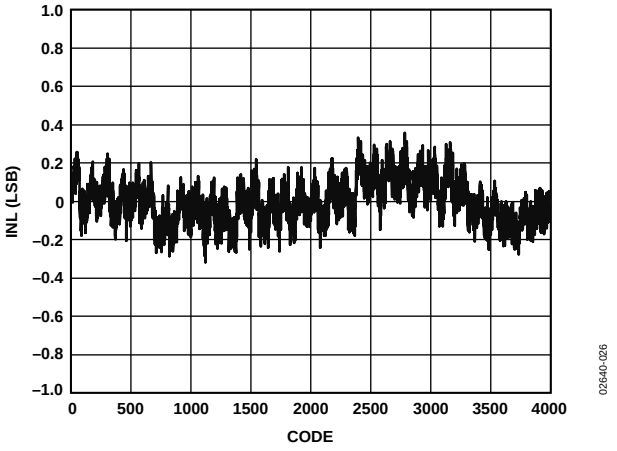


Figure 27. AD9238-65 Typical INL

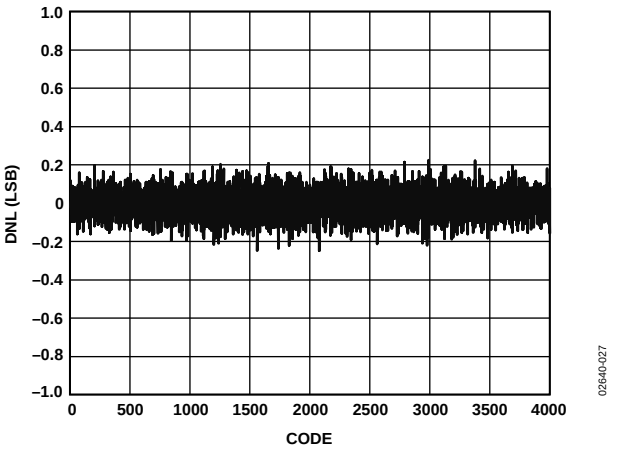


Figure 28. AD9238-65 Typical DNL

EQUIVALENT CIRCUITS

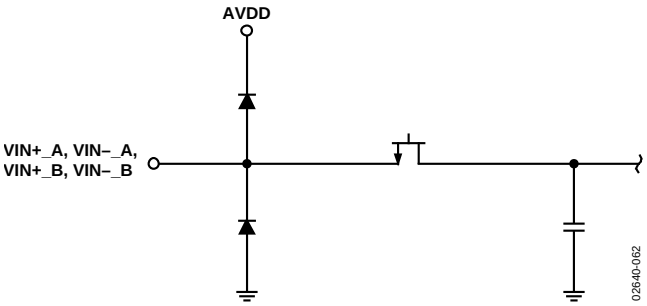


Figure 29. Equivalent Analog Input Circuit

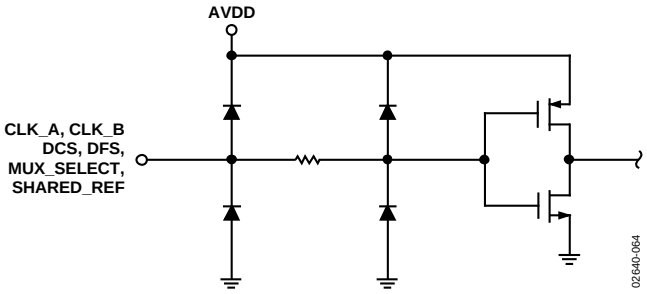


Figure 31. Equivalent Digital Input Circuit

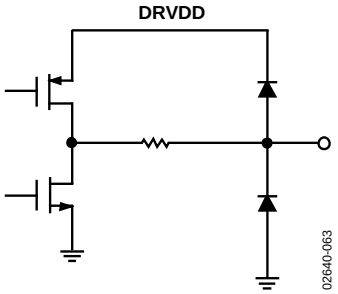


Figure 30. Equivalent Digital Output Circuit

THEORY OF OPERATION

The AD9238 consists of two high performance ADCs that are based on the AD9235 converter core. The dual ADC paths are independent, except for a shared internal band gap reference source, VREF. Each of the ADC paths consists of a proprietary front end SHA followed by a pipelined switched-capacitor ADC. The pipelined ADC is divided into three sections, consisting of a 4-bit first stage, followed by eight 1.5-bit stages, and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stages. The quantized outputs from each stage are combined through the digital correction logic block into a final 12-bit result. The pipelined architecture permits the first stage to operate on a new input sample, while the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the respective clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC and a residual multiplier to drive the next stage of the pipeline. The residual multiplier uses the flash ADC output to control a switched-capacitor digital-to-analog converter (DAC) of the same resolution. The DAC output is subtracted from the stage's input signal and the residual is amplified (multiplied) to drive the next pipeline stage. The residual multiplier stage is also called a multiplying DAC (MDAC). One bit of redundancy is used in each one of the stages to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage contains a differential SHA that can be configured as ac- or dc-coupled in differential or single-ended modes. The output-staging block aligns the data, carries out the error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing.

ANALOG INPUT

The analog input to the AD9238 is a differential, switched-capacitor, SHA that has been designed for optimum performance while processing a differential input signal. The SHA input accepts inputs over a wide common-mode range. An input common-mode voltage of midsupply is recommended to maintain optimal performance.

The SHA input is a differential, switched-capacitor circuit. In Figure 32, the clock signal alternatively switches the SHA between sample mode and hold mode. When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within one-half of a clock cycle. A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. Also, a small shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In IF undersampling applications, any shunt capacitors should be removed. In combination with the driving source impedance, they limit the input bandwidth. For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched such that common-mode settling errors are symmetrical. These errors are reduced by the common-mode rejection of the ADC.

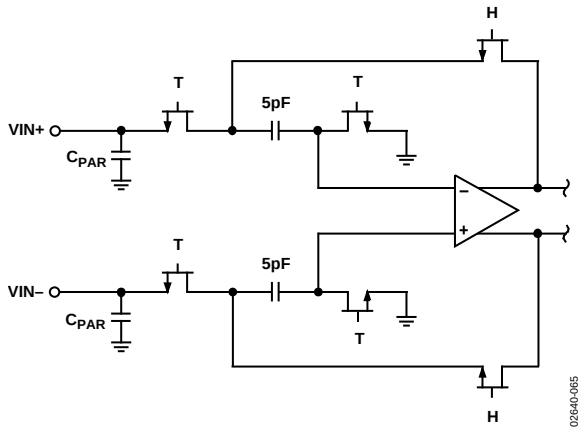


Figure 32. Switched-Capacitor Input

An internal differential reference buffer creates positive and negative reference voltages, REFT and REFB, respectively, that define the span of the ADC core. The output common mode of the reference buffer is set to midsupply, and the REFT and REFB voltages and span are defined as:

$$REFT = ½(AVDD + VREF)$$

$$REFB = ½ (AVDD - VREF)$$

$$Span = 2 \times (REFT - REFB) = 2 \times VREF$$

The equations above show that the *REFT* and *REFB* voltages are symmetrical about the midsupply voltage and, by definition, the input span is twice the value of the VREF voltage.

The internal voltage reference can be pin-strapped to fixed values of 0.5 V or 1.0 V or adjusted within the same range as discussed in the Internal Reference Connection section. Maximum SNR performance is achieved with the AD9238 set to the largest input span of 2 V p-p. The relative SNR degradation is 3 dB when changing from 2 V p-p mode to 1 V p-p mode.

The SHA may be driven from a source that keeps the signal peaks within the allowable range for the selected reference voltage. The minimum and maximum common-mode input levels are defined as:

$$VCM_{MIN} = VREF/2$$

$$VCM_{MAX} = (AVDD + VREF)/2$$

The minimum common-mode input level allows the AD9238 to accommodate ground-referenced inputs. Although optimum performance is achieved with a differential input, a single-ended source may be driven into VIN+ or VIN−. In this configuration, one input accepts the signal, while the opposite input should be set to midscale by connecting it to an appropriate reference. For example, a 2 V p-p signal may be applied to VIN+, while a 1 V reference is applied to VIN−. The AD9238 then accepts an input signal varying between 2 V and 0 V. In the single-ended configuration, distortion performance may degrade significantly as compared to the differential case. However, the effect is less noticeable at lower input frequencies and in the lower speed grade models (AD9238-40 and AD9238-20).

Differential Input Configurations

As previously detailed, optimum performance is achieved while driving the AD9238 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC. The output common-mode voltage of the AD8138 is easily set to AVDD/2, and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

At input frequencies in the second Nyquist zone and above, the performance of most amplifiers is not adequate to achieve the true performance of the AD9238. This is especially true in IF under-sampling applications where frequencies in the 70 MHz to 200 MHz range are being sampled. For these applications, differential transformer coupling is the recommended input configuration, as shown in Figure 33.

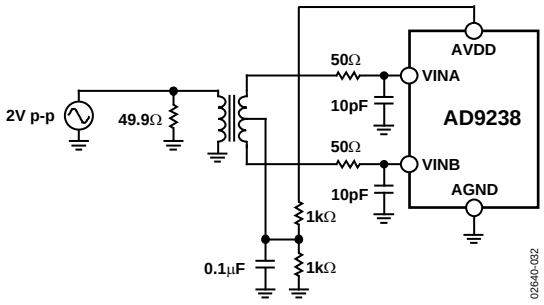


Figure 33. Differential Transformer Coupling

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

Single-Ended Input Configuration

A single-ended input may provide adequate performance in cost-sensitive applications. In this configuration, there is a degradation in SFDR and distortion performance due to the large input common-mode swing. However, if the source impedances on each input are matched, there should be little effect on SNR performance.

CLOCK INPUT AND CONSIDERATIONS

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to the clock duty cycle. Commonly, a 5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9238 provides separate clock inputs for each channel. The optimum performance is achieved with the clocks operated at the same frequency and phase. Clocking the channels asynchronously may degrade performance significantly. In some applications, it is desirable to skew the clock timing of adjacent channels. The AD9238's separate clock inputs allow for clock timing skew (typically ±1 ns) between the channels without significant performance degradation.

The AD9238 contains two clock duty cycle stabilizers, one for each converter, that retime the nonsampling edge, providing an internal clock with a nominal 50% duty cycle. When proper track-and-hold times for the converter are required to maintain high performance, maintaining a 50% duty cycle clock is particularly important in high speed applications. It may be difficult to maintain a tightly controlled duty cycle on the input clock on the PCB (see Figure 24). DCS can be enabled by tying the DCS pin high.

The duty cycle stabilizer uses a delay-locked loop to create the nonsampling edge. As a result, any changes to the sampling frequency require approximately 2 µs to 3 µs to allow the DLL to acquire and settle to the new rate.

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR at a given full-scale input frequency (f_{INPUT}) due only to aperture jitter (t_J) can be calculated as

$$SNR = 20 \times \log\left[\frac{1}{\left(2 \times \pi \times f_{INPUT} \times t_j\right)}\right]$$

In the equation, the rms aperture jitter, t_J, represents the root-sum square of all jitter sources, which includes the clock input, analog input signal, and ADC aperture jitter specification. Undersampling applications are particularly sensitive to jitter.

For optimal performance, especially in cases where aperture jitter may affect the dynamic range of the AD9238, it is important to minimize input clock jitter. The clock input circuitry should use stable references; for example, use analog power and ground planes to generate the valid high and low digital levels for the AD9238 clock input. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

POWER DISSIPATION AND STANDBY MODE

The power dissipated by the AD9238 is proportional to its sampling rates. The digital (DRVDD) power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit. The digital drive current can be calculated by

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLOCK} \times N$$

where N is the number of bits changing, and C_{LOAD} is the average load on the digital pins that changed.

The analog circuitry is optimally biased so that each speed grade provides excellent performance while affording reduced power consumption. Each speed grade dissipates a baseline power at low sample rates that increases with clock frequency.

Either channel of the AD9238 can be placed into standby mode independently by asserting the PDWN_A or PDWN_B pins.

It is recommended that the input clock(s) and analog input(s) remain static during either independent or total standby, which results in a typical power consumption of 1 mW for the ADC. Note that if DCS is enabled, it is mandatory to disable the clock of an independently powered-down channel. Otherwise, significant distortion results on the active channel. If the clock inputs remain active while in total standby mode, typical power dissipation of 12 mW results.

The minimum standby power is achieved when both channels are placed into full power-down mode (PDWN_A = PDWN_B = HI). Under this condition, the internal references are powered down. When either or both of the channel paths are enabled after a power-down, the wake-up time is directly related to the recharging of the REFT and REFB decoupling capacitors and to the duration of the power-down. Typically, it takes approximately 5 ms to restore full operation with fully discharged 0.1 µF and 10 µF decoupling capacitors on REFT and REFB.

A single channel can be powered down for moderate power savings. The powered-down channel shuts down internal circuits, but both the reference buffers and shared reference remain powered on. Because the buffer and voltage reference remain powered on, the wake-up time is reduced to several clock cycles.

DIGITAL OUTPUTS

The AD9238 output drivers can be configured to interface with 2.5 V or 3.3 V logic families by matching DRVDD to the digital supply of the interfaced logic. The output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance. Applications requiring the ADC to drive large capacitive loads or large fanouts may require external buffers or latches.

The data format can be selected for either offset binary or twos complement. See the Data Format section for more information.

TIMING

The AD9238 provides latched data outputs with a pipeline delay of seven clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal. Refer to Figure 2 for a detailed timing diagram.

The internal duty cycle stabilizer can be enabled on the AD9238 using the DCS pin. This provides a stable 50% duty cycle to internal circuits.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9238. These transients can detract from the converter's dynamic performance. The lowest typical conversion rate of the AD9238 is 1 MSPS. At clock rates below 1 MSPS, dynamic performance may degrade.

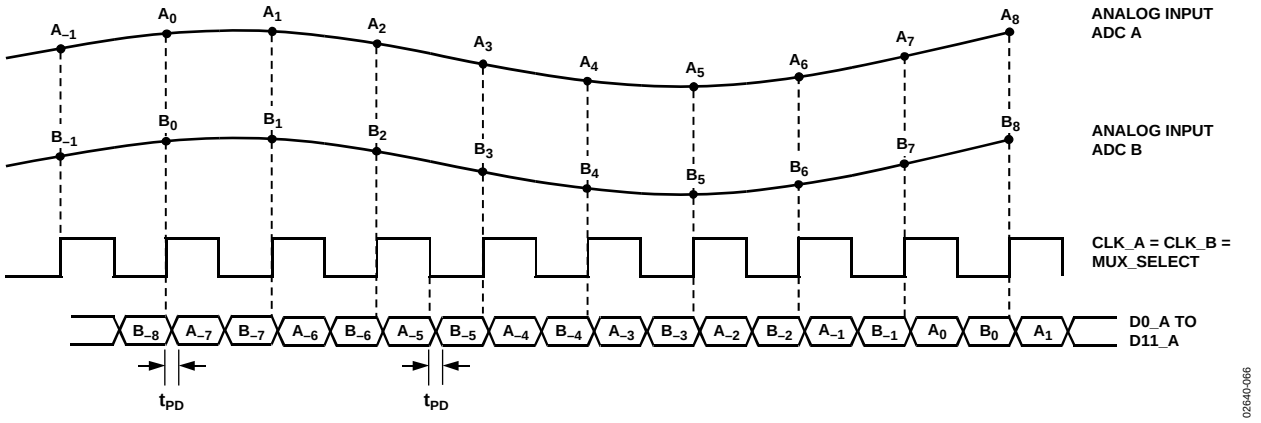


Figure 34. Multiplexed Data Format Using the Channel A Output and the Same Clock Tied to CLK_A, CLK_B, and MUX_SELECT

DATA FORMAT

The AD9238 data output format can be configured for either twos complement or offset binary. This is controlled by the data format select pin (DFS). Connecting DFS to AGND produces offset binary output data. Conversely, connecting DFS to AVDD formats the output data as twos complement.

The output data from the dual ADCs can be multiplexed onto a single 12-bit output bus. The multiplexing is accomplished by toggling the MUX_SELECT bit, which directs channel data to the same or opposite channel data port. When MUX_SELECT is logic high, the Channel A data is directed to the Channel A output bus, and the Channel B data is directed to the Channel B output bus. When MUX_SELECT is logic low, the channel data is reversed, that is the Channel A data is directed to the Channel B output bus, and the Channel B data is directed to the Channel A output bus. By toggling the MUX_SELECT bit, multiplexed data is available on either of the output data ports.

If the ADCs run with synchronized timing, this same clock can be applied to the MUX_SELECT pin. Any skew between CLK_A, CLK_B, and MUX_SELECT can degrade ac performance. It is recommended to keep the clock skew <100 pS. After the MUX_SELECT rising edge, either data port has the data for its respective channel; after the falling edge, the alternate channel's data is placed on the bus. Typically, the other unused bus would be disabled by setting the appropriate OEB high to reduce power consumption and noise. Figure 34 shows an example of multiplex mode. When multiplexing data, the data rate is two times the sample rate. Note that both channels must remain active in this mode and that each channel's power-down pin must remain low.

VOLTAGE REFERENCE

A stable and accurate 0.5 V voltage reference is built into the AD9238. The input range can be adjusted by varying the reference voltage applied to the AD9238, using either the internal reference with different external resistor configurations or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. If the ADC is being driven differentially through a transformer, the reference voltage can be used to bias the center tap (common-mode voltage).

The shared reference mode allows the user to connect the references from the dual ADCs together externally for superior gain and offset matching performance. If the ADCs are to function independently, the reference decoupling can be treated independently and can provide superior isolation between the dual channels. To enable shared reference mode, the SHARED_REF pin must be tied high and the external differential references must be externally shorted. (REFT_A must be externally shorted to REFT_B, and REFB_A must be shorted to REFB_B.)

Internal Reference Connection

A comparator within the AD9238 detects the potential at the SENSE pin and configures the reference into four possible states, which are summarized in Table 7. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 35), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected, as shown in Figure 36, the switch is again set to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times (1 + R2/R1)$$

In all reference configurations, REFT and REFB drive the ADC core and establish its input span. The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

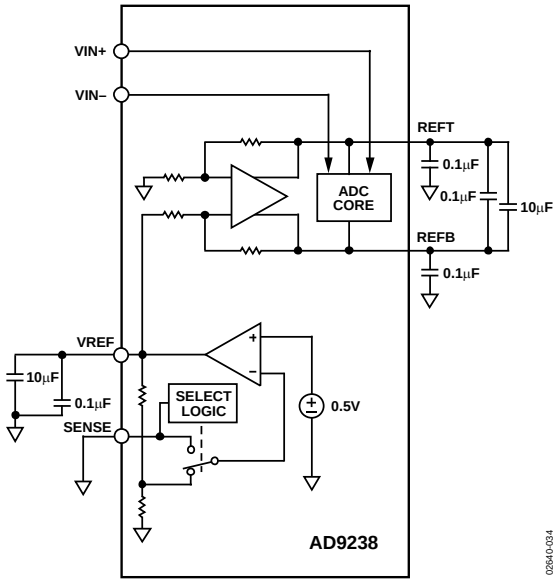


Figure 35. Internal Reference Configuration

Table 7. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	0.5 × (1 + R2/R1)	2 × VREF (See Figure 36)
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or to improve thermal drift characteristics. When multiple ADCs track one another, a single reference (internal or external) may be necessary to reduce gain matching errors to an acceptable level. A high precision external reference may also be selected to provide lower gain and offset temperature drift. Figure 37 shows the typical drift characteristics of the internal reference in both 1 V and 0.5 V modes. When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 7 kΩ load. The internal buffer still generates the positive and negative full-scale references, REFT and REFB, for the ADC core. The input span is always twice the value of the reference voltage; therefore, the external reference must be limited to a maximum of 1 V. If the internal reference of the AD9238 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 38 depicts how the internal reference voltage is affected by loading.

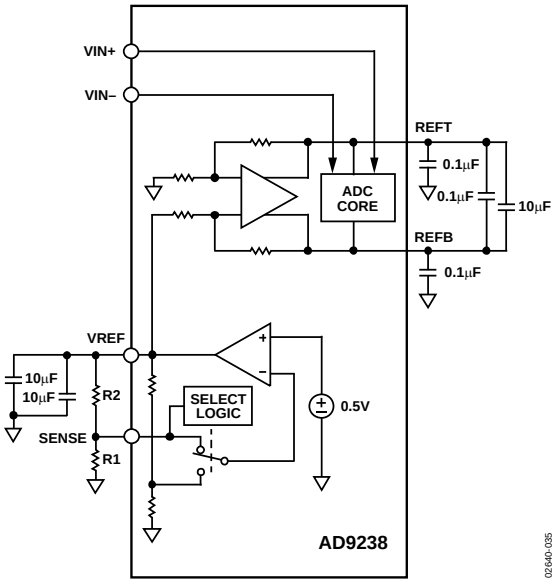


Figure 36. Programmable Reference Configuration

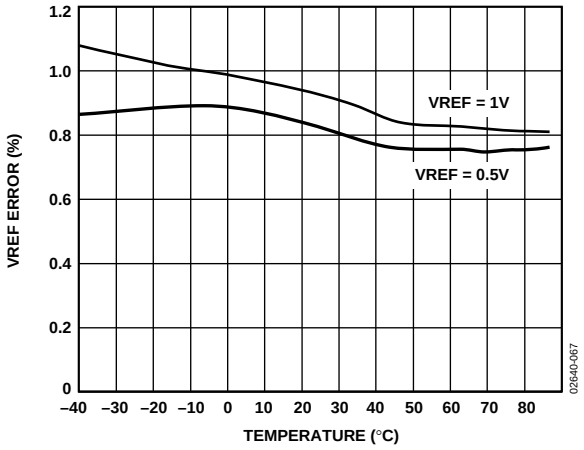


Figure 37. Typical VREF Drift

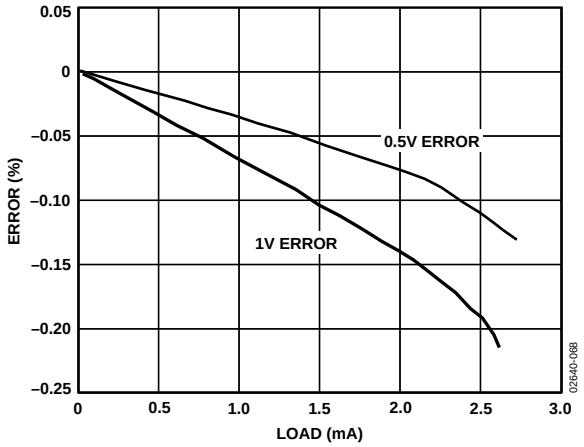


Figure 38. VREF Accuracy vs. Load

AD9238 LQFP EVALUATION BOARD

The evaluation board supports both the AD9238 and AD9248 and has five main sections: clock circuitry, inputs, reference circuitry, digital control logic, and outputs. A description of each section follows. Table 8 shows the jumper settings and notes assumptions in the comment column.

Four supply connections to TB1 are necessary for the evaluation board: the analog supply of the DUT, the on-board analog circuitry supply, the digital driver DUT supply, and the on-board digital circuitry supply. Separate analog and digital supplies are recommended, and on each supply 3 V is nominal. Each supply is decoupled on-board, and each IC, including the DUT, is decoupled locally. All grounds should be tied together.

CLOCK CIRCUITRY

The clock circuitry is designed for a low jitter sine wave source to be ac-coupled and level shifted before driving the 74VHC04 hex inverter chips (U8 and U9) whose output provides the clock to the part. The POT (R32 and R31) on the level shifting circuitry allows the user to vary the duty cycle if desired. The amplitude of the sine wave must be large enough for the trip points of the hex inverter and within the supplies to avoid noise from clipping. To ensure a 50% duty cycle internal to the part, the AD9238-65 has an on-chip duty cycle stabilizer circuit that is enabled by putting in Jumper JP11. The duty cycle stabilizer circuitry should only be used at clock rates above 40 MSPS.

Each channel has its own clock circuitry, but normally both clock pins are driven by a single 74VHC04, and the solder Jumper JP24 is used to tie the clock pins together. When the clock pins are tied together and only one 74VHC04 is being used, the series termination resistor for the other channel must be removed (either R54 or R55, depending on which inverter is being used).

A data capture clock for each channel is created and sent to the output buffers in order to be used in the data capture system if needed. Jumpers JP25 and JP26 are used to invert the data clock if necessary and can be used to debug data capture timing problems.

ANALOG INPUTS

The AD9238 achieves the best performance with a differential input. The evaluation board has two input options for each channel, a transformer (XFMR) and an AD8138, both of which perform single-ended-to-differential conversions. The XFMR allows for the best high frequency performance, and the AD8138 is ideal for dc evaluation, low frequency inputs, and driving an ADC differentially without loading the single-ended signal.

The common-mode level for both input options is set to midsupply by a resistor divider off the AVDD supply but can also be overdriven with an external supply using the (test points) TP12, TP13 for the AD8138s and TP14, TP15 for the XFMRs. For low distortion of full-scale input signals when using an AD8138, put JP17 and JP22 in Position B and put an external negative supply on TP10 and TP11.

For best performance, use low jitter input sources and a high performance band-pass filter after the signal source, before the evaluation board (see Figure 39). For XFMR inputs, use solder Jumpers JP13, JP14 for Channel A and JP20, JP21 for Channel B. For AD8138 inputs, use solder Jumpers JP15, JP16 for Channel A and JP18, JP19 for Channel B. Remove all solder from the jumpers not being used.

REFERENCE CIRCUITRY

The evaluation board circuitry allows the user to select a reference mode through a series of jumpers and provides an external reference if necessary. Refer to Table 9 to find the jumper settings for each reference mode. The external reference on the board is a simple resistor divider/zener diode circuit buffered by an AD822 (U4). The POT (R4) can be used to change the level of the external reference to fine adjust the ADC full scale.

DIGITAL CONTROL LOGIC

The digital control logic on the evaluation board is a series of jumpers and pull-down resistors used as digital inputs for the following pins on the AD9238: the power-down and output enable bar for each channel, the duty cycle restore circuitry, the twos complement output mode, the shared reference mode, and the MUX_SELECT pin. Refer to Table 8 for normal operating jumper positions.

OUTPUTS

The outputs of the AD9238 (and the data clock discussed earlier) are buffered by 74VHC541s (U2, U3, U7, U10) to ensure the correct load on the outputs of the DUT, as well as the extra drive capability to the next part of the system. The 74VHC541s are latches, but on this evaluation board, they are wired and function as buffers. JP30 can be used to tie the data clocks together if desired. If the data clocks are tied, R39 or R40 must be removed, depending on which clock circuitry is being used.

Table 8. PCB Jumpers

JP	Description	Normal Setting	Comment
1	Reference	Out	1 V Reference Mode
2	Reference	In	1 V Reference Mode
3	Reference	Out	1 V Reference Mode
4	Reference	Out	1 V Reference Mode
5	Reference	Out	1 V Reference Mode
6	Shared Reference	Out	
7	Shared Reference	Out	
8	PDWN B	Out	
9	PDWN A	Out	
10	Shared Reference	Out	
11	Duty Cycle	In	Duty Cycle Restore On
12	Twos Complement	Out	
13	Input	In	Using XFMR Input
14	Input	In	Using XFMR Input
15	Input	Out	Using XFMR Input
16	Input	Out	Using XFMR Input
17	AD8138 Supply	A	Using XFMR Input
18	Input	Out	Using XFMR Input
19	Input	Out	
20	Input	In	
21	Input	In	
22	AD8138 Supply	A	
23	Mux Select	Out	
24	Tie Clocks	In	Using One Signal for Clock
25	Data Clock	A	
26	Data Clock	Out	Using One Signal for Clock
27	Mux Select	In	
28	OEB_A	Out	
29	Mux Select	Out	
30	Data Clock	Out	
35	OEB_B	Out	

Table 9. Reference Jumpers

Reference Mode	JP1	JP2	JP3	JP4	JP5
1 V Internal	Out	In	Out	Out	Out
0.5 V Internal	Out	Out	In	Out	Out
External	In	Out	Out	Out	In

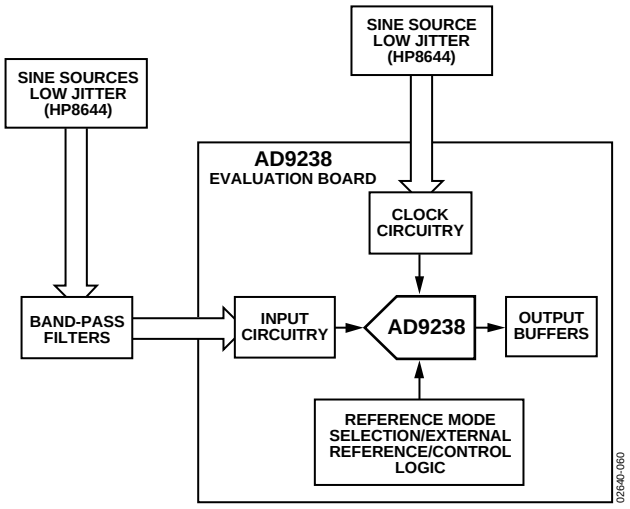


Figure 39. PCB Test Setup

LQFP EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 10.

No.	Quantity	Reference Designator	Device	Package	Value
1	18	C1, C2, C11, C12, C27, C28, C33, C34, C50, C51, C73 to C76, C87 to C90	Capacitors	ACASE	10 µF
2	23	C3 to C10, C29 to C31, C56, C61 to C65, C77, C79, C80, C84 to C86	Capacitors	0805	0.1 µF
3	7	C13, C15, C18, C19, C21, C23, C25	Capacitors	0603	0.001 µF
4	15	C6, C14, C16, C17, C20, C22, C24, C26, C32, C35 to C40	Capacitors	0603	0.1 µF
5	4	C41 to C44	Capacitors	DCASE	22 µF
6	4	C45 to C48	Capacitors	1206	0.1 µF
7	2	C49, C53	Capacitors	ACASE	6.3 V
8	2	C52, C57	Capacitors	0201	0.01 µF
9	4	C54, C55, C68, C69	Capacitors	0805	
10	4	C58, C59, C70, C71	Capacitors	0603	DNP
11	2	C60, C72	Capacitors	0603	20 pF
12	1	D1	AD1580	SOT-23CAN	1.2 V
13	1	J1			SAM080UPM
14	14	JP1 to JP5, JP8 to JP12, JP23, JP28, JP29, JP35		JPRBLK02	
15	13	JP6, JP7, JP13, JP14 to JP16, JP18 to JP21, JP24, JP27, JP30		JPRSLD02	
16	4	JP17, JP22, JP25, JP26		JPRBLK03	
17	4	L1 to L4	IND1210	LC1210	10 µH
18	6	R1, R2, R13, R14, R23, R27	Resistors	1206	33 Ω
19	1	R3	Resistor	1206	5.49 kΩ
20	1	R4	Resistor	RV3299UP	10 kΩ
21	7	R5, R6, R38, R41, R43, R44, R51	Resistors	0805	5 kΩ
22	6	R7, R8, R19, R20, R52, R53	Resistors	1206	49.9 Ω
23	8	R9, R18, R29, R30, R47 to R50	Resistors	0805	1 kΩ
24	6	R10, R12, R15, R24, R25, R28	Resistors	1206	499 Ω
25	2	R11, R26	Resistors	1206	523 Ω
26	4	R16, R17, R21, R22	Resistors	1206	40 Ω
27	2	R31, R32	Resistors	RV3299W	10 kΩ
28	4	R33 to R35, R42	Resistors	0805	500 Ω
29	2	R36, R37	Resistors	1206	10 kΩ
30	2	R39, R40	Resistors	0805	22 Ω
31	2	R54, R55	Resistors	1206	0 Ω
32	16	RP1 to RP16	Resistor Pack	RCA74204	22 Ω
33	6	S1 to S6		SMA200UP	
34	2	T1, T2		DIP06RCUP	T1-1T
35	1	TB1			TBLK06REM
36	4	TP1, TP3, TP5, TP7		LOOPTP	RED
37	4	TP2, TP4, TP6, TP8		LOOPTP	BLK
38	7	TP9, TP12 to TP17		LOOPMINI	WHT
39	2	TP10, TP11		LOOPMINI	RED
40	1	U1		64LQFP7X7	AD9238
41	4	U2, U3, U7, U10		SOL20	74VHC541
42	1	U4		SOIC-8	AD822
43	2	U5, U6		SO8NC7	AD8138
44	2	U8, U9		TSSOP-14	74VHC04

LQFP EVALUATION BOARD SCHEMATICS

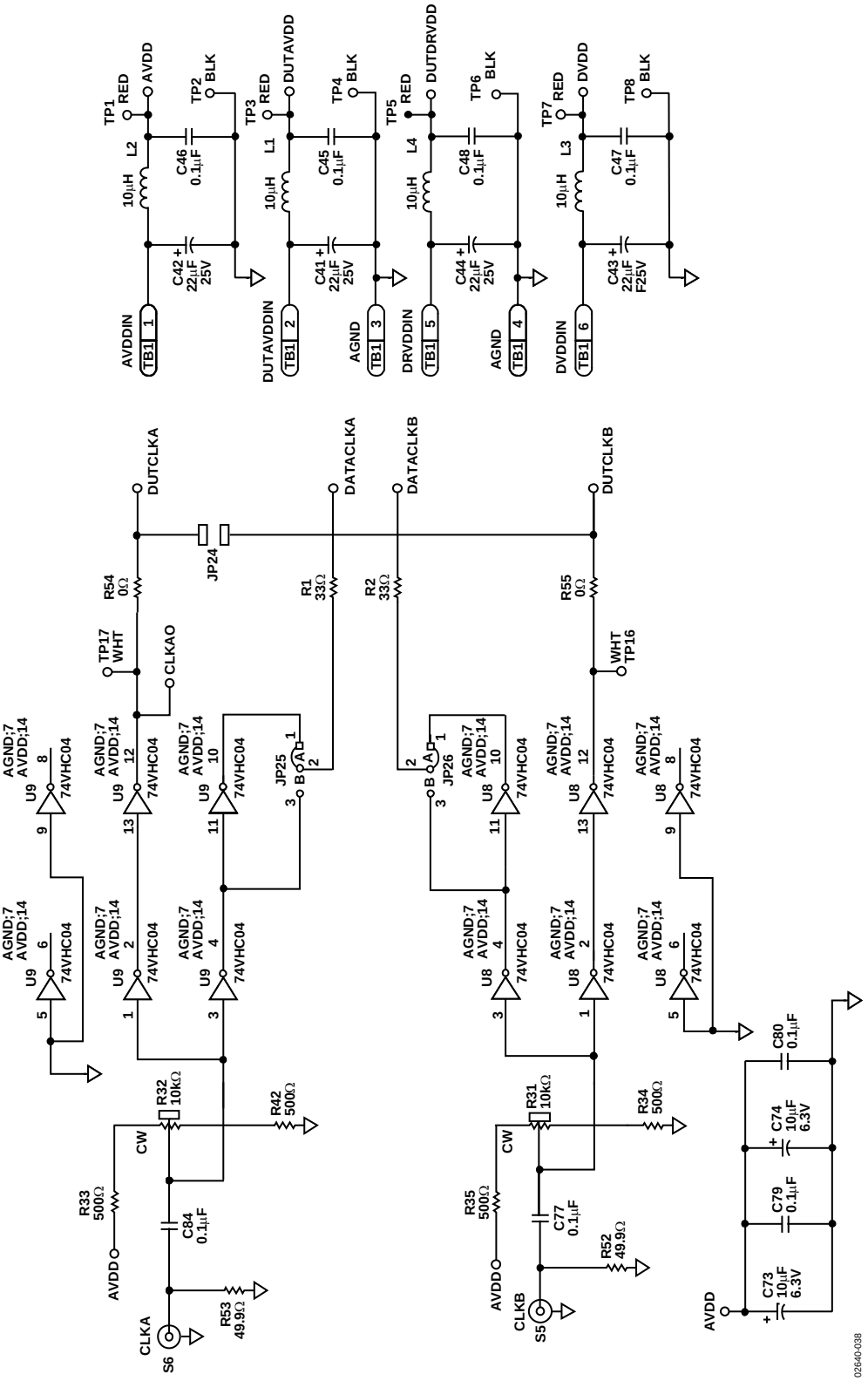


Figure 40. Evaluation Board Schematic

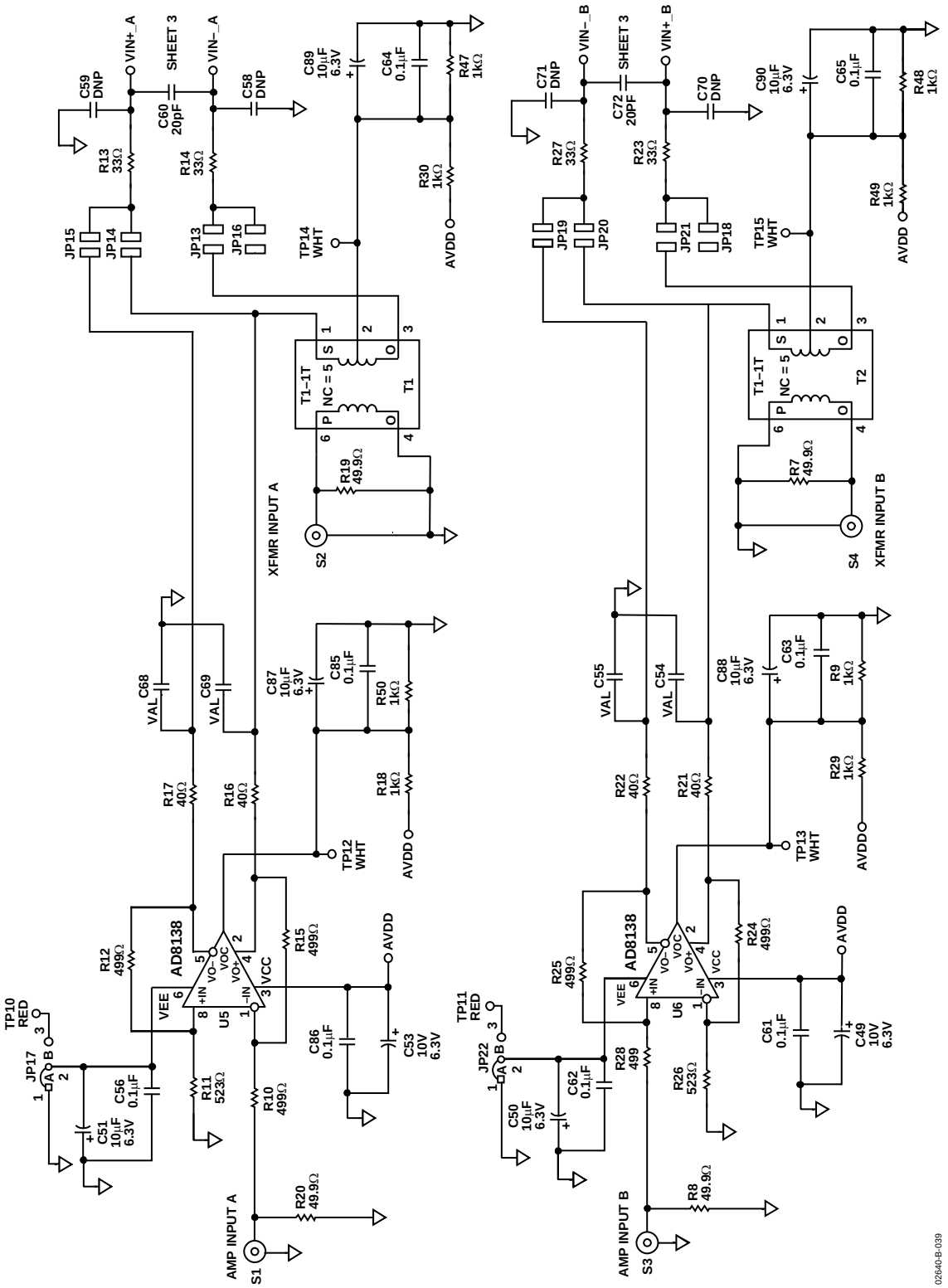


Figure 41. Evaluation Board Schematic (Continued)

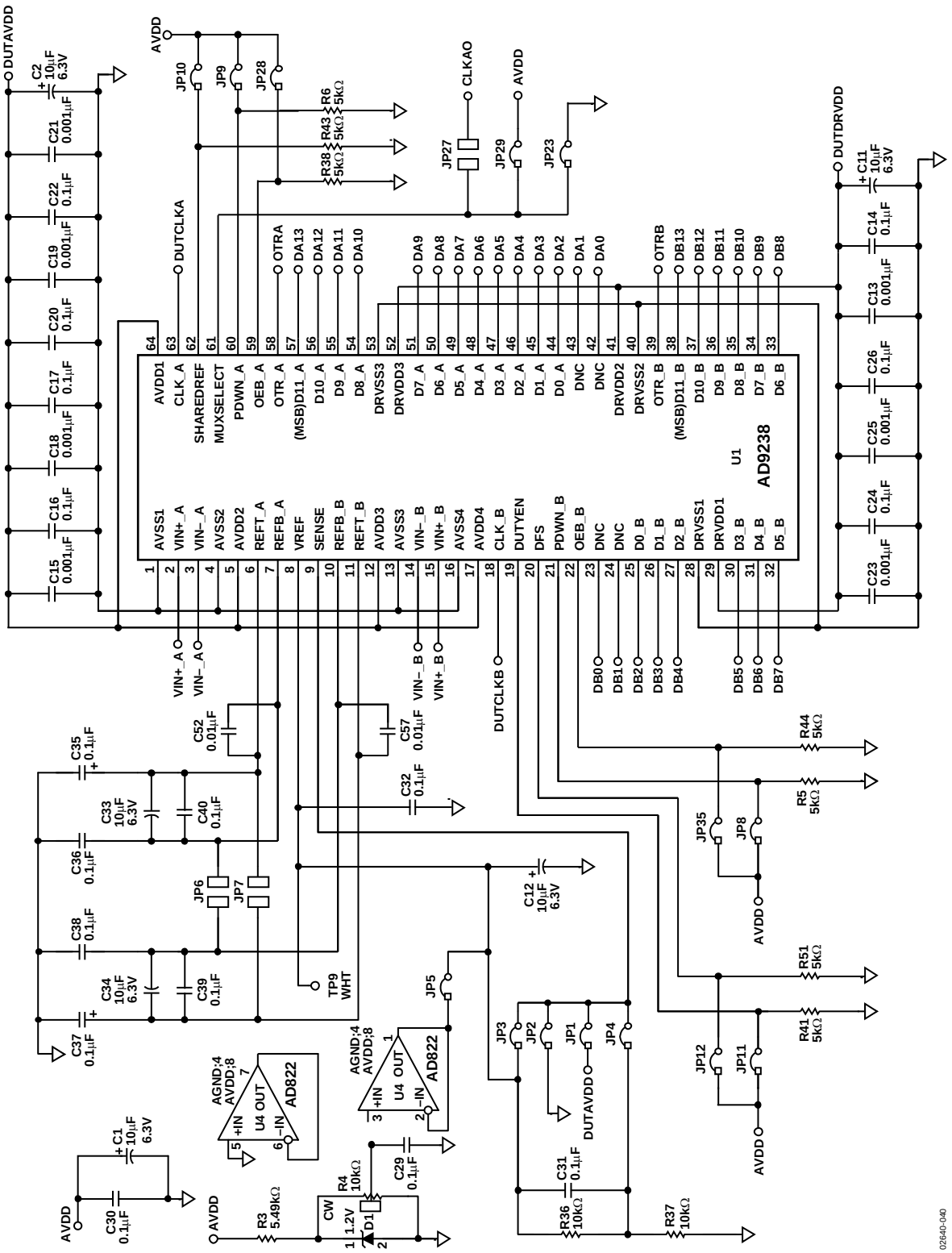


Figure 42. Evaluation Board Schematic (Continued)

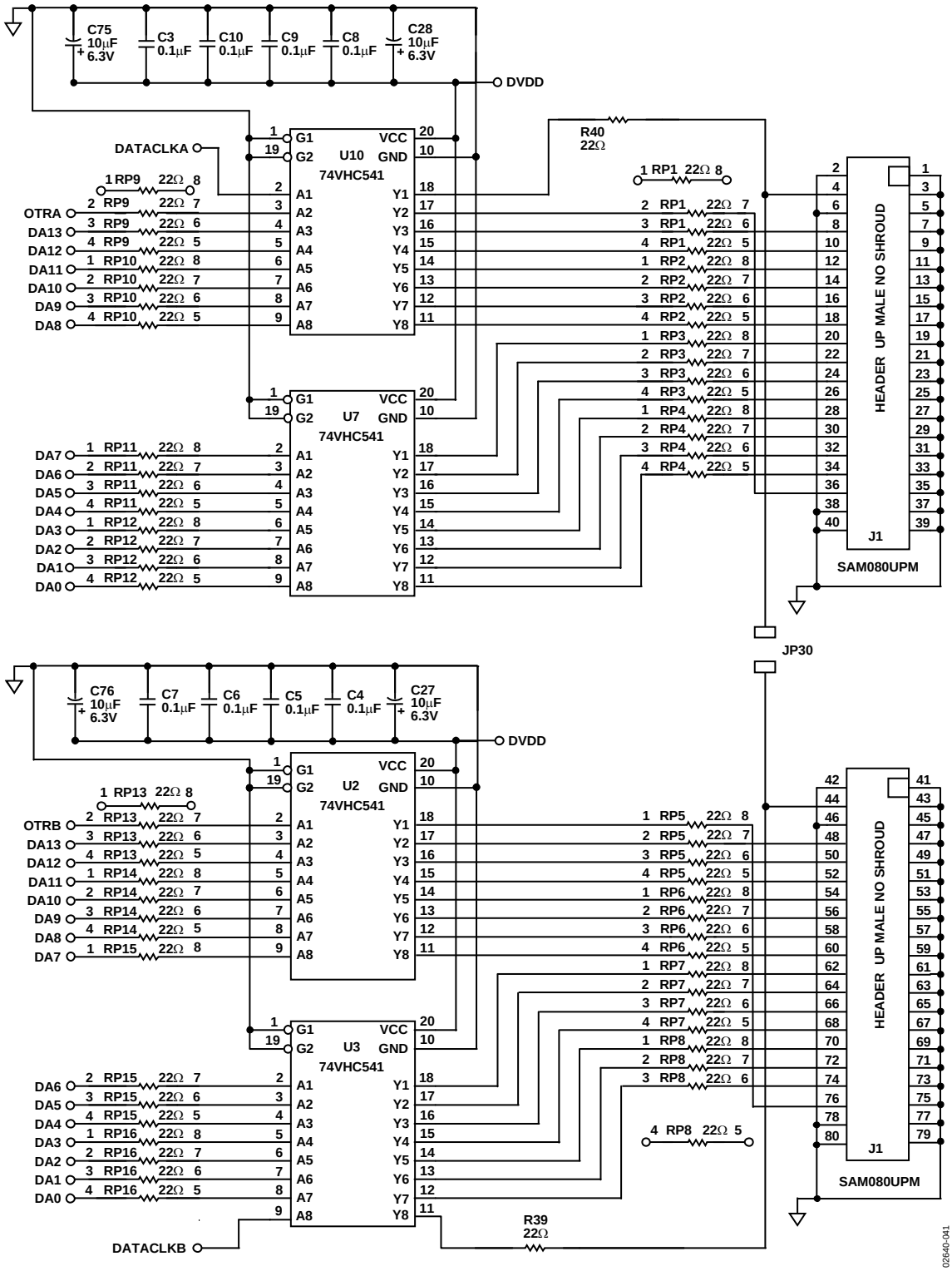


Figure 43. Evaluation Board Schematic (Continued)

LQFP PCB LAYERS

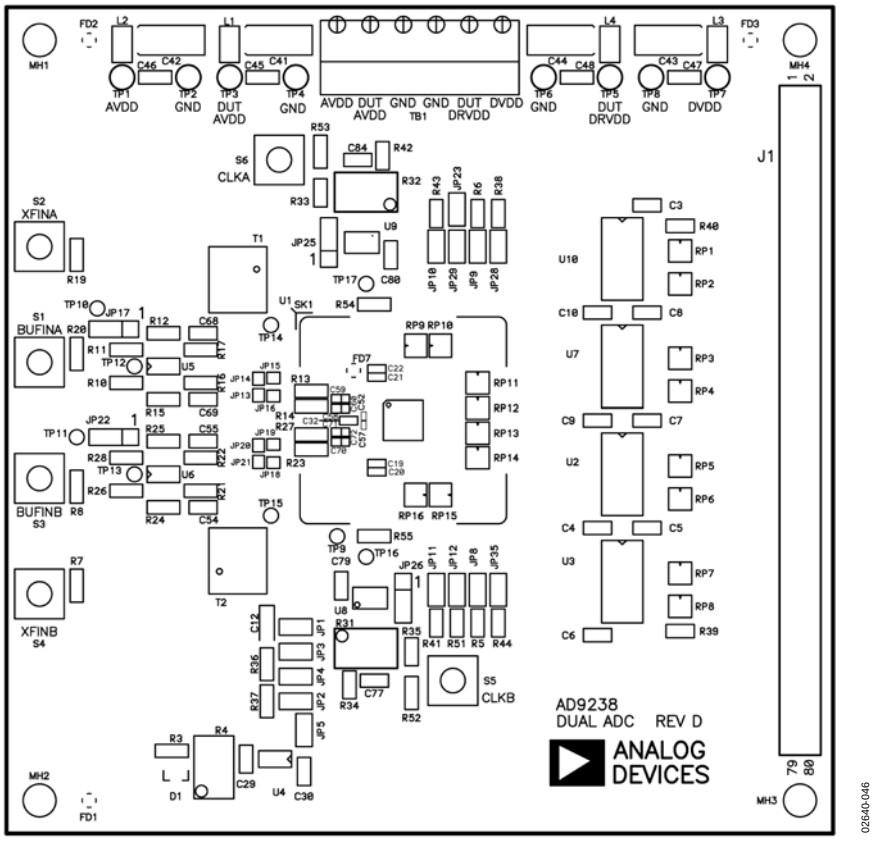


Figure 44. PCB Top Side Silkscreen

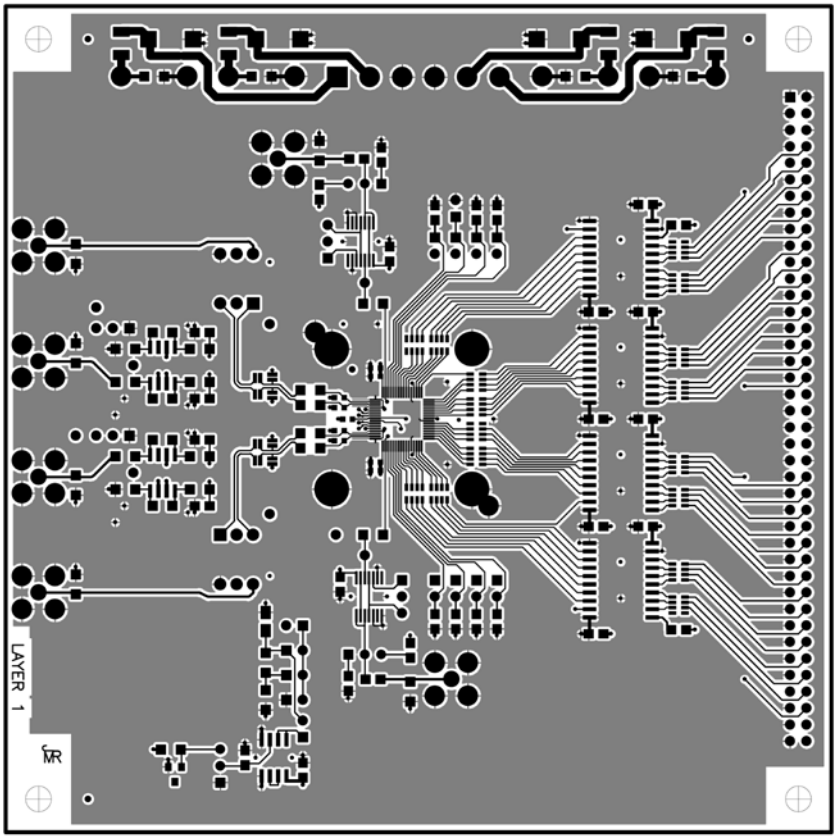


Figure 45. PCB Top Layer

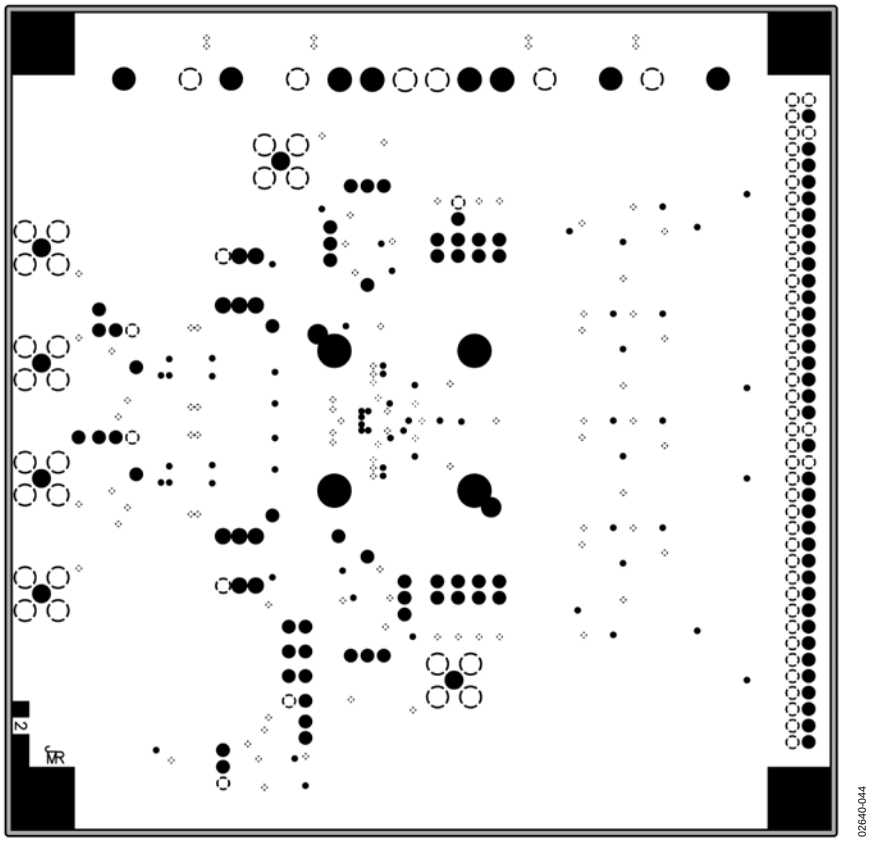


Figure 46. PCB Ground Plane

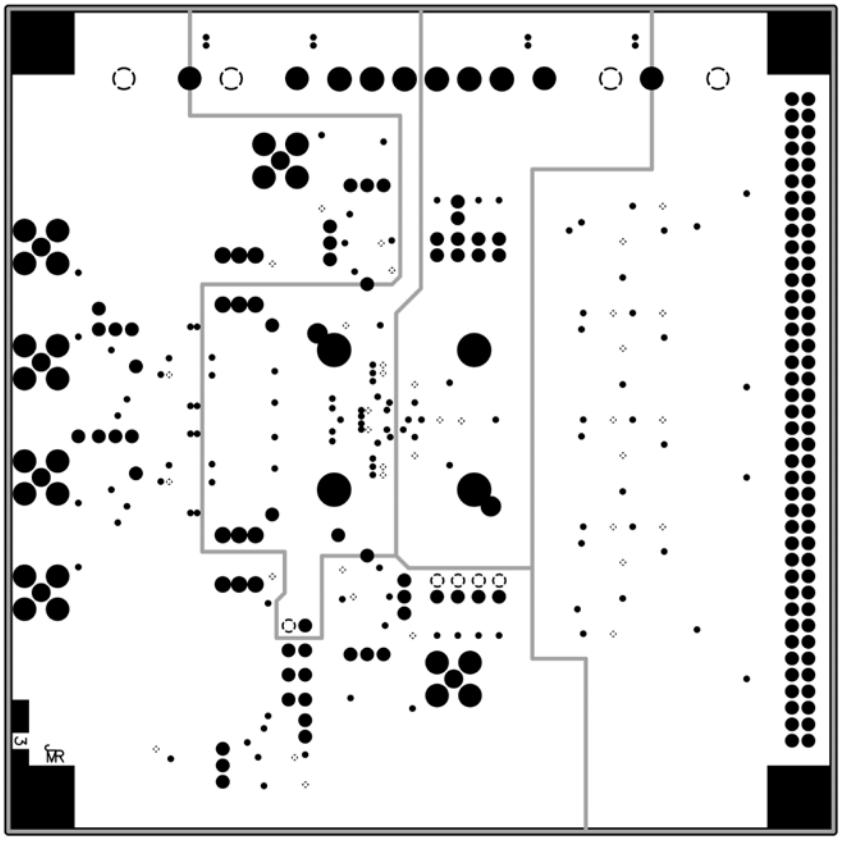


Figure 47. PCB Split Power Plane

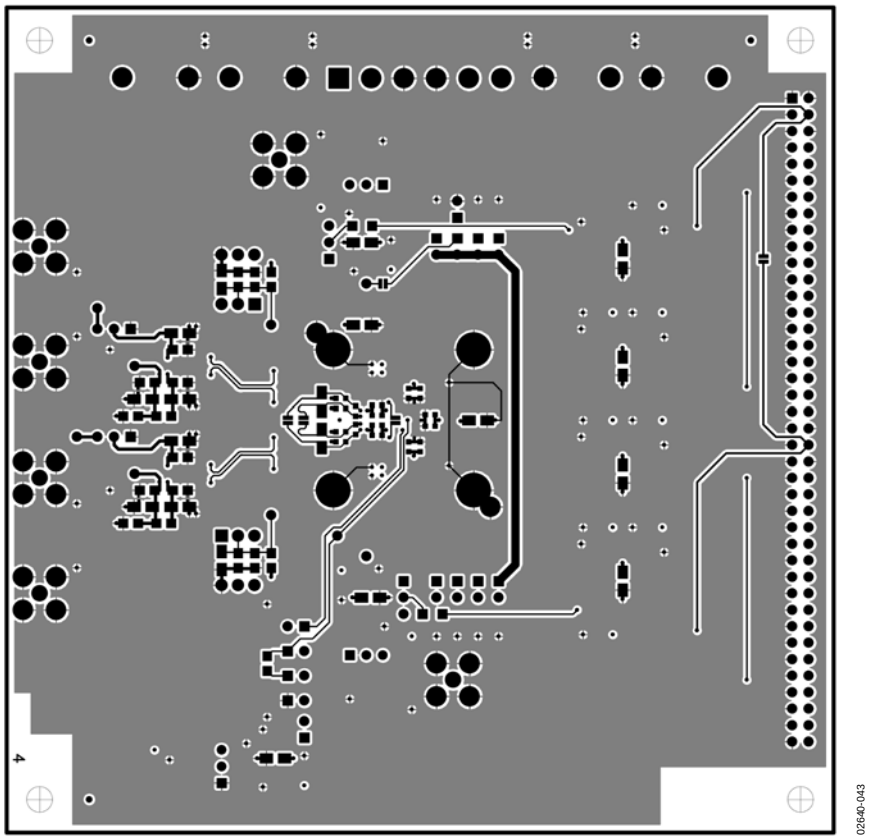


Figure 48. PCB Bottom Layer

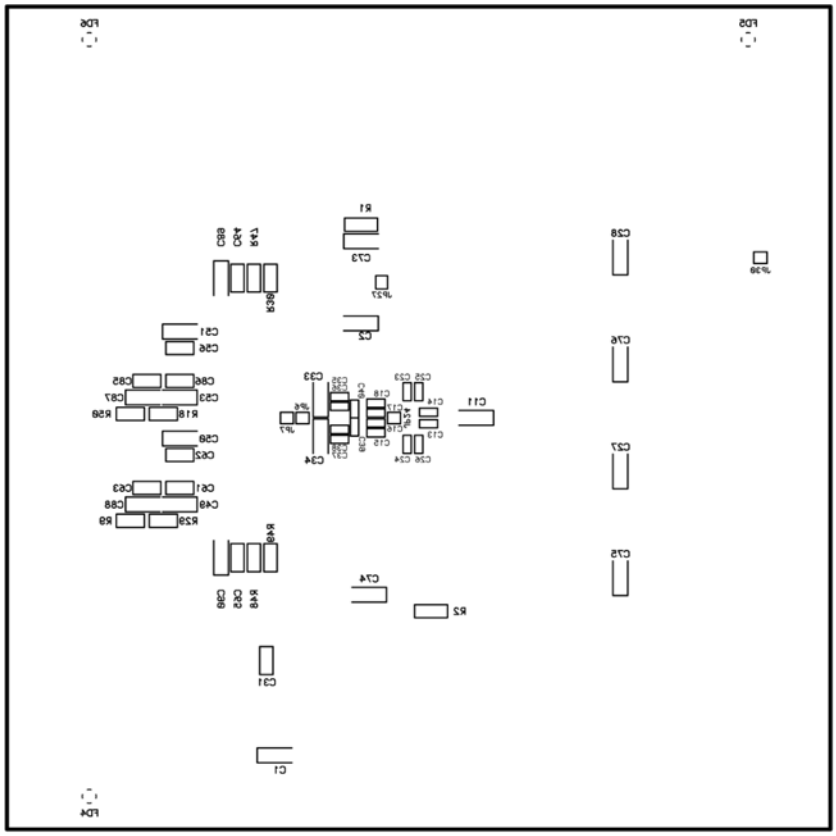


Figure 49. PCB Bottom Silkscreen

DUAL ADC LFCSP PCB

The LFCSP PCB requires a low jitter clock source, analog sources, and power supplies. The PCB interfaces directly with Analog Devices standard dual-channel data capture board (HSC-ADC-EVAL-DC), which together with ADI's ADC Analyzer™ software allows for quick ADC evaluation.

POWER CONNECTOR

Power is supplied to the board via three detachable 4-lead power strips.

Table 11. Power Connector

Terminal	Comments
VCC[1] 3.0 V	Analog supply for ADC
VDD[1] 3.0 V	Output supply for ADC
VDL[1] 3.0 V	Supply circuitry
VREF	Optional external VREF
+5 V	Optional op amp supply
−5 V	Optional op amp supply

[1]VCC, VDD, and VDL are the minimum required power connections.

ANALOG INPUTS

The evaluation board accepts a 2 V p-p analog input signal centered at ground at two SMB connectors, Input A and Input B. These signals are terminated at their respective transformer primary side. T1 and T2 are wideband RF transformers that provide the single-ended-to-differential conversion, allowing the ADC to be driven differentially, minimizing even-order harmonics. The analog signals can be low-pass filtered at the transformer secondary to reduce high frequency aliasing.

OPTIONAL OPERATIONAL AMPLIFIER

The PCB has been designed to accommodate an optional AD8139 op amp that can serve as a convenient solution for dc-coupled applications. To use the AD8139 op amp, remove C14, R4, R5, C13, R37, and R36. Place R22, R23, R30, and R24.

CLOCK

The clock inputs are buffered on the board at U5 and U6. These gates provide buffered clocks to the on-board latches, U2 and U4, ADC input clocks, and DRA and DRB that are available at the output Connector P3, P8. The clocks can be inverted at the timing jumpers labeled with the respective clocks. The clock paths also provide for various termination options. The ADC input clocks can be set to bypass the buffers at P2 to P9 and P10, P12. An optional clock buffer U3, U7 can also be placed. The clock inputs can be bridged at TIEA, TIEB (R20, R40) to allow one to clock both channels from one clock source; however, optimal performance is obtained by driving J2 and J3.

Table 12. Jumpers

Terminal	Comments
OEB A	Output Enable for A Side
PDWN A	Power-Down A
MUX	Mux Input
SHARED REF	Shared Reference Input
DR A	Invert DR A
LATA	Invert A Latch Clock
ENC A	Invert Encode A
OEB B	Output Enable for B Side
PDWN B	Power-Down B
DFS	Data Format Select
SHARED REF	Shared Reference Input
DR B	Invert DR B
LATB	Invert B Latch Clock
ENC B	Invert Encode B

VOLTAGE REFERENCE

The ADC SENSE pin is brought out to E41, and the internal reference mode is selected by placing a jumper from E41 to ground (E27). External reference mode is selected by placing a jumper from E41 to E25 and E30 to E2. R56 and R45 allow for programmable reference mode selection.

DATA OUTPUTS

The ADC outputs are latched on the PCB at U2 and U4. The ADC outputs have the recommended series resistors in line to limit switching transient effects on ADC performance.

LFCSP EVALUATION BOARD BILL OF MATERIALS (BOM)

Table 13.

No.	Quantity	Reference Designator	Device	Package	Value
1	2	C1, C3	Capacitors	0201	20 pF
2	7	C2, C5, C7, C9, C10, C22, C36	Capacitors	0805	10 µF
3	44	C4, C6, C8, C11 to C15, C20, C21, C24 to C27, C29 to C35, C39 to C61	Capacitors	0402	0.1 µF
4	6	C16 to C19, C37, C38	Capacitors	TAJD	10 µF
5	2	C23, C28	Capacitors	0201	0.1 µF
6	6	J1 to J6	SMBs		
7	3	P1, P4, P11	Power Connector Posts	Z5.531.3425.0	Wieland
8	3	P1, P4, P11	Detachable Connectors	25.602.5453.0	Wieland
9	2	P3[1], P8	Connectors		
10	4	R1, R2, R32, R34	Resistors	0402	36 Ω
11	6	R3, R7, R11, R14, R51, R61	Resistors	0402	50 Ω
12	4	R4, R5, R36, R37	Resistors	0402	33 Ω
13	9	R9, R10, R12, R13, R20, R35, R38, R40, R43	Resistors	0402	0 Ω
14	6	R15, R16, R18, R26, R29, R31	Resistors	0402	499 Ω
15	2	R17, R25	Resistors	0402	525 Ω
16	27	R19, R21, R27, R28, R39, R41, R44, R46 to R49, R52, R54, R55, R57 to R60, R62 to R70	Resistors	0402	1 kΩ
17	4	R22 to R24, R30	Resistors	0402	40 Ω
18	2	R45, R56	Resistors	0402	10 kΩ
19	1	R50	Resistor	0402	22 Ω
20	8	RZ1 to RZ6, RZ9, RZ10	Resistor Pack		220 Ω
21	2	T1, T2	Transformers	AWT-1WT	Mini-Circuits®
22	1	U1	AD9238	LFCSP-64	
23	2	U2, U4	SN74LVCH16373A	TSSOP-48	
24	2	U3[2], U7	SN74LVC1G04	SOT-70	
25	2	U5, U6	SN74VCX86	SO-14	
26	2	U11, U12	AD8139	SO-8/EP	
27	4	R6, R8, R33, R42	Resistors	0402	100 Ω

[1] P3 and P8 implemented as one 80-pin connector SAMTEC TSW-140-08-L-D-RA.
[2] U3 and U7 not placed.

LFCSP PCB SCHEMATICS

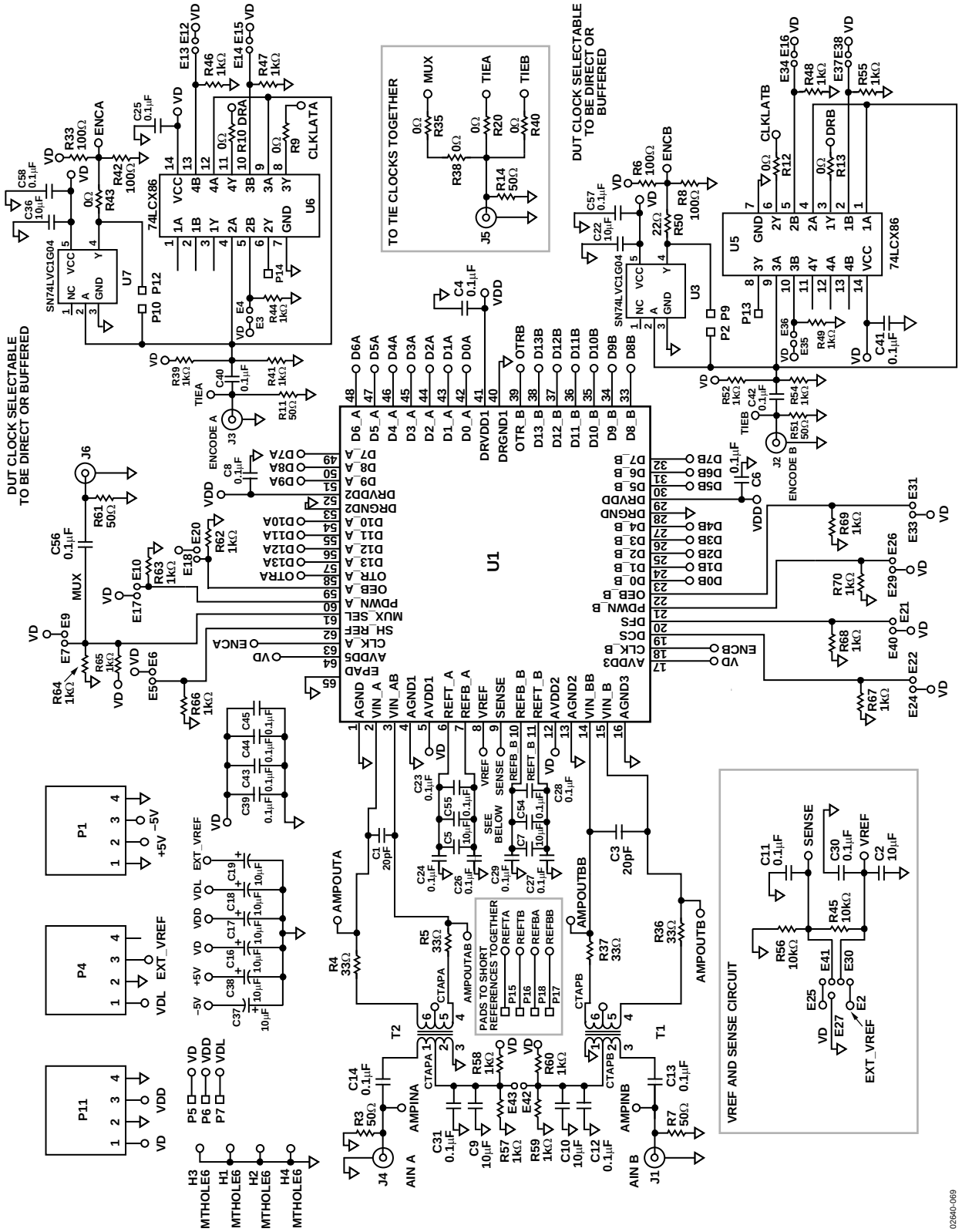


Figure 50. PCB Schematic (1 of 3)

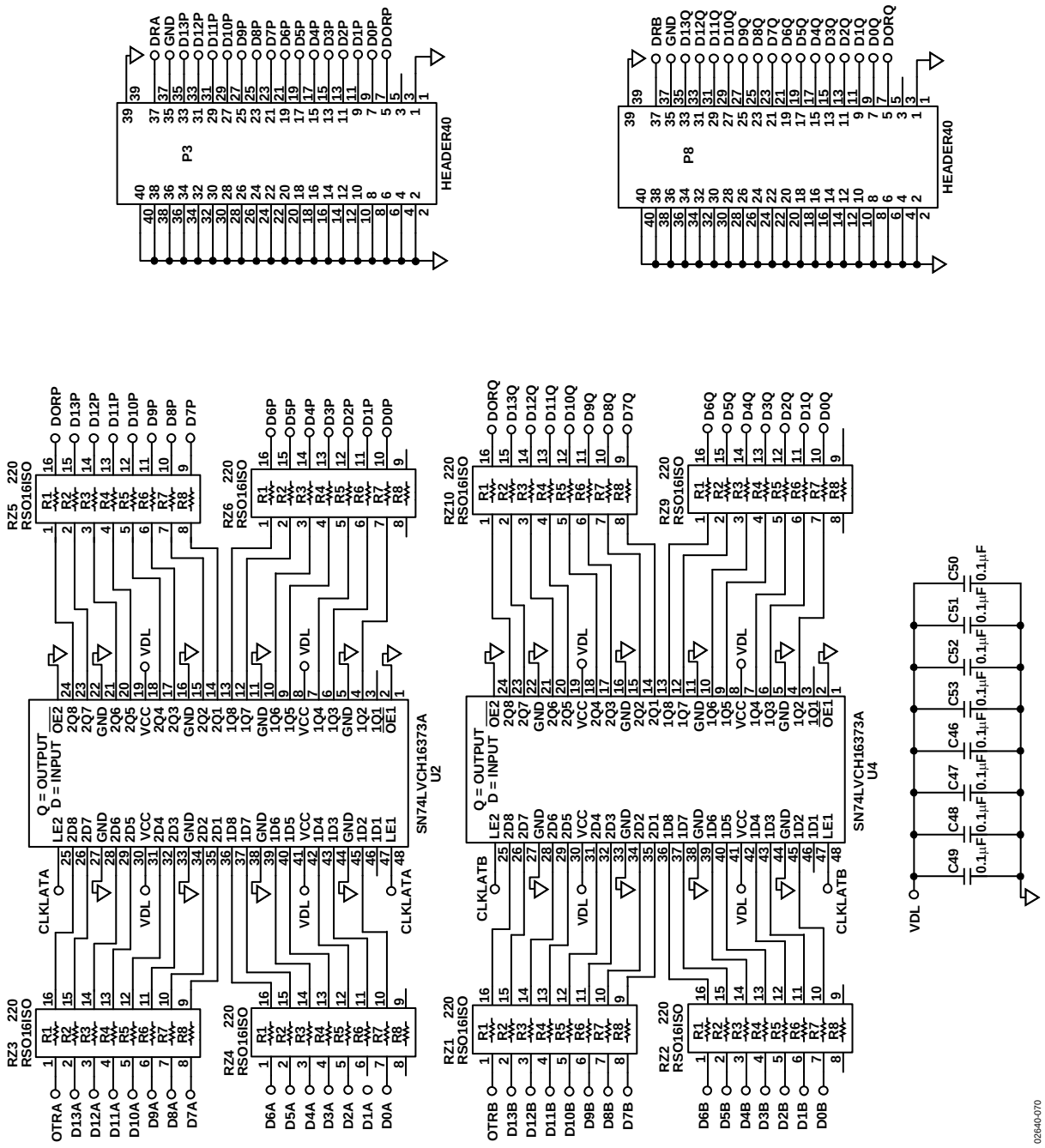


Figure 51. PCB Schematic (2 of 3)

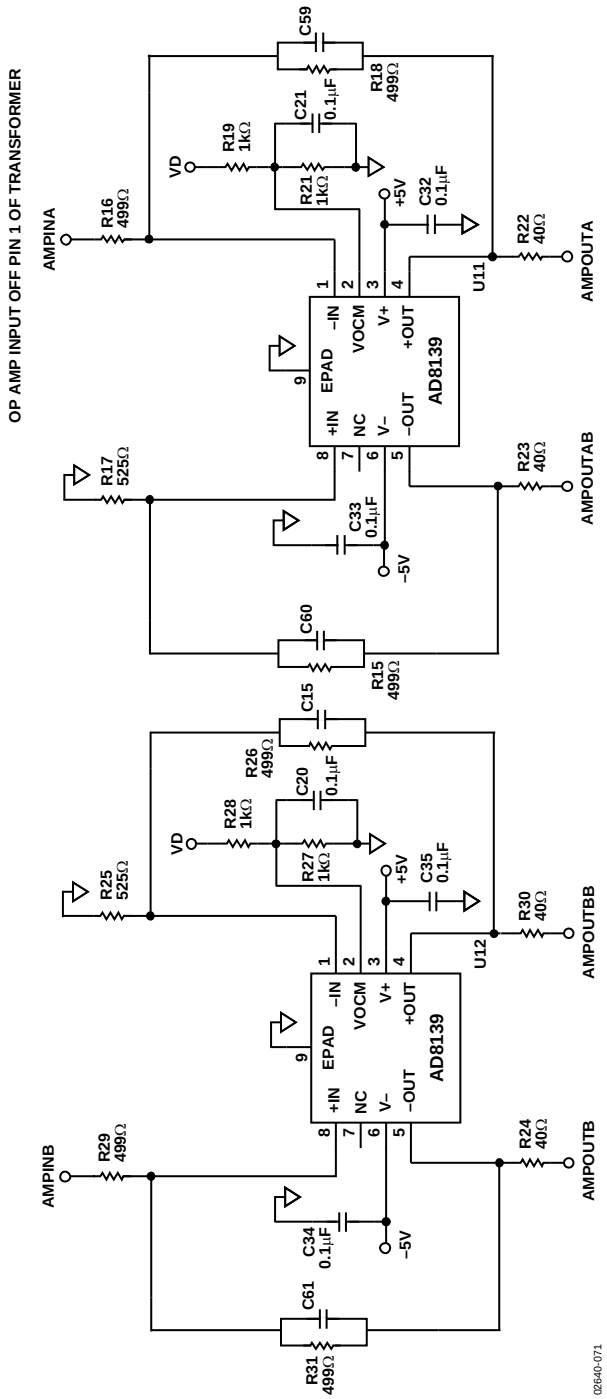


Figure 52. PCB Schematic (3 of 3)

LFCSP PCB LAYERS

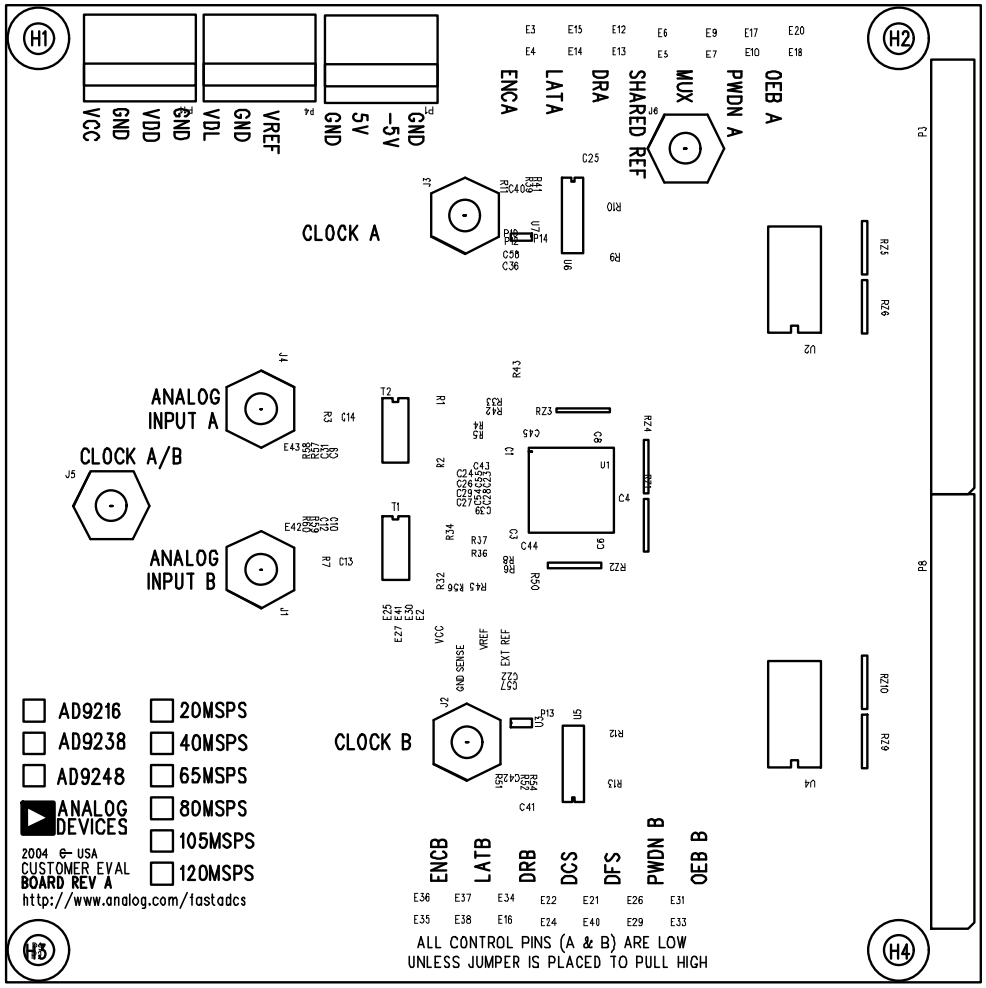


Figure 53. PCB Top-Side Silkscreen

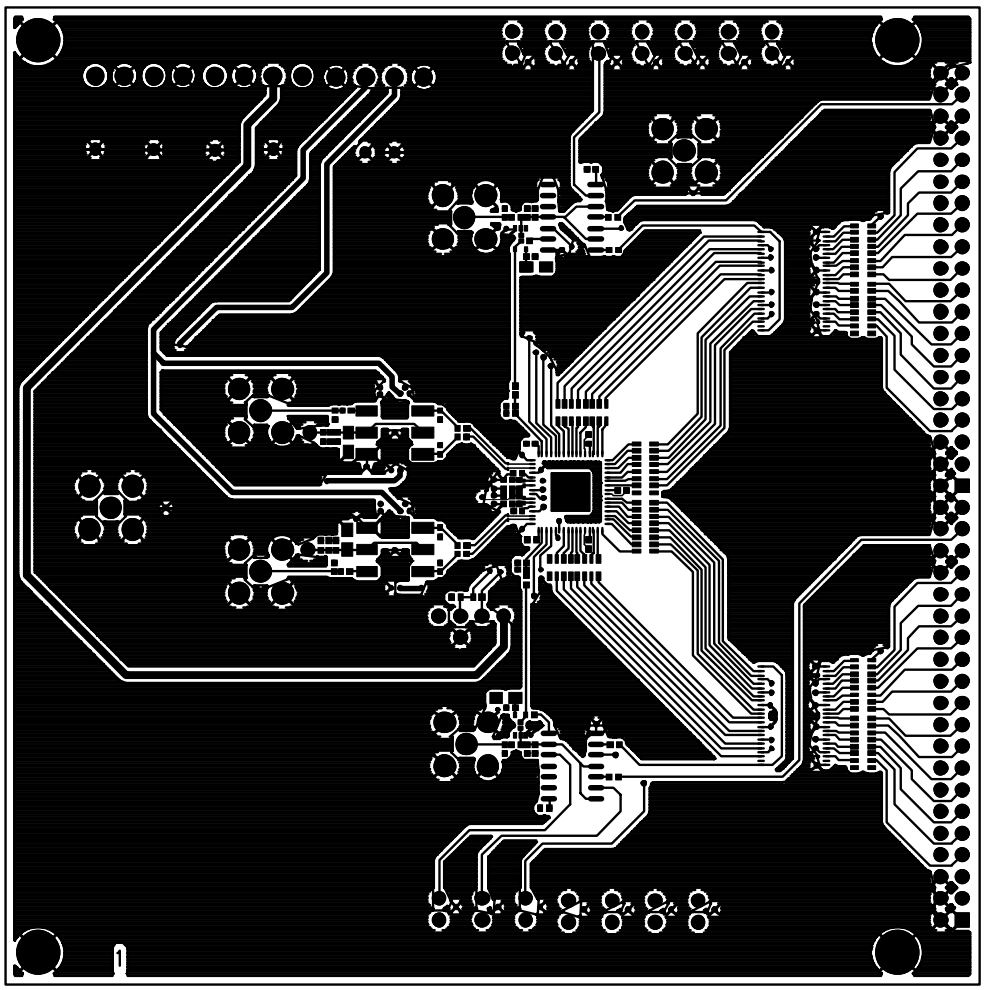


Figure 54. PCB Top-Side Copper Routing

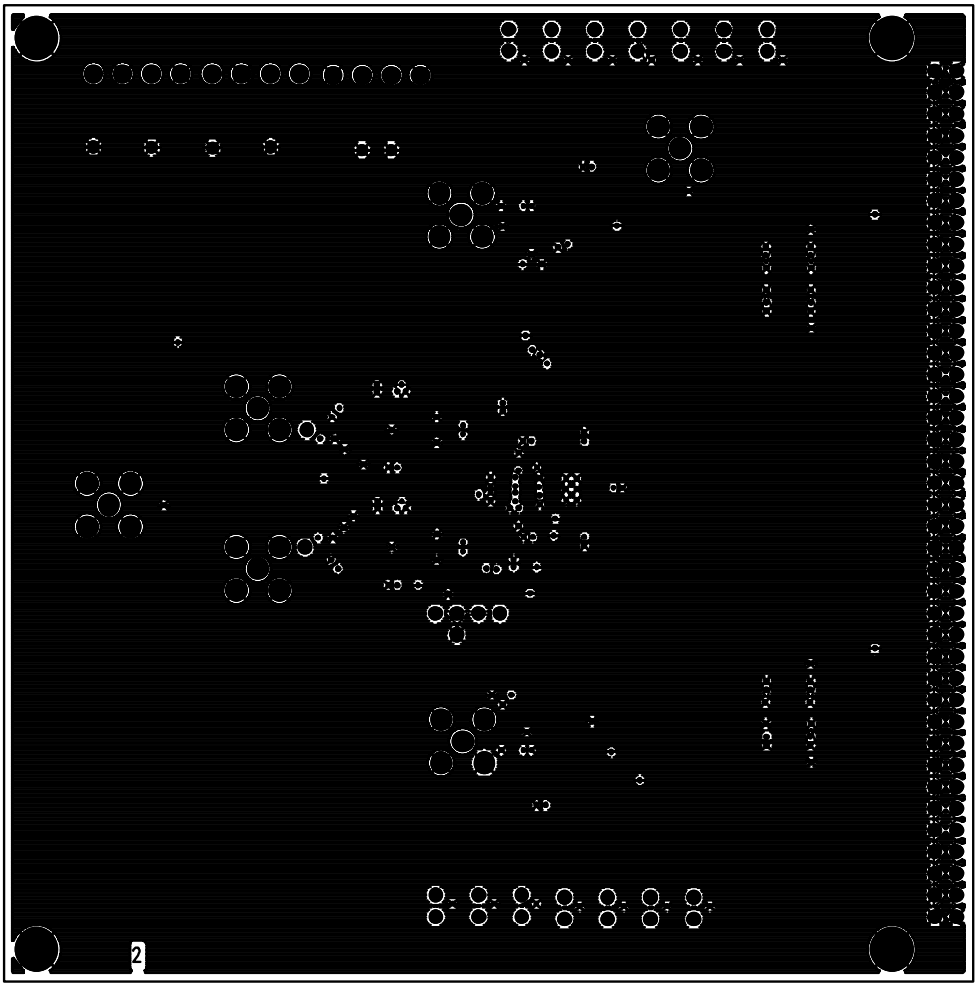


Figure 55. PCB Ground Layer

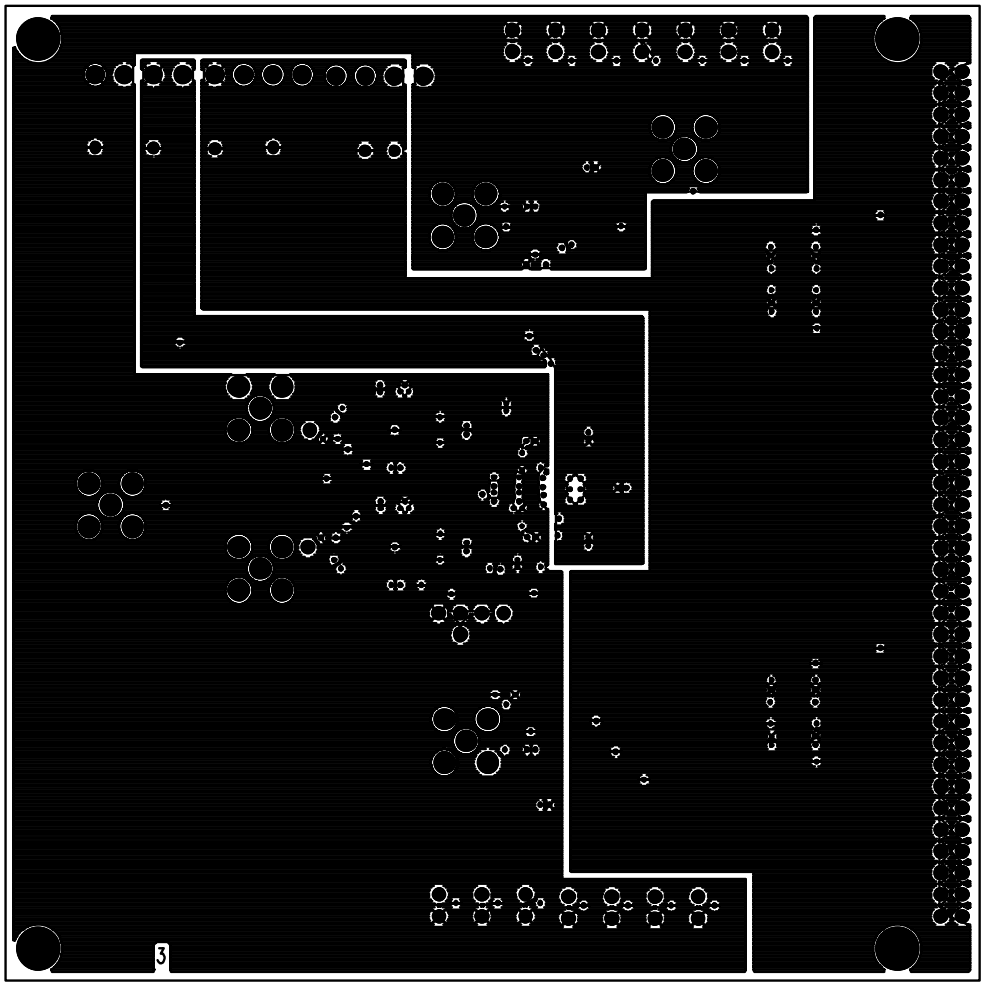


Figure 56. PCB Split Power Plane

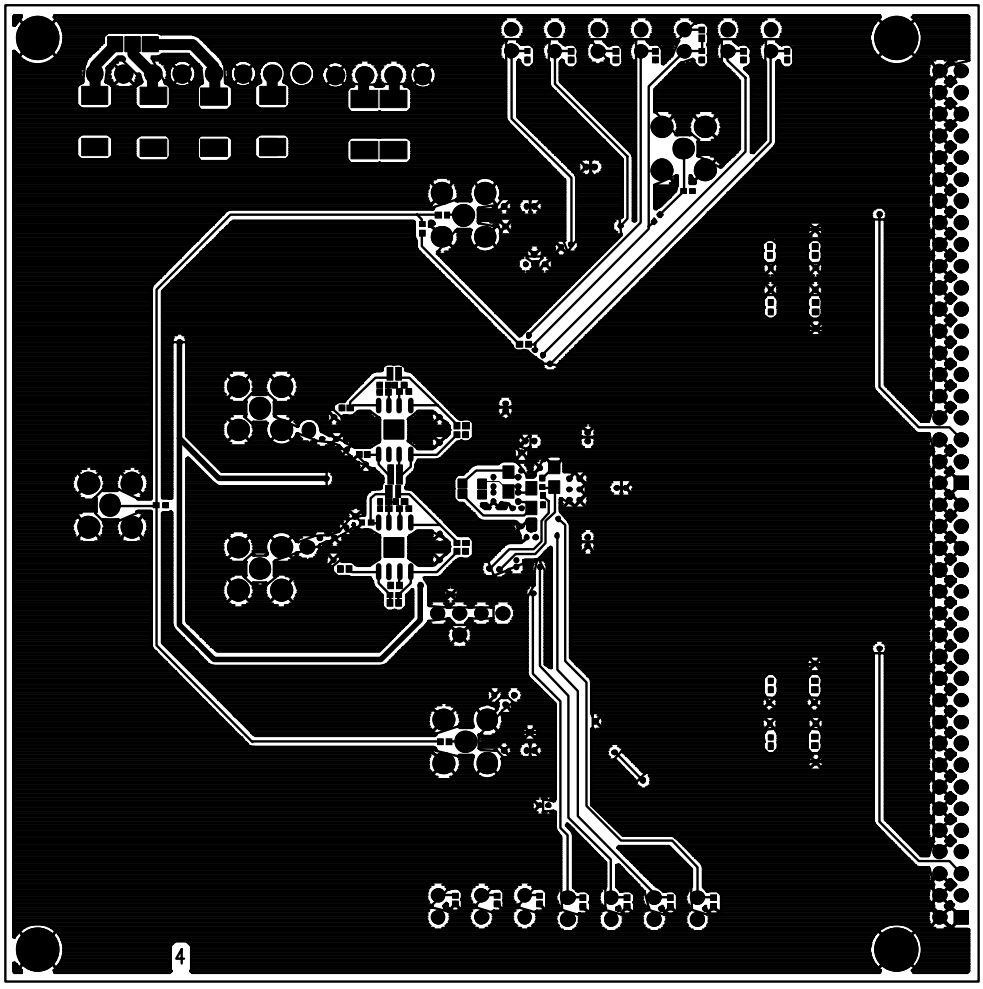


Figure 57. PCB Bottom-Side Copper Routing

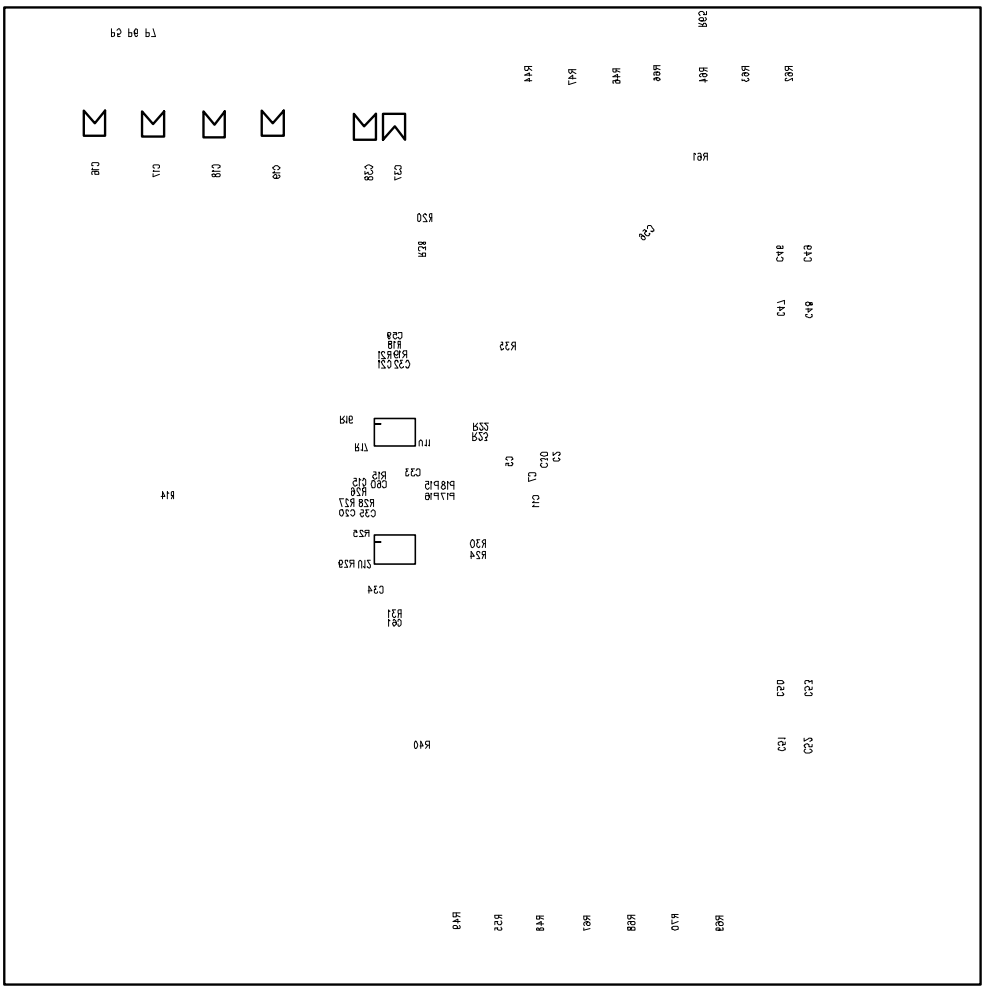


Figure 58. PCB Bottom-Side Silkscreen

THERMAL CONSIDERATIONS

The AD9238 LFCSP has an integrated heat slug that improves the thermal and electrical properties of the package when locally attached to a ground plane at the PCB. A thermal (filled) via array to a ground plane beneath the part provides a path for heat to escape the package, lowering junction temperature. Improved electrical performance also results from the reduction in package parasitics due to proximity of the ground plane. Recommended array is 0.3 mm vias on 1.2 mm pitch. θ_{JA} = 26.4°C/W with this recommended configuration. Soldering the slug to the PCB is a requirement for this package.

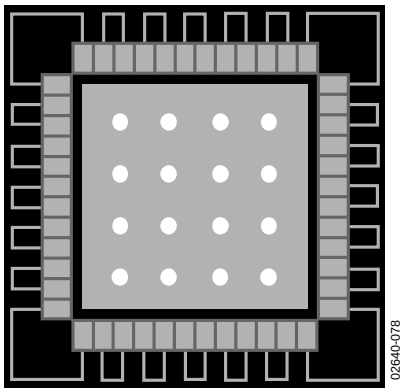
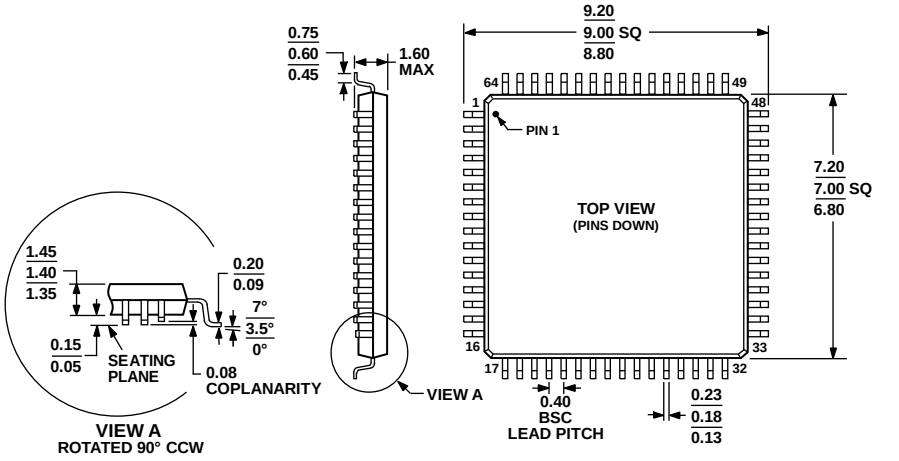


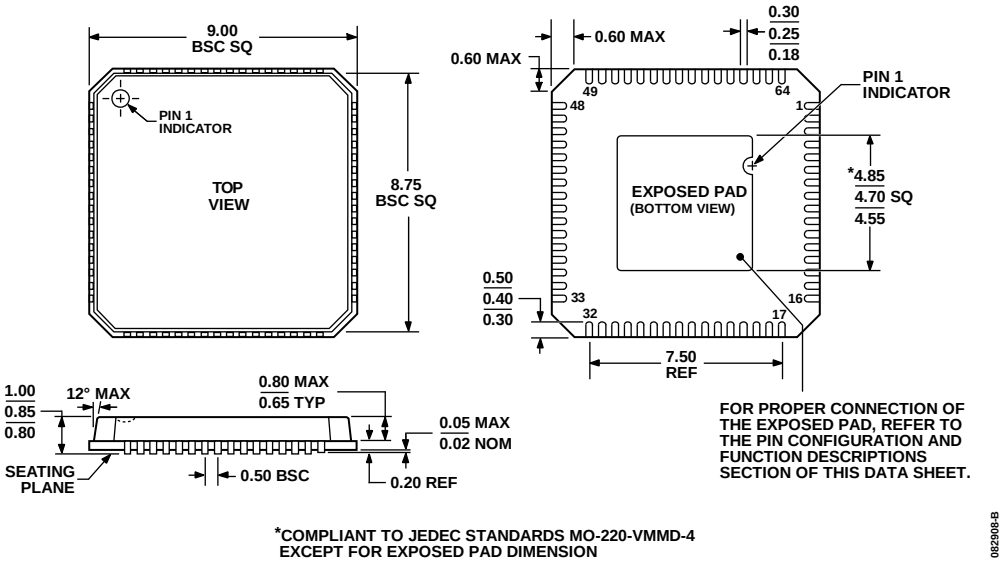
Figure 59. Thermal Via Array

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BBD

Figure 60. 64-Lead Low Profile Quad Flat Package [LQFP]
(ST-64-1)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 61. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9238BST-20	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZ-20	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZRL-20	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BST-40	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTRL-40	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZ-40	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZRL-40	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BST-65	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTRL-65	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZ-65	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BSTZRL-65	–40°C to +85°C	64-Lead Low Profile Quad Flat Package (LQFP)	ST-64-1
AD9238BCPZ-20	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCPZRL-20	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCPZ-40	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCPZRL-40	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCPZ-65	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCPZRL-65	–40°C to +85°C	64-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-64-1
AD9238BCP-65EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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