



# THE DATASHEET OF ADS8912BRGET



# ADS891xB 18-Bit, High-Speed SAR ADCs

## With Integrated Reference Buffer and Enhanced Performance Features

### 1 Features

- Resolution: 18-Bits
- High Sample Rate With No Latency Output:
  - ADS8910B: 1-MSPS
  - ADS8912B: 500-kSPS
  - ADS8914B: 250-kSPS
- Integrated LDO Enables Single-Supply Operation
- Low-Power Reference Buffer With No Droop
- Excellent AC and DC Performance:
  - SNR: 102.5-dB, THD: –125-dB
  - INL:  $\pm 0.5$ -LSB
  - DNL:  $\pm 0.2$ -LSB, 18-Bit No-Missing-Codes
- Wide Input Range:
  - Unipolar Differential Input Range:  $\pm V_{REF}$
  - $V_{REF}$  Input Range: 2.5-V to 5-V
- Single-Supply, Low-Power Operation (Includes Internal Reference Buffer and LDO)
  - ADS8910B : 21-mW at 1-MSPS
  - ADS8912B : 16-mW at 500-kSPS
  - ADS8914B : 14-mW at 250-kSPS
- Enhanced-SPI Digital Interface
  - Interface SCLK: 20-MHz at 1-MSPS
  - Configurable Data Parity Output
- Extended Temperature Range:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- Small Footprint: 4-mm  $\times$  4-mm VQFN

### 2 Applications

- Test and Measurement
- Medical Imaging
- High-Precision, High-Speed Data Acquisition

### 3 Description

The ADS8910B, ADS8912B, and ADS8914B (ADS891xB) belong to a family of pin-to-pin compatible, high-speed, single-channel, high-precision, 18-bit successive approximation register (SAR) analog-to-digital converters (ADCs) with an integrated reference buffer and integrated low-dropout regulator (LDO). The device family includes the ADS890xB (20-bit) and ADS892xB (16-bit) resolution variants.

The ADS891xB boost analog performance while maintaining high-resolution data transfer by using TI's enhanced-SPI feature. Enhanced-SPI enables the ADS89xxB to achieve high throughput at lower clock speeds, thereby simplifying the board layout and lowering system cost. Enhanced-SPI also simplifies clocking-in of data, thereby making this device an excellent choice for applications involving FPGAs, DSPs. The ADS89xxB is compatible with a standard SPI Interface.

The ADS891xB has an internal data parity feature that can be appended to the ADC data output. ADC data validation by the host, using parity bits, improves system reliability.

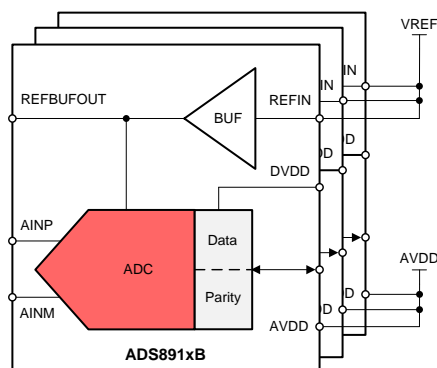
#### SPI Interface Clock at 1 MSPS

DEVICE RESOLUTION	3-WIRE SPI	3-WIRE ENHANCED SPI
20 bits	70 MHz	22 MHz
18 bits	58 MHz	20 MHz
16 bits	52 MHz	18 MHz

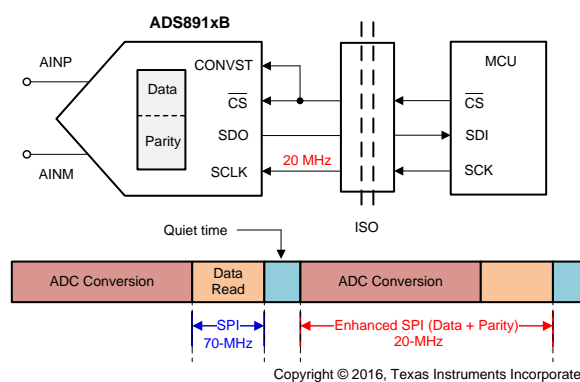
(1) For all features of the enhanced SPI, see the [Interface Module](#) section.

### Ease of System Design With ADS89xxB Integrated Features

Multi-ADC System With Single Supply and Reference



Lowest Clock Speeds at 1-MSPS Using 3-Wire Enhanced-SPI



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

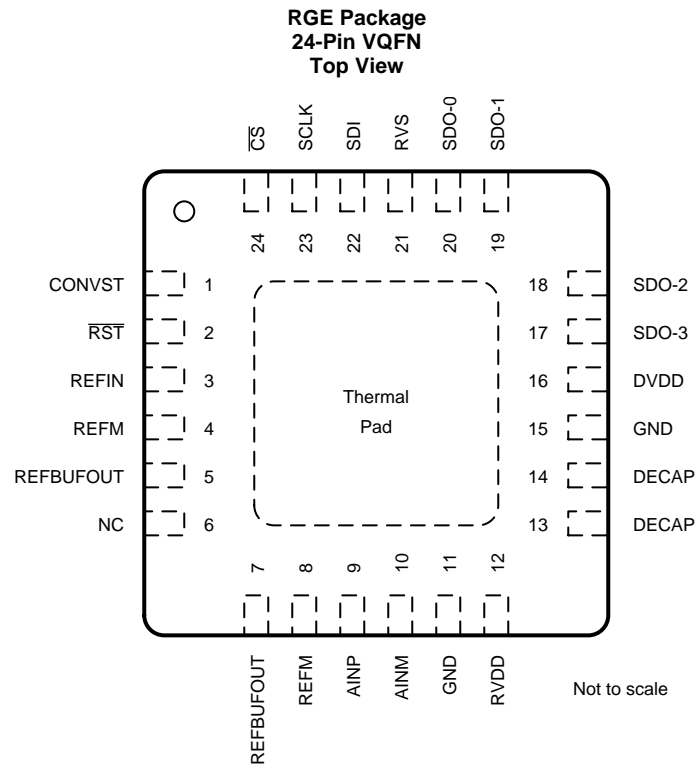
Changes from Revision A (July 2016) to Revision B	Page
• Changed front-page diagram.....	1
• Changed REFBUFOUT pin description from "Reference buffer output, ADC reference input" to "Internal reference buffer output, external reference input" .....	4
• Changed DV <sub>DD</sub> range in condition line of Electrical Characteristics from 2.35 V to 3.6 V to 1.65 V to 5.5 V .....	7
• Changed maximum value for DV <sub>DD</sub> range in specifications tables from 3.6 V to 5.5 V .....	7
• Added T <sub>A</sub> = 25°C to reference buffer offset voltage test condition in <i>Electrical Characteristics</i> table .....	7
• Changed input offset thermal drift typ value from 10 to 1 .....	7
• Added 100-kHz condition to SNR and THD parameters in the Electrical Characteristics .....	8
• Added f <sub>IN</sub> = 2 kHz test condition to SFDR in <i>Electrical Characteristics</i> table .....	8
• Added new conditions to serial clock frequency in the <i>Timing Requirements</i> table .....	9
• Added serial clock frequency conditions in <i>Timing Characteristics</i> table .....	9
• Added strobe output time to <i>Switching Characteristics</i> table .....	10
• Added Figure 26, <i>Noise Performance vs Input Frequency</i> .....	16
• Added Figure 27, <i>Distortion Performance vs Input Frequency</i> .....	16
• Added descriptive text and one figure to the <i>Reference Buffer Module</i> section .....	19
• Changed t <sub>d_RVS</sub> to t <sub>d_CSRDY</sub> in step 3 of <i>Data Transfer Frame</i> section .....	31
• Deleted text from first note element regarding data transfer activity in zone 2.....	34
• Added new note (1) for SCLK in Table 9 .....	44
• Changed <i>Data Acquisition (DAQ) Circuit for Lowest Distortion and Noise Performance...</i> section for clarity .....	59
• Added more design parameters to <i>Design Parameters</i> table .....	59
• Changed <i>Detailed Design Procedure</i> section for clarity .....	60
• Added two new application curves .....	60
• Added new typical application subsection .....	61
• Added text to <i>Power-Supply Recommendations</i> section for clarity .....	64

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**Changes from Original (June 2016) to Revision A****Page**

- 
- Changed from product preview to production data ..... 1
  - Changed  $DV_{DD}$  specified throughput value in the *Recommended Operating Conditions* from 3.6 V to 5.5 V..... 6
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## 5 Pin Configuration and Functions



### Pin Functions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
AINM	10	Analog input	Negative analog input
AINP	9	Analog input	Positive analog input
$\overline{\text{CS}}$	24	Digital input	Chip-select input pin; active low The device takes control of the data bus when $\overline{\text{CS}}$ is low. The SDO-x pins go to Hi-Z when $\overline{\text{CS}}$ is high.
CONVST	1	Digital input	Conversion start input pin. A CONVST rising edge brings the device from ACQ state to CNV state.
DECAP	13, 14	Power supply	Place decoupling capacitor here for internal power supply. Short pin 13 and 14 together.
DVDD	16	Power supply	Interface power supply pin
GND	11, 15	Power supply	Ground
NC	6	No connection	Float these pins; no external connection.
REFBUFOUT	5, 7	Analog input/output	Internal reference buffer output, external reference input. Short pin 5 and 7 together.
REFIN	3	Analog input	Reference voltage input
REFM	4, 8	Analog input	Reference ground potential
$\overline{\text{RST}}$	2	Digital input	Asynchronous reset input pin. A low pulse on the $\overline{\text{RST}}$ pin resets the device. All register bits return to the default state.
RVDD	12	Power supply	Analog power supply pin.
RVS	21	Digital output	Multifunction output pin. With $\overline{\text{CS}}$ held high, RVS reflects the status of the internal ADCST signal. With $\overline{\text{CS}}$ low, the status of RVS depends on the output protocol selection.
SCLK	23	Digital input	Clock input pin for the serial interface. All system-synchronous data transfer protocols are timed with respect to the SCLK signal.
SDI	22	Digital input	Serial data input pin. This pin is used to feed data or commands into the device.

**Pin Functions (continued)**

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
SDO-0	20	Digital output	Serial communication pin: data output 0
SDO-1	19	Digital output	Serial communication pin: data output 1
SDO-2	18	Digital output	Serial communication pin: data output 2
SDO-3	17	Digital output	Serial communication pin: data output 3
Thermal pad		Supply	Exposed thermal pad; connect to GND.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

	MIN	MAX	UNIT
RVDD to GND	-0.3	7	V
DVDD to GND	-0.3	7	V
REFIN to REFM	-0.3	RV <sub>DD</sub> + 0.3	V
REFM to GND	-0.1	0.1	V
Analog Input (AINP, AINM) to GND	-0.3	V <sub>REF</sub> + 0.3	V
Digital input ( $\overline{\text{RST}}$ , CONVST, $\overline{\text{CS}}$ , SCLK, SDI) to GND	-0.3	DV <sub>DD</sub> + 0.3	V
Digital output (RVS, SDO-0, SDO-1, SDO-2, SDO-3) to GND	-0.3	DV <sub>DD</sub> + 0.3	V
Analog Input (AINP, AINM) to RVDD and GND	-130	130	mA
Operating free-air temperature, T <sub>A</sub>	-40	125	°C
Storage temperature, T <sub>stg</sub>	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
RV <sub>DD</sub>	Analog supply voltage (RVDD to AGND)	3	5	5.5	V
DV <sub>DD</sub>	Digital supply voltage (DVDD to AGND)	Operating	3	5.5	V
		Specified throughput	2.35	3	
V <sub>REF</sub>	Reference input voltage on REFIN	2.5		RV <sub>DD</sub> - 0.3	V
C <sub>REFBUF</sub>	External ceramic decoupling capacitor	10	22		µF
R <sub>ESR</sub>	External series resistor	0	1	1.3	Ω
T <sub>A</sub>	Specified free-air operating temperature	-40	25	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		ADS891xB	UNITS
		RGE (VQFN)	
		24 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	31.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	29.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	8.9	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	8.9	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

At  $V_{DD} = 5.5\text{ V}$ ,  $DV_{DD} = 1.65\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum throughput (unless otherwise noted). Minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; typical values at  $T_A = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
FSR	Full-scale input range (AINP – AINM)		$-V_{REF}$		$V_{REF}$	V
$V_{IN}$	Absolute input voltage (AINP and AINM to REFM)		0		$V_{REF}$	V
$V_{CM}$	Common-mode voltage (AINP + AINM) / 2		$(V_{REF} / 2) - 0.1$	$V_{REF} / 2$	$(V_{REF} / 2) + 0.1$	V
$C_{IN}$	Input capacitance	Sample mode		60		pF
		Hold mode		4		pF
<b>VOLTAGE REFERENCE INPUT (REFIN)</b>						
$I_{REF}$	Reference input current	$V_{REF} = 5\text{ V}$		0.1	1	$\mu\text{A}$
$C_{REF}$	Internal capacitance			10		pF
<b>REFERENCE BUFFER OUTPUT (REFBUFOUT)</b>						
$V_{(RO)}$	Reference buffer offset voltage ( $V_{REFBUFOUT} - V_{REF}$ )	With EN_MARG = 0b <sup>(1)</sup> , $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	-250		250	$\mu\text{V}$
$C_{REFBUF}$	External ceramic decoupling capacitor		10	22		$\mu\text{F}$
$R_{ESR}$	External series resistor		0	1	1.3	$\Omega$
$I_{SHRT}$	Short-circuit current			30		mA
	Margining range	With EN_MARG = 1b <sup>(1)</sup>		$\pm 4.5$		mV
	Margining resolution	With EN_MARG = 1b <sup>(1)</sup>		280		$\mu\text{V}$
<b>DC ACCURACY<sup>(3)</sup> (<math>C_{REFBUF} = 22\ \mu\text{F}</math>, <math>R_{ESR} = 1\ \Omega</math>)</b>						
	Resolution			18		Bits
NMC	No missing codes		18			Bits
INL	Integral nonlinearity <sup>(4)</sup>		-1.5	$\pm 0.5$	1.5	LSB <sup>(5)</sup>
DNL	Differential nonlinearity <sup>(4)</sup>		-0.5	$\pm 0.2$	0.5	LSB <sup>(5)</sup>
$E_{(IO)}$	Input offset error <sup>(4)</sup>	$T_A = 25^\circ\text{C}$ <sup>(2)</sup>	-3	$\pm 0.5$	3	LSB <sup>(5)</sup>
		$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ <sup>(2)</sup>	-20	$\pm 3$	20	
$dV_{OS}/dT$	Input offset thermal drift <sup>(2)</sup>			1		$\mu\text{V}/^\circ\text{C}$
$G_E$	Gain error <sup>(4)</sup>	EN_MARG = 0b <sup>(1)(6)</sup>	-0.02	$\pm 0.005$	0.02	%FSR
$dG_E/dT$	Gain error thermal drift	EN_MARG = 0b <sup>(1)(6)</sup>		2.5		ppm/ $^\circ\text{C}$
TNS	Transition noise			0.72		LSB <sup>(5)</sup>
	First output code deviation for burst-mode data acquisition	See <a href="#">Reference Buffer Module</a>	-3		3	TNS
CMRR	Common-mode rejection ratio	dc to 20 kHz		80		dB
<b>SAMPLING DYNAMICS</b>						
	Aperture delay			4		ns
$t_{j-rms}$	Aperture jitter			2		ps RMS
$f_{3-DB(\text{small})}$	Small-signal bandwidth			23		MHz

(1) See the [REF\\_MRG Register](#).

(2) For selected  $V_{REF}$ , see the [OFST\\_CAL Register](#).

(3) While operating with internal reference buffer and LDO.

(4) See [Figure 8](#), [Figure 9](#), [Figure 14](#), and [Figure 15](#) for statistical distribution data for DNL, INL, offset, and gain error parameters.

(5) LSB = least-significant bit. 1 LSB at 18-bit resolution is approximately 3.8 ppm.

(6) Includes internal reference buffer errors and drifts.

## Electrical Characteristics (continued)

At  $R_{V_{DD}} = 5.5\text{ V}$ ,  $DV_{DD} = 1.65\text{ V to }5.5\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum throughput (unless otherwise noted).  
Minimum and maximum values at  $T_A = -40^\circ\text{C to }+125^\circ\text{C}$ ; typical values at  $T_A = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC ACCURACY<sup>(3)(7)</sup> (<math>C_{REFBUF} = 22\ \mu\text{F}</math>, <math>R_{ESR} = 1\ \Omega</math>)</b>						
SINAD	Signal-to-noise + distortion	$f_{IN} = 2\text{ kHz}$	100	102.48		dB
SNR	Signal-to-noise ratio	$f_{IN} = 2\text{ kHz}$	101	102.5		dB
		$f_{IN} = 100\text{ kHz}$		99		
THD	Total harmonic distortion	$f_{IN} = 2\text{ kHz}$		-125		dB
		$f_{IN} = 100\text{ kHz}$		-110		
SFDR	Spurious-free dynamic range	$f_{IN} = 2\text{ kHz}$		125		dB
<b>LDO OUTPUT (DECAP)</b>						
$V_{LDO}$	LDO output voltage (DECAP pins)			2.85		V
$C_{LDO}$	External ceramic capacitor on DECAP pins		1			$\mu\text{F}$
$t_{PU\_LDO}$	LDO power-up time	$C_{LDO} = 1\ \mu\text{F}$ , $R_{V_{DD}} > V_{LDO}$		1		ms
$I_{SHRT-LDO}$	Short-circuit current			100		mA
<b>DIGITAL INPUTS</b>						
$V_{IH}$	High-level input voltage	$1.65\text{ V} < DV_{DD} < 2.3\text{ V}$	$0.8 DV_{DD}$		$DV_{DD} + 0.3$	V
		$2.3\text{ V} < DV_{DD} < 5.5\text{ V}$	$0.7 DV_{DD}$		$DV_{DD} + 0.3$	
$V_{IL}$	Low-level input voltage	$1.65\text{ V} < DV_{DD} < 2.3\text{ V}$	-0.3		$0.2 DV_{DD}$	V
		$2.3\text{ V} < DV_{DD} < 5.5\text{ V}$	-0.3		$0.3 DV_{DD}$	
	Input current			$\pm 0.01$	0.1	$\mu\text{A}$
<b>DIGITAL OUTPUTS</b>						
$V_{OH}$	High-level output voltage	$I_{OH} = 500\text{-}\mu\text{A source}$	$0.8 DV_{DD}$		$DV_{DD}$	V
$V_{OL}$	Low-level output voltage	$I_{OH} = 500\text{-}\mu\text{A sink}$	0		$0.2 DV_{DD}$	V
<b>POWER SUPPLY</b>						
$I_{RVDD}$	Analog supply current	ADS8910B at $R_{V_{DD}} = 5\text{ V}$ , 1-MSPS		4.2	5.8	mA
		ADS8912B at $R_{V_{DD}} = 5\text{ V}$ , 500-KSPS		3.2	4	mA
		ADS8914B at $R_{V_{DD}} = 5\text{ V}$ , 250-KSPS		2.8	3.6	mA
		Static, no conversion		970		$\mu\text{A}$
		Static, $PD\_ADC = 1b^{(8)}$		900		$\mu\text{A}$
		Static, $PD\_REFBUF = 1b^{(8)}$		120		$\mu\text{A}$
		Static, $PD\_ADC = 1b$ and $PD\_REFBUF = 1b^{(8)}$		40		$\mu\text{A}$
$I_{DVDD}$	Digital supply current	$DV_{DD} = 3\text{ V}$ , $C_{LOAD} = 10\text{ pF}$ , no conversion		1		$\mu\text{A}$
$P_{RVDD}$	Power dissipation	ADS8910B at $R_{V_{DD}} = 5\text{ V}$ , 1-MSPS		21	29	mW
		ADS8912B at $R_{V_{DD}} = 5\text{ V}$ , 500-KSPS		16	20	
		ADS8914B at $R_{V_{DD}} = 5\text{ V}$ , 250-KSPS		14	18	

(7) For  $V_{IN} = -0.1\text{ dBFS}$ .

(8) See the [PD\\_CNTL Register](#).

## 6.6 Timing Requirements

		MIN	TYP	MAX	UNIT	TIMING DIAGRAM
<b>CONVERSION CYCLE</b>						
$f_{\text{cycle}}$	Sampling frequency	ADS8910B		1000	kHz	Figure 1
		ADS8912B		500		
		ADS8914B		250		
$t_{\text{cycle}}$	ADC cycle-time period	ADS8910B	1		$\mu\text{s}$	
		ADS8912B	2			
		ADS8914B	4			
$t_{\text{wh\_CONVST}}$	Pulse duration: CONVST high	30			ns	
$t_{\text{wl\_CONVST}}$	Pulse duration: CONVST low	30			ns	
$t_{\text{acq}}$	Acquisition time	300			ns	
$t_{\text{qt\_acq}}$	Quiet acquisition time	30			ns	
$t_{\text{d\_onvcap}}$	Quiet aperture time	20			ns	
<b>ASYNCHRONOUS RESET, AND LOW POWER MODES</b>						
$t_{\text{wl\_RST}}$	Pulse duration: $\overline{\text{RST}}$ low	100			ns	Figure 2
<b>SPI-COMPATIBLE SERIAL INTERFACE</b>						
$f_{\text{CLK}}$	Serial clock frequency	$2.35\text{ V} \leq \text{DV}_{\text{DD}} \leq 5.5\text{ V}$ , $T_{\text{A}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{\text{IH}} > 0.7\text{ DV}_{\text{DD}}$ , $V_{\text{IL}} < 0.3\text{ DV}_{\text{DD}}$		70	MHz	Figure 3
		$1.65\text{ V} \leq \text{DV}_{\text{DD}} < 2.35\text{ V}$ , $T_{\text{A}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{\text{IH}} > 0.8\text{ DV}_{\text{DD}}$ , $V_{\text{IL}} < 0.2\text{ DV}_{\text{DD}}$		20		
		$1.65\text{ V} \leq \text{DV}_{\text{DD}} < 2.35\text{ V}$ , $T_{\text{A}} = 0^{\circ}\text{C}$ to $+60^{\circ}\text{C}$ , $V_{\text{IH}} > 0.8\text{ DV}_{\text{DD}}$ , $V_{\text{IL}} < 0.2\text{ DV}_{\text{DD}}$		57		
		$1.65\text{ V} \leq \text{DV}_{\text{DD}} < 2.35\text{ V}$ , $T_{\text{A}} = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$ , $V_{\text{IH}} > 0.9\text{ DV}_{\text{DD}}$ , $V_{\text{IL}} < 0.1\text{ DV}_{\text{DD}}$		68		
$t_{\text{CLK}}$	Serial clock time period	$1/f_{\text{CLK}}$			ns	Figure 3
$t_{\text{ph\_CK}}$	SCLK high time	0.45		0.55	$t_{\text{CLK}}$	Figure 3
$t_{\text{pl\_CK}}$	SCLK low time	0.45		0.55	$t_{\text{CLK}}$	
$t_{\text{su\_CSCK}}$	Setup time: $\overline{\text{CS}}$ falling to the first SCLK capture edge	12			ns	
$t_{\text{su\_CKDI}}$	Setup time: SDI data valid to the SCLK capture edge	1.5			ns	
$t_{\text{ht\_CKDI}}$	Hold time: SCLK capture edge to (previous) data valid on SDI	1			ns	
$t_{\text{ht\_CKCS}}$	Delay time: last SCLK falling to $\overline{\text{CS}}$ rising	7			ns	
<b>SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)<sup>(1)</sup></b>						
$f_{\text{CLK}}$	Serial clock frequency	SDR (DATA_RATE = 0b), $2.35\text{ V} \leq \text{DV}_{\text{DD}} \leq 5.5\text{ V}$		70	MHz	Figure 4, see Data Transfer Protocols
		DDR (DATA_RATE = 1b), $2.35\text{ V} \leq \text{DV}_{\text{DD}} \leq 5.5\text{ V}$		35		
$t_{\text{CLK}}$	Serial clock time period	$1/f_{\text{CLK}}$			ns	

(1) The external clock option is not recommended when operating with  $\text{DV}_{\text{DD}} < 2.35\text{ V}$ . See [Table 9](#).

## 6.7 Switching Characteristics

At  $V_{DD} = 5.5\text{ V}$ ,  $DV_{DD} = 1.65\text{ V}$  to  $5.5\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum throughput (unless otherwise noted). Minimum and maximum values at  $T_A = -40^\circ\text{C}$  to  $+125^\circ\text{C}$ ; typical values at  $T_A = 25^\circ\text{C}$ .

PARAMETER		MIN	TYP	MAX	UNIT	TIMING DIAGRAM
<b>CONVERSION CYCLE</b>						
$t_{conv}$	Conversion time	ADS8910B		640	ns	Figure 1
		ADS8912B	1100	1200		
		ADS8914B	2400	2500		
<b>ASYNCHRONOUS RESET, AND LOW POWER MODES</b>						
$t_{d\_rst}$	Delay time: $\overline{\text{RST}}$ rising to RVS rising			3	ms	Figure 2
$t_{PU\_ADC}$	Power-up time for converter module	1			ms	See PD_CNTL Register
$t_{PU\_REFBUF}$	Power-up time for internal reference buffer, $C_{REFBUF} = 22\ \mu\text{F}$	10			ms	
$t_{PU\_Device}$	Power-up time for device $C_{LDO} = 1\ \mu\text{F}$ , $C_{REFBUF} = 22\ \mu\text{F}$	10			ms	
<b>SPI-COMPATIBLE SERIAL INTERFACE</b>						
$t_{den\_CSDO}$	Delay time: $\overline{\text{CS}}$ falling to data enable			9	ns	Figure 3
$t_{dz\_CSDO}$	Delay time: $\overline{\text{CS}}$ rising to SDO going to Hi-Z			10	ns	
$t_{d\_CKDO}$	Delay time: SCLK launch edge to (next) data valid on SDO			13	ns	
$t_{d\_CSRDY\_f}$	Delay time: $\overline{\text{CS}}$ falling to RVS falling			12	ns	Figure 4
$t_{d\_CSRDY\_r}$	Delay time: $\overline{\text{CS}}$ rising to RVS rising	After NOP operation		30	ns	Figure 4
		After WR or RD operation		120		
<b>SOURCE-SYNCHRONOUS SERIAL INTERFACE (External Clock)<sup>(1)</sup></b>						
$t_{d\_CKSTR\_r}$	Delay time: SCLK launch edge to RVS rising			13	ns	Figure 4
$t_{d\_CKSTR\_f}$	Delay time: SCLK launch edge to RVS falling			13	ns	
$t_{off\_STRDO\_f}$	Time offset: RVS falling to (next) data valid on SDO	-2		2	ns	
$t_{off\_STRDO\_r}$	Time offset: RVS rising to (next) data valid on SDO	-2		2	ns	
$t_{ph\_STR}$	Strobe output high time, $2.35\text{ V} \leq DV_{DD} \leq 5.5\text{ V}$	0.45		0.55	$t_{STR}$	
$t_{pl\_STR}$	Strobe output low time, $2.35\text{ V} \leq DV_{DD} \leq 5.5\text{ V}$	0.45		0.55	$t_{STR}$	
<b>SOURCE-SYNCHRONOUS SERIAL INTERFACE (Internal Clock)</b>						
$t_{d\_CSSTR}$	Delay time: $\overline{\text{CS}}$ falling to RVS rising	15		50	ns	Figure 5
$t_{STR}$	Strobe output time period	INTCLK option		15	ns	
		INTCLK / 2 option		30		
		INTCLK / 4 option		60		
$t_{ph\_STR}$	Strobe output high time	0.45		0.55	$t_{STR}$	
$t_{pl\_STR}$	Strobe output low time	0.45		0.55	$t_{STR}$	

(1) The external clock option is not recommended when operating with  $DV_{DD} < 2.35\text{ V}$ . See [Table 9](#).

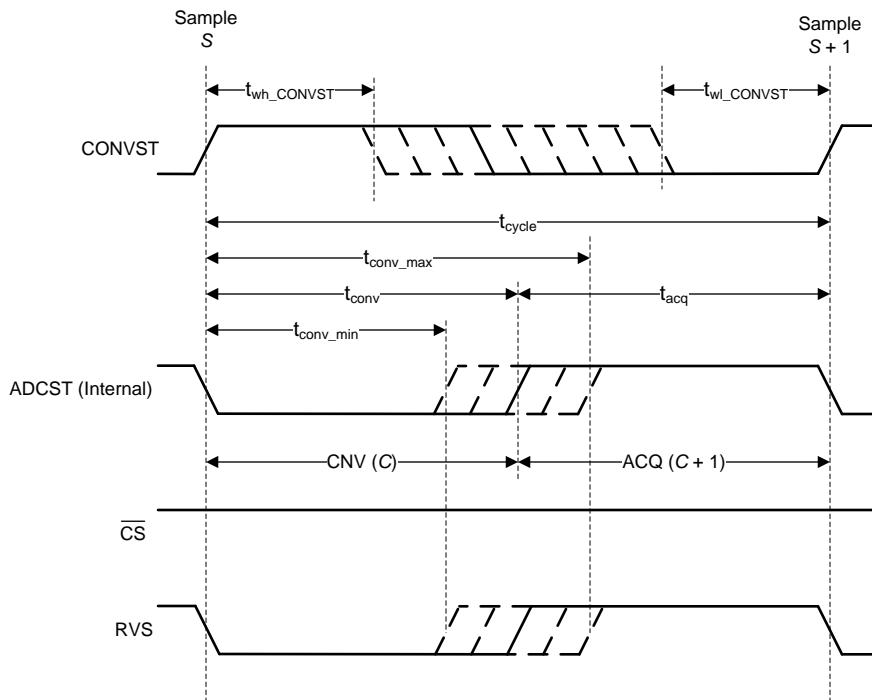


Figure 1. Conversion Cycle Timing

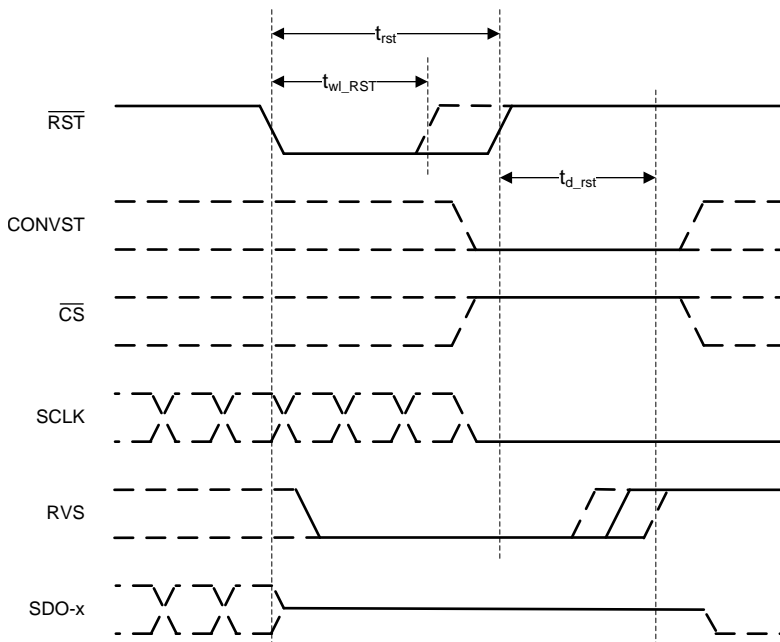
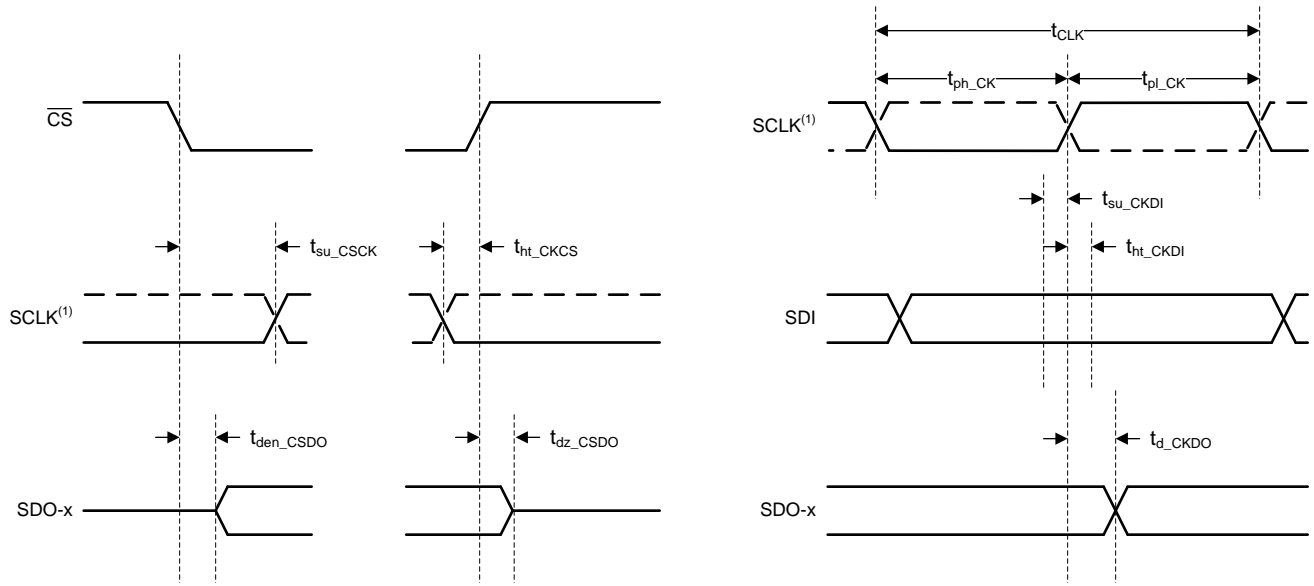
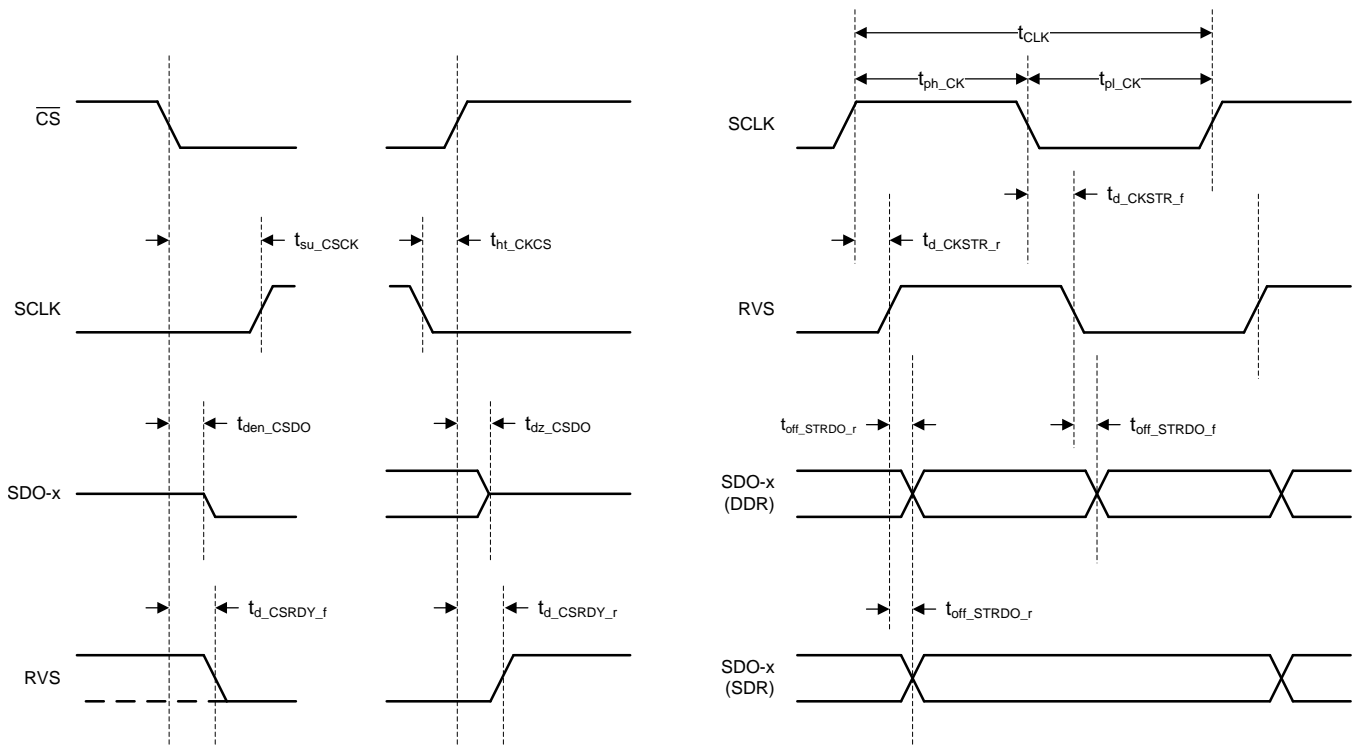


Figure 2. Asynchronous Reset Timing



(1) The SCLK polarity, launch edge, and capture edge depend on the SPI protocol selected.

**Figure 3. SPI-Compatible Serial Interface Timing**



**Figure 4. Source-Synchronous Serial Interface Timing (External Clock)**

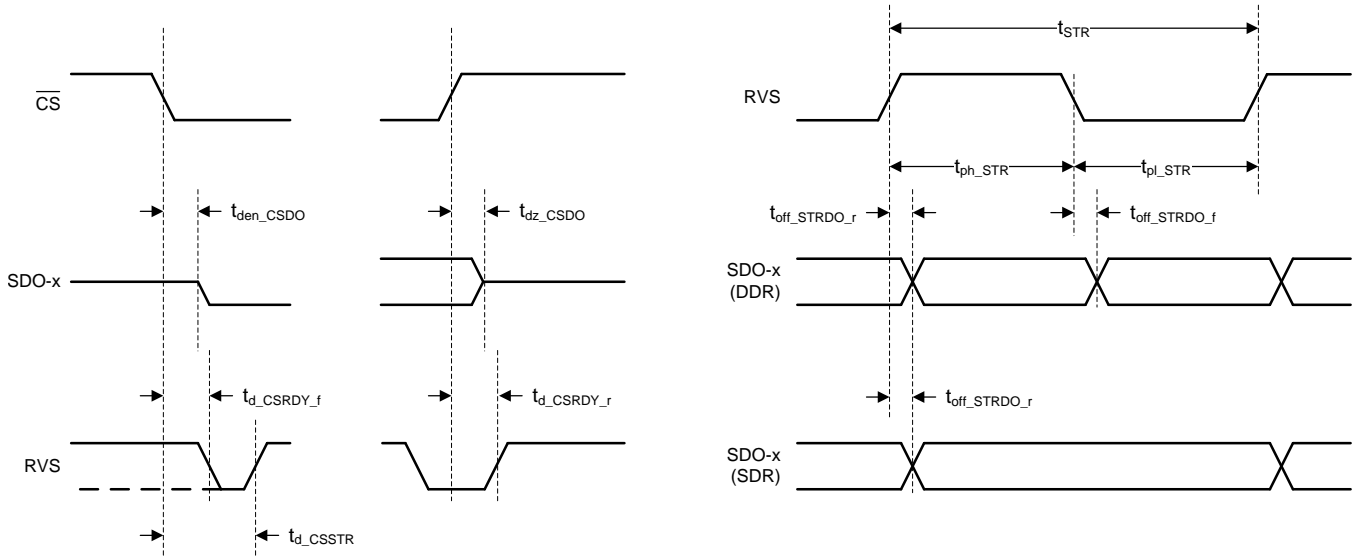
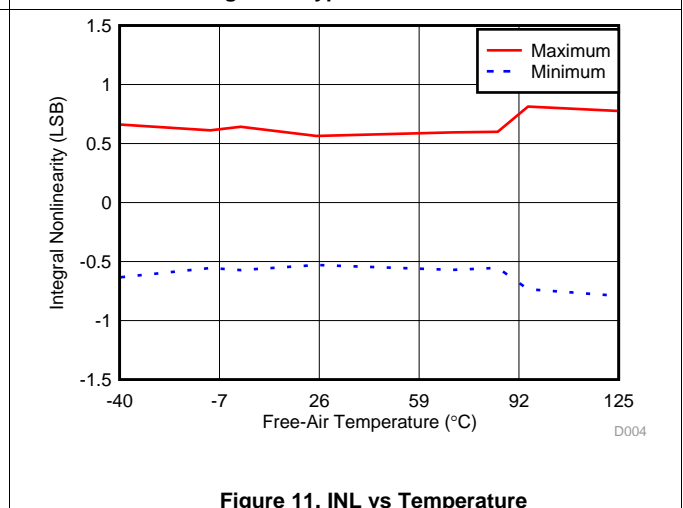
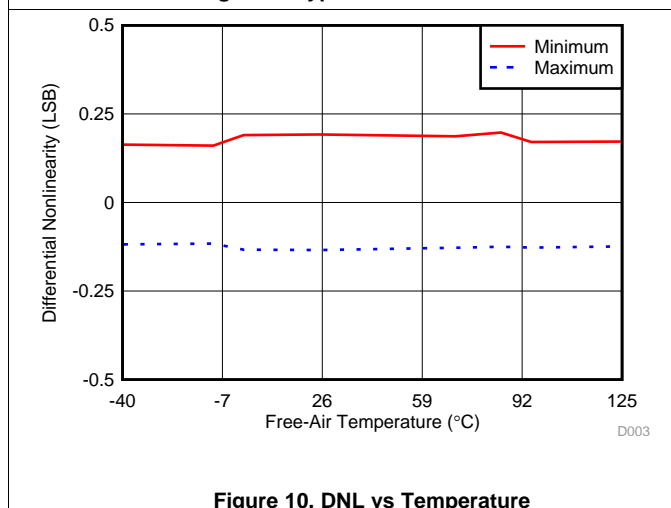
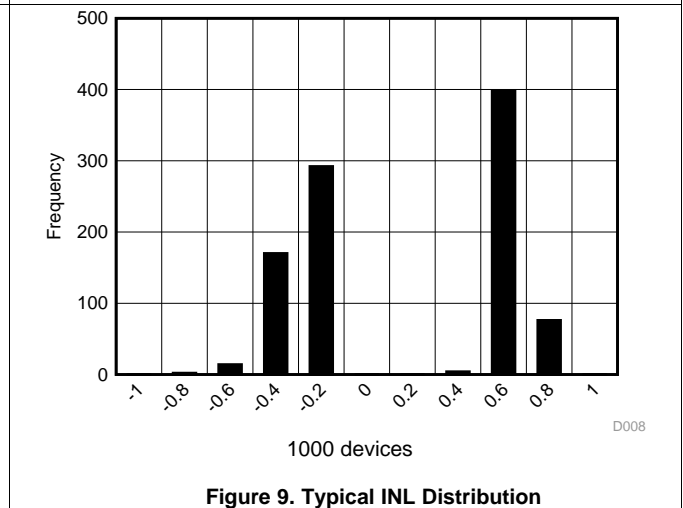
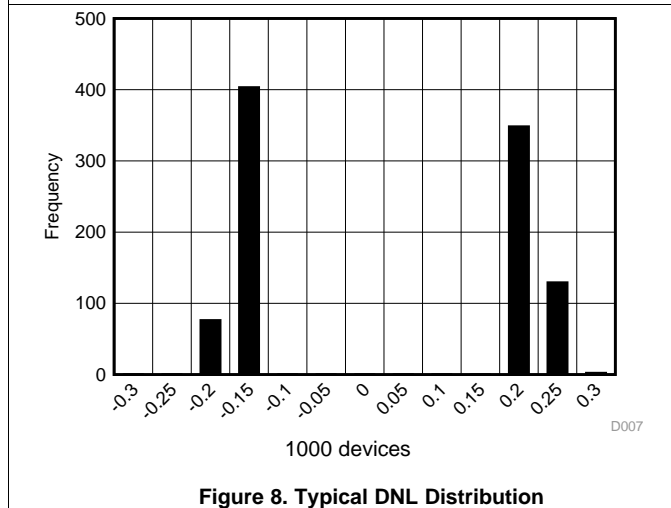
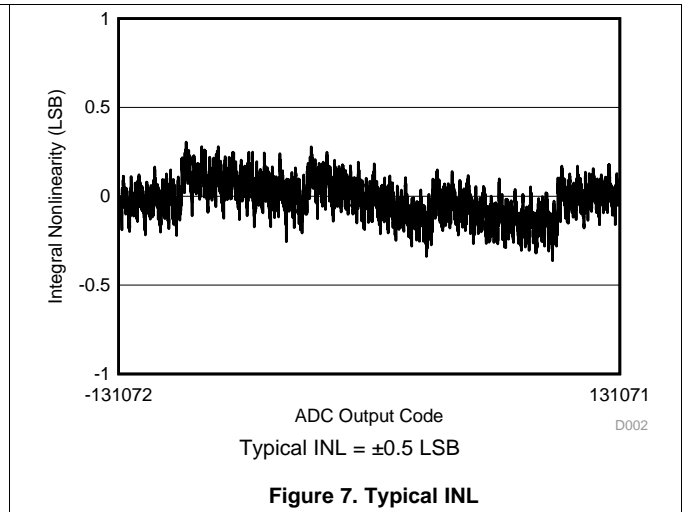
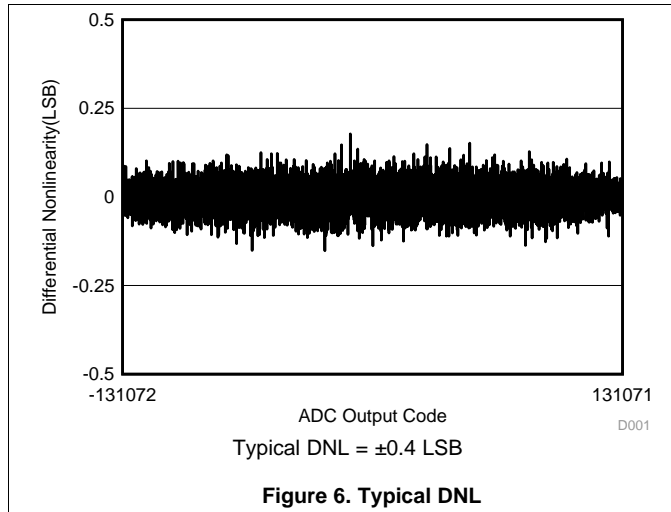


Figure 5. Source-Synchronous Serial Interface Timing (Internal Clock)

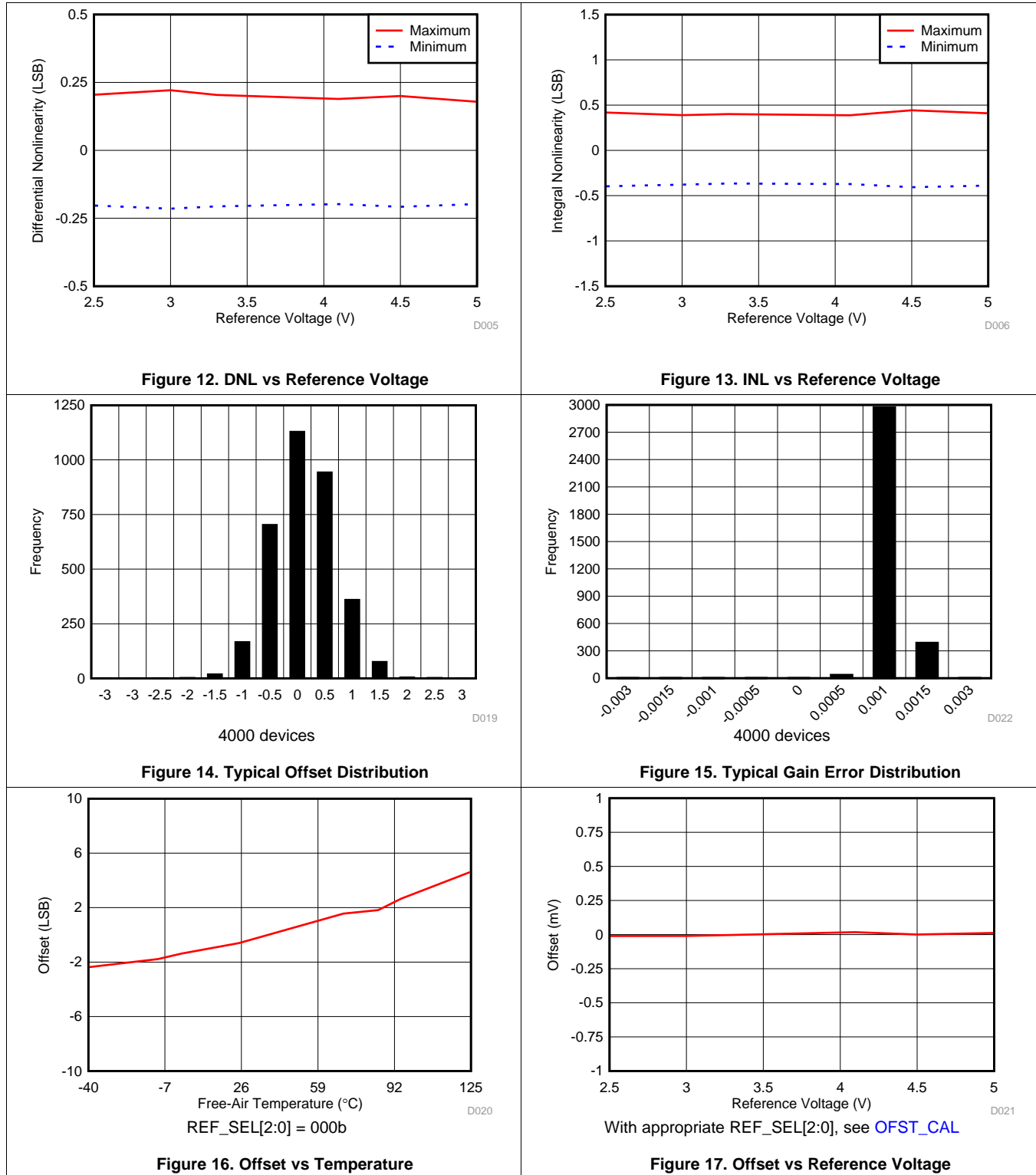
## 6.8 Typical Characteristics

at  $T_A = 25^\circ\text{C}$ ,  $R_{V_{DD}} = 5.5\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum-rated throughput (unless otherwise noted)



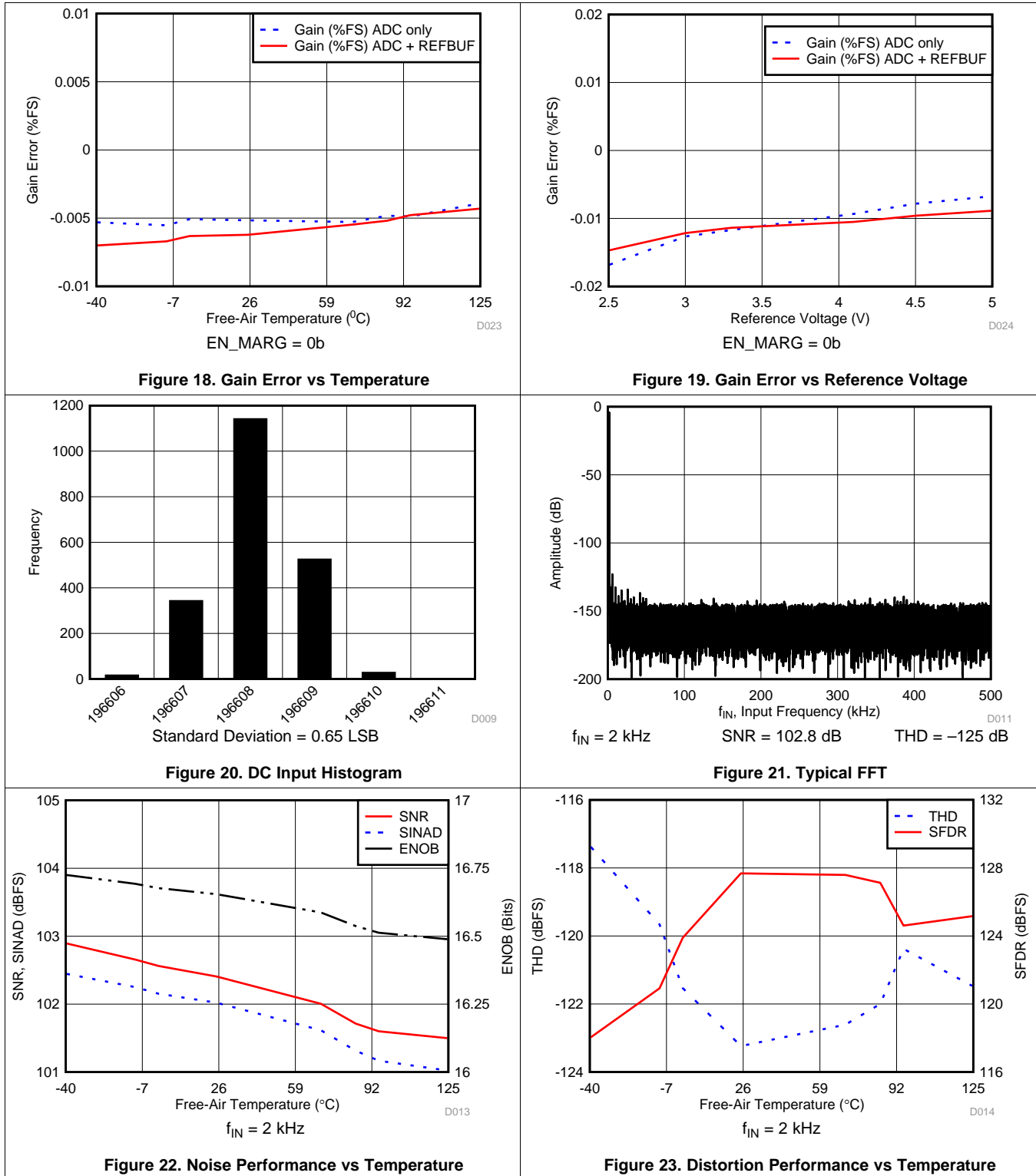
### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_{V_{DD}} = 5.5\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum-rated throughput (unless otherwise noted)



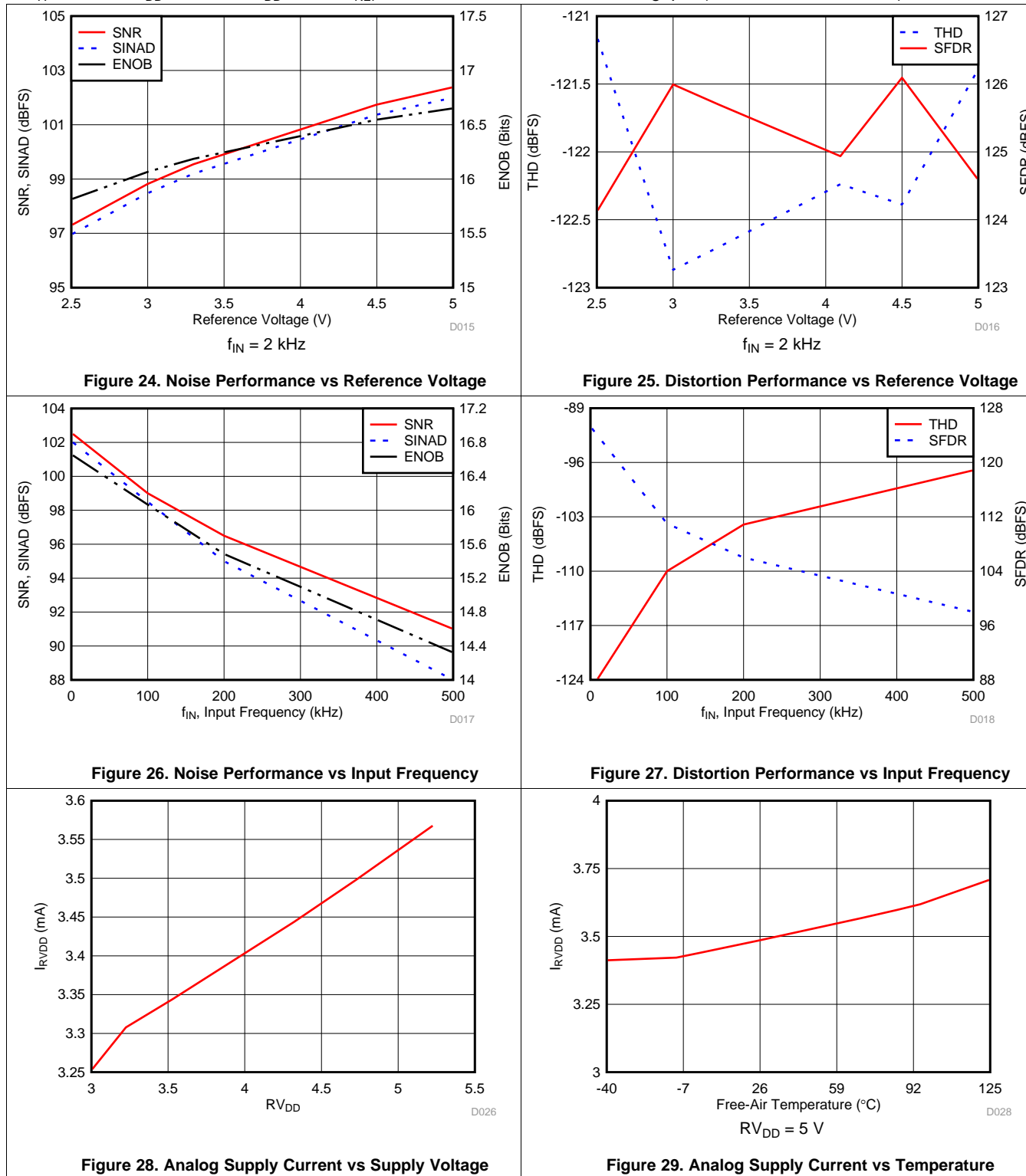
**Typical Characteristics (continued)**

at  $T_A = 25^\circ\text{C}$ ,  $R_{V_{DD}} = 5.5\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum-rated throughput (unless otherwise noted)



### Typical Characteristics (continued)

at  $T_A = 25^\circ\text{C}$ ,  $R_{V_{DD}} = 5.5\text{ V}$ ,  $DV_{DD} = 3\text{ V}$ ,  $V_{REF} = 5\text{ V}$ , and maximum-rated throughput (unless otherwise noted)



## 7 Detailed Description

### 7.1 Overview

The ADS891xB is a family of high-speed, successive approximation register (SAR), analog-to-digital converters (ADC) based on a charge redistribution architecture. These compact devices integrate a reference buffer and LDO, and feature high performance at a high throughput rate with low power consumption.

This device family supports unipolar, fully differential, analog input signals. The integrated reference buffer supports the burst mode of data acquisition for external reference voltages in the range 2.5 V to 5 V, and offers a wide selection of input ranges without additional input scaling.

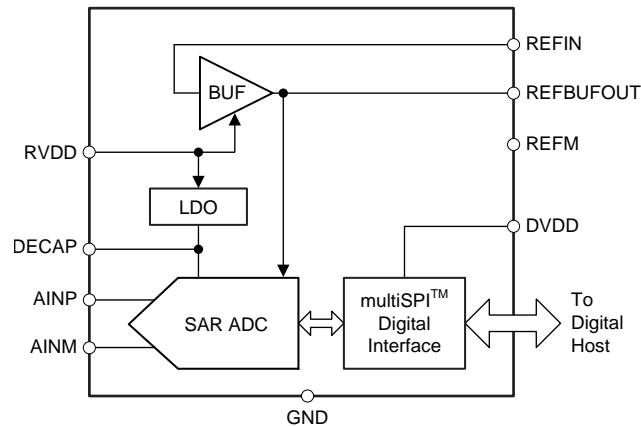
When a conversion is initiated, the differential input between the AINP and AINM pins is sampled on the internal capacitor array. The device uses an internal clock to perform conversions. During the conversion process, both analog inputs are disconnected from the internal circuit. At the end of conversion process, the device reconnects the sampling capacitors to the AINP and AINM pins and enters an acquisition phase.

The integrated LDO allows the device to operate on a single supply,  $V_{DD}$ . The device consumes only 21 mW, 16 mW, or 14 mW of power when operating at the rated maximum throughput of 1 MSPS, 500 kSPS, or 250 kSPS, respectively, with the internal reference buffer and LDO enabled.

The enhanced multiSPI™ digital interface is backward-compatible with traditional SPI protocol. Configurable features simplify board layout, timing, and firmware, and support high throughput at lower clock speeds, thus allowing an easy interface with a variety of microcontrollers, DSPs, and FPGAs.

The ADS891xB enables test and measurement, medical, and industrial applications to achieve fast, low-noise, low-distortion, low-power data acquisition in small form factors.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

From a functional perspective, the device comprises four modules: the low-dropout regulator (LDO), the reference buffer (BUF), the converter (SAR ADC), and the interface (multiSPI digital interface), as shown in the [Functional Block Diagram](#) section.

The LDO module is powered by the  $R_{VDD}$  supply, and generates the bias voltage for internal circuit blocks of the device. The reference buffer module buffers the external reference voltage source from the dynamic, capacitive switching load present on the reference pins during the conversion process. The converter module samples and converts the analog input into an equivalent digital output code. The interface module facilitates communication and data transfer between the device and the host controller.

### 7.3.1 LDO Module

To enable single-supply operation, the device features an internal low-dropout regulator (LDO). The LDO is powered by the  $R_{VDD}$  supply, and the output is available on the two DECAP pins. This LDO output powers the critical analog blocks within the device, and must not be used for any other external purposes.

Short the two DECAP pins together, and decouple with the GND pin by placing a 1- $\mu$ F, X7R-grade, ceramic capacitor with a 10-V rating, as shown in [Figure 30](#). There is no upper limit on the value of the decoupling capacitor; however, a larger decoupling capacitor results in a longer power-up time for the device. See the [Layout](#) section for layout recommendations.

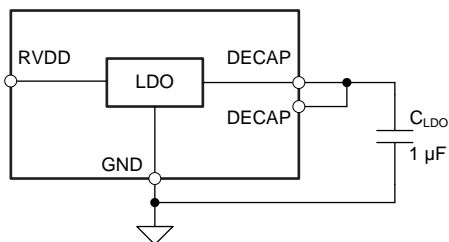


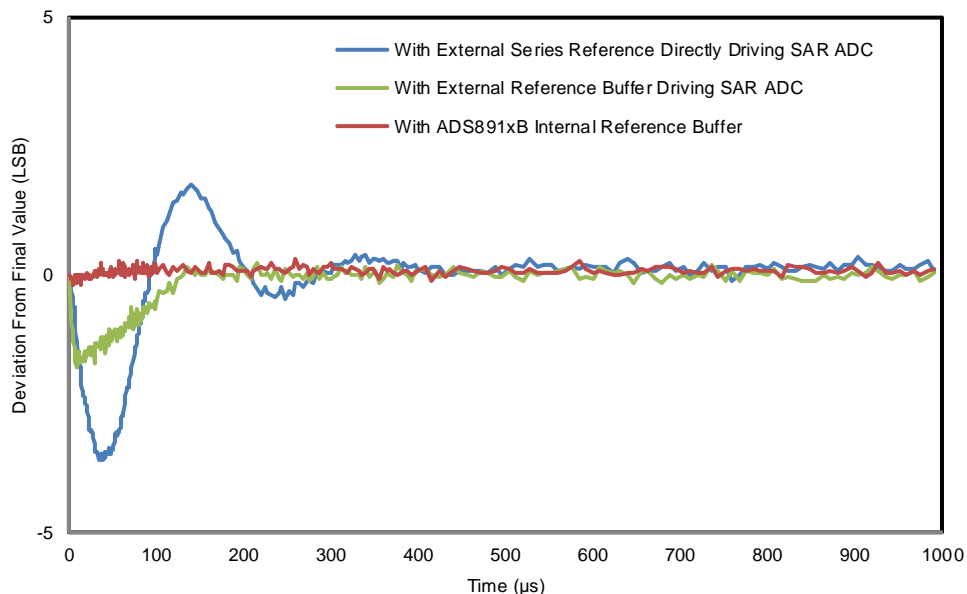
Figure 30. Internal LDO Connections

### 7.3.2 Reference Buffer Module

On the CONVST rising edge, the device moves from ACQ state to CONV state, and the internal capacitors are switched to the REFBUFOUT pins as per the successive approximation algorithm. Most of the switching charge required during the conversion process is provided by external decoupling capacitor  $C_{REFBUF}$ . If the charge lost from the  $C_{REFBUF}$  is not replenished before the next CONVST rising edge, the voltage on REFBUFOUT pins is less than  $V_{REFBUFOUT}$ . The subsequent conversion occurs with this different reference voltage, and causes a proportional error in the output code. The internal reference buffer of the device maintains the voltage on REFBUFOUT pins within 0.5-LSB of  $V_{REFBUFOUT}$ . All the performance characteristics of the device are specified with the internal reference buffer and specified values of  $C_{REFBUF}$  and  $R_{ESR}$ .

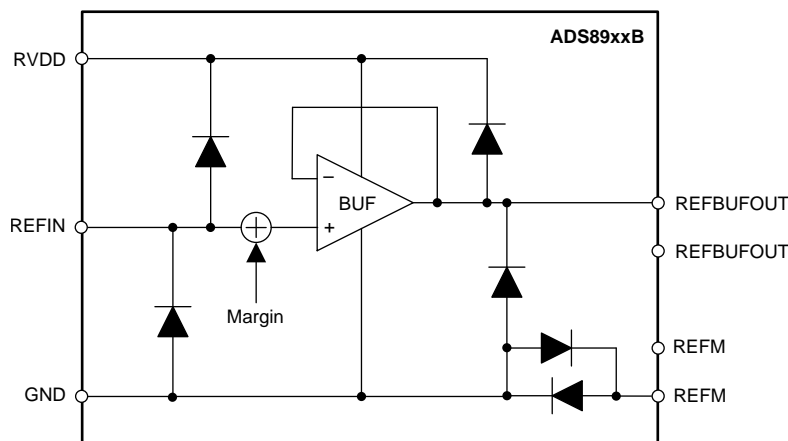
In burst-mode of operation, the device stays in ACQ state for a long duration of time and then performs a burst of conversions. During the acquisition state (ACQ), the sampling capacitor ( $C_S$ ) is connected to the differential input pins and no charge is drawn from the REFBUFOUT pins. However, during the very first conversion cycle, there is a step change in the current drawn from the REFBUFOUT pins. This sudden change in load triggers a transient settling response in the reference buffer. For a fixed input voltage, any transient settling error at the end of the conversion cycle results in a change in output codes over the subsequent conversions, as shown in [Figure 31](#). The internal reference buffer of the ADS89xxB, when used with the recommended values of  $C_{REFBUF}$  and  $R_{ESR}$ , keeps the transient settling error at the end of each conversion cycle within 0.5-LSB. Therefore, the device supports burst-mode of operation with every conversion result being as per the datasheet specifications.

## Feature Description (continued)



**Figure 31. ADC Output Codes in Burst-Mode Operation With Various ADC Reference Buffers**

Figure 32 shows the block diagram of the internal reference buffer.



**Figure 32. Internal Reference Buffer Block Diagram**

The input range for the device is set by the external voltage applied at the REFIN pin ( $V_{REF}$ ). The REFIN pin has electrostatic discharge (ESD) protection diodes to the RVDD and GND pins. For minimum input offset error (see  $E_{(IO)}$  specified in the [Electrical Characteristics](#)), set the REF\_SEL[2:0] bits to the value closest to  $V_{REF}$  (see the [OFST\\_CAL](#) register).

The internal reference buffer has a typical gain of 1 V/V with minimal offset error (see  $V_{(RO)}$  specified in the [Electrical Characteristics](#)), and the output of the buffer is available between the REFBUFOUT pins and the REF pins. Set the REF\_OFST[4:0] bits to add or subtract an intentional offset voltage (see the [REF\\_MRG](#) register).

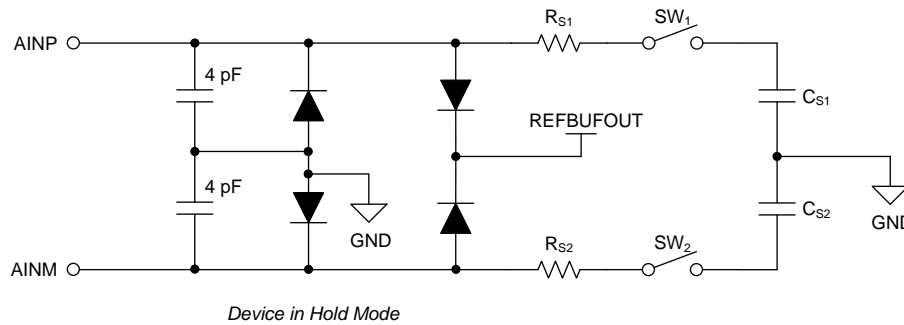
Figure 33 shows the external connections required for the internal reference buffer.



## Feature Description (continued)

### 7.3.3.1 Sample-and-Hold Circuit

These devices support unipolar, fully differential, analog input signals. [Figure 35](#) shows a small-signal equivalent circuit of the sample-and-hold circuit. Each sampling switch is represented by a resistance ( $R_{S1}$  and  $R_{S2}$ , typically  $50\ \Omega$ ) in series with an ideal switch ( $SW_1$  and  $SW_2$ ). The sampling capacitors,  $C_{S1}$  and  $C_{S2}$ , are typically  $60\ \text{pF}$ .



**Figure 35. Input Sampling Stage Equivalent Circuit**

During the acquisition process (ACQ state), both positive and negative inputs are individually sampled on  $C_{S1}$  and  $C_{S2}$ , respectively. During the conversion process (CNV state), the device converts for the voltage difference between the two sampled values:  $V_{AINP} - V_{AINM}$ .

Each analog input pin has electrostatic discharge (ESD) protection diodes to REFBUFOUT and GND. Keep the analog inputs within the specified range to avoid turning the diodes on.

[Equation 1](#) and [Equation 2](#) show the full-scale input range (FSR) and common-mode voltage ( $V_{CM}$ ), respectively, supported at the analog inputs for any external reference voltage provided on the REFIN pin ( $V_{REF}$ ).

$$\text{FSR} = \pm V_{REF} \quad (1)$$

$$V_{CM} = \left( \frac{V_{REF}}{2} \right) \pm 0.1\ \text{V} \quad (2)$$

## Feature Description (continued)

### 7.3.3.2 Internal Oscillator

The device family features an internal oscillator (OSC) that provides the conversion clock; see [Figure 34](#). The conversion duration is bound by the minimum and maximum value of  $t_{conv}$ , as specified in the [Switching Characteristics](#) table.

The interface module uses this internal clock (OSC), an external clock (provided by the host controller on the SCLK pin), or a combination of both the internal and external clocks, to execute the data transfer operations between the device and host controller; see the [Interface Module](#) section for more details.

### 7.3.3.3 ADC Transfer Function

The device family supports unipolar, fully differential analog inputs. The device output is in two's complement format. [Figure 36](#) and [Table 1](#) show the ideal transfer characteristics for the device.

The least significant bit (LSB) for the ADC is given by [Equation 3](#):

$$1 \text{ LSB} = \frac{\text{FSR}}{2^{18}} = 2 \times \frac{V_{\text{REF}}}{2^{18}} \quad (3)$$

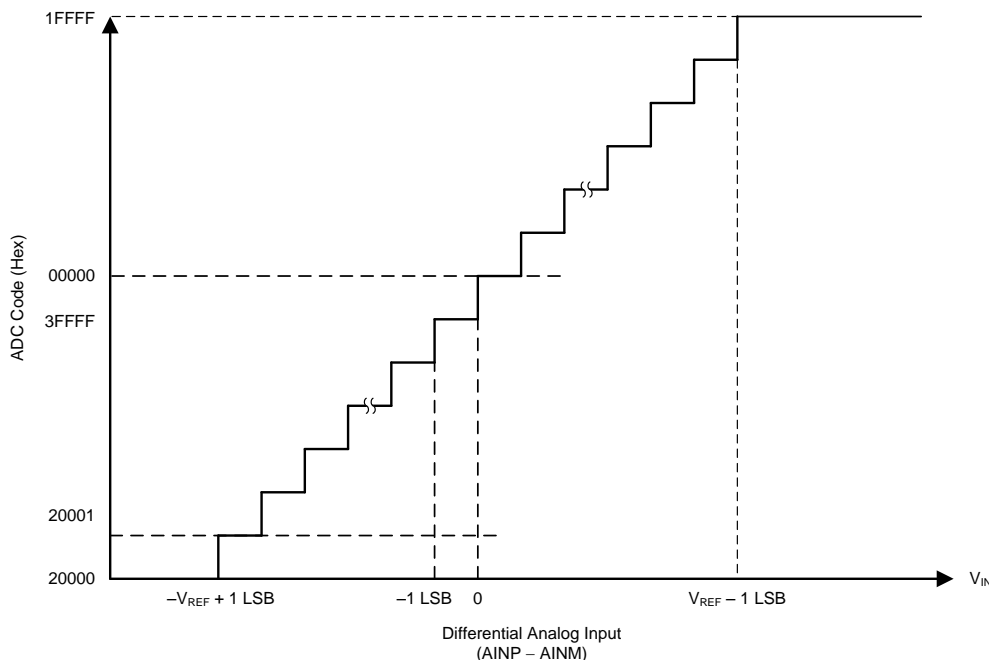


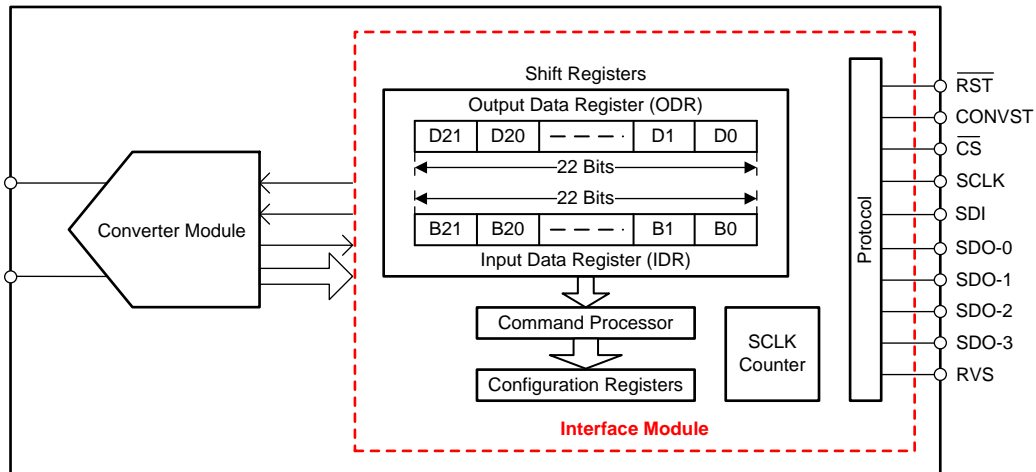
Figure 36. Differential Transfer Characteristics

Table 1. Transfer Characteristics

DIFFERENTIAL ANALOG INPUT VOLTAGE (AINP - AINM)	OUTPUT CODE (HEX)
$< -V_{\text{REF}}$	20000
$-V_{\text{REF}} + 1 \text{ LSB}$	20001
$-1 \text{ LSB}$	3FFFF
0	00000
1 LSB	00001
$> V_{\text{REF}} - 1 \text{ LSB}$	1FFFF

### 7.3.4 Interface Module

The interface module facilitates the communication and data transfer between the device and the host controller. As shown in [Figure 37](#), the module consists of shift registers (both input and output), configuration registers, and a protocol unit.



**Figure 37. Interface Module**

The [Pin Configuration and Functions](#) section provides descriptions of the interface pins. The [Data Transfer Frame](#) section details the functions of shift registers, the SCLK counter, and the command processor. The [Data Transfer Protocols](#) section details supported protocols. The [Register Maps](#) section explains the configuration registers and bit settings.

## 7.4 Device Functional Modes

As shown in Figure 38, this device family supports three functional states: RST, ACQ, and CNV. The device state is determined by the status of the CONVST and  $\overline{\text{RST}}$  control signals provided by the host controller.

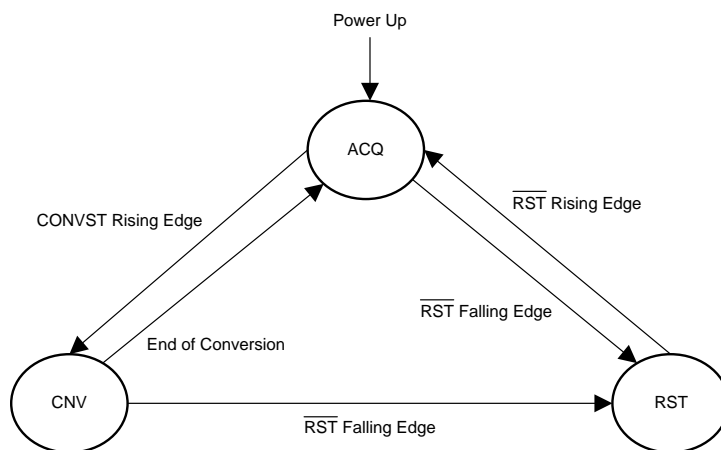


Figure 38. Device Functional States

### 7.4.1 RST State

The  $\overline{\text{RST}}$  pin is an asynchronous digital input for the device. To enter RST state, the host controller pulls the  $\overline{\text{RST}}$  pin low and keeps it low for the  $t_{\text{wl\_RST}}$  duration (as specified in the [Timing Requirements](#) table).

In RST state, all configuration registers (see the [Register Maps](#) section) are reset to their default values, the RVS pin remains low, and the SDO-x pins are Hi-Z.

To exit RST state, the host controller pulls the  $\overline{\text{RST}}$  pin high, with CONVST and SCLK held low and  $\overline{\text{CS}}$  held high, as shown in Figure 39. After a delay of  $t_{\text{d\_rst}}$ , the device enters ACQ state and the RVS pin goes high.

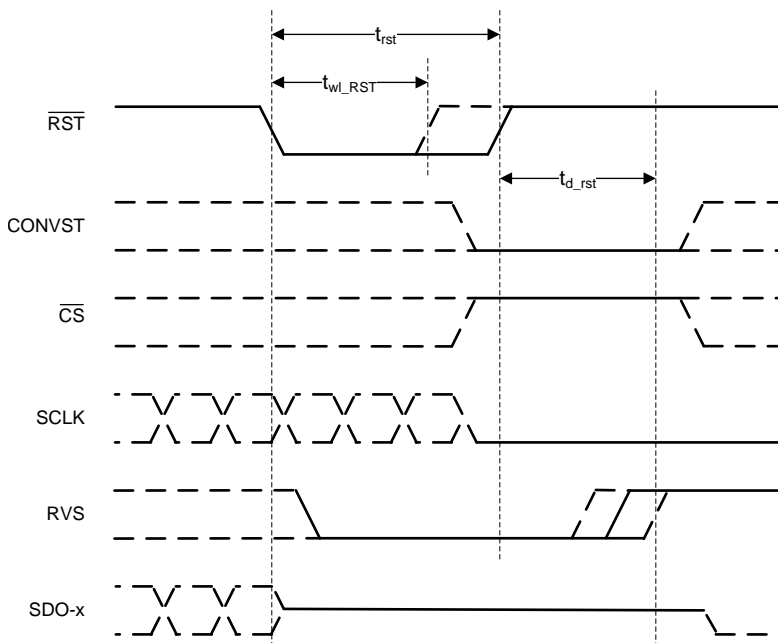


Figure 39. Asynchronous Reset

To operate the device in either ACQ or CNV state,  $\overline{\text{RST}}$  must be held high. With  $\overline{\text{RST}}$  held high, transitions on the CONVST pin determine the functional state of the device.

## Device Functional Modes (continued)

Figure 40 shows a typical conversion process. The internal ADCST signal goes low during conversion and goes high at the end of conversion. With  $\overline{\text{CS}}$  held high, RVS reflects the status of ADCST.

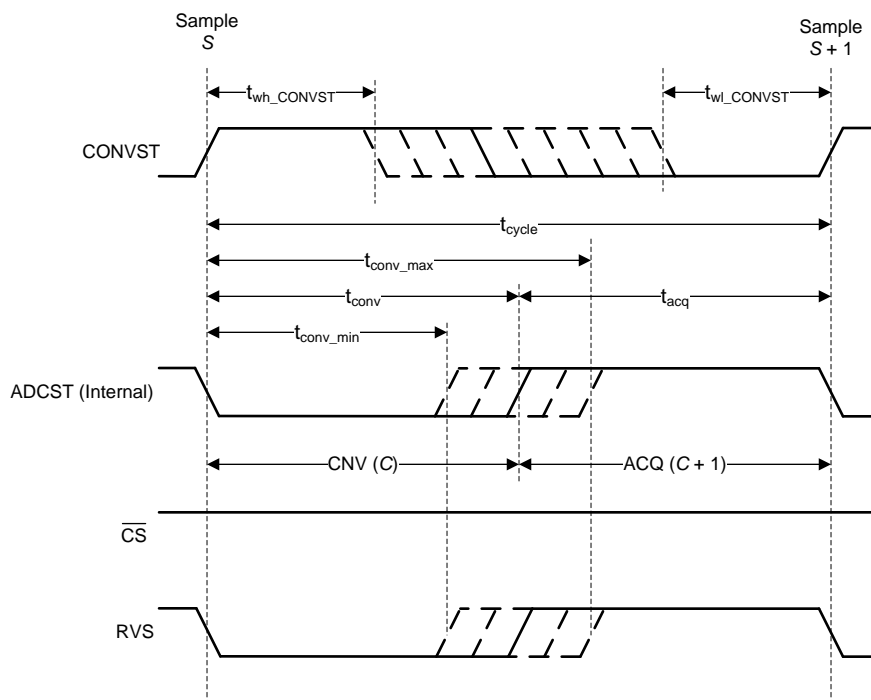


Figure 40. Typical Conversion Process

### 7.4.2 ACQ State

In ACQ state, the device acquires the analog input signal. The device enters ACQ state at power-up, when coming out of power down (See the [PD Control](#) section), after any asynchronous reset, and at the end of every conversion.

An  $\overline{\text{RST}}$  falling edge takes the device from ACQ state to RST state. A CONVST rising edge takes the device from ACQ state to CNV state.

### 7.4.3 CNV State

The device moves from ACQ state to CNV state on a rising edge of the CONVST pin. The conversion process uses an internal clock. The device ignores any further transitions on the CONVST signal until the ongoing conversion is complete (that is, during the time interval of  $t_{\text{conv}}$ ).

At the end of conversion, the device enters ACQ state. The cycle time for the device is given by [Equation 4](#):

$$t_{\text{cycle-min}} = t_{\text{conv}} + t_{\text{acq-min}} \quad (4)$$

#### NOTE

The conversion time,  $t_{\text{conv}}$ , varies within the specified limits of  $t_{\text{conv-min}}$  and  $t_{\text{conv-max}}$  (as specified in the [Switching Characteristics](#) table). After initiating a conversion, the host controller must monitor for a low-to-high transition on the RVS pin or wait for the  $t_{\text{conv-max}}$  duration to elapse before initiating a new operation (data transfer or conversion). If RVS is not monitored, substitute  $t_{\text{conv}}$  in [Equation 4](#) with  $t_{\text{conv-max}}$ .

## 7.5 Programming

This device family features nine configuration registers (as described in the [Register Maps](#) section). To access the internal configuration registers, these devices support the commands listed in [Table 2](#).

**Table 2. Supported Commands**

B[21:17]	B[16:8]	B[7:0]	COMMAND ACRONYM	COMMAND DESCRIPTION
00000	000000000	00000000	NOP	No operation
10000	<9-bit address>	<8-bit unmasked bits>	CLR_BITS	Clear <8-bit unmasked bits> from <9-bit address>
10001	<9-bit address>	00000000	RD_REG	Read contents from the <9-bit address>
10010	<9-bit address>	<8-bit data>	WR_REG	Write <8-bit data> to the <9-bit address>
10011	<9-bit address>	<8-bit unmasked bits>	SET_BITS	Set <8-bit unmasked bits> from <9-bit address>
11111	111111111	11111111	NOP	No operation
Remaining combinations	xxxxxxxxx	xxxxxxxxx	Reserved	These commands are reserved and treated by the device as no operation

These devices support two types of data transfer operations: *data write* (the host controller configures the device), and *data read* (the host controller reads data from the device).

Any data write to the device is always synchronous to the external clock provided on the SCLK pin. The WR\_REG command writes the 8-bit data into the 9-bit address specified in the command string. The CLR\_BITS command clears the specified bits (identified by 1) at the 9-bit address (without affecting the other bits), and the SET\_BITS command sets the specified bits (identified by 1) at the 9-bit address (without affecting the other bits).

The data read from the device can be synchronized to the same external clock or to an internal clock of the device by programming the configuration registers (see the [Data Transfer Protocols](#) section for details).

### 7.5.1 Output Data Word

In any data transfer frame, the contents of an internal, 22-bit, output data word are shifted out on the SDO pins. The D[21:4] bits of the 22-bit output data word for any frame  $F + 1$ , are determined by:

- Value of the DATA\_VAL bit applicable to frame  $F + 1$  (see the [DATA\\_CNTL register](#))
- The command issued in frame  $F$

If a valid RD\_REG command is executed in frame  $F$ , then the D[21:14] bits in frame  $F + 1$  reflect the contents of the selected register, and the D[13:0] bits are zeros.

If the DATA\_VAL bit for frame  $F + 1$  is set to 1, then the D[21:4] bits in frame  $F + 1$  are replaced by the DATA\_PATN[17:0] bits.

For all other combinations, the D[21:4] bits for frame  $F + 1$  are the latest conversion result.

[Figure 41](#) shows the output data word. [Figure 42](#) shows further details of the parity computation unit illustrated in [Figure 41](#).

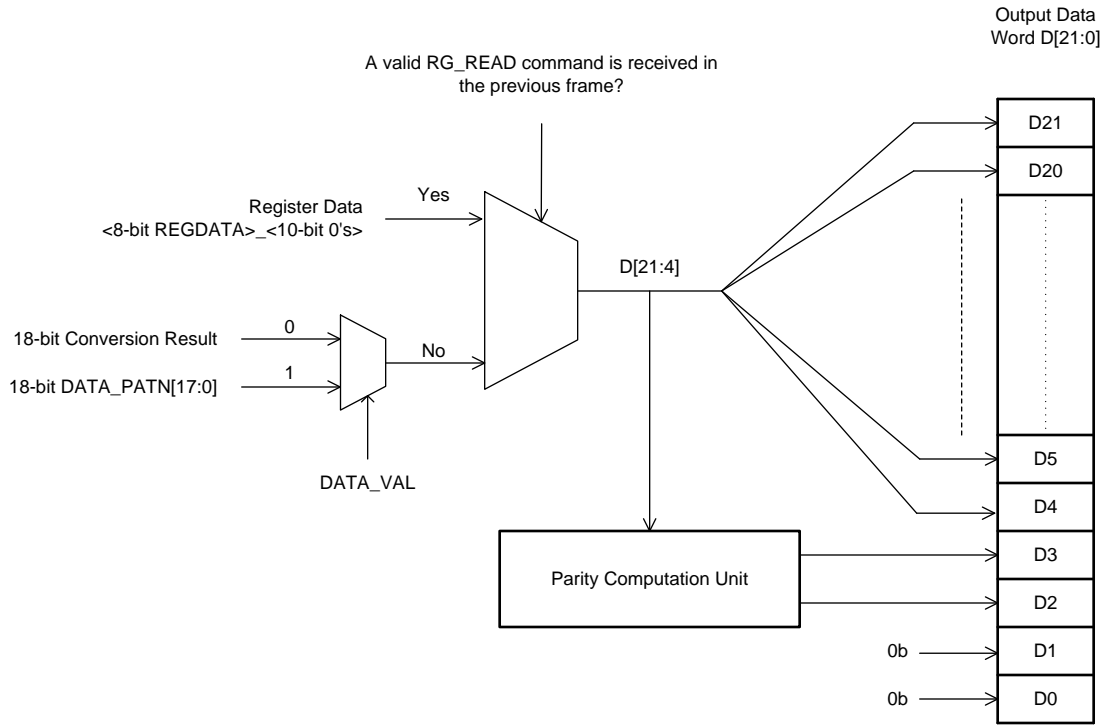
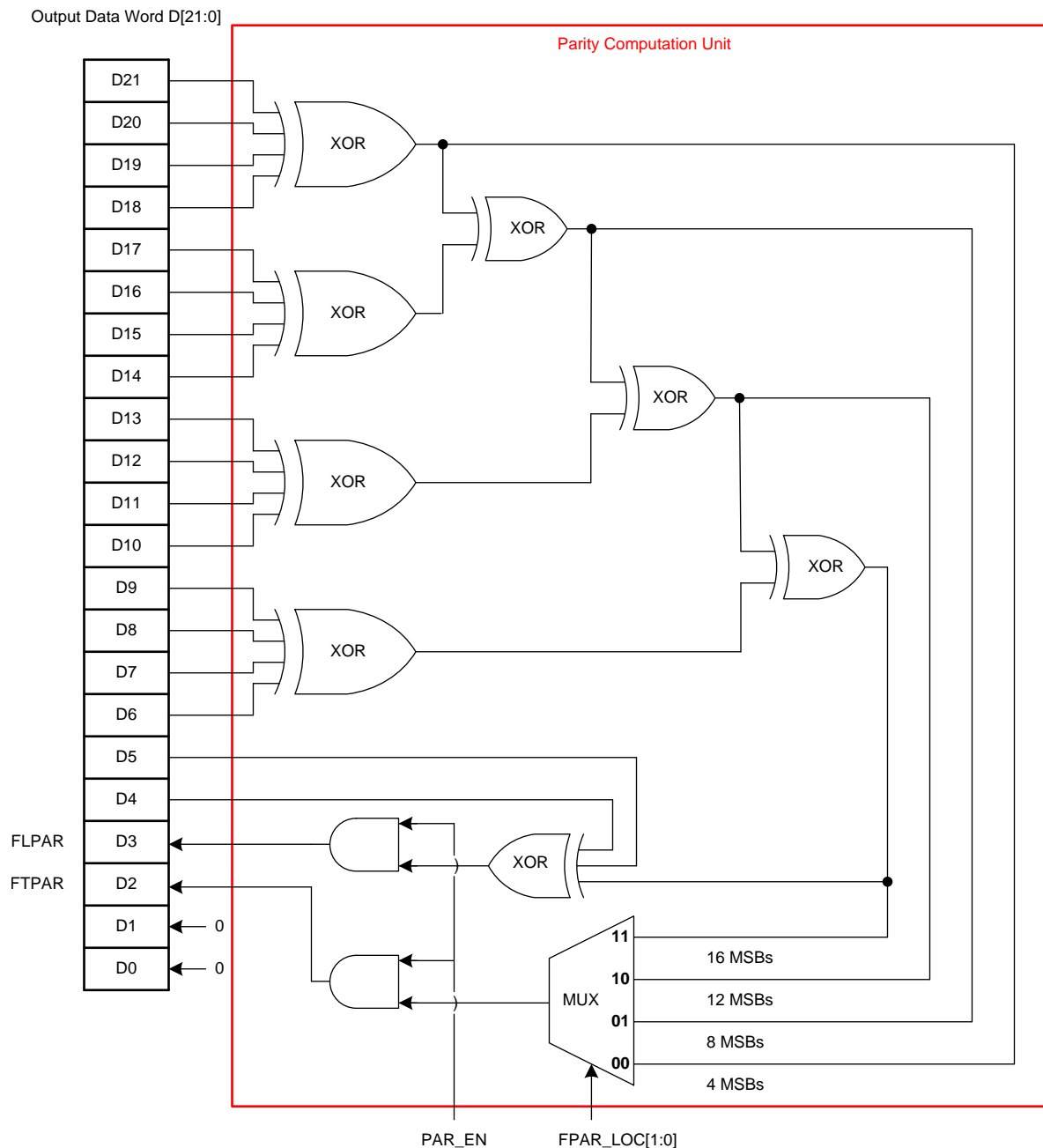


Figure 41. Output Data Word (D[21:0])



**Figure 42. Parity Bits Computation**

With the PAR\_EN bit set to 0, the D[3] and D[2] bits of the output data word are set to 0 (default configuration).

When the PAR\_EN bit is set to 1, the device calculates the parity bits (FLPAR and FTPAR) and appends them as bits D[3] and D[2].

- FLPAR is the even parity calculated on bits D[21:4].
- FTPAR is the even parity calculated on the bits defined by FPAR\_LOC[1:0].

See the [DATA\\_CNTL register](#) for more details on the FPAR\_LOC[1:0] bit settings. Bits D[1:0] are set to 00b.

## 7.5.2 Data Transfer Frame

A data transfer frame between the device and the host controller is bounded between a  $\overline{\text{CS}}$  falling edge and the subsequent  $\overline{\text{CS}}$  rising edge. The host controller can initiate a data transfer frame (as shown in Figure 43) at any time irrespective of the status of the CONVST signal; however, the data read during such a data transfer frame is a function of relative timing between the CONVST and  $\overline{\text{CS}}$  signals.

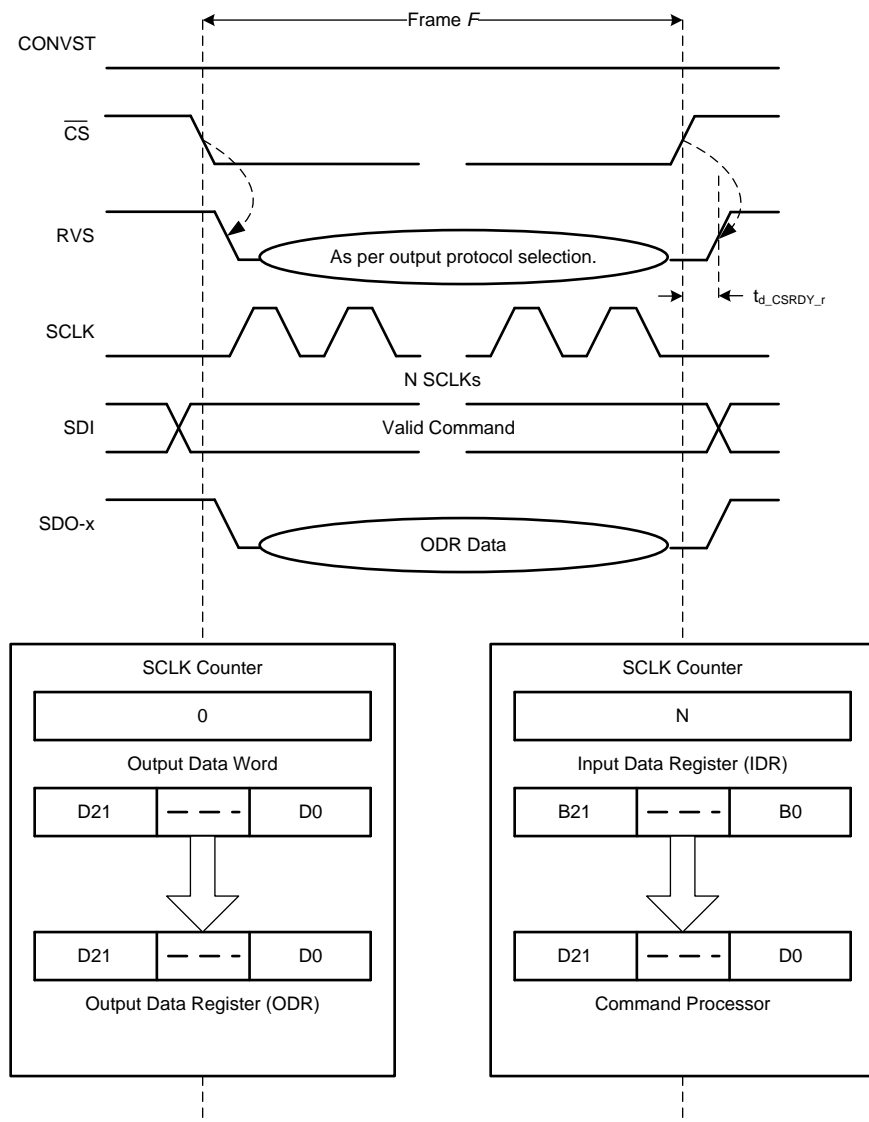


Figure 43. Data Transfer Frame

For this discussion, assume that the CONVST signal remains low.

A typical data transfer frame  $F$  follows this order:

1. The host controller pulls  $\overline{\text{CS}}$  low to initiate a data transfer frame. On the  $\overline{\text{CS}}$  falling edge:
  - RVS goes low, indicating the beginning of the data transfer frame.
  - The SCLK counter is reset to 0.
  - The device takes control of the data bus. As shown in Figure 43, the 22-bit contents of the output data word (see Figure 41) are loaded in to the 22-bit output data register (ODR; see Figure 37).
  - The 22-bit input data register (IDR; see Figure 37) is reset to 00000h, corresponding to a NOP command.

2. During the frame, the host controller provides clocks on the SCLK pin. Inside the device:
  - For each SCLK capture edge, the SCLK counter is incremented and the data bit received on the SDI pin is shifted in to the IDR.
  - For each launch edge of the output clock (SCLK in this case), ODR data are shifted out on the selected SDO-x pins.
  - The status of the RVS pin depends on the output protocol selection (see the [Protocols for Reading From the Device](#) section).
3. The host controller pulls  $\overline{CS}$  high to end the data transfer frame. On the  $\overline{CS}$  rising edge:
  - The SDO-x pins go to Hi-Z.
  - RVS goes high (after a delay of  $t_{d\_CSRDY\_r}$ ).
  - As illustrated in [Figure 43](#), the 22-bit contents of the IDR are transferred to the command processor (see [Figure 37](#)) for decoding and further action.

After pulling  $\overline{CS}$  high, the host controller monitors for a low-to-high transition on the RVS pin, or waits for the  $t_{d\_CSRDY\_r}$  time (see the [Switching Characteristics](#) table) to elapse before initiating a new operation (data transfer or conversion). The delay,  $t_{d\_CSRDY\_r}$ , for any data transfer frame  $F$  varies based on the data transfer operation executed in frame  $F$ .

At the end of data transfer frame  $F$ :

- If the SCLK counter is  $< 22$ , then the IDR captured less than 22 bits from the SDI. In this case, the device treats frame  $F$  as a *short command frame*. At the end of a short command frame, the IDR is not updated and the device treats the frame as a no operation (NOP) command.
- If the SCLK counter = 22, then the IDR captured exactly 22 bits from SDI. In this case, the device treats the frame  $F$  as a *optimal command frame*. At the end of an optimal command frame, the command processor decodes the 22-bit contents of the IDR as a valid command word.
- If the SCLK counter  $> 22$ , then the IDR captured more than 22 bits from the SDI; however, only the *last 22 bits* are retained. In this case, the device treats frame  $F$  as a *long command frame*. At the end of a long command frame, the command processor treats the 22-bit contents of the IDR as a valid command word. There is no restriction on the maximum number of clocks that can be provided within any data transfer frame  $F$ . However, as explained above, make sure that the last 22 bits shifted into the device before the  $\overline{CS}$  rising edge constitute the desired command.

In a short command frame, the write operation to the device is invalidated; however, the output data bits transferred during the short command frame are still valid output data. Therefore, the host controller can use such shorter data transfer frames to read only the required number of MSB bits from the 22-bit output data word. As shown in [Figure 41](#), an *optimal read frame* for the ADS891xB devices must read only the 18 MSB bits of the output data word. The length of an optimal read frame depends on the output protocol selection; see the [Protocols for Reading From the Device](#) section for more details.

---

#### NOTE

The previous example shows data-read and data-write operations synchronous to the external clock provided on the SCLK pin.

However, the device also supports data read operation synchronous to the internal clock; see the [Protocols for Reading From the Device](#) section for more details. In this case, while the ODR contents are shifted on the SDO (or SDOs) on the launch edge of the internal clock, the device continues to capture the SDI data into the IDR (and increment the SCLK counter) on SCLK capture edges.

---

### 7.5.3 Interleaving Conversion Cycles and Data Transfer Frames

The host controller operates the device at the desired throughput by interleaving the conversion cycles and the data transfer frames.

The cycle time of the device,  $t_{\text{cycle}}$ , is the time difference between two consecutive CONVST rising edges provided by the host controller. The response time of the device,  $t_{\text{resp}}$ , is the time difference between the host controller initiating conversion C, and the host controller receiving the complete result for conversion C.

Figure 44 shows three conversion cycles: C, C + 1, and C + 2. Conversion C is initiated by a CONVST rising edge at time  $t = 0$ , and the conversion result becomes available for data transfer at  $t_{\text{conv}}$ . However, this result is loaded into the ODR only on the subsequent CS falling edge. This CS falling edge must be provided before the completion of conversion C + 1 (that is, before  $t_{\text{cycle}} + t_{\text{conv}}$ ).

To achieve the rated performance specifications, the host controller must make sure that no digital signals toggle during the quiet acquisition time ( $t_{\text{qt\_acq}}$ ) and quiet aperture time ( $t_{\text{d\_cnvcap}}$ ). Any noise during  $t_{\text{d\_cnvcap}}$  may negatively affect the result of the ongoing conversion, whereas any noise during  $t_{\text{qt\_acq}}$  may negatively affect the result of the subsequent conversion.

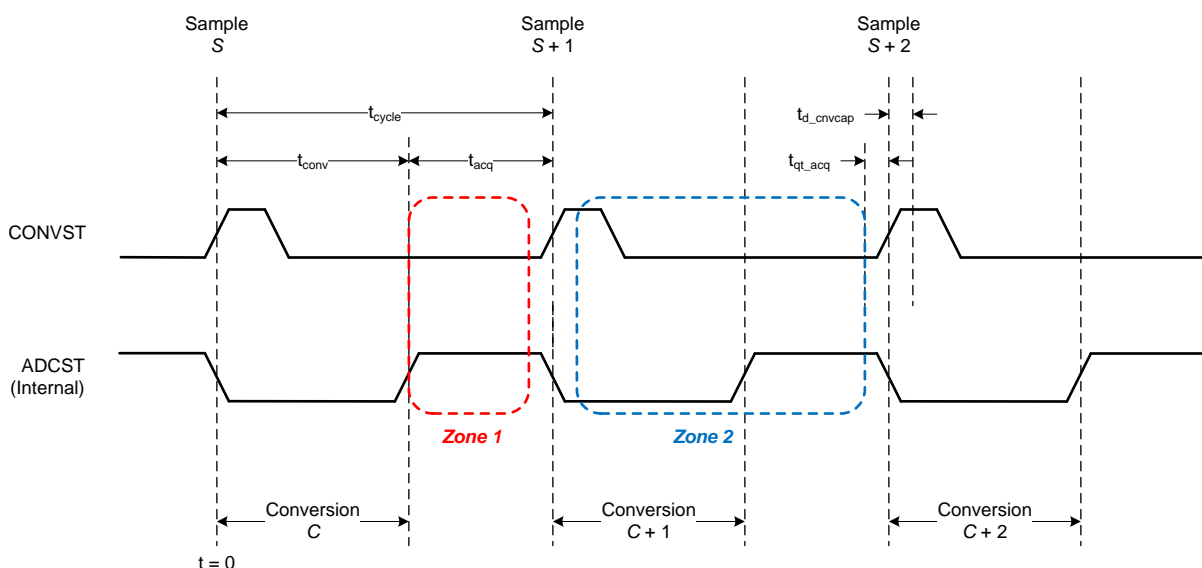


Figure 44. Data Transfer Zones

This architecture allows for two distinct time zones (zone 1 and zone 2) to transfer data for each conversion. Zone 1 and zone 2 for conversion C are defined in Table 3.

Table 3. Data Transfer Zones Timing

ZONE	STARTING TIME	ENDING TIME
Zone 1 for conversion C	$t_{\text{conv}}$	$t_{\text{cycle}} - t_{\text{qt\_acq}}$
Zone 2 for conversion C	$t_{\text{cycle}} + t_{\text{d\_cnvcap}}$	$t_{\text{cycle}} + t_{\text{cycle}} - t_{\text{qt\_acq}}$

The response time includes the conversion time and the data transfer time, and thus is a function of the selected data transfer zone.

Figure 45 and Figure 46 illustrate interleaving of three conversion cycles (C, C + 1, and C + 2) with three data transfer frames (F, F + 1, and F + 2) in zone 1 and in zone 2, respectively.

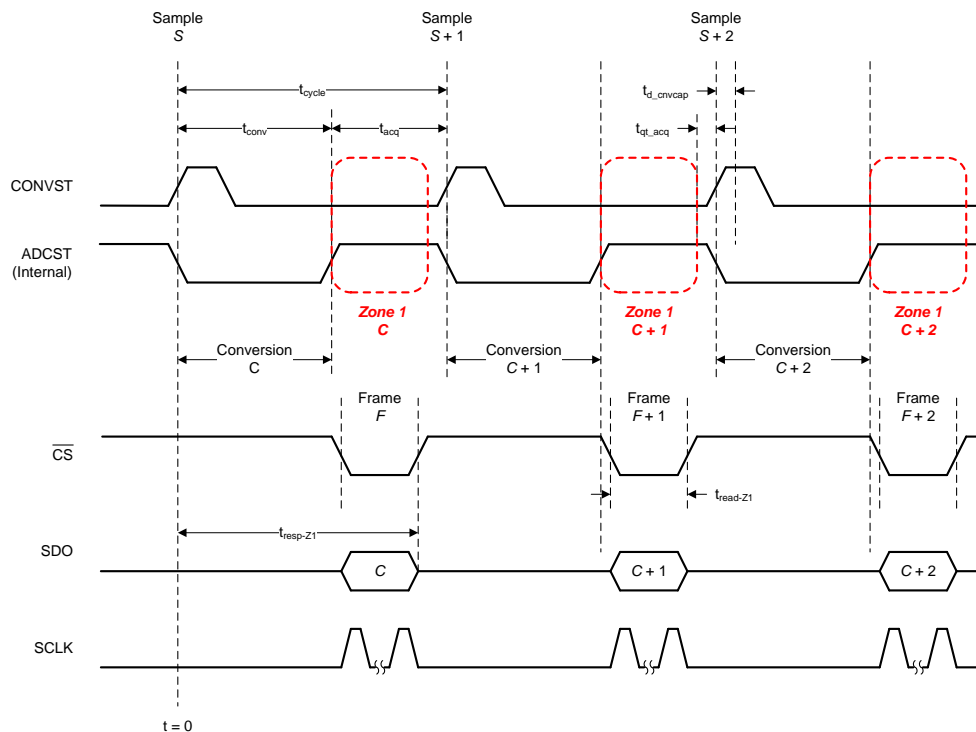


Figure 45. Zone 1 Data Transfer

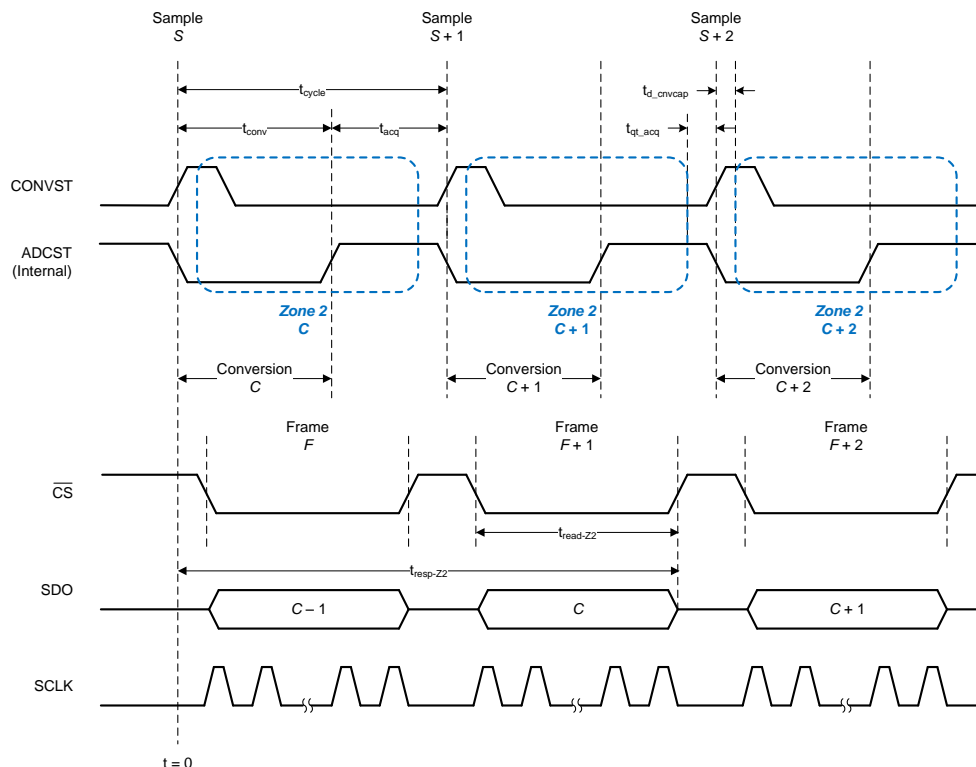


Figure 46. Zone 2 Data Transfer

To achieve cycle time  $t_{\text{cycle}}$ , the read time in zone 1 is given by Equation 5:

$$t_{\text{read-Z1}} \leq t_{\text{cycle}} - t_{\text{conv}} - t_{\text{qt\_acq}} \quad (5)$$

For an optimal data transfer frame, Equation 5 results in an SCLK frequency given by Equation 6:

$$f_{\text{SCLK}} \geq \frac{18}{t_{\text{read-Z1}}} \quad (6)$$

Then, the zone 1 data transfer achieves a response time defined by Equation 7:

$$t_{\text{resp-Z1-min}} = t_{\text{conv}} + t_{\text{read-Z1}} \quad (7)$$

At lower SCLK speeds,  $t_{\text{read-Z1}}$  increases, resulting in slower response times and higher cycle times.

To achieve the same cycle time,  $t_{\text{cycle}}$ , the read time in zone 2 is given by Equation 8:

$$t_{\text{read-Z2}} \leq t_{\text{cycle}} - t_{\text{d\_cnvcap}} - t_{\text{qt\_acq}} \quad (8)$$

For an optimal data transfer frame, Equation 8 results in an SCLK frequency given by Equation 9:

$$f_{\text{SCLK}} \geq \frac{18}{t_{\text{read\_Z2}}} \quad (9)$$

Then, the zone 2 data transfer achieves a response time defined by Equation 10:

$$t_{\text{resp-Z2-min}} = t_{\text{cycle}} + t_{\text{d\_cnvcap}} + t_{\text{read-Z2}} \quad (10)$$

Any increase in  $t_{\text{read-Z2}}$  increases response time and may increase cycle time.

For a given cycle time, the zone 1 data transfer clearly achieves faster response time, but also requires a higher SCLK speed (as evident from Equation 5, Equation 6, and Equation 7); whereas, the zone 2 data transfer clearly requires a lower SCLK speed but has a slower response time (as evident from Equation 8, Equation 9, and Equation 10). For more information about benefits of zone 2 data transfer when using isolated digital interface or MCU refer to TI TechNote - Simplify Isolation Designs Using an Enhanced-SPI ADC Interface.

---

**NOTE**

A data transfer frame can begin in zone 1, and then extend into zone 2; however, the host controller must make sure that no digital transitions occur during the  $t_{\text{qt\_acq}}$  and  $t_{\text{d\_cnvcap}}$  time intervals.

---

**NOTE**

For data transfer operations in zone 2 using the ADC-Clock-Master protocol (SDO\_MODE[1:0] = 11b), the device supports only the external-clock-echo option (SSYNC\_CLK\_SEL[1:0] = 00b); see Table 9.

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#### 7.5.4 Data Transfer Protocols

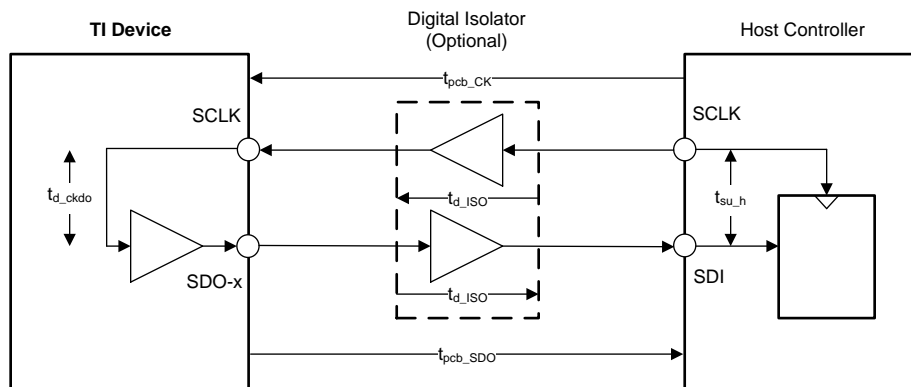
This device family features a multiSPI digital interface that allows the host controller to operate at slower SCLK speeds and still achieve the required throughput and response time. The multiSPI digital interface module offers three options to reduce the SCLK speed required for data transfer:

- Increase the width of the output data bus.
- Enable double data rate (DDR) transfer.
- Extended data transfer window, as shown in Figure 46.

These three options can be combined to achieve further reduction in SCLK speed.

There are various factors that limit the maximum SCLK frequency in a system.

Figure 47 shows the delays in the communication channel between the host controller and the device in a typical serial communication.



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Figure 47. Delays in Serial Communication

For example, if  $t_{pcb\_CK}$  and  $t_{pcb\_SDO}$  are the delays introduced by the printed circuit board (PCB) traces for the serial clock and SDO signals,  $t_{d\_CKDO}$  is the clock-to-data delay of the device,  $t_{d\_ISO}$  is the propagation delay introduced by the digital isolator, and  $t_{su\_h}$  is the setup time specification of the host controller, then the total delay in the path is given by Equation 11:

$$t_{d\_total\_serial} = t_{pcb\_CK} + t_{d\_iso} + t_{d\_ckdo} + t_{d\_iso} + t_{pcb\_SDO} + t_{su\_h} \quad (11)$$

In a standard SPI protocol, the host controller and the device launch and capture data bits on alternate SCLK edges. Therefore, the  $t_{d\_total\_serial}$  delay must be kept to less than half of the SCLK duration. Equation 12 shows the fastest clock allowed by the SPI protocol:

$$f_{clk-SPI} \leq \frac{1}{2 \times t_{d\_total\_serial}} \quad (12)$$

Larger values of the  $t_{d\_total\_serial}$  delay restricts the maximum SCLK speed for the SPI protocol, resulting in higher read and response times, and can possibly limit the throughput.

Figure 48 shows a delay ( $t_{d\_delcap}$ ) introduced in the capture path (inside the host controller).

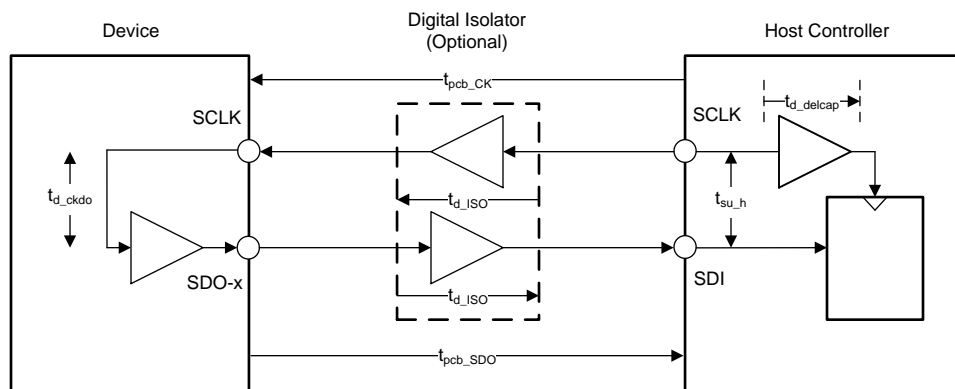


Figure 48. Delayed Capture

The total delay in the path modifies to Equation 13:

$$t_{d\_total\_serial} = t_{pcb\_CK} + t_{d\_iso} + t_{d\_ckdo} + t_{d\_iso} + t_{pcb\_SDO} + t_{su\_h} - t_{d\_delcap} \quad (13)$$

This reduction in total delay allows the SPI protocol to operate at higher clock speeds.

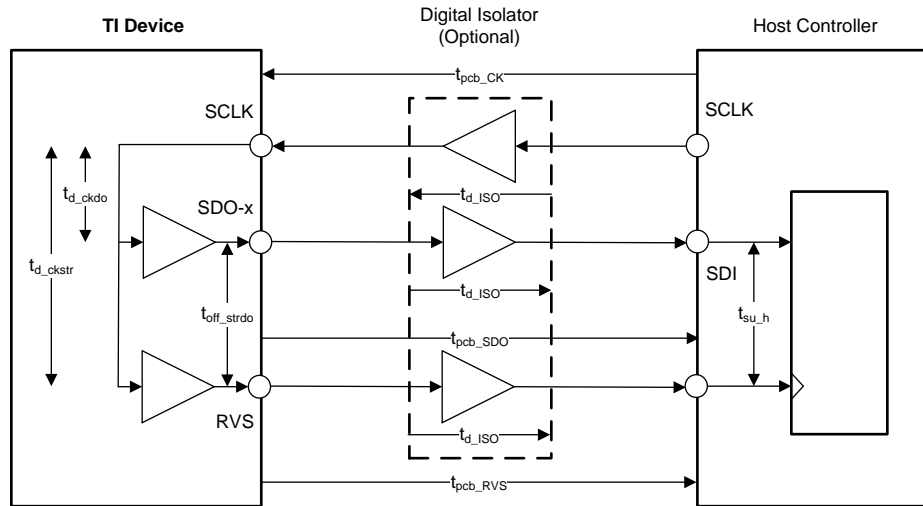
The multiSPI digital interface module offers two additional options to remove the restriction on the SCLK speed:

- Early data launch (EDL) mode of operation  
 In EDL mode, the device launches the output data on SDO-x pin (or pins) half a clock earlier compared to the standard SPI protocol. Therefore, Equation 12 modifies to Equation 14:

$$f_{\text{clk-SPI}} \leq \frac{1}{t_{\text{d\_total-serial}}} \quad (14)$$

The reduction in total delay allows the serial interface to operate at higher clock speeds.

- ADC-Clock-Master (*source-synchronous*) mode of operation  
 As illustrated in Figure 49, in ADC-Clock-Master mode, the device provides a synchronous output clock (on the RVS pin) along with the output data (on the SDO-x pins).



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**Figure 49. Delays in ADC-Clock-Master (Source-Synchronous) Mode**

For negligible values of  $t_{\text{off\_STRDO}}$ , the total delay in the path for a source-synchronous data transfer, is given by Equation 15:

$$t_{\text{d\_total\_srcsync}} = t_{\text{pcb\_RVS}} - t_{\text{pcb\_SDO}} + t_{\text{su\_h}} \quad (15)$$

As shown by the difference between Equation 11 and Equation 15, using ADC-Clock-Master mode completely eliminates the effect of isolator delays ( $t_{\text{d\_ISO}}$ ) and clock-to-data delays ( $t_{\text{d\_CKDO}}$ ); typically, the largest contributors in the overall delay computation.

Furthermore, the actual values of  $t_{\text{pcb\_RVS}}$  and  $t_{\text{pcb\_SDO}}$  do not matter. In most cases, the  $t_{\text{d\_total\_srcsync}}$  delay can be kept at a minimum by routing the RVS and SDO lines together on the PCB. Therefore, the ADC-Clock-Master mode allows the data transfer between the host controller and the device to operate at much higher SCLK speeds. For more information about using ADC-Clock-Master mode to achieve fast SCLK speeds, with an isolated interface or high routing delays, see *Optimizing Data Transfer on High-Resolution, High Throughput Data Converters*. Zone 2 data transfer also enables longer quiet time for analog input settling, and is discussed in *Improving Input Settling for Precision Data Converters*.

### 7.5.4.1 Protocols for Configuring the Device

As shown in [Table 4](#), the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to write data to the device.

**Table 4. SPI Protocols for Configuring the Device**

PROTOCOL	SCLK POLARITY (At CS Falling Edge)	SCLK PHASE (Capture Edge)	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Command Frame)	TIMING DIAGRAM
SPI-00-S	Low	Rising	00h	00h	22	<a href="#">Figure 50</a>
SPI-01-S	Low	Falling	01h	00h	22	<a href="#">Figure 51</a>
SPI-10-S	High	Falling	02h	00h	22	<a href="#">Figure 52</a>
SPI-11-S	High	Rising	03h	00h	22	<a href="#">Figure 53</a>

At power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data-read and data-write operations.

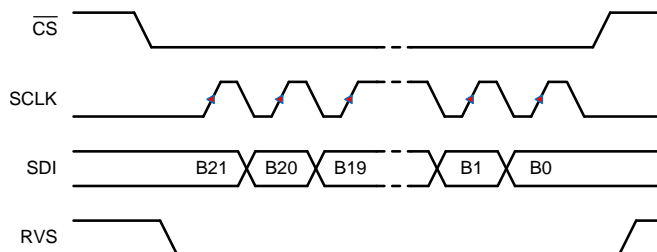
To select a different SPI-compatible protocol, program the SDI\_MODE[1:0] bits in the [SDI\\_CNTL register](#). This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.

[Figure 50](#) to [Figure 53](#) detail the four protocols using an optimal command frame; see the [Timing Requirements](#) and [Switching Characteristics](#) tables for associated timing parameters.

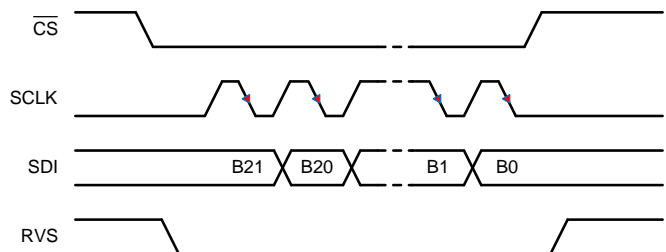
**NOTE**

As explained in the [Data Transfer Frame](#) section, a valid write operation to the device requires a minimum of 22 SCLKs to be provided within a data transfer frame.

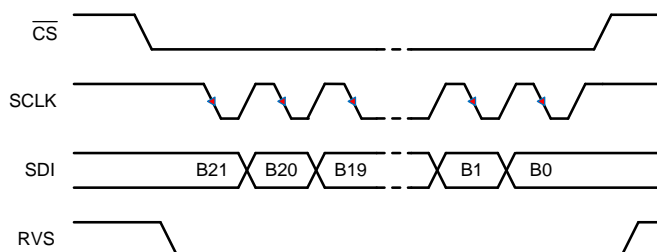
Any data write operation to the device must continue to follow the SPI-compatible protocol selected in the [SDI\\_CNTL register](#), irrespective of the protocol selected for the data-read operation.



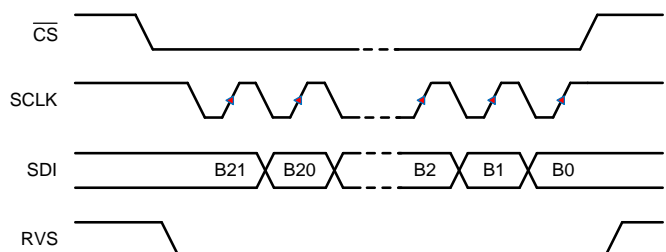
**Figure 50. SPI-00-S Protocol, Optimal Command Frame**



**Figure 51. SPI-01-S Protocol, Optimal Command Frame**



**Figure 52. SPI-10-S Protocol, Optimal Command Frame**



**Figure 53. SPI-11-S Protocol, Optimal Command Frame**

### 7.5.4.2 Protocols for Reading From the Device

The protocols for the data-read operation can be broadly classified into three categories:

1. Legacy, SPI-compatible (SPI-xy-S) protocol
2. SPI-compatible protocols with bus width options (SPI-xy-D and SPI-xy-Q)
3. Source-synchronous (SRC) protocols

#### 7.5.4.2.1 Legacy, SPI-Compatible (SYS-xy-S) Protocols

As shown in [Table 5](#), the host controller can use any of the four legacy, SPI-compatible protocols (SPI-00-S, SPI-01-S, SPI-10-S, or SPI-11-S) to read data from the device.

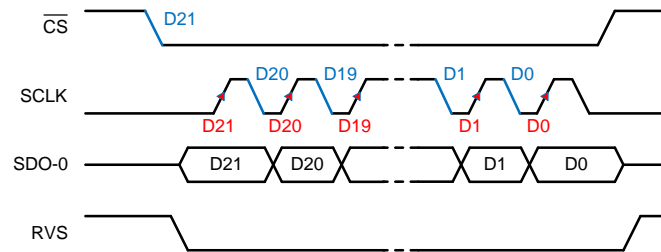
**Table 5. SPI Protocols for Reading From the Device**

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00-S	Low	Rising	$\overline{CS}$ falling	00h	00h	18	<a href="#">Figure 54</a>
SPI-01-S	Low	Falling	1 <sup>st</sup> SCLK rising	01h	00h	18	<a href="#">Figure 55</a>
SPI-10-S	High	Falling	$\overline{CS}$ falling	02h	00h	18	<a href="#">Figure 56</a>
SPI-11-S	High	Rising	1 <sup>st</sup> SCLK falling	03h	00h	18	<a href="#">Figure 57</a>

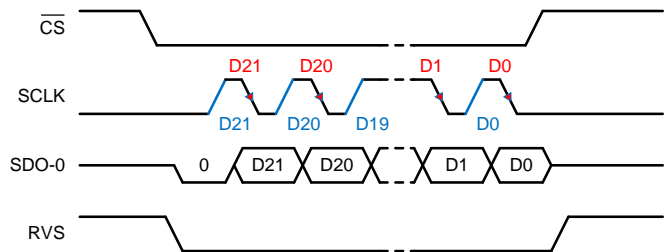
At power-up or after coming out of any asynchronous reset, the device supports the SPI-00-S protocol for data-read and data-write operations. To select a different SPI-compatible protocol for both the data transfer operations:

1. Program the SDI\_MODE[1:0] bits in the [SDI\\_CNTL register](#). This first write operation must adhere to the SPI-00-S protocol. Any subsequent data transfer frames must adhere to the newly selected protocol.
2. Set the SDO\_MODE[1:0] bits = 00b in the [SDO\\_CNTL register](#).

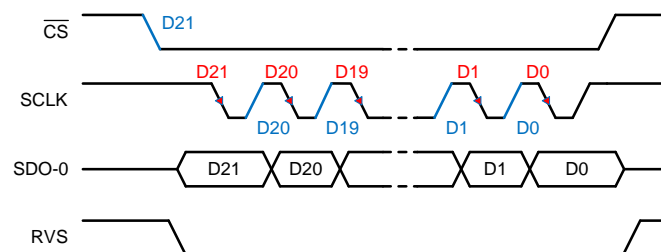
[Figure 54](#) to [Figure 57](#) explain the details of the four protocols using an optimal command frame to read all 22 bits of the output data word. [Table 5](#) shows the number of SCLK required in an optimal read frame for the different output protocol selections.



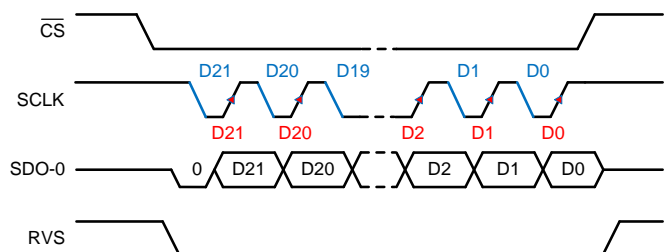
**Figure 54. SPI-00-S Protocol, 22 SCLKs**



**Figure 55. SPI-01-S Protocol, 22 SCLKs**



**Figure 56. SPI-10-S Protocol, 22 SCLKs**



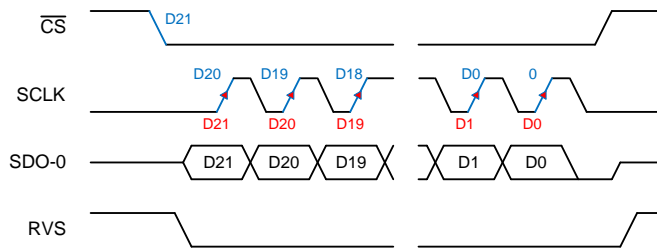
**Figure 57. SPI-11-S Protocol, 22 SCLKs**

For SDI\_MODE[1:0] = 00b or 10b, the device supports an *Early Data Launch* (EDL) option. Set SDO\_MODE[1:0] = 01b in the [SDO\\_CNTL register](#) to enable the feature (see [Table 6](#)). Setting SDO\_MODE[1:0] = 01b has no effect if SDI\_MODE[1:0] = 01b or 11b.

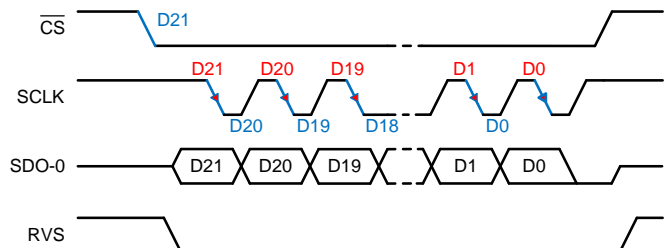
**Table 6. SPI Protocols with Early Data Launch**

PROTOCOL	SCLK POLARITY (At $\overline{CS}$ Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00-S-EDL	Low	Rising	$\overline{CS}$ falling	00h	01h	18	<a href="#">Figure 54</a>
SPI-10-S-EDL	High	Falling	$\overline{CS}$ falling	02h	01h	18	<a href="#">Figure 56</a>

As shown in [Figure 58](#), and [Figure 59](#), the device launches the output data bit on the SDO-0 pin half clock earlier compared to the standard SPI protocol.



**Figure 58. SPI-00-S-EDL Protocol, 22 SCLKs**



**Figure 59. SPI-10-S-EDL Protocol, 22 SCLKs**

When using these SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the [Timing Requirements](#) and [Switching Characteristics](#) tables for associated timing parameters.

With SDO\_CNTL[7:0] = 00h or 01h, if the host controller uses a long data transfer frame, the device exhibits daisy-chain operation (see the [Multiple Devices: Daisy-Chain Topology](#) section).

**NOTE**

Use SPI-compatible protocols to execute the RD\_REG, WR\_REG, CLR\_BITS, and SET\_BITS commands specified in [Table 2](#).

### 7.5.4.2.2 SPI-Compatible Protocols with Bus Width Options

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or four bits (quad SDO) when operating with any of the four legacy, SPI-compatible protocols.

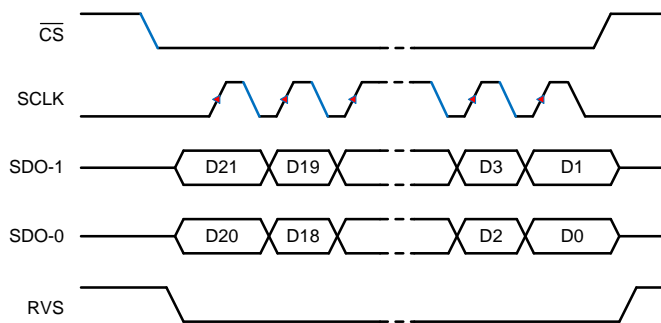
Set the SDO\_WIDTH[1:0] bits in the [SDO\\_CNTL register](#) to select the SDO bus width. The SCLK launch edge depends on the SPI protocol selection (as shown in [Table 7](#)).

**Table 7. SPI-Compatible Protocols with Bus Width Options**

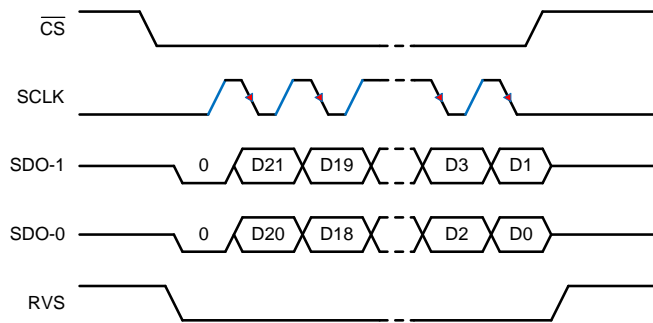
PROTOCOL	SCLK POLARITY (At CS Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	#SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00-D	Low	Rising	$\overline{CS}$ falling	00h	08h	9	<a href="#">Figure 60</a>
SPI-01-D	Low	Falling	First SCLK rising	01h	08h	9	<a href="#">Figure 61</a>
SPI-10-D	High	Falling	$\overline{CS}$ falling	02h	08h	9	<a href="#">Figure 62</a>
SPI-11-D	High	Rising	First SCLK falling	03h	08h	9	<a href="#">Figure 63</a>
SPI-00-Q	Low	Rising	$\overline{CS}$ falling	00h	0Ch	5	<a href="#">Figure 64</a>
SPI-01-Q	Low	Falling	First SCLK rising	01h	0Ch	5	<a href="#">Figure 65</a>
SPI-10-Q	High	Falling	$\overline{CS}$ falling	02h	0Ch	5	<a href="#">Figure 66</a>
SPI-11-Q	High	Rising	First SCLK falling	03h	0Ch	5	<a href="#">Figure 67</a>

In dual-SDO mode (SDO\_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK launch edge.

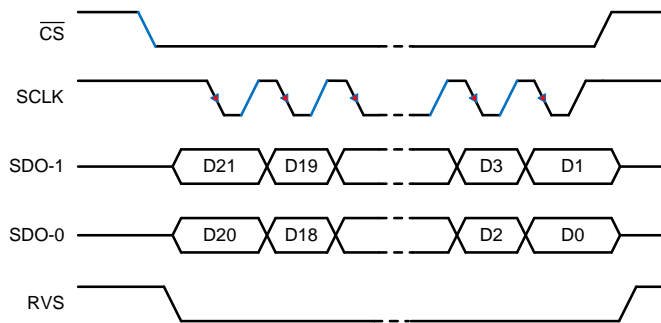
In quad-SDO mode (SDO\_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK launch edge.



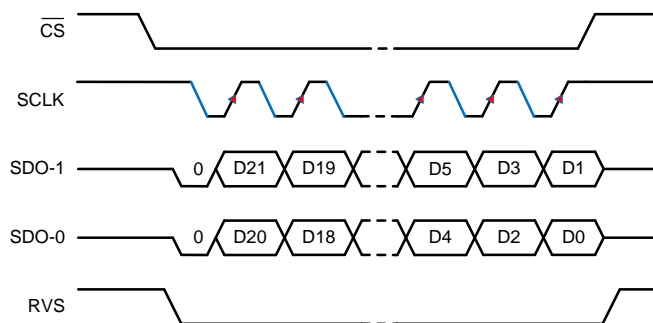
**Figure 60. SPI-00-D Protocol**



**Figure 61. SPI-01-D Protocol**



**Figure 62. SPI-10-D Protocol**



**Figure 63. SPI-11-D Protocol**

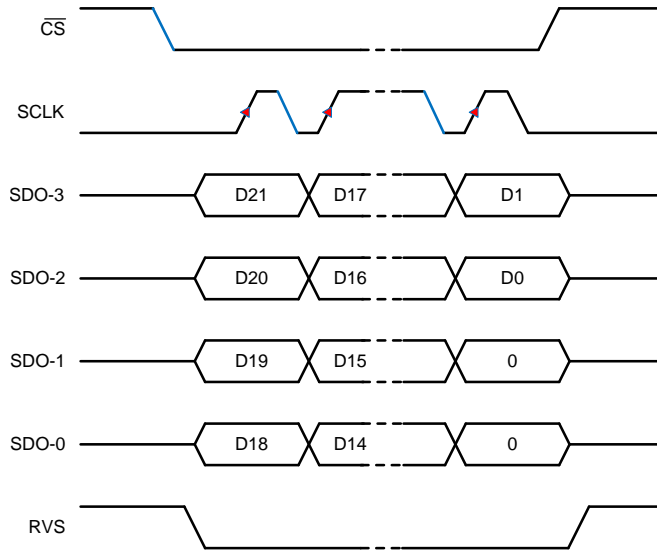


Figure 64. SPI-00-Q Protocol

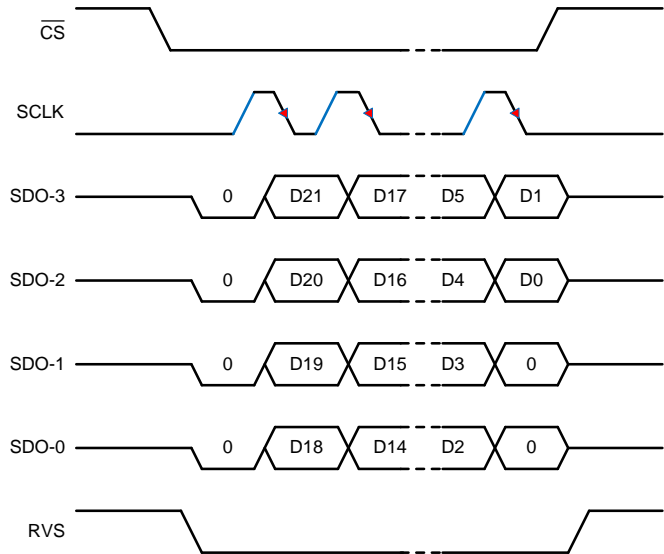


Figure 65. SPI-01-Q Protocol

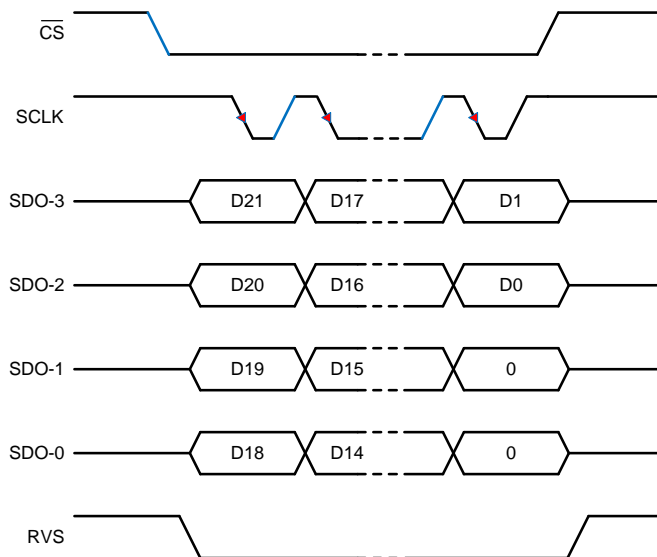


Figure 66. SPI-10-Q Protocol

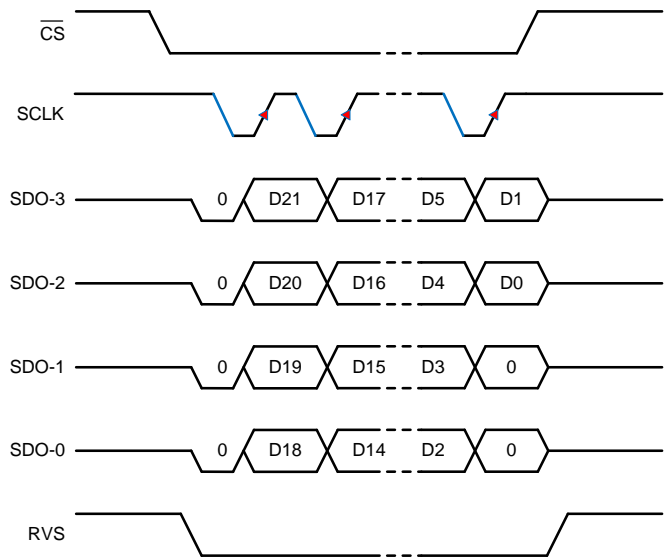


Figure 67. SPI-11-Q Protocol

For SDI\_MODE[1:0] = 00b or 10b, the device supports an early data launch (EDL) option. Set SDO\_MODE[1:0] = 01b in the [SDO\\_CNTL register](#) to enable the feature (see [Table 8](#)). Setting SDO\_MODE[1:0] = 01b has no effect if SDI\_MODE[1:0] = 01b or 11b.

Table 8. SPI Protocols with Early Data Launch

PROTOCOL	SCLK POLARITY (At CS Falling Edge)	SCLK PHASE (Capture Edge)	MSB BIT LAUNCH EDGE	SDI_CNTL	SDO_CNTL	NO. OF SCLK (Optimal Read Frame)	TIMING DIAGRAM
SPI-00-D-EDL	Low	Rising	CS falling	00h	09h	9	<a href="#">Figure 60</a>
SPI-10-D-EDL	High	Falling	CS falling	02h	09h	9	<a href="#">Figure 62</a>
SPI-00-Q-EDL	Low	Rising	CS falling	00h	0Dh	5	<a href="#">Figure 64</a>
SPI-10-Q-EDL	High	Falling	CS falling	02h	0Dh	5	<a href="#">Figure 66</a>

As shown in [Figure 58](#), and [Figure 59](#), the device launches the output data bits on the SDO-x pins half clock earlier compared to the standard SPI protocol.

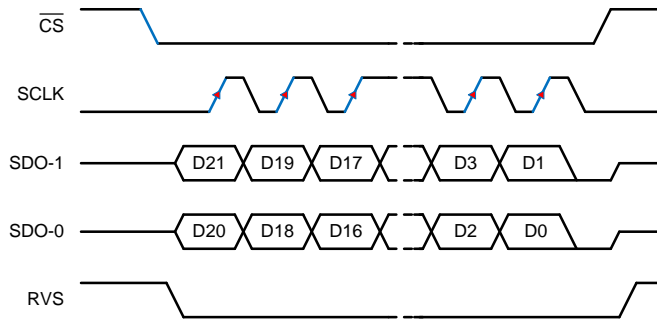


Figure 68. SPI-00-D-EDL Protocol

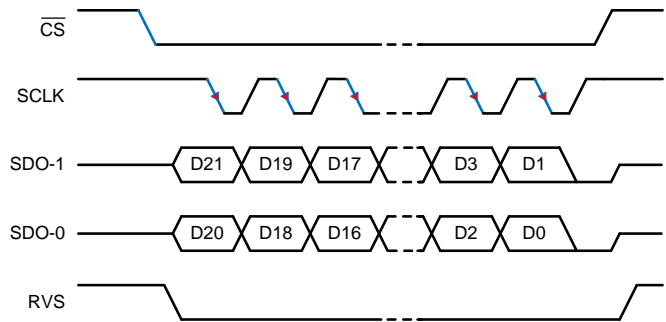


Figure 69. SPI-10-D-EDL Protocol

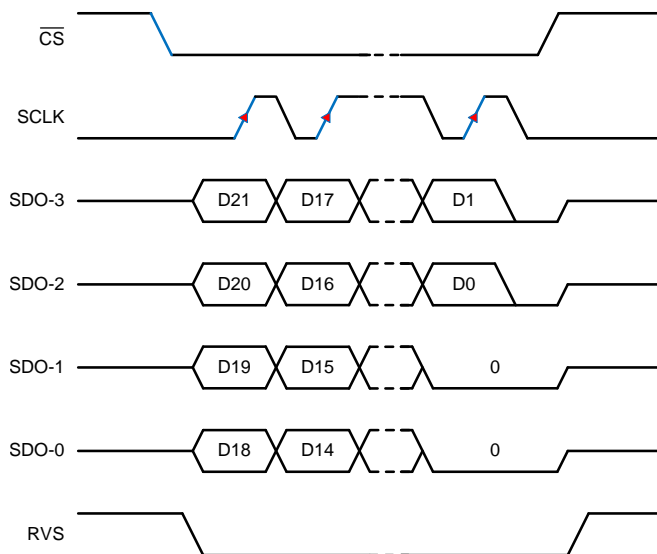


Figure 70. SPI-00-Q-EDL Protocol

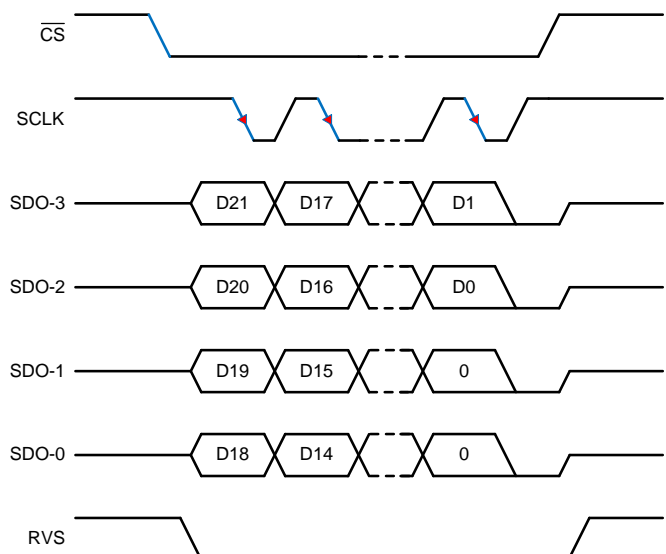


Figure 71. SPI-10-Q-EDL Protocol

When using any of the SPI-compatible protocols, the RVS output remains low throughout the data transfer frame; see the [Timing Requirements](#) and [Switching Characteristics](#) tables for associated timing parameters.

[Figure 60](#) to [Figure 71](#) illustrate how the wider data bus allows the host controller to read all 22 bits of the output data word using shorter data transfer frames. [Table 7](#) and [Table 8](#) show the number of SCLK required in an optimal read frame for the different output protocol selections.

**NOTE**

With SDO\_CNTL[7:0] ≠ 00h or 01h, a long data transfer frame does not result in daisy-chain operation. On SDO pin (or pins), the 22 bits of output data word are followed by zeros.

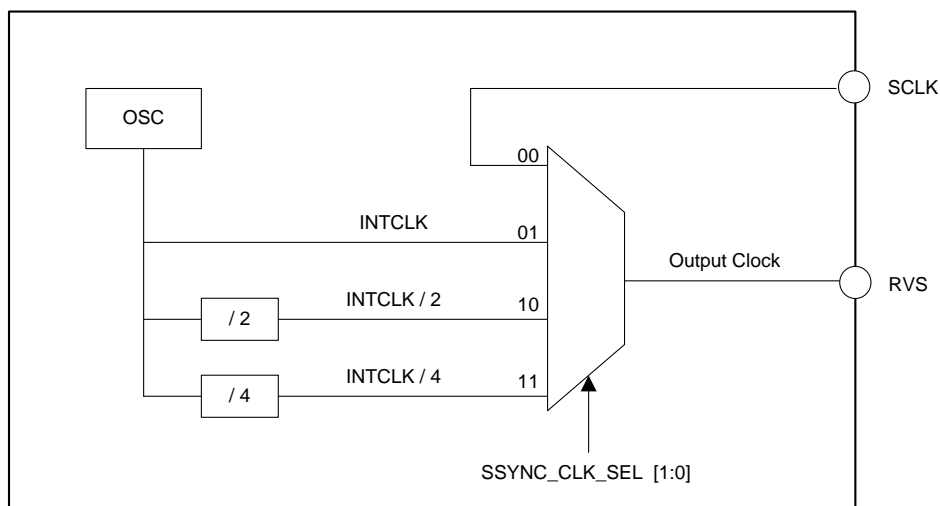
### 7.5.4.2.3 Source-Synchronous (SRC) Protocols

As described in the [Data Transfer Protocols](#) section, the multiSPI digital interface supports an ADC-Clock-Master or a *source-synchronous* mode of data transfer between the device and host controller. In this mode, the device provides an output clock that is synchronous with the output data. Furthermore, the host controller can also select the output clock source, data bus width, and data transfer rate.

#### 7.5.4.2.3.1 Output Clock Source Options with SRC Protocols

In all SRC protocols, the RVS pin provides the output clock. The device allows this output clock to be synchronous to either the external clock provided on the SCLK pin or to the internal clock of the device. Furthermore, this internal clock can be divided by a factor of two or four to lower the data rates.

As shown in [Figure 72](#), set the SSYNC\_CLK\_SEL[1:0] bits in the [SDO\\_CNTL](#) register to select the output clock source.



**Figure 72. Output Clock Source Options With SRC Protocols**

### 7.5.4.2.3.2 Bus Width Options With SRC Protocols

The device provides an option to increase the SDO bus width from one bit (default, single SDO) to two bits (dual SDO) or to four bits (quad SDO) when operating with any of the SRC protocols. Set the SDO\_WIDTH[1:0] bits in the SDO\_CNTL register to select the SDO bus width.

In dual-SDO mode (SDO\_WIDTH[1:0] = 10b), two bits of data are launched on the two SDO pins (SDO-0 and SDO-1) on every SCLK rising edge.

In quad-SDO mode (SDO\_WIDTH[1:0] = 11b), four bits of data are launched on the four SDO pins (SDO-0, SDO-1, SDO-2, and SDO-3) on every SCLK rising edge.

### 7.5.4.2.3.3 Output Data Rate Options With SRC Protocols

The device provides an option to transfer the data to the host controller at a single data rate (default, SDR) or at a double data rate (DDR). Set the DATA\_RATE bit in the SDO\_CNTL register to select the data transfer rate.

In SDR mode (DATA\_RATE = 0b), the RVS pin toggles from low to high, and the output data bits are launched on the SDO pins on the output clock rising edge.

In DDR mode (DATA\_RATE = 1b), the RVS pin toggles (from low-to-high or high-to-low), and the output data bits are launched on the SDO pins on every output clock edge, starting with the first rising edge.

The device supports all 24 combinations of output clock source, bus width, and output data rate, as shown in Table 9.

**Table 9. SRC Protocol Combinations**

PROTOCOL	OUTPUT CLOCK SOURCE	BUS WIDTH	OUTPUT DATA RATE	SDI_CNTL	SDO_CNTL	#OUTPUT CLOCK (Optimal Read Frame)	TIMING DIAGRAM
SRC-EXT-SS	SCLK <sup>(1)</sup>	Single	SDR	00h, 01h, 02h, or 03h <sup>(2)</sup>	03h	9	Figure 73
SRC-INT-SS	INTCLK <sup>(3)</sup>	Single	SDR		43h	9	Figure 74
SRC-IB2-SS	INTCLK / 2 <sup>(3)</sup>	Single	SDR		83h	9	
SRC-IB4-SS	INTCLK / 4 <sup>(3)</sup>	Single	SDR		C3h	9	
SRC-EXT-DS	SCLK <sup>(1)</sup>	Dual	SDR		0Bh	9	Figure 77
SRC-INT-DS	INTCLK <sup>(3)</sup>	Dual	SDR		4Bh	9	Figure 78
SRC-IB2-DS	INTCLK / 2 <sup>(3)</sup>	Dual	SDR		8Bh	9	
SRC-IB4-DS	INTCLK / 4 <sup>(3)</sup>	Dual	SDR		CBh	9	
SRC-EXT-QS	SCLK <sup>(1)</sup>	Quad	SDR		0Fh	5	Figure 81
SRC-INT-QS	INTCLK <sup>(3)</sup>	Quad	SDR		4Fh	5	Figure 82
SRC-IB2-QS	INTCLK / 2 <sup>(3)</sup>	Quad	SDR		8Fh	5	
SRC-IB4-QS	INTCLK / 4 <sup>(3)</sup>	Quad	SDR		CFh	5	
SRC-EXT-SD	SCLK <sup>(1)</sup>	Single	DDR		13h	9	Figure 75
SRC-INT-SD	INTCLK <sup>(3)</sup>	Single	DDR		53h	9	Figure 76
SRC-IB2-SD	INTCLK / 2 <sup>(3)</sup>	Single	DDR		93h	9	
SRC-IB4-SD	INTCLK / 4 <sup>(3)</sup>	Single	DDR		D3h	9	
SRC-EXT-DD	SCLK <sup>(1)</sup>	Dual	DDR		1Bh	5	Figure 79
SRC-INT-DD	INTCLK <sup>(3)</sup>	Dual	DDR		5Bh	5	Figure 80
SRC-IB2-DD	INTCLK / 2 <sup>(3)</sup>	Dual	DDR		9Bh	5	
SRC-IB4-DD	INTCLK / 4 <sup>(3)</sup>	Dual	DDR		DBh	5	
SRC-EXT-QD	SCLK <sup>(1)</sup>	Quad	DDR		1Fh	3	Figure 83
SRC-INT-QD	INTCLK <sup>(3)</sup>	Quad	DDR		5Fh	3	Figure 84
SRC-IB2-QD	INTCLK / 2 <sup>(3)</sup>	Quad	DDR		9Fh	3	
SRC-IB4-QD	INTCLK / 4 <sup>(3)</sup>	Quad	DDR		DFh	3	

(1) The EXTCLK option is not recommended when operating with DV<sub>DD</sub> < 2.35 V.

(2) Any of the four values can be used; see the [Protocols for Configuring the Device](#) section for more information.

(3) The device supports INTCLK, INTCLK / 2, and INTCLK / 4 options only for data transfer operations in zone 1. The EXTCLK option is supported in zone 1 and zone 2; see [Figure 44](#).

Figure 73 to Figure 84 show the details of various source synchronous protocols. Table 9 shows the number of output clocks required in an optimal read frame for the different output protocol selections.

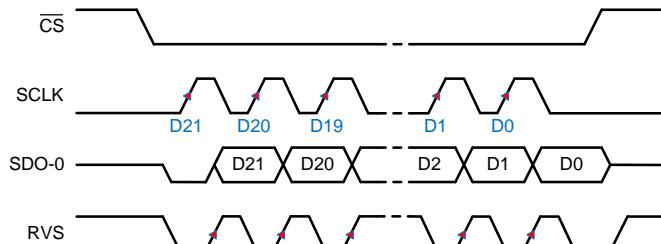


Figure 73. SRC-EXT-SS: SRC, SCLK, Single SDO, SDR

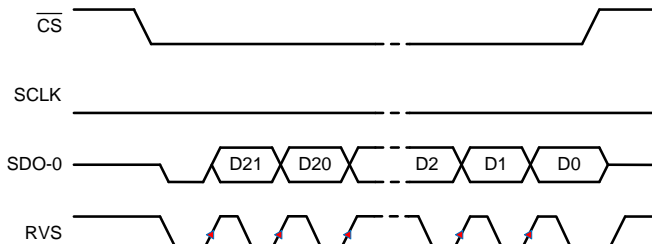


Figure 74. SRC-INT-SS: SRC, INTCLK, Single SDO, SDR

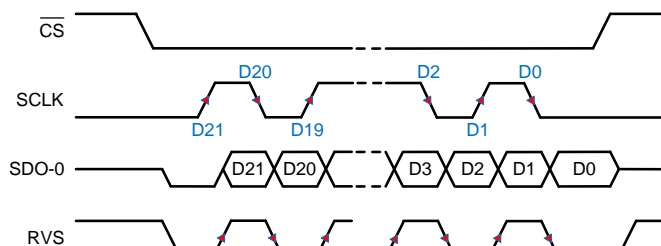


Figure 75. SRC-EXT-SD: SRC, SCLK, Single SDO, DDR

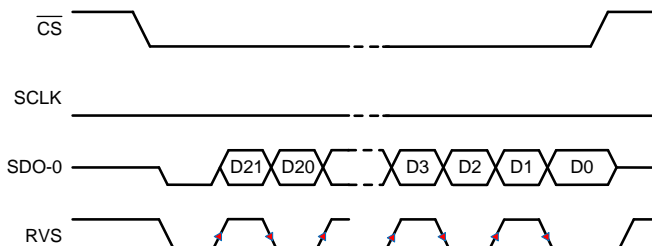


Figure 76. SRC-INT-SD: SRC, INTCLK, Single SDO, DDR

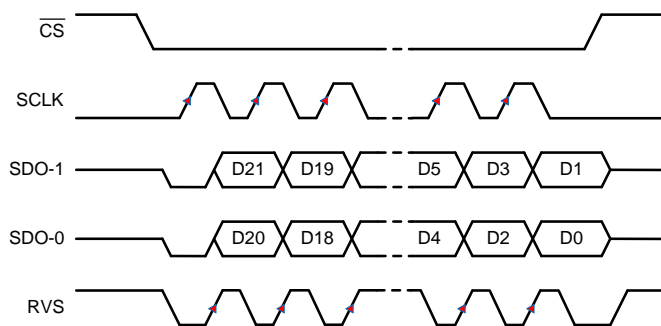


Figure 77. SRC-EXT-DS: SRC, SCLK, Dual SDO, SDR

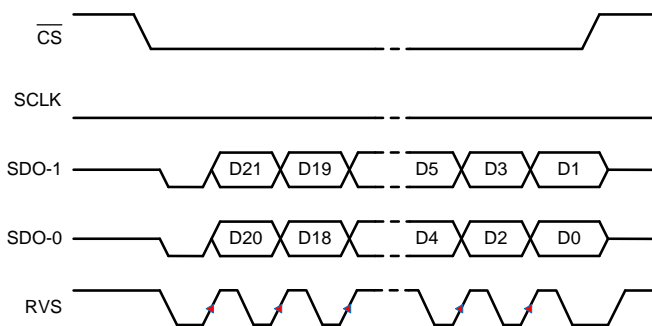
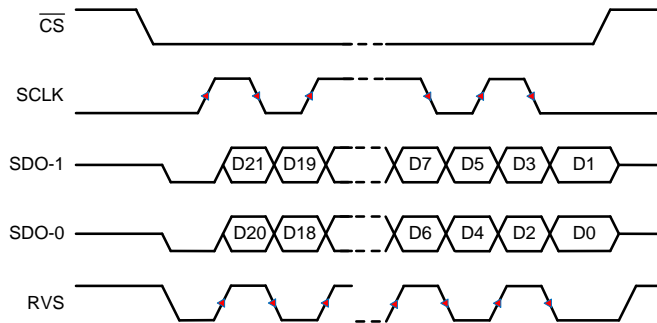
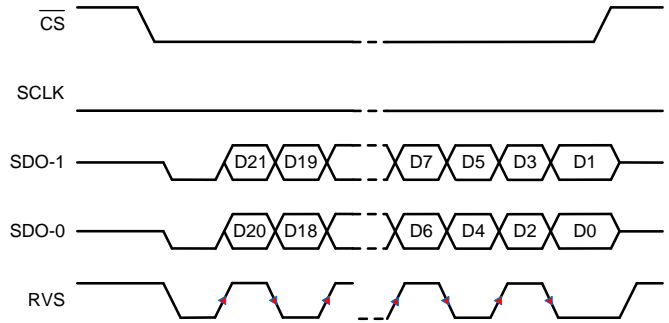


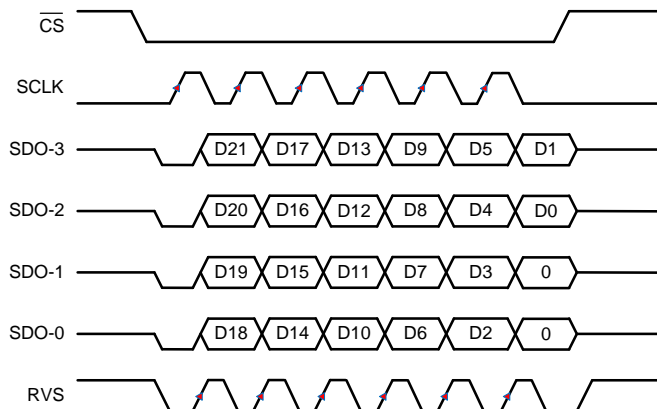
Figure 78. SRC-INT-DS: SRC, INTCLK, Dual SDO, SDR



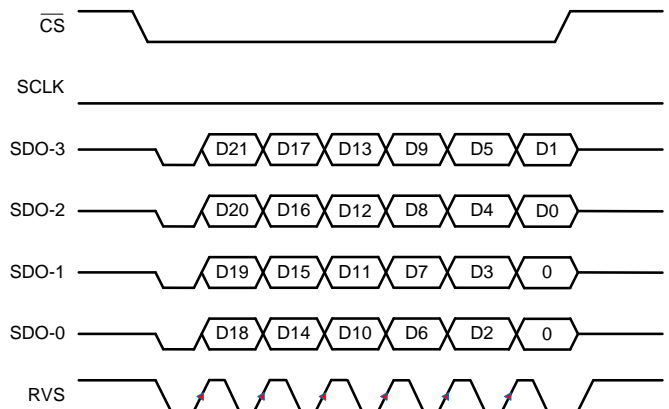
**Figure 79. SRC-EXT-DD: SRC, SCLK, Dual SDO, DDR**



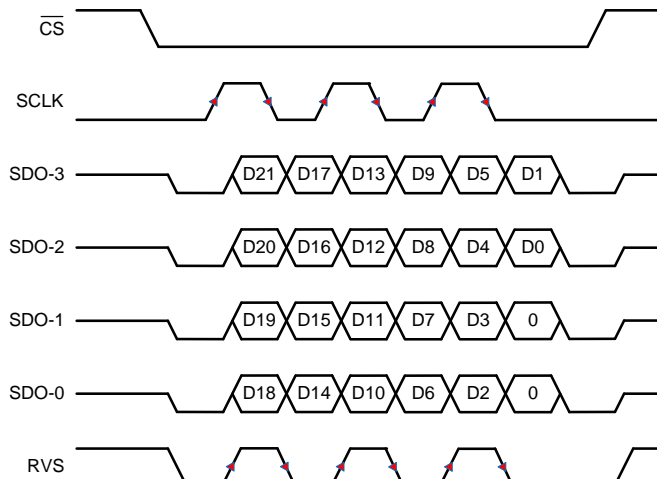
**Figure 80. SRC-INT-DD: SRC, INTCLK, Dual SDO, DDR**



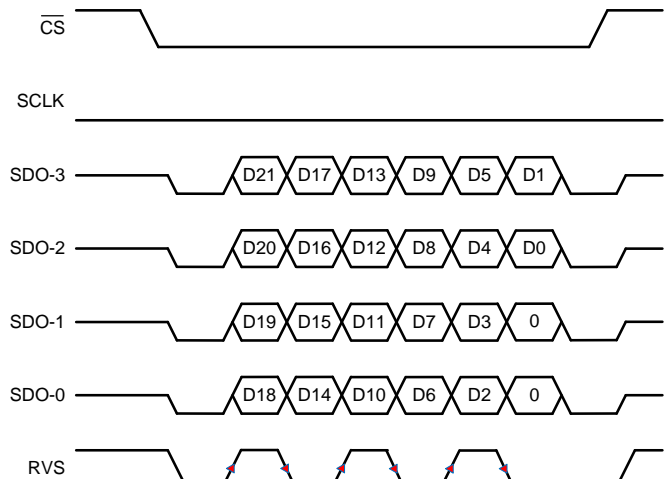
**Figure 81. SRC-EXT-QS: SRC, SCLK, Quad SDO, SDR**



**Figure 82. SRC-INT-QS: SRC, INTCLK, Quad SDO, SDR**



**Figure 83. SRC-EXT-QD: SRC, SCLK, Quad SDO, DDR**



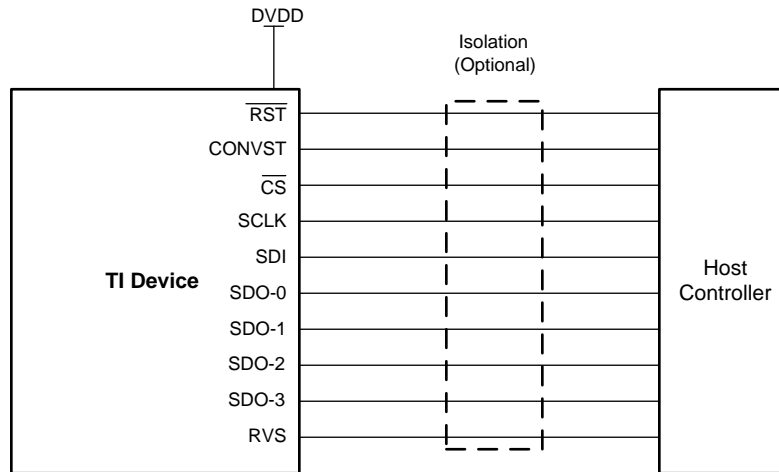
**Figure 84. SRC-INT-QD: SRC, INTCLK, Quad SDO, DDR**

## 7.5.5 Device Setup

The multiSPI digital interface and the device configuration registers offer multiple operation modes. This section describes how to select the hardware connection topology to meet different system requirements.

### 7.5.5.1 Single Device: All multiSPI Options

Figure 85 shows the connections between a host controller and a single device in order to exercise all options provided by the multiSPI digital interface.

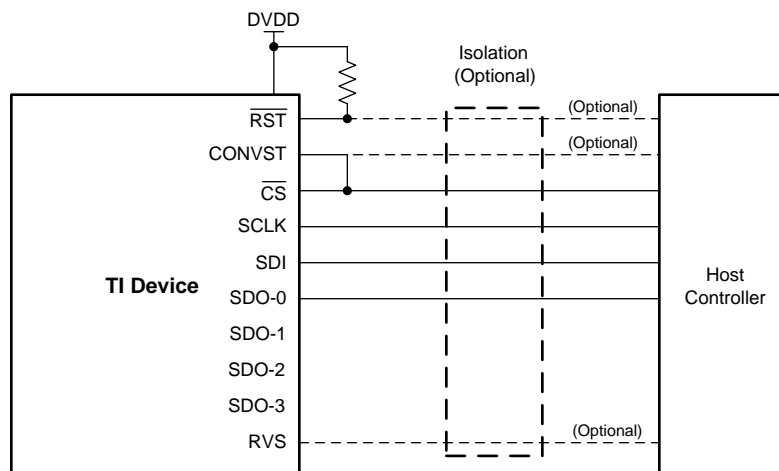


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Figure 85. MultiSPI Digital Interface, All Pins

### 7.5.5.2 Single Device: Minimum Pins for a Standard SPI Interface

Figure 86 shows the minimum-pin interface for applications using a standard SPI protocol.



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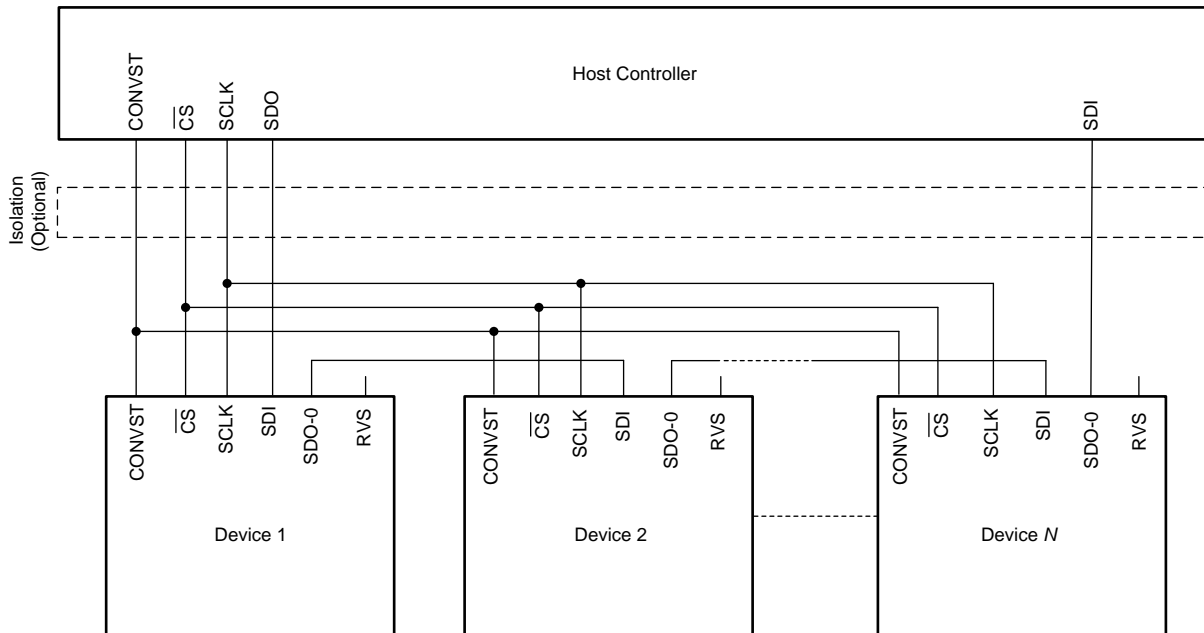
Figure 86. SPI Interface, Minimum Pins

The  $\overline{CS}$ , SCLK, SDI, and SDO-0 pins constitute a standard SPI port of the host controller. The CONVST pin is tied to  $\overline{CS}$ , and the  $\overline{RST}$  pin is tied to DVDD. The SDO-1, SDO-2, and SDO-3 pins have no external connections. The following features are also available:

- Control the CONVST pin independently to get additional timing flexibility.
- Control  $\overline{RST}$  pin independently to add asynchronous reset functionality.
- Monitor the RVS pin for additional timing benefits.

### 7.5.5.3 Multiple Devices: Daisy-Chain Topology

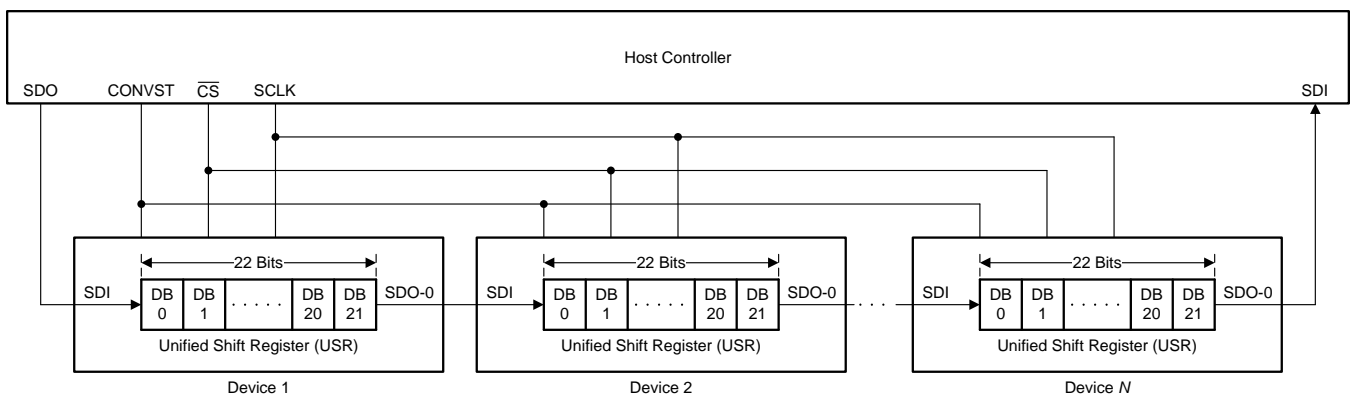
A typical connection diagram showing multiple devices in a daisy-chain topology is shown in [Figure 87](#).



**Figure 87. Daisy-Chain Connections**

The CONVST,  $\overline{CS}$ , and SCLK inputs of all devices are connected together and controlled by a single CONVST,  $\overline{CS}$ , and SCLK pin of the host controller, respectively. The SDI input pin of the first device in the chain (Device 1) is connected to the SDO pin of the host controller, the SDO-0 output pin of Device 1 is connected to the SDI input pin of Device 2, and so on. The SDO-0 output pin of the last device in the chain (Device N) is connected to the SDI pin of the host controller.

To operate multiple devices in a daisy-chain topology, the host controller sets the configuration registers in each device with identical values and operates with any of the legacy, SPI-compatible protocols for data-read and data-write operations (SDO\_CNT[7:0] = 00h or 01h). With these configurations settings, the 22-bit ODR and 22-bit IDR registers in each device collapse to form a single, 22-bit unified shift register (USR) per device, as shown in [Figure 88](#).



**Figure 88. Unified Shift Register**

All devices in the daisy-chain topology sample the respective device analog input signals on the CONVST rising edge. The data transfer frame starts with a  $\overline{CS}$  falling edge. On each SCLK launch edge, every device in the chain shifts out the MSB of the respective USR on to the respective SDO-0 pin. On every SCLK capture edge, each device in the chain shifts in data received on the respective SDI pin as the LSB bit of the respective USR. Therefore, in a daisy-chain configuration, the host controller receives the data of Device  $N$ , followed by the data of Device  $N - 1$ , and so on (MSB-first). On the  $\overline{CS}$  rising edge, each device decodes the contents in the respective USR, and takes appropriate action.

A typical timing diagram for three devices connected in daisy-chain topology using the SPI-00-S protocol is shown in Figure 89.

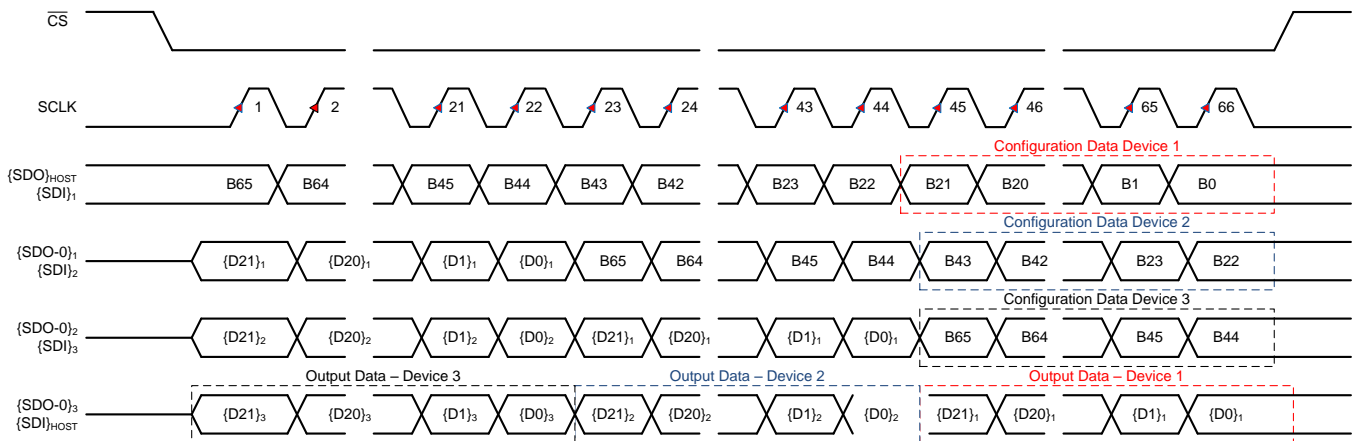


Figure 89. Three-Device, Daisy-Chain Timing

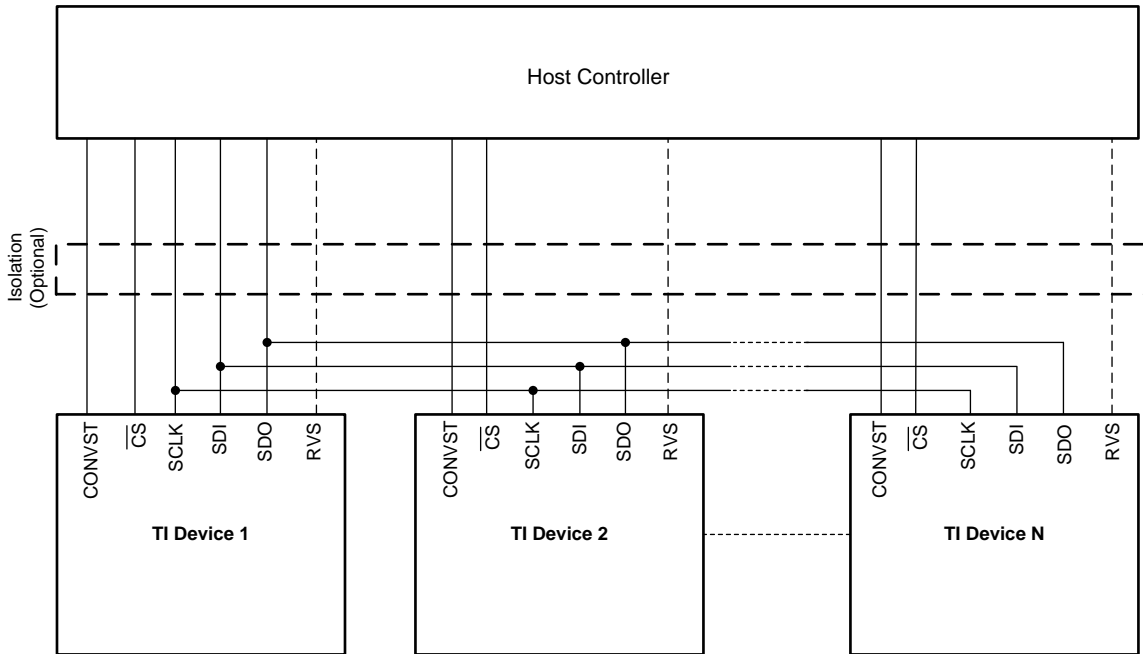
In daisy-chain topology, the overall throughput of the system is proportionally reduced as more devices are connected in the daisy-chain.

**NOTE**

For  $N$  devices connected in daisy-chain topology, an optimal data transfer frame must contain  $22 \times N$  SCLK capture edges. For a longer data transfer frame (number of SCLK in the frame  $> 22 \times N$ ), the host controller must appropriately align the configuration data for each device before bringing  $\overline{CS}$  high. A shorter data transfer frame (number of SCLK in the frame  $< 22 \times N$ ) might result in an erroneous device configuration, and *must be avoided*.

### 7.5.5.4 Multiple Devices: Star Topology

A typical connection diagram showing multiple devices in a star topology is shown in Figure 90. The CONVST, SDI, and SCLK inputs of all devices are connected together, and are controlled by a single CONVST, SDO, and SCLK pin of the host controller, respectively. Similarly, the SDO output pin of all devices are tied together and connected to the a single SDI input pin of the host controller. The  $\overline{\text{CS}}$  input pin of each device is individually controlled by separate  $\overline{\text{CS}}$  control lines from the host controller.



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Figure 90. Star-Topology Connection

The timing diagram for three devices connected in the star topology is shown in Figure 91. In order to avoid any conflict related to multiple devices driving the SDO line at the same time, make sure that the host controller pulls down the  $\overline{\text{CS}}$  signal for *only one device at any particular time*.

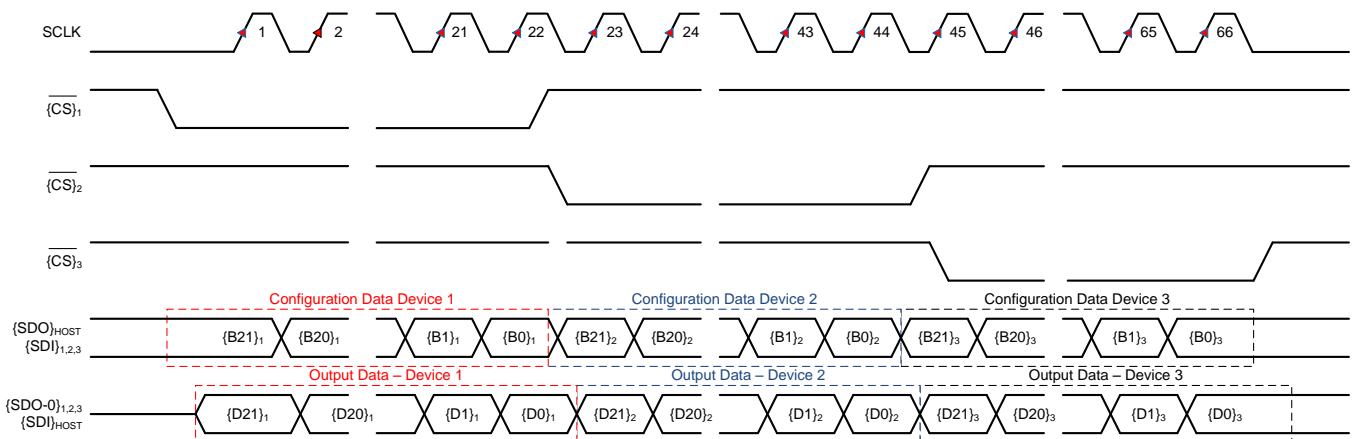


Figure 91. Three-Device, Star Connection Timing

## 7.6 Register Maps

### 7.6.1 Device Configuration and Register Maps

The device features nine configuration registers, mapped as described in [Table 10](#).

**Table 10. Configuration Registers Mapping**

ADDRESS	REGISTER NAME	REGISTER DESCRIPTION
004h	<a href="#">PD_CNTL</a>	Low-power modes control
008h	<a href="#">SDI_CNTL</a>	SDI input protocol selection
00Ch	<a href="#">SDO_CNTL</a>	SDO output protocol selection
010h	<a href="#">DATA_CNTL</a>	Output data word configuration
014h	<a href="#">PATN_LSB</a>	Eight least significant bits (LSB) of the output pattern
015h	<a href="#">PATN_MID</a>	Eight middle bits of the output pattern
016h	<a href="#">PATN_MSB</a>	Four most significant bits (MSB) of the output pattern
020h	<a href="#">OFST_CAL</a>	Offset calibration
030h	<a href="#">REF_MRG</a>	Reference margin

#### 7.6.1.1 PD\_CNTL Register (address = 04h) [reset = 00h]

This register controls the low-power modes offered by the device.

**Figure 92. PD\_CNTL Register**

7	6	5	4	3	2	1	0
0	0	0	0	0	PD_REFBUF	PD_ADC	0
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 11. PD\_CNTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	0	R	00000b	Reserved bits. Reads return 00000b.
2	PD_REFBUF	R/W	0b	This bit powers down the internal reference buffer. 0b = Internal reference buffer is powered up 1b = Internal reference buffer is powered down
1	PD_ADC	R/W	0b	This bit powers down the converter module. 0b = converter module is powered up 1b = converter module is powered down
0	0	R	0b	Reserved bits. Do not write. Reads return 0b.

To power-down the converter module, set the PD\_ADC bit in the [PD\\_CNTL register](#). The converter module powers down on the rising edge of  $\overline{CS}$ . To power-up the converter module, reset the PD\_ADC bit in the [PD\\_CNTL register](#). The converter module starts to power-up on the rising edge of  $\overline{CS}$ . Wait for  $t_{PU\_ADC}$  before initiating any conversion or data transfer operation.

To power-down the internal reference buffer, set the PD\_REFBUF bit in the [PD\\_CNTL register](#). The internal reference buffer powers down on the rising edge of  $\overline{CS}$ . To power-up the internal reference buffer, reset the PD\_REFBUF bit in the [PD\\_CNTL register](#). The internal reference buffer starts to power-up on the rising edge of  $\overline{CS}$ . Wait for  $t_{PU\_REFBUF}$  before initiating any conversion.

### 7.6.1.2 SDI\_CNTL Register (address = 008h) [reset = 00h]

This register selects the SPI protocol for writing data to the device.

**Figure 93. SDI\_CNTL Register**

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SDI_MODE[1:0]	
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 12. SDI\_CNTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	0	R	000000b	Reserved bits. Do not write. Reads return 000000b.
1-0	SDI_MODE[1:0]	R/W	00b	These bits select the protocol for writing data into the device. 00b = Standard SPI with CPOL = 0 and CPHASE = 0 01b = Standard SPI with CPOL = 0 and CPHASE = 1 10b = Standard SPI with CPOL = 1 and CPHASE = 0 11b = Standard SPI with CPOL = 1 and CPHASE = 1

### 7.6.1.3 SDO\_CNTL Register (address = 0Ch) [reset = 00h]

This register configures the protocol for reading data from the device.

**Figure 94. SDO\_CNTL Register**

7	6	5	4	3	2	1	0
SSYNC_CLK_SEL[1:0]		0	DATA_RATE	SDO_WIDTH[1:0]		SDO_MODE[1:0]	
R/W-00b		R-0b	R/W-0b	R/W-00b		R/W-00b	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 13. SDO\_CNTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	SSYNC_CLK_SEL[1:0]	R/W	00b	These bits select the source and frequency of the clock for the ADC-Clock-Master mode, and are valid only if SDO_MODE[1:0] = 11b. 00b = External SCLK echo 01b = Internal clock (INTCLK) 10b = Internal clock / 2 (INTCLK / 2) 11b = Internal clock / 4 (INTCLK / 4)
5	0	R	0b	Reserved bit. Do not write. Reads return 0b.
4	DATA_RATE	R/W	0b	This bit is ignored if SDO_MODE[1:0] = 00b. When SDO_MODE[1:0] = 11b: 0b = SDOs are updated at single data rate (SDR) with respect to the output clock 1b = SDOs are updated at double data rate (DDR) with respect to the output clock
3-2	SDO_WIDTH[1:0]	R/W	00b	These bits set the width of the output bus. 0xb = Data are output only on SDO-0 10b = Data are output only on SDO-0 and SDO-1 11b = Data are output on SDO-0, SDO-1, SDO-2, and SDO-3
1-0	SDO_MODE[1:0]	R/W	00b	These bits select the protocol for reading data from the device. 00b = SDO follows the SPI protocol selected in the <a href="#">SDI_CNTL register</a> 01b = SDO follows the SPI protocol selected in the <a href="#">SDI_CNTL register</a> but with <i>Early Data Launch</i> feature enabled. See <a href="#">Table 6</a> . 10b = Invalid configuration, not supported by the device 11b = SDO follows the source-synchronous protocol

### 7.6.1.4 DATA\_CNTL Register (address = 010h) [reset = 00h]

This register configures the contents of the 22-bit output data word (D[21:0]).

**Figure 95. DATA\_CNTL Register**

7	6	5	4	3	2	1	0
0	0	0	0	FPAR_LOC[1:0]		PAR_EN	DATA_VAL
R-0b	R-0b	R-0b	R-0b	R/W-00b		R/W-0b	R/W-0b

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 14. DATA\_CNTL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-2	FPAR_LOC[1:0]	R/W	00b	These bits control the data span for calculating the FTPAR bit (bit D[2] in the output data word). 00b = D[2] reflects even parity calculated for 4 MSB 01b = D[2] reflects even parity calculated for 8 MSB 10b = D[2] reflects even parity calculated for 12 MSB 11b = D[2] reflects even parity calculated for 16 MSB
1	PAR_EN	R/W	0b	0b = Output data does not contain any parity information D[3] = 0 D[2] = 0 1b = Parity information is appended to the LSB of the output data D[3] = Even parity calculated on bits D[21:4] D[2] = Even parity computed on selected number of MSB of D[21:4] as per FPAR_LOC[1:0] setting See <a href="#">Figure 42</a> for further details of parity computation.
0	DATA_VAL	R/W	0b	These bits control bits D[21:4] of the output data word. 0b = 18-bit conversion output 1b = 18-bit contents of the fixed-pattern registers See <a href="#">PATN_CNTL</a> for more details.

### 7.6.1.5 PATN\_LSB Register (address = 014h) [reset = 00h]

This register controls the eight LSB of the output pattern when DATA\_VAL = 1b; see Figure 99.

Figure 96. PATN\_LSB Register

7	6	5	4	3	2	1	0
PATN_LSB_BITS							
R/W-0000000b							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 15. PATN\_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATN_LSB_BITS	R/W	0000000b	8 LSB of the output pattern

### 7.6.1.6 PATN\_MID Register (address = 015h) [reset = 00h]

This register controls the middle eight bits of the output pattern when DATA\_VAL = 1b; see Figure 99.

Figure 97. PATN\_MID Register

7	6	5	4	3	2	1	0
PATN_MID_BITS							
R/W-0000000b							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 16. PATN\_MID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PATN_MID_BITS	R/W	0000000b	8 middle bits of the output pattern

### 7.6.1.7 PATN\_MSB Register (address = 016h) [reset = 00h]

This register controls the four MSB of the output pattern when DATA\_VAL = 1b; see Figure 99.

Figure 98. PATN\_MSB Register

7	6	5	4	3	2	1	0
0	0	0	0	PATN_MSB_BITS			
R-0b	R-0b	R-0b	R-0b	R/W-0000b			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 17. PATN\_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	R	0000b	Reserved bits. Reads return 0000b.
3-0	PATN_MSB_BITS	R/W	0000b	4 MSB of the output pattern

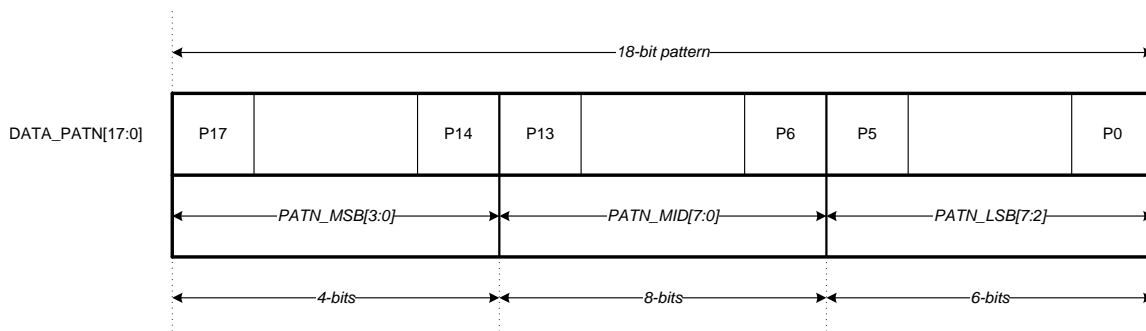


Figure 99. DATA\_PATN[17:0]

### 7.6.1.8 OFST\_CAL Register (address = 020h) [reset = 00h]

This register selects the external reference range for optimal offset calibration.

**Figure 100. OFST\_CAL Register**

7	6	5	4	3	2	1	0
0	0	0	0	0	REF_SEL[2:0]		
R-0b	R-0b	R-0b	R-0b	R-0b	R/W-000b		

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 18. OFST\_CAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-3	0	R	00000b	Reserved bits. Reads return 00000b.
2-0	REF_SEL[2:0]	R/W	000b	These bits select the external reference range for optimal offset. 000b = Optimum offset calibration for $V_{REF} = 5.0$ V 001b = Optimum offset calibration for $V_{REF} = 4.5$ V 010b = Optimum offset calibration for $V_{REF} = 4.096$ V 011b = Optimum offset calibration for $V_{REF} = 3.3$ V 100b = Optimum offset calibration for $V_{REF} = 3.0$ V 101b = Optimum offset calibration for $V_{REF} = 2.5$ V 110b = Optimum offset calibration for $V_{REF} = 5.0$ V 111b = Optimum offset calibration for $V_{REF} = 5.0$ V

### 7.6.1.9 REF\_MRG Register (address = 030h) [reset = 00h]

This register selects the margining to be added to or subtracted from the reference buffer output; see the [Reference Buffer Module](#) section.

**Figure 101. REF\_MRG Register**

7	6	5	4	3	2	1	0
0	0	EN_MARG	REF_OFST[4:0]				
R-0b	R-0b	R/W-0b	R/W-00000b				

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

**Table 19. REF\_MRG Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-6	0	R	00b	Reserved bits. Reads return 00b.
5	EN_MARG	R/W	0b	This bit enables margining feature. 0b = Margining is disabled 1b = Margining is enabled
4-0	REF_OFST[4:0]	R/W	00000b	These bits select the reference offset value as per <a href="#">Table 20</a> .

**Table 20. REF\_OFST[4:0] settings**

REF_OFST[4:0]	$\Delta V_{\text{REFBUFOUT}}$ (typical <sup>(1)</sup> )
00000b	0 mV
00001b	280 $\mu$ V
00010b	580 $\mu$ V
00011b	840 $\mu$ V
00100b	1.12 mV
00101b	1.4 mV
00110b	1.68 mV
00111b	1.96 mV
01000b	2.24 mV
01001b	2.52 mV
01010b	2.8 mV
01011b	3.08 mV
01100b	3.36 mV
01101b	3.64 mV
01110b	3.92 mV
01111b	4.2 mV
10000b	-4.5 mV
10001b	-4.22 mV
10010b	-3.94 mV
10011b	-3.66 mV
10100b	-3.38 mV
10101b	-3.1 mV
10110b	-2.82 mV
10111b	-2.54 mV
11000b	-2.26 mV
11001b	-1.98 mV
11010b	-1.7 mV
11011b	-1.42 mV
11100b	-1.14 mV
11101b	-860 $\mu$ V
11110b	-580 $\mu$ V
11111b	-280 $\mu$ V

(1) The actual  $V_{\text{REFBUFOUT}}$  value may vary by  $\pm 10\%$  from [Table 20](#)

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The two primary circuits required to maximize the performance of a high-precision, successive approximation register (SAR), analog-to-digital converter (ADC) are the input driver and the reference driver circuits. This section presents general principles for designing these circuits, followed by an application circuit designed using the ADS891xB.

#### 8.1.1 ADC Reference Driver

The external reference source must provide low-drift and very accurate voltage at the REFIN pin of the ADS891xB. The output broadband noise of most references can be in the order of a few hundred  $\mu\text{V}_{\text{RMS}}$ . Therefore, to prevent any degradation in the noise performance of the ADC, appropriately filter the output of the voltage reference by using a low-pass filter with a cutoff frequency of a few hundred hertz.

The internal reference buffer of the ADS891xB provides the dynamic load posed on the REFBUFOUT pin during the conversion process. Decouple the REFBUFOUT pin with the REFM pin using the recommended  $C_{\text{REFBUF}}$  and  $R_{\text{ESR}}$ . See the [Layout](#) section for layout recommendations.

#### 8.1.2 ADC Input Driver

The input driver circuit for a high-precision ADC mainly consists of two parts: a driving amplifier and a charge kickback filter. The amplifier is used for signal conditioning of the input signal and the low output impedance of the amplifier provides a buffer between the signal source and the switched capacitor inputs of the ADC. The charge kickback filter helps attenuate the sampling charge injection from the switched-capacitor input stage of the ADC, and band-limits the wideband noise contributed by the front-end circuit. Careful design of the front-end circuit is critical to meet the linearity and noise performance of the ADS891xB.

##### 8.1.2.1 Charge-Kickback Filter

The charge-kickback filter is an RC filter at the input pins of the ADC that filters the broadband noise from the front-end drive circuitry, and attenuates the sampling charge injection from the switched-capacitor input stage of the ADC. A filter capacitor,  $C_{\text{FLT}}$ , is connected from each input pin of the ADC to the ground (as shown in [Figure 102](#)). This capacitor helps reduce the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. Generally, the value of this capacitor must be at least 20 times the specified value of the ADC sampling capacitance. For the ADS891xB, the input sampling capacitance is equal to 60 pF; therefore, for optimal performance, keep  $C_{\text{FLT}}$  greater than 1.2 nF. This capacitor must be a COG- or NPO-type. The type of dielectric used in COG or NPO ceramic capacitors provides the most stable electrical properties over voltage, frequency, and temperature changes.

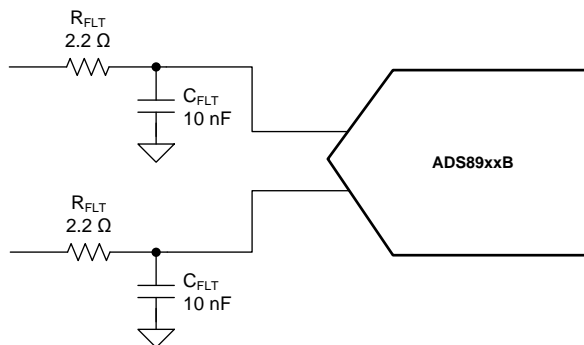


Figure 102. Charge Kickback Filter Configuration

## Application Information (continued)

Driving capacitive loads can degrade the phase margin of the input amplifier, thus making the amplifier marginally unstable. To avoid amplifier stability issues, series isolation resistors ( $R_{FLT}$ ) are used at the output of the amplifiers. A higher value of  $R_{FLT}$  helps with amplifier stability, but adds distortion as a result of interactions with the nonlinear input impedance of the ADC. Distortion increases with source impedance, input signal frequency, and input signal amplitude. Therefore, the selection of  $R_{FLT}$  requires balancing the stability of the driver amplifier and distortion performance of the design. Always verify the stability and settling behavior of the driving amplifier and charge-kickback filter by TINA-TI™ SPICE simulation. Keep the tolerance of the selected resistors less than 1% to keep the inputs balanced.

### 8.1.2.2 Input Amplifier Selection

Selection criteria for the input amplifiers is highly dependent on the input signal type, as well as the performance goals, of the data acquisition system. Some key amplifier specifications to consider when selecting an appropriate amplifier to drive the inputs of the ADC are:

- **Small-signal bandwidth.** Select the small-signal bandwidth of the input amplifiers to be as high as possible after meeting the power budget of the system. Higher bandwidth reduces the closed-loop output impedance of the amplifier, thus allowing the amplifier to more easily drive the ADC sample-and-hold capacitor and the RC filter ([Charge-Kickback Filter](#)) at the inputs of the ADC. Higher bandwidth amplifiers offer faster settling times while driving the capacitive load of the charge-kickback filter, thus reducing harmonic distortion at higher input frequencies. In order to maintain the overall stability of the input driver circuit, select the amplifier with a unity gain bandwidth (UGB) as described in [Equation 16](#):

$$UGB \geq 4 \times \left( \frac{1}{2\pi \times R_{FLT} \times C_{FLT}} \right) \quad (16)$$

- **Distortion.** Both the ADC and the input driver introduce distortion in a data acquisition block. To make sure that the distortion performance of the data acquisition system is not limited by the front-end circuit, the distortion of the input driver must be at least 10 dB less than the distortion of the ADC, as shown in [Equation 17](#).

$$THD_{AMP} \leq THD_{ADC} - 10 \text{ (dB)} \quad (17)$$

- **Noise.** Noise contribution of the front-end amplifiers must be as low as possible to prevent any degradation in SNR performance of the system. Generally, to make sure that the noise performance of the data acquisition system is not limited by the front-end circuit, the total noise contribution from the front-end circuit must be kept below 20% of the input-referred noise of the ADC. Noise from the input driver circuit is band-limited by designing a low cutoff frequency, charge-kickback filter, as explained in [Equation 18](#).

$$N_G \times \sqrt{2} \times \sqrt{\left( \frac{V_{1/f\_AMP\_PP}}{6.6} \right)^2 + e_{n\_RMS}^2 \times \frac{\pi}{2} \times f_{-3dB}} \leq \frac{1}{5} \times \frac{V_{REF}}{\sqrt{2}} \times 10^{-\left( \frac{SNR(dB)}{20} \right)}$$

where:

- $V_{1/f\_AMP\_PP}$  is the peak-to-peak flicker noise in  $\mu V$
  - $e_{n\_RMS}$  is the amplifier broadband noise density in  $nV/\sqrt{Hz}$
  - $f_{-3dB}$  is the 3-dB bandwidth of the charge-kickback filter
  - $N_G$  is the noise gain of the front-end circuit that is equal to 1 in a buffer configuration (18)
- **Settling Time.** For dc signals with fast transients that are common in a multiplexed application, the input signal must settle within an 18-bit accuracy at the device inputs during the acquisition time window. This condition is critical to maintain the overall linearity performance of the ADC. Typically, amplifier data sheets specify the output settling performance only up to 0.1% to 0.001%, which may not be sufficient for the desired 18-bit accuracy. Therefore, always verify the settling behavior of the input driver by TINA-TI SPICE simulations before selecting the amplifier.

## 8.2 Typical Application

### 8.2.1 Data Acquisition (DAQ) Circuit for Lowest Distortion and Noise Performance With Differential Input

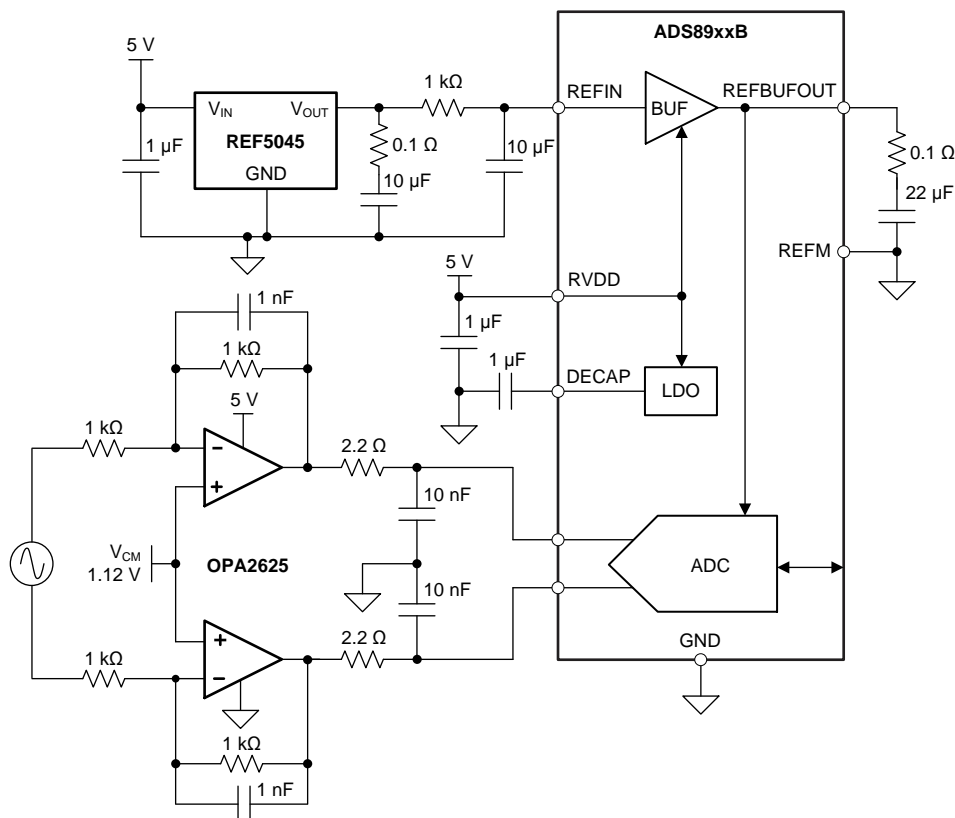


Figure 103. Differential-Input DAQ Circuit for Lowest Distortion and Noise Using the ADS891xB

#### 8.2.1.1 Design Requirements

For this example, the design parameters are listed in [Table 21](#).

Table 21. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
ADC sample rate	Maximum-specified throughput
Input signal	2-kHz input, 4.5-V <sub>PP</sub> fully differential
Noise performance, SNR	> 101-dB
Distortion, THD	< -120-dB
Linearity, INL	< ±1-LSB,
Reference	4.5 V
Power supply	< 5.5-V analog, 3.3-V I/O

#### 8.2.1.2 Detailed Design Procedure

The application circuit is illustrated in [Figure 103](#). For simplicity, power-supply decoupling capacitors are not shown in these circuit diagrams; see the [Power-Supply Recommendations](#) section for suggested guidelines.

The reference voltage of 4.5 V is generated by the high-precision, low-noise [REF5045](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The low-power [OPA2625](#) (a high-bandwidth, low-distortion, high-precision amplifier in an inverting gain configuration) as an input driver provides exceptional ac performance because of its extremely low-distortion and high-bandwidth specifications. The distortion resulting from variation in the common-mode signal is eliminated by using the OPA2625 in an inverting gain configuration. To exercise the complete dynamic range of the device, the common-mode voltage at the ADS891xB inputs is established at a value of 2.25 V (4.5 V / 2) by using the noninverting pins of the OPA2625 amplifiers. In addition, the components of the charge kickback filter keep the noise from the front-end circuit low without adding distortion to the input signal.

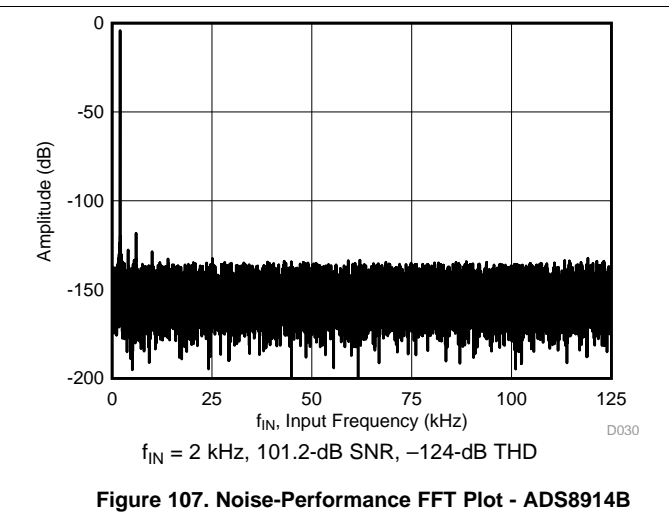
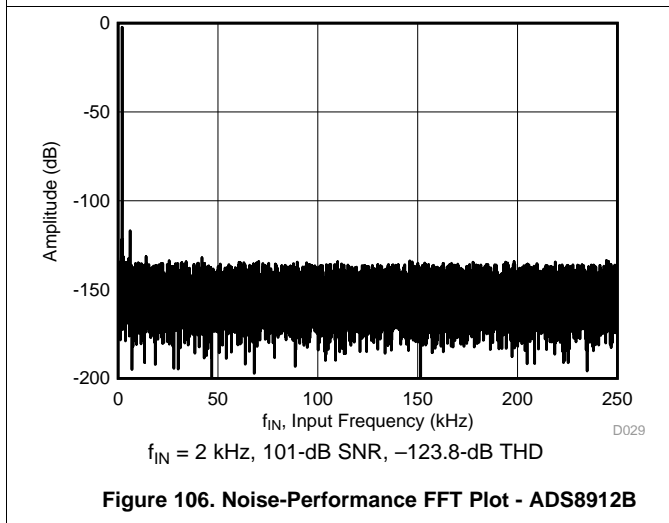
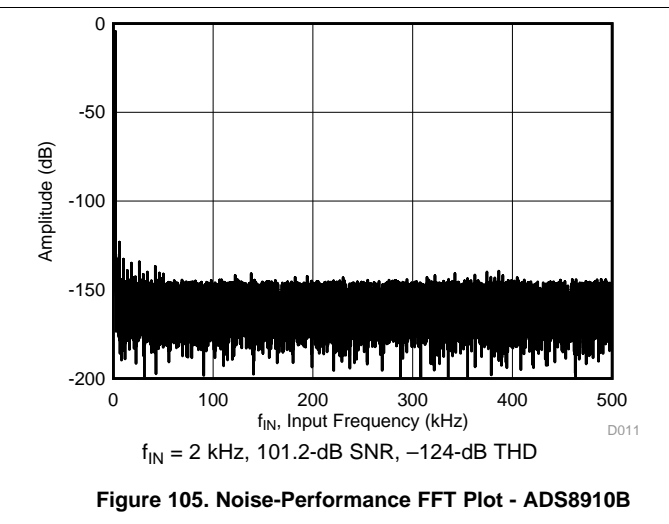
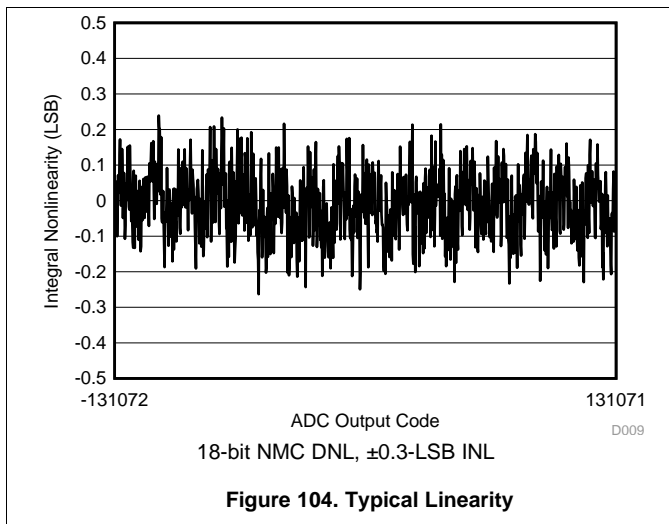
For a complete schematic, see the [ADS8910BEVM-PDK user's guide](#) located in the [ADS8910B SAR Analog to Digital Converter Evaluation Module](#) web folder at www.ti.com.

A similar circuit is used in reference design TIPD211, a step-by-step process to design a [20-Bit, 1-MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications](#) using four [ADS8900B](#) SAR ADCs, four [OPA2625](#) precision amplifiers and one [REF5050](#) precision reference.



For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation results, and test results, refer to [TI Precision Design TIPD211, 18-Bit, 1-MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications \(TIDUBW7\)](#).

### 8.2.1.3 Application Curves





**Table 22. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
ADC sample rate	Maximum-specified throughput
Input signal	2-kHz input, $\pm 4.5\text{-V}_{PP}$ fully differential and $\pm 4.5\text{-V}_{PP}$ single-ended bipolar signal
Noise performance, SNR	> 101-dB
Distortion, THD	< -120-dB,
Linearity, INL	< $\pm 1\text{-LSB}$
Reference	4.5 V
Power supply	< 5.4-V analog, 3.3-V I/O

### 8.2.4 Detailed Design Procedure

The application circuits are shown in [Figure 108](#) and [Figure 109](#). In both applications, the input signal is processed through a high-bandwidth, low-distortion, fully-differential amplifier (FDA) designed in a gain of 1 V/V and a low-pass RC filter before going to the ADC.

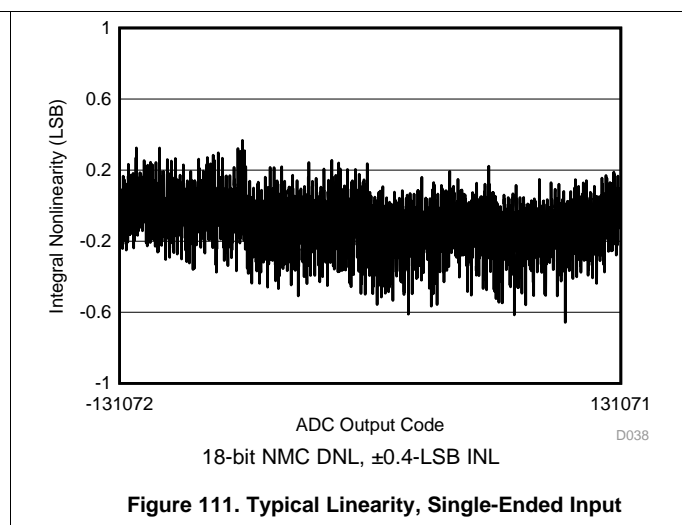
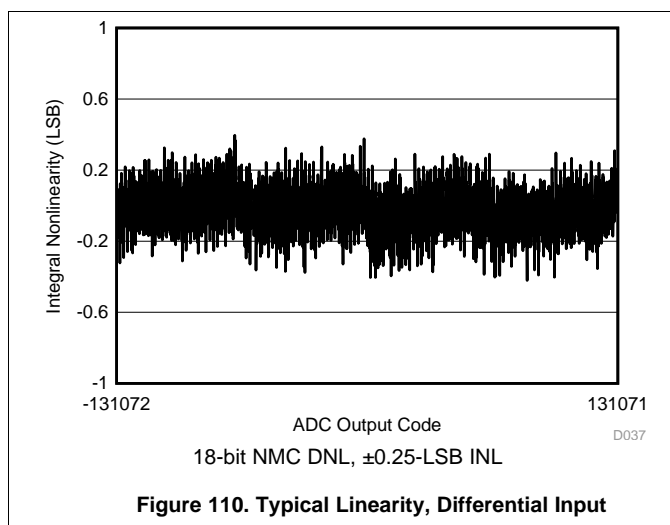
The reference voltage of 4.5 V generated by the high-precision, low-noise [REF5045](#) circuit. The output broadband noise of the reference is heavily filtered by a low-pass filter with a 3-dB cutoff frequency of 16 Hz.

Generally, the distortion from the input driver must be at least 10 dB less than the ADC distortion. The distortion resulting from variation in the common-mode signal is eliminated by using the FDA in an inverting gain configuration that establishes a fixed common-mode level for the circuit. This configuration also eliminates the requirement of a rail-to-rail swing at the amplifier input. Therefore, these circuits use the low-power [THS4551](#) as an input driver that provides exceptional ac performance because of its extremely low-distortion and high bandwidth specifications. In addition, the components of the charge kickback filter keep the noise from the front-end circuit low without adding distortion to the input signal.

The circuit in [Figure 108](#) shows a fully-differential data acquisition (DAQ) block optimized for low distortion and noise using the THS4551 and ADS891xB. This front-end circuit configuration requires a differential signal at the input of the FDA and provides a differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4551 (not shown in [Figure 108](#)). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider.

The circuit in [Figure 109](#) shows a single-ended to differential DAQ block optimized for low distortion and noise using the THS4551 and the ADS891xB. This front-end circuit configuration requires a single-ended bipolar signal at the input of the FDA and provides a fully-differential output to drive the ADC inputs. The common-mode voltage of the input signal provided to the ADC is set by the  $V_{OCM}$  pin of the THS4551 (not shown in [Figure 109](#)). To use the complete dynamic range of the ADC,  $V_{OCM}$  can be set to  $V_{REF} / 2$  by using a simple resistive divider.

### 8.2.5 Application Curves



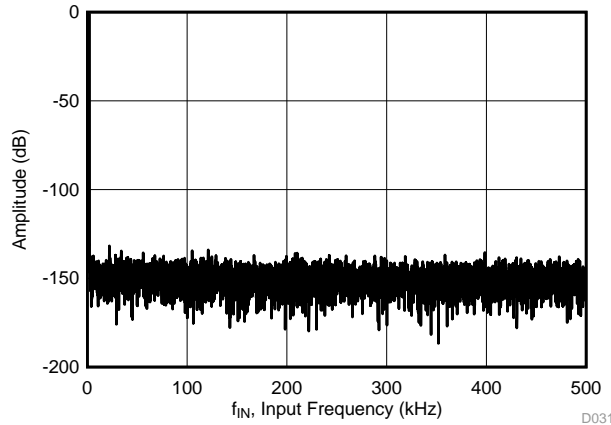


Figure 112. Noise-Performance FFT Plot: ADS8910B, Differential Input

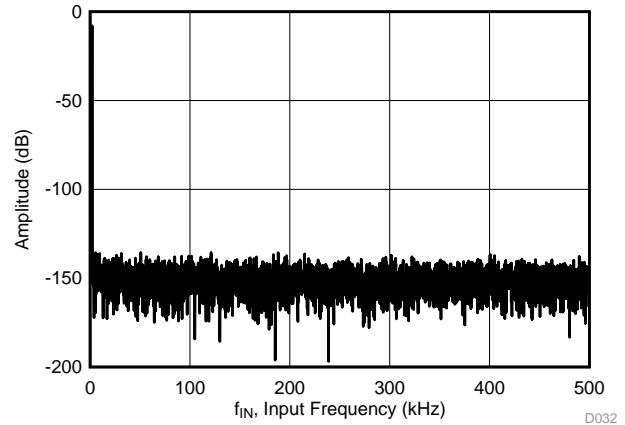


Figure 113. Noise-Performance FFT Plot: ADS8910B, Single-Ended Input

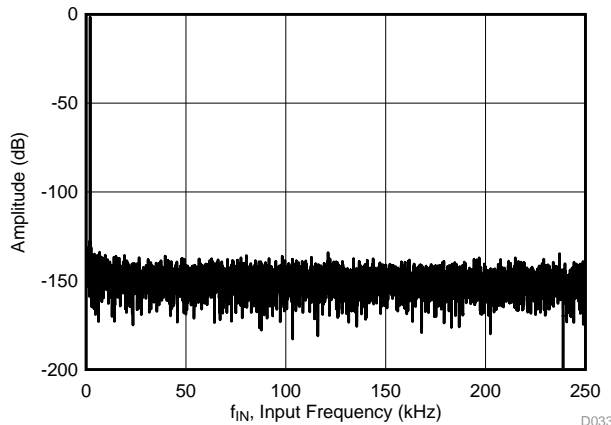


Figure 114. Noise-Performance FFT Plot: ADS8912B, Differential Input

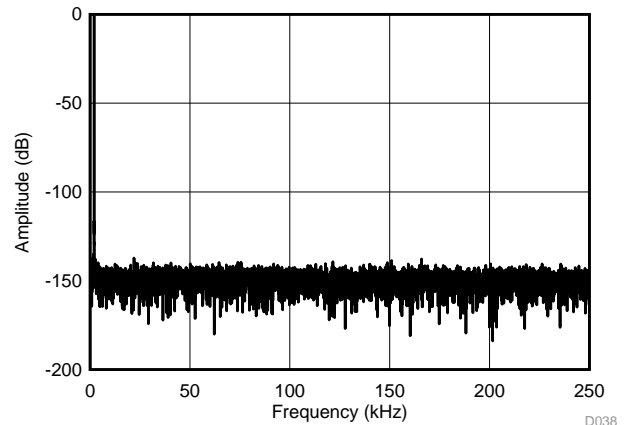


Figure 115. Noise-Performance FFT Plot: ADS8912B, Single-Ended Input

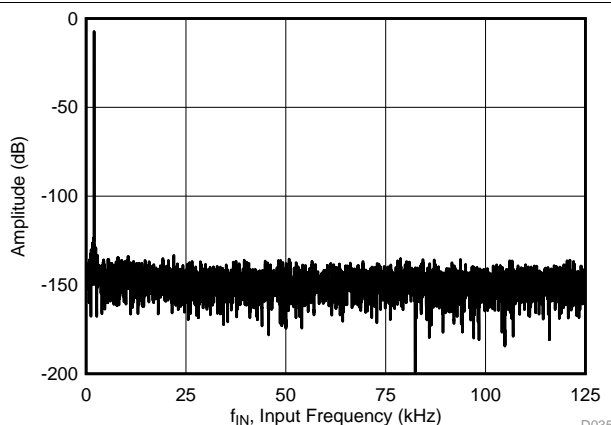


Figure 116. Noise-Performance FFT Plot: ADS8914B, Differential Input

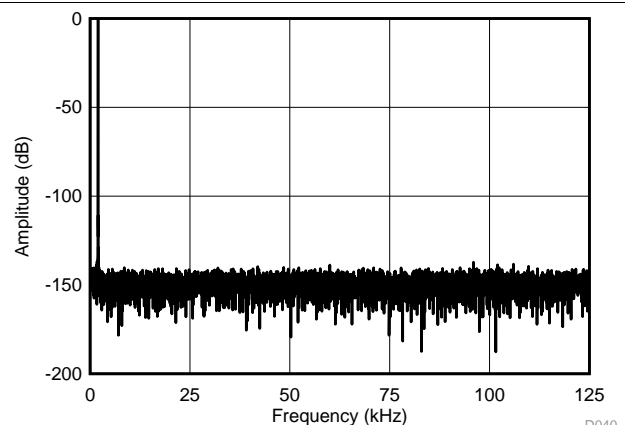


Figure 117. Noise-Performance FFT Plot: ADS8914B, Single-Ended Input

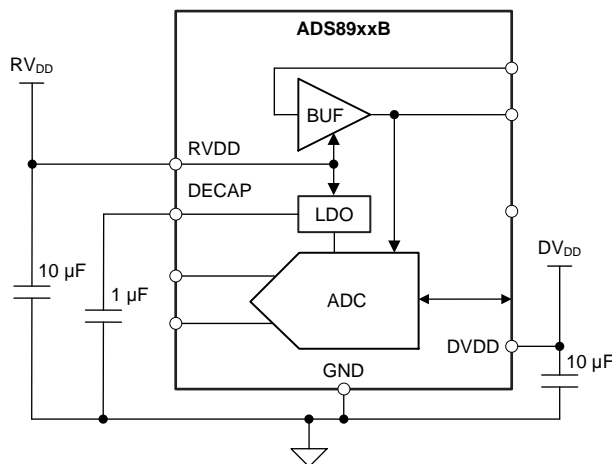
## 9 Power-Supply Recommendations

The devices have two separate power supplies:  $RV_{DD}$  and  $DV_{DD}$ . The internal reference buffer and the internal LDO operate on  $RV_{DD}$ . The ADC core operates on the LDO output (available on the DECAP pins).  $DV_{DD}$  is used for the interface circuits.  $RV_{DD}$  and  $DV_{DD}$  can be independently set to any value within their permissible ranges. During normal operation, if  $RV_{DD}$  supply drops below the  $RV_{DD}$  minimum specification, ramp the  $RV_{DD}$  supply down to  $\leq 0.7$  V before power-up. During power-up,  $RV_{DD}$  must rise monotonically to the recommended minimum operating voltage.

The  $RV_{DD}$  supply voltage value defines the permissible range for the external reference voltage  $V_{REF}$  on REFIN pin as:

$$2.5 \text{ V} \leq V_{REF} \leq (RV_{DD} - 0.3) \text{ V} \quad (19)$$

Place a 10- $\mu\text{F}$  decoupling capacitor between the  $RV_{DD}$  and GND pins, and between the  $DV_{DD}$  and GND pins, as shown in [Figure 118](#). Use a minimum 1- $\mu\text{F}$  decoupling capacitor between the DECAP pins and the GND pin.



**Figure 118. Power-Supply Decoupling**

## 10 Layout

### 10.1 Layout Guidelines

This section provides some layout guidelines for achieving optimum performance with the ADS891xB device family.

#### 10.1.1 Signal Path

As illustrated in [Figure 119](#), the analog input signals are routed in opposite directions to the digital connections. The reference decoupling components are kept away from the switching digital signals. This arrangement prevents noise generated by digital switching activity from coupling to sensitive analog signals.

#### 10.1.2 Grounding and PCB Stack-Up

Low inductance grounding is critical for achieving optimum performance. Grounding inductance is kept below 1 nH with 15-mil grounding vias and a printed circuit board (PCB) layout design that has at least four layers. Place all critical components of the signal chain on the top layer with a solid analog ground from subsequent inner layers to minimize via length to ground.

For lowest inductance grounding, connect the GND pins of the ADS891xB (pin 11 and pin 15) directly to the device thermal pad and place at least four 8-mil grounding vias on the device thermal pad.

#### 10.1.3 Decoupling of Power Supplies

Place the decoupling capacitors on  $R_{V_{DD}}$ , the LDO output, and  $DV_{DD}$  within 20 mil from the respective pins, and use a 15-mil via to ground from each capacitor. Avoid placing vias between any supply pin and the respective decoupling capacitor.

#### 10.1.4 Reference Decoupling

Dynamic currents are also present at the REFBUFOUT and REFM pins during the conversion phase, and excellent decoupling is required to achieve optimum performance. Place a 22- $\mu$ F, X7R-grade, ceramic capacitor with at least 10-V rating and an ESR of 1- $\Omega$  between the REFBUFOUT and the REFM pins, as illustrated in [Figure 119](#). Select 0603- or 0805-size capacitors to keep equivalent series inductance (ESL) low. Connect the REFM pins to the decoupling capacitor before a ground via.

#### 10.1.5 Differential Input Decoupling

Dynamic currents are also present at the differential analog inputs of the ADS891xB. Use C0G- or NPO-type capacitors to decouple these inputs because with these type of capacitors, capacitance stays almost constant over the full input voltage range. Lower-quality capacitors (such as X5R and X7R) have large capacitance changes over the full input-voltage range that may cause degradation in the performance of the device.

## 10.2 Layout Example

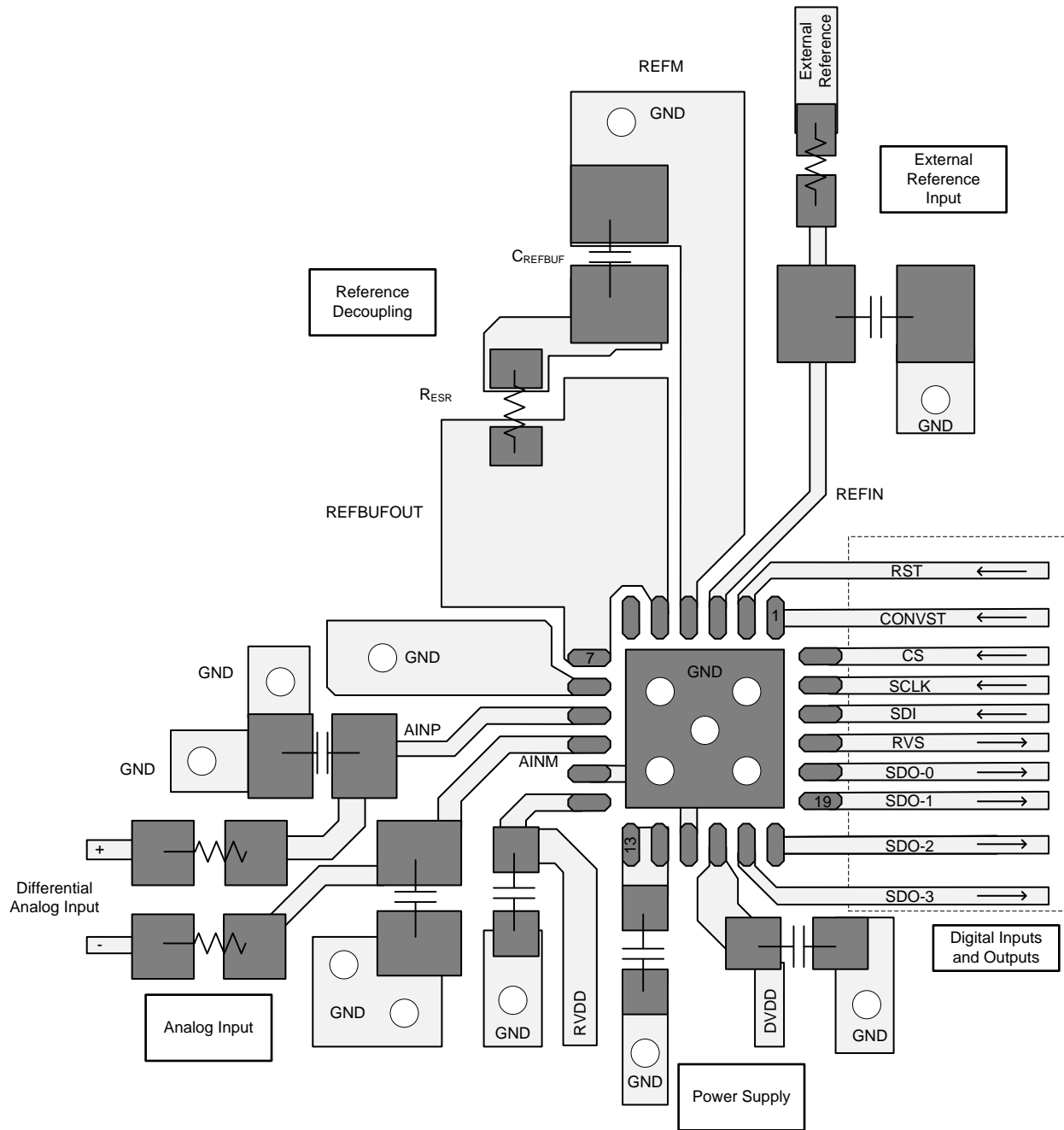


Figure 119. Recommended Layout

## 11 Device and Documentation Support

### 11.1 Documentation Support

#### 11.1.1 Related Documentation

For related documentation see the following:

- [ADS8910BEVM-PDK User's Guide \(SBAU268\)](#)
- [Enabling Faster, Smarter, and More Robust System Solutions for SAR ADCs With TI's multiSPI™ Digital Interface](#)
- [Ultrasound CW Doppler Summing and 20-bit True Raw Data Conversion Reference Design](#)
- [20-Bit, 1-MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications Reference Design](#)
- [20-Bit, 1-MSPS Isolator Optimized Data Acquisition Reference Design Maximizing SNR and Sample Rate](#)
- [A 20-bit, 1 MSPS Isolated Data Acquisition \(DAQ\) Reference Design Optimizing Jitter for Maximum SNR and Sample Rate](#)
- [Simplify Isolation Designs Using an Enhanced-SPI ADC Interface](#)
- [Optimizing Data Transfer on High-Resolution, High Throughput Data Converters](#)
- [Improving Input Settling for Precision Data Converters](#)
- [OPAx625 High-Bandwidth, High-Precision, Low THD+N, 16-Bit and 18-Bit Analog-to-Digital Converter \(ADC\) Drivers Data Sheet](#)
- [REF5050 Low-Noise, Very Low Drift, Precision Voltage Reference Data Sheet](#)
- [THS4551 Low Noise, Precision, 150MHz, Fully Differential Amplifier](#)

#### 11.2 Related Links

The following table lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

**Table 23. Related Links**

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
ADS8910B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADS8912B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
ADS8914B	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

#### 11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

#### 11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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## 11.5 Trademarks

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## 11.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8910BRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8910B	<a href="#">Samples</a>
ADS8910BRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8910B	<a href="#">Samples</a>
ADS8912BRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8912B	<a href="#">Samples</a>
ADS8912BRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8912B	<a href="#">Samples</a>
ADS8914BRGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8914B	<a href="#">Samples</a>
ADS8914BRGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	8914B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

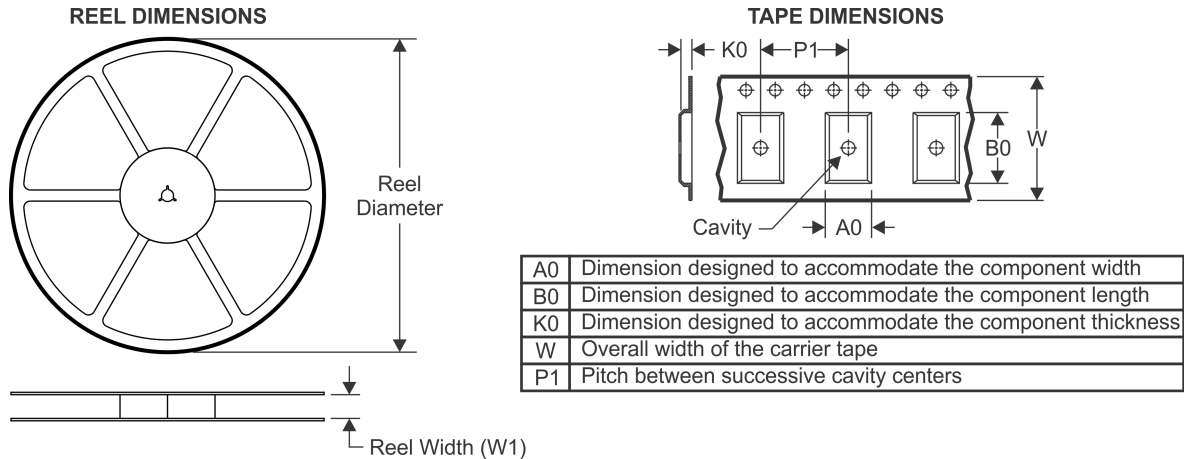
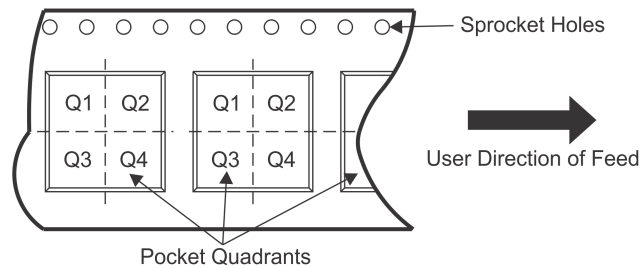
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

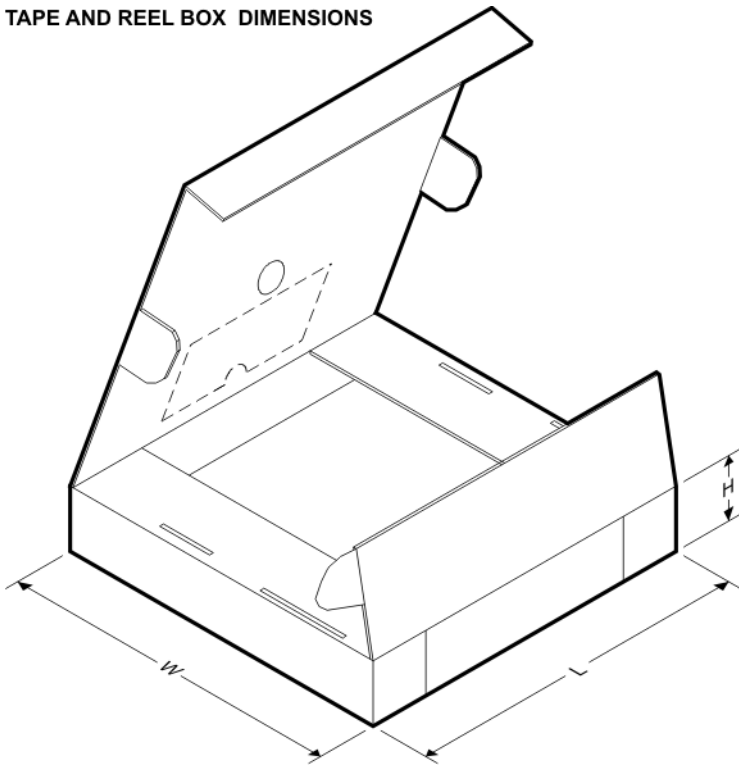
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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8910BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8910BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8912BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8912BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8914BRGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
ADS8914BRGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

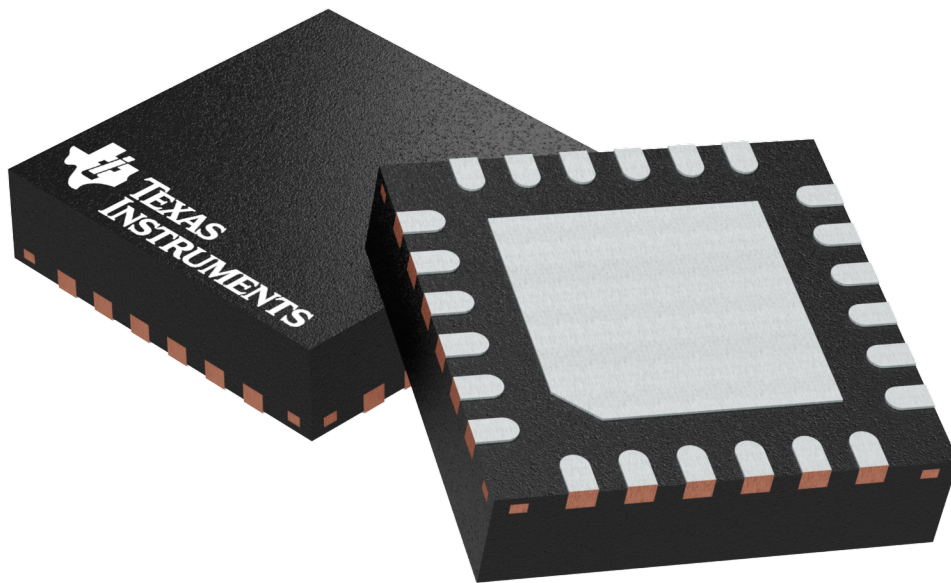
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8910BRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8910BRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8912BRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8912BRGET	VQFN	RGE	24	250	210.0	185.0	35.0
ADS8914BRGER	VQFN	RGE	24	3000	367.0	367.0	35.0
ADS8914BRGET	VQFN	RGE	24	250	210.0	185.0	35.0

**RGE 24**

**GENERIC PACKAGE VIEW**

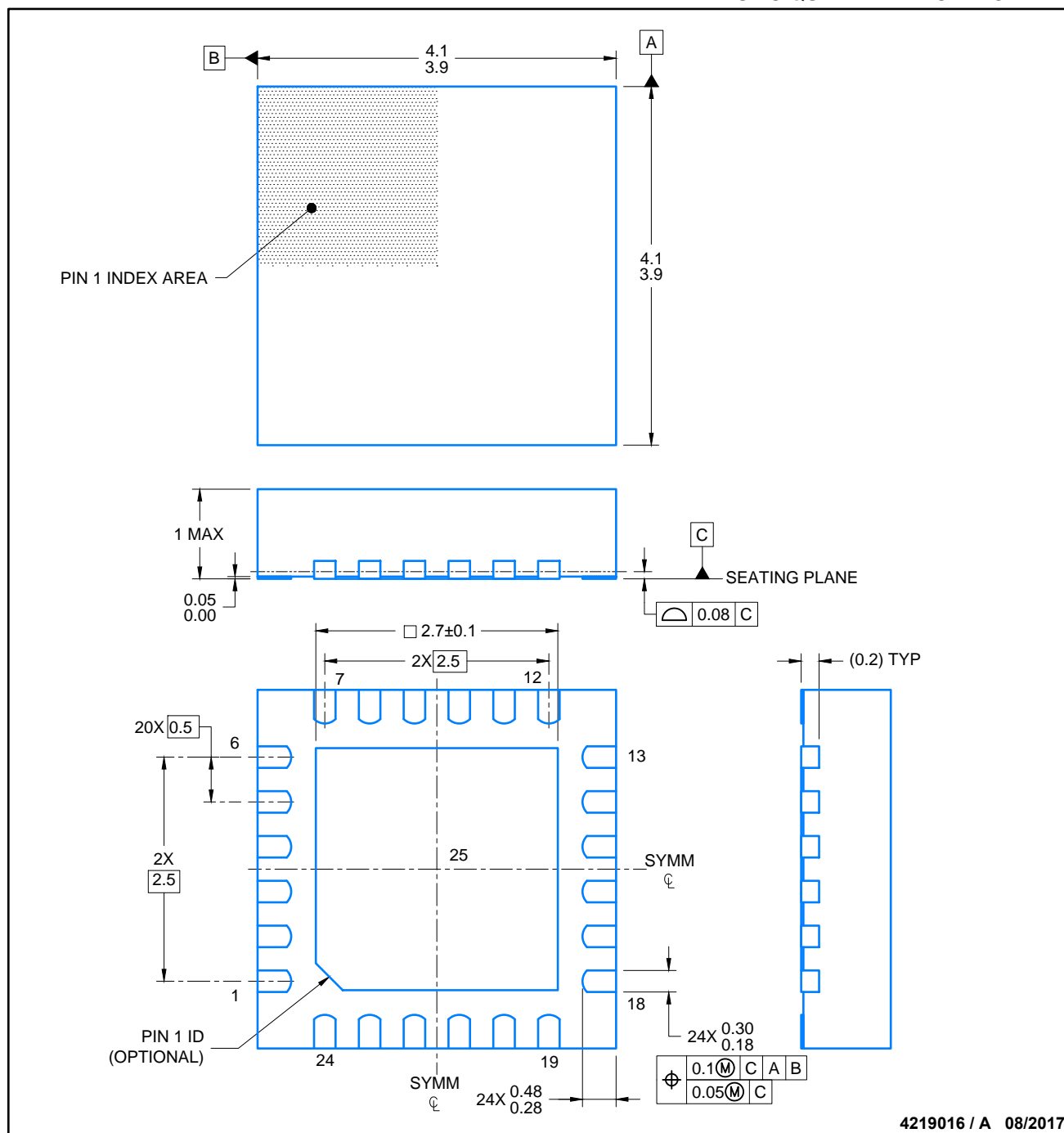
**VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



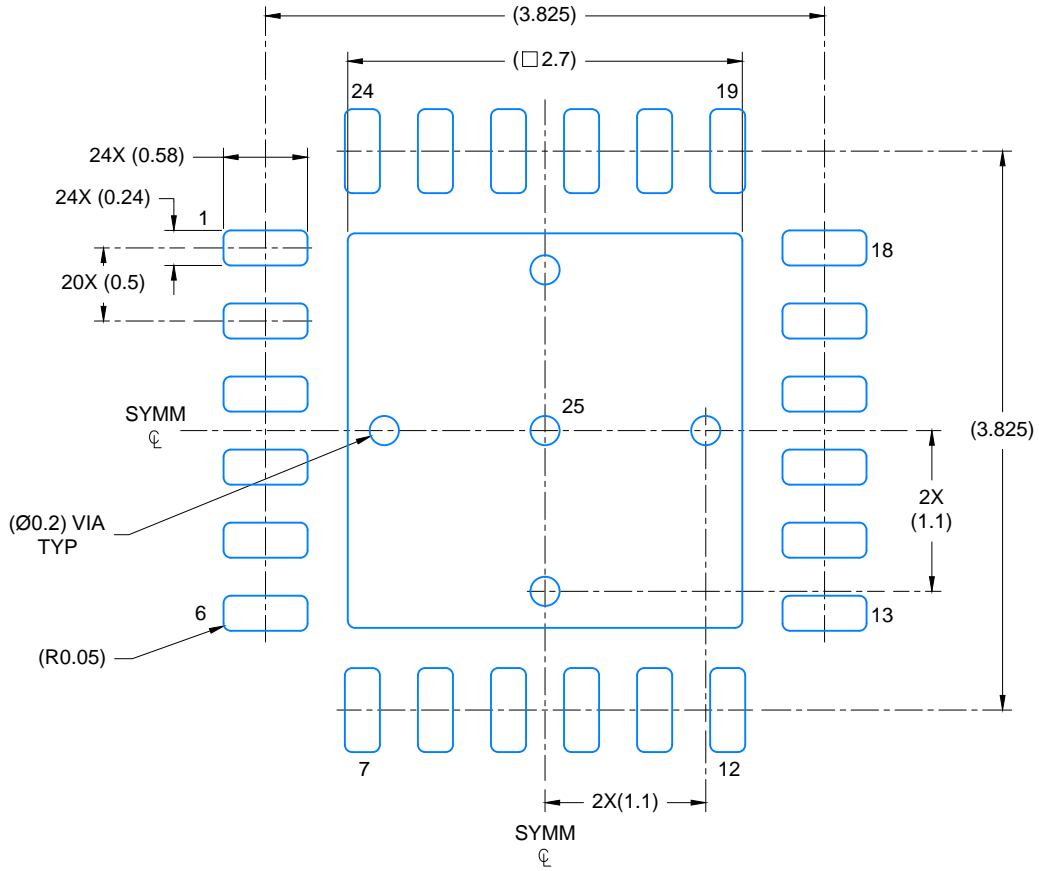
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4204104/H

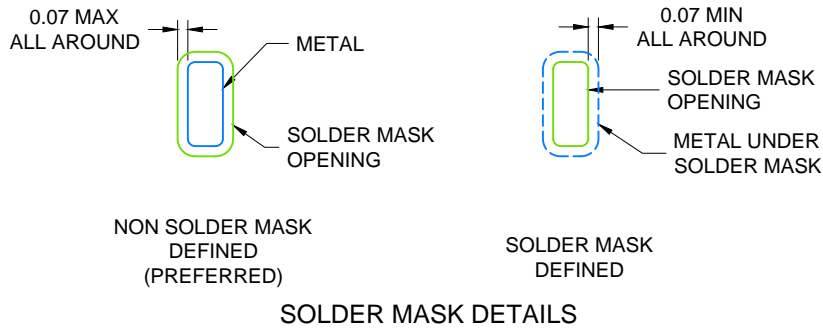


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



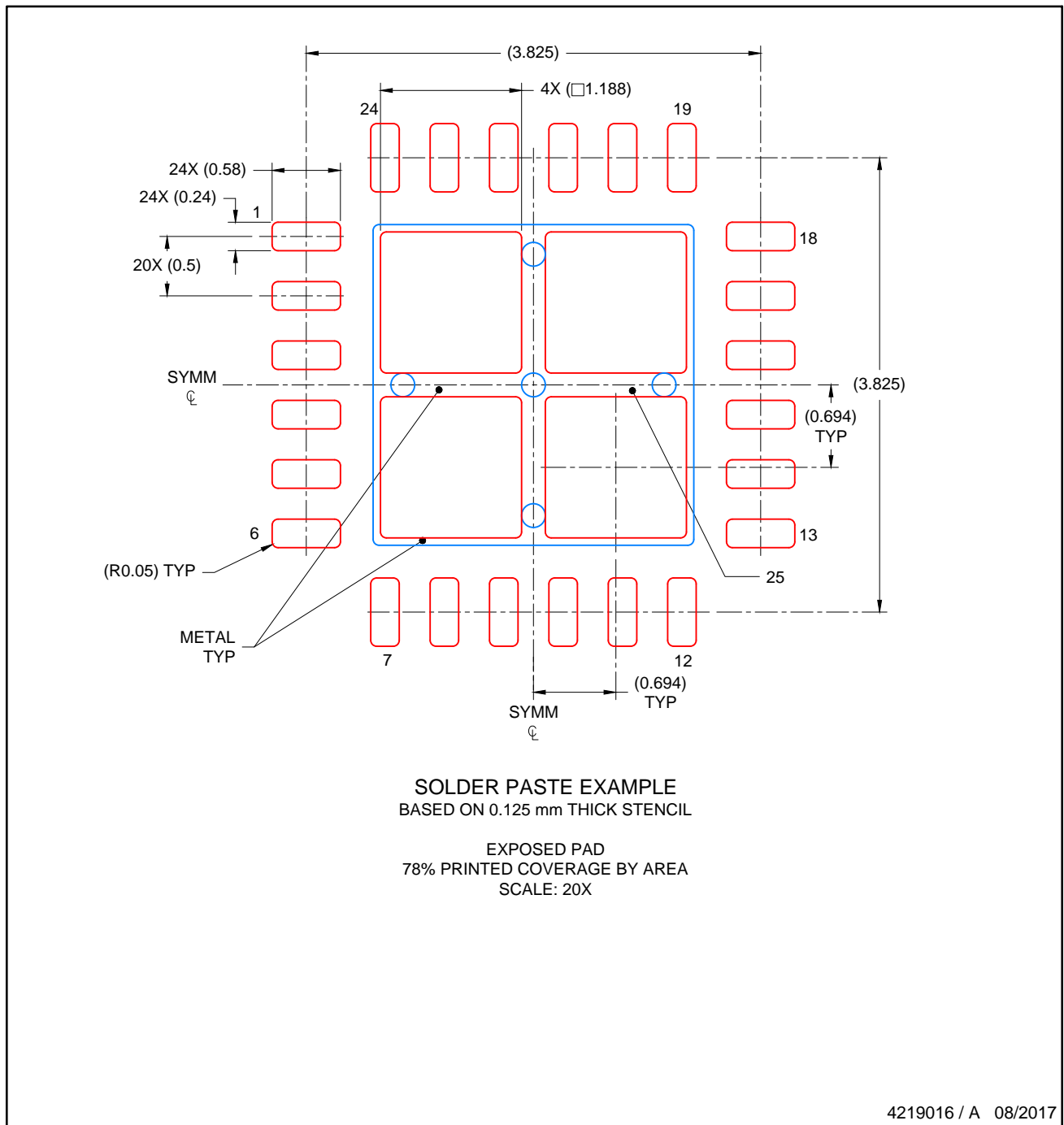
LAND PATTERN EXAMPLE  
SCALE: 20X



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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



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NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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