



**THE DATASHEET OF  
LX7157BCLD**





## Description

LX7157B is a step-down PWM regulator IC with integrated high side P-CH MOSFET and low side N-CH MOSFET. The 2.2MHz switching frequency facilitates small output filter components.

The operational input voltage range of LX7157B is from 3V to 5.5V. LX7157B uses current mode operation with internal compensation allowing for fast transient response with minimum external components.

LX7157B employs a pulse SKIP method at light load to improve the light load efficiency; as a result, the battery life is extended. The internal soft-start limits the inrush current.

Cycle-by-cycle current limit protects the regulator against over-current conditions. The LX7157B operates in hiccup mode to further enhance the robustness of the converter for heavy over-load or short circuit fault, and it recovers automatically once the fault is cleared.

The thermal protection shuts down the regulator under an over-temperature condition.

## Features

- ◆ 3A Step-down Regulator
- ◆ Input Supply Voltage Range: 3V to 5.5V
- ◆ Integrated PMOS and NMOS
- ◆ Internal Compensation
- ◆ Internal Slope Compensation
- ◆ 2.2MHz Switching Frequency
- ◆ SKIP Pulse to Improve Light Load Efficiency
- ◆ Input UVLO and OV Protection
- ◆ Enable & Power Good
- ◆ Internal Soft-start
- ◆ Cycle-by-Cycle Over Current Protection
- ◆ Hiccup Mode Operation Under OCP
- ◆ RoHS compliant, DFN 3.5mm x 3mm 12L

## Applications

- Set-top box and LCD TV's
- Notebook/Netbook
- Server and Workstations
- Routers
- Video Cards
- PC Peripherals
- PoE Powered Devices

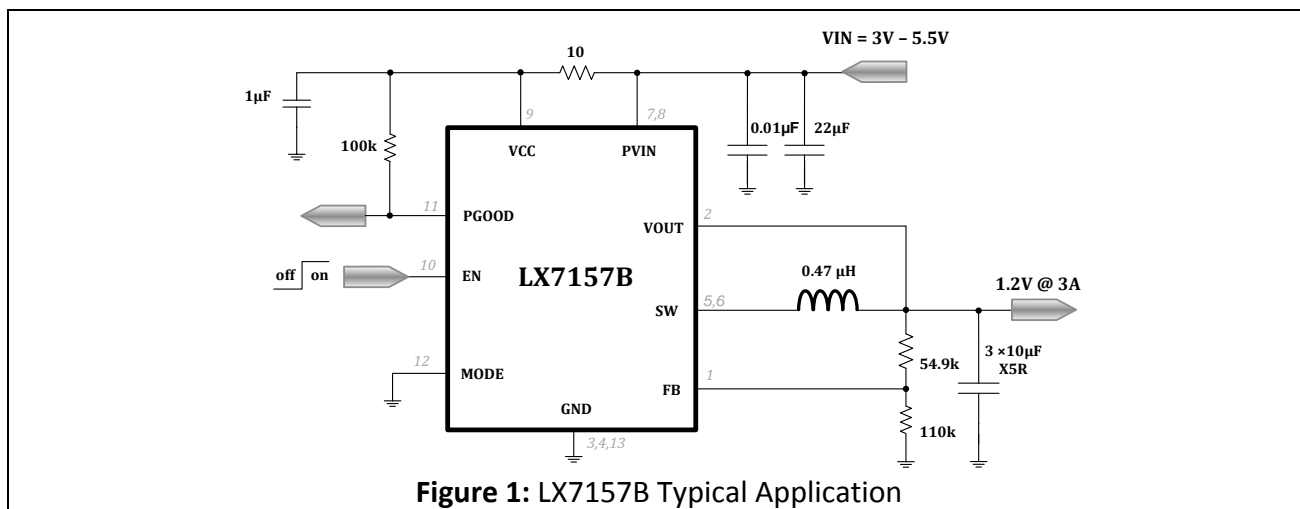
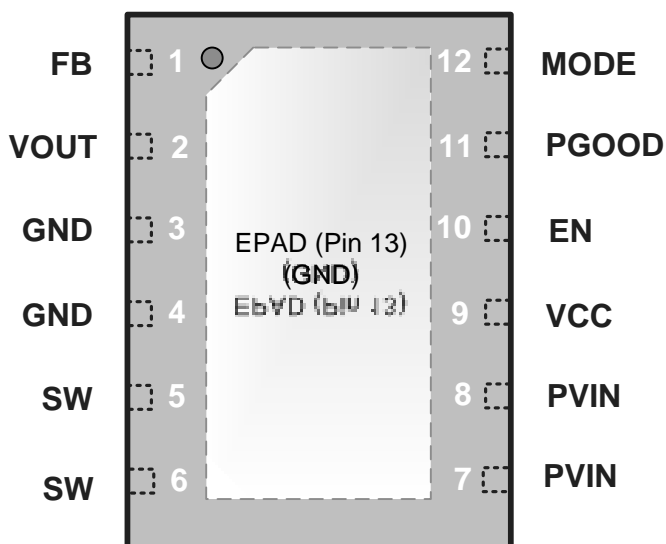


Figure 1: LX7157B Typical Application



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### Pin Configuration and Pinout



**LX7157B**  
**DFN 3.5mm x 3mm 12L**  
**Top View**

Part Marking:

7157B

XXXX

MSC

XXXX = Date/Lot Code

**Figure 2:** LX7157B Pinout

### Ordering Information

Ambient Temperature	Type	Package	Part Number	Packaging Type
-10 to 85°C	RoHS compliant, Pb-free	DFN 3.5mm x 3mm 12L	LX7157BCLD	Bulk
			LX7157BCLD-TR	Tape and Reel

# 3V Input, High Frequency, 3A Step-Down Converter Production Datasheet



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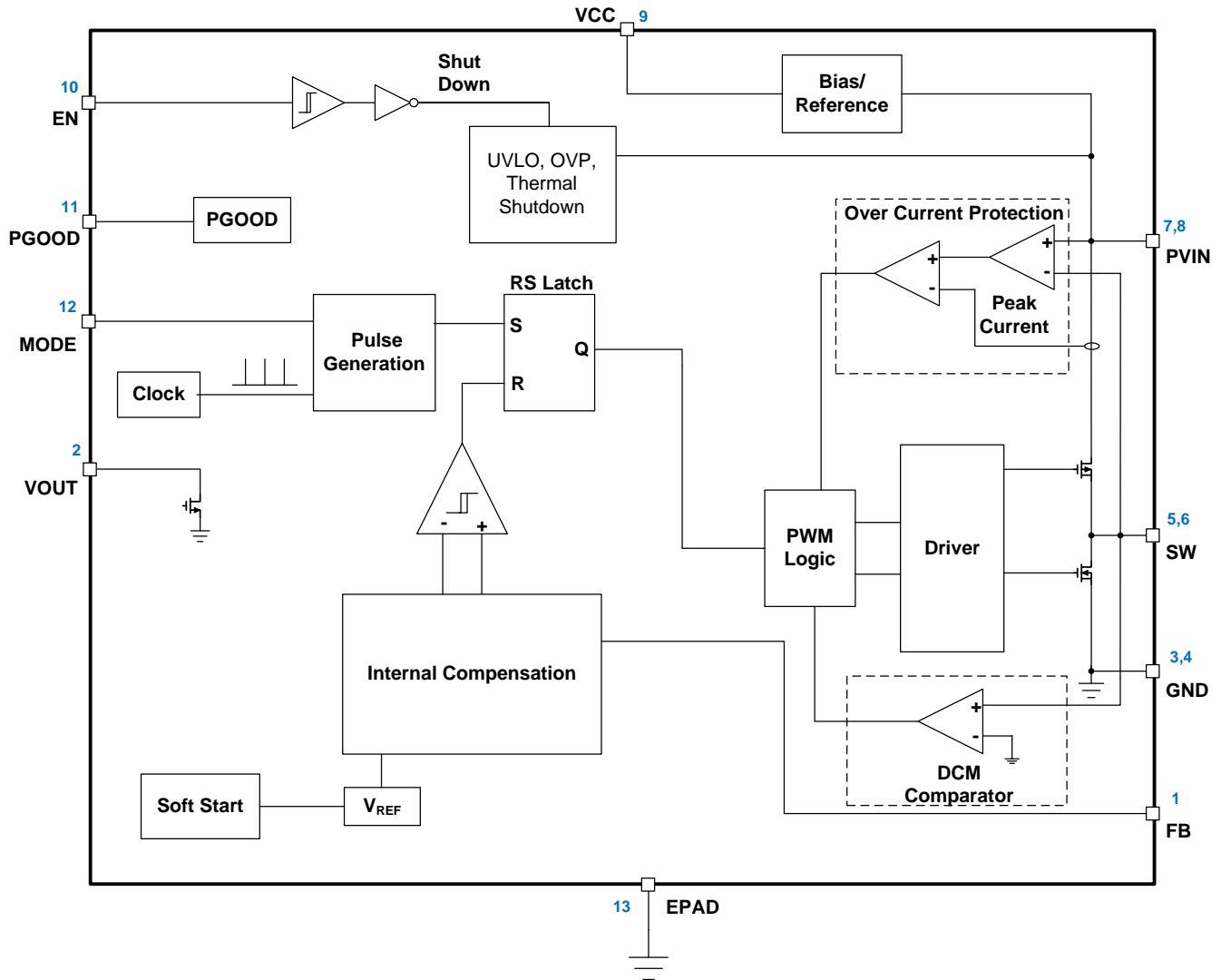
## Pin Description

Pin Number	Pin Designator	Description
1	FB	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired voltage. The upper resistor of the divider is part of the closed loop stability and must be selected properly to insure the stability of the regulator. Table 1 shows the proper values of this network for selected output voltages.
2	VOUT	Output sense pin.
3, 4, 13	GND	Ground pin.
5,6	SW	Switch-node pin. Connect the output inductor between this pin and output capacitor.
7,8	PVIN	Input voltage pin of the regulator. A minimum of 10 $\mu$ F, X5R type ceramic capacitor must be connected as close as possible from this pin to GND plane to insure proper operation.
9	VCC	Internal chip supply. Decouple this pin to GND with a 1 $\mu$ F, X5R type (or better) ceramic capacitor and connect it via a 10 $\Omega$ resistor to the input rail.
10	EN	Pulling this pin higher than 1.7V will enable the regulator. When pulled below 0.4V, the regulator will turn off.
11	PGOOD	Power-good pin. This is an open-drain output and should be connected to a voltage rail (for example, VIN) with an external pull-up resistor. During the power on, this pin switches from low to high state when FB voltage reaches above the power good threshold and the internal soft start has finished its operation. It will be pulled low, when the FB falls below the power good threshold minus the hysteresis. It will turn back on, when the pull FB rises above the threshold.
12	MODE	This PIN should be connected to GND; skip mode is enabled to improve the light load efficiency.



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### Block Diagram



**Figure 3: Block Diagram**


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## Absolute Maximum Ratings

Performance is not necessarily guaranteed over this entire range. These are maximum stress ratings only. Exceeding these ratings, even momentarily, can cause immediate damage, or negatively impact long-term operating reliability.

	Min	Max	Units
PVIN, VCC, EN, FB, PGOOD, VOUT, MODE to GND	-0.3	7	V
SW to GND	-0.3	7	V
SW to GND (Shorter than 50ns)	-2	7	V
Maximum Operating Junction Temperature		150	°C
Storage Temperature Range	-65	150	°C
Lead Soldering Temperature (40s, reflow)		260 (+0, -5)	°C
ESD Protection at all I/O Pins (HBM, Note 1)	-2	2	kV

Note 1: PVIN & SW pins are ESD sensitive.

## Operating Ratings

Performance is generally guaranteed over this range as further detailed below under Electrical Characteristics.

	Min	Max	Units
VCC, PVIN (Note 2)	3	5.5	V
VOUT	0.8	1.8	V
Ambient Temperature	-10	85	°C
Output Current	0	3	A

Note 2: Minimum input voltage 3.5V is required in order to have 3A output current

## Thermal Properties

Thermal Resistance	Min	Typ	Max	Units
$\theta_{JA}$		46		°C/W

**Note:** The  $\theta_{JA}$  numbers assume no forced airflow. Junction Temperature is calculated using  $T_J = T_A + (P_D \times \theta_{JA})$ . In particular,  $\theta_{JA}$  is a function of the PCB construction. The stated number above is for a four-layer board in accordance with JESD-51 (JEDEC).

# 3V Input, High Frequency, 3A Step-Down Converter Production Datasheet


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## Electrical Characteristics

Unless otherwise specified under conditions, the Min and Max ratings stated below apply over the entire specified operating range  $0^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$  of the device. Typical parameter refers to  $T_J = 25^{\circ}\text{C}$ .  
VCC = PVIN = 5V, MODE = GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OPERATING CURRENT</b>						
$I_Q$	Input Current	$I_{LOAD} = 0, V_{FB}=0.8V$		700		$\mu\text{A}$
$I_{IN}$	Input Current at Shut Down	EN = GND		0.1	3	$\mu\text{A}$
<b>VCC INPUT UVLO</b>						
VCC	Under Voltage Lockout	VCC rising		2.6		V
$V_{HYS}$	UVLO Hysteresis			80		mV
<b>FEEDBACK</b>						
$V_{REF}$	Feedback Voltage Internal Reference	$T_A = 25^{\circ}\text{C}$	0.792	0.800	0.808	V
		$-10 < T_A < 85^{\circ}\text{C}$	0.788		0.812	V
$I_{FB}$	FB Pin Input Current				100	nA
	Line Regulation	VIN from 3V to 5.5V, $I_{OUT} = 1.5A$		0.5		%/V
	Load Regulation	$I_{LOAD} = 0$ to 3A,		-0.3		%/A
<b>OUTPUT DEVICE</b>						
$R_{DSON\_H}$	$R_{DSON}$ of High Side			60		m $\Omega$
$R_{DSON\_L}$	$R_{DSON}$ of Low Side			40		m $\Omega$
$I_L$	Current Limit			5.3		A
$T_{SH}$	Thermal Shut Down Threshold			150		$^{\circ}\text{C}$
$T_H$	Hysteresis			20		$^{\circ}\text{C}$
<b>PVIN OVP</b>						
$OVP_R$	Rising Threshold			6.5		V
$OVP_F$	Falling Threshold			6.1		V
<b>FB UVLO</b>						
$V_{FBULVO}$	FB UVLO Threshold			70%		$V_{REF}$

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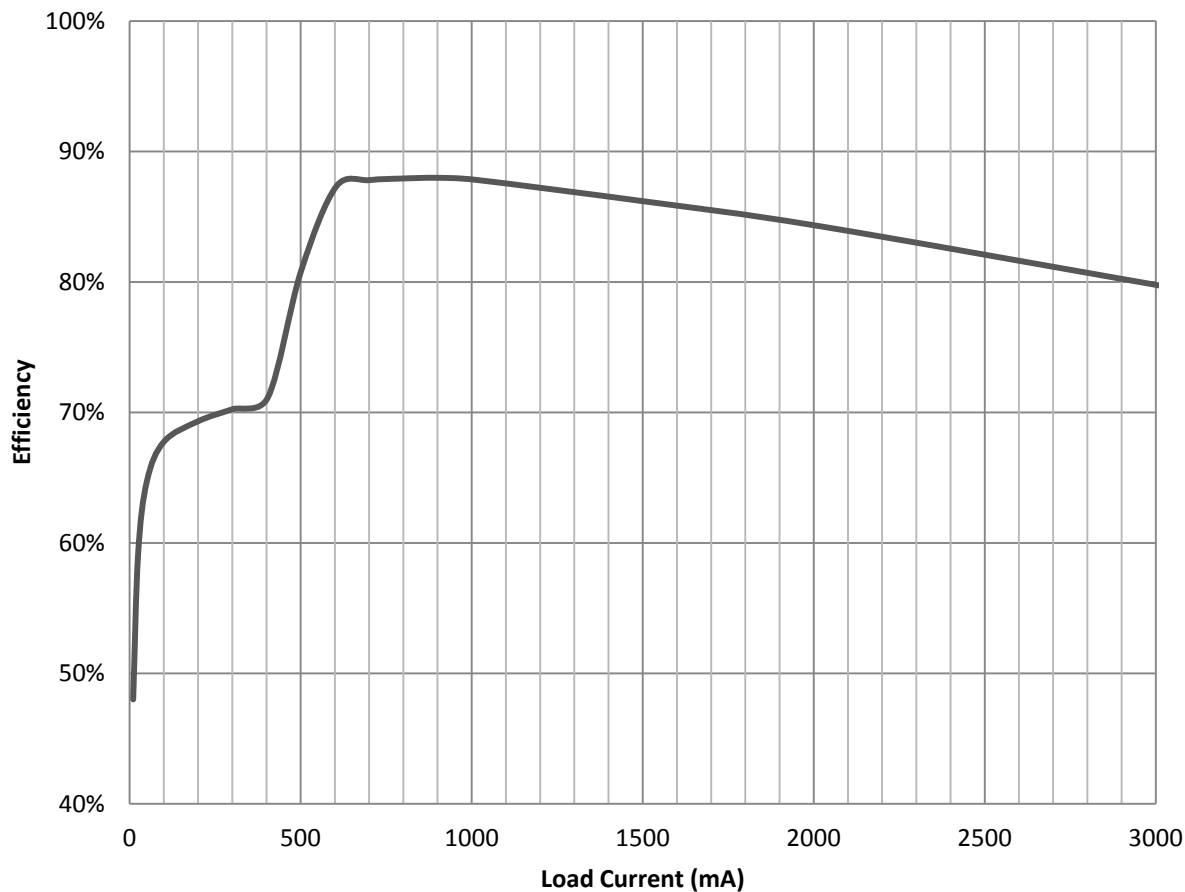
Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OSCILLATOR FREQUENCY</b>						
$f_{sw}$	PWM Switching Frequency Range			2.2		MHz
$f_{FB}$	Switching Frequency at Fold back	$V_{FB} < 0.3V$		0.75		MHz
<b>SOFT START</b>						
$T_{SS}$	Soft Start Time	From EN high to VOUT reach regulation.		465		$\mu s$
$T_{HICCUP}$	Hiccup time	$V_{FB} = 0.2V$		11		ms
<b>EN INPUT</b>						
$EN_{VIH}$	Input High		1.7			V
$EN_{VIL}$	Input Low				0.4	V
$EN_H$	Hysteresis			0.1		V
$EN_{II}$	Input Bias			0.01	1	$\mu A$
<b>POWER-GOOD</b>						
$V_{PG}$	Power-good High Threshold	$V_{FB}$ rising, in percentage of output voltage set-point.		85		%
$V_{PGHY}$	Hysteresis	Either $V_{FB}$ rising or falling		52		mV
$PGD_{filt}$	Power Good filter			6		Clock cycles
$PG_{RDSON}$	Power-good Internal FET $R_{DSON}$	$VCC = 5V$		18		$\Omega$
$I_{PGD}$	PGOOD FET Leakage Current			0.01	1	$\mu A$



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### Typical Efficiency Curve

**LX7157B Efficiency / VIN = 5V, VOUT = 1.2V**



**Figure 4: Efficiency Curve**



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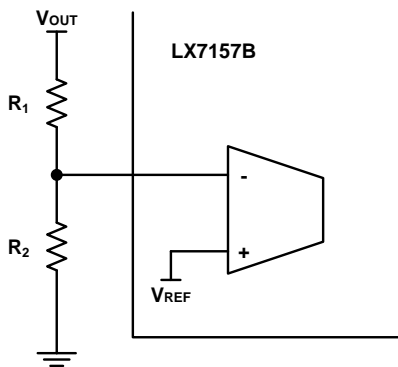
### Application Information

#### Output Voltage Calculation

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of the ratio of two resistors so that the output voltage applied at the FB pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between output voltage and voltage divider.

$$V_{OUT} = V_{REF} \times \left( 1 + \frac{R_1}{R_2} \right) \dots\dots\dots (1)$$

The value of upper feedback resistor  $R_1$  has to be set properly in order to have stable system. The recommended value of  $R_1$  is shown in the table 1,  $R_2$  can be derived from equation 1.



**Figure 5:** Voltage Divider

Output Capacitor	$R_1$ ( $\Omega$ )
2 x 10 $\mu$ F (X5R, 6.3V)	80.6k
3 x 10 $\mu$ F (X5R, 6.3V)	54.9k
2 x 22 $\mu$ F (X5R, 6.3V)	49.9k
3 x 22 $\mu$ F (X5R, 6.3V)	33.2k

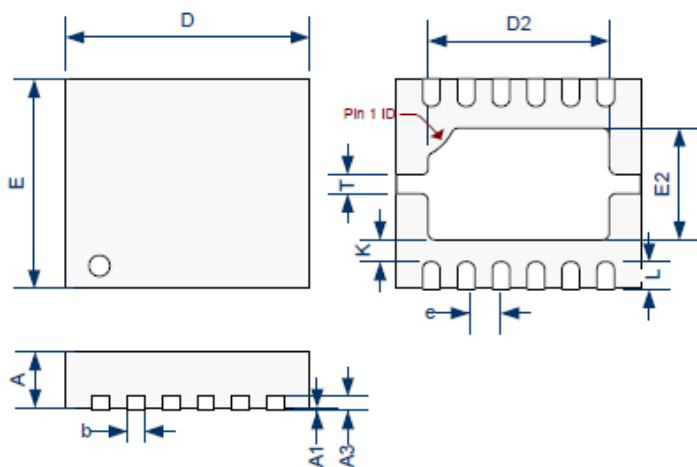
**Table 1:** Recommended upper resistor value of feedback resistor divider for typical application ( $L = 0.47\mu$ H)



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### Package Dimensions

12-Pin Plastic DFN 3.5mm x 3mm with Exposed Pad




Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.027	0.031
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.50 BSC		0.138 BSC	
D2	2.45	2.70	0.096	0.106
e	0.50 BSC		0.019 BSC	
E	3.00 BSC		0.118 BSC	
E2	1.45	1.70	0.057	0.067
L	0.35	0.55	0.014	0.022
T	0.20	0.30	0.008	0.012

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