



**THE DATASHEET OF
A8837EEJTR-T**

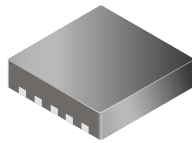


Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

- Power with 1 Li+ or 2 Alkaline/NiMH/NiCAD batteries
- Eight-level, digitally-programmable current limits from 700 mA to 2 A
- Voltage sensing feedback before output diode for low leakage
- Adjustable output voltage
- No primary-side Schottky diode needed
- Integrated IGBT driver with trigger
- Charge complete indication
- >75% efficiency
- Low-profile (0.75 mm high) 3 mm × 3 mm MLP/TDFN 10-contact package

Package: 10-contact TDFN/MLP (suffix EJ)



Approximate Scale



Description

The A8837 is a highly integrated IC that charges photoflash capacitors for digital and film cameras. An integrated MOSFET switch drives the transformer in a flyback topology. It also features an integrated IGBT driver that facilitates the flash discharge function and saves board space.

The CHARGE pin enables the A8837 and starts the charging of the output capacitor. When the designated output voltage is reached, the A8837 stops the charging until the CHARGE pin is toggled again. The DONE pin is an open-drain indicator of when the designated output voltage is reached.

The peak current limit can be adjusted to eight different levels between 700 mA and 2 A, by clocking the CHARGE pin. This allows the user to operate the flash even at low battery voltages.

The A8837 can be used with two Alkaline/NiMH/NiCAD or one single-cell Li+ battery connected to the transformer primary. Connect the VIN pin to a 3.0 to 5.5 V supply, which can be either the system rail or the Li+ battery, if used.

The A8837 is available in a very low profile (0.75 mm) 10-contact 3 mm × 3 mm MLP/TDFN package, making it ideal for space-constrained applications. It is lead (Pb) free, with 100% matte-tin leadframe plating.

Applications include the following:

- Digital camera flash
- Cell phone flash
- Film camera flash
- Emergency strobe light

Typical Applications

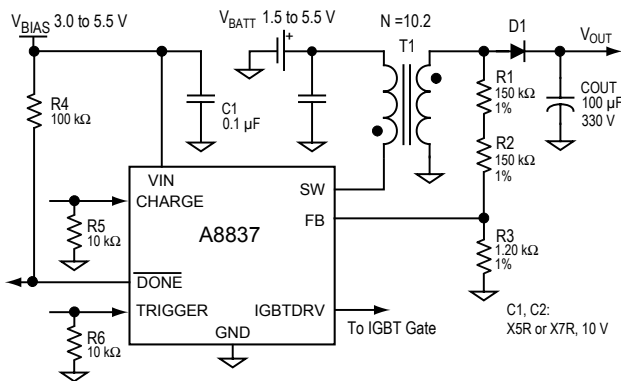


Figure 1. Typical circuit with separate power supply to transformer

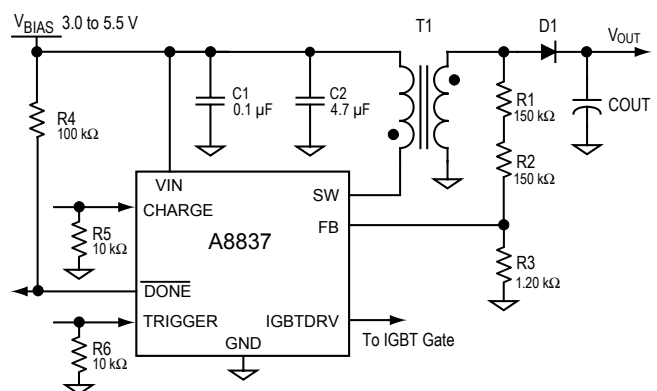


Figure 2. Typical circuit with single power supply

Selection Guide

Part Number	Package	Packing*
A8837EEJTR-T	10-pin TDFN/MLP	1500 pieces/ 7-in. reel

*Contact Allegro for additional packing options



Absolute Maximum Ratings

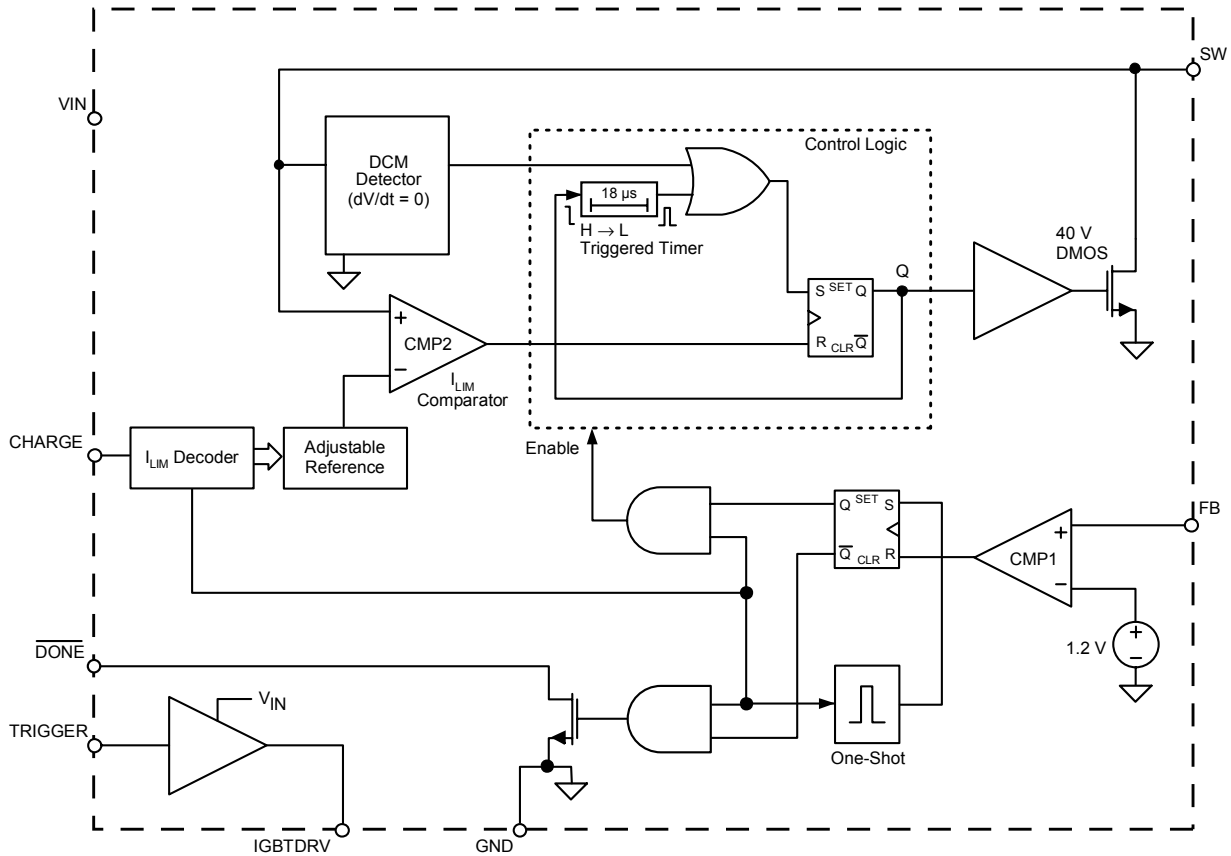
Characteristic	Symbol	Notes	Rating	Units
SW pin	V_{SW}		-0.3 to 40	V
IGBTDRV pin	$V_{IGBTDRV}$		-0.3 to $V_{IN} + 0.3$	V
FB pin	V_{FB}		-0.3 to V_{IN}	V
All other pins	V_X		-0.3 to 7	V
Operating Ambient Temperature	T_A	Range E	-40 to 85	°C
Maximum Junction Temperature	$T_J(max)$		150	°C
Storage Temperature	T_{stg}		-55 to 150	°C

Package Thermal Characteristics

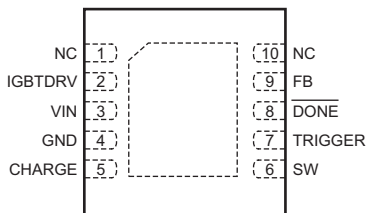
Characteristic	Symbol	Test Conditions*	Rating	Units
Package Thermal Resistance	$R_{\theta JA}$	4layer PCB, based on JEDEC standard	45	°C/W

*Additional information is available on the Allegro website.

Functional Block Diagram



Device Pin-out Diagram



Terminal List Table

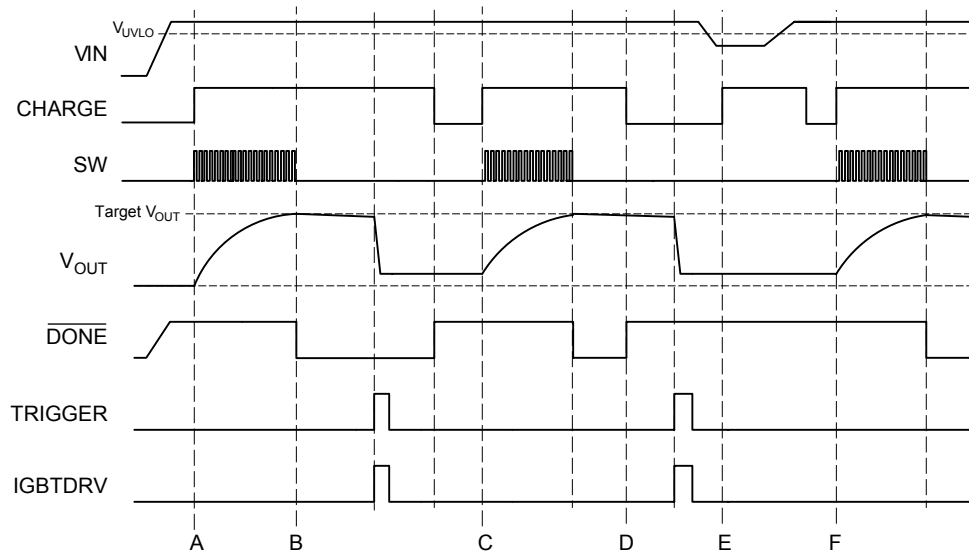
Number	Name	Function
1,10	NC	No connection
2	IGBTDRV	IGBT driver gate drive output
3	VIN	Power supply input
4	GND	Device ground
5	CHARGE	Charging enable and ISWLIM code input; set to low to power-off the A8837
6	SW	Switch, internally connected to the DMOS power FET drain
7	TRIGGER	Strobe signal input
8	$\overline{\text{DONE}}$	Open drain, when pulled low by internal MOSFET, indicates that charging target level has been reached
9	FB	Output voltage feedback

ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$ and $V_{IN} = 3.3\text{ V}$ (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage*	V_{IN}		3	–	5.5	V
Supply Current	I_{IN}	Charging	–	1.5	–	mA
		Charging done	–	1	10	μA
		Shutdown ($V_{CHARGE} = 0\text{ V}$, $V_{TRIGGER} = 0\text{ V}$)	–	0.01	1	μA
Primary Side Current Limit (ILIM clock input at CHARGE pin)	I_{SWLIM1}		1.8	2.0	2.2	A
	I_{SWLIM2}		–	1.8	–	A
	I_{SWLIM3}		–	1.6	–	A
	I_{SWLIM4}		–	1.4	–	A
	I_{SWLIM5}		–	1.2	–	A
	I_{SWLIM6}		–	1	–	A
	I_{SWLIM7}		–	0.86	–	A
	I_{SWLIM8}		–	0.7	–	A
SW On Resistance	$R_{DS(On)SW}$	$V_{IN} = 3.3\text{ V}$, $I_D = 800\text{ mA}$	–	0.27	–	Ω
SW Leakage Current*	I_{SWLKG}	$V_{SW} = 35\text{ V}$	–	–	1	μA
SW Maximum Off-Time	$t_{OFF(Max)}$		–	18	–	μs
SW Maximum On-Time	$t_{ON(Max)}$		–	18	–	μs
CHARGE Input Current	I_{CHARGE}	$V_{CHARGE} = V_{IN}$	–	–	1	μA
CHARGE Input Voltage*	$V_{CHARGE(H)}$		2	–	–	V
	$V_{CHARGE(L)}$		–	–	0.8	V
ILIM Clock High Time at CHARGE Pin	$t_{ILIM1(H)}$	Initial pulse	20	–	–	μs
	$t_{ILIM(H)}$	Subsequent pulses	0.2	–	–	μs
ILIM Clock Low Time at CHARGE Pin	$t_{ILIM(L)}$		0.2	–	–	μs
Total ILIM Setup Time	$t_{ILIM(SU)}$		–	54	–	μs
$\overline{\text{DONE}}$ Output Leakage Current*	$I_{DONELKG}$		–	–	1	μA
$\overline{\text{DONE}}$ Output Low Voltage*	$V_{DONE(L)}$	32 μA into $\overline{\text{DONE}}$ pin	–	–	100	mV
FB Voltage Threshold*	V_{FB}		1.187	1.205	1.223	V
FB Input Current	I_{FB}	$V_{FB} = 1.205\text{ V}$	–	–120	–	nA
UVLO Enable Threshold	V_{UVLO}	V_{IN} rising	2.55	2.65	2.75	V
UVLO Hysteresis	$V_{UVLOHYS}$		–	150	–	mV
IGBT Driver						
IGBTDRV On Resistance to V_{IN}	$R_{DS(On)I-V}$	$V_{IN} = 3.3\text{ V}$, $V_{IGBTDRV} = 1.5\text{ V}$, $V_{TRIGGER} = V_{IN}$	–	5	–	Ω
IGBTDRV On Resistance to GND	$R_{DS(On)I-G}$	$V_{IN} = 3.3\text{ V}$, $V_{IGBTDRV} = 1.5\text{ V}$, $V_{TRIGGER} = 0\text{ V}$	–	6	–	Ω
TRIGGER Input Current	$I_{TRIGGER}$	$V_{TRIGGER} = V_{IN}$	–	–	1	μA
TRIGGER Input Voltage*	$V_{TRIGGER(H)}$		2	–	–	V
	$V_{TRIGGER(L)}$		–	–	0.8	V
Propagation Delay, Rising	t_{Dr}	$R_{gate} = 12\ \Omega$, $C_{LOAD} = 6500\text{ pF}$, $V_{IN} = 3.3\text{ V}$	–	30	–	ns
Propagation Delay, Falling	t_{Df}	$R_{gate} = 12\ \Omega$, $C_{LOAD} = 6500\text{ pF}$, $V_{IN} = 3.3\text{ V}$	–	30	–	ns
Output Rise Time	t_r	$R_{gate} = 12\ \Omega$, $C_{LOAD} = 6500\text{ pF}$, $V_{IN} = 3.3\text{ V}$	–	70	–	ns
Output Fall Time	t_f	$R_{gate} = 12\ \Omega$, $C_{LOAD} = 6500\text{ pF}$, $V_{IN} = 3.3\text{ V}$	–	70	–	ns
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	30	–	V/ μs

*Guaranteed by design and characterization over operating temperature range, -40°C to 85°C .

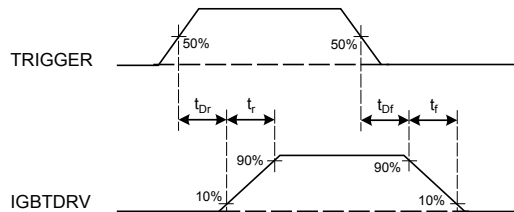
Operation Timing Diagram



Explanation of Events:

- A. Start charging by pulling CHARGE to high, provided that V_{IN} is above the V_{UVLO} level.
- B. Charging stops when V_{OUT} reaches the target voltage. \overline{DONE} goes low, to signal the completion of the charging process.
- C. Start a new charging process with a low-to-high transition at the CHARGE pin.
- D. Pull CHARGE to low, to put the controller in low-power standby mode.
- E. Charging does not start, because V_{IN} is below V_{UVLO} level when CHARGE goes high.
- F. After V_{IN} goes above V_{UVLO} , another low-to-high transition at the CHARGE pin is required to start charging.

IGBT Drive Timing Definition



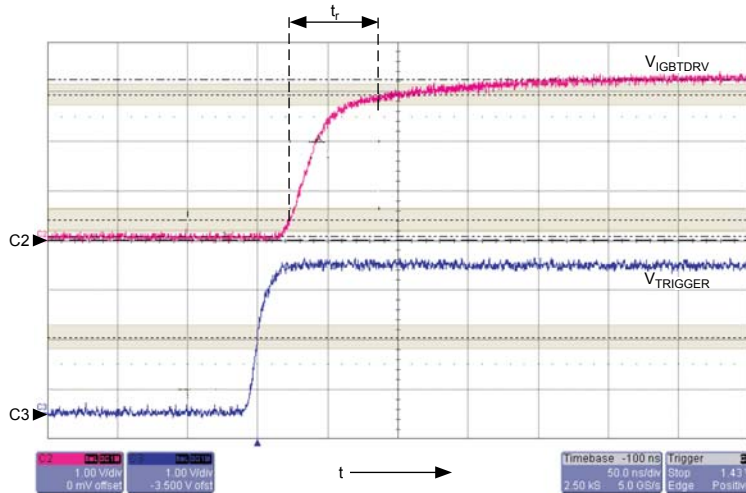
Performance Characteristics

IGBT Drive waveforms are measured with R-C load (12 Ω, 6800 pF)

IGBT Drive Performance

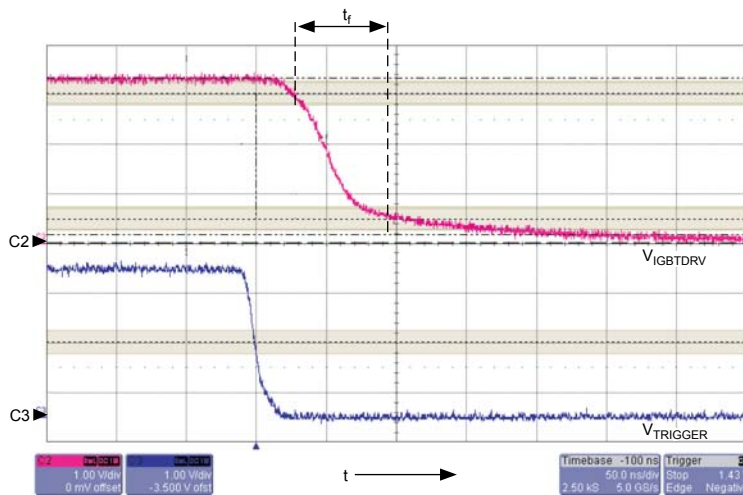
Rising Signal

Symbol	Parameter	Units/Division
C2	V _{IGBTDRV}	1 V
C3	V _{TRIGGER}	1 V
t	time	50 ns
Conditions	Parameter	Value
	t _{Dr}	22.881 ns
	t _r	63.125 ns
	C _{LOAD}	6800 pF
	R _{gate}	12 Ω



Falling Signal

Symbol	Parameter	Units/Division
C2	V _{IGBTDRV}	1 V
C3	V _{TRIGGER}	1 V
t	time	50 ns
Conditions	Parameter	Value
	t _{Dr}	27.427 ns
	t _f	65.529 ns
	C _{LOAD}	6800 pF
	R _{gate}	12 Ω



Functional Description

Overview

The A8837 is a photoflash capacitor charger control IC with adjustable input current limiting. It also integrates an IGBT driver for strobe operation of the flash tube, dramatically saving board space in comparison to discrete solutions for strobe flash operation. The control logic is shown in the functional block diagram.

The charging operation of the A8837 is started by a low-to-high signal on the CHARGE pin, provided that V_{IN} is above V_{UVLO} level. If CHARGE is already high before V_{IN} reaches V_{UVLO} , another low-to-high transition on the CHARGE pin is required to start the charging. The primary peak current is set by input clock signals from the CHARGE pin. When a charging cycle is initiated, the transformer primary side current, $I_{Primary}$, ramps up linearly at a rate determined by the combined effect of the battery voltage, V_{BATT} , and the primary side inductance, $L_{Primary}$. When $I_{Primary}$ reaches the current limit, I_{SWLIM} , the internal MOSFET is turned off immediately, allowing the energy to be pushed into the photoflash capacitor, C_{OUT} , from the secondary winding. The secondary side current drops linearly as C_{OUT} charges. The switching cycle starts again, either after the transformer flux is reset, or after a predetermined time period, $t_{OFF(Max)}$ (18 μ s), whichever occurs first.

The output voltage, V_{OUT} , is sensed by a resistor string, R_1 , R_2 , and R_3 (see application circuit diagrams), connected across the transformer secondary winding. This resistor string forms a voltage divider that feeds back to the FB pin. The resistors must be sized to achieve a desired output voltage level based on a typical value of 1.205 V at the FB pin. As soon as V_{OUT} reaches the desired value, the charging process is terminated. Toggling the CHARGE pin can start a refresh operation.

Input Current Limiting

The peak current limit can be adjusted to eight different levels, from 700 mA to 2.0 A, by clocking the CHARGE pin. An internal digital circuit decodes the input clock signals to a counter, which sets the charging time. This flexible scheme allows the user to operate the flash circuit according to different battery

input voltages. The battery life can be effectively extended by setting a lower current limit at low battery voltages.

Figure 4 shows the ILIM clock timing scheme protocol. The total ILIM setup time, $t_{ILIM(SU)}$, denotes the time needed for the decoder circuit to receive ILIM inputs and set I_{SWLIM} . Apply current limit pulses during $t_{ILIM(SU)}$ (54 μ s) period.

Figure 5 shows the timing definition of the primary current limiting circuit. At the end of the setup period, $t_{ILIM(SU)}$, primary

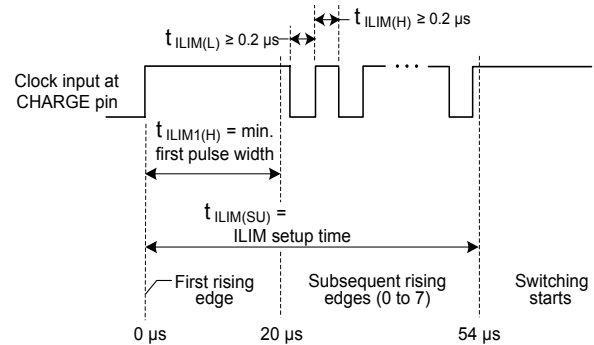


Figure 4. ILIM Clock Timing Definition

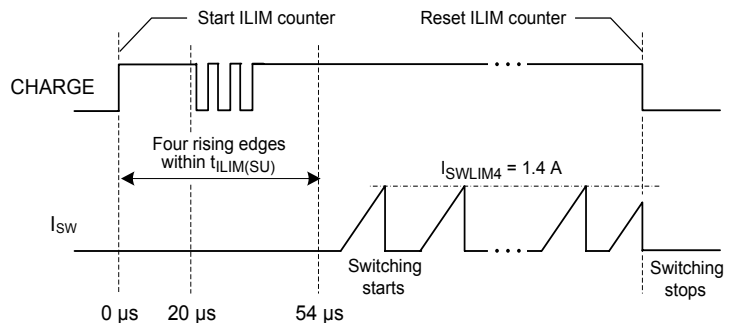


Figure 5. Current Limit Programming Example (I_{SWLIM4} selected).

current starts to ramp up to the set I_{SWLIM} . The I_{SWLIM} setting remains in effect as long as the CHARGE pin is high. To reset the ILIM counter, pull the CHARGE pin low before clocking in the new setting.

After the first start-up or an ILIM counter reset, each new current limit can be set by sending a burst of pulses to the CHARGE pin. The first rising edge starts the ILIM counter, and up to 8 rising edges will be counted to set the I_{SWLIM} level. The first pulse width, $t_{ILIM1(H)}$, must be at least 20 μs long. Subsequent pulses (up to 7 more) can be as short as 0.2 μs . The last low-to-high edge must arrive within 54 μs from the first edge. The CHARGE pin will stay high afterwards.

Figure 6 shows the last charging cycle, when the CHARGE pin is forced low before charging has been completed.

The A8837 implements an adaptive off-time, t_{OFF} , control. After the switch is turned off, a sensing circuit tracks the flyback voltage at the SW node. A special dV/dt detection circuit is used to allow minimum-voltage switching, even if the SW voltage does not drop to zero volts. This enables fast-charging to start earlier than previously possible, thereby reducing the overall charging time. However, when the photoflash capacitor charger circuit starts up at low output voltage, a timeout may be triggered to limit the maximum switch off-time to 18 μs .

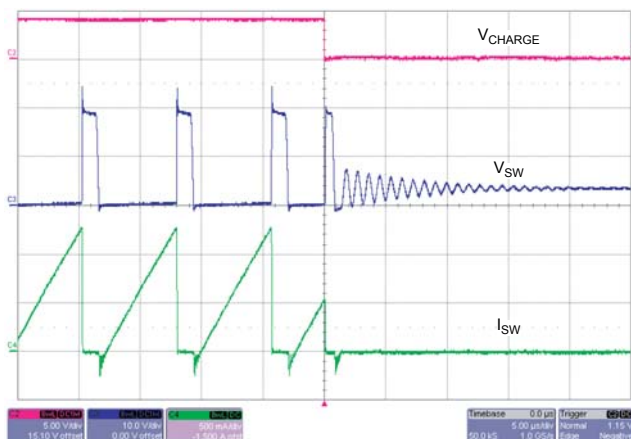


Figure 6. Last charging cycle, when the CHARGE pin is forced low before charging is complete.

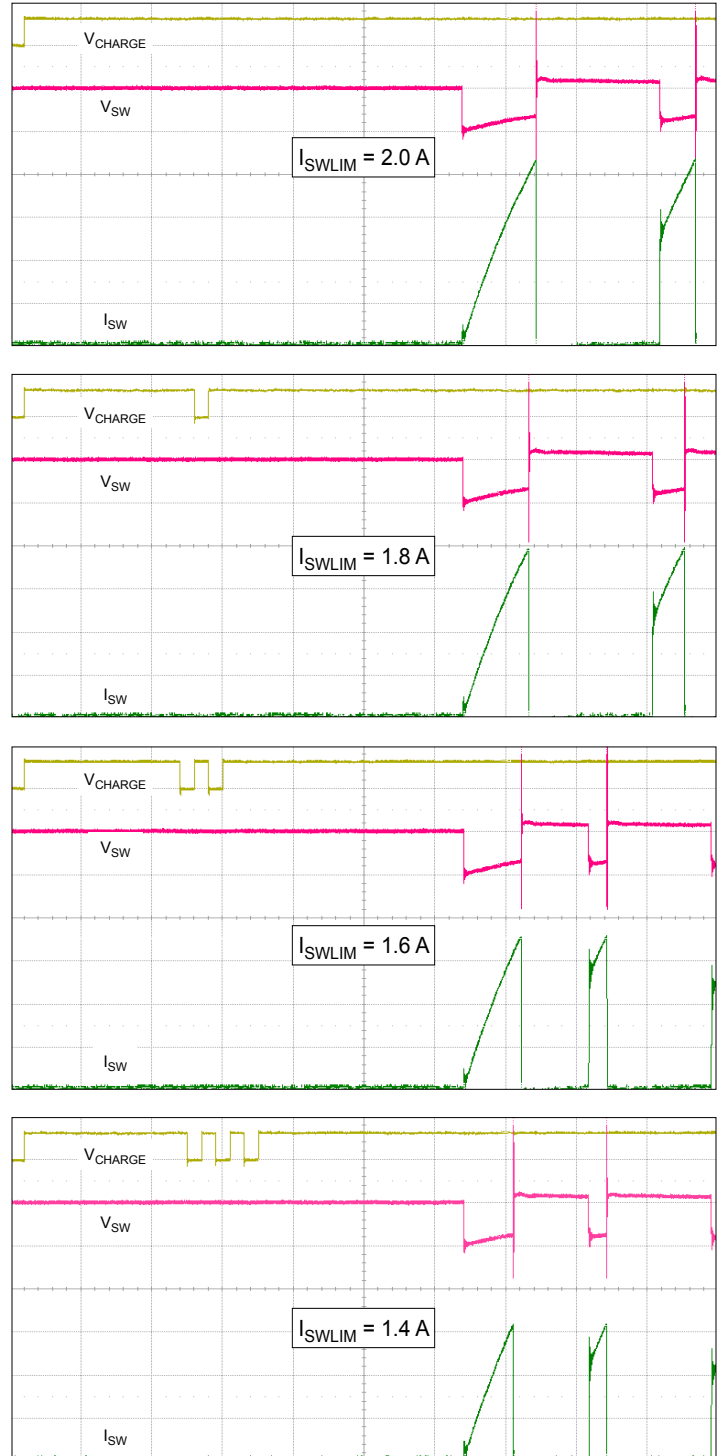


Figure 7. ILIM programming waveforms for various I_{SWLIM} ; $V_{IN} = 3.3 V$, $V_{BAT} = 2.0 V$, $V_{CHARGE} 5 V/div$, $V_{SW} 2 V/div$, $I_{SW} 500 mA/div$, time scale 10 $\mu s/div$.

Applications Information

Transformer Design

Turns Ratio. The minimum transformer turns ratio, N , (Secondary : Primary) should be chosen based on the following formula:

$$N \geq \frac{V_{OUT} + V_{D_Drop}}{40 - V_{BATT}} \quad (1)$$

where:

V_{OUT} (V) is the required output voltage level,
 V_{D_Drop} (V) is the forward voltage drop of the output diode(s),
 V_{BATT} (V) is the transformer battery supply, and
 40 (V) is the rated voltage for the internal MOSFET switch,
 representing the maximum allowable reflected voltage from the output to the SW pin.

For example, if V_{BATT} is 3.5 V and V_{D_Drop} is 1.7 V (which could be the case when two high voltage diodes were in series), and the desired V_{OUT} is 320 V, then the turns ratio should be at least 8.9.

In a worst case, when V_{BATT} is highest and V_{D_Drop} and V_{OUT} are at their maximum tolerance limit, N will be higher. Taking $V_{BATT} = 5.5$ V, $V_{D_Drop} = 2$ V, and $V_{OUT} = 320$ V \times 102 % = 326.4 V as the worst case condition, N can be determined to be 9.5.

In practice, always choose a turns ratio that is higher than the calculated value to give some safety margin. In the worst case example, a minimum turns ratio of $N = 10$ is recommended.

Primary Inductance. As a loose guideline when choosing the primary inductance, $L_{Primary}$ (μ H), use the following formula:

$$L_{Primary} \geq \frac{300 \times 10^{-9} \times V_{OUT}}{N \times I_{SWLIM}} \quad (2)$$

Ideally, the charging time is not affected by transformer primary inductance. In practice, however, it is recommended that a primary inductance be chosen between 10 μ H and 20 μ H. When $L_{Primary}$ is lower than 10 μ H, the converter operates at higher frequency, which increases switching loss proportionally. This leads to lower efficiency and longer charging time. When $L_{Primary}$ is greater than 20 μ H, the rating of the transformer must be dramatically increased to handle the required power density, and the series resistances are usually higher. A design that is optimized to achieve a small footprint solution would have an $L_{Primary}$ of 12 to 14 μ H, with minimized leakage inductance and secondary capacitance, and minimized primary and secondary series resistance. See the table Recommended Components for more information.

Recommended Components

Component	Rating	Part Number	Source	Remarks
C1, Input Capacitor	0.1 μ F, \pm 10%, 16 V X7R ceramic capacitor (0603)	GRM188R71C104KA01D	Murata	10 V minimum rating can be used
C2, Input Capacitor	4.7 μ F, \pm 10%, 10 V, X5R ceramic capacitor (0805)	LMK212BJ475KG	Taiyo Yuden	
COUT, Photoflash Capacitor	330 V 100 μ F (or 19 to 180 μ F)	EPH-331ELL101B131S	Chemi-Con	
D1, Output Diode	2 x 250 V, 225 mA, 5 pF	BAV23S	Philips Semiconductor, Fairchild Semiconductor	
R1, R2, FB Resistors	150 k Ω each $\frac{1}{4}$ W, \pm 1%; 1206, 0805, or 0603 resistors rated for 150 V			Instead of two resistors, a single 300 k Ω resistor with 350 V rating can be used
R3, FB Resistor	1.2 k Ω $\frac{1}{10}$ W \pm 1% (0603 or 0402)			
T1, Transformer	$L_P = 14.2$ μ H, $I_P = 2$ A, $N = 10$	T-15-154M	Tokyo Coil	Suitable for I_{LIM} from 0.7 to 2.0 A
	$L_P = 7.4$ μ H, $I_P = 2$ A, $N = 10$	T-16-103A	Tokyo Coil	Suitable for I_{LIM} from 1.2 to 2.0 A only
	$L_P = 14$ μ H, $I_P = 1.5$ A, $N=10$	ST-652956A	Asatech	Suitable for I_{LIM} from 0.7 to 1.4 A only

Leakage Inductance and Secondary Capacitance. The transformer design should minimize the leakage inductance to ensure the turn-off voltage spike at the SW node does not exceed the 40 V limit. An achievable minimum leakage inductance for this application, however, is usually compromised by an increase in parasitic capacitance. Furthermore, the transformer secondary capacitance should be minimized. Any secondary capacitance is multiplied by N^2 when reflected to the primary, leading to high initial current swings when the switch turns on, and to reduced efficiency.

Adjusting Output Voltage

The A8436 senses output voltage during switch off-time. This allows the voltage divider network, R1 through R3, to be connected at the anode of the high voltage output diode, D1, eliminating power loss due to the feedback network when charging is complete. The output voltage can be adjusted by selecting proper values of the voltage divider resistors. Use the following equation to calculate values for Rx (Ω):

$$\frac{R_1 + R_2}{R_3} = \frac{V_{OUT}}{V_{FB}} - 1 \quad (3)$$

R1 and R2 together need to have a breakdown voltage of at least 300 V. A typical 1206 surface mount resistor has a 150 V breakdown voltage rating. It is recommended that R1 and R2 have similar values to ensure an even voltage stress between them.

Recommended values are:

$$R1 = R2 = 150 \text{ k}\Omega \text{ (1206)}$$

$$R3 = 1.2 \text{ k}\Omega \text{ (0603)}$$

which together yield a stop voltage of 303 V. Using higher resistance values for R1, R2, and R3 does not offer significant efficiency improvement, because the power loss of the feedback network occurs mainly during switch off-time, and because the off-time is only a small fraction of each charging cycle.

Output Diode Selection

Choose the rectifying diode(s), D1, to have small parasitic capacitance (short reverse recovery time) while satisfying the reverse voltage and forward current requirements.

The peak reverse voltage of the diode, V_{D_Peak} , occurs when the internal MOSFET switch is closed, and the primary-side current starts to ramp-up. It can be calculated as:

$$V_{D_Peak} = V_{OUT} + N \times V_{BATT} \quad (4)$$

The peak current of the rectifying diode, I_{D_Peak} , is calculated as:

$$I_{D_Peak} = I_{Primary_Peak} / N \quad (5)$$

Input Capacitor Selection

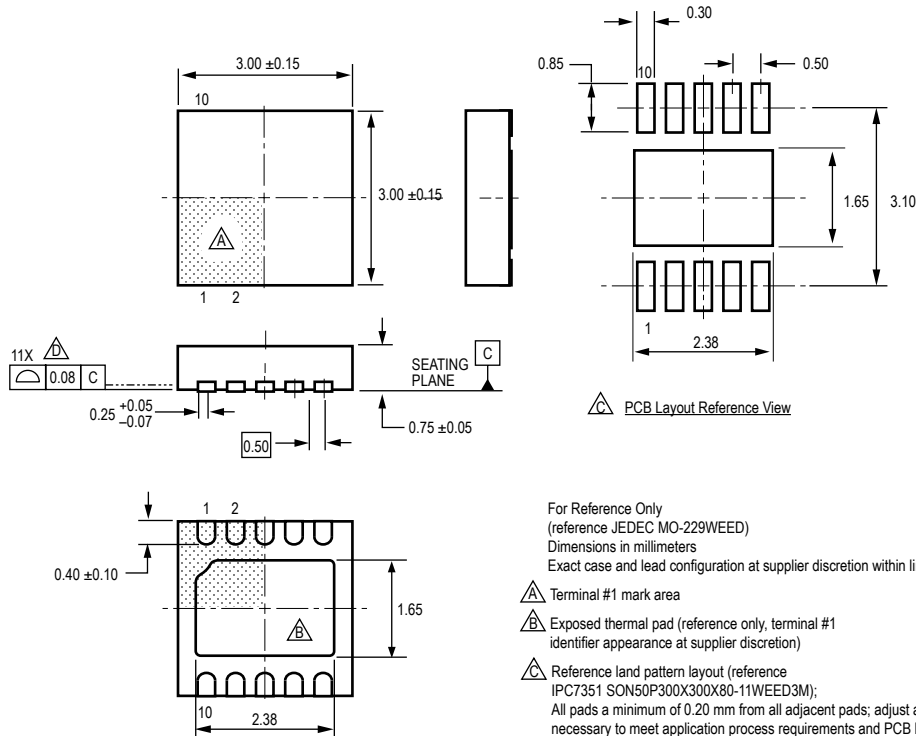
Ceramic capacitors with X5R or X7R dielectrics are recommended for the input capacitor, C2. It should be rated at least 4.7 μ F/6.3 V to decouple the battery input, V_{BATT} , at the primary of the transformer. When using a separate bias, V_{BIAS} , for the A8837 VIN supply, connect at least a 0.1 μ F/6.3 V bypass capacitor to the VIN pin.

Layout Guidelines

Key to a good layout for the photoflash capacitor charger circuit is to keep the parasitics minimized on the power switch loop (transformer primary side) and the rectifier loop (secondary side). Use short, thick traces for connections to the transformer primary and SW pin.

Output voltage sensing circuit elements must be kept away from switching nodes such as SW pin. Make sure that there is no ground plane underneath R1 and R2, because parasitic capacitance to ground will affect sensing accuracy. It is important that the \overline{DONE} signal trace and other signal traces be routed away from the transformer and other switching traces, in order to minimize noise pickup. In addition, high voltage isolation rules must be followed carefully to avoid breakdown failure of the circuit board.

Package EJ, 10-Contact TDFN/MLP



For Reference Only
(reference JEDEC MO-229WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

- △ Terminal #1 mark area
- △ Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- △ Reference land pattern layout (reference IPC7351 SON50P300X300X80-11WEED3M); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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