THE DATASHEET OF

MAX14656EWE+T

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EVALUATION KIT AVAILABLE

MAX14656

USB Charger Detection with Integrated Overvoltage Protector

General Description

The MAX14656 is a USB charger detector compliant with USB Battery Charging Specification Revision 1.2. The USB charger detection circuitry detects USB standard downstream ports (SDPs), USB charging downstream ports (CDPs), or dedicated charger ports (DCPs), and controls an external lithium-ion (Li+) battery charger.

The device implements USB Battery Charging Specification Revision 1.2-compliant detection logic. The device also includes Apple® charger detection that allows identification of resistor divider networks on D+/D-.

The internal double-pole double-throw (DPDT) USB switch is compliant to Hi-Speed USB, full-speed USB, low-speed USB, and UART signals. The device's internal switch features low on-resistance, low on-resistance flatness, and very low capacitance. The ID pin controls the DPDT switch position. The MAX14656 features high-ESD protection up to ±15kV Human Body Model (HBM)on CD+, CD-, and ID pins.

The MAX14656 is available in a 16-bump, 0.4mm pitch, 1.8mm x 1.9mm WLP package and operates over the -40ºC to +85ºC extended temperature range.

Applications

- DSCs and Camcorders
- Tablet PCs
- Smartphones
- e-Readers

Benefits and Features

- Consumes Less Power
  - Low Battery Standby Current 5µA (typ)
- Delivers USB Compliance and Flexibility
  - Compliant to USB Battery Charging Specification Revision 1.2
  - Data Contact Detection for Foolproof Connector Insertion Detection
  - Dedicated Charger Detection
  - Standard Downstream Port Detection
  - Charging Downstream Port Detection
  - Apple Charger Detection
  - Sony® Charger Detection*
- Facilitates System Design
  - Integrated Precision 1.5A Overvoltage Protection (OVP)
  - Negative Audio Capable DPDT Hi-Speed USB Switches
  - Automatic Switch and Charger Interface Control
  - Full Control by I^2C Interface
  - Interrupt for Device Status Change
- Saves Board Space
  - V_{BUS} Connection Capable of 36V
  - ±15kV HBM ESD Protection
  - 1.8mm x 1.9mm WLP Package

***Ordering Information* and *Typical Operating Circuit* appears at end of data sheet.**

**Contact factory for the list of compatible chargers.*

Apple is a registered trademark of Apple, Inc.
Sony is a registered trademark and registered service mark of Kabushiki Kaisha TA Sony Corporation.

19-6569; Rev 2; 8/17

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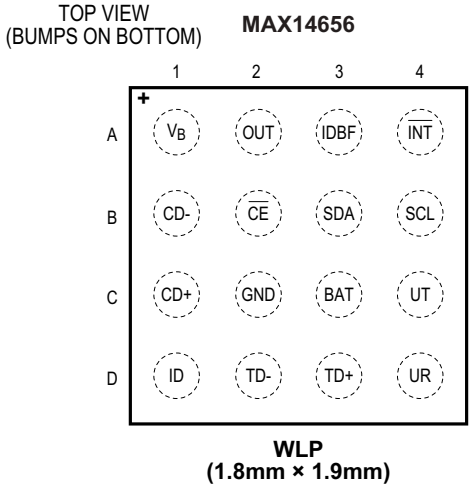
Bump Configuration



WLP
(1.8mm × 1.9mm)

Bump Description

BUMP	NAME	FUNCTION
A1	V_B	USB Connector V_{BUS} Connection. Bypass V_B with a 1µF capacitor to GND.
A2	OUT	Overvoltage-Protected USB Transceiver V_{BUS} Power Output. Bypass OUT with a 1µF capacitor to GND.
A3	IDBF	Push-Pull Digital ID Buffer Output
A4	$\overline{INT}$	Active-Low, Open-Drain, Interrupt Request Fault Output. Connect $\overline{INT}$ to an external pullup resistor.
B1	CD-	USB Connector D- Connection
B2	$\overline{CE}$	Active-Low, Open-Drain, Charger Control Enable Output. Connect $\overline{CE}$ to an external pullup resistor.
B3	SDA	I^2C Serial-Data Input/Output. Connect SDA to an external pullup resistor.
B4	SCL	I^2C Serial-Clock Input. Connect SCL to an external pullup resistor.
C1	CD+	USB Connector D+ Connection
C2	GND	Ground
C3	BAT	Battery Connection Input. Bypass BAT with a 1µF capacitor to GND.
C4	UT	UART Tx Line from Device
D1	ID	USB Connector ID Connection. Bypass ID with a 1nF (max) capacitor to GND.
D2	TD-	USB Transceiver D- Connection
D3	TD+	USB Transceiver D+ Connection
D4	UR	UART Rx Line from Device

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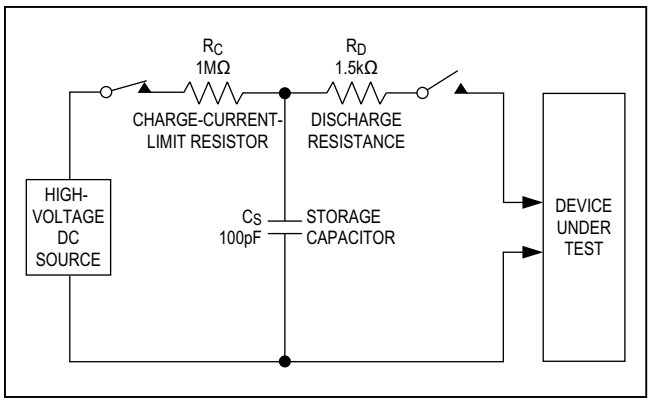

Figure 11. Human Body ESD Test Model

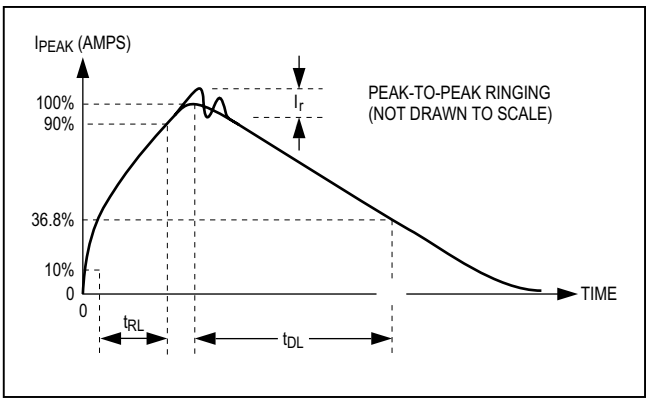

Figure 12. Human Body Current Waveform

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 11 shows the Human Body Model, and Figure 12 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a 1.5kI resistor.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14656EWE+T	-40°C to +85°C	16 WLP	AAG

+Denotes a lead(Pb)-free/RoHS-compliant package.

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 WLP	W161C1+1	21-0491	Refer to Application Note 1891

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