THE DATASHEET OF

AD9640ABCPZ-80

www.win-source.net 0086-755-83957316

14-Bit, 80/105/125/150 MSPS, 1.8 V Dual Analog-to-Digital Converter

AD9640

FEATURES

- SNR = 71.8 dBc (72.8 dBFS) to 70 MHz @ 125 MSPS
- SFDR = 85 dBc to 70 MHz @ 125 MSPS
- Low power: 750 mW @ 125 MSPS
- SNR = 71.6 dBc (72.6 dBFS) to 70 MHz @ 150 MSPS
- SFDR = 84 dBc to 70 MHz @ 150 MSPS
- Low power: 820 mW @ 150 MSPS
- 1.8 V analog supply operation
- 1.8 V to 3.3V CMOS output supply or 1.8 V LVDS output supply
- Integer 1 to 8 input clock divider
- IF sampling frequencies to 450 MHz
- Internal ADC voltage reference
- Integrated ADC sample-and-hold inputs
- Flexible analog input range: 1 V p-p to 2 V p-p
- Differential analog inputs with 650 MHz bandwidth
- ADC clock duty cycle stabilizer
- 95 dB channel isolation/crosstalk
- Serial port control
- User-configurable, built-in self-test (BIST) capability
- Energy-saving power-down modes
- Integrated receive features
  - Fast detect/threshold bits
  - Composite signal monitor

APPLICATIONS

- Communications
- Diversity radio systems
- Multimode digital receivers
  - GSM, EDGE, WCDMA, LTE, CDMA2000, WiMAX, TD-SCDMA
- I/Q demodulation systems
- Smart antenna systems
- General-purpose software radios
- Broadband data applications

FUNCTIONAL BLOCK DIAGRAM

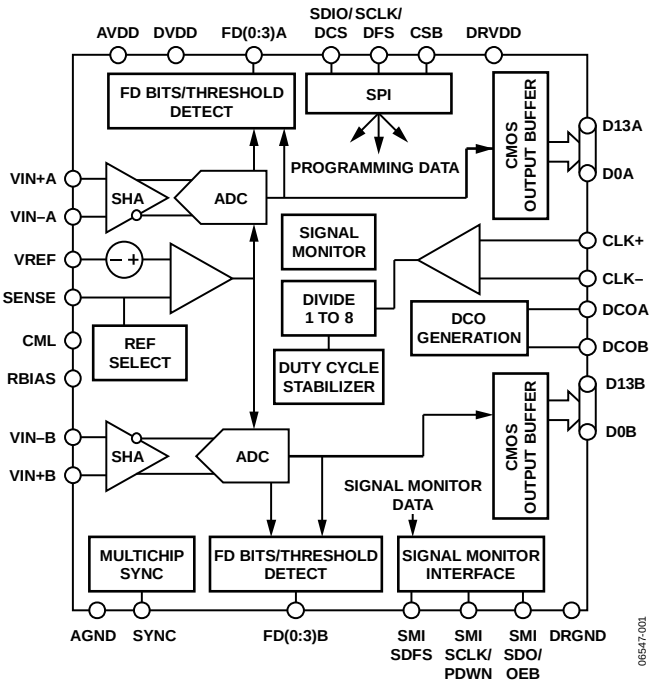

Figure 1.

PRODUCT HIGHLIGHTS

1. Integrated dual 14-bit, 80/105/125/150 MSPS ADC.
2. Fast overrange detect and signal monitor with serial output.
3. Signal monitor block with dedicated serial output mode.
4. Proprietary differential input that maintains excellent SNR performance for input frequencies up to 450 MHz.
5. Operation from a single 1.8 V supply and a separate digital output driver supply to accommodate 1.8 V to 3.3 V logic families.
6. A standard serial port interface that supports various product features and functions, such as data formatting (offset binary, twos complement, or gray coding), enabling the clock DCS, power-down, and voltage reference mode.
7. Pin compatibility with the AD9627, AD9627-11, and the AD9600 for a simple migration from 14 bits to 12 bits, 11 bits, or 10 bits.

Rev. B
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REVISION HISTORY

12/09—Rev. A to Rev. B

Added CP-64-6 Package ..... Universal
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6/09—Rev. 0 to Rev. A

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6/07—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD9640 is a dual 14-bit, 80/105/125/150 MSPS analog-to-digital converter (ADC). The AD9640 is designed to support communications applications where low cost, small size, and versatility are desired.

The dual ADC core features a multistage, differential pipelined architecture with integrated output error correction logic. Each ADC features wide bandwidth differential sample-and-hold analog input amplifiers supporting a variety of user-selectable input ranges. An integrated voltage reference eases design considerations. A duty cycle stabilizer is provided to compensate for variations in the ADC clock duty cycle, allowing the converters to maintain excellent performance.

The AD9640 has several functions that simplify the automatic gain control (AGC) function in the system receiver. The fast detect feature allows fast overrange detection by outputting four bits of input level information with very short latency.

In addition, the programmable threshold detector allows monitoring of the incoming signal power using the four fast detect bits of the ADC with very low latency. If the input signal level exceeds the programmable threshold, the fine upper threshold indicator goes high. Because this threshold is set from the four MSBs, the user can quickly turn down the system gain to avoid an overrange condition.

The second AGC-related function is the signal monitor. This block allows the user to monitor the composite magnitude of the incoming signal, which aids in setting the gain to optimize the dynamic range of the overall system.

The ADC output data can be routed directly to the two external 14-bit output ports. These outputs can be set from 1.8 V to 3.3 V CMOS or 1.8 V LVDS.

Flexible power-down options allow significant power savings, when desired.

Programming for setup and control is accomplished using a 3-bit SPI-compatible serial interface.

The AD9640 is available in a 64-lead LFCSP and is specified over the industrial temperature range of −40°C to +85°C.

SPECIFICATIONS

ADC DC SPECIFICATIONS—AD9640ABCPZ-80, AD9640BCPZ-80, AD9640ABCPZ-105, AND AD9640BCPZ-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect outputs disabled, and signal monitor disabled, unless otherwise noted.

Table 1.

		AD9640ABCPZ-80/AD9640BCPZ-80			AD9640ABCPZ-105/AD9640BCPZ-105			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.6		±0.3	±0.6	% FSR
Gain Error	Full		±0.2	±3.0		±0.2	±3.0	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.9			±0.9	LSB
	25°C		±0.4			±0.4		LSB
Integral Nonlinearity (INL)[1]	Full			±5.0			±5.0	LSB
	25°C		±2.0			±2.0		LSB
MATCHING CHARACTERISTIC								
Offset Error	Full		±0.3	±0.6		±0.4	±0.7	% FSR
Gain Error	Full		±0.1	±0.5		±0.1	±0.5	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±2	±15		±2	±15	mV
Load Regulation @ 1.0 mA	Full		7			7		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		1.3			1.3		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1, 3]	Full		233	277		310	371	mA
I_{DVDD}[1, 3]	Full		26			34		mA
I_{DRVDD}[1] (3.3 V CMOS)	Full		27			35		mA
I_{DRVDD}[1] (1.8 V CMOS)	Full		12			18		mA
I_{DRVDD}[1] (1.8 V LVDS)	Full		54			55		mA
POWER CONSUMPTION								
DC Input	Full		452	492		603	657	mW
Sine Wave Input[1] (DRVDD = 1.8 V)	Full		487			645		mW
Sine Wave Input[1] (DRVDD = 3.3 V)	Full		550			730		mW
Standby Power[4]	Full		52			68		mW
Power-Down Power	Full		2.5	6		2.5	6	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 8 for the equivalent analog input structure.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input and with the CLK pins (CLK+, CLK−) inactive (set to AVDD or AGND).

ADC DC SPECIFICATIONS—AD9640ABCPZ-125, AD9640BCPZ-125, AD9640ABCPZ-150, AND AD9640BCPZ-150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect outputs disabled, and signal monitor disabled, unless otherwise noted.

Table 2.

		AD9640ABCPZ-125/ AD9640BCPZ-125			AD9640ABCPZ-150/ AD9640BCPZ-150			
Parameter	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	Full	14			14			Bits
ACCURACY								
No Missing Codes	Full		Guaranteed			Guaranteed		
Offset Error	Full		±0.3	±0.6		±0.3	±0.6	% FSR
Gain Error	Full		±0.2	±3.0		±0.2	±3.0	% FSR
Differential Nonlinearity (DNL)[1]	Full			±0.9			−0.95/+1.5	LSB
	25°C		±0.4			−0.4/+0.6		LSB
Integral Nonlinearity (INL)[1]	Full			±5.0			±5.0	LSB
	25°C		±2			±2		LSB
MATCHING CHARACTERISTIC								
Offset Error	25°C		±0.4	±0.7		±0.4	±0.7	% FSR
Gain Error	25°C		±0.1	±0.6		±0.2	±0.6	% FSR
TEMPERATURE DRIFT								
Offset Error	Full		±15			±15		ppm/°C
Gain Error	Full		±95			±95		ppm/°C
INTERNAL VOLTAGE REFERENCE								
Output Voltage Error (1 V Mode)	Full		±2	±15		±3	±15	mV
Load Regulation @ 1.0 mA	Full		7			7		mV
INPUT REFERRED NOISE								
VREF = 1.0 V	25°C		1.3			1.3		LSB rms
ANALOG INPUT								
Input Span, VREF = 1.0 V	Full		2			2		V p-p
Input Capacitance[2]	Full		8			8		pF
VREF INPUT RESISTANCE	Full		6			6		kΩ
POWER SUPPLIES								
Supply Voltage								
AVDD, DVDD	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
DRVDD (CMOS Mode)	Full	1.7	3.3	3.6	1.7	3.3	3.6	V
DRVDD (LVDS Mode)	Full	1.7	1.8	1.9	1.7	1.8	1.9	V
Supply Current								
I_{AVDD}[1, 3]	Full		385	470		419	517	mA
I_{DVDD}[1, 3]	Full		42			50		mA
I_{DRVDD}[1] (3.3 V CMOS)	Full		44			53		mA
I_{DRVDD}[1] (1.8 V CMOS)	Full		22			27		mA
I_{DRVDD}[1] (1.8 V LVDS)			56			57		
POWER CONSUMPTION								
DC Input	Full		750	846		820	938	mW
Sine Wave Input[1] (DRVDD = 1.8 V)	Full		810			895		mW
Sine Wave Input[1] (DRVDD = 3.3 V)	Full		910			1000		mW
Standby Power[4]	Full		77			77		mW
Power-Down Power	Full		2.5	6		2.5	6	mW

[1] Measured with a low input frequency, full-scale sine wave, with approximately 5 pF loading on each output bit.
[2] Input capacitance refers to the effective capacitance between one differential input pin and AGND. See Figure 8 for the equivalent analog input structure.
[3] The maximum limit applies to the combination of I_{AVDD} and I_{DVDD} currents.
[4] Standby power is measured with a dc input and with the CLK pins (CLK+, CLK−) inactive (set to AVDD or AGND).

ADC AC SPECIFICATIONS—AD9640ABCPZ-80, AD9640BCPZ-80, AD9640ABCPZ-105, AND AD9640BCPZ-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect outputs disabled, and signal monitor disabled, unless otherwise noted.

Table 3.

		AD9640ABCPZ-80/ AD9640BCPZ-80			AD9640ABCPZ-105/ AD9640BCPZ-105			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.3 MHz	25°C		72.5			72.3		dB
f_{IN} = 70 MHz	25°C		72.1			71.9		dB
	Full	70.5			70.2			dB
f_{IN} = 140 MHz	25°C		71.6			71.3		dB
f_{IN} = 200 MHz	25°C		71.0			70.3		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 2.3 MHz	25°C		72.2			72.0		dB
f_{IN} = 70 MHz	25°C		71.6			71.6		dB
	Full	69			69.5			dB
f_{IN} = 140 MHz	25°C		71.1			70.9		dB
f_{IN} = 200 MHz	25°C		70.4			70.0		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.3 MHz	25°C		11.9			11.8		Bits
f_{IN} = 70 MHz	25°C		11.8			11.8		Bits
f_{IN} = 140 MHz	25°C		11.7			11.7		Bits
f_{IN} = 200 MHz	25°C		11.6			11.5		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.3 MHz	25°C		−87			−87		dBc
f_{IN} = 70 MHz	25°C		−85			−85		dBc
	Full			−75			−74	dBc
f_{IN} = 140 MHz	25°C		−84			−84		dBc
f_{IN} = 200 MHz	25°C		−83			−83		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.3 MHz	25°C		87			87		dBc
f_{IN} = 70 MHz	25°C		85			85		dBc
	Full	75			74			dBc
f_{IN} = 140 MHz	25°C		84			84		dBc
f_{IN} = 200 MHz	25°C		83			83		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 2.3 MHz	25°C		−93			−93		dBc
f_{IN} = 70 MHz	25°C		−89			−89		dBc
	Full			−82			−81	dBc
f_{IN} = 140 MHz	25°C		−89			−89		dBc
f_{IN} = 200 MHz	25°C		−89			−89		dBc
TWO TONE SFDR								
f_{IN} = 29.1 MHz, 32.1 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.1 MHz, 172.1 MHz (−7 dBFS)	25°C		82			82		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See Application Note AN-835, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and no input on the alternate channel.

ADC AC SPECIFICATIONS—AD9640ABCPZ-125, AD9640BCPZ-125, AD9640ABCPZ-150, AND AD9640BCPZ 150

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, fast detect outputs disabled, and signal monitor disabled, unless otherwise noted.

Table 4.

		AD9640ABCPZ-125 AD9640BCPZ-125			AD9640ABCPZ-150/ AD9640BCPZ-150			
Parameter[1]	**Temperature**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
SIGNAL-TO-NOISE RATIO (SNR)								
f_{IN} = 2.3 MHz	25°C		72.1			71.9		dB
f_{IN} = 70 MHz	25°C		71.8			71.6		dB
	Full	70.2			69.5			dB
f_{IN} = 140 MHz	25°C		71.4			70.9		dB
f_{IN} = 200 MHz	25°C		70.8			70.0		dB
SIGNAL-TO-NOISE AND DISTORTION (SINAD)								
f_{IN} = 2.3 MHz	25°C		71.8			71.6		dB
f_{IN} = 70 MHz	25°C		71.4			71.0		dB
	Full	69.5			67.5			dB
f_{IN} = 140 MHz	25°C		71.0			70.5		dB
f_{IN} = 200 MHz	25°C		70.3			69.9		dB
EFFECTIVE NUMBER OF BITS (ENOB)								
f_{IN} = 2.3 MHz	25°C		11.8			11.8		Bits
f_{IN} = 70 MHz	25°C		11.7			11.8		Bits
f_{IN} = 140 MHz	25°C		11.7			11.6		Bits
f_{IN} = 200 MHz	25°C		11.6			11.5		Bits
WORST SECOND OR THIRD HARMONIC								
f_{IN} = 2.3 MHz	25°C		−86.5			−86.5		dBc
f_{IN} = 70 MHz	25°C		−85			−84		dBc
	Full			−74			−73	dBc
f_{IN} = 140 MHz	25°C		−84			−83.5		dBc
f_{IN} = 200 MHz	25°C		−83			−77		dBc
SPURIOUS-FREE DYNAMIC RANGE (SFDR)								
f_{IN} = 2.3 MHz	25°C		86.5			86.5		dBc
f_{IN} = 70 MHz	25°C		85			84		dBc
	Full	74			73			dBc
f_{IN} = 140 MHz	25°C		84			83.5		dBc
f_{IN} = 200 MHz	25°C		83			77		dBc
WORST OTHER HARMONIC OR SPUR								
f_{IN} = 2.3 MHz	25°C		−92			−92		dBc
f_{IN} = 70 MHz	25°C		−89			−90		dBc
	Full			−80			−80	dBc
f_{IN} = 140 MHz	25°C		−89			−90		dBc
f_{IN} = 200 MHz	25°C		−89			−90		dBc
TWO TONE SFDR								
f_{IN} = 29.1 MHz, 32.1 MHz (−7 dBFS)	25°C		85			85		dBc
f_{IN} = 169.1 MHz, 172.1 MHz (−7 dBFS)	25°C		82			82		dBc
CROSSTALK[2]	Full		−95			−95		dB
ANALOG INPUT BANDWIDTH	25°C		650			650		MHz

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for a complete set of definitions.
[2] Crosstalk is measured at 100 MHz with −1 dBFS on one channel and no input on the alternate channel.

DIGITAL SPECIFICATIONS

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, and DCS enabled, unless otherwise noted.

Table 5.

Parameter	Temperature	Min	Typ	Max	Unit
DIFFERENTIAL CLOCK INPUTS (CLK+, CLK–)					
Logic Compliance			CMOS/LVDS/LVPECL		
Internal Common-Mode Bias	Full		1.2		V
Differential Input Voltage	Full	0.2		6	V p-p
Input Voltage Range	Full	AGND – 0.3		AVDD + 1.6	V
Input Common-Mode Range	Full	1.1		AVDD	V
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
SYNC INPUT					
Logic Compliance			CMOS		
Internal Bias	Full		1.2		V
Input Voltage Range	Full	AGND – 0.3		AVDD + 1.6	V
High Level Input Voltage	Full	1.2		3.6	V
Low Level Input Voltage	Full	0		0.8	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	−10		+10	µA
Input Capacitance	Full		4		pF
Input Resistance	Full	8	10	12	kΩ
LOGIC INPUT (CSB)[1]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	40		132	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUT (SCLK/DFS)[2]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 3.3 V)	Full	−92		−135	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		2		pF
LOGIC INPUTS/OUTPUTS (SDIO/DCS, SMI SDFS)[1]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current	Full	−10		+10	µA
Low Level Input Current	Full	38		128	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF
LOGIC INPUTS/OUTPUTS (SMI SDO/OEB, SMI SCLK/PDWN)[2]					
High Level Input Voltage	Full	1.22		3.6	V
Low Level Input Voltage	Full	0		0.6	V
High Level Input Current (VIN = 3.3 V)	Full	−90		−134	µA
Low Level Input Current	Full	−10		+10	µA
Input Resistance	Full		26		kΩ
Input Capacitance	Full		5		pF

Parameter	Temperature	Min	Typ	Max	Unit
DIGITAL OUTPUTS					
CMOS Mode—DRVDD = 3.3 V					
High Level Output Voltage (I_{OH} = 50 µA)	Full	3.29			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	3.25			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (I_{OL} = 50 µA)	Full			0.05	V
CMOS Mode—DRVDD = 1.8 V					
High Level Output Voltage (I_{OH} = 50 µA)	Full	1.79			V
High Level Output Voltage (I_{OH} = 0.5 mA)	Full	1.75			V
Low Level Output Voltage (I_{OL} = 1.6 mA)	Full			0.2	V
Low Level Output Voltage (I_{OL} = 50 µA)	Full			0.05	V
LVDS Mode—DRVDD = 1.8 V					
Differential Output Voltage (V_{OD}), ANSI Mode	Full	250	350	450	mV
Output Offset Voltage (V_{OS}), ANSI Mode	Full	1.15	1.25	1.35	V
Differential Output Voltage (V_{OD}), Reduced Swing Mode	Full	150	200	280	mV
Output Offset Voltage (V_{OS}), Reduced Swing Mode	Full	1.15	1.25	1.35	V

[1] Pull up.
[2] Pull down.

SWITCHING SPECIFICATIONS—AD9640ABCPZ-80, AD9640BCPZ-80, AD9640ABCPZ-105, AND AD9640BCPZ-105

AVDD = 1.8 V, DVDD = 1.8 V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 6.

		AD9640ABCPZ-80 AD9640BCPZ-80			AD9640ABCPZ-105/ AD9640BCPZ-105			
Parameter	**Temp**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate								
DCS Enabled[1]	Full	20		80	20		105	MSPS
DCS Disabled[1]	Full	10		80	10		105	MSPS
CLK Period—Divide by 1 Mode (t_{CLK})	Full	12.5			9.5			ns
CLK Pulse Width High								
Divide by 1 Mode, DCS Enabled	Full	3.75	6.25	8.75	2.85	4.75	6.65	ns
Divide by 1 Mode, DCS Disabled	Full	5.63	6.25	6.88	4.28	4.75	5.23	ns
Divide by 2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide by 3 Through 8, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	2.2	4.5	6.4	2.2	4.5	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.0	6.8	3.8	5.0	6.8	ns
Setup Time (t_S)	Full		6.25			5.25		ns
Hold Time (t_H)	Full		5.75			4.25		ns
CMOS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.4	5.2	6.9	2.4	5.2	6.9	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.6	7.3	4.0	5.6	7.3	ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	3.0	3.7	4.4	3.0	3.7	4.4	ns
DCO Propagation Delay (t_{DCO})	Full	5.4	7.0	8.4	5.2	6.4	7.6	ns

Parameter	Temp	AD9640ABCPZ-80 AD9640BCPZ-80 Min	Typ	Max	AD9640ABCPZ-105/ AD9640BCPZ-105 Min	Typ	Max	Unit
CMOS Mode Pipeline Delay (Latency)	Full		12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B			12/12.5			12/12.5		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		µs
OUT-OF-RANGE RECOVERY TIME	Full		2			2		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

SWITCHING SPECIFICATIONS—AD9640ABCPZ-125, AD9640BCPZ-125, AD9640ABCPZ-150, AND AD9640BCPZ-150

AVDD = 1.8 V, DVDD = 1.8V, DRVDD = 3.3 V, maximum sample rate, VIN = −1.0 dBFS differential input, 1.0 V internal reference, DCS enabled, unless otherwise noted.

Table 7.

Parameter	Temperature	AD9640ABCPZ-125/ AD9640BCPZ-125 Min	Typ	Max	AD9640ABCPZ-150/ AD9640BCPZ-150 Min	Typ	Max	Unit
CLOCK INPUT PARAMETERS								
Input Clock Rate	Full			625			625	MHz
Conversion Rate								
DCS Enabled[1]	Full	20		125	20		150	MSPS
DCS Disabled[1]	Full	10		125	10		150	MSPS
CLK Period—Divide by 1 Mode (t_{CLK})	Full	8			6.66			ns
CLK Pulse Width High								
Divide by 1 Mode, DCS Enabled	Full	2.4	4	5.6	2.0	3.33	4.66	ns
Divide by 1 Mode, DCS Disabled	Full	3.6	4	4.4	3.0	3.33	3.66	ns
Divide by 2 Mode, DCS Enabled	Full	1.6			1.6			ns
Divide by 3 Through 8, DCS Enabled	Full	0.8			0.8			ns
DATA OUTPUT PARAMETERS (DATA, FD)								
CMOS Mode—DRVDD = 3.3 V								
Data Propagation Delay (t_{PD})[2]	Full	2.2	4.5	6.4	2.2	4.5	6.4	ns
DCO Propagation Delay (t_{DCO})	Full	3.8	5.0	6.8	3.8	5.0	6.8	ns
Setup Time (t_S)	Full		4.5			3.83		ns
Hold Time (t_H)	Full		3.5			2.83		ns
CMOS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	2.4	5.2	6.9	2.4	5.2	6.9	ns
DCO Propagation Delay (t_{DCO})	Full	4.0	5.6	7.3	4.0	5.6	7.3	ns
LVDS Mode—DRVDD = 1.8 V								
Data Propagation Delay (t_{PD})[2]	Full	3.0	3.8	4.5	3.0	3.8	4.5	ns
DCO Propagation Delay (t_{DCO})	Full	5.0	6.2	7.4	4.8	5.9	7.3	ns
CMOS Mode Pipeline Delay (Latency)	Full		12			12		Cycles
LVDS Mode Pipeline Delay (Latency) Channel A/Channel B			12/12.5			12/12.5		Cycles
Aperture Delay (t_A)	Full		1.0			1.0		ns
Aperture Uncertainty (Jitter, t_J)	Full		0.1			0.1		ps rms
Wake-Up Time[3]	Full		350			350		µs
OUT-OF-RANGE RECOVERY TIME	Full		3			3		Cycles

[1] Conversion rate is the clock rate after the divider.
[2] Output propagation delay is measured from CLK 50% transition to DATA 50% transition, with 5 pF load.
[3] Wake-up time is dependent on the value of the decoupling capacitors.

TIMING SPECIFICATIONS

Table 8.

Parameter	Conditions	Min	Typ	Max	Unit
SYNC TIMING REQUIREMENTS					
t_{SSYNC}	SYNC to rising edge of CLK setup time		0.24		ns
t_{HSYNC}	SYNC to rising edge of CLK hold time		0.40		ns
SPI TIMING REQUIREMENTS					
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between CSB and SCLK	2			ns
t_H	Hold time between CSB and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}	Time required for the SDIO pin to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}	Time required for the SDIO pin to switch from an output to an input relative to the SCLK rising edge	10			ns
SPORT TIMING REQUIREMENTS					
t_{CSSCLK}	Delay from rising edge of CLK+ to rising edge of SMI SCLK	3.2	4.5	6.2	ns
$t_{SSCLKSDO}$	Delay from rising edge of SMI SCLK to SMI SDO	−0.4	0	+0.4	ns
$t_{SSCLKSDFS}$	Delay from rising edge of SMI SCLK to SMI SDFS	−0.4	0	+0.4	ns

Timing Diagrams

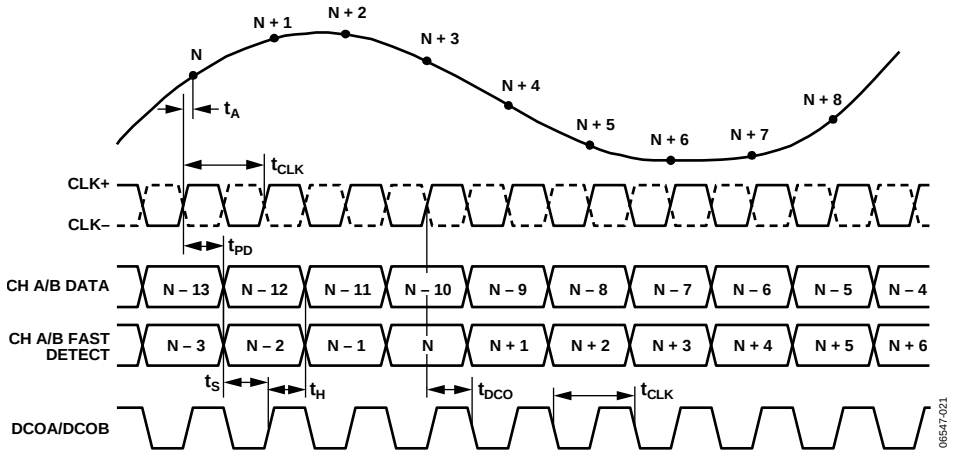


Figure 2. CMOS Output Mode Data and Fast Detect Output Timing (Fast Detect Mode 0)

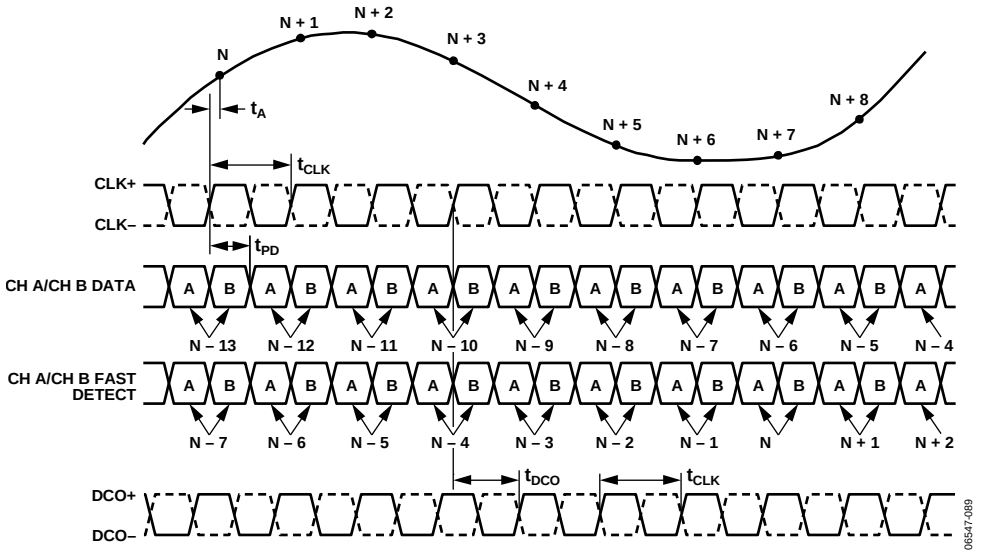


Figure 3. LVDS Mode Data and Fast Detect Output Timing (Fast Detect Mode 1 Through Fast Detect Mode 5)

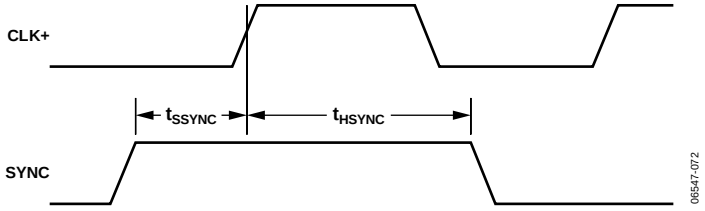


Figure 4. SYNC Input Timing Requirements

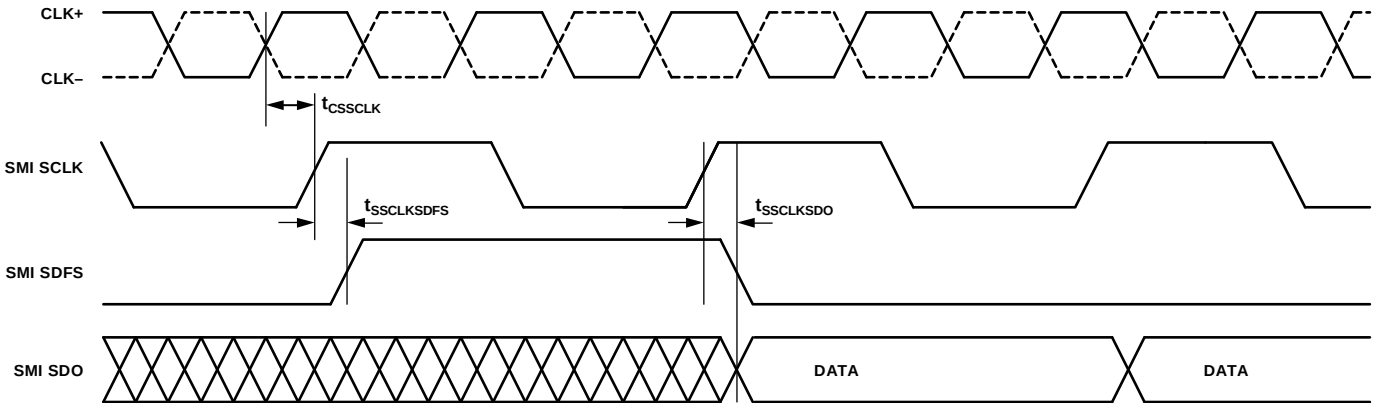


Figure 5. Signal Monitor SPORT Output Timing (Divide by 2 Mode)

ABSOLUTE MAXIMUM RATINGS

Table 9.

Parameter	Rating
ELECTRICAL	
AVDD, DVDD to AGND	−0.3 V to +2.0 V
DRVDD to DRGND	−0.3 V to +3.9 V
AGND to DRGND	−0.3 V to +0.3 V
AVDD to DRVDD	−3.9 V to +2.0 V
VIN+A/VIN+B, VIN−A/VIN−B to AGND	−0.3 V to AVDD + 0.2 V
CLK+, CLK− to AGND	−0.3 V to +3.9 V
SYNC to AGND	−0.3 V to +3.9 V
VREF to AGND	−0.3 V to AVDD + 0.2 V
SENSE to AGND	−0.3 V to AVDD + 0.2 V
CML to AGND	−0.3 V to AVDD + 0.2 V
RBIAS to AGND	−0.3 V to AVDD + 0.2 V
CSB to AGND	−0.3 V to +3.9 V
SCLK/DFS to DRGND	−0.3 V to +3.9 V
SDIO/DCS to DRGND	−0.3 V to DRVDD + 0.3 V
SMI SDO/OEB	−0.3 V to DRVDD + 0.3 V
SMI SCLK/PDWN	−0.3 V to DRVDD + 0.3 V
SMI SDFS	−0.3 V to DRVDD + 0.3 V
D0A/D0B through D13A/D13B to DRGND	−0.3 V to DRVDD + 0.3 V
FD0A/FD0B through FD3A/FD3B to DRGND	−0.3 V to DRVDD + 0.3 V
DCOA/DCOB to DRGND	−0.3 V to DRVDD + 0.3 V
ENVIRONMENTAL	
Operating Temperature Range (Ambient)	−40°C to +85°C
Maximum Junction Temperature Under Bias	150°C
Storage Temperature Range (Ambient)	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

The exposed paddle must be soldered to the ground plane for the LFCSP package. Soldering the exposed paddle to the customer board increases the reliability of the solder joints and maximizes the thermal capability of the package.

Table 10. Thermal Resistance

Package Type	Airflow Velocity (m/s)	θ_{JA}[1,2]	θ_{JC}[1,3]	θ_{JB}[1,4]	Unit
64-lead LFCSP 9 mm × 9 mm	0	18.8	0.6	6.0	°C/W
	1.0	16.5			°C/W
	2.0	15.8			°C/W

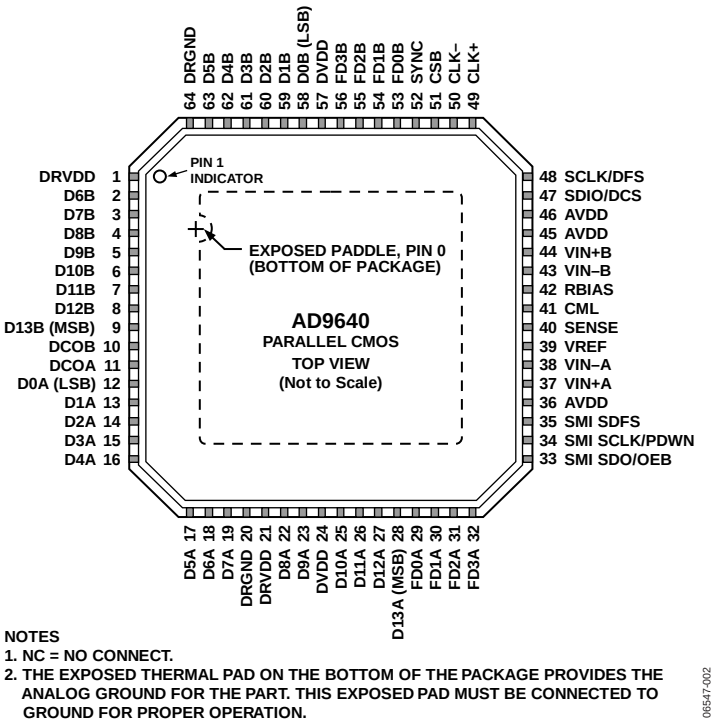
[1] JEDEC 51-7, plus JEDEC 25-5 2S2P test board.
[2] Per JEDEC JESD51-2 (still air) or JEDEC JESD51-6 (moving air).
[3] Per MIL-Std 883, Method 1012.1.
[4] Per JEDEC JESD51-8 (still air).

Typical θ_{JA} is specified for a 4-layer PCB with a solid ground plane. As shown, airflow improves heat dissipation, which reduces θ_{JA}. In addition, metal in direct contact with the package leads from metal traces, through holes, ground, and power planes, reduces the θ_{JA}.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THE EXPOSED THERMAL PAD ON THE BOTTOM OF THE PACKAGE PROVIDES THE ANALOG GROUND FOR THE PART. THIS EXPOSED PAD MUST BE CONNECTED TO GROUND FOR PROPER OPERATION.

Figure 6. Pin Configuration, LFCSP Parallel CMOS (Top View)

Table 11. Pin Function Descriptions (Parallel CMOS Mode)

Pin No.	Mnemonic	Type	Description
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. See Table 14 for details.
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.

Pin No.	Mnemonic	Type	Description
ADC Fast Detect Outputs			
29	FD0A	Output	Channel A Fast Detect Indicator. See Table 18 for details.
30	FD1A	Output	Channel A Fast Detect Indicator. See Table 18 for details.
31	FD2A	Output	Channel A Fast Detect Indicator. See Table 18 for details.
32	FD3A	Output	Channel A Fast Detect Indicator. See Table 18 for details.
53	FD0B	Output	Channel B Fast Detect Indicator. See Table 18 for details.
54	FD1B	Output	Channel B Fast Detect Indicator. See Table 18 for details.
55	FD2B	Output	Channel B Fast Detect Indicator. See Table 18 for details.
56	FD3B	Output	Channel B Fast Detect Indicator. See Table 18 for details.
Digital Inputs			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
12	D0A (LSB)	Output	Channel A CMOS Output Data.
13	D1A	Output	Channel A CMOS Output Data.
14	D2A	Output	Channel A CMOS Output Data.
15	D3A	Output	Channel A CMOS Output Data.
16	D4A	Output	Channel A CMOS Output Data.
17	D5A	Output	Channel A CMOS Output Data.
18	D6A	Output	Channel A CMOS Output Data.
19	D7A	Output	Channel A CMOS Output Data.
22	D8A	Output	Channel A CMOS Output Data.
23	D9A	Output	Channel A CMOS Output Data.
25	D10A	Output	Channel A CMOS Output Data.
26	D11A	Output	Channel A CMOS Output Data.
27	D12A	Output	Channel A CMOS Output Data.
28	D13A (MSB)	Output	Channel A CMOS Output Data.
58	D0B (LSB)	Output	Channel B CMOS Output Data.
59	D1B	Output	Channel B CMOS Output Data.
60	D2B	Output	Channel B CMOS Output Data.
61	D3B	Output	Channel B CMOS Output Data.
62	D4B	Output	Channel B CMOS Output Data.
63	D5B	Output	Channel B CMOS Output Data.
2	D6B	Output	Channel B CMOS Output Data.
3	D7B	Output	Channel B CMOS Output Data.
4	D8B	Output	Channel B CMOS Output Data.
5	D9B	Output	Channel B CMOS Output Data.
6	D10B	Output	Channel B CMOS Output Data.
7	D11B	Output	Channel B CMOS Output Data.
8	D12B	Output	Channel B CMOS Output Data.
9	D13B (MSB)	Output	Channel B CMOS Output Data.
11	DCOA	Output	Channel A Data Clock Output.
10	DCOB	Output	Channel B Data Clock Output.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer in External Pin Mode.
51	CSB	Input	SPI Chip Select (Active Low).
Serial Port			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode.

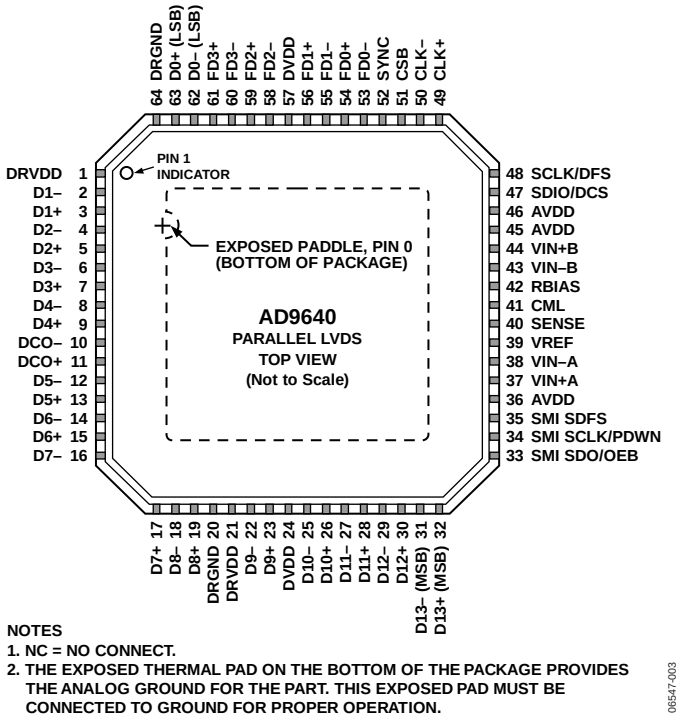


Figure 7. Pin Configuration, LFCSP LVDS (Top View)

Table 12. Pin Function Descriptions (Interleaved Parallel LVDS Mode)

Pin No.	Mnemonic	Type	Function
ADC Power Supplies			
20, 64	DRGND	Ground	Digital Output Ground.
1, 21	DRVDD	Supply	Digital Output Driver Supply (1.8 V to 3.3 V).
24, 57	DVDD	Supply	Digital Power Supply (1.8 V Nominal).
36, 45, 46	AVDD	Supply	Analog Power Supply (1.8 V Nominal).
0	AGND, Exposed Pad	Ground	The exposed thermal pad on the bottom of the package provides the analog ground for the part. This exposed pad must be connected to ground for proper operation.
ADC Analog			
37	VIN+A	Input	Differential Analog Input Pin (+) for Channel A.
38	VIN−A	Input	Differential Analog Input Pin (−) for Channel A.
44	VIN+B	Input	Differential Analog Input Pin (+) for Channel B.
43	VIN−B	Input	Differential Analog Input Pin (−) for Channel B.
39	VREF	Input/Output	Voltage Reference Input/Output.
40	SENSE	Input	Voltage Reference Mode Select. See Table 14 for details.
42	RBIAS	Input/Output	External Reference Bias Resistor.
41	CML	Output	Common-Mode Level Bias Output for Analog Inputs.
49	CLK+	Input	ADC Clock Input—True.
50	CLK−	Input	ADC Clock Input—Complement.
ADC Fast Detect Outputs			
54	FD0+	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—True. See Table 18 for details.
53	FD0−	Output	Channel A/Channel B LVDS Fast Detect Indicator 0—Complement. See Table 18 for details.
56	FD1+	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—True. See Table 18 for details.
55	FD1−	Output	Channel A/Channel B LVDS Fast Detect Indicator 1—Complement. See Table 18 for details.
59	FD2+	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—True. See Table 18 for details.
58	FD2−	Output	Channel A/Channel B LVDS Fast Detect Indicator 2—Complement. See Table 18 for details.
61	FD3+	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—True. See Table 18 for details.
60	FD3−	Output	Channel A/Channel B LVDS Fast Detect Indicator 3—Complement. See Table 18 for details.

Pin No.	Mnemonic	Type	Function
Digital Inputs			
52	SYNC	Input	Digital Synchronization Pin. Slave mode only.
Digital Outputs			
63	D0+ (LSB)	Output	Channel A/Channel B LVDS Output Data 0—True.
62	D0– (LSB)	Output	Channel A/Channel B LVDS Output Data 0—Complement.
3	D1+	Output	Channel A/Channel B LVDS Output Data 1—True.
2	D1–	Output	Channel A/Channel B LVDS Output Data 1—Complement.
5	D2+	Output	Channel A/Channel B LVDS Output Data 2—True.
4	D2–	Output	Channel A/Channel B LVDS Output Data 2—Complement.
7	D3+	Output	Channel A/Channel B LVDS Output Data 3—True.
6	D3–	Output	Channel A/Channel B LVDS Output Data 3—Complement.
9	D4+	Output	Channel A/Channel B LVDS Output Data 4—True.
8	D4–	Output	Channel A/Channel B LVDS Output Data 4—Complement.
13	D5+	Output	Channel A/Channel B LVDS Output Data 5—True.
12	D5–	Output	Channel A/Channel B LVDS Output Data 5—Complement.
15	D6+	Output	Channel A/Channel B LVDS Output Data 6 —True.
14	D6–	Output	Channel A/Channel B LVDS Output Data 6—Complement.
17	D7+	Output	Channel A/Channel B LVDS Output Data 7—True.
16	D7–	Output	Channel A/Channel B LVDS Output Data 7—Complement.
19	D8+	Output	Channel A/Channel B LVDS Output Data 8—True.
18	D8–	Output	Channel A/Channel B LVDS Output Data 8—Complement.
23	D9+	Output	Channel A/Channel B LVDS Output Data 9—True.
22	D9–	Output	Channel A/Channel B LVDS Output Data 9—Complement.
26	D10+	Output	Channel A/Channel B LVDS Output Data 10—True.
25	D10–	Output	Channel A/Channel B LVDS Output Data 10—Complement.
28	D11+	Output	Channel A/Channel B LVDS Output Data 11—True.
27	D11–	Output	Channel A/Channel B LVDS Output Data 11—Complement.
30	D12+	Output	Channel A/Channel B LVDS Output Data 12—True.
29	D12–	Output	Channel A/Channel B LVDS Output Data 12—Complement.
32	D13+ (MSB)	Output	Channel A/Channel B LVDS Output Data 13—True.
31	D13– (MSB)	Output	Channel A/Channel B LVDS Output Data 13—Complement.
11	DCO+	Output	Channel A/Channel B LVDS Data Clock Output—True.
10	DCO–	Output	Channel A/Channel B LVDS Data Clock Output—Complement.
SPI Control			
48	SCLK/DFS	Input	SPI Serial Clock/Data Format Select Pin in External Pin Mode.
47	SDIO/DCS	Input/Output	SPI Serial Data I/O/Duty Cycle Stabilizer in External Pin Mode.
51	CSB	Input	SPI Chip Select (Active Low).
Signal Monitor Ports			
33	SMI SDO/OEB	Input/Output	Signal Monitor Serial Data Output/Output Enable Input (Active Low) in External Pin Mode.
35	SMI SDFS	Output	Signal Monitor Serial Data Frame Sync.
34	SMI SCLK/PDWN	Input/Output	Signal Monitor Serial Clock Output/Power-Down Input in External Pin Mode.

EQUIVALENT CIRCUITS

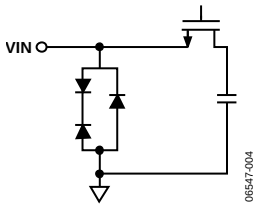


Figure 8. Equivalent Analog Input Circuit

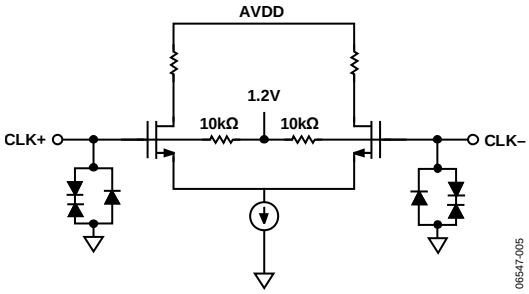


Figure 9. Equivalent Clock Input Circuit

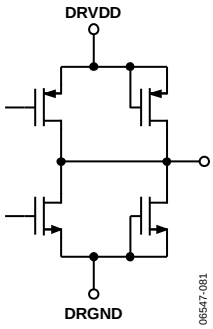


Figure 10. Digital Output

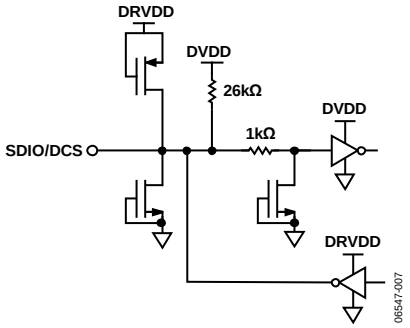


Figure 11. Equivalent SDIO/DCS or SMI SDFS Circuit

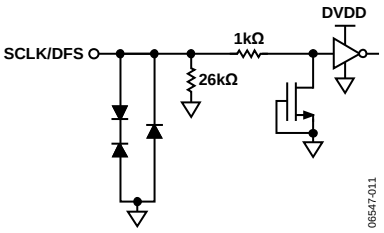


Figure 12. Equivalent SCLK/DFS Input Circuit

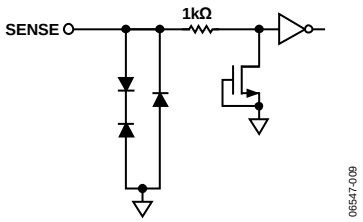


Figure 13. Equivalent SENSE Circuit

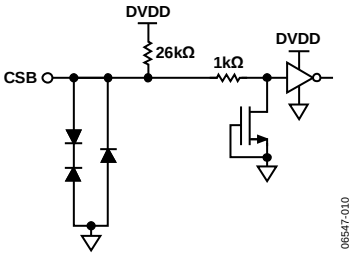


Figure 14. Equivalent CSB Input Circuit

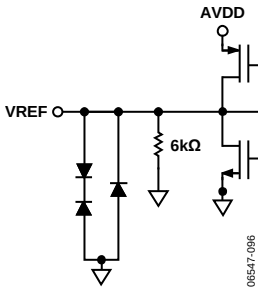


Figure 15. Equivalent VREF Circuit

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = 1.8 V; DVDD = 1.8 V; DRVDD = 3.3 V; sample rate = 150 MSPS, DCS enabled, 1 V internal reference; 2 V p-p differential input; VIN = −1.0 dBFS; and 64k sample; T_A = 25°C, unless otherwise noted.

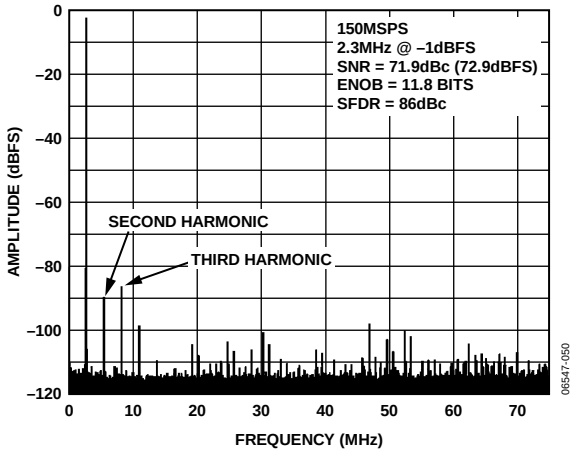


Figure 16. AD9640-150 Single-Tone FFT with f_{IN} = 2.3 MHz

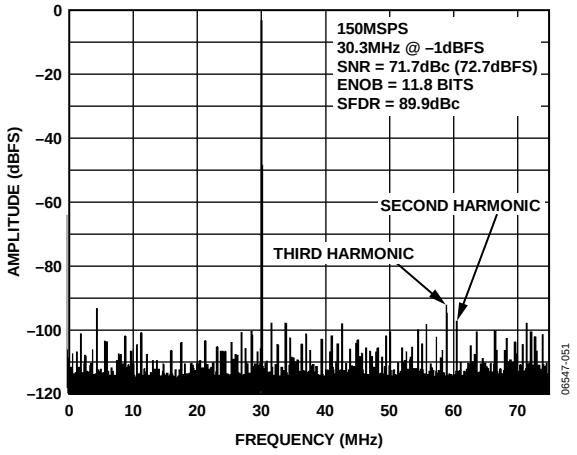


Figure 17. AD9640-150 Single-Tone FFT with f_{IN} = 30.3 MHz

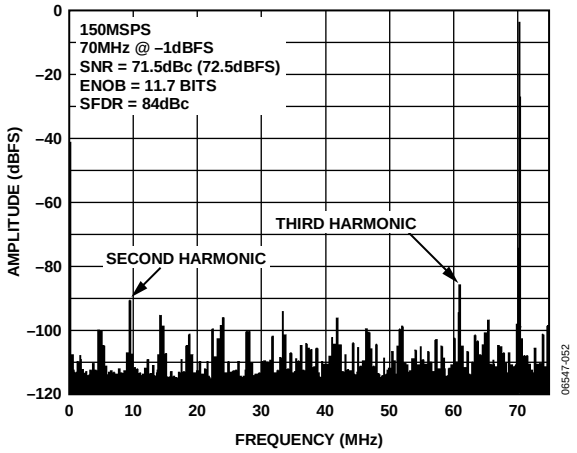


Figure 18. AD9640-150 Single-Tone FFT with f_{IN} = 70 MHz

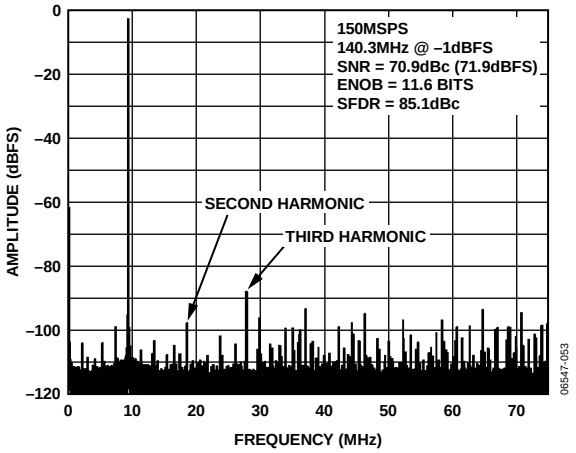


Figure 19. AD9640-150 Single-Tone FFT with f_{IN} = 140.3 MHz

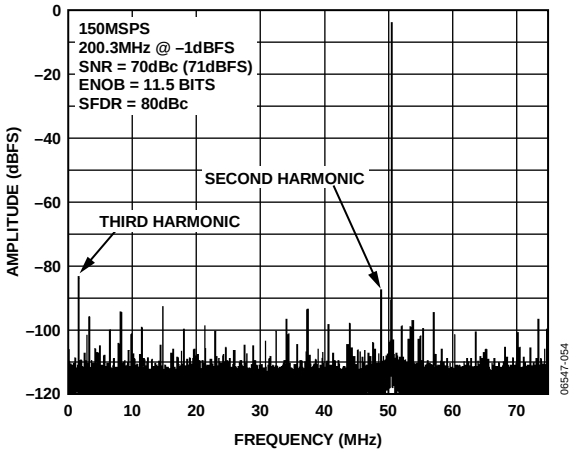


Figure 20. AD9640-150 Single-Tone FFT with f_{IN} = 200.3 MHz

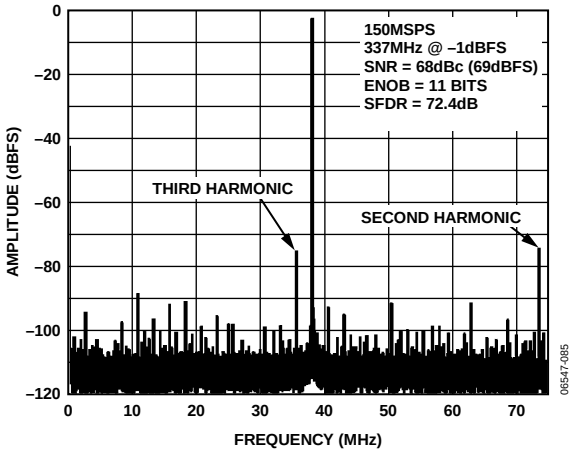


Figure 21. AD9640-150 Single-Tone FFT with f_{IN} = 337 MHz

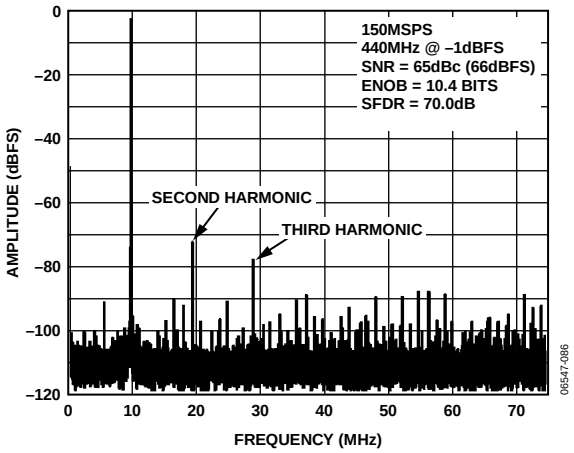


Figure 22. AD9640-150 Single-Tone FFT with f_{IN} = 440 MHz

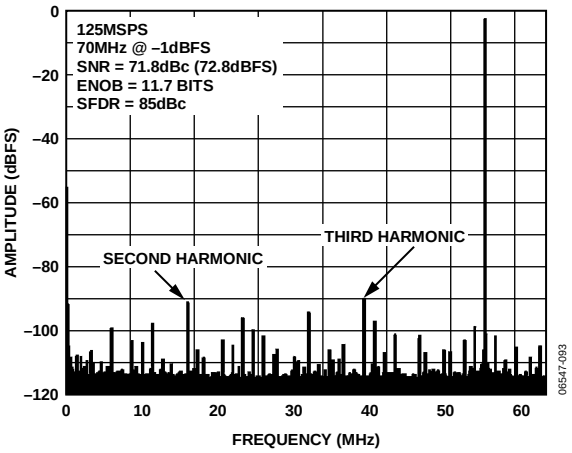


Figure 25. AD9640-125 Single-Tone FFT with f_{IN} = 70 MHz

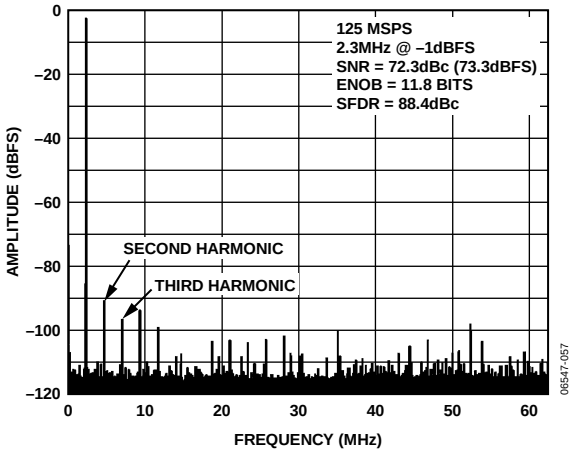


Figure 23. AD9640-125 Single-Tone FFT with f_{IN} = 2.3 MHz

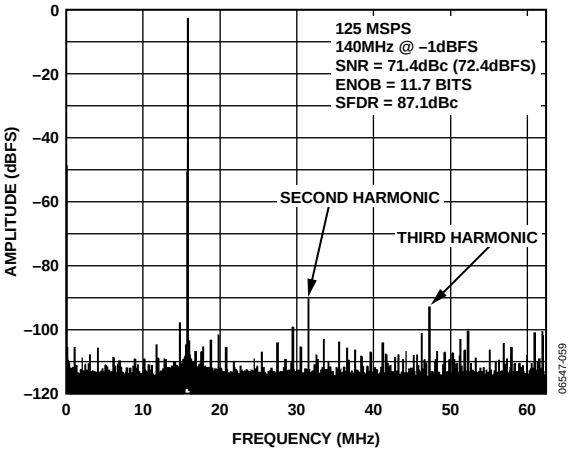


Figure 26. AD9640-125 Single-Tone FFT with f_{IN} = 140 MHz

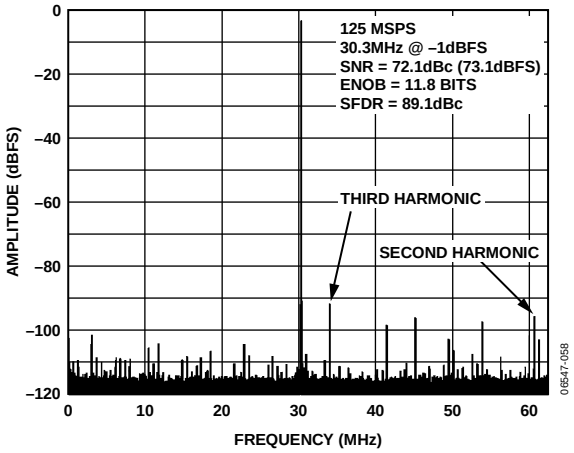


Figure 24. AD9640-125 Single-Tone FFT with f_{IN} = 30.3 MHz

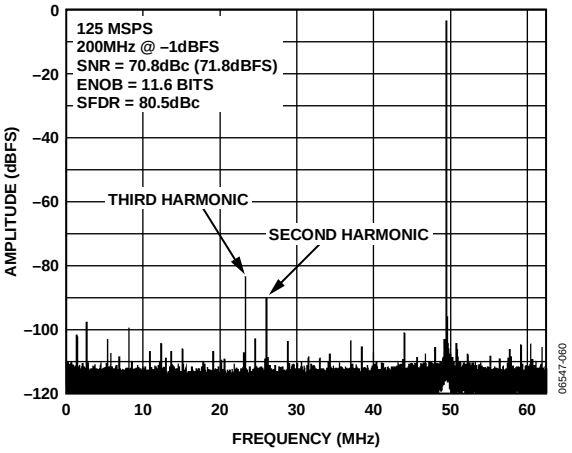


Figure 27. AD9640-125 Single-Tone FFT with f_{IN} = 200 MHz

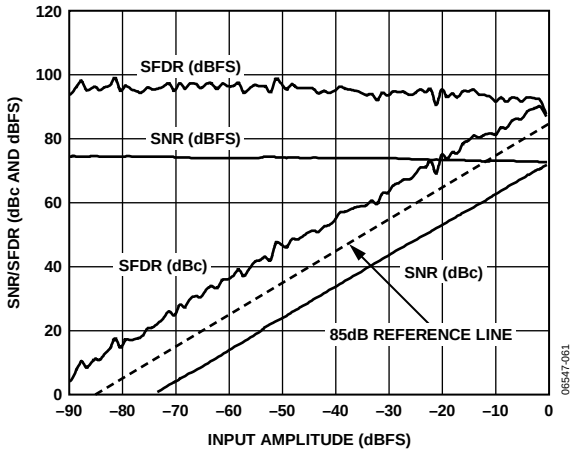


Figure 28. AD9640-150 Single-Tone SNR/SFDR vs. Input Amplitude (A_{IN}) with f_{IN} = 2.3 MHz

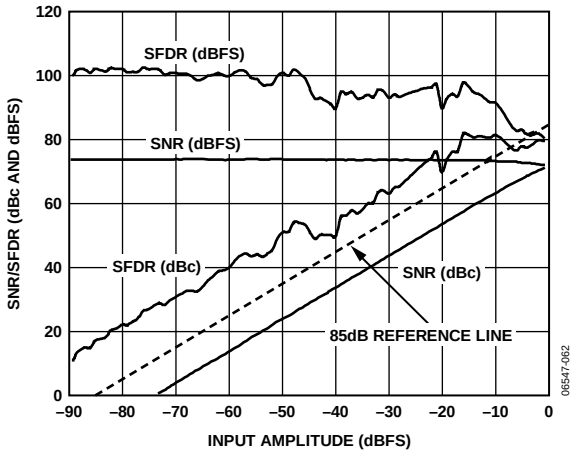


Figure 29. AD9640-150 Single-Tone SFDR vs. Input Amplitude with f_{IN} = 98.12 MHz

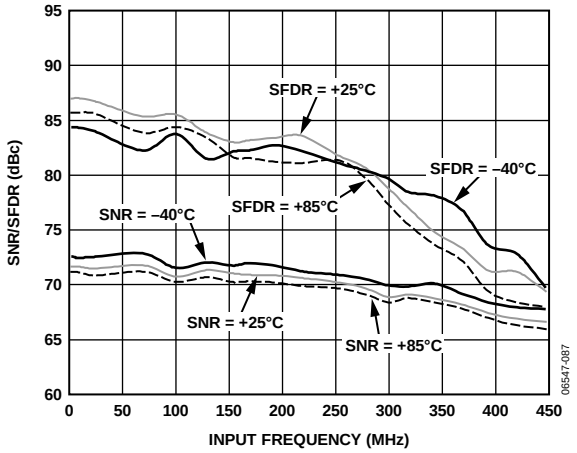


Figure 30. AD9640-150 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 2 V p-p Full Scale

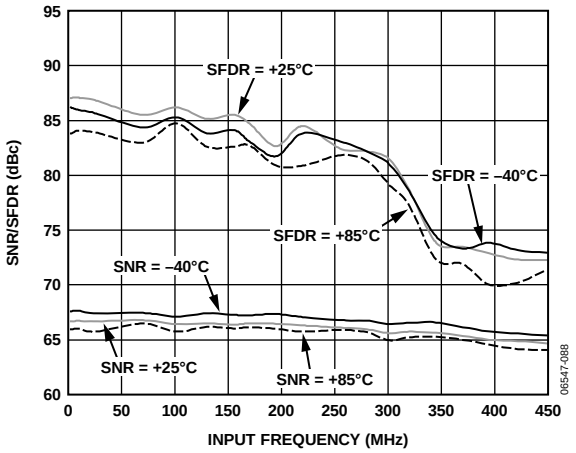


Figure 31. AD9640-150 Single-Tone SNR/SFDR vs. Input Frequency (f_{IN}) and Temperature with 1 V p-p Full Scale

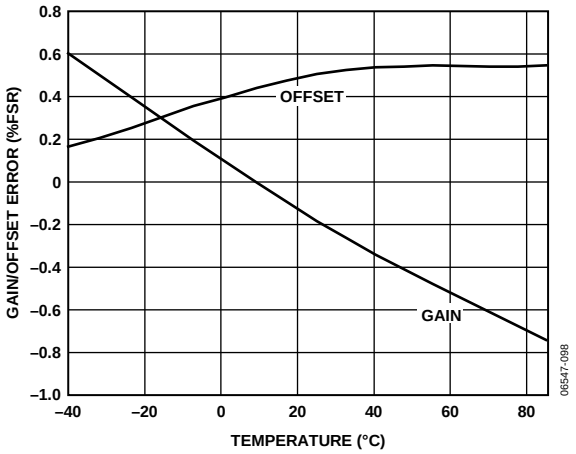


Figure 32. AD9640 Gain and Offset vs. Temperature

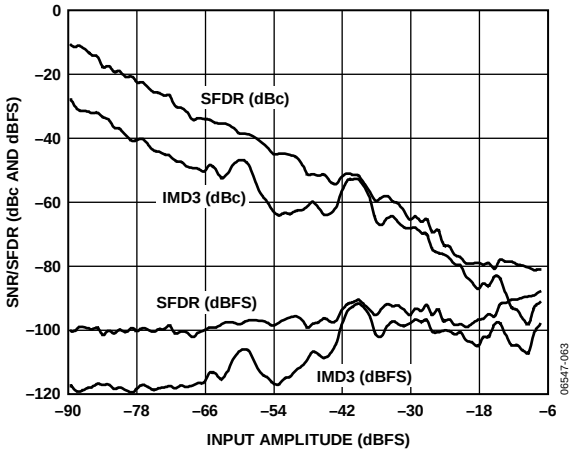


Figure 33. AD9640-150 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 29.1 MHz, f_{IN2} = 32.1 MHz, f_S = 150 MSPS

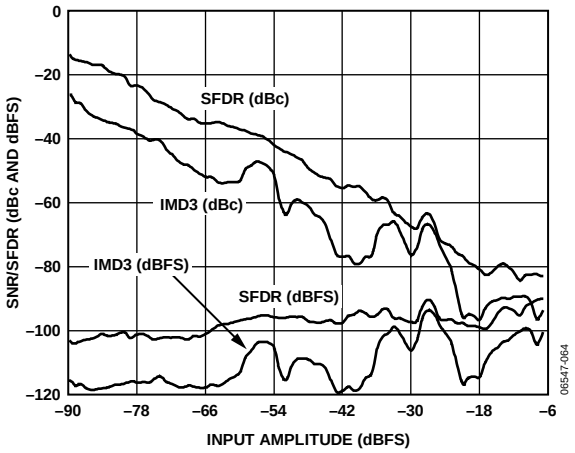


Figure 34. AD9640-150 Two-Tone SFDR/IMD3 vs. Input Amplitude (A_{IN}) with f_{IN1} = 169.1 MHz, f_{IN2} = 172.1 MHz, f_S = 150 MSPS

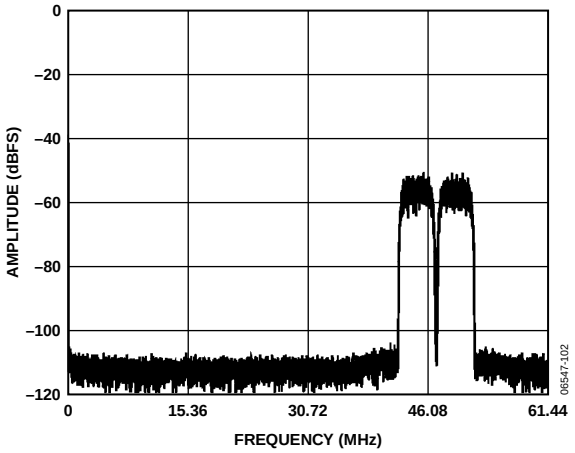


Figure 35. AD9640-125, Two 64 k WCDMA Carriers with f_{IN} = 170 MHz, f_S = 122.88 MSPS

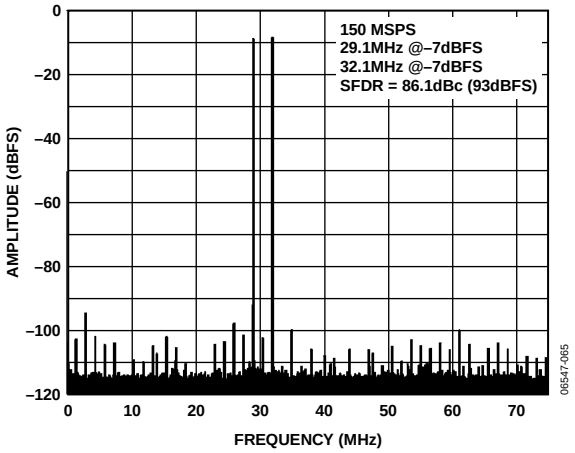


Figure 36. AD9640-150 Two-Tone FFT with f_{IN1} = 29.1 MHz and f_{IN2} = 32.1 MHz

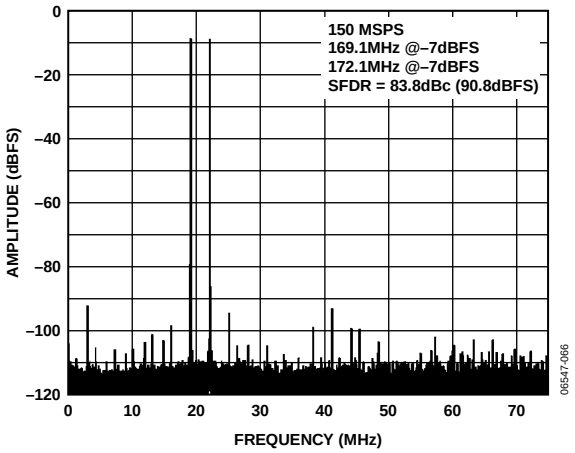


Figure 37. AD9640-150 Two-Tone FFT with f_{IN1} = 169.1 MHz and f_{IN2} = 172.1 MHz

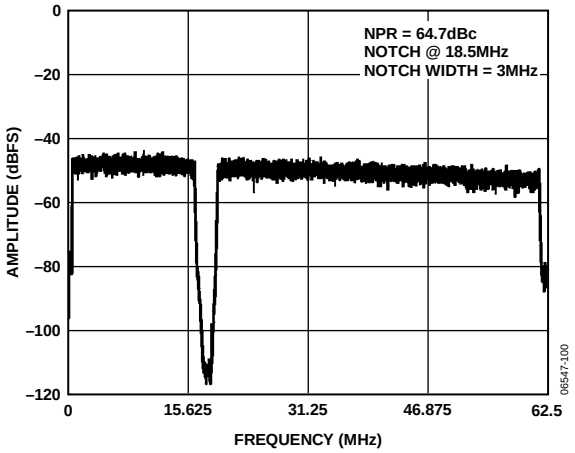


Figure 38. AD9640 Noise Power Ratio (NPR)

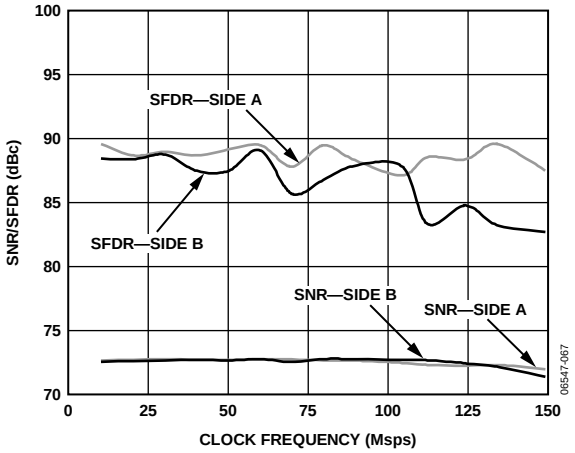


Figure 39. AD9640-125 Single-Tone SNR/SFDR vs. Clock Frequency (f_S) with f_{IN} = 2.3 MHz

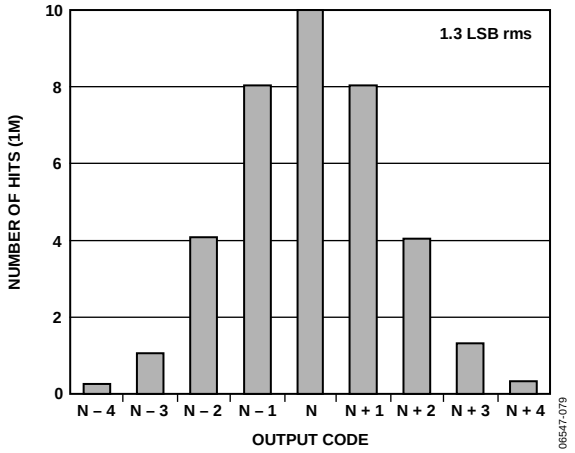


Figure 40. AD9640 Grounded Input Histogram

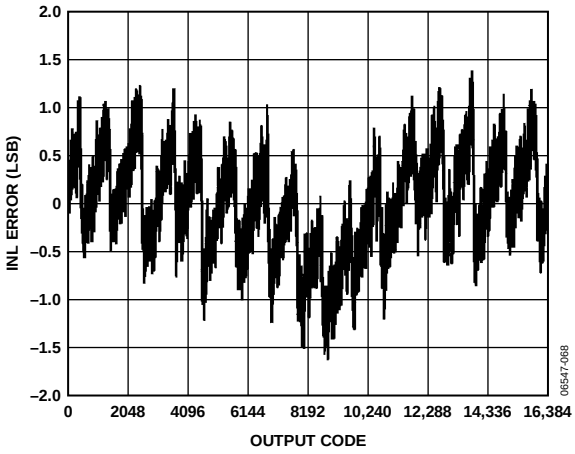


Figure 41. AD9640 INL with f_{IN} = 10.3 MHz

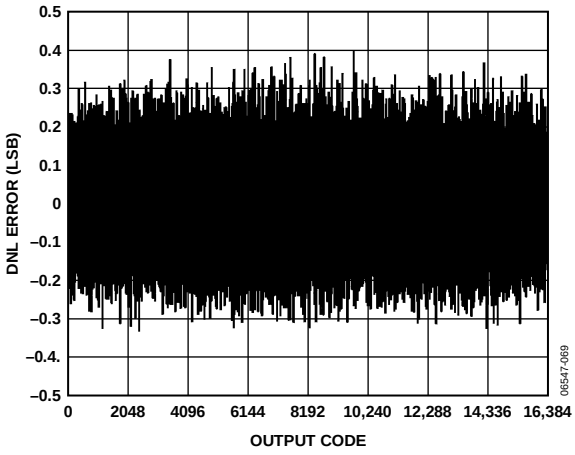


Figure 42. AD9640 DNL with f_{IN} = 10.3 MHz

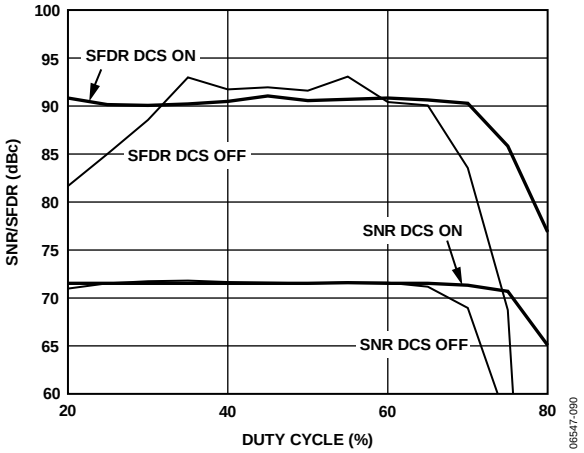


Figure 43. AD9640 SNR/SFDR vs. Duty Cycle with f_{IN} = 10.3 MHz

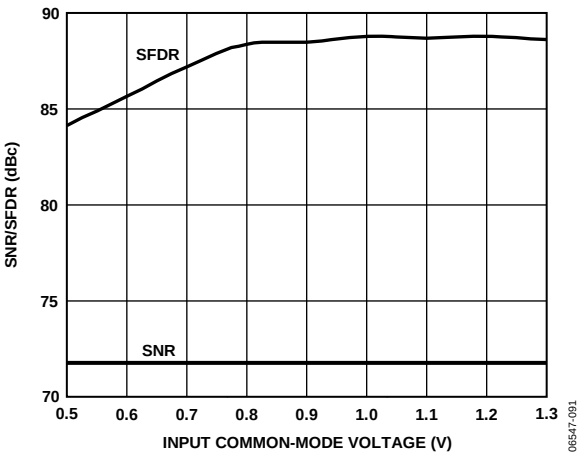


Figure 44. AD9640 SNR/SFDR vs. Input Common Mode Voltage (VCM) with f_{IN} = 30 MHz

THEORY OF OPERATION

The AD9640 dual ADC design can be used for diversity reception of signals, where the ADCs are operating identically on the same carrier but from two separate antennae. The ADCs can also be operated with independent analog inputs. The user can sample any $f_S/2$ frequency segment from dc to 200 MHz using appropriate low-pass or band-pass filtering at the ADC inputs with little loss in ADC performance. Operation to 450 MHz analog input is permitted but occurs at the expense of increased ADC distortion.

In nondiversity applications, the AD9640 can be used as a baseband receiver, where one ADC is used for I input data and the other is used for Q input data.

Synchronizaton capability is provided to allow synchronized timing between multiple channels or multiple devices.

Programming and control of the AD9640 are accomplished using a 3-bit SPI-compatible serial interface.

ADC ARCHITECTURE

The AD9640 architecture consists of a dual front-end sample-and-hold amplifier (SHA), followed by a pipelined, switched capacitor ADC. The quantized outputs from each stage are combined into a final 14-bit result in the digital correction logic. The pipelined architecture permits the first stage to operate on a new input sample, and the remaining stages operate on preceding samples. Sampling occurs on the rising edge of the clock.

Each stage of the pipeline, excluding the last, consists of a low resolution flash ADC connected to a switched capacitor digital-to-analog converter (DAC) and an interstage residue amplifier (MDAC). The residue amplifier magnifies the difference between the reconstructed DAC output and the flash input for the next stage in the pipeline. One bit of redundancy is used in each stage to facilitate digital correction of flash errors. The last stage simply consists of a flash ADC.

The input stage of each channel contains a differential SHA that can be ac- or dc-coupled in differential or single-ended modes. The output staging block aligns the data, carries out error correction, and passes the data to the output buffers. The output buffers are powered from a separate supply, allowing adjustment of the output voltage swing. During power-down, the output buffers go into a high impedance state.

ANALOG INPUT CONSIDERATIONS

The analog input to the AD9640 is a differential switched capacitor SHA that has been designed for optimum performance while processing a differential input signal.

The clock signal alternatively switches the SHA between sample mode and hold mode (see Figure 45). When the SHA is switched into sample mode, the signal source must be capable of charging the sample capacitors and settling within ½ of a clock cycle.

A small resistor in series with each input can help reduce the peak transient current required from the output stage of the driving source. A shunt capacitor can be placed across the inputs to provide dynamic charging currents. This passive network creates a low-pass filter at the ADC input; therefore, the precise values are dependent on the application.

In intermediate frequency (IF) undersampling applications, any shunt capacitors should be reduced. In combination with the driving source impedance, they limit the input bandwidth. See the AN-742 Application Note, *Frequency Domain Response of Switched-Capacitor ADCs*; the AN-827 Application Note, *A Resonant Approach to Interfacing Amplifiers to Switched-Capacitor ADCs*; and the *Analog Dialogue* article, "Transformer-Coupled Front-End for Wideband A/D Converters" for more information on this subject.

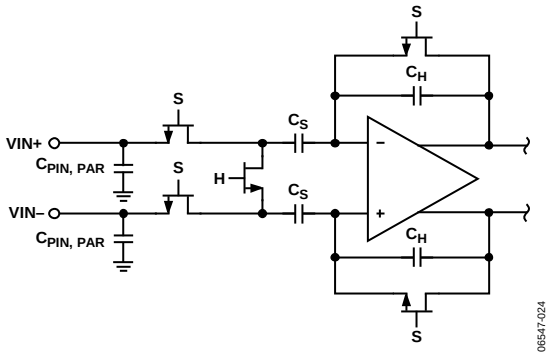


Figure 45. Switched-Capacitor SHA Input

For best dynamic performance, the source impedances driving VIN+ and VIN− should be matched.

An internal differential reference buffer creates positive and negative reference voltages that define the input span of the ADC core. The span of the ADC core is set by the buffer to 2 × VREF.

Input Common Mode

The analog inputs of the AD9640 are not internally dc biased. In ac-coupled applications, the user must provide this bias externally. Setting the device so that V_{CM} = 0.55 × AVDD is recommended for optimum performance, but the device functions over a wider range with reasonable performance (see Figure 44). An on-board common-mode voltage reference is included in the design and is available from the CML pin. Optimum performance is achieved when the common-mode voltage of the analog input is set by the CML pin voltage (typically 0.55 × AVDD). The CML pin must be decoupled to ground by a 0.1 µF capacitor, as described in the Applications Information section.

Differential Input Configurations

Optimum performance is achieved while driving the AD9640 in a differential input configuration. For baseband applications, the AD8138 differential driver provides excellent performance and a flexible interface to the ADC.

The output common-mode voltage of the AD8138 is easily set with the CML pin of the AD9640 (see Figure 46), and the driver can be configured in a Sallen-Key filter topology to provide band limiting of the input signal.

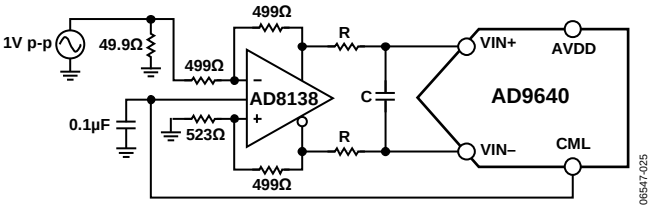


Figure 46. Differential Input Configuration Using the AD8138

For baseband applications where SNR is a key parameter, differential transformer coupling is the recommended input configuration. An example is shown in Figure 47. To bias the analog input, the CML voltage can be connected to the center tap of the transformer's secondary winding.

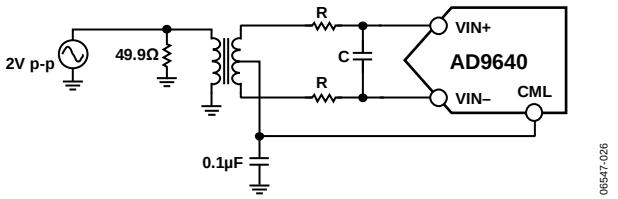


Figure 47. Differential Transformer-Coupled Configuration

The signal characteristics must be considered when selecting a transformer. Most RF transformers saturate at frequencies below a few MHz, and excessive signal power can also cause core saturation, which leads to distortion.

At input frequencies in the second Nyquist zone and above, the noise performance of most amplifiers is not adequate to achieve the true SNR performance of the AD9640. For applications where SNR is a key parameter, differential double balun coupling is the recommended input configuration (see Figure 49 for an example).

An alternative to using a transformer coupled input at frequencies in the second Nyquist zone is to use the AD8352 differential driver. An example is shown in Figure 50. See the AD8352 data sheet for more information.

In any configuration, the value of Shunt Capacitor C is dependent on the input frequency and source impedance and may need to be reduced or removed. Table 13 displays recommended values to set the RC network. However, these values are dependent on the input signal and should be used only as a starting guide.

Table 13. Example RC Network

Frequency Range (MHz)	R Series (Ω Each)	C Differential (pF)
0 to 70	33	15
70 to 200	33	5
200 to 300	15	5
>300	15	Open

Single-Ended Input Configuration

A single-ended input can provide adequate performance in cost sensitive applications. In this configuration, SFDR and distortion performance degrade due to the large input common-mode swing. If the source impedances on each input are matched, there should be little effect on SNR performance. Figure 48 details a typical single-ended input configuration.

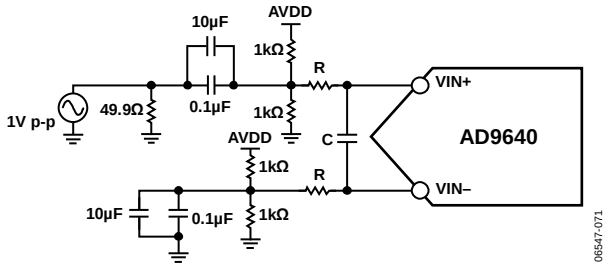


Figure 48. Single-Ended Input Configuration

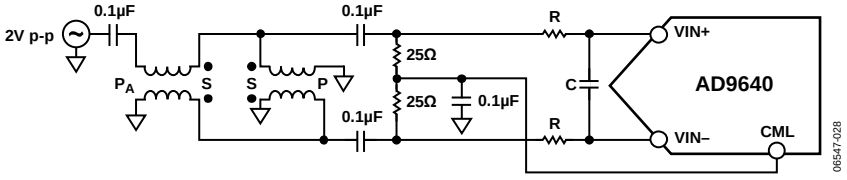


Figure 49. Differential Double Balun Input Configuration

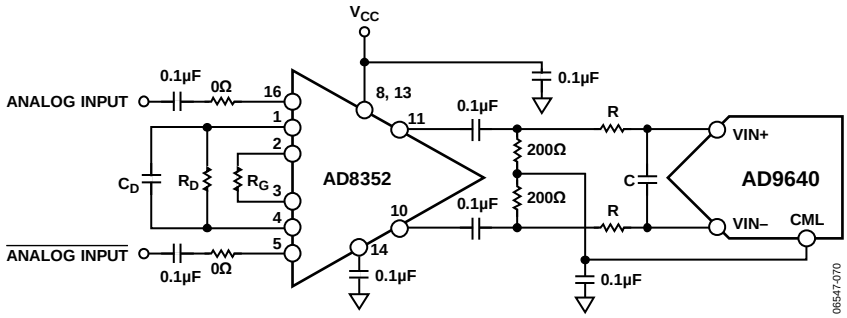


Figure 50. Differential Input Configuration Using the AD8352

VOLTAGE REFERENCE

A stable and accurate voltage reference is built into the AD9640. The input range can be adjusted by varying the reference voltage applied to the AD9640, using either the internal reference or an externally applied reference voltage. The input span of the ADC tracks reference voltage changes linearly. The various reference modes are summarized in the next few sections. The Reference Decoupling section describes the best practices PCB layout of the reference.

Internal Reference Connection

A comparator within the AD9640 detects the potential at the SENSE pin and configures the reference into four possible modes, which are summarized in Table 14. If SENSE is grounded, the reference amplifier switch is connected to the internal resistor divider (see Figure 51), setting VREF to 1 V. Connecting the SENSE pin to VREF switches the reference amplifier output to the SENSE pin, completing the loop and providing a 0.5 V reference output. If a resistor divider is connected external to the chip, as shown in Figure 52, the switch again sets to the SENSE pin. This puts the reference amplifier in a noninverting mode with the VREF output defined as

$$VREF = 0.5 \times \left(1 + \frac{R2}{R1}\right)$$

The input range of the ADC always equals twice the voltage at the reference pin for either an internal or an external reference.

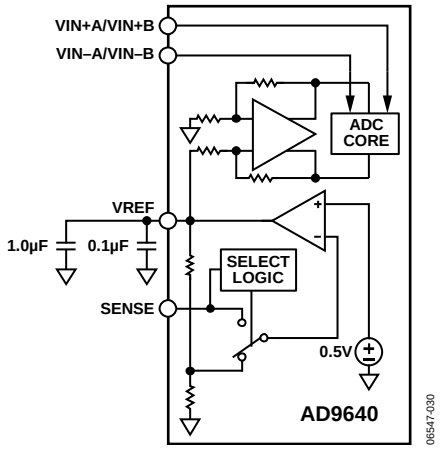


Figure 51. Internal Reference Configuration

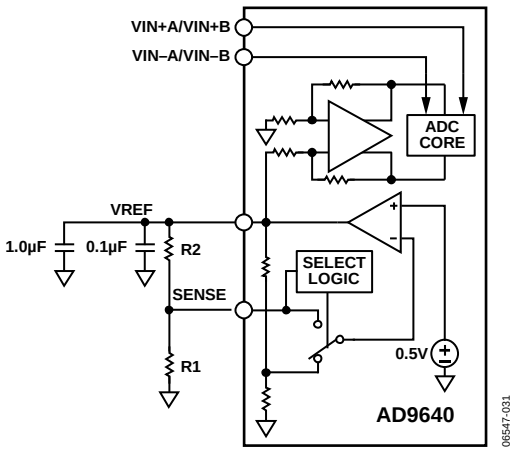


Figure 52. Programmable Reference Configuration

If the internal reference of the AD9640 is used to drive multiple converters to improve gain matching, the loading of the reference by the other converters must be considered. Figure 53 shows how the internal reference voltage is affected by loading.

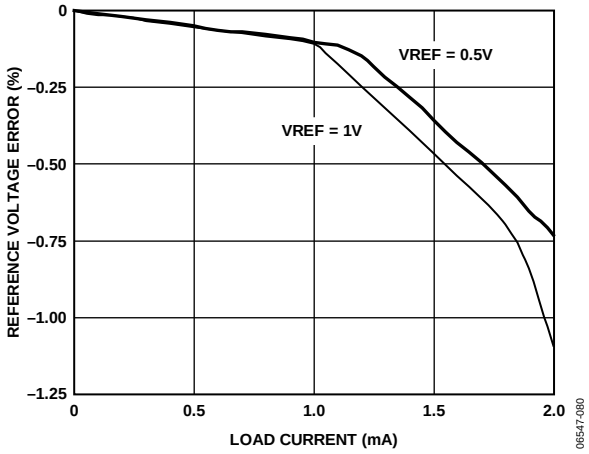


Figure 53. VREF Accuracy vs. Load

External Reference Operation

The use of an external reference may be necessary to enhance the gain accuracy of the ADC or improve thermal drift characteristics. Figure 54 shows the typical drift characteristics of the internal reference in 1 V mode.

Table 14. Reference Configuration Summary

Selected Mode	SENSE Voltage	Resulting VREF (V)	Resulting Differential Span (V p-p)
External Reference	AVDD	N/A	2 × External Reference
Internal Fixed Reference	VREF	0.5	1.0
Programmable Reference	0.2 V to VREF	$0.5 \times \left(1 + \frac{R2}{R1}\right)$ (see Figure 52)	2 × VREF
Internal Fixed Reference	AGND to 0.2 V	1.0	2.0

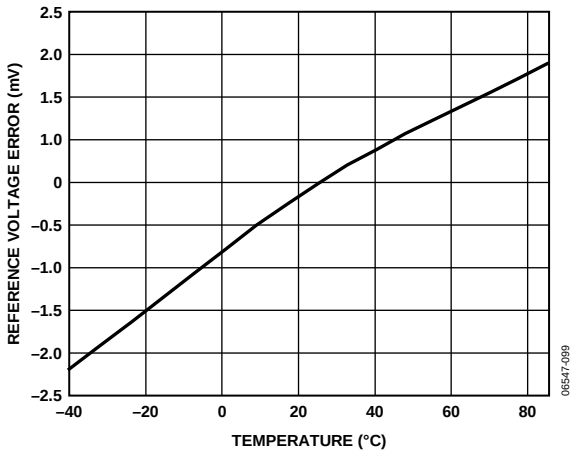


Figure 54. Typical VREF Drift

When the SENSE pin is tied to AVDD, the internal reference is disabled, allowing the use of an external reference. An internal reference buffer loads the external reference with an equivalent 6 kΩ load (see Figure 15). The internal buffer generates the positive and negative full-scale references for the ADC core. Therefore, the external reference must be limited to a maximum of 1 V.

CLOCK INPUT CONSIDERATIONS

For optimum performance, the AD9640 sample clock inputs CLK+, and CLK– should be clocked with a differential signal. The signal is typically ac-coupled into the CLK+ and CLK– pins via a transformer or capacitors. These pins are biased internally (see Figure 55) and require no external bias.

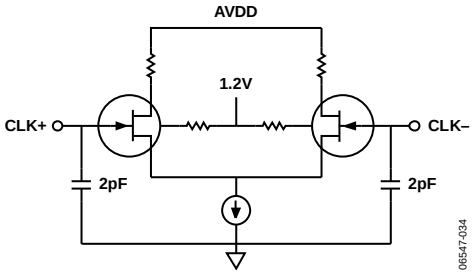


Figure 55. Equivalent Clock Input Circuit

Clock Input Options

The AD9640 has a very flexible clock input structure. Clock input can be a CMOS, LVDS, LVPECL, or sine wave signal. Regardless of the type of signal being used, the jitter of the clock source is of the most concern, as described in the Jitter Considerations section.

Figure 56 and Figure 57 show two preferred methods for clocking the AD9640 (at clock rates to 625 MHz). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF balun or an RF transformer. The RF balun configuration is recommended for clock frequencies between 125 MHz and 625 MHz, and the RF transformer is recommended for clock frequencies from 10 MHz to 200MHz. The back-to-back Schottky diodes across the transformer/balun secondary limit clock excursions into the AD9640 to approximately 0.8 V p-p differential.

This helps prevent the large voltage swings of the clock from feeding through to other portions of the AD9640, while preserving the fast rise and fall times of the signal that are critical to a low jitter performance.

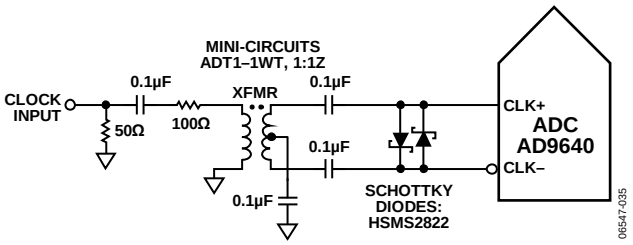


Figure 56. Transformer Coupled Differential Clock (Up to 200 MHz)

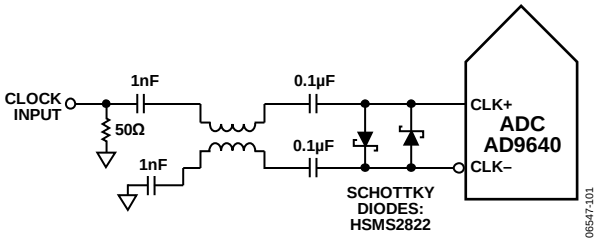


Figure 57. Balun Coupled Differential Clock (Up to 625 MHz)

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input pins, as shown in Figure 58. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

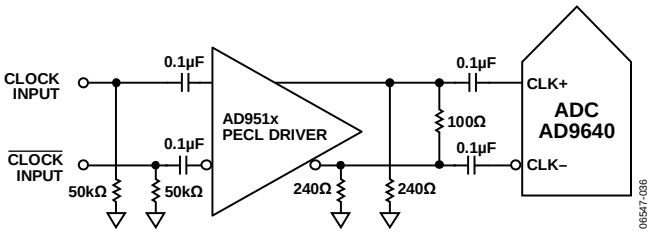


Figure 58. Differential PECL Sample Clock (Up to 625 MHz)

A third option is to ac-couple a differential LVDS signal to the sample clock input pins, as shown in Figure 59. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516 clock drivers offer excellent jitter performance.

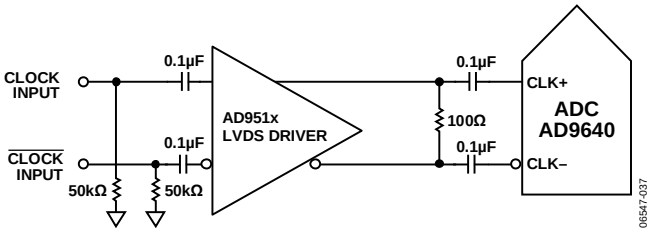


Figure 59. Differential LVDS Sample Clock (Up to 625 MHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended CMOS signal. In such applications, CLK+ should be directly driven from a CMOS gate, and the CLK– pin should be bypassed to ground with a 0.1 µF capacitor in parallel with a 39 kΩ resistor (see Figure 60).

CLK+ can be directly driven from a CMOS gate. Although the CLK+ input circuit supply is AVDD (1.8 V), this input is designed to withstand input voltages up to 3.6 V, making the selection of the drive logic voltage very flexible.

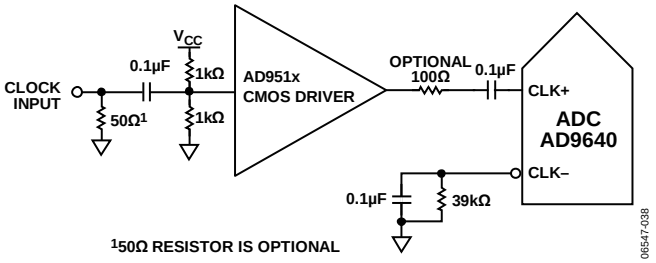


Figure 60. Single-Ended 1.8 V CMOS Sample Clock (Up to 150 MSPS)

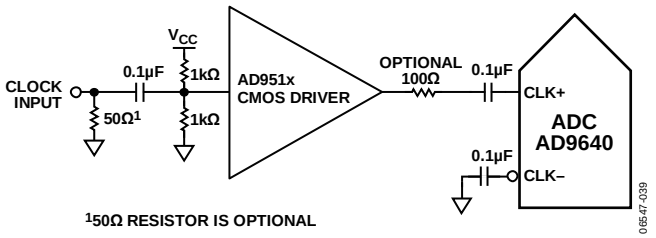


Figure 61. Single-Ended 3.3 V CMOS Sample Clock (Up to 150 MSPS)

Input Clock Divider

The AD9640 contains an input clock divider with the ability to divide the input clock by integer values between 1 and 8. If a divide ratio other than 1 is selected, the duty cycle stabilizer is automatically enabled.

The AD9640 clock divider can be synchronized using the external SYNC input. Bit 1 and Bit 2 of Register 0x100 allow the clock divider to be resynchronized on every SYNC signal or only on the first SYNC signal after the register is written. A valid SYNC causes the clock divider to reset to its initial state. This synchronization feature allows multiple parts to have their clock dividers aligned to guarantee simultaneous input sampling.

Clock Duty Cycle

Typical high speed ADCs use both clock edges to generate a variety of internal timing signals and, as a result, may be sensitive to clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The AD9640 contains a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. This allows the user to provide a wide range of clock input duty cycles without affecting the performance of the AD9640. Noise and distortion performance are nearly flat for a wide range of duty cycles with the DCS on, as shown in Figure 43.

Jitter in the rising edge of the input is still of paramount concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates less than 20 MHz nominally. The loop has a time constant associated with it that needs to be considered where the clock rate can change dynamically. This requires a wait time of 1.5 µs to 5 µs after a dynamic clock frequency increase or decrease before the DCS loop is relocked to the input signal. During the time period the loop is not locked, the DCS loop is bypassed, and internal device timing is dependent on the duty cycle of the input clock signal. In such applications, it may be appropriate to disable the duty cycle stabilizer. In all other applications, enabling the DCS circuit is recommended to maximize ac performance.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The degradation in SNR from the low frequency SNR (SNR_{LF}) at a given input frequency (f_{INPUT}) due to jitter (t_{JRMS}) can be calculated by

$$SNR_{HF} = -10 \log[(2\pi \times f_{INPUT} \times t_{JRMS})^2 + 10^{(-SNR_{LF}/10)}]$$

In the equation, the rms aperture jitter represents the clock input jitter specification. IF undersampling applications are particularly sensitive to jitter, as illustrated in Figure 62.

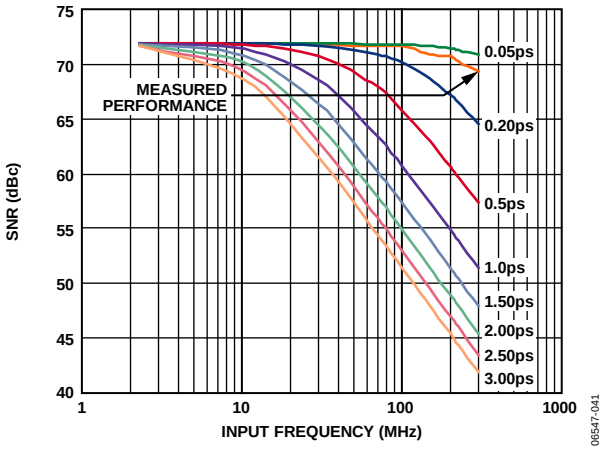


Figure 62. SNR vs. Input Frequency and Jitter

The clock input should be treated as an analog signal in cases where aperture jitter may affect the dynamic range of the AD9640. Power supplies for clock drivers should be separated from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal-controlled oscillators make the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it should be retimed by the original clock at the last step.

See the AN-501 Application Note and AN-756 Application Note for more information about jitter performance as it relates to ADCs.

POWER DISSIPATION AND STANDBY MODE

As shown in Figure 63, the power dissipated by the AD9640 is proportional to its sample rate. In CMOS output mode, the digital power dissipation is determined primarily by the strength of the digital drivers and the load on each output bit.

The maximum DRVDD current (I_{DRVDD}) can be calculated as

$$I_{DRVDD} = V_{DRVDD} \times C_{LOAD} \times f_{CLK} \times N$$

where N is the number of output bits (30 in the case of the AD9640 with the FD bits disabled). This maximum current occurs when every output bit switches on every clock cycle, that is, a full-scale square wave at the Nyquist frequency of $f_{CLK}/2$. In practice, the DRVDD current is established by the average number of output bits switching, which is determined by the sample rate and the characteristics of the analog input signal.

Reducing the capacitive load presented to the output drivers can minimize digital power consumption. The data in Figure 63 was taken with the same operating conditions as the Typical Performance Characteristics, with a 5 pF load on each output driver.

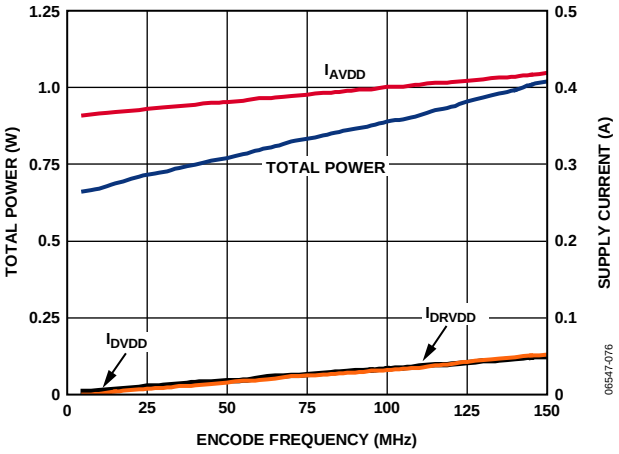


Figure 63. AD9640-150 Power and Current vs. Clock Frequency

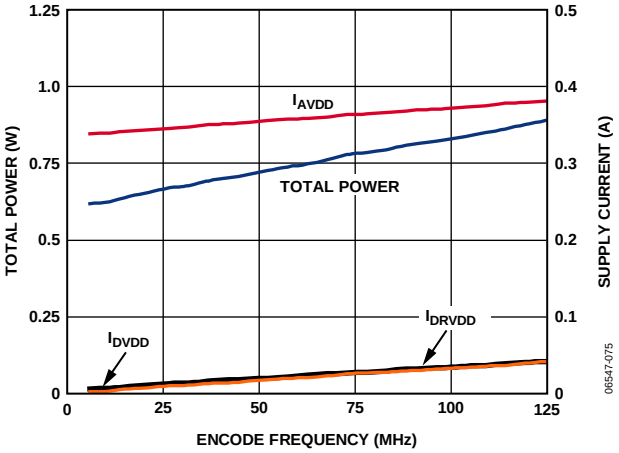


Figure 64. AD9640-125 Power and Current vs. Clock Frequency

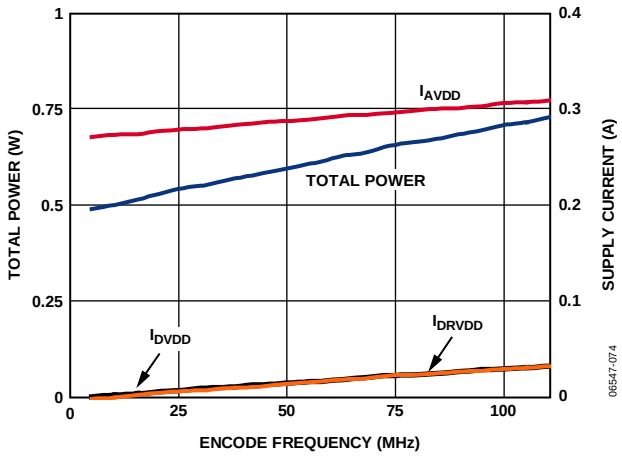


Figure 65. AD9640-105 Power and Current vs. Clock Frequency

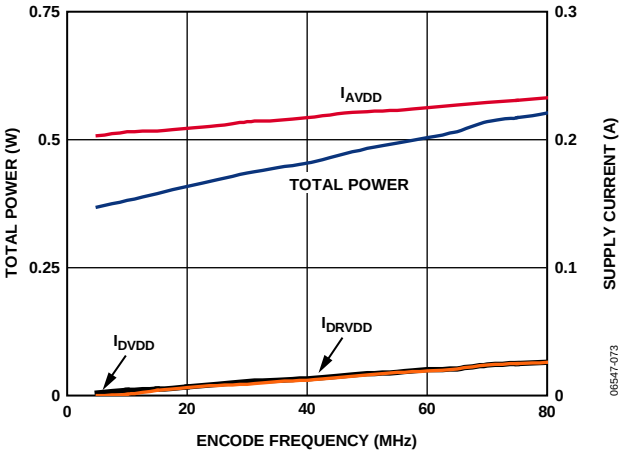


Figure 66. AD9640-80 Power and Current vs. Clock Frequency

By asserting PDWN (either through the SPI port or by asserting the PDWN pin high), the AD9640 is placed in power-down mode. In this state, the ADC typically dissipates 2.5 mW. During power-down, the output drivers are placed in a high impedance state. Asserting the PDWN pin low returns the AD9640 to its normal operational mode. Note that PDWN is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

Low power dissipation in power-down mode is achieved by shutting down the reference, reference buffer, biasing networks, and clock. Internal capacitors are discharged when entering power-down mode and then must be recharged when returning to normal operation. As a result, wake-up time is related to the time spent in power-down mode, and shorter power-down cycles result in proportionally shorter wake-up times.

When using the SPI port interface, the user can place the ADC in power-down mode or standby mode. Standby mode allows the user to keep the internal reference circuitry powered when faster wake-up times are required. See the Memory Map Register Description section for more details.

DIGITAL OUTPUTS

The AD9640 output drivers can be configured to interface with 1.8 V to 3.3 V CMOS logic families by matching DRVDD to the digital supply of the interfaced logic. The AD9640 can also be configured for LVDS outputs using a DRVDD supply voltage of 1.8 V.

In CMOS output mode, the output drivers are sized to provide sufficient output current to drive a wide variety of logic families. However, large drive currents tend to cause current glitches on the supplies that may affect converter performance.

Applications requiring the ADC to drive large capacitive loads or large fan-outs may require external buffers or latches.

The output data format can be selected for either offset binary or twos complement by setting the SCLK/DFS pin when operating in the external pin mode (see Table 15).

As detailed in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, the data format can be selected for offset binary, twos complement, or gray code when using the SPI control.

Table 15. SCLK/DFS Mode Selection (External Pin Mode)

Voltage at Pin	SCLK/DFS	SDIO/DCS
AGND	Offset binary (default)	DCS disabled
AVDD	Twos complement	DCS enabled (default)

Digital Output Enable Function (OEB)

The AD9640 has a flexible three-state ability for the digital output pins. The three-state mode is enabled using the SMI SDO/OEB pin or through the SPI interface. If the SMI SDO/OEB pin is low, the output data drivers are enabled. If the SMI SDO/OEB pin is high, the output data drivers are placed in a high impedance state. This OEB function is not intended for rapid access to the data bus. Note that OEB is referenced to the digital supplies (DRVDD) and should not exceed that supply voltage.

When using the SPI interface, the data and fast detect outputs of each channel can be independently three-stated by using the output enable bar bit in Register 0x14.

TIMING

The AD9640 provides latched data with a pipeline delay of twelve clock cycles. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the clock signal.

The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9640. These transients can degrade converter dynamic performance.

The lowest typical conversion rate of the AD9640 is 10 MSPS. At clock rates below 10 MSPS, dynamic performance can degrade.

Data Clock Output (DCO)

The AD9640 provides two data clock output (DCO) signals intended for capturing the data in an external register. The data outputs are valid on the rising edge of DCO, unless the DCO clock polarity has been changed via the SPI. See Figure 2 and Figure 3 for a graphical timing description.

Table 16. Output Data Format

Input (V)	Condition (V)	Offset Binary Output Mode	Twos Complement Mode	OVR
VIN+ – VIN–	< –VREF – 0.5 LSB	00 0000 0000 0000	10 0000 0000 0000	1
VIN+ – VIN–	= –VREF	00 0000 0000 0000	10 0000 0000 0000	0
VIN+ – VIN–	= 0	10 0000 0000 0000	00 0000 0000 0000	0
VIN+ – VIN–	= +VREF – 1.0 LSB	11 1111 1111 1111	01 1111 1111 1111	0
VIN+ – VIN–	> +VREF – 0.5 LSB	11 1111 1111 1111	01 1111 1111 1111	1

ADC OVERRANGE AND GAIN CONTROL

In receiver applications, it is desirable to have a mechanism to reliably determine when the converter is about to be clipped. The standard overflow indicator provides after-the-fact information on the state of the analog input that is of limited usefulness. Therefore, it is helpful to have a programmable threshold below full scale that allows time to reduce the gain before the clip actually occurs. In addition, because input signals can have significant slew rates, latency of this function is of major concern. Highly pipelined converters can have significant latency. A good compromise is to use the output bits from the first stage of the ADC for this function. Latency for these output bits is very low, and overall resolution is not highly significant. Peak input signals are typically between full scale and 6 dB to 10 dB below full scale. A 3-bit or 4-bit output provides adequate range and resolution for this function.

Using the SPI port, the user can provide a threshold above which an overrange output is active. As long as the signal is below that threshold, the output should remain low. The fast detect outputs can also be programmed via the SPI port so that one of the pins functions as a traditional overrange pin for customers who currently use this feature. In this mode, all 14 bits of the converter are examined in the traditional manner, and the output is high for the condition normally defined as overflow. In either mode, the magnitude of the data is considered in the calculation of the condition (but the sign of the data is not considered). The threshold detection responds identically to positive and negative signals outside the desired range (magnitude).

FAST DETECT OVERVIEW

The AD9640 contains circuitry to facilitate fast overrange detection, allowing very flexible external gain control implementations. Each ADC has four fast detect (FD) output pins that are used to output information about the current state of the ADC input level. The function of these pins is programmable via the fast detect mode select bits and the fast detect enable bit in Register 0x104, allowing range information to be output from several points in the internal datapath. These output pins can also be set up to indicate the presence of overrange or underrange conditions, according to programmable threshold levels. Table 17 shows the six configurations available for the fast detect pins.

Table 17. Fast Detect Mode Select Bits Settings

Fast Detect Mode Select Bits (Register 0x104[3:1])	Information Presented on Fast Detect (FD) Pins of Each ADC[1, 2]			
	FD3	FD2	FD1	FD0
000	ADC fast magnitude (see Table 18)			
001	ADC fast magnitude (see Table 19)			OR
010	ADC fast magnitude (see Table 20)		OR	F_LT
011	ADC fast magnitude (see Table 20)		C_UT	F_LT
100	OR	C_UT	F_UT	F_LT
101	OR	F_UT	IG	DG

[1] The fast detect pins are FD0A/FD0B to FD3A/FD3B for the CMOS mode configuration and FD0+/FD0– to FD3+/FD3– for the LVDS mode configuration.
[2] See the ADC Overrange (OR) and Gain Switching sections for more information about OR, C_UT, F_UT, F_LT, IG, and DG.

ADC FAST MAGNITUDE

When the fast detect output pins are configured to output the ADC fast magnitude (that is, when the fast detect mode select bits are set to 0b000), the information presented is the ADC level from an early converter stage with a latency of only two clock cycles (when in CMOS output mode). Using the fast detect output pins in this configuration provides the earliest possible level indication information. Because this information is provided early in the datapath, there is significant uncertainty in the level indicated. The nominal levels, along with the uncertainty indicated by the ADC fast magnitude, are shown in Table 18.

Table 18. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 000

ADC Fast Magnitude on FD[3:0] Pins	Nominal Input Magnitude Below FS (dB)	Nominal Input Magnitude Uncertainty (dB)
0000	<−24	Minimum to −18.07
0001	−24 to −14.5	−30.14 to −12.04
0010	−14.5 to −10	−18.07 to −8.52
0011	−10 to −7	−12.04 to −6.02
0100	−7 to −5	−8.52 to −4.08
0101	−5 to −3.25	−6.02 to −2.5
0110	−3.25 to −1.8	−4.08 to −1.16
0111	−1.8 to −0.56	−2.5 to FS
1000	−0.56 to 0	−1.16 to 0

When the fast detect mode select bits are set to 0b001, 0b010, or 0b011, a subset of the fast detect output pins is available. In these modes, the fast detect output pins have a latency of six clock cycles. Table 19 shows the corresponding ADC input levels when the fast detect mode select bits are set to 0b001 (that is, when ADC fast magnitude is presented on the FD[3:1] pins).

Table 19. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 001

ADC Fast Magnitude on FD[3:1] Pins	Nominal Input Magnitude Below FS (dB)	Nominal Input Magnitude Uncertainty (dB)
000	<−24	Minimum to −18.07
001	−24 to −14.5	−30.14 to −12.04
010	−14.5 to −10	−18.07 to −8.52
011	−10 to −7	−12.04 to −6.02
100	−7 to −5	−8.52 to −4.08
101	−5 to −3.25	−6.02 to −2.5
110	−3.25 to −1.8	−4.08 to −1.16
111	−1.8 to 0	−2.5 to 0

When the fast detect mode select bits are set to 0b010 or 0b011 (that is, when ADC fast magnitude is presented on the FD[3:2] pins), the LSB is not provided. The input ranges for this mode are shown in Table 20.

Table 20. ADC Fast Magnitude Nominal Levels with Fast Detect Mode Select Bits = 010 or 011

ADC Fast Magnitude on FD[2:1] Pins	Nominal Input Magnitude Below FS (dB)	Nominal Input Magnitude Uncertainty (dB)
00	<−14.5	Minimum to −12.04
01	−14.5 to −7	−18.07 to −6.02
10	−7 to −3.25	−8.52 to −2.5
11	−3.25 to 0	−4.08 to 0

ADC OVERRANGE (OR)

The ADC overrange indicator is asserted when an overrange is detected on the input of the ADC. The overrange condition is determined at the output of the ADC pipeline and, therefore, is subject to a latency of 12 ADC clock cycles. An overrange at the input is indicated by this bit 12 clock cycles after it occurs.

GAIN SWITCHING

The AD9640 includes circuitry that is useful in applications either where large dynamic ranges exist or where gain ranging converters are employed. This circuitry allows digital thresholds to be set such that an upper threshold and a lower threshold can be programmed. Fast detect mode select bit = 010 through fast detect mode select bit = 101 support various combinations of the gain switching options.

One such use is to detect when an ADC is about to reach full scale with a particular input condition. The result is to provide an indicator that can be used to quickly insert an attenuator that prevents ADC overdrive.

Coarse Upper Threshold (C_UT)

The coarse upper threshold indicator is asserted if the ADC fast magnitude input level is greater than the level programmed in the coarse upper threshold register (Address 0x105[2:0]). The coarse upper threshold output is output two clock cycles after the level is exceeded at the input and, therefore, provides a fast indication of the input signal level. The coarse upper threshold levels are listed in Table 21. This indicator remains asserted for a minimum of two ADC clock cycles or until the signal drops below the threshold level.

Table 21. Coarse Upper Threshold Levels

Coarse Upper Threshold Register 0x105[2:0]	C_UT Is Active When Signal Magnitude Below FS Is Greater Than (dB)
000	<−24
001	−24
010	−14.5
011	−10
100	−7
101	−5
110	−3.25
111	−1.8

Fine Upper Threshold (F_UT)

The fine upper threshold indicator is asserted if the input magnitude exceeds the value programmed in the fine upper threshold register located in Register 0x106 and Register 0x107. The 13-bit threshold register is compared with the signal magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but is accurate in terms of the converter resolution. The fine upper threshold magnitude is defined by the following equation:

$$dBFS = 20 \log(Threshold\ Magnitude/2^{13})$$

Fine Lower Threshold (F_LT)

The fine lower threshold indicator is asserted if the input magnitude is less than the value programmed in the fine lower threshold register located at Register 0x108 and Register 0x109. The fine lower threshold register is a 13-bit register that is compared with the signal magnitude at the output of the ADC. This comparison is subject to ADC clock latency but is accurate in terms of the converter resolution. The fine lower threshold magnitude is defined by the following equation:

$$dBFS = 20 \log(Threshold\ Magnitude/2^{13})$$

The operation of the fine upper threshold indicators and fine lower threshold indicators is shown in Figure 67.

Increment Gain (IG) and Decrement Gain (DG)

The increment gain and decrement gain indicators are intended to be used together to provide information to enable external gain control. The decrement gain indicator works in conjunction with the coarse upper threshold bits, asserting when the input magnitude is greater than the 3-bit value in the coarse upper threshold register (Address 0x105). The increment gain indicator,

similarly, corresponds to the fine lower threshold bits, except that it is asserted only if the input magnitude is less than the value programmed in the fine lower threshold register after the dwell time elapses. The dwell time is set by the 16-bit dwell time value located at Address 0x10A and Address 0x10B and is set in units of ADC input clock cycles ranging from 1 to 65,535. The fine lower threshold register is a 13-bit register that is compared with the magnitude at the output of the ADC. This comparison is subject to the ADC clock latency but allows a finer, more accurate comparison. The fine upper threshold magnitude is defined by the following equation:

$$dBFS = 20 \log(Threshold\ Magnitude/2^{13})$$

The decrement gain output works from the ADC fast detect output pins, providing a fast indication of potential overrange conditions. The increment gain uses the comparison at the output of the ADC, requiring the input magnitude to remain below an accurate, programmable level for a predefined period before signaling external circuitry to increase the gain.

The operation of the increment gain output and the decrement gain output is shown in Figure 67.

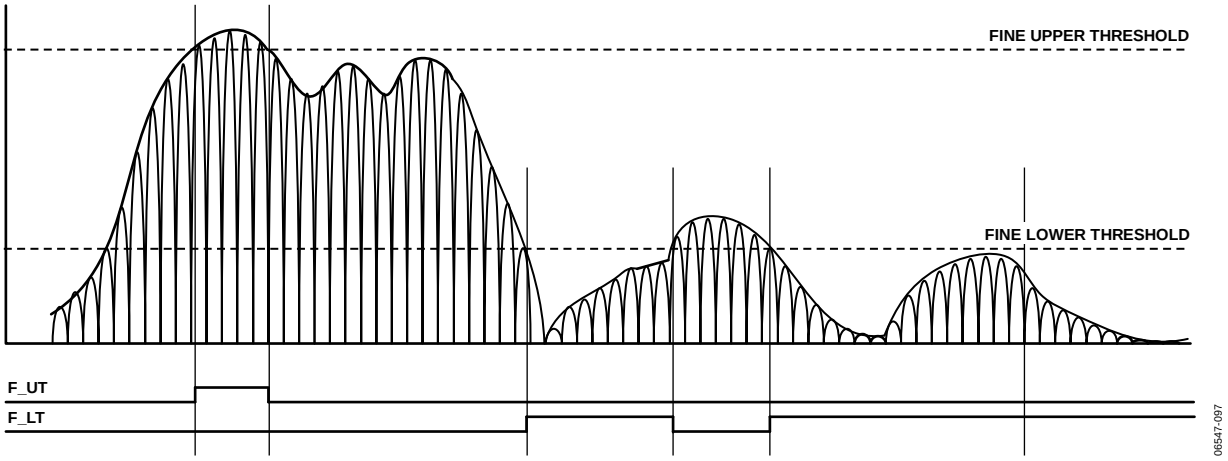


Figure 67. Threshold Settings for F_UT and F_LT

SIGNAL MONITOR

The signal monitor block provides additional information about the signal being digitized by the ADC. The signal monitor computes the rms input magnitude, the peak magnitude, and/or the number of samples by which the magnitude exceeds a particular threshold. Together, these functions can be used to gain insight into the signal characteristics and to estimate the peak/average ratio or even the shape of the complementary cumulative distribution function (CCDF) curve of the input signal. This information can be used to drive an AGC loop to optimize the range of the ADC in the presence of real-world signals.

The signal monitor result values can be obtained from the part by reading back internal registers at Address 0x116 to Address 0x11B, using the SPI port or the signal monitor SPORT output. The output contents of the SPI-accessible signal monitor registers are set via the two signal monitor mode bits of the signal monitor control register. Both ADC channels must be configured for the same signal monitor mode (Address 0x112). Separate SPI-accessible, 20-bit signal monitor result (SMR) registers are provided for each ADC channel. Any combination of the signal monitor functions can also be output to the user via the serial SPORT interface. These outputs are enabled using the peak detector output enable bit, the rms/ms magnitude output enable bit, and the threshold crossing output enable bit in the signal monitor SPORT control register.

For each signal monitor measurement, a programmable signal monitor period register (SMPR) controls the duration of the measurement. This period of time is programmed as the number of input clock cycles in a 24-bit signal monitor period register located at Address 0x113, Address 0x114, and Address 0x115. This register can be programmed with a period from 128 samples to 16.78 (2^{24}) million samples.

Because the dc offset of the ADC can be significantly larger than the signal of interest (affecting the results from the signal monitor), a dc correction circuit is included as part of the signal monitor block to null the dc offset before measuring the power.

PEAK DETECTOR MODE

The magnitude of the input port signal is monitored over a programmable time period (determined by the SMPR) to give the peak value detected. This function is enabled by programming a Logic 1 in the signal monitor mode bits of the signal monitor control register or by setting the peak detector output enable bit in the signal monitor SPORT control register. The 24-bit SMPR must be programmed before activating this mode.

After enabling this mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started. The magnitude of the input signal is compared with the value in the internal peak level holding register (not accessible to the user), and the greater of the two is updated as the current peak level. The initial value of the peak level holding register is set to the current ADC input signal magnitude. This comparison continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the 13-bit peak level value is transferred to the signal monitor holding register (not accessible to the user), which can be read through the SPI port or output through the SPORT serial interface. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the magnitude of the first input sample is updated in the peak level holding register, and the comparison and update procedure, as explained previously, continues.

Figure 68 is a block diagram of the peak detector logic. The SMR register contains the absolute magnitude of the peak detected by the peak detector logic.

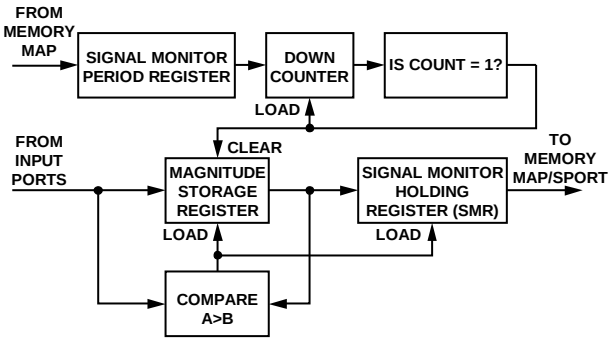


Figure 68. ADC Input Peak Detector Block Diagram

RMS/MS MAGNITUDE MODE

In this mode, the root-mean-square (rms) or mean-square (ms) magnitude of the input port signal is integrated (by adding an accumulator) over a programmable period of time (determined by the SMPR) to give the rms or ms magnitude of the input signal. This mode is set by programming Logic 0 in the signal monitor mode bits of the signal monitor control register or by setting the rms/ms magnitude output enable bit in the signal monitor SPORT control register. The 24-bit SMPR, representing the period over which integration is performed, must be programmed before activating this mode.

After enabling the rms/ms magnitude mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started immediately. Each input sample is converted to floating-point format and squared. It is then converted to 11-bit, fixed-point format and added to the contents of the 24-bit accumulator. The integration continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the square root of the value in the accumulator is taken and transferred, after some formatting, to the signal monitor holding register, which can be read through the SPI port or output through the SPORT serial port. The monitor period timer is reloaded with the value in the SMPR, and the countdown is restarted. In addition, the first input sample signal power is updated in the accumulator, and the accumulation continues with the subsequent input samples.

Figure 69 illustrates the rms magnitude monitoring logic.

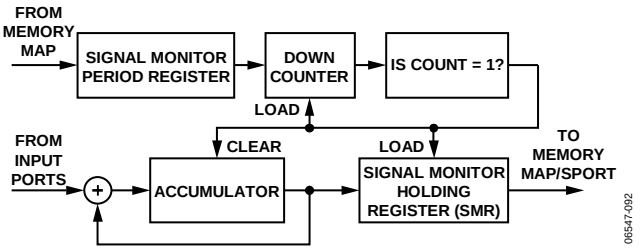


Figure 69. ADC Input RMS Magnitude Monitoring Block Diagram

For rms magnitude mode, the value in the signal monitor result (SMR) register is a 20-bit fixed-point number. The following equation can be used to determine the rms magnitude in dBFS from the MAG value in the register. Note that if the signal monitor period (SMP) is a power of 2, the second term in the equation becomes 0.

$$RMS\ Magnitude = 20\log\left(\frac{MAG}{2^{20}}\right) - 10\log\left[\frac{SMP}{2^{ceil[\log_2(SMP)]}}\right]$$

For ms magnitude mode, the value in the SMR is a 20-bit fixed-point number. The following equation can be used to determine the ms magnitude in dBFS from the MAG value in the register. Note that if the SMP is a power of 2, the second term in the equation becomes 0.

$$MS\ Magnitude = 10\log\left(\frac{MAG}{2^{20}}\right) - 10\log\left[\frac{SMP}{2^{ceil[\log_2(SMP)]}}\right]$$

THRESHOLD CROSSING MODE

In the threshold crossing mode of operation, the magnitude of the input port signal is monitored over a programmable time period (given by the SMPR) to count the number of times it crosses a certain programmable threshold value. This mode is set by programming Logic 1x (where x is a don't care bit) in the signal monitor mode bits of the signal monitor control register or by setting the threshold crossing output enable bit in the signal monitor SPORT control register. Before activating this mode, the user needs to program the 24-bit SMPR and the 13-bit upper threshold register for each individual input port. The same upper threshold register is used for both signal monitoring and gain control (see the ADC Overrange and Gain Control section).

After entering this mode, the value in the SMPR is loaded into a monitor period timer, and the countdown is started. The magnitude of the input signal is compared with the upper threshold register (programmed previously) on each input clock cycle. If the input signal has a magnitude greater than the upper threshold register, the internal count register is incremented by 1.

The initial value of the internal count register is set to 0. This comparison and incrementing of the internal count register continues until the monitor period timer reaches a count of 1.

When the monitor period timer reaches a count of 1, the value in the internal count register is transferred to the signal monitor holding register, which can be read through the SPI port or output through the SPORT serial port.

The monitor period timer is reloaded with the value in the SMPR register, and the countdown is restarted. The internal count register is also cleared to a value of 0. Figure 70 illustrates the threshold crossing logic. The value in the SMR register is the number of samples that have a magnitude greater than the threshold register.

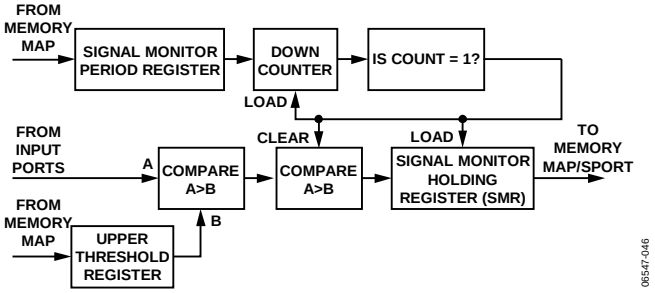


Figure 70. ADC Input Threshold Crossing Block Diagram

ADDITIONAL CONTROL BITS

For additional flexibility in the signal monitoring process, two control bits are provided in the signal monitor control register. They are the signal monitor enable bit and the complex power calculation mode enable bit.

Signal Monitor Enable Bit

The signal monitor enable bit, Bit 0 of Register 0x112, enables operation of the signal monitor block. If the signal monitor function is not needed in a particular application, this bit should be cleared (default) to conserve power.

Complex Power Calculation Mode Enable Bit

When this bit is set, the part assumes that Channel A is digitizing the I data and Channel B is digitizing the Q data for a complex input signal (or vice versa). In this mode, the power reported is equal to the following:

$$\sqrt{I^2 + Q^2}$$

This result is presented in the Signal Monitor DC Value Channel A register if the signal monitor mode bits are set to 00. The Signal Monitor DC Value Channel B register continues to compute the Channel B value.

DC CORRECTION

Because the dc offset of the ADC may be significantly larger than the signal being measured, a dc correction circuit is included to null the dc offset before measuring the power. The dc correction circuit can also be switched into the main signal path, but this may not be appropriate if the ADC is digitizing a time-varying signal with significant dc content, such as GSM.

DC Correction Bandwidth

The dc correction circuit is a high-pass filter with a programmable bandwidth (ranging between 0.15 Hz and 1.2 kHz at 125 MSPS). The bandwidth is controlled by writing Bits[5:2] of the signal monitor dc correction control register, located at Address 0x10C.

The following equation can be used to compute the bandwidth value for the dc correction circuit:

$$DC_Corr_BW = 2^{-k-14} \times \frac{f_{CLK}}{2 \times \pi}$$

where:

k is the 4 bit value programmed in Register 0x10C, Bits[5:2] (values between 0 and 13 are valid for k; programming 14 or 15 provides the same result as programming 13).

f_{CLK} is the ADC sample rate in hertz (Hz).

DC Correction Readback

The current dc correction value can be read back in Register 0x10D and Register 0x10E for Channel A and in Register 0x10F and Register 0x110 for Channel B. The dc correction value is a 14-bit value that can span the entire input range of the ADC.

DC Correction Freeze

Setting Bit 6 of Register 0x10C freezes the dc correction at its current state and continues to use the last updated value as the dc correction value. Clearing this bit restarts dc correction and adds the currently calculated value to the data.

DC Correction Enable Bits

Setting Bit 0 of Register 0x10C enables dc correction for use in the signal monitor calculations. The calculated dc correction value can be added to the output data signal path by setting Bit 1 of Register 0x10C.

SIGNAL MONITOR SPORT OUTPUT

The SPORT is a serial interface with three output pins: SMI SCLK (SPORT clock), SMI SDFS (SPORT frame sync), and SMI SDO (SPORT data output). The SPORT is the master and drives all three SPORT output pins on the chip.

SMI SCLK

The data output and frame sync are driven on the positive edge of the SMI SCLK. The SMI SCLK has three possible baud rates: 1/2, 1/4, or 1/8 the ADC clock rate, based on the SPORT controls. The SMI SCLK can also be gated off when not sending any data, based on the SPORT SMI SCLK sleep bit. Using this bit to disable the SMI SCLK when it is not needed can reduce any coupling errors back into the signal path, if these prove to be a problem in the system. Doing so, however, has the disadvantage of spreading the frequency content of the clock. If desired, the SMI SCLK can be left running to ease frequency planning.

SMI SDFS

The SMI SDFS is the serial data frame sync, and it defines the start of a frame. One SPORT frame includes data from both datapaths. The data from Datapath A is sent just after the frame sync, followed by data from Datapath B.

SMI SDO

The SMI SDO is the serial data output of the block. The data is sent MSB first on the next positive edge after the SMI SDFS. Each data output block includes one or more rms/ms magnitude, peak level, and threshold crossing values from each datapath in the stated order. If enabled, the data is sent, rms first, followed by peak and threshold, as shown in Figure 71.

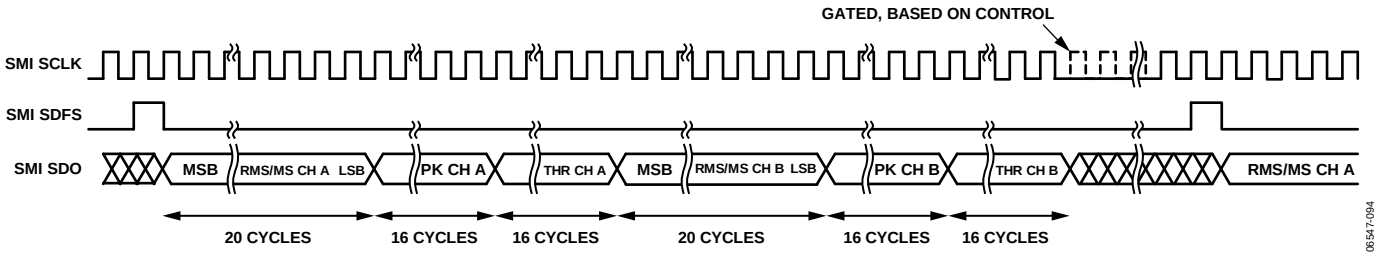


Figure 71. Signal Monitor SPORT Output Timing (RMS/MS, Peak, and Threshold Enabled)

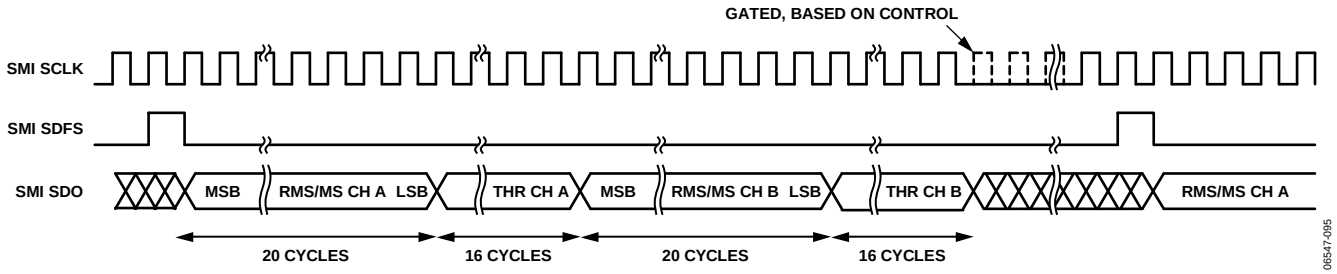


Figure 72. Signal Monitor SPORT Output Timing (RMS/MS and Threshold Enabled)

BUILT-IN SELF-TEST (BIST) AND OUTPUT TEST

The AD9640 includes built-in test features to enable verification of the integrity of each channel as well as to facilitate board level debugging. A built-in self-test (BIST) feature is included that verifies the integrity of the digital data path of the AD9640. Various output test options are also provided to place predictable values on the outputs of the AD9640.

BUILT-IN SELF-TEST (BIST)

The BIST is a thorough test of the digital portion of the selected AD9640 signal path. When enabled, the test runs from an internal PN source through the digital data path starting at the ADC block output. The BIST sequence runs for 512 cycles and stops. The BIST signature value for Channel A or Channel B is placed in Register 0x024 and Register 0x025. If one channel is chosen, its BIST signature is written to the two registers. If both channels are chosen, the results from the A channel are placed in the BIST signature register.

The outputs are not disconnected during this test, so the PN sequence can be observed as it runs. The PN sequence can be continued from its last value or started from the beginning, based on the value programmed in Register 0x00E, Bit 2. The BIST signature result varies based on the channel configuration.

OUTPUT TEST MODES

The output test options are shown in Table 25. When an output test mode is enabled, the analog section of the ADC is disconnected from the digital backend blocks and the test pattern is run through the output formatting block. Some of the test patterns are subject to output formatting and some are not. The seed value for the PN sequence tests can be forced if the PN reset bits are used to hold the generator in reset mode by setting Bit 4 or Bit 5 of Register 0x0D. These tests can be performed with or without an analog signal (if present, the analog signal is ignored), but they do require an encode clock. For more information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CHANNEL/CHIP SYNCHRONIZATION

The AD9640 has a SYNC input that allows the user flexible synchronization options for synchronizing the internal blocks. The clock divider sync feature is useful to guarantee synchronized sample clocks across multiple ADCs. The signal monitor block can also be synchronized using the SYNC input allowing properties of the input signal to be measured during a specific time period. The input clock divider can be enabled to synchronize on a single occurrence of the sync signal or on every occurrence. The signal monitor block is synchronized on every SYNC input signal.

The SYNC input is internally synchronized to the sample clock; however, to ensure there is no timing uncertainty between multiple parts, the SYNC input signal should be externally synchronized to the input clock signal, meeting the setup and hold times shown in Table 8. The SYNC input should be driven using a single-ended CMOS-type signal.

SERIAL PORT INTERFACE (SPI)

The AD9640 serial port interface (SPI) allows the user to configure the converter for specific functions or operations through a structured register space provided inside the ADC. This gives the user added flexibility and customization depending on the application. Addresses are accessed via the serial port and can be written to or read from via the port. Memory is organized into bytes that can be further divided into fields, which are documented in the Memory Map section. For detailed operational information, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

CONFIGURATION USING THE SPI

There are three pins that define the SPI of this ADC. They are the SCLK/DFS pin, the SDIO/DCS pin, and the CSB pin (see Table 22). The SCLK/DFS (a serial clock) is used to synchronize the read and write data presented from and to the ADC. The SDIO/DCS (serial data input/output) is a dual-purpose pin that allows data to be sent and read from the internal ADC memory map registers. The CSB (chip select bar) is an active-low control that enables or disables the read and write cycles.

Table 22. Serial Port Interface Pins

Pin	Function
SCLK	Serial Clock. The serial shift clock input. SCLK is used to synchronize serial interface reads and writes.
SDIO	Serial Data Input/Output. A dual-purpose pin. The typical role for this pin is an input and output depending on the instruction being sent and the relative position in the timing frame.
CSB	Chip Select Bar. An active-low control that gates the read and write cycles.

The falling edge of the CSB, in conjunction with the rising edge of the SCLK, determines the start of the framing. An example of the serial timing and its definitions can be found in Figure 73 and Table 8.

Other modes involving the CSB are available. The CSB can be held low indefinitely, which permanently enables the device; this is called streaming. The CSB may stall high between bytes to allow for additional external timing. When CSB is tied high, SPI functions are placed in high impedance mode. This mode turns on any SPI pin secondary functions.

During an instruction phase, a 16-bit instruction is transmitted. Data follows the instruction phase, and its length is determined by the W0 and W1 bits. All data is composed of 8-bit words. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. This allows the serial data input/output (SDIO) pin to change direction from an input to an output.

In addition to word length, the instruction phase determines if the serial frame is a read or write operation, allowing the serial port to be used to both program the chip as well as read the contents of the on-chip memory. If the instruction is a readback operation, performing a readback causes the serial data input/output (SDIO) pin to change direction from an input to an output at the appropriate point in the serial frame.

Data can be sent in MSB first mode or LSB first mode. MSB first is the default on power-up and can be changed via the configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

HARDWARE INTERFACE

The pins described in Table 22 comprise the physical interface between the user's programming device and the serial port of the AD9640. The SCLK pin and the CSB pin function as inputs when using the SPI interface. The SDIO pin is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface Boot Circuit*.

The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK signal, the CSB signal, and the SDIO signal are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is utilized for other devices, it may be necessary to provide buffers between this bus and the AD9640 to keep these signals from transitioning at the converter inputs during critical sampling periods.

Some pins serve a dual function when the SPI interface is not being used. When the pins are strapped to AVDD or ground during device power-on, they are associated with a specific function. The Digital Outputs section describes the strappable functions supported on the AD9640.

CONFIGURATION WITHOUT THE SPI

In applications that do not interface to the SPI control registers, the SDIO/DCS pin, the SCLK/DFS pin, the SMI SDO/OEB pin, and the SMI SCLK/PDWN pin serve as standalone, CMOS-compatible control pins. When the device is powered up, it is assumed that the user intends to use the pins as static control lines for the duty cycle stabilizer, output data format, output enable, and power-down feature control. In this mode, the CSB chip select should be connected to AVDD, which disables the serial port interface.

Table 23. Mode Selection

Pin	External Voltage	Configuration
SDIO/DCS	AVDD (default)	Duty cycle stabilizer enabled.
	AGND	Duty cycle stabilizer disabled.
SCLK/DFS	AVDD	Twos complement enabled.
	AGND (default)	Offset binary enabled.
SMI SDO/OEB	AVDD	Outputs in high impedance.
	AGND (default)	Outputs enabled.
SMI SCLK/PDWN	AVDD	Chip in power-down or standby.
	AGND (default)	Normal operation.

SPI ACCESSIBLE FEATURES

A brief description of general features accessible via the SPI follows. These features are described in detail in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. The AD9640 part-specific features are described in detail following Table 25, the external memory map register table.

Table 24. Features Accessible Using the SPI

Feature Name	Description
Modes	Allows user to set either power-down mode or standby mode.
Clock	Allows user to access the DCS via the SPI.
Offset	Allows user to digitally adjust the converter offset.
Test I/O	Allows user to set test modes to have known data on output bits.
Output Mode	Allows user to set up outputs.
Output Phase	Allows user to set the output clock polarity.
Output Delay	Allows user to vary the DCO delay.
VREF	Allows user to set the reference voltage.

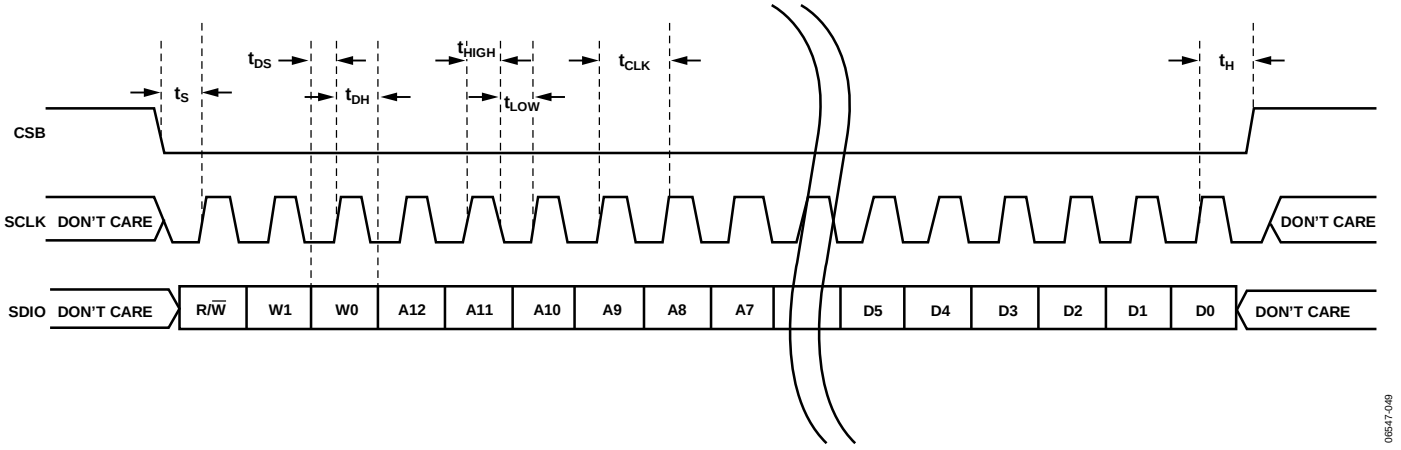


Figure 73. Serial Port Interface Timing Diagram

MEMORY MAP

READING THE MEMORY MAP TABLE

Each row in the memory map table has eight bit locations. The memory map is roughly divided into four sections: chip configuration and ID register map (Address 0x00 to Address 0x02); ADC setup, control, and test (Address 0x08 to Address 0x25); the channel index and transfer register map (Address 0x05 to Address 0xFF); and digital feature control (Address 0x100 to Address 0x11B).

Starting from the right hand column, the memory map register in Table 25 documents the default hex value for each hex address shown. The column with the heading Bit 7 (MSB) is the start of the default hex value given. For example, Address 0x18, VREF select, has a hex default value of 0xC0. This means Bit 7 = 1, Bit 6 = 1, and the remaining bits are 0s. This setting is the default reference selection setting. The default value uses a 2.0 V peak-to-peak reference. For more information on this function and others, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This document details the functions controlled by Register 0x00 to Register 0xFF. The remaining registers, from Register 0x100 to Register 0x11B, are documented in the Memory Map Register Description section.

Open Locations

All address and bit locations that are not included in Table 25 are currently not supported for this device. Unused bits of a valid address location should be written with 0s. Writing to these locations is required only when part of an address location is open (for example, Address 0x18). If the entire address location is open (for example, Address 0x13), this address location should not be written.

Default Values

Coming out of reset, critical registers are loaded with default values. The default values for the registers are given in the memory map register table, Table 25.

Logic Levels

An explanation of logic level terminology follows:

- "Bit is set" is synonymous with "Bit is set to Logic 1" or "Writing Logic 1 for the bit."
- "Clear a bit" is synonymous with "Bit is set to Logic 0" or "Writing Logic 0 for the bit."

Transfer Register Map

Address 0x08 to Address 0x18 are shadowed. Writes to these addresses do not affect part operation until a transfer command is issued by writing 0x01 to Address 0xFF, setting the transfer bit. This allows these registers to be updated internally and simultaneously when the transfer bit is set. The internal update takes place when the transfer bit is set, and the bit autoclears.

Channel-Specific Registers

Some channel setup functions, such as the signal monitor thresholds, can be programmed differently for each channel. In these cases, channel address locations are internally duplicated for each channel. These registers are designated in the parameter name column of Table 25 as local registers. These local registers can be accessed by setting the appropriate Channel A or Channel B bits in Register 0x05. If both bits are set, the subsequent write affects the registers of both channels. In a read cycle, only Channel A or Channel B should be set to read one of the two registers. If both bits are set during an SPI read cycle, the part returns the value for Channel A. Registers designated as global in the parameter name column of Table 25 affect the entire part or the channel features where independent settings are not allowed between the channels. The settings in Register 0x05 do not affect the global registers.

EXTERNAL MEMORY MAP

Table 25. Memory Map Registers

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
Chip Configuration Registers											
0x00	SPI Port Configuration (Global)	0	LSB first	Soft reset	1	1	Soft reset	LSB first	0	0x18	The nibbles are mirrored so that LSB-first mode or MSB-first mode registers correctly, regardless of shift mode
0x01	Chip ID (Global)	8-bit Chip ID[7:0] (AD9640 = 0x11) (default)								0x11 Read only	Read only
0x02	Chip Grade (Global)	Open	Open	Speed grade ID 00 = 150 MSPS 01 = 125 MSPS 10 = 105 MSPS 11 = 80 MSPS		Open	Open	Open	Open	Read only	Speed grade ID used to differentiate devices
Channel Index and Transfer Registers											
0x05	Channel Index	Open	Open	Open	Open	Open	Open	Data Channel B (default)	Data Channel A (default)	0x03	Bits are set to determine which device on the chip receives the next write command; applies to local registers
0xFF	Device Update	Open	Open	Open	Open	Open	Open	Open	Transfer	0x00	Synchronously transfers data from the master shift register to the slave
ADC Functions											
0x08	Power Modes	Open	Open	External power-down pin function (global) 0 = pdwn 1 = stndby	Open	Open	Open	Internal power-down mode (local) 00 = normal operation 01 = full power-down 10 = standby 11 = normal operation		0x00	Determines various generic modes of chip operation
0x09	Global Clock (Global)	Open	Open	Open	Open	Open	Open	Open	Duty cycle stabilizer (default)	0x01	
0x0B	Clock Divide (Global)	Open	Open	Open	Open	Open	Clock divide ratio 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Clock divide values other than 000 automatically cause the duty cycle stabilizer to become active
0x0D	Test Mode (Local)	Open	Open	Reset PN long gen	Reset PNshort gen	Open	Output test mode 000 = off (default) 001 = midscale short 010 = positive FS 011 = negative FS 100 = alternating checker board 101 = PN long sequence 110 = PN short sequence 111 = one/zero word toggle			0x00	When set, the test data is placed on the output pins in place of normal data

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x0E	BIST Enable (Local)	Open	Open	Open	Open	Open	Reset BIST sequence	Open	BIST enable	0x00	
0x10	Offset Adjust (Local)	Open	Open	Offset adjust in LSBs from +31 to −32 (twos complement format)						0x00	
0x14	Output Mode	Drive strength 0 V to 3.3 V CMOS or ANSI LVDS: 1 V to 1.8 V CMOS or reduced: LVDS (global)	Output type 0 = CMOS 1 = LVDS (global)	Open	Output enable bar (local)	Open	Output invert (local)	00 = offset binary 01 = twos complement 01 = gray code 11 = offset binary (local)		0x00	Configures the outputs and the format of the data
0x16	Clock Phase Control (Global)	Invert DCO clock	Open	Open	Open	Open	Input clock divider phase adjust 000 = no delay 001 = 1 input clock cycle 010 = 2 input clock cycles 011 = 3 input clock cycles 100 = 4 input clock cycles 101 = 5 input clock cycles 110 = 6 input clock cycles			0x00	Allows selection of clock delays into the input clock divider
0x17	DCO Output Delay (Global)	Open	Open	Open	DCO clock delay (delay = 2500 ps × register value/31) 00000 = 0 ps 00001 = 81 ps 00010 = 161 ps … 11110 = 2419 ps 11111 = 2500 ps					0x00	
0x18	VREF Select (Global)	Reference voltage selection 00 = 1.25 V p-p 01 = 1.5 V p-p 10 = 1.75 V p-p 11 = 2.0 V p-p (default)		Open	Open	Open	Open	Open	Open	0xC0	
0x24	BIST Signature LSB (Local)	BIST signature[7:0]								0x00	Read only
0x25	BIST Signature MSB (Local)	BIST signature[15:8]								0x00	Read only
Digital Feature Control											
0x100	Sync Control (Global)	SM sync enable	Open	Open	Open	Open	Clock divider next sync only	Clock divider sync enable	Master sync enable	0x00	
0x104	Fast Detect Control (Local)	Open	Open	Open	Open	Fast Detect Mode Select[2:0]			Fast detect enable	0x00	
0x106	Fine Upper Threshold Register 0 (Local)	Fine Upper Threshold[7:0]								0x00	
0x107	Fine Upper Threshold Register 1 (Local)	Open	Open	Open	Fine Upper Threshold[12:8]					0x00	
0x108	Fine Lower Threshold Register 0 (Local)	Fine Lower Threshold[7:0]								0x00	
0x109	Fine Lower Threshold Register 1 (Local)	Open	Open	Open	Fine Lower Threshold[12:8]					0x00	

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x10C	Signal Monitor DC Correction Control (Global)	Open	DC correction freeze	DC Correction Bandwidth[3:0]				DC correction for signal path enable	DC correction for SM enable	0x00	
0x10D	Signal Monitor DC Value Channel A Register 0 (Global)	DC Value Channel A[7:0]									Read only
0x10E	Signal Monitor DC Value Channel A Register 1 (Global)	Open	Open	DC Value Channel A[13:8]							Read only
0x10F	Signal Monitor DC Value Channel B Register 0 (Global)	DC Value Channel B[7:0]									Read only
0x110	Signal Monitor DC Value Channel B Register 1 (Global)	Open	Open	DC Value Channel B[13:8]							Read only
0x111	Signal Monitor SPORT Control (Global)	Open	RMS/MS magnitude output enable	Peak power output enable	Threshold crossing output enable	SPORT SMI CLK divide 00 = undefined 01 = divide by 2 10 = divide by 4 11 = divide by 8		SPORT SMI SCLK sleep	Signal monitor SPORT output enable	0x04	
0x112	Signal Monitor Control (Global)	Complex power calculation mode enable	Open	Open	Open	MS mode 0 = rms 1 = ms	Signal monitor mode 00 = RMS/MS Magnitude 01 = peak power 1x = threshold count		Signal monitor enable	0x00	
0x113	Signal Monitor Period Register 0 (Global)	Signal Monitor Period[7:0]								0x40	In ADC clock cycles
0x114	Signal Monitor Period Register 1 (Global)	Signal Monitor Period[15:8]								0x00	In ADC clock cycles
0x115	Signal Monitor Period Register 2 (Global)	Signal Monitor Period[23:16]								0x00	In ADC clock cycles
0x116	Signal Monitor Result Channel A Register 0 (Global)	Signal Monitor Result Channel A[7:0]									Read only
0x117	Signal Monitor Result Channel A Register 1 (Global)	Signal Monitor Result Channel A[15:8]									Read only
0x118	Signal Monitor Result Channel A Register 2 (Global)	Open	Open	Open	Open	Signal Monitor Value Channel A[19:16]					Read only
0x119	Signal Monitor Result Channel B Register 0 (Global)	Signal Monitor Result Channel B[7:0]									Read only

Addr (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Default Notes/ Comments
0x11A	Signal Monitor Result Channel B Register 1 (Global)	Signal Monitor Result Channel B[15:8]									Read only
0x11B	Signal Monitor Result Channel B Register 2 (Global)	Open	Open	Open	Open	Signal Monitor Result Channel B[19:16]					Read only

MEMORY MAP REGISTER DESCRIPTION

For additional information about functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Sync Control (Register 0x100)

Bit 7—Signal Monitor Sync Enable

Bit 7 enables the sync pulse from the external SYNC input to the signal monitor block. The sync signal is passed when Bit 7 is high and Bit 0 is high. This is continuous sync mode.

Bits[6:3]—Reserved

Bit 2—Clock Divider Next Sync Only

If the sync enable bit (Address 0x100[0]) is high and the clock divider sync enable (Address 0x100[1]) is high, Bit 2 allows the clock divider to sync to the first sync pulse it receives and ignore the rest. Address 0x100[1] resets after it syncs.

Bit 1—Clock Divider Sync Enable

Bit 1 gates the sync pulse to the clock divider. The sync signal is passed when Bit 1 is high and Bit 0 is high. This is continuous sync mode.

Bit 0—Master Sync Enable

Bit 0 must be high to enable any of the sync functions.

Fast Detect Control (Register 0x104)

Bits[7:4]—Reserved

Bits[3:1]—Fast Detect Mode Select

These bits set the mode of the fast detect output bits according to Table 17.

Bit 0—Fast Detect Enable

Bit 0 is used to enable the fast detect bits. When the fast detect outputs are disabled, the outputs go into a high impedance state. In LVDS mode, when the outputs are interleaved, the outputs go high-Z only if both channels are turned off (power-down/standby/output disabled). If only one channel is turned off (power-down/standby/output disabled), the fast detect outputs repeat the data of the active channel.

Fine Upper Threshold (Register 0x106 and Register 0x107)

Register 0x106, Bits[7:0]—Fine Upper Threshold[7:0]

Register 0x107, Bits[7:5]—Reserved

Register 0x107, Bits[4:0]—Fine Upper Threshold[12:8]

These registers provide the fine upper limit threshold. This 13-bit value is compared to the 13-bit magnitude from the ADC block and, if the ADC magnitude exceeds this threshold value, the F_UT flag is set.

Fine Lower Threshold (Register 0x108 and Register 0x109)

Register 0x108, Bits[7:0]—Fine Lower Threshold[7:0]
Register 0x109, Bits[7:5]—Reserved
Register 0x109, Bits[4:0]—Fine Lower Threshold[12:8]

These registers provide a fine lower limit threshold. This 13-bit value is compared to the 13-bit magnitude from the ADC block and, if the ADC magnitude is less than this threshold value, the F_LT flag is set.

Signal Monitor DC Correction Control (Register 0x10C)

Bit 7—Reserved
Bit 6—DC Correction Freeze

When Bit 6 is set high, the dc correction is no longer updated to the signal monitoring block. It holds the last dc value it calculated.

Bits[5:2]—DC Correction Bandwidth

These bits set the averaging time of the signal monitor dc correction function. It is a 4-bit word that sets the bandwidth of the correction block (see Table 26).

Table 26. DC Correction Bandwidth

DC Correction Control Register 0x10C[5:2]	Bandwidth (Hz)
0000	1218.56
0001	609.28
0010	304.64
0011	152.32
0100	76.16
0101	38.08
0110	19.04
0111	9.52
1000	4.76
1001	2.38
1010	1.19
1011	0.60
1100	0.30
1101	0.15
1110	0.15
1111	0.15

Bit 1—DC Correction for Signal Path Enable

Setting Bit 1 high causes the output of the dc measurement block to be summed with the data in the signal path to remove the dc offset from the signal path.

Bit 0—DC Correction for SM Enable

Bit 0 enables the dc correction function in the signal monitoring block. The dc correction is an averaging function that can be used by the signal monitor to remove dc offset in the signal. Removing this dc from the measurement allows a more accurate reading.

Signal Monitor DC Value Channel A (Register 0x10D and Register 0x10E)

Register 0x10D, Bits[7:0]—Channel A DC Value[7:0]

Register 0x10E, Bits[7:0]—Channel A DC Value[13:8]

These read-only registers hold the latest dc offset value computed by the signal monitor for Channel A.

Signal Monitor DC Value Channel B (Register 0x10F and Register 0x110)

Register 0x10F Bits[7:0]—Channel B DC Value[7:0]

Register 0x110 Bits[7:0]—Channel B DC Value[13:8]

These read-only registers hold the latest dc offset value computed by the signal monitor for Channel B.

Signal Monitor SPORT Control (Register 0x111)

Bit 7—Reserved

Bit 6—RMS/MS Magnitude Output Enable

These bits enable the 20-bit rms or ms magnitude measurement as output on the SPORT.

Bit 5—Peak Power Output Enable

Bit 5 enables the 13-bit peak measurement as output on the SPORT.

Bit 4—Threshold Crossing Output Enable

Bit 4 enables the 13-bit threshold measurement as output on the SPORT.

Bits[3:2]—SPORT SMI SCLK Divide

The values of these bits set the SPORT SMI SCLK divide ratio from the input clock. A value of 0x01 sets divide by 2 (default), a value of 0x10 sets divide by 4, and a value of 0x11 sets divide by 8.

Bit 1— SPORT SMI SCLK Sleep

Setting Bit 1 high causes the SMI SCLK to remain low when the signal monitor block has no data to transfer.

Bit 0—Signal Monitor SPORT Output Enable

When set, Bit 0 enables the SPORT output of the signal monitor to begin shifting out the result data from the signal monitor block.

Signal Monitor Control (Register 0x112)

Bit 7—Complex Power Calculation Mode Enable

This mode assumes I data is present on one channel and Q data is present on the opposite channel. The result reported is the complex power, measured as

$$\sqrt{I^2 + Q^2}$$

Bits[6:4]—Reserved

Bit 3—Signal Monitor RMS/MS Select

Setting Bit 3 low selects rms power measurement mode. Setting Bit 3 high selects ms power measurement mode.

Bits[2:1]—Signal Monitor Mode

Bit 2 and Bit 1 set the mode of the signal monitor for data output to Register 0x116 to Register 0x11B. Setting Bit 2 and Bit 1 to 0x00 selects rms/ms power output; setting these bits to 0x01 selects peak power output; and setting 0x10 or 0x11 selects threshold crossing output.

Bit 0—Signal Monitor Enable

Setting Bit 0 high enables the signal monitor block.

Signal Monitor Period (Register 0x113 to Register 0x115)

Register 0x113, Bits[7:0]—Signal Monitor Period[7:0]

Register 0x114, Bits[7:0]—Signal Monitor Period[15:8]

Register 0x115, Bits[7:0]—Signal Monitor Period[23:16]

This 24-bit value sets the number of clock cycles over which the signal monitor performs its operation. Although this register defaults to 64 (0x40), the minimum value for this register is 128 (0x80) cycles – writing values less than 128 can cause inaccurate results.

Signal Monitor Result Channel A (Register 0x116 to Register 0x118)

Register 0x116, Bits[7:0]—Signal Monitor Result Channel A[7:0]

Register 0x117, Bits[7:0]—Signal Monitor Result Channel A[15:8]

Register 0x118, Bits[7:4]—Reserved

Register 0x118, Bits[3:0]—Signal Monitor Result Channel A[19:16]

This 20-bit value contains the result calculated by the signal monitoring block for Channel A. The content is dependent on the settings in Register 0x112[2:1].

Signal Monitor Result Channel B (Register 0x119 to Register 0x11B)

Register 0x119, Bits[7:0]— Signal Monitor Result Channel B[7:0]

Register 0x11A, Bits[7:0]—Signal Monitor Result Channel B[15:8]

Register 0x11B, Bits[7:4]—Reserved

Register 0x11B, Bits[3:0]—Signal Monitor Result Channel B[19:16]

This 20-bit value contains the result calculated by the signal monitoring block for Channel B. The content is dependent on the settings in Register 0x112[2:1].

APPLICATIONS INFORMATION

DESIGN GUIDELINES

Before starting design and layout of the AD9640 as a system, it is recommended that the designer become familiar with these guidelines, which discuss the special circuit connections and layout requirements needed for certain pins.

Power and Ground Recommendations

When connecting power to the AD9640, it is recommended that two separate 1.8 V supplies be used: one supply should be used for analog (AVDD) and digital (DVDD), and a separate supply should be used for the digital outputs (DRVDD). The AVDD and DVDD supplies, while derived from the same source, should be isolated with a ferrite bead or filter choke and separate decoupling capacitors. The user can employ several different decoupling capacitors to cover both high and low frequencies. These should be located close to the point of entry at the PC board level and close to the part's pins with minimal trace length.

A single PCB ground plane should be sufficient when using the AD9640. With proper decoupling and smart partitioning of the PCB analog, digital, and clock sections, optimum performance is easily achieved.

LVDS Operation

The AD9640 defaults to CMOS output mode on power-up. If LVDS operation is desired, this mode must be programmed using the SPI configuration registers after power-up. When the AD9640 powers up in CMOS mode with LVDS termination resistors (100 Ω) on the outputs, the DRVDD current may be higher than the typical value until the part is placed in LVDS mode. This additional DRVDD current does not cause damage to the AD9640, but it should be taken into account when considering the maximum DRVDD current for the part.

To avoid this additional DRVDD current, the AD9640 outputs can be disabled at power-up by taking the OEB pin high. After the part is placed into LVDS mode via the SPI port, the OEB pin can be taken low to enable the outputs.

Exposed Paddle Thermal Heat Slug Recommendations

It is mandatory that the exposed paddle on the underside of the ADC be connected to analog ground (AGND) to achieve the best electrical and thermal performance. A continuous, exposed (no solder mask), copper plane on the PCB should mate to the AD9640 exposed paddle, Pin 0.

The copper plane should have several vias to achieve the lowest possible resistive thermal path for heat dissipation to flow through the bottom of the PCB. These vias should be filled or plugged with nonconductive epoxy.

To maximize the coverage and adhesion between the ADC and PCB, a silkscreen should be overlaid to partition the continuous plane on the PCB into several uniform sections. This provides several tie points between the two during the reflow process. Using one continuous plane with no partitions guarantees only one tie point between the ADC and PCB. See the evaluation board for a PCB layout example. For detailed information about packaging and PCB layout of chip scale packages, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

CML

The CML pin should be decoupled to ground with a 0.1 µF capacitor, as shown in Figure 47.

RBIAS

The AD9640 requires that a 10 kΩ resistor be placed between the RBIAS pin and ground. This resistor sets the master current reference of the ADC core and should have at least a 1% tolerance.

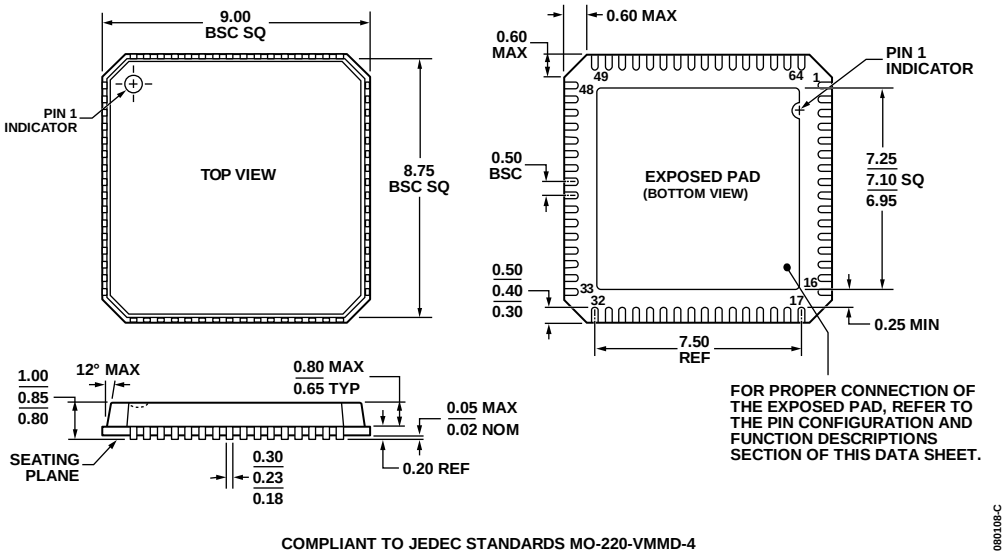
Reference Decoupling

The VREF pin should be externally decoupled to ground with a low ESR 1.0 µF capacitor in parallel with a 0.1 µF ceramic, low ESR capacitor.

SPI Port

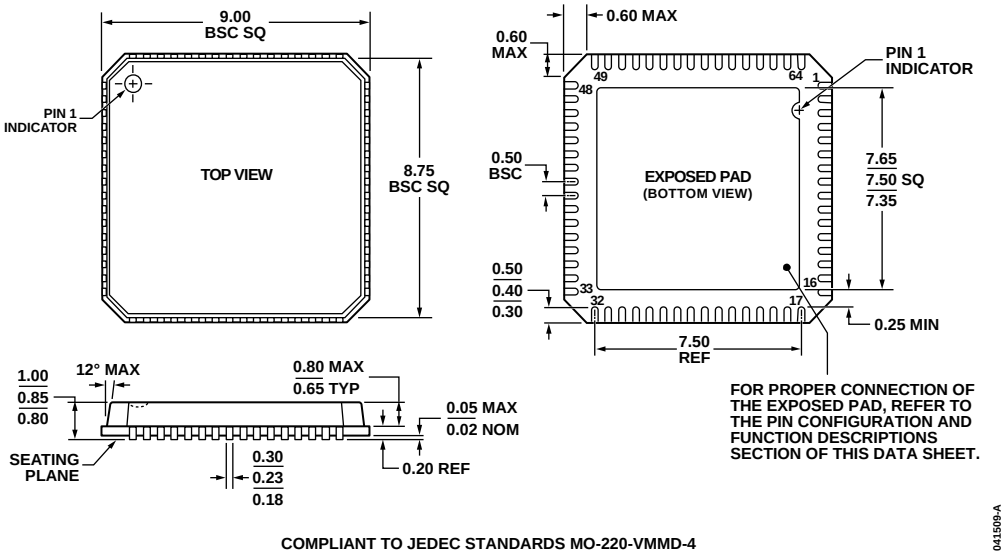
The SPI port should not be active during periods when the full dynamic performance of the converter is required. Because the SCLK, CSB, and SDIO signals are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the AD9640 to keep these signals from transitioning at the converter inputs during critical sampling periods.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 74. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4

Figure 75. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-6)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9640ABCPZ-150[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9640ABCPZ-125[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9640ABCPZ-105[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9640ABCPZ-80[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9640ABCPZRL7-80[1, 2]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-6
AD9640BCPZ-150[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-125[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-105[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640BCPZ-80[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-3
AD9640-150EBZ[1]		Evaluation Board	
AD9640-125EBZ[1]		Evaluation Board	
AD9640-105EBZ[1]		Evaluation Board	
AD9640-80EBZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.
[2] Recommended for use in new designs; reference PCN 09_0156.

NOTES

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