



**THE DATASHEET OF
MC74LVX139DR2G**



MC74LVX139

Dual 2-to-4 Decoder/ Demultiplexer

The MC74LVX139 is an advanced high speed CMOS 2-to-4 decoder/demultiplexer fabricated with silicon gate CMOS technology.

When the device is enabled (\bar{E} = low), it can be used for gating or as a data input for demultiplexing operations. When the enable input is held high, all four outputs are fixed high, independent of other inputs.

The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

Features

- High Speed: $t_{PD} = 6.0$ ns (Typ) at $V_{CC} = 3.3$ V
- Low Power Dissipation: $I_{CC} = 4$ μ A (Max) at $T_A = 25^\circ$ C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: $V_{OLP} = 0.5$ V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 100 FETs or 25 Equivalent Gates
- ESD Performance:
 - Human Body Model > 2000 V;
 - Machine Model > 200 V
- These Devices are Pb-Free and are RoHS Compliant

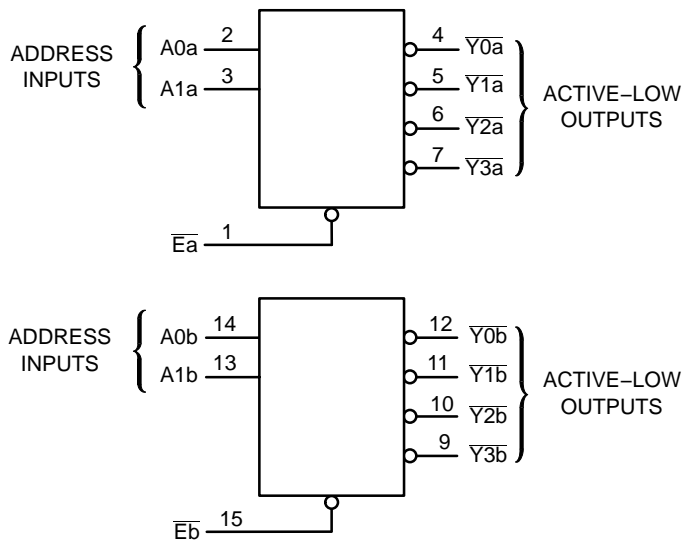
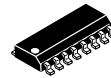


Figure 1. Logic Diagram



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SOIC-16
D SUFFIX
CASE 751B

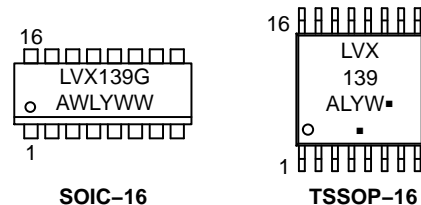


TSSOP-16
DT SUFFIX
CASE 948F

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-16

TSSOP-16

LVX139 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

| Inputs | | | Outputs | | | |
|--------|----|----|---------|----|----|----|
| E | A1 | A0 | Y0 | Y1 | Y2 | Y3 |
| H | X | X | H | H | H | H |
| L | L | L | L | H | H | H |
| L | L | H | H | L | H | H |
| L | H | L | H | H | L | H |
| L | H | H | H | H | H | L |

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

MC74LVX139

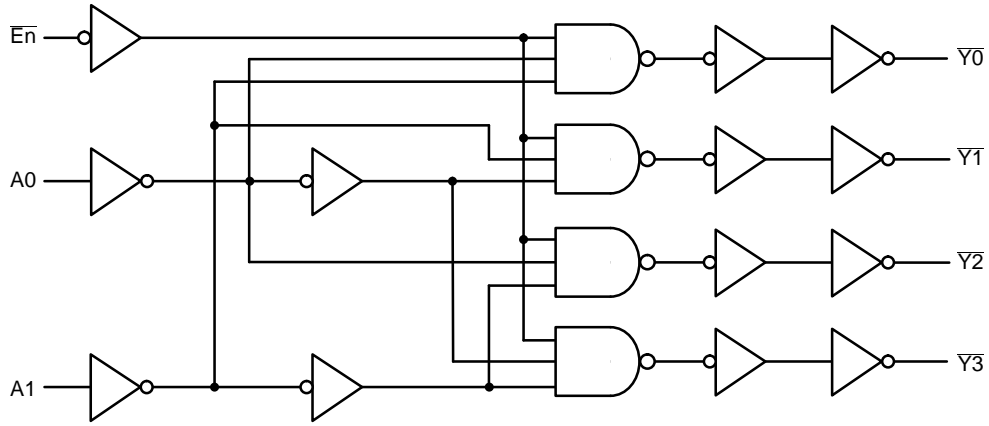


Figure 2. Expanded Logic Diagram
(1/2 of Device)

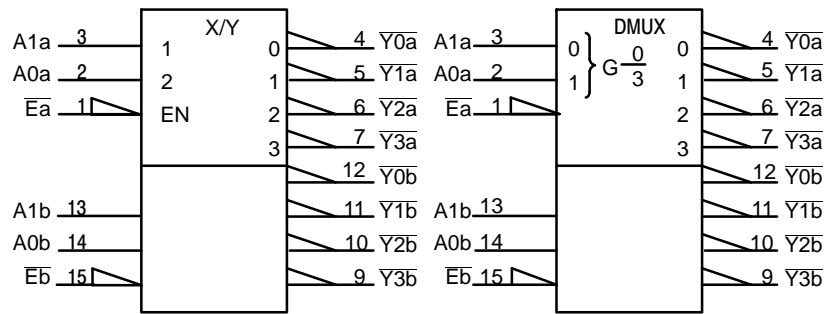


Figure 3. IEC Logic Diagram

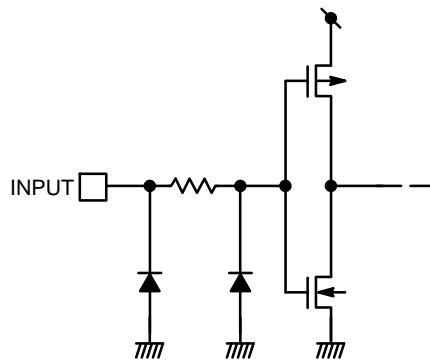


Figure 4. Input Equivalent Circuit

MC74LVX139

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|----------------------|-------------------------------------------------|-------------------------------------------------------------------------------------------------------------------|------------|
| V _{CC} | Positive DC Supply Voltage | -0.5 to +7.0 | V |
| V _{IN} | Digital Input Voltage | -0.5 to +7.0 | V |
| V _{OUT} | DC Output Voltage | -0.5 to V _{CC} +0.5 | V |
| I _{IK} | Input Diode Current | -20 | mA |
| I _{OK} | Output Diode Current | ±20 | mA |
| I _{OUT} | DC Output Current, per Pin | ±25 | mA |
| I _{CC} | DC Supply Current, V _{CC} and GND Pins | ±75 | mA |
| P _D | Power Dissipation in Still Air | SOIC Package 200 TSSOP 180 | mW |
| T _{STG} | Storage Temperature Range | -65 to +150 | °C |
| V _{ESD} | ESD Withstand Voltage | Human Body Model (Note 1) > 2000 Machine Model (Note 2) > 200 Charged Device Model (Note 3) > 2000 | V |
| I _{LATCHUP} | Latchup Performance | Above V _{CC} and Below GND at 125°C (Note 4) | ±300 mA |
| θ _{JA} | Thermal Resistance, Junction-to-Ambient | SOIC Package 143 TSSOP 164 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A
2. Tested to EIA/JESD22-A115-A
3. Tested to JESD22-C101-A
4. Tested to EIA/JESD78

RECOMMENDED OPERATING CONDITIONS

| Symbol | Characteristics | Min | Max | Unit |
|---------------------------------|------------------------------------------------|-----|-----------------|------|
| V _{CC} | DC Supply Voltage | 2.0 | 3.6 | V |
| V _{IN} | DC Input Voltage | 0 | 5.5 | V |
| V _{OUT} | DC Output Voltage | 0 | V _{CC} | V |
| | Output in 3-State High or Low State | | | |
| T _A | Operating Temperature Range, all Package Types | -40 | 85 | °C |
| t _r , t _f | Input Rise or Fall Time | 0 | 100 | ns/V |
| | V _{CC} = 5.0 V ± 0.5 V | | | |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

MC74LVX139

DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | V _{CC} (V) | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | Unit |
|-----------------|------------------------------------------------|------------------------------------------|------------------------|-----------------------|-----|----------------------|-------------------------------|----------------------|------|
| | | | | Min | Typ | Max | Min | Max | |
| V _{IH} | Minimum High-Level Input Voltage | | 2.0 | 0.75 V _{CC} | - | - | 0.75 V _{CC} | - | V |
| | | | 3.0 | 0.7 V _{CC} | - | - | 0.7 V _{CC} | - | |
| | | | 3.6 | 0.7 V _{CC} | - | - | 0.7 V _{CC} | - | |
| V _{IL} | Maximum Low-Level Input Voltage | | 2.0 | - | - | 0.25 V _{CC} | - | 0.25 V _{CC} | V |
| | | | 3.0 | - | - | 0.3 V _{CC} | - | 0.3 V _{CC} | |
| | | | 3.6 | - | - | 0.3 V _{CC} | - | 0.3 V _{CC} | |
| V _{OH} | High-Level Output Voltage | I _{OH} = -50 μA | 2.0 | 1.9 | 2.0 | - | 1.9 | - | V |
| | | I _{OH} = -50 μA | 3.0 | 2.9 | 3.0 | - | 2.9 | - | |
| | | I _{OH} = -4 mA | 3.0 | 2.58 | 3.0 | - | 2.48 | - | |
| V _{OL} | Low-Level Output Voltage | I _{OL} = 50 μA | 2.0 | - | 0.0 | 0.1 | - | 0.1 | V |
| | | I _{OL} = 50 μA | 3.0 | - | - | 0.1 | - | 0.1 | |
| | | I _{OL} = 4 mA | 3.0 | - | - | 0.36 | - | 0.44 | |
| I _{IN} | Input Leakage Current | V _{IN} = 5.5 V or GND | 0 to 3.6 | - | - | ±0.1 | - | ±1.0 | μA |
| I _{CC} | Maximum Quiescent Supply Current (per package) | V _{IN} = V _{CC} or GND | 3.6 | 1.0 | 1.0 | 2.0 | - | - | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS Input t_r = t_f = 3.0 ns

| Symbol | Parameter | Test Conditions | T _A = 25°C | | | -40°C ≤ T _A ≤ 85°C | | Unit |
|----------------------------------------|-------------------------------------------|-----------------------------------------------------------|-----------------------------------------|------|------|-------------------------------|------|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to Y | V _{CC} = 2.7 V C _L = 15 pF | - | 8.5 | 15.0 | 1.0 | 17.8 | ns |
| | | C _L = 50 pF | - | 11.0 | 16.5 | 1.0 | 18.0 | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, \bar{E} to Y | V _{CC} = 3.3 V ± 0.3 V C _L = 15 pF | - | 6.0 | 10.0 | 1.0 | 12.0 | ns |
| | | | C _L = 50 pF | - | 8.5 | 13.0 | 1.0 | |
| | | V _{CC} = 2.7 V C _L = 15 pF | - | 8.0 | 13.0 | 1.0 | 15.5 | |
| | | | C _L = 50 pF | - | 10.0 | 16.5 | 1.0 | |
| C _{IN} | Maximum Input Capacitance | | - | 4 | 10 | - | 10 | pF |
| | | | | | | | | |
| C _{PD} | Power Dissipation Capacitance (Note 5) | | Typical @ 25°C, V _{CC} = 3.3 V | | | | | pF |
| | | | 26 | | | | | |

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per decoder). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

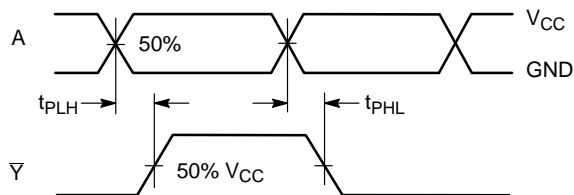


Figure 5. Switching Waveform

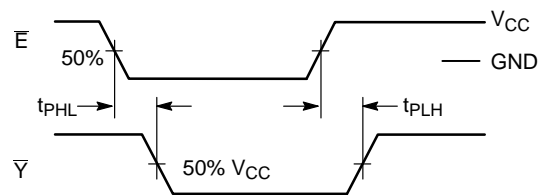
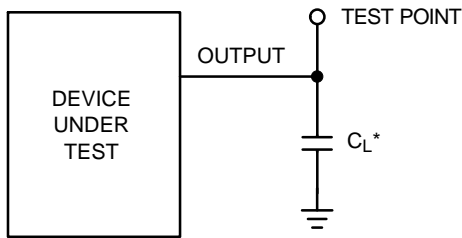


Figure 6. Switching Waveform

MC74LVX139



*Includes all probe and jig capacitance

Figure 7. Test Circuit

ORDERING INFORMATION

| Device | Package | Shipping† |
|-----------------|-----------------------|------------------|
| MC74LVX139DR2G | SOIC-16 (Pb-Free) | 2500 Tape & Reel |
| MC74LVX139DTR2G | TSSOP-16 (Pb-Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

EMBOSSED CARRIER DIMENSIONS (See Notes 6 and 7)

| Tape Size | B ₁ Max | D | D ₁ | E | F | K | P | P ₀ | P ₂ | R | T | W |
|-----------|---------------------|-------------------------------------|---------------------------|---------------------------------------|----------------------------------------|----------------------------|--------------------------------------------------------------------------------------------------------------------------|--------------------------------------|--------------------------------------|------------------|-------------------|---------------------------------------|
| 8 mm | 4.35 mm (0.179") | 1.5 mm + 0.1 -0.0 (0.059") | 1.0 mm Min (0.179") | 1.75 mm ±0.1 (0.069 ±0.004") | 3.5 mm ±0.5 (1.38 ±0.002") | 2.4 mm Max (0.094") | 4.0 mm ±0.10 (0.157 ±0.004") | 4.0 mm ±0.1 (0.157 ±0.004") | 2.0 mm ±0.1 (0.079 ±0.004") | 25 mm (0.98") | 0.6 mm (0.024) | 8.3 mm (0.327) |
| 12 mm | 8.2 mm (0.323") | +0.004 -0.0 | 1.5 mm Min (0.060) | | 5.5 mm ±0.5 (0.217 ±0.002") | 6.4 mm Max (0.252") | 4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") | | | 30 mm (1.18") | | 12.0 mm ±0.3 (0.470 ±0.012") |
| 16 mm | 12.1 mm (0.476") | | | | 7.5 mm ±0.10 (0.295 ±0.004") | 7.9 mm Max (0.311") | 4.0 mm ±0.10 (0.157 ±0.004") 8.0 mm ±0.10 (0.315 ±0.004") 12.0 mm ±0.10 (0.472 ±0.004") | | | | | 16.3 mm (0.642) |
| 24 mm | 20.1 mm (0.791") | | | | 11.5 mm ±0.10 (0.453 ±0.004") | 11.9 mm Max (0.468") | 16.0 mm ±0.10 (0.63 ±0.004") | | | | | 24.3 mm (0.957) |

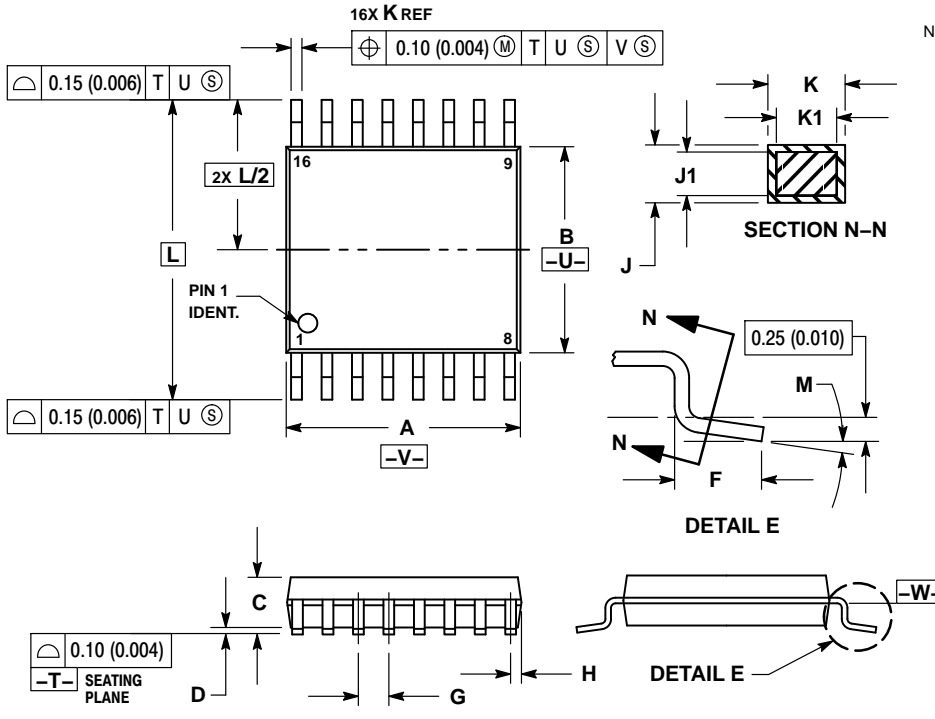
6. Metric Dimensions Govern-English are in parentheses for reference only.

7. A₀, B₀, and K₀ are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min to 0.50 mm max. The component cannot rotate more than 10° within the determined cavity

MC74LVX139

PACKAGE DIMENSIONS

TSSOP-16
CASE 948F
ISSUE B

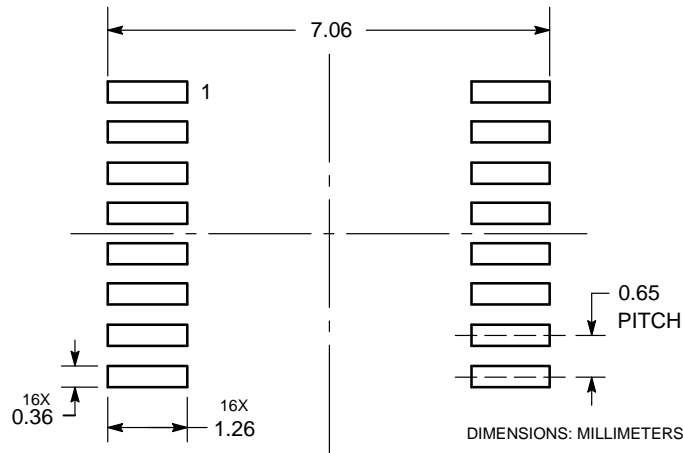


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

SOLDERING FOOTPRINT*

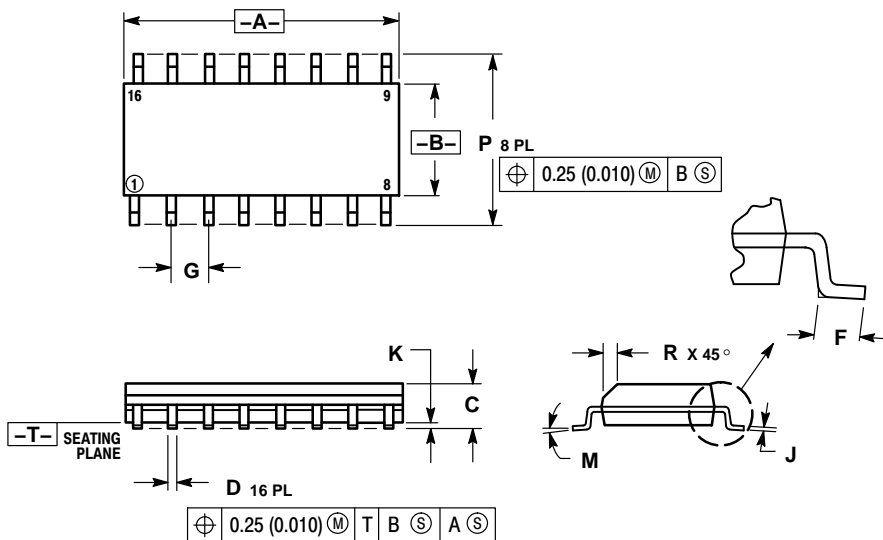


*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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PACKAGE DIMENSIONS

SOIC-16
CASE 751B-05
ISSUE K

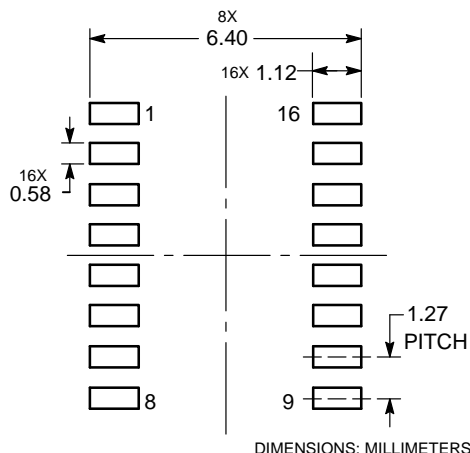


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| MILLIMETERS | | INCHES | | |
|-------------|----------|--------|-----------|-------|
| DIM | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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