THE DATASHEET OF

LTC2756BCG#PBF

Serial 18-Bit SoftSpan I_{OUT} DAC

FEATURES

- **Maximum 18-Bit INL Error: ±1 LSB Over Temperature**
- **Program or Pin-Strap Six Output Ranges: 0V to 5V, 0V to 10V, –2.5V to 7.5V, ±2.5V, ±5V, ±10V**
- **Guaranteed Monotonic Over Temperature**
- **Glitch Impulse 0.4nV•s (3V), 2nV•s (5V)**
- **18-Bit Settling Time: 2.1µs**
- 2.7V to 5.5V Single Supply Operation
- Reference Current Constant for All Codes
- Voltage-Controlled Offset and Gain Trims
- Serial Interface with Readback of All Registers
- Clear and Power-On-Reset to 0V Regardless of Output Range
- 28-Pin SSOP Package

APPLICATIONS

- Instrumentation
- Medical Devices
- Automatic Test Equipment
- Process Control and Industrial Automation

DESCRIPTION

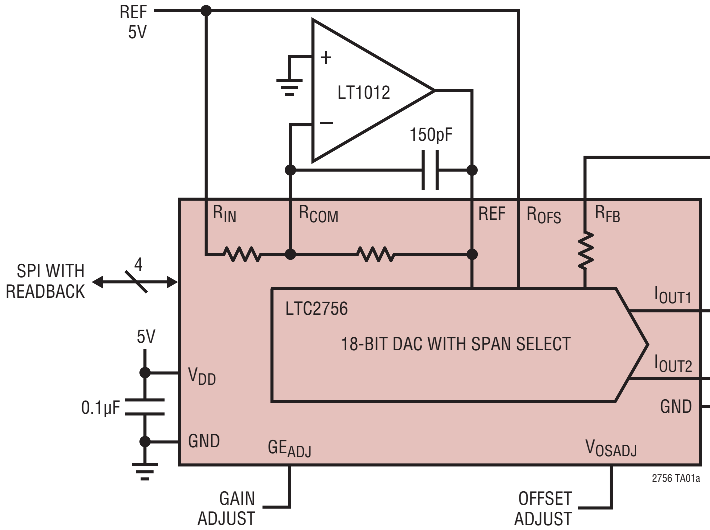
The LTC®2756 is an 18-bit multiplying serial-input, current-output digital-to-analog converter. LTC2756A provides full 18-bit performance—INL and DNL of ±1LSB maximum—over temperature without any adjustments. 18-bit monotonicity is guaranteed in all performance grades. This SoftSpan™ DAC operates from a single 3V to 5V supply and offers six output ranges (up to ±10V) that can be programmed through the 3-wire SPI serial interface or pin-strapped for operation in a single range.

Any on-chip register (including DAC output-range settings) can be read for verification in just one instruction cycle; and if you change register content, the altered register will be automatically read back during the next instruction cycle.

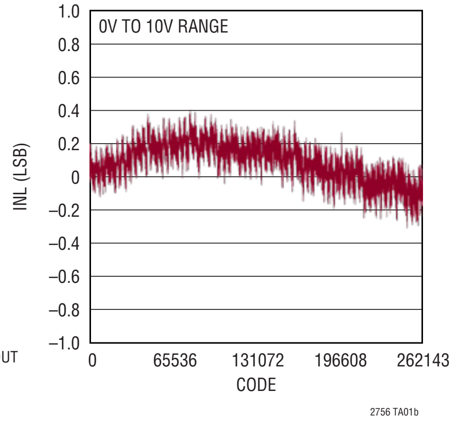
Voltage-controlled offset and gain adjustments are also provided; and the power-on reset circuit and $\overline{CLR}$ pin both reset the DAC output to 0V regardless of output range.

TYPICAL APPLICATION

18-Bit Voltage Output DAC with Software-Selectable Ranges



LTC2756 Integral Nonlinearity

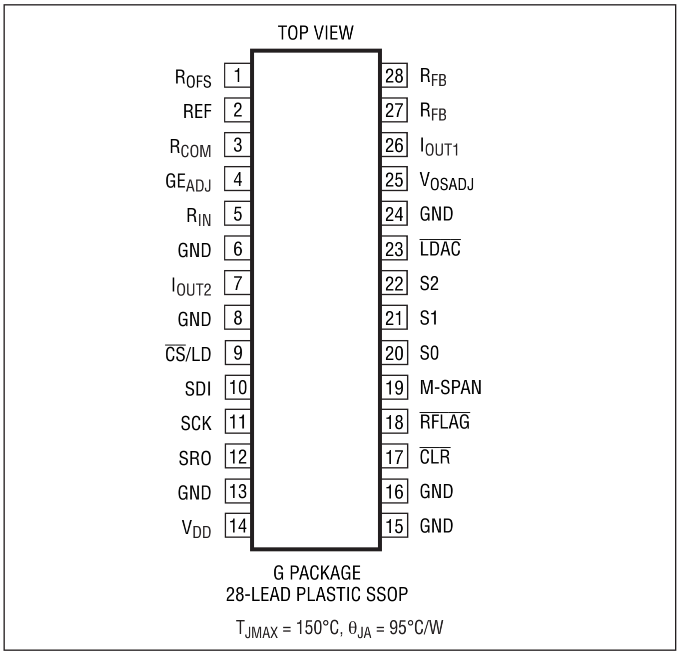


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

I_{OUT1}, I_{OUT2} to GND	±0.3V
R_{IN}, R_{COM}, REF, R_{FB}, R_{OFS}, V_{OSADJ}, GE_{ADJ} to GND	±18V
V_{DD} to GND	–0.3V to 7V
Digital Inputs to GND	–0.3V to 7V
Digital Outputs to GND	–0.3V to V_{DD}+0.3V (Max 7V)
Operating Temperature Range	
LTC2756C	0°C to 70°C
LTC2756I	–40°C to 85°C
Maximum Junction Temperature	150°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION



ORDER INFORMATION

http://www.linear.com/product/LTC2756#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2756BCG#PBF	LTC2756BCG#TRPBF	LTC2756G	28-Lead Plastic SSOP	0°C to 70°C
LTC2756BIG#PBF	LTC2756BIG#TRPBF	LTC2756G	28-Lead Plastic SSOP	–40°C to 85°C
LTC2756ACG#PBF	LTC2756ACG#TRPBF	LTC2756G	28-Lead Plastic SSOP	0°C to 70°C
LTC2756AIG#PBF	LTC2756AIG#TRPBF	LTC2756G	28-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, $V(R_{IN})$ = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		LTC2756B			LTC2756A			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
Static Performance										
	Resolution		●	18			18			Bits
	Monotonicity		●	18			18			Bits
DNL	Differential Nonlinearity		●			±1		±0.25	±1	LSB
INL	Integral Nonlinearity		●			±2		±0.5	±1	LSB
GE	Gain Error	All Output Ranges	●			±40		±5	±28	LSB
	Gain Error Temperature Coefficient	∆Gain/∆Temp			±0.25			±0.25		ppm/°C
BZE	Bipolar Zero Error	All Bipolar Ranges	●			±24		±2.5	±16	LSB
	Bipolar Zero Temperature Coefficient				±0.15			±0.15		ppm/°C
	Unipolar Zero-Scale Error	Unipolar Ranges (Note 3)	●		±0.03	±3.2		±0.03	±3.2	LSB
PSR	Power Supply Rejection	V_{DD} = 5V, ±10% V_{DD} = 3V, ±10%	● ●			±1.6 ±4		±0.05 ±0.2	±0.8 ±2	LSB/V LSB/V
I_{LKG}	I_{OUT1} Leakage Current	T_A = 25°C T_{MIN} to T_{MAX}	 ●		±0.05	±2 ±5		±0.05	±2 ±5	nA nA

V_{DD} = 5V, $V(R_{IN})$ = 5V unless otherwise specified. The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Pins							
	Reference Inverting Resistors	(Note 4)	●	16	20		kΩ
R_{REF}	DAC Input Resistance	(Notes 5, 6)	●	8	10		kΩ
R_{FB}	Feedback Resistors	(Note 6)	●	8	10		kΩ
R_{OFS}	Bipolar Offset Resistors	(Note 6)	●	16	20		kΩ
R_{VOSADJ}	Offset Adjust Resistors		●	1024	1280		kΩ
R_{GEADJ}	Gain Adjust Resistors		●	2048	2560		kΩ
C_{IOUT1}	Output Capacitance	Full-Scale Zero-Scale			90 40		pF
Dynamic Performance							
	Output Settling Time	Span Code = 0000, 10V Step. To ±0.0004% FS (Note 7)			2.1		µs
	Glitch Impulse	V_{DD} = 5V (Note 8) V_{DD} = 3V (Note 8)			2 0.4		nV•s nV•s
	Digital-to-Analog Glitch Impulse	V_{DD} = 5V (Note 9) V_{DD} = 3V (Note 9)			2.6 0.6		nV•s nV•s
	Reference Multiplying BW	0V to 5V Range, Code = Full Scale, –3dB Bandwidth			1		MHz
	Multiplying Feedthrough Error	0V to 5V Range, V_{REF} = ±10V, 10kHz Sine Wave			0.4		mV
THD	Total Harmonic Distortion	(Note 10) Multiplying			–108		dB
	Output Noise Voltage Density	(Note 11) at I_{OUT1}			13		$nV/\sqrt{Hz}$

ELECTRICAL CHARACTERISTICS

V_{DD} = 5V, $V(R_{IN})$ = 5V unless otherwise specified. The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply							
V_{DD}	Supply Voltage		●	2.7		5.5	V
I_{DD}	Supply Current, V_{DD}	Digital Inputs = 0V or V_{DD}	●		0.5	1	µA
Digital Inputs							
V_{IH}	Digital Input High Voltage	$3.3V \le V_{DD} \le 5.5V$ $2.7V \le V_{DD} < 3.3V$	● ●	2.4 2			V V
V_{IL}	Digital Input Low Voltage	$4.5V < V_{DD} \le 5.5V$ $2.7V \le V_{DD} \le 4.5V$	● ●			0.8 0.6	V V
	Hysteresis Voltage				0.1		V
I_{IN}	Digital Input Current	V_{IN} = GND to V_{DD}	●			±1	µA
C_{IN}	Digital Input Capacitance	V_{IN} = 0V (Note 12)	●			6	pF
Digital Outputs							
V_{OH}	I_{OH} = 200µA	$2.7V \le V_{DD} \le 5.5V$	●	$V_{DD} - 0.4$			V
V_{OL}	I_{OL} = 200µA	$2.7V \le V_{DD} \le 5.5V$	●			0.4	V

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} = 4.5V to 5.5V							
t_1	SDI Valid to SCK Set-Up		●	7			ns
t_2	SDI Valid to SCK Hold		●	7			ns
t_3	SCK High Time		●	11			ns
t_4	SCK Low Time		●	11			ns
t_5	$\overline{CS}$/LD Pulse Width		●	9			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	4			ns
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	4			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	4			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			18	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	36			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	15			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 12)	●			50	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ High	C_{LOAD} = 10pF (Note 12)	●			40	ns
	SCK Frequency	50% Duty Cycle (Note 13)	●			40	MHz
V_{DD} = 2.7V to 3.3V							
t_1	SDI Valid to SCK Set-Up		●	9			ns
t_2	SDI Valid to SCK Hold		●	9			ns
t_3	SCK High Time		●	15			ns
t_4	SCK Low Time		●	15			ns
t_5	$\overline{CS}$/LD Pulse Width		●	12			ns
t_6	LSB SCK High to $\overline{CS}$/LD High		●	5			ns

TIMING CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_7	$\overline{CS}$/LD Low to SCK Positive Edge		●	5			ns
t_8	$\overline{CS}$/LD High to SCK Positive Edge		●	5			ns
t_9	SRO Propagation Delay	C_{LOAD} = 10pF	●			26	ns
t_{10}	$\overline{CLR}$ Pulse Width Low		●	60			ns
t_{11}	$\overline{LDAC}$ Pulse Width Low		●	20			ns
t_{12}	$\overline{CLR}$ Low to $\overline{RFLAG}$ Low	C_{LOAD} = 10pF (Note 12)	●			70	ns
t_{13}	$\overline{CS}$/LD High to $\overline{RFLAG}$ high	C_{LOAD} = 10pF (Note 12)	●			60	ns
	SCK Frequency	50% Duty Cycle (Note 13)	●			25	MHz

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: Calculation from feedback resistance and I_{OUT1} leakage current specifications; not production tested. In most applications, unipolar zero-scale error is dominated by contributions from the output amplifier.

Note 4: Input resistors measured from R_{IN} to R_{COM}; feedback resistors measured from R_{COM} to REF.

Note 5: DAC input resistance is independent of code.

Note 6: Parallel combination of the resistances from the specified pin to I_{OUT1} and from the specified pin to I_{OUT2}.

Note 7: Using LT1468 with $C_{FEEDBACK}$ = 27pF. A ±0.0004% settling time of 1.8µs can be achieved by optimizing the time constant on an individual basis. See Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC.*

Note 8: Measured at the major carry transition, 0V to 5V range. Output amplifier: LT1468; C_{FB} = 50pF.

Note 9: Full-scale transition; REF = 0V.

Note 10: REF = $6V_{RMS}$ at 1kHz. 0V to 5V range. DAC code = FS. Output amplifier = LT1468.

Note 11: Calculation from $V_n = \sqrt{4kTRB}$, where k = 1.38E-23 J/°K (Boltzmann constant), R = resistance (Ω), T = temperature (°K), and B = bandwidth (Hz). 0V to 5V Range; zero-, mid-, or full-scale.

Note 12: Guaranteed by design; not production tested.

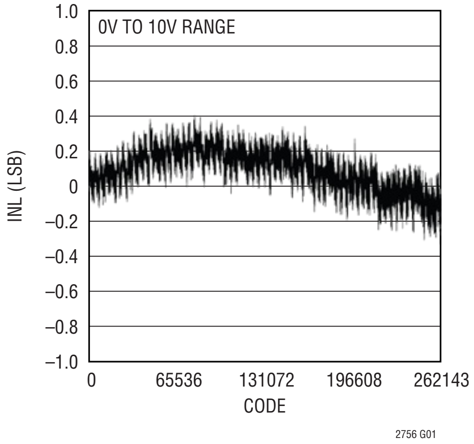
Note 13: When using SRO, maximum SCK frequency f_{MAX} is limited by SRO propagation delay t_9 as follows:

$$f_{MAX} = \left(\frac{1}{2(t_9 + t_S)}\right)$$, where t_S is the setup time of the receiving device.

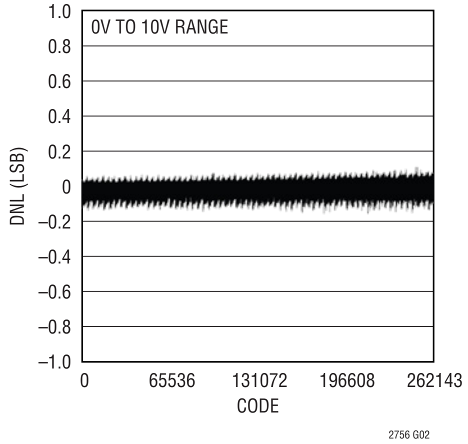
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, $V(R_{IN})$ = 5V, T_A = 25°C, unless otherwise noted.

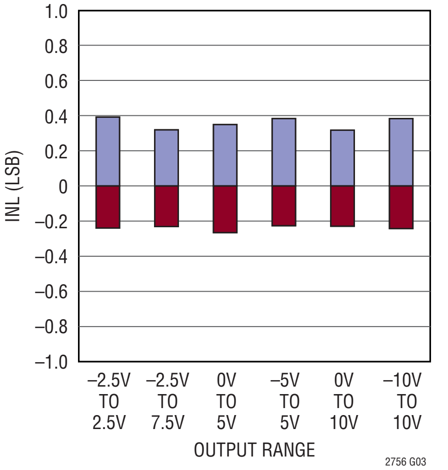
Integral Nonlinearity (INL)



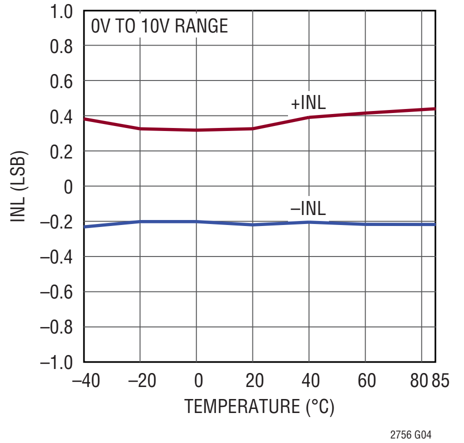
Differential Nonlinearity (DNL)



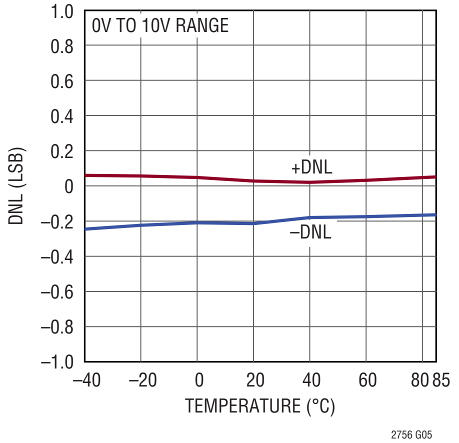
INL vs Output Range



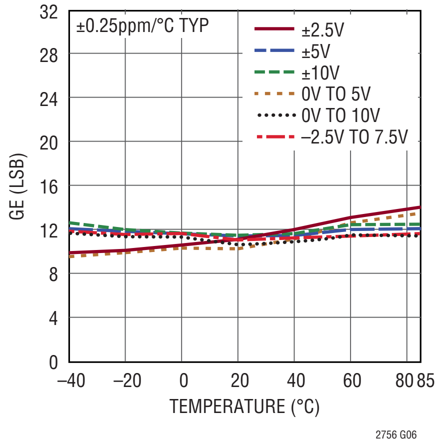
INL vs Temperature



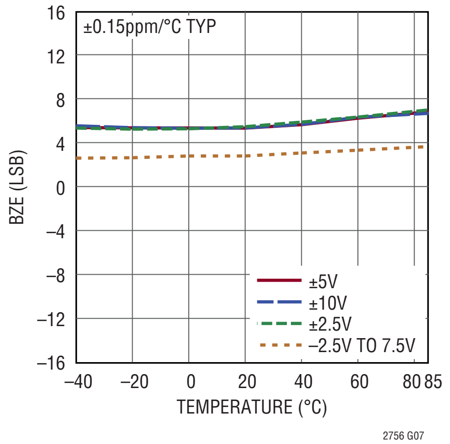
DNL vs Temperature



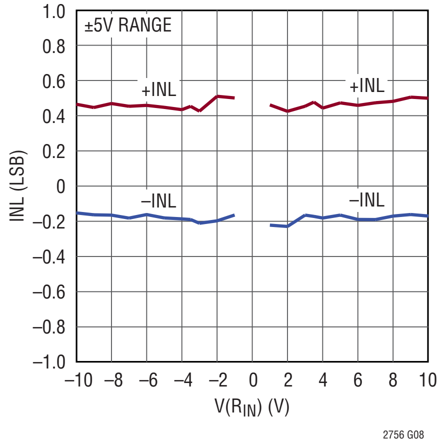
Gain Error vs Temperature



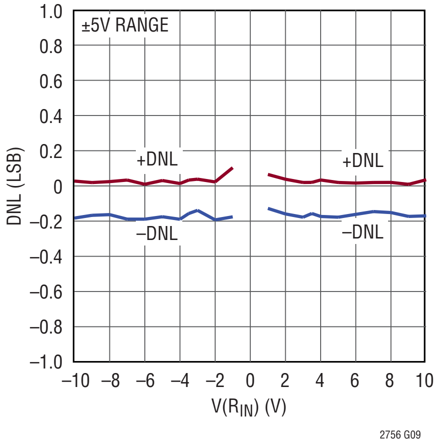
Bipolar Zero Error vs Temperature



INL vs Reference Voltage



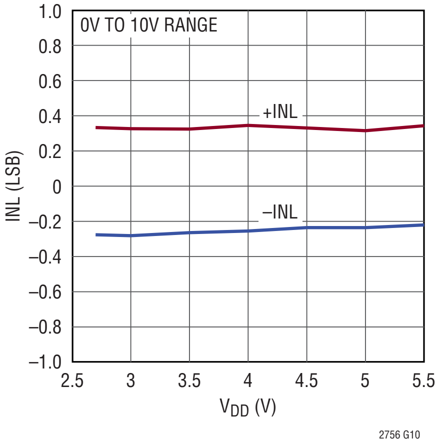
DNL vs Reference Voltage



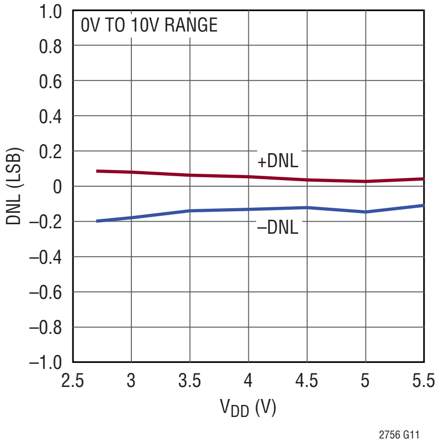
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} = 5V, $V(R_{IN})$ = 5V, T_A = 25°C, unless otherwise noted.

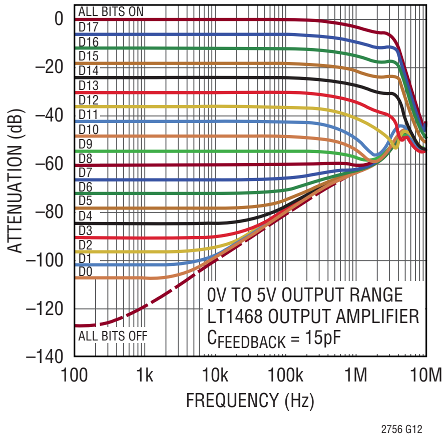
INL vs V_{DD}



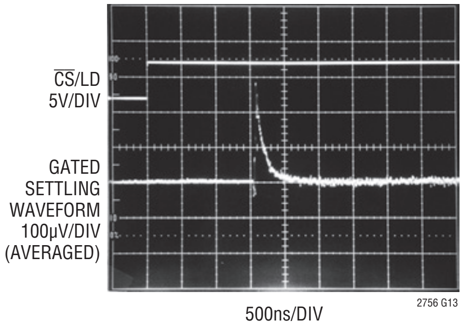
DNL vs V_{DD}



Multiplying Frequency Response vs Digital Code

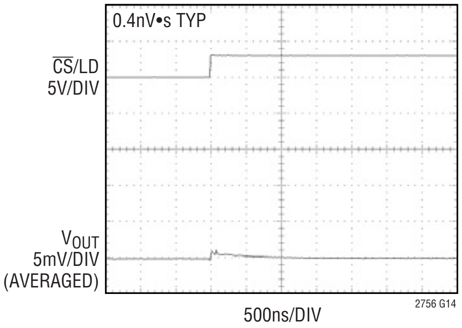


Settling Full-Scale Step



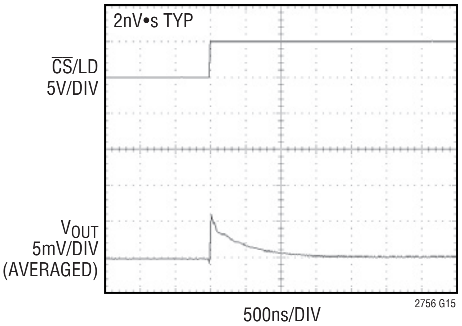
LT1468 AMP; $C_{FEEDBACK}$ = 20pF
0V TO 10V STEP
V_{REF} = –10V; SPAN CODE = 0000
t_{SETTLE} = 1.8μs to 0.0004% (18 BITS)

Mid-Scale Glitch (V_{DD} = 3V)



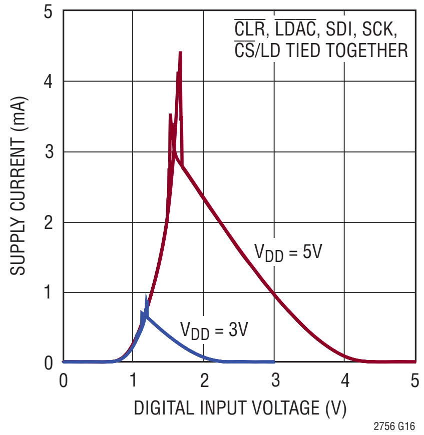
0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER.

Mid-Scale Glitch (V_{DD} = 5V)

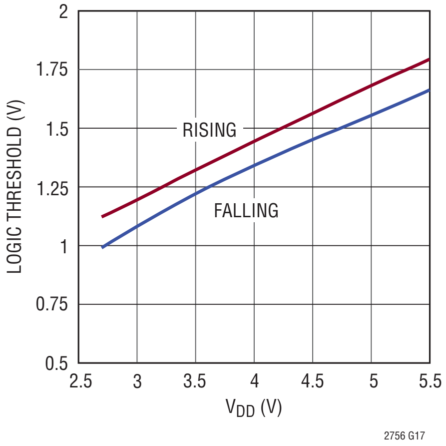


0V TO 5V RANGE
LT1468 OUTPUT AMPLIFIER
$C_{FEEDBACK}$ = 50pF
RISING MAJOR CARRY TRANSITION.
FALLING TRANSITION IS SIMILAR OR BETTER.

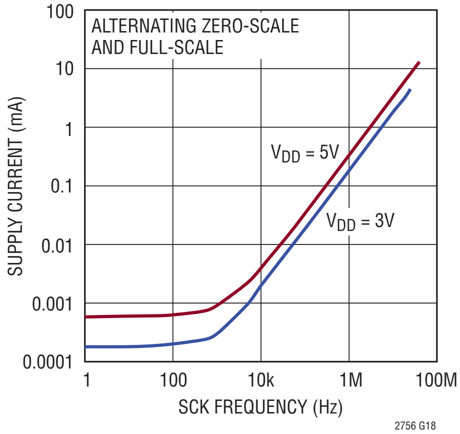
Supply Current vs Logic Input Voltage



Logic Threshold vs Supply Voltage



Supply Current vs Update Frequency



PIN FUNCTIONS

R_{OFS} (Pin 1): Bipolar Offset Resistor. This pin provides the translation of the output voltage range for bipolar spans. Accepts up to ±15V; for normal operation tie to the positive reference voltage at R_{IN} (Pin 5).

REF (Pin 2): DAC Reference Input, and Feedback Resistor for the Reference Inverting Amplifier. The external reference inverting amplifier sees as its load the 10k DAC reference input resistance in parallel with the 20k feedback resistor. For normal operation tie this pin to the output of the reference inverting amplifier (see the Typical Applications section). Typically 5V; accepts up to ±15V.

R_{COM} (Pin 3): Virtual Ground Point for the On-Chip Reference Inverting Resistors. These precision-matched 20k resistors are included on the chip to facilitate generation of the negative reference voltage needed to produce a positive output polarity. They are connected internally from R_{IN} to R_{COM} and from R_{COM} to REF (see Block Diagram). For normal operation tie R_{COM} to the negative input of the external reference inverting amplifier (see the Typical Applications section).

GE_{ADJA} (Pin 4): Gain Adjust Pin. This control pin can be used to null gain error or to compensate for reference errors. Nominal adjustment range is ±2048 LSB for a voltage input range of $\pm V_{RIN}$ (i.e., ±5V for a 5V reference input). Tie to ground if not used.

R_{IN} (Pin 5): Input Resistor for Reference Inverting Amplifier. The 20k input resistor is connected internally from R_{IN} to R_{COM}. For normal operation tie R_{IN} to the external reference voltage (see the Typical Applications section). Typically 5V; accepts up to ±15V.

GND (Pins 6, 8, 13, 15, 16, 24): Ground; tie to ground.

I_{OUT2} (Pin 7): Current Output Complement. Tie to ground via a clean, low-impedance path.

$\overline{CS}$/LD (Pin 9): Synchronous Chip Select and Load Input Pin. A logic low on this pin enables SDI, SCK and SRO (Pins 10, 11 and 12) for input and output of serial data.

SDI (Pin 10): Serial Data Input. Data is clocked in on the rising edge of the serial clock (SCK, Pin 11) when $\overline{CS}$/LD (Pin 9) is low.

SCK (Pin 11): Serial Clock.

SRO (Pin 12): Serial Readback Output. Data is clocked out on the falling edge of SCK. Readback data begins clocking out after the first byte is clocked in. SRO is an active output only when the chip is selected (i.e., when $\overline{CS}$/LD is low). Otherwise SRO presents a high-impedance output in order to allow other parts to control the bus.

V_{DD} (Pin 14): Positive Supply Input; $2.7V \le V_{DD} \le 5.5V$. Bypass with a 0.1μF low-ESR capacitor to ground.

$\overline{CLR}$ (Pin 17): Asynchronous Clear Input. When this pin is low, all DAC registers (both code and span) are cleared to zero. The DAC output is cleared to zero volts.

$\overline{RFLAG}$ (Pin 18): Reset Flag Output. An active low output is asserted when there is a power-on reset or a clear event. Returns high when an Update command is executed.

M-SPAN (Pin 19): Manual Span Control Pin. M-SPAN is used in conjunction with pins S0, S1 and S2 (Pins 20, 21 and 22) to configure the DAC for operation in a single, fixed output range.

To configure the part for manual-span use, tie M-SPAN directly to V_{DD}. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span.

To configure the part for SoftSpan use, tie M-SPAN directly to GND. The output ranges are then individually controllable through the SPI port; and pins S2, S1 and S0 have no effect.

See Manual Span Configuration in the Operation section. M-SPAN must be connected either directly to GND (SoftSpan configuration) or to V_{DD} (manual-span configuration).

PIN FUNCTIONS

S0 (Pin 20): Span Bit 0 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or V_{DD} even if they are unused.

S1 (Pin 21): Span Bit 1 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or V_{DD} even if they are unused.

S2 (Pin 22): Span Bit 2 Input. In Manual Span mode (M-SPAN tied to V_{DD}), pins S0, S1 and S2 are pin-strapped to select a single fixed output range. These pins must be tied to either GND or V_{DD} even if they are unused.

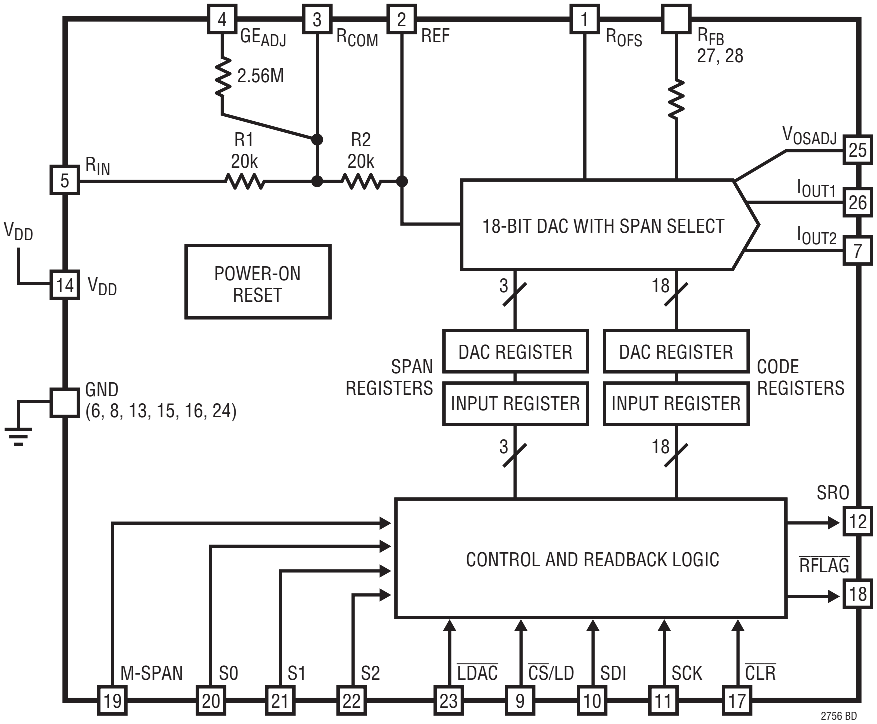
$\overline{\text{LDAC}}$ (Pin 23): Asynchronous DAC Load Input. When $\overline{\text{LDAC}}$ is logic low, the DAC is updated ($\overline{\text{CS}}$/LD must be high).

V_{OSADJ} (Pin 25): Offset Adjust Pin. This control pin can be used to null unipolar offset or bipolar zero error. The offset-voltage delta is inverted and attenuated such that a 5V control voltage applied to V_{OSADJ} produces ΔV_{OS} = –2048 LSB in any output range (assumes a 5V reference voltage at R_{IN}). See *System Offset and Gain Adjustments* in the Operation section. Tie to ground if not used.

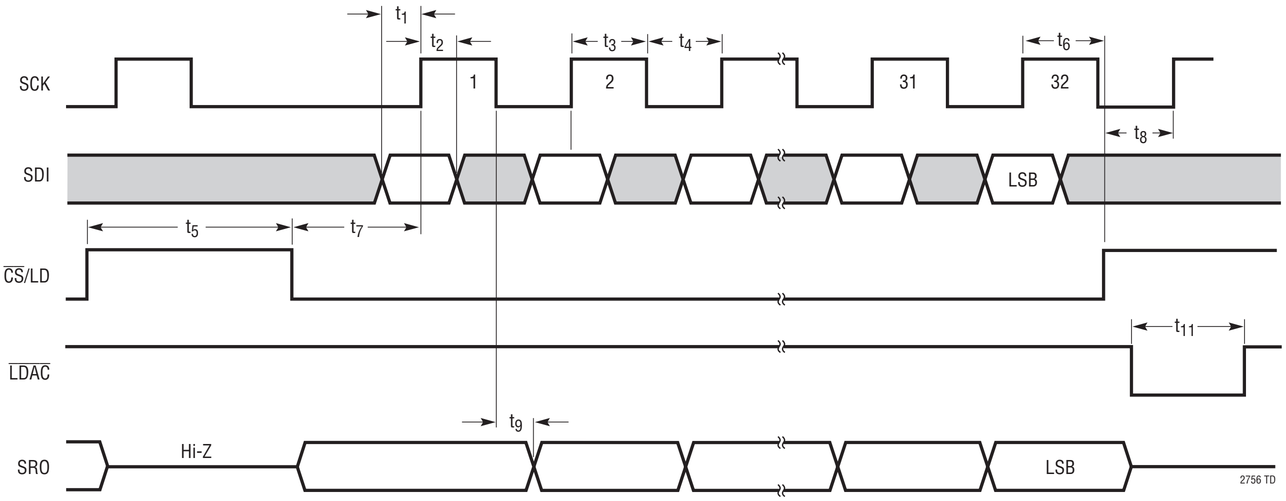
I_{OUT1} (Pin 26): Current Output Pin. This pin is a virtual ground when the DAC is operating and should reside at 0V. For normal operation tie to the negative input of the I/V converter amplifier (see the Typical Applications section).

R_{FB} (Pins 27, 28): Feedback Resistor. For normal operation tie both pins to the output of the I/V converter amplifier (see the Typical Applications section). The DAC output current from I_{OUT1} flows through the feedback resistor to the R_{FB} pins.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Output Ranges

The LTC2756 is a current-output, serial-input precision multiplying DAC with selectable output ranges. Ranges can either be programmed in software for maximum flexibility—the DAC can be programmed to any one of six output ranges—or hardwired through pin-strapping. Two unipolar ranges are available (0V to 5V and 0V to 10V), and four bipolar ranges (±2.5V, ±5V, ±10V and –2.5V to 7.5V). These ranges are obtained when an external precision 5V reference is used. The output ranges for other reference voltages are easy to calculate by observing that each range is a multiple of the external reference voltage. The ranges can then be expressed: 0 to 1×, 0 to 2×, ±0.5×, ±1×, ±2×, and –0.5× to 1.5×.

Manual Span Configuration

Multiple output ranges are not needed in some applications. To configure the LTC2756 to operate in a single span without additional operational overhead, tie the M-SPAN pin directly to V_{DD}. The active output range is then set via hardware pin strapping of pins S2, S1 and S0 (rather than through the SPI port); and Write and Update commands have no effect on the active output span. See Figure 1 and Table 2.

Tie the M-SPAN pin to ground for normal SoftSpan operation.

Input and DAC Registers

The LTC2756 has two sets of double-buffered registers—one set for the code data, and one for the output range of the DAC—plus one readback register, for a total of five registers. Double buffering provides the capability to simultaneously update the span (output range) and code, which allows smooth voltage transitions when changing output ranges.

Each set of double-buffered registers comprises an Input register and a DAC register.

Input register: The Write operation shifts data from the SDI pin into a chosen Input register. The Input registers are holding buffers; Write operations do not affect the DAC outputs.

DAC register: The Update operation copies the contents of an Input register to its associated DAC register. The contents of a DAC register directly updates the associated DAC output voltage or output range.

Note that updates always include both Code and Span register sets; but the values held in the DAC registers will only change if the associated Input register values have previously been altered via a Write operation.

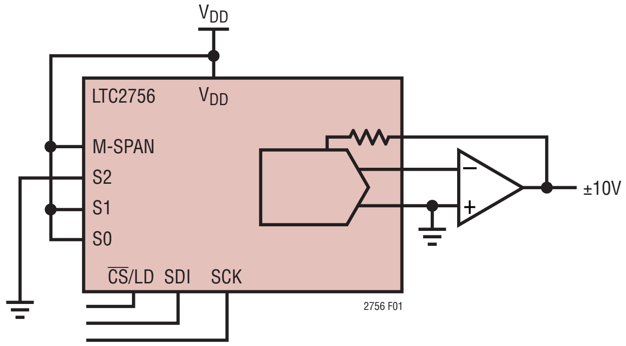


Figure 1. Using M-SPAN to Configure the LTC2756 for Single-Span Operation (±10V Range Shown)

OPERATION

Serial Interface

When the $\overline{\text{CS}}$/LD pin is taken low, the data on the SDI pin is loaded into the shift register on the rising edge of the clock (SCK pin). The loading sequence required for the LTC2756 is one byte consisting of a 4-bit command word (C3 C2 C1 C0) and four zeros, then three bytes (24 bits) of data.

When writing a code, the code data is left (MSB) justified; so that the 24-bit data field consists of 18 code bits followed by 6 don't-care bits.

When writing an output range, the span data should occupy the last 4 bits of the second data byte, ordered S3 through S0. Figure 2 shows the SDI input word syntax for writing.

When $\overline{\text{CS}}$/LD is low, the SRO pin (Serial Readback Output) is an active output. The readback data begins after the first byte has been shifted in to SDI. SRO outputs a logic low from the falling edge of $\overline{\text{CS}}$/LD until the Readback data begins.

When $\overline{\text{CS}}$/LD is high, the SRO pin presents a high impedance (three-state) output.

$\overline{\text{LDAC}}$ is an asynchronous update pin. When $\overline{\text{LDAC}}$ is taken low, the DAC is updated with code and span data (data in the Input buffers is copied into the DAC buffers). $\overline{\text{CS}}$/LD must be high during this operation; otherwise $\overline{\text{LDAC}}$ is locked out and will have no effect. The use of $\overline{\text{LDAC}}$ is functionally identical to the serial input command.

The codes for the command (C3-C0) are defined in Table 1.

Readback

In addition to the Code and Span register sets, the LTC2756 has one Readback register. At the end of every instruction cycle, the contents of one of the on-chip registers is copied into the Readback register and serially shifted out through the SRO pin.

Readback data always appears in the 24-bit data field, starting on the falling SCK edge immediately after the first byte is shifted in on SDI. When reading a code, code data occupies the first 18 bits of the 24-bit field; and the span bits are the last four bits of the second data byte when checking the output range. In both cases, all other bits in the 24-bit data field are filled by zeros. Figure 2 shows the input and readback sequences.

The data outputted by SRO is always in the same position and sequence as the input data. Note, however, that this means that the SRO data shifts out one-half clock cycle *earlier* than the corresponding bit shifting in on SDI. For example, code bit D9, which is shifted in to SDI on the rising edge of SCK clock 17, is clocked out of SRO on the *falling* edge of clock 16. This allows D9 to be clocked to an external microprocessor on the rising edge of clock 17.

For Read commands, the requested data is shifted out of SRO in the 3-byte (24-bit) data field immediately after the command byte. There is no instruction-cycle latency for Read commands; the data shifts out in the same instruction cycle in which it was requested.

For non-read (i.e., Write and/or Update) commands, SRO automatically shifts out the contents of the buffer that was acted upon in the preceding command. This "rolling readback" default mode of operation can dramatically reduce the number of instruction cycles needed, since most commands can be verified during subsequent commands with no additional overhead. A conceptual flow diagram is shown in Figure 3. Table 1 shows, for each antecedent command, which register ('readback pointer') will be copied into the Readback register and outputted from SRO during the following instruction cycle.

Span Readback in Manual Span Configuration

If the Span DAC register is chosen for readback, SRO responds by outputting the actual output span; this is true whether the LTC2756 is configured for SoftSpan (M-SPAN tied to GND) or manual span (M-SPAN tied to V_{DD}).

In SoftSpan configuration, SRO outputs the span code from the Span DAC register (programmed through the SPI port). In manual span configuration, the active output range is controlled by pins S2, S1 and S0, so SRO outputs the logic values of these pins. The span code bits S2, S1 and S0 always appear in the same order and positions in the SRO output sequence; see Figure 2.

OPERATION

Table 1. Command Codes

CODE C3	C2	C1	C0	COMMAND	READBACK POINTER– CURRENT INPUT WORD W_0	READBACK POINTER– NEXT INPUT WORD W_{+1}
0	0	1	0	Write Span	Set by Previous Command	Input Span Register
0	0	1	1	Write Code	Set by Previous Command	Input Code Register
0	1	0	0	Update	Set by Previous Command	DAC Span Register
0	1	1	0	Write Span; Update	Set by Previous Command	DAC Span Register
0	1	1	1	Write Code; Update	Set by Previous Command	DAC Code Register
1	0	1	0	Read Input Span Register	Input Span Register	Input Span Register
1	0	1	1	Read Input Code Register	Input Code Register	Input Code Register
1	1	0	0	Read DAC Span Register	DAC Span Register	DAC Span Register
1	1	0	1	Read DAC Code Register	DAC Code Register	DAC Code Register
1	1	1	1	No Operation	Set by Previous Command	DAC Code Register
—				System Clear	—	DAC Span Register
—				Initial Power-Up or Power Interrupt	—	DAC Span Register

Codes not shown are reserved—do not use.

Table 2. Span Codes

S3	S2	S1	S0	SPAN
0	0	0	0	Unipolar 0V to 5V
0	0	0	1	Unipolar 0V to 10V
0	0	1	0	Bipolar –5V to 5V
0	0	1	1	Bipolar –10V to 10V
0	1	0	0	Bipolar –2.5V to 2.5V
0	1	0	1	Bipolar –2.5V to 7.5V

Codes not shown are reserved–do not use.

OPERATION

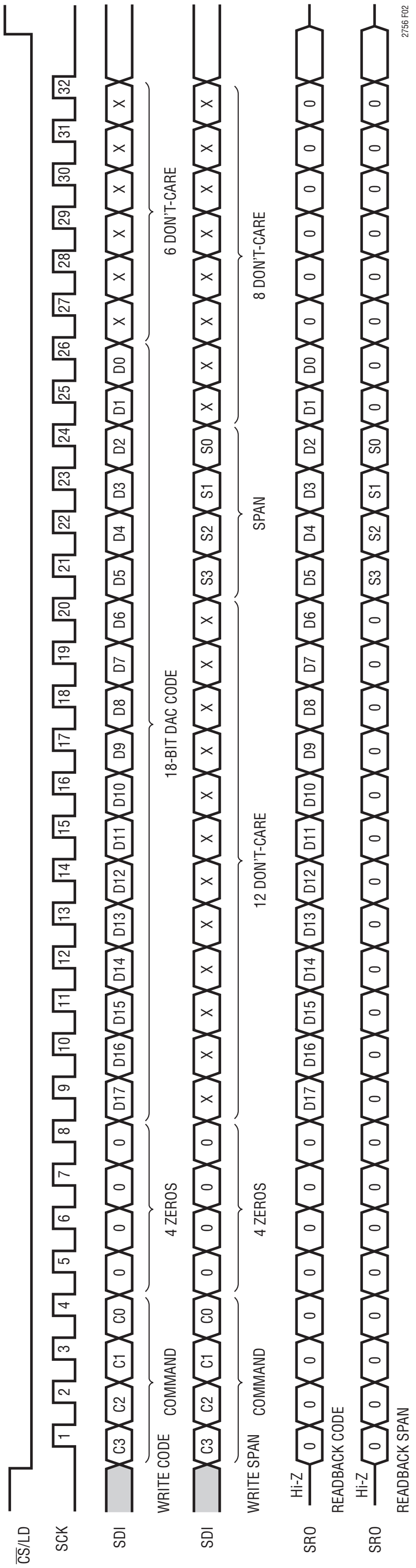


Figure 2. Serial Input and Output Sequences

OPERATION

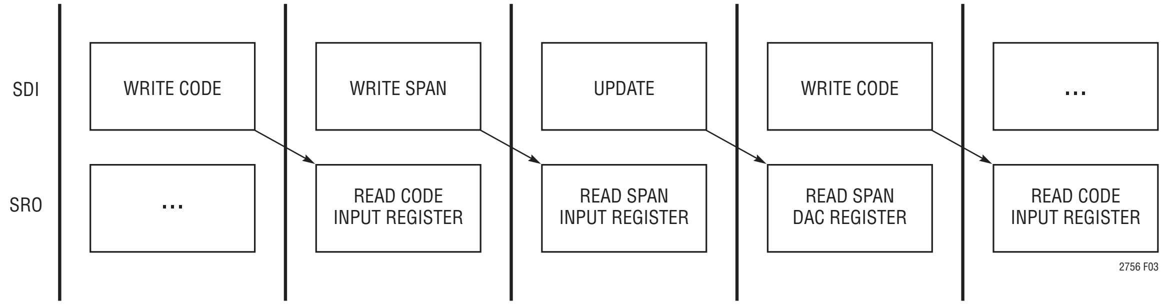


Figure 3. Rolling Readback Example

OPERATION

Examples

1. Load ±5V range with the output at 0V. Note that since span and code are updated together, the output stays at 0V throughout the example.

   a) $\overline{CS}$/LD ↓. Clock SDI:
   00100000 XXXXXXXX XXXX0010 XXXXXXXX

   b) $\overline{CS}$/LD ↑
   Span Input register – range set to bipolar ±5V.

   c) $\overline{CS}$/LD ↓. Clock SDI:
   00110000 10000000 00000000 00XXXXXX

   d) $\overline{CS}$/LD ↑
   Code Input register – code set to mid-scale.

   e) $\overline{CS}$/LD ↓. Clock SDI:
   01000000 XXXXXXXX XXXXXXXX XXXXXXXX

   f) $\overline{CS}$/LD ↑
   Update code and range.
   Alternatively steps e and f could be replaced with LDAC ⊔.

2. Load ±10V range with the output at 5V, changing to –5V.

   a) $\overline{CS}$/LD ↓. Clock SDI:
   00110000 11000000 00000000 00XXXXXX

   b) $\overline{CS}$/LD ↑
   Code Input register set to ¾-scale code.

   c) $\overline{CS}$/LD ↓. Clock SDI:
   01100000 XXXXXXXX XXXX0011 XXXXXXXX

   d) $\overline{CS}$/LD ↑
   Span Input register set to ±10V range. Update code and range. Output goes to 5V.

   g) $\overline{CS}$/LD ↓. Clock SDI:
   01110000 01000000 00000000 00XXXXXX

   h) $\overline{CS}$/LD ↑
   Code Input register set to ¼-scale code. Update code and range (note update does not change range, since no new range has been written).
   Output goes to –5V.

3. Write and update mid-scale code in 0V to 10V range (V_{OUT} = 5V) using readback to check the contents of the Input registers before updating.

   a) $\overline{CS}$/LD ↓. Clock SDI:
   00110000 10000000 00000000 00XXXXXX

   b) $\overline{CS}$/LD ↑
   Code Input register set to mid-scale.

   c) $\overline{CS}$/LD ↓. Clock SDI:
   00100000 XXXXXXXX XXXX0001 XXXXXXXX
   Data out on SRO:
   00000000 10000000 00000000 00000000
   Verifies Code Input register set to mid-scale.

   d) $\overline{CS}$/LD ↑
   Span Input register set to 0V to 10V range.

   e) $\overline{CS}$/LD ↓. Clock SDI:
   10100000 XXXXXXXX XXXXXXXX XXXXXXXX
   Data out on SRO:
   00000000 00000000 00000001 00000000
   Verifies Span Input register set to 0V to 10V range.

   f) $\overline{CS}$/LD ↑

   g) $\overline{CS}$/LD ↓. Clock SDI:
   01000000 XXXXXXXX XXXXXXXX XXXXXXXX

   h) $\overline{CS}$/LD ↑
   Update code and range. Output goes to 5V.

OPERATION

System Offset and Reference Adjustments

Many systems require compensation for overall system offset. This may be an order of magnitude or more greater than the offset of the LTC2756, which is so low as to be dominated by external output amplifier errors even when using the most precise op amps.

The offset adjust pin V_{OSADJ} can be used to null unipolar offset or bipolar zero error. The offset change expressed in LSB is the same for any output range:

$$\Delta V_{OS}\left[\text{LSB}\right]=\frac{-V(V_{OSADJ})}{V(R_{IN})}\bullet 2048$$

A 5V control voltage applied to V_{OSADJ} produces ΔV_{OS} = –2048 LSB in any output range, assuming a 5V reference voltage at R_{IN}.

In voltage terms, the offset delta is attenuated by a factor of 32, 64 or 128, depending on the output range. (These functions hold regardless of reference voltage.)

$\Delta V_{OS} = -(^1/_{128})V_{OSADJ}$ [0V to 5V, ±2.5V spans]

$\Delta V_{OS} = -(^1/_{64})V_{OSADJ}$ [0V to 10V, ±5V, –2.5V to 7.5V spans]

$\Delta V_{OS} = -(^1/_{32})V_{OSADJ}$ [±10V span]

The gain error adjust pins GE_{ADJ} can be used to null gain error or to compensate for reference errors. The gain error change expressed in LSB is the same for any output range:

$$\Delta GE=\frac{V(GE_{ADJ})}{V(R_{IN})}\bullet 2048$$

The gain-error delta is non-inverting for positive reference voltages.

Note that this pin compensates the gain by altering the inverted reference voltage V(REF). In voltage terms, the V(REF) delta is inverted and attenuated by a factor of 128.

$\Delta V(REF) = -(^1/_{128})GE_{ADJ}$

The nominal input range of these pins is ±5V; other voltages of up to ±15V may be used if needed. However, do not use voltages divided down from power supplies; reference-quality, low-noise inputs are required to maintain the best DAC performance.

The V_{OSADJ} pin has an input impedance of 1.28MΩ. It should be driven with a Thevenin-equivalent impedance of 10k or less to preserve the settling performance of the LTC2756. The V_{OSADJ} pin should be shorted to GND if not used.

The GE_{ADJ} pin has an input impedance of 2.56MΩ, and is intended for use with fixed reference voltages only. It should be shorted to GND if not used.

Power-On Reset and Clear

When power is first applied to the LTC2756, the DAC powers up in unipolar 5V mode (S3 S2 S1 S0 = 0000). All internal DAC registers are reset to 0 and the DAC output initializes to zero volts.

If the part is configured for manual span operation, the DAC will be set into the pin-strapped range at the first Update command. This allows the user to simultaneously update span and code for a smooth voltage transition into the chosen output range.

When the $\overline{\text{CLR}}$ pin is taken low, a system clear results. The DAC buffers are reset to 0 and the DAC output is reset to zero volts. The Input buffers are left intact, so that any subsequent Update command (including the use of $\overline{\text{LDAC}}$) restores the DAC to its previous state.

If $\overline{\text{CLR}}$ is asserted during an instruction, i.e., when $\overline{\text{CS}}$/LD is low, the instruction is aborted. Integrity of the relevant Input buffers is not guaranteed under these conditions, therefore the contents should be checked using readback or replaced.

The $\overline{\text{RFLAG}}$ pin is used as a flag to notify the system of a loss of data integrity. The $\overline{\text{RFLAG}}$ output is asserted low at power-up, system clear, or if the supply V_{DD} dips below approximately 2V; and stays asserted until any valid Update command is executed.

APPLICATIONS INFORMATION

Op Amp Selection

Because of the extremely high accuracy of the 18-bit LTC2756, careful thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Table 3. Coefficients for the Equations of Table 4

OUTPUT RANGE	A1	A2	A3	A4	A5
5V	1.1	2	1	–	1
10V	2.2	3	0.5	–	1.5
±5V	2	2	1	1	1.5
±10V	4	4	0.83	1	2.5
±2.5V	1	1	1.4	1	1
–2.5V to 7.5V	1.9	3	0.7	0.5	1.5

Tables 3 and 4 contain equations for evaluating the effects of op amp parameters on the LTC2756's accuracy when programmed in a unipolar or bipolar output range. These are the changes the op amp can cause to the INL, DNL, unipolar offset, unipolar gain error, bipolar zero and bipolar gain error.

Table 5 contains a partial list of LTC precision op amps recommended for use with the LTC2756. The easy-to-use design equations simplify the selection of op amps to meet the system's specified error budget. Select the amplifier from Table 5 and insert the specified op amp parameters in Table 4. Add up all the errors for each category to determine the effect the op amp has on the accuracy of the part. Arithmetic summation gives an (unlikely) worst-case effect. A root-sum-square (RMS) summation produces a more realistic estimate.

Table 4. Easy-to-Use Equations Determine Op Amp Effects on DAC Accuracy in All Output Ranges (Circuit of Page 1). Subscript 1 Refers to Output Amp, Subscript 2 Refers to Reference Inverting Amp.

OP AMP	INL (LSB)	DNL (LSB)	UNIPOLAR OFFSET (LSB)	BIPOLAR ZERO ERROR (LSB)	UNIPOLAR GAIN ERROR (LSB)	BIPOLAR GAIN ERROR (LSB)
V_{OS1} (mV)	$V_{OS1} \bullet 12.1 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 3.1 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$A3 \bullet V_{OS1} \bullet 78.6 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS1} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B1} (nA)	$I_{B1} \bullet 0.0012 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.00032 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0072 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B1} \bullet 0.0072 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL1} (V/mV)	$A1 \bullet \left(\frac{66}{A_{VOL1}}\right)$	$A2 \bullet \left(\frac{6}{A_{VOL1}}\right)$	0	0	$A5 \bullet \left(\frac{524}{A_{VOL1}}\right)$	$A5 \bullet \left(\frac{524}{A_{VOL1}}\right)$
V_{OS2} (mV)	0	0	0	$A4 \bullet V_{OS2} \bullet 52.4 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 104.8 \bullet \left(\frac{5V}{V_{REF}}\right)$	$V_{OS2} \bullet 104.8 \bullet \left(\frac{5V}{V_{REF}}\right)$
I_{B2} (nA)	0	0	0	$A4 \bullet I_{B2} \bullet 0.524 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 1.048 \bullet \left(\frac{5V}{V_{REF}}\right)$	$I_{B2} \bullet 1.048 \bullet \left(\frac{5V}{V_{REF}}\right)$
A_{VOL2} (V/mV)	0	0	0	$A4 \bullet \left(\frac{262}{A_{VOL2}}\right)$	$\left(\frac{524}{A_{VOL2}}\right)$	$\left(\frac{524}{A_{VOL2}}\right)$

Table 5. Partial List of LTC Precision Amplifiers Recommended for Use with the LTC2756 with Relevant Specifications

	AMPLIFIER SPECIFICATIONS								
AMPLIFIER	V_{OS} µV	I_B nA	A_{VOL} V/mV	VOLTAGE NOISE nV/√Hz	CURRENT NOISE pA/√Hz	SLEW RATE V/µs	GAIN BANDWIDTH PRODUCT MHz	$t_{SETTLING}$ with LTC2756 µs	POWER DISSIPATION mW
LTC1150	10	0.05	5600	90	0.0018	3	2.5	10ms	24
LT1001	25	2	800	10	0.12	0.25	0.8	120	46
LT1012	25	0.1	2000	14	0.02	0.2	1	120	11.4
LT1097	50	0.35	2500	14	0.008	0.2	0.7	120	11
LT1468	75	10	5000	5	0.6	22	90	2.1	117

APPLICATIONS INFORMATION

Op amp offset contributes mostly to DAC output offset and gain error, and has minimal effect on INL and DNL. For example, consider the LTC2756 in unipolar 5V output range. (Note that for this example, the LSB size is 19µV.) An op amp offset of 35µV will cause 1.8LSB of output offset, and 1.8LSB of gain error; but 0.4LSB of INL, and just 0.1LSB of DNL.

While not directly addressed by the simple equations in Tables 3 and 4, temperature effects can be handled just as easily for unipolar and bipolar applications. First, consult an op amp's data sheet to find the worst-case V_{OS} and I_B over temperature. Then, plug these numbers in the V_{OS} and I_B equations from Table 4 and calculate the temperature-induced effects.

For applications where fast settling time is important, Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC*, offers a thorough discussion of 18-bit DAC settling time and op amp selection.

Recommendations

For DC or low-frequency applications, the LTC1150 is the simplest 18-bit accurate output amplifier. An auto-zero amp, its exceptionally low offset (10µV max) and offset drift (0.01µV/°C) make nulling unnecessary. For swings above 8V, add an LT®1010 buffer to boost the load current capability. The settling of auto-zero amps is a special case; see Application Note 120, *1ppm Settling Time Measurement for a Monolithic 18-Bit DAC*, Appendix E, for details.

The LT1012 and LT1001 are good intermediate output-amp solutions that achieve moderate speed and good accuracy. They are also excellent choices for the reference inverting amplifier in fixed-reference applications.

For high speed applications, the LT1468 settles in 2.1µs. Note that the 75µV max offset will degrade the INL at the DAC output by up to 0.9LSB. For high-speed applications demanding higher precision, the amplifier offset can be nulled with a digital potentiometer.

Figure 5 shows a composite output amplifier that achieves fast settling (8µs) and very low offset (3µV max) without offset nulling. This circuit offers high open-loop gain (1000V/mV min), low input bias current (0.15nA max), fast slew rate (25V/µs min), and a high gain-bandwidth product (30MHz typ). The high speed path consists of an LTC6240HV, which is an 18MHz ultralow bias current amplifier, followed by an LT1360, a 50MHz fast-slewing amplifier which provides additional gain and the ability to swing to ±10V at the output. Compensation is taken from the output of the LTC6240HV, allowing the use of a much larger compensation capacitor than if taken after the gain-of-five stage. An LTC2054HV auto-zero amplifier senses the voltage at I_{OUT1} and drives the non-inverting input of the LTC6240HV to eliminate the offset of the high speed path. The 100:1 attenuator and input filter reduce the low frequency noise in this stage while maintaining low DC offset.

Precision Voltage Reference Considerations

Much in the same way selecting an operational amplifier for use with the LTC2756 is critical to the performance of the system, selecting a precision voltage reference also requires due diligence. The output voltage of the LTC2756 is directly affected by the voltage reference; thus, any voltage reference error will appear as a DAC output voltage error.

There are three primary error sources to consider when selecting a precision voltage reference for 18-bit applications: output voltage initial tolerance, output voltage temperature coefficient and output voltage noise.

Initial reference output voltage tolerance, if uncorrected, generates a full-scale error term. Choosing a reference with low output voltage initial tolerance, like the LTC6655 (±0.025%), minimizes the gain error caused by the reference; however, a calibration sequence that corrects for system zero- and full-scale error is always recommended.

A reference's output voltage temperature coefficient affects not only the full-scale error, but can also affect the circuit's INL and DNL performance. If a reference is chosen with a loose output voltage temperature coefficient, then the DAC output voltage along its transfer characteristic will be very dependent on ambient conditions. Minimizing the error due to reference temperature coefficient can be achieved by choosing a precision reference with a low output voltage temperature coefficient and/or tightly controlling the ambient temperature of the circuit to minimize temperature gradients.

APPLICATIONS INFORMATION

Table 6. Partial List of LTC Precision References Recommended for Use with the LTC2756 with Relevant Specifications

REFERENCE	INITIAL TOLERANCE	TEMPERATURE DRIFT	0.1Hz to 10Hz NOISE
LT1019A-5, LT1019A-10	±0.05% max	5ppm/°C max	$12\mu V_{P-P}$
LT1236A-5, LT1236A-10	±0.05% max	5ppm/°C max	$3\mu V_{P-P}$
LT1460A-5, LT1460A-10	±0.075% max	10ppm/°C max	$20\mu V_{P-P}$
LT1790A-2.5	±0.05% max	10ppm/°C max	$12\mu V_{P-P}$
LTC6652A-5	±0.05% max	5ppm/°C max	$2.8ppm_{P-P}$
LTC6655A-2.5 LTC6655A-5	±0.025% max	2ppm/°C max	$0.25ppm_{P-P}$

As precision DAC applications move to 18-bit performance, reference output voltage noise may contribute a dominant share of the system's noise floor. This in turn can degrade system dynamic range and signal-to-noise ratio. Care should be exercised in selecting a voltage reference with as low an output noise voltage as practical for the system resolution desired. Precision voltage references like the LT1236 or LTC6655 produce low output noise in the 0.1Hz to 10Hz region, well below the 18-bit LSB level in 5V or 10V full-scale systems. However, as the circuit bandwidths increase, filtering the output of the reference may be required to minimize output noise.

Grounding

As with any high-resolution converter, clean grounding is important. A low-impedance analog ground plane is necessary, as are star grounding techniques. Keep the board layer used for star ground continuous to minimize ground resistances; that is, use the star-ground concept without using separate star traces. The I_{OUT2} pin is of particular importance; INL will be degraded by the code-dependent currents carried by I_{OUT2} if voltage drops to ground are allowed to develop. The best strategy here is to tie the pins to the star ground plane by multiple vias located directly underneath the part. Alternatively, the pin may be routed to the star ground point if necessary; route a trace of no more than 30 squares of 1oz copper.

In the rare case in which neither of these alternatives is practicable, a force/sense amplifier should be used as a ground buffer (see Figure 4). Note, however, that the voltage offset of the ground buffer amp directly contributes to the effects on accuracy specified in Table 4 under 'V_{OS1}'. The combined effects of the offsets can be calculated by substituting the total offset from I_{OUT1} to I_{OUT2} for V_{OS1} in the equations.

APPLICATIONS INFORMATION

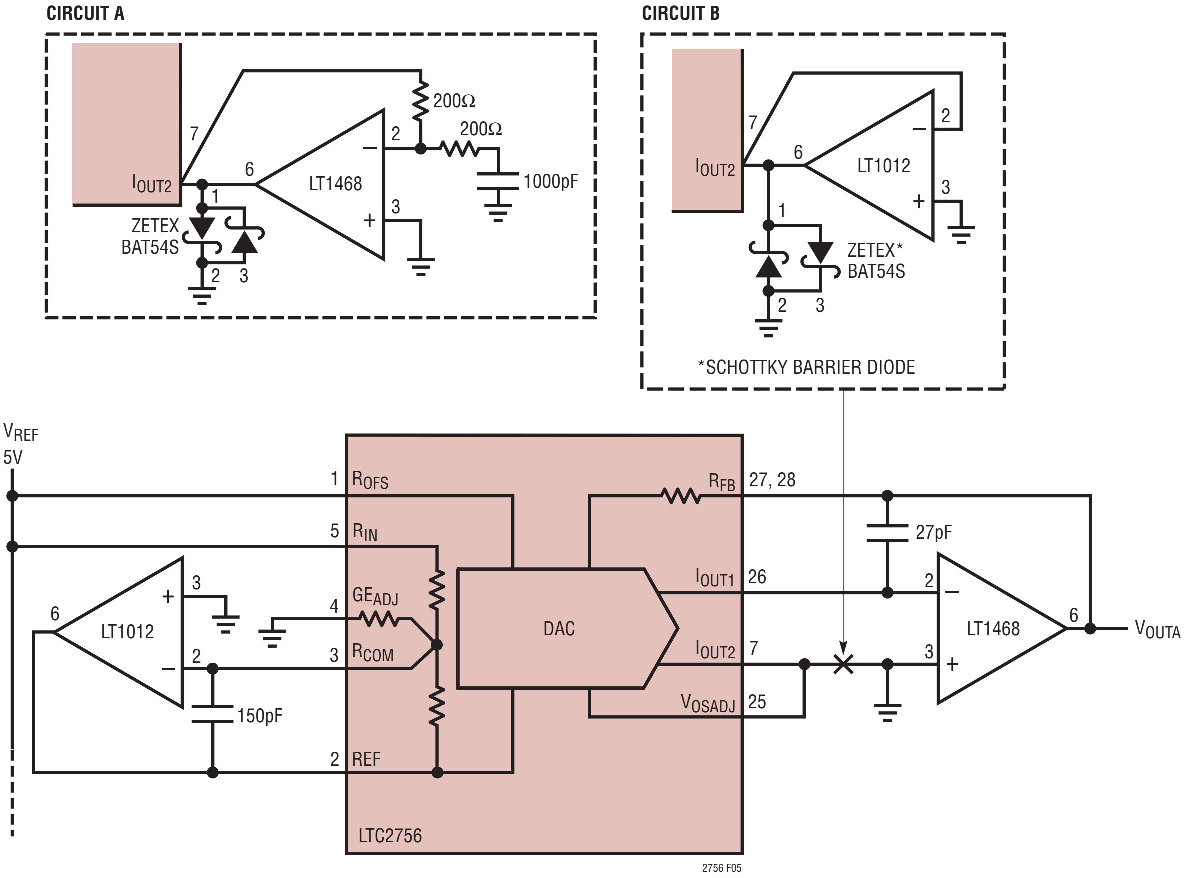
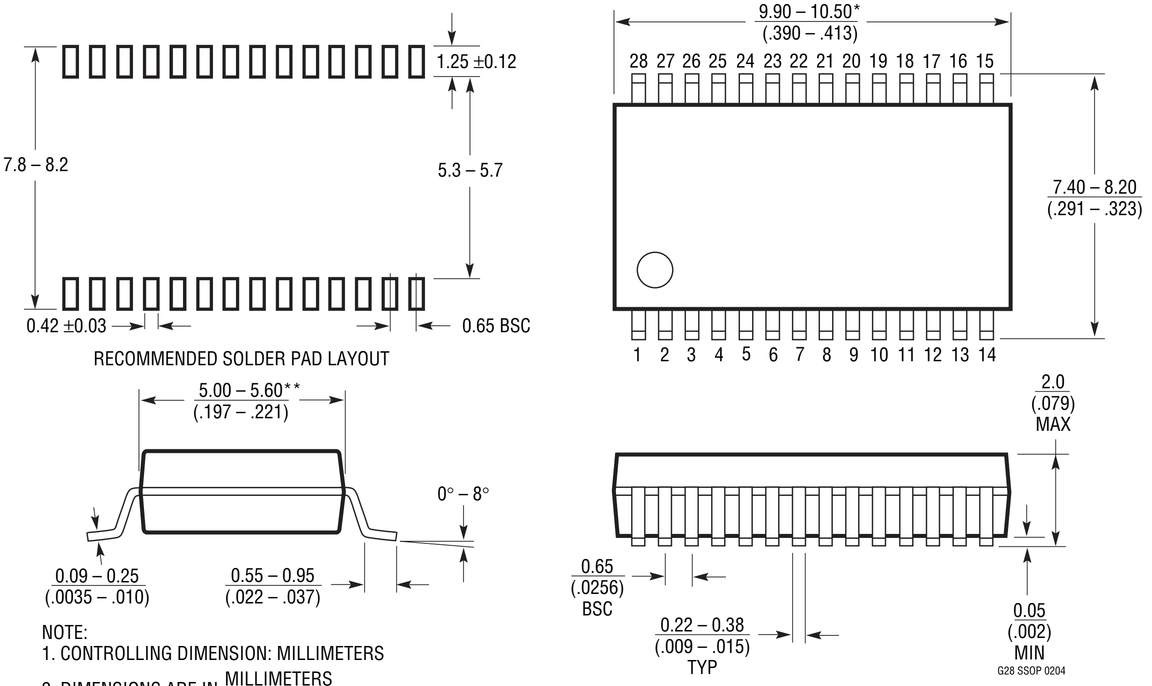


Figure 4. If a Low-Impedance GND Plane Is Unavailable, Drive I_{OUT2} with a Force/Sense Amplifier As Shown. Use Circuit A to Minimize Impact on Settling Time, or Circuit B for Lower Power Consumption and Better Accuracy

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2756#packaging for the most recent package drawings.

G Package
28-Lead Plastic SSOP (5.3mm)
(Reference LTC DWG # 05-08-1640)



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .152mm (.006") PER SIDE
**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED .254mm (.010") PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	12/16	Updated amplifier part numbers.	19, 24

TYPICAL APPLICATION

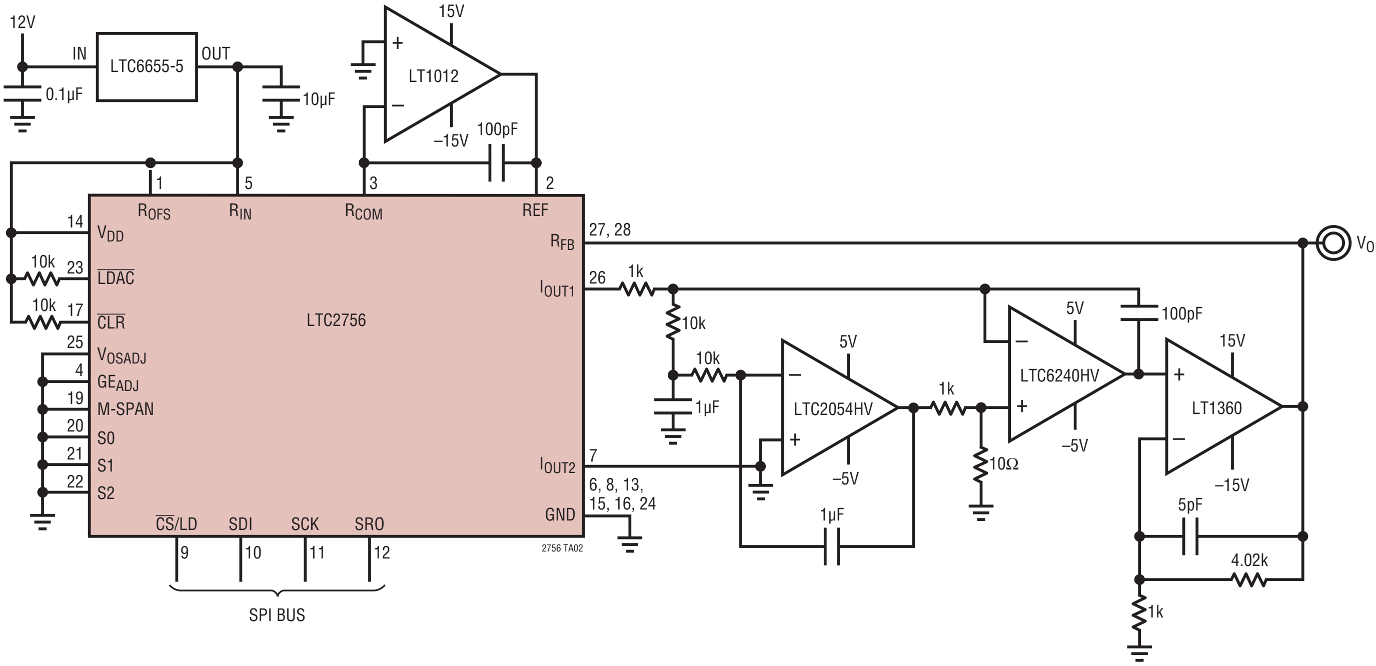


Figure 5. Composite Amplifier Provides Both 18-Bit Precision and Fast Settling

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2757	Single Parallel 18-Bit I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package
LTC1592	Single Serial 16-/14-/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 16-Lead SSOP Package
LTC2751	Single Parallel 16-/14-/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 5mm × 7mm QFN-38 Package
LTC1597/LTC1591	Single Parallel 16-/14-Bit I_{OUT} DACs	±1LSB INL/DNL, Integrated 4-Quadrant Resistors, 28-Lead SSOP Package
LTC2758	Dual Serial 18-Bit I_{OUT} SoftSpan DAC	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 7mm LQFP-48 Package
LTC2754	Quad Serial 16-/12-Bit I_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, 7mm × 8mm QFN-52 Package
LTC2704	Quad Serial 16-/14-/12-Bit V_{OUT} SoftSpan DACs	±1LSB INL/DNL, Software-Selectable Ranges, Integrated Amplifiers
LTC2641/LTC2642	16-/14-/12-Bit V_{OUT} DACs	±1LSB INL/DNL, 0.5nV•s Glitch, 1µs Settling, 3mm × 3mm DFN
References		
LTC6655A-2.5/ LTC6655A-5	Low Drift Precision Buffered Reference	0.025% Max Tolerance, 2ppm/°C Max, 0.25ppm_{P-P} 0.1Hz to 10Hz Noise
LT1236A-5/ LT1236A-10	Precision Reference	0.05% Max Tolerance, 5ppm/°C Max, 3µV_{P-P} 0.1Hz to 10Hz Noise
LT1460A-5/ LT1460A-10	Micropower Precision Series Reference	0.075% Max Tolerance, 10ppm/°C Max, 20µV_{P-P} 0.1Hz to 10Hz Noise
LT1790A-2.5	Micropower Low Dropout Reference	0.05% Max Tolerance, 10ppm/°C Max, 12µV_{P-P} 0.1Hz to 10Hz Noise
LTC6652A-5	Precision Low Drift Low Noise Buffered Reference	0.05% Max Tolerance, 5ppm/°C Max, 2.8ppm_{P-P} 0.1Hz to 10Hz Noise
Amplifiers		
LTC1150	Zero-Drift Op Amp with Internal Capacitors	10µV Max Offset, ±16V High Voltage Operation, 1.8µV_{P-P} Noise
LT1012	Precision Op Amp	25µV Max Offset, 100pA Max Input Current, 0.5µV_{P-P} Noise, 380µA Supply Current
LT1001	Precision Op Amp	25µV Max Offset, 0.3µV_{P-P} Noise, High Output Drive
LT1468	Single 16-Bit Accurate Op Amp	900ns Settling, 90MHz GBW, 22V/µs Slew Rate, 75µV Max Offset

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