

AD9760
FEATURES

Member of Pin-Compatible TxDAC Product Family
125 MSPS Update Rate
10-Bit Resolution
Excellent Spurious Free Dynamic Range Performance
SFDR to Nyquist @ 40 MHz Output: 52 dBc
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 175 mW @ 5 V to 45 mW @ 3 V
Power-Down Mode: 25 mW @ 5 V
On-Chip 1.20 V Reference
Single +5 V or +3 V Supply Operation
Packages: 28-Lead SOIC and TSSOP
Edge-Triggered Latches

APPLICATIONS

Communication Transmit Channel:
Basestations
Set Top Boxes
Digital Radio Link
Direct Digital Synthesis (DDS)
Instrumentation

PRODUCT DESCRIPTION

The AD9760 and AD9760-50 are the 10-bit resolution members of the TxDAC series of high performance, low power CMOS digital-to-analog converters (DACs). The AD9760-50 is a lower performance option that is guaranteed and specified for 50 MSPS operation. The TxDAC family that consists of pin compatible 8-, 10-, 12- and 14-bit DACs is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package and pinout, thus providing an upward or downward component selection path based on performance, resolution and cost. Both the AD9760 and AD9760-50 offer exceptional ac and dc performance while supporting update rates up to 125 MSPS and 60 MSPS respectively.

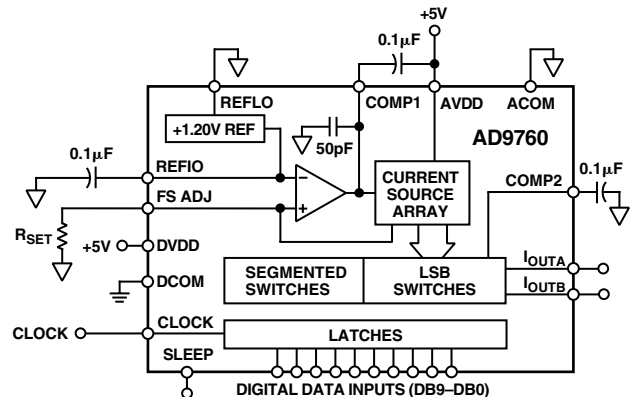
The AD9760's flexible single-supply operating range of 2.7 V to 5.5 V and low power dissipation are well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 45 mW without a significant degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 25 mW.

The AD9760 is manufactured on an advanced CMOS process. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated bandgap reference have been integrated to provide a complete monolithic DAC solution. Flexible supply options support +3 V and +5 V CMOS logic families.

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FUNCTIONAL BLOCK DIAGRAM


The AD9760 is a current-output DAC with a nominal full-scale output current of 20 mA and > 100 kΩ output impedance. Differential current outputs are provided to support single-ended or differential applications. Matching between the two current outputs ensures enhanced dynamic performance in a differential output configuration. The current outputs may be tied directly to an output resistor to provide two complementary, single-ended voltage outputs or fed directly into a transformer. The output voltage compliance range is 1.25 V.

The on-chip reference and control amplifier are configured for maximum accuracy and flexibility. The AD9760 can be driven by the on-chip reference or by a variety of external reference voltages. The internal control amplifier that provides a wide (>10:1) adjustment span allows the AD9760 full-scale current to be adjusted over a 2 mA to 20 mA range while maintaining excellent dynamic performance. Thus, the AD9760 may operate at reduced power levels or be adjusted over a 20 dB range to provide additional gain ranging capabilities.

The AD9760 is available in a 28-lead SOIC and TSSOP packages. It is specified for operation over the industrial temperature range.

PRODUCT HIGHLIGHTS

1. The AD9760 is a member of the TxDAC product family that provides an upward or downward component selection path based on resolution (8 to 14 bits), performance and cost.
2. Manufactured on a CMOS process, the AD9760 uses a proprietary switching technique that enhances dynamic performance beyond what was previously attainable by higher power/cost bipolar or BiCMOS devices.
3. On-chip, edge-triggered input CMOS latches interface readily to +3 V and +5 V CMOS logic families. The AD9760 can support update rates up to 125 MSPS.
4. A flexible single-supply operating range of 2.7 V to 5.5 V and a wide full-scale current adjustment span of 2 mA to 20 mA allow the AD9760 to operate at reduced power levels.
5. The current output(s) of the AD9760 can be easily configured for various single-ended or differential circuit topologies.

AD9760/AD9760-50—SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, unless otherwise noted)

Parameter	Min	Typ	Max	Units
RESOLUTION	10			Bits
DC ACCURACY ¹				
Integral Linearity Error (INL)	-1.0	±0.5	+1.0	LSB
Differential Nonlinearity (DNL)	-0.5	±0.25	+0.5	LSB
MONOTONICITY	Guaranteed Over Specified Temperature Range			
ANALOG OUTPUT				
Offset Error	-0.025		+0.025	% of FSR
Gain Error (Without Internal Reference)	-10	±2	+10	% of FSR
Gain Error (With Internal Reference)	-10	±1	+10	% of FSR
Full-Scale Output Current ²	2.0		20.0	mA
Output Compliance Range	-1.0		1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.08	1.20	1.32	V
Reference Output Current ³		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance		1		MΩ
Small Signal Bandwidth (w/o C _{COMP1}) ⁴		1.4		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD ⁵	2.7	5.0	5.5	V
DVDD	2.7	5.0	5.5	V
Analog Supply Current (I _{AVDD})		25	30	mA
Digital Supply Current (I _{DVDD}) ⁶		3	5	mA
Supply Current Sleep Mode (I _{AVDD})			8.5	mA
Power Dissipation ⁶ (5 V, I _{OUTFS} = 20 mA)		140	175	mW
Power Dissipation ⁷ (5 V, I _{OUTFS} = 20 mA)		190		mW
Power Dissipation ⁷ (3 V, I _{OUTFS} = 2 mA)		45		mW
Power Supply Rejection Ratio—AVDD	-0.04		+0.04	% of FSR/V
Power Supply Rejection Ratio—DVDD	-0.025		+0.025	% of FSR/V
OPERATING RANGE	-40		+85	°C

NOTES

¹Measured at I_{OUTA}, driving a virtual ground.

²Nominal full-scale current, I_{OUTFS}, is 32 × the I_{REF} current.

³Use an external buffer amplifier to drive any external load.

⁴Reference bandwidth is a function of external cap at COMP1 pin and signal level. Refer to Figure 41.

⁵For operation below 3 V, it is recommended that the output current be reduced to 12 mA or less to maintain optimum performance.

⁶Measured at f_{CLOCK} = 50 MSPS and f_{OUT} = 1.0 MHz.

⁷Measured as unbuffered voltage output into 50 Ω R_{LOAD} at I_{OUTA} and I_{OUTB}, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS (T_{MIN} to T_{MAX} , $AVDD = +5\text{ V}$, $DVDD = +5\text{ V}$, $I_{OUTFS} = 20\text{ mA}$, Differential Transformer Coupled Output, $50\ \Omega$ Doubly Terminated, unless otherwise noted)

Model Parameter	AD9760			AD9760-50			Units
	Min	Typ	Max	Min	Typ	Max	
DYNAMIC PERFORMANCE							
Maximum Output Update Rate (f_{CLOCK})	125			50	60		MSPS
Output Settling Time (t_{ST}) (to 0.1%) ¹		35			35		ns
Output Propagation Delay (t_{PD})		1			1		ns
Glitch Impulse		5			5		pV-s
Output Rise Time (10% to 90%) ¹		2.5			2.5		ns
Output Fall Time (10% to 90%) ¹		2.5			2.5		ns
Output Noise ($I_{OUTFS} = 20\text{ mA}$)		50			50		$\text{pA}/\sqrt{\text{Hz}}$
Output Noise ($I_{OUTFS} = 2\text{ mA}$)		30			30		$\text{pA}/\sqrt{\text{Hz}}$
AC LINEARITY							
Spurious-Free Dynamic Range to Nyquist							
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 1.00\text{ MHz}$							
$T_A = +25^\circ\text{C}$	70	73		68	73		dBc
T_{MIN} to T_{MAX}	68			66			dBc
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 2.51\text{ MHz}$		73			73		dBc
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 5.02\text{ MHz}$		68			68		dBc
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 20.2\text{ MHz}$		55			55		dBc
$f_{CLOCK} = 100\text{ MSPS}$; $f_{OUT} = 2.51\text{ MHz}$		74			N/A		dBc
$f_{CLOCK} = 100\text{ MSPS}$; $f_{OUT} = 5.04\text{ MHz}$		68			N/A		dBc
$f_{CLOCK} = 100\text{ MSPS}$; $f_{OUT} = 20.2\text{ MHz}$		60			N/A		dBc
$f_{CLOCK} = 100\text{ MSPS}$; $f_{OUT} = 40.4\text{ MHz}$		52			N/A		dBc
Spurious-Free Dynamic Range within a Window							
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 1.00\text{ MHz}$							
$T_A = +25^\circ\text{C}$	74	78		72	78		dBc
T_{MIN} to T_{MAX}	72			70			dBc
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 5.02\text{ MHz}$; 2 MHz Span		76			76		dBc
$f_{CLOCK} = 100\text{ MSPS}$; $f_{OUT} = 5.04\text{ MHz}$; 4 MHz Span		76			N/A		dBc
Total Harmonic Distortion							
$f_{CLOCK} = 50\text{ MSPS}$; $f_{OUT} = 1.00\text{ MHz}$							
$T_A = +25^\circ\text{C}$		-76	-73		-76	-70	dBc
T_{MIN} to T_{MAX}			-71			-68	dBc
$f_{CLOCK} = 50\text{ MHz}$; $f_{OUT} = 2.00\text{ MHz}$		-71			-71		dBc
$f_{CLOCK} = 100\text{ MHz}$; $f_{OUT} = 2.00\text{ MHz}$		-71			N/A		dBc

NOTES

¹Measured single ended into $50\ \Omega$ load.

Specifications subject to change without notice.

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DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX} , AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA unless otherwise noted)

Parameter	Min	Typ	Max	Units
DIGITAL INPUTS				
Logic "1" Voltage @ DVDD = +5 V	3.5	5		V
Logic "1" Voltage @ DVDD = +3 V	2.1	3		V
Logic "0" Voltage @ DVDD = +5 V		0	1.3	V
Logic "0" Voltage @ DVDD = +3 V		0	0.9	V
Logic "1" Current	-10		+10	μ A
Logic "0" Current	-10		+10	μ A
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	3.5			ns

Specification subject to change without notice.

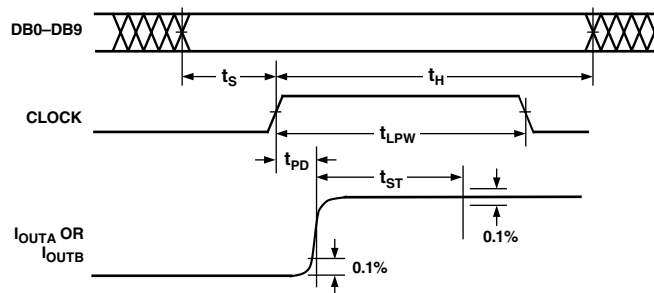


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min Max		Units
		Min	Max	
AVDD	ACOM	-0.3	+6.5	V
DVDD	DCOM	-0.3	+6.5	V
ACOM	DCOM	-0.3	+0.3	V
AVDD	DVDD	-6.5	+6.5	V
CLOCK, SLEEP	DCOM	-0.3	DVDD + 0.3	V
Digital Inputs	DCOM	-0.3	DVDD + 0.3	V
I_{OUTA} , I_{OUTB}	ACOM	-1.0	AVDD + 0.3	V
COMP1, COMP2	ACOM	-0.3	AVDD + 0.3	V
REFIO, FSADJ	ACOM	-0.3	AVDD + 0.3	V
REFLO	ACOM	-0.3	+0.3	V
Junction Temperature			+150	$^{\circ}$ C
Storage Temperature		-65	+150	$^{\circ}$ C
Lead Temperature (10 sec)			+300	$^{\circ}$ C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9760 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ORDERING GUIDE

Model	Temperature Range	Package Descriptions	Package Options
AD9760AR	-40 $^{\circ}$ C to +85 $^{\circ}$ C	28-Lead 300 mil SOIC	R-28
AD9760ARU	-40 $^{\circ}$ C to +85 $^{\circ}$ C	28-Lead 170 mil TSSOP	RU-28
AD9760AR50	-40 $^{\circ}$ C to +85 $^{\circ}$ C	28-Lead 300 mil SOIC	R-28
AD9760ARU50	-40 $^{\circ}$ C to +85 $^{\circ}$ C	28-Lead 170 mil TSSOP	RU-28
AD9760-EB	Evaluation Board		

THERMAL CHARACTERISTICS

Thermal Resistance

28-Lead 300 mil (7.5 mm) SOIC

$$\theta_{JA} = 71.4^{\circ}\text{C/W}$$

$$\theta_{JC} = 23^{\circ}\text{C/W}$$

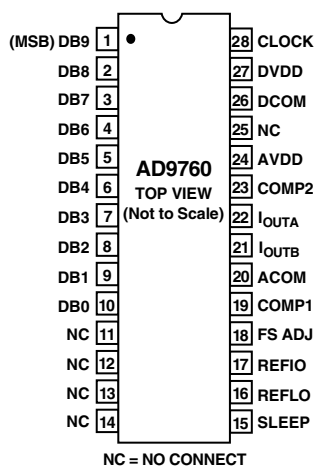
28-Lead 170 mil (4.4 mm) TSSOP

$$\theta_{JA} = 97.9^{\circ}\text{C/W}$$

$$\theta_{JC} = 14.0^{\circ}\text{C/W}$$



PIN CONFIGURATION



PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description
1	DB9	Most Significant Data Bit (MSB).
2–9	DB8–DB1	Data Bits 1–8.
10	DB0	Least Significant Data Bit (LSB).
11–14, 25	NC	No Internal Connection.
15	SLEEP	Power-Down Control Input. Active High. Contains active pull-down circuit, thus may be left unterminated if not used.
16	REFLO	Reference Ground when Internal 1.2 V Reference Used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., Tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., Tie REFLO to ACOM). Requires 0.1 μ F capacitor to ACOM when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust.
19	COMP1	Bandwidth/Noise Reduction Node. Add 0.1 μ F to AVDD for optimum performance.
20	ACOM	Analog Common.
21	I _{OUTB}	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	I _{OUTA}	DAC Current Output. Full-scale current when all data bits are 1s.
23	COMP2	Internal Bias Node for Switch Driver Circuitry. Decouple to ACOM with 0.1 μ F capacitor.
24	AVDD	Analog Supply Voltage (+2.7 V to +5.5 V).
26	DCOM	Digital Common.
27	DVDD	Digital Supply Voltage (+2.7 V to +5.5 V).
28	CLOCK	Clock Input. Data latched on positive edge of clock.

Typical AC Characterization Curves @ +5 V Supplies

(AVDD = +5 V, DVDD = +5 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted)

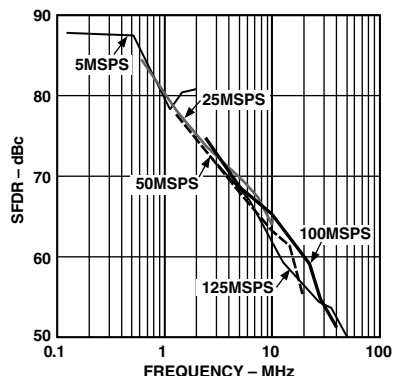


Figure 3. SFDR vs. f_{OUT} @ 0 dBFS

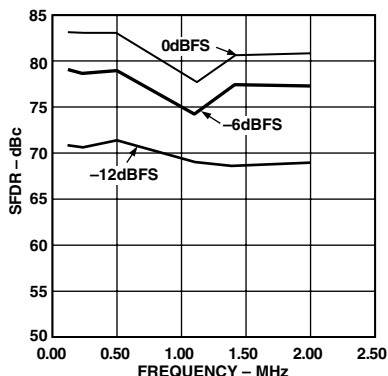


Figure 4. SFDR vs. f_{OUT} @ 5 MSPS

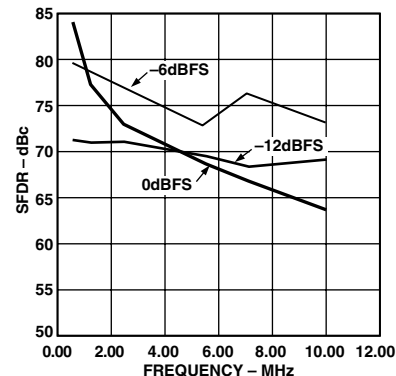


Figure 5. SFDR vs. f_{OUT} @ 25 MSPS

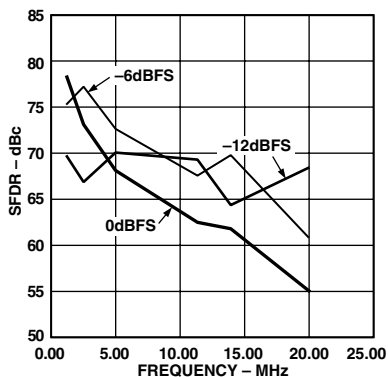


Figure 6. SFDR vs. f_{OUT} @ 50 MSPS

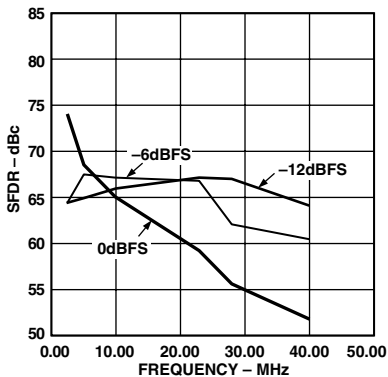


Figure 7. SFDR vs. f_{OUT} @ 100 MSPS

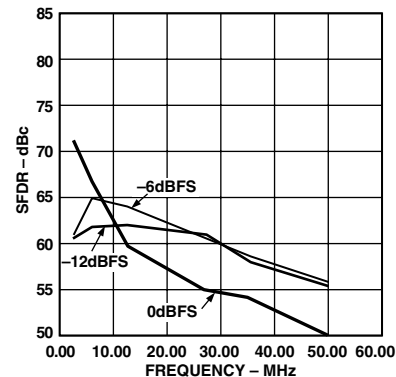


Figure 8. SFDR vs. f_{OUT} @ 125 MSPS

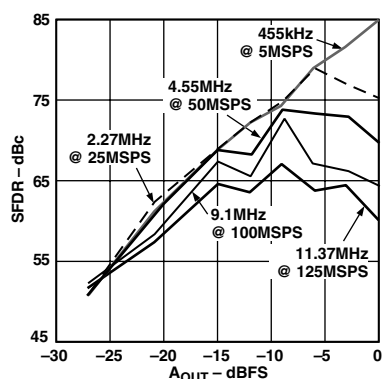


Figure 9. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

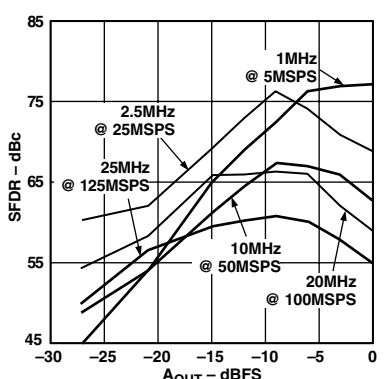


Figure 10. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

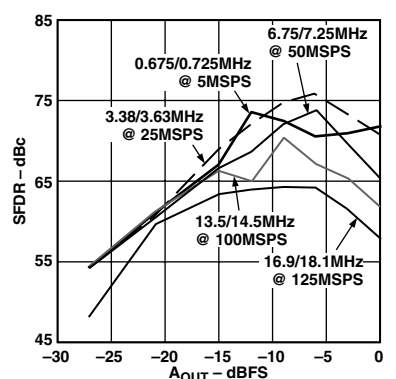


Figure 11. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/7$

AD9760

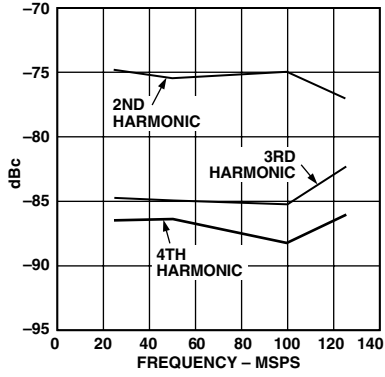


Figure 12. THD vs. f_{CLOCK} @ $f_{\text{OUT}} = 2 \text{ MHz}$

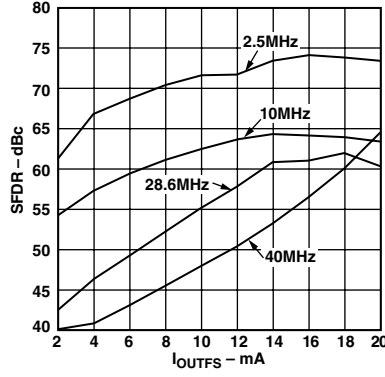


Figure 13. SFDR vs. f_{OUT} and I_{OUTFS} @ 100 MSPS, 0 dBFS

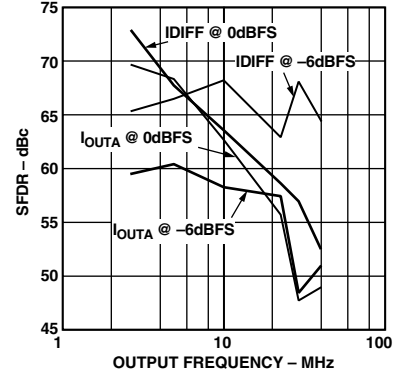


Figure 14. Differential vs. Single-Ended SFDR vs. f_{OUT} @ 100 MSPS

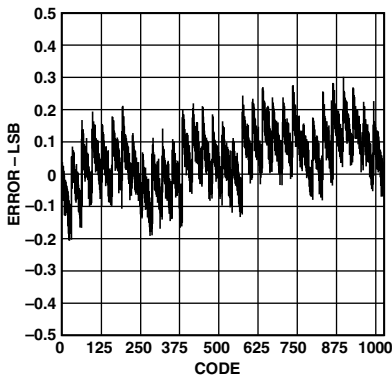


Figure 15. Typical INL

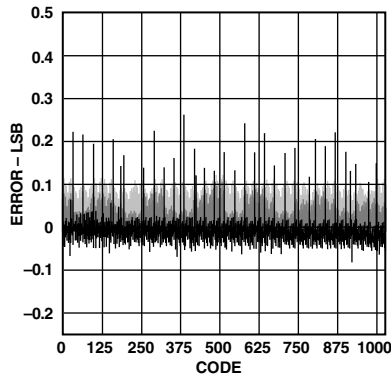


Figure 16. Typical DNL

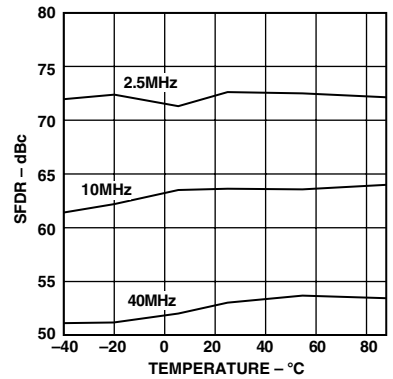


Figure 17. SFDR vs. Temperature @ 100 MSPS, 0 dBFS

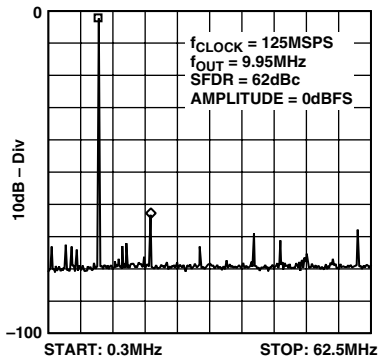


Figure 18. Single-Tone SFDR

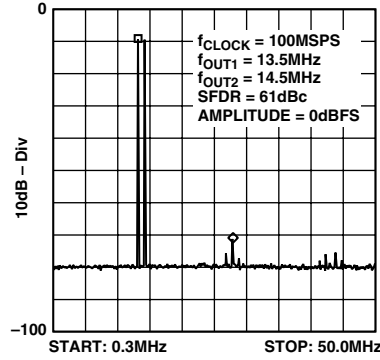


Figure 19. Dual-Tone SFDR

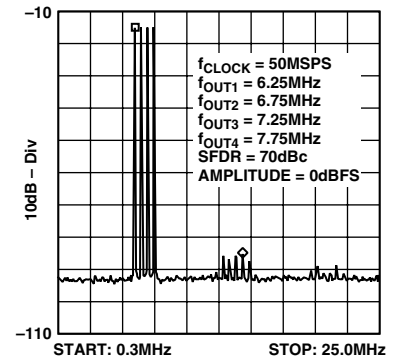


Figure 20. Four-Tone SFDR

Typical AC Characterization Curves @ +3 V Supplies

(AVDD = +3 V, DVDD = +3 V, I_{OUTFS} = 20 mA, 50 Ω Doubly Terminated Load, Differential Output, T_A = +25°C, SFDR up to Nyquist, unless otherwise noted)

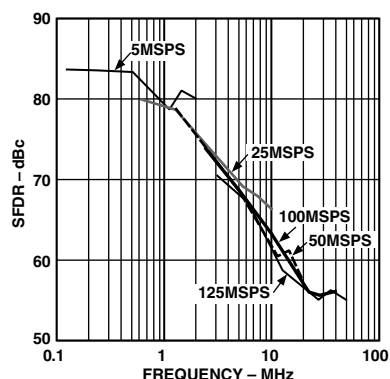


Figure 21. SFDR vs. f_{OUT} @ 0 dBFS

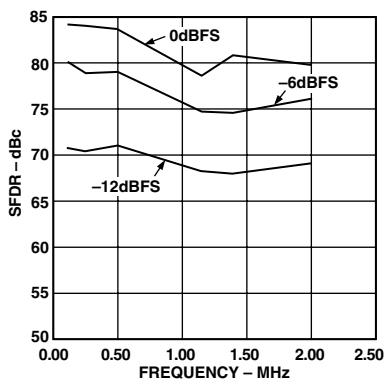


Figure 22. SFDR vs. f_{OUT} @ 5 MSPS

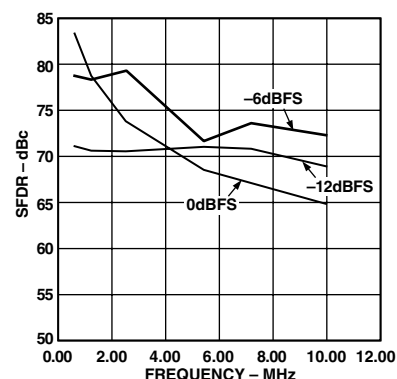


Figure 23. SFDR vs. f_{OUT} @ 25 MSPS

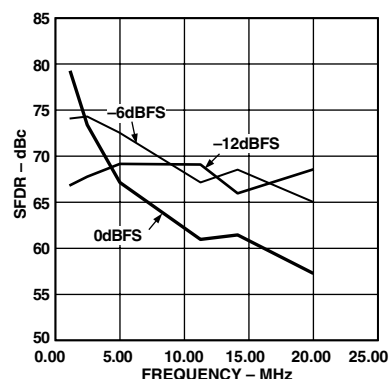


Figure 24. SFDR vs. f_{OUT} @ 50 MSPS

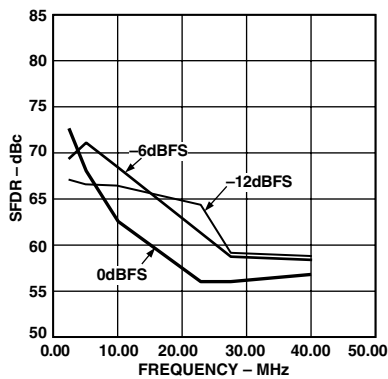


Figure 25. SFDR vs. f_{OUT} @ 100 MSPS

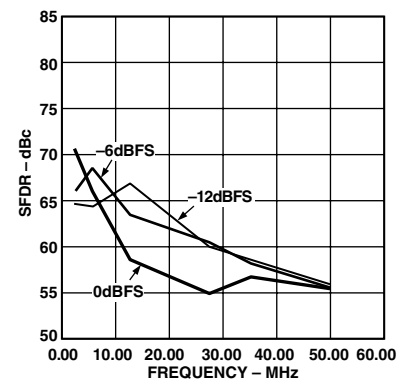


Figure 26. SFDR vs. f_{OUT} @ 125 MSPS

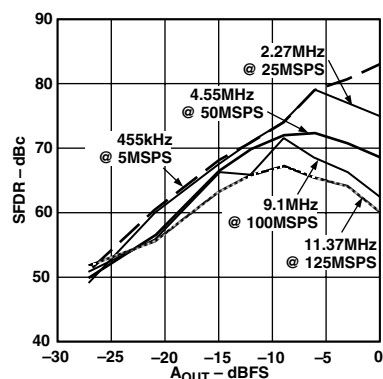


Figure 27. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

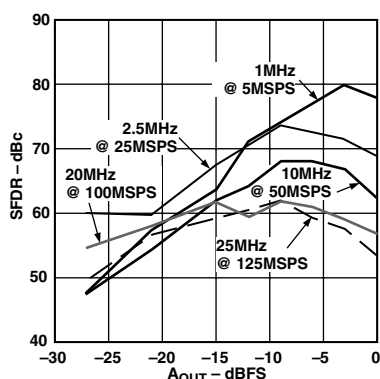


Figure 28. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

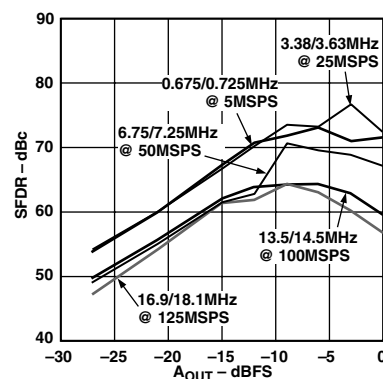


Figure 29. Dual-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/7$

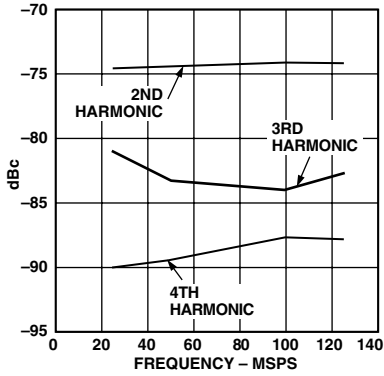


Figure 30. THD vs. f_{CLOCK}
 $f_{\text{OUT}} = 2 \text{ MHz}$

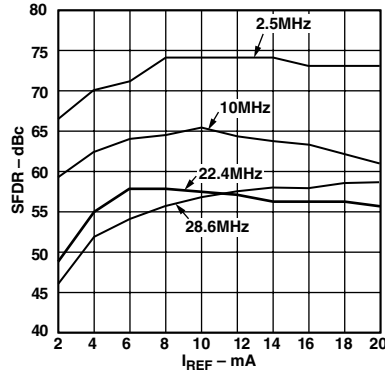


Figure 31. SFDR vs. f_{OUT} and I_{OUTFS}
@ 100 MSPS, 0 dBFS

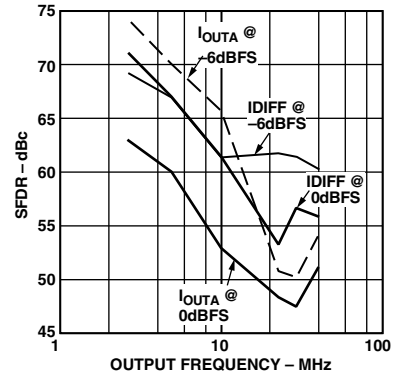


Figure 32. Differential vs. Single Ended SFDR vs. f_{OUT} @ 100 MSPS

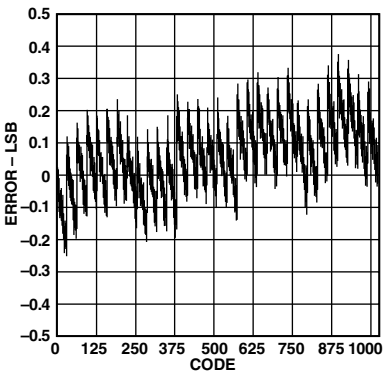


Figure 33. Typical INL

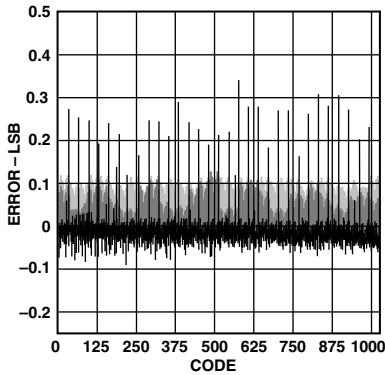


Figure 34. Typical DNL

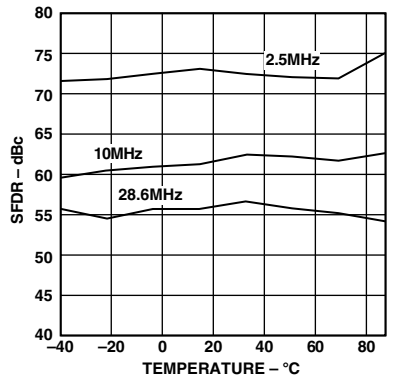


Figure 35. SFDR vs. Temperature
@ 100 MSPS, 0 dBFS

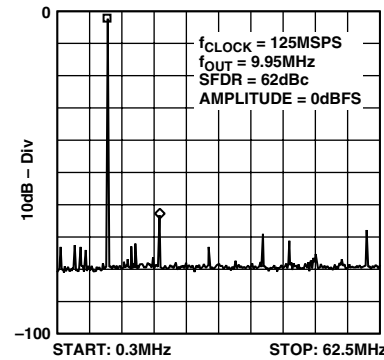


Figure 36. Single-Tone SFDR

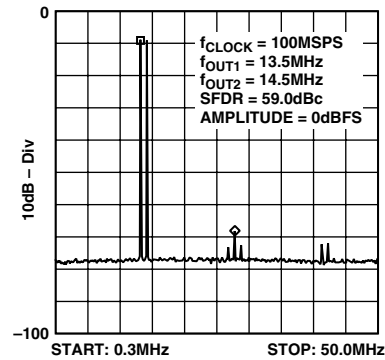


Figure 37. Dual-Tone SFDR

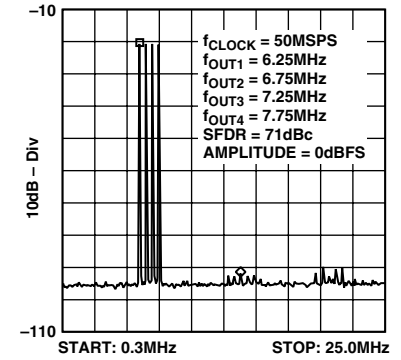


Figure 38. Four-Tone SFDR

FUNCTIONAL DESCRIPTION

Figure 39 shows a simplified block diagram of the AD9760. The AD9760 consists of a large PMOS current source array that is capable of providing up to 20 mA of total current. The array is divided into 31 equal currents that make up the 5 most significant bits (MSBs). The next 4 bits or middle bits consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs is a binary weighted fraction of the middle-bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., I_{OUTA} or I_{OUTB}) via PMOS differential current switches. The switches are based on a new architecture that drastically improves distortion performance. This new switch architecture reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9760 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 2.7 volt to 5.5 volt range. The digital section, which is capable of operating up to a 125 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.20 V bandgap voltage reference and a reference control amplifier.

The full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is mirrored over to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is thirty-two times the value of I_{REF}.

DAC TRANSFER FUNCTION

The AD9760 provides complementary current outputs, I_{OUTA} and I_{OUTB}. I_{OUTA} will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 1023) while I_{OUTB}, the complementary output, provides no current. The current output appearing at I_{OUTA} and I_{OUTB} is a function of both the input code and I_{OUTFS} and can be expressed as:

$$I_{OUTA} = (DAC\ CODE/1024) \times I_{OUTFS} \quad (1)$$

$$I_{OUTB} = (1023 - DAC\ CODE)/1024 \times I_{OUTFS} \quad (2)$$

where DAC CODE = 0 to 1023 (i.e., Decimal Representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO} and external resistor R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \quad (3)$$

where $I_{REF} = V_{REFIO}/R_{SET}$ (4)

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTA} and I_{OUTB} should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by I_{OUTA} or I_{OUTB} as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the I_{OUTA} and I_{OUTB} nodes is simply:

$$V_{OUTA} = I_{OUTA} \times R_{LOAD} \quad (5)$$

$$V_{OUTB} = I_{OUTB} \times R_{LOAD} \quad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

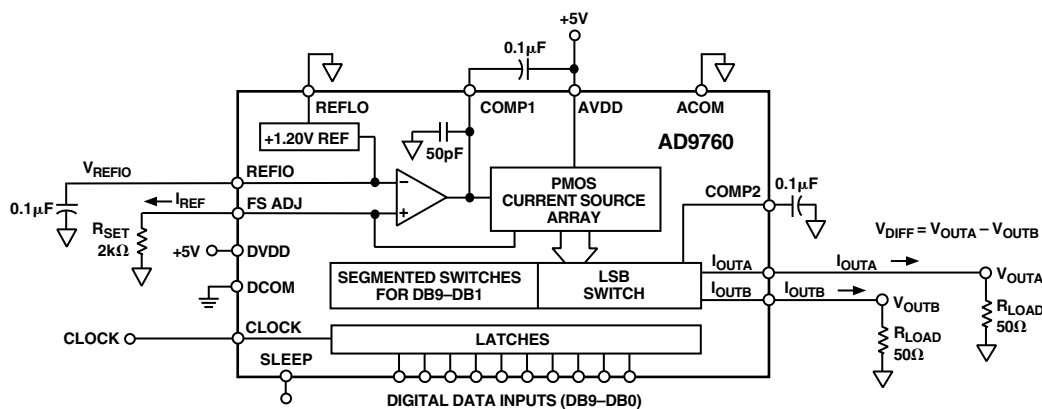


Figure 39. Functional Block Diagram

AD9760

The differential voltage, V_{DIFF} , appearing across I_{OUTA} and I_{OUTB} is:

$$V_{DIFF} = (I_{OUTA} - I_{OUTB}) \times R_{LOAD} \quad (7)$$

Substituting the values of I_{OUTA} , I_{OUTB} and I_{REF} ; V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2 \text{ DAC CODE} - 1023)/1024\} \times (32 R_{LOAD}/R_{SET}) \times V_{REFIO} \quad (8)$$

These last two equations highlight some of the advantages of operating the AD9760 differentially. First, the differential operation will help cancel common-mode error sources associated with I_{OUTA} and I_{OUTB} such as noise, distortion and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF} , is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9760 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

REFERENCE OPERATION

The AD9760 contains an internal 1.20 V bandgap reference that can be easily disabled and overridden by an external reference. REFIO serves as either an *input* or *output* depending on whether the internal or an external reference is selected. If REFLO is tied to ACOM, as shown in Figure 40, the internal reference is activated and REFIO provides a 1.20 V output. In this case, the internal reference *must* be compensated externally with a ceramic chip capacitor of 0.1 μ F or greater from REFIO to REFLO. Also, REFIO should be buffered with an external amplifier having an input bias current less than 100 nA if any additional loading is required.

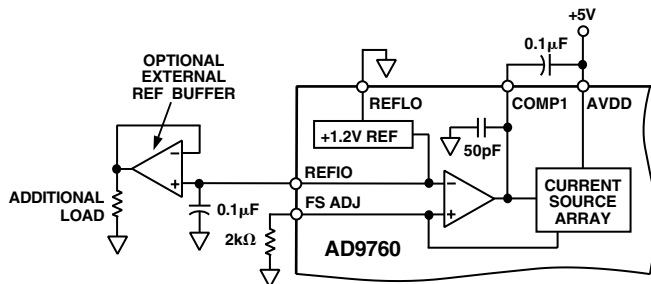


Figure 40. Internal Reference Configuration

The internal reference can be disabled by connecting REFLO to AVDD. In this case, an external reference may be applied to REFIO as shown in Figure 41. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 μ F compensation capacitor is not required since the internal reference is disabled, and the high input impedance (i.e., 1 M Ω) of REFIO minimizes any loading of the external reference.

REFERENCE CONTROL AMPLIFIER

The AD9760 also contains an internal control amplifier that is used to regulate the DAC's full-scale output current, I_{OUTFS} . The control amplifier is configured as a V-I converter as shown in Figure 41, so that its current output, I_{REF} , is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET} , as stated in Equation 4. I_{REF} is copied over to the segmented current sources with the proper scaling factor to set I_{OUTFS} as stated in Equation 3.

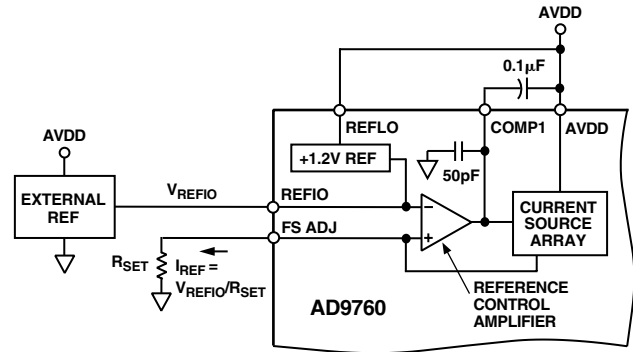


Figure 41. External Reference Configuration

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 μ A and 625 μ A. The wide adjustment span of I_{OUTFS} provides several application benefits. The first benefit relates directly to the power dissipation of the AD9760, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second benefit relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 1.4 MHz and can be reduced by connecting an external capacitor between COMP1 and AVDD. The output of the control amplifier, COMP1, is internally compensated via a 50 pF capacitor that limits the control amplifier small-signal bandwidth and reduces its output impedance. Any additional external capacitance further limits the bandwidth and acts as a filter to reduce the noise contribution from the reference amplifier. Figure 42 shows the relationship between the external capacitor and the small signal -3 dB bandwidth of the reference amplifier. Since the -3 dB bandwidth corresponds to the dominant pole, and hence the time constant, the settling time of the control amplifier to a stepped reference input response can be approximated.

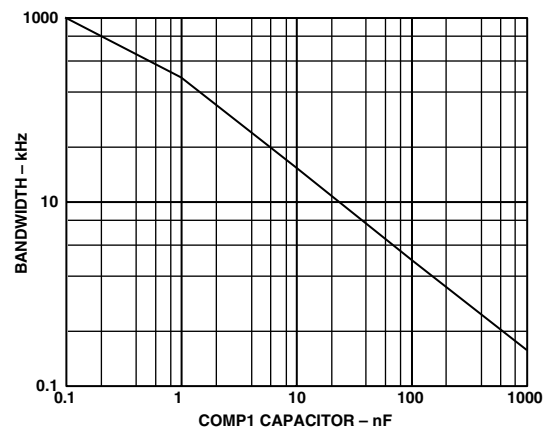


Figure 42. External COMP1 Capacitor vs. -3 dB Bandwidth

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The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of I_{OUTA} and I_{OUTB} are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9760 to provide the required power and voltage levels to different loads. Refer to Applying the AD9760 section for examples of various output configurations.

The output impedance of I_{OUTA} and I_{OUTB} is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 k Ω in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining I_{OUTA} and/or I_{OUTB} at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note the INL/DNL specifications for the AD9760 are measured with I_{OUTA} maintained at a virtual ground via an op amp.

I_{OUTA} and I_{OUTB} also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of -1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9760.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS} . It degrades slightly from its nominal 1.25 V for an $I_{OUTFS} = 20$ mA to 1.00 V for an $I_{OUTFS} = 2$ mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at I_{OUTA} and I_{OUTB} does not exceed 0.5 V. Applications requiring the AD9760's output (i.e., V_{OUTA} and/or V_{OUTB}) to extend its output compliance range should size R_{LOAD} accordingly. Operation beyond this compliance range will adversely affect the AD9760's linearity performance and subsequently degrade its distortion performance.

DIGITAL INPUTS

The AD9760's digital input consists of 10 data input pins and a clock input pin. The 10-bit parallel data inputs follow standard positive binary coding where DB9 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). I_{OUTA} produces a full-scale output current when all data bits are at Logic 1. I_{OUTB} produces a complementary output with the full-scale current split between the two outputs as a function of the input code.

The digital interface is implemented using an edge-triggered master slave latch. The DAC output is updated following the rising edge of the clock as shown in Figure 1 and is designed to support a clock rate as high as 125 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulse-width. The setup and hold times can also be varied within the

clock cycle as long as the specified minimum times are met although the location of these transition edges may affect digital feedthrough and distortion performance. *Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.*

The digital inputs are CMOS compatible with logic thresholds, $V_{THRESHOLD}$ set to approximately half the digital positive supply (DVDD) or

$$V_{THRESHOLD} = DVDD/2 (\pm 20\%)$$

The internal digital circuitry of the AD9760 is capable of operating over a digital supply range of 2.7 V to 5.5 V. As a result, the digital inputs can also accommodate TTL levels when DVDD is set to accommodate the maximum high level voltage $V_{OH(MAX)}$. A DVDD of 3 V to 3.3 V will typically ensure proper compatibility with most TTL logic families. Figure 46 shows the equivalent digital input circuit for the data and clock inputs. The sleep mode input is similar with the exception that it contains an active pull-down circuit, ensuring that the AD9760 remains enabled if this input is left disconnected.

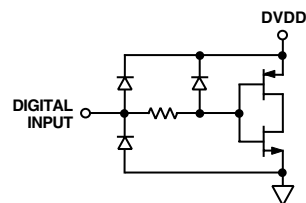


Figure 46. Equivalent Digital Input

Since the AD9760 is capable of being updated up to 125 MSPS, the quality of the clock and data input signals are important in achieving the optimum performance. The drivers of the digital data interface circuitry should be specified to meet the minimum setup and hold times of the AD9760 as well as its required min/max input logic level thresholds. Typically, the selection of the slowest logic family that satisfies the above conditions will result in the lowest data feedthrough and noise.

Digital signal paths should be kept short and run lengths matched to avoid propagation delay mismatch. The insertion of a low value resistor network (i.e., 20 Ω to 100 Ω) between the AD9760 digital inputs and driver outputs may be helpful in reducing any overshooting and ringing at the digital inputs that contribute to data feedthrough. For longer run lengths and high data update rates, strip line techniques with proper termination resistors should be considered to maintain "clean" digital inputs. Also, operating the AD9760 with reduced logic swings and a corresponding digital supply (DVDD) will also reduce data feedthrough.

The external clock driver circuitry should provide the AD9760 with a low jitter clock input meeting the min/max logic levels while providing fast edges. Fast clock edges will help minimize any jitter that will manifest itself as phase noise on a reconstructed waveform. Thus, the clock input should be driven by the fastest logic family suitable for the application.

Note, the clock input could also be driven via a sine wave that is centered around the digital threshold (i.e., $DVDD/2$), and meets the min/max logic threshold. This will typically result in a slight degradation in the phase noise, that becomes more noticeable at higher sampling rates and output frequencies. Also, at higher sampling rates, the 20% tolerance of the digital logic threshold should be considered since it will affect the effective clock duty cycle and subsequently cut into the required data setup and hold times.

SLEEP MODE OPERATION

The AD9760 has a power-down function that turns off the output current and reduces the supply current to less than 8.5 mA over the specified supply range of 2.7 V to 5.5 V and temperature range. This mode can be activated by applying a logic level “1” to the SLEEP pin. This digital input also contains an active pull-down circuit that ensures that the AD9760 remains enabled if this input is left disconnected. The SLEEP input with active pull-down requires $40 \mu A$ of drive current.

The power-up and power-down characteristics of the AD9760 are dependent upon the value of the compensation capacitor connected to COMP1. With a nominal value of 0.1 μF , the AD9760 takes less than 5 μs to power down and approximately 3.25 ms to power back up. Note, the SLEEP MODE should not be used when the external control amplifier is used as shown in Figure 45.

POWER DISSIPATION

The power dissipation, P_D , of the AD9760 is dependent on several factors that include: (1) $AVDD$ and $DVDD$, the power supply voltages; (2) I_{OUTFS} , the full-scale current output; (3) f_{CLOCK} , the update rate; (4) and the reconstructed digital input waveform. The power dissipation is directly proportional to the analog supply current, I_{AVDD} , and the digital supply current, I_{DVDD} . I_{AVDD} is directly proportional to I_{OUTFS} as shown in Figure 47 and is insensitive to f_{CLOCK} .

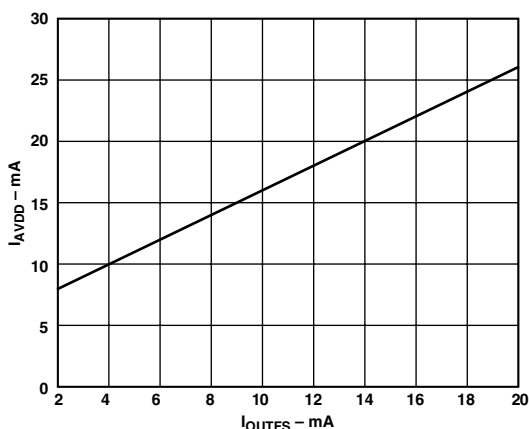


Figure 47. I_{AVDD} vs. I_{OUTFS}

Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK} , and digital supply $DVDD$. Figures 48 and 49 show I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with $DVDD = 5$ V and $DVDD = 3$ V, respectively. Note how I_{DVDD} is reduced by more than a factor of 2 when $DVDD$ is reduced from 5 V to 3 V.

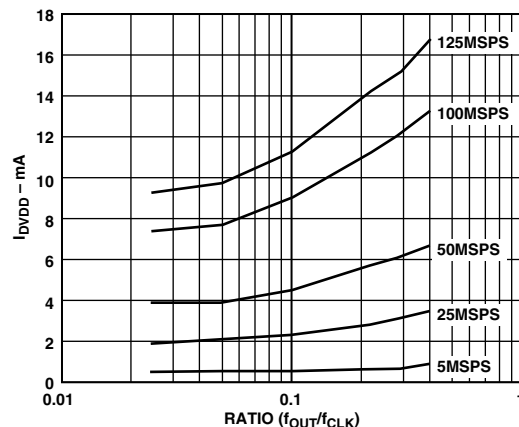


Figure 48. I_{DVDD} vs. Ratio @ $DVDD = 5$ V

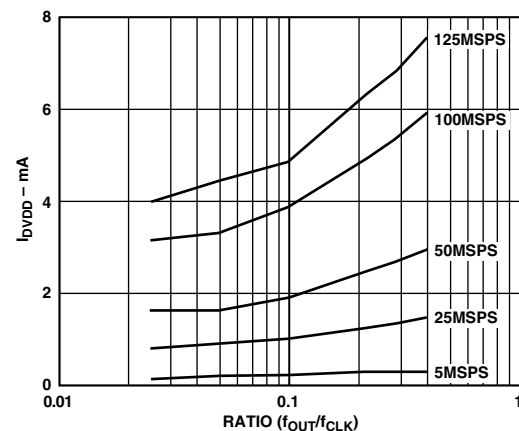


Figure 49. I_{DVDD} vs. Ratio @ $DVDD = 3$ V

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APPLYING THE AD9760 OUTPUT CONFIGURATIONS

The following sections illustrate some typical output configurations for the AD9760. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high frequency performance and is recommended for any application allowing for ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain and/or level shifting.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if I_{OUTA} and/or I_{OUTB} is connected to an appropriately sized load resistor, R_{LOAD} , referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting I_{OUTA} or I_{OUTB} into a negative unipolar voltage. This configuration provides the best dc linearity since I_{OUTA} or I_{OUTB} is maintained at a virtual ground. Note that I_{OUTA} provides slightly better performance than I_{OUTB} .

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 50. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer such as the Mini-Circuits T1-1T provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.

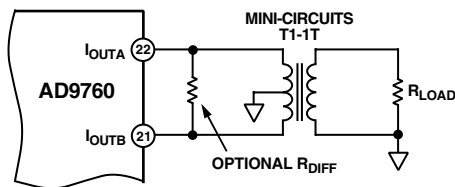


Figure 50. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both I_{OUTA} and I_{OUTB} . The complementary voltages appearing at I_{OUTA} and I_{OUTB} (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9760. A differential resistor, R_{DIFF} , may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD} , via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF} .

DIFFERENTIAL USING AN OP AMP

An op amp can also be used to perform a differential to single-ended conversion as shown in Figure 51. The AD9760 is configured with two equal load resistors, R_{LOAD} , of 25 Ω . The differential voltage developed across I_{OUTA} and I_{OUTB} is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across I_{OUTA} and I_{OUTB} , forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DACs high slewing output from overloading the op amp's input.

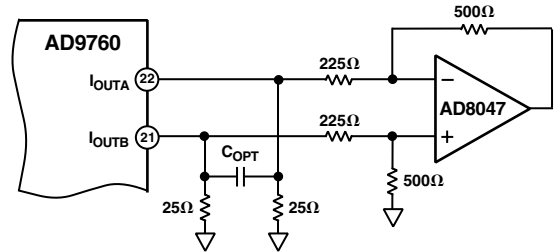


Figure 51. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ± 1.0 V. A high speed amplifier capable of preserving the differential performance of the AD9760 while meeting other system level objectives (i.e., cost, power) should be selected. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 52 provides the necessary level-shifting required in a single supply system. In this case, AVDD which is the positive analog supply for both the AD9760 and the op amp is also used to level-shift the differential output of the AD9760 to midsupply (i.e., $AVDD/2$). The AD8041 is a suitable op amp for this application.

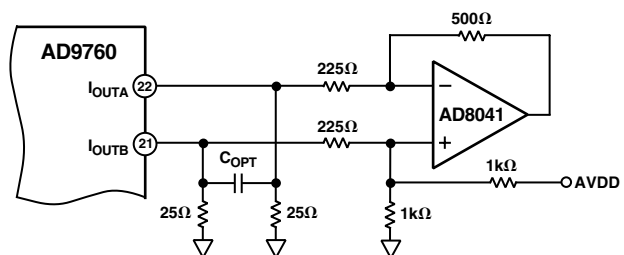


Figure 52. Single-Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT

Figure 53 shows the AD9760 configured to provide a unipolar output range of approximately 0 V to +0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS} , of 20 mA flows through the equivalent R_{LOAD} of 25 Ω . In this case, R_{LOAD} represents the equivalent load resistance seen by I_{OUTA} or I_{OUTB} . The unused output (I_{OUTA} or I_{OUTB}) can be connected to ACOM directly or via a matching R_{LOAD} . Different values of

I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.

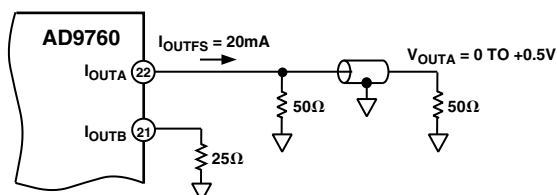


Figure 53. 0 V to +0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION

Figure 54 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9760 output current. U1 maintains I_{OUTA} (or I_{OUTB}) at a virtual ground, thus minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slewing capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS} . The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB} . An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink will be subsequently reduced.

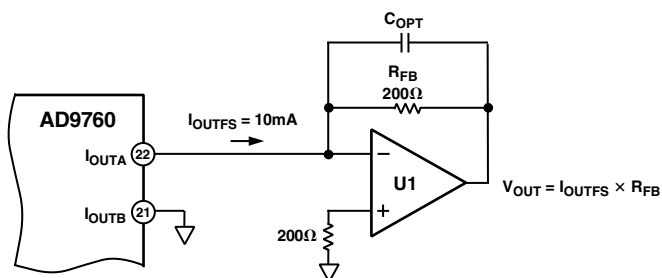


Figure 54. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS

In systems seeking to simultaneously achieve high speed and high performance, the implementation and construction of the printed circuit board design is often as important as the circuit design. Proper RF techniques must be used in device selection, placement and routing, and supply bypassing and grounding. The evaluation board for the AD9760, which uses a four-layer PC board, serves as a good example for the above-mentioned considerations. Figures 60–65 illustrate the recommended printed circuit board ground, power and signal plane layouts that are implemented on the AD9760 evaluation board.

Proper grounding and decoupling should be a primary objective in any high speed, high resolution system. The AD9760 features separate analog and digital supply and ground pins to optimize

the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close as physically possible.

For those applications that require a single +5 V or +3 V supply for both the analog and digital supply, a clean analog supply may be generated using the circuit shown in Figure 55. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained using low ESR type electrolytic and tantalum capacitors.

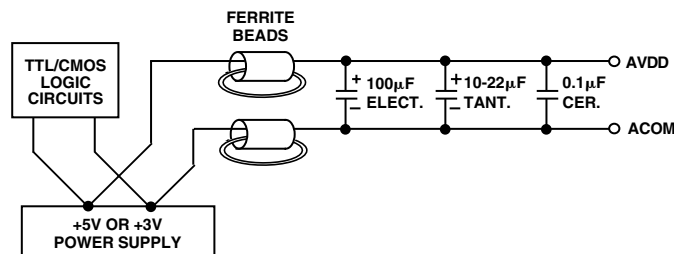


Figure 55. Differential LC Filter for Single +5 V or +3 V Applications

Maintaining low noise on power supplies and ground is critical to obtain optimum results from the AD9760. If properly implemented, ground planes can perform a host of functions on high speed circuit boards: bypassing, shielding, current transport, etc. In mixed signal design, the analog and digital portions of the board should be distinct from each other, with the analog ground plane confined to the areas covering the analog signal traces, and the digital ground plane confined areas covering the digital interconnects.

All analog ground pins of the DAC, reference and other analog components should be tied directly to the analog ground plane. The two ground planes should be connected by a path 1/8 to 1/4 inch wide underneath or within 1/2 inch of the DAC to maintain optimum performance. Care should be taken to ensure that the ground plane is uninterrupted over crucial signal paths. On the digital side, this includes the digital input lines running to the DAC as well as any clock signals. On the analog side, this includes the DAC output signal, reference signal and the supply feeders.

The use of wide runs or planes in the routing of power lines is also recommended. This serves the dual role of providing a low series impedance power supply to the part and providing some "free" capacitive decoupling to the appropriate ground plane. It is essential that care be taken in the layout of signal and power ground interconnects to avoid inducing extraneous voltage drops in the signal ground paths. It is recommended that all connections be short, direct and as physically close to the package as possible to minimize the sharing of conduction paths between different currents. When runs exceed an inch in length, strip line techniques with proper termination resistor should be considered. The necessity and value of this resistor will be dependent upon the logic family used.

For a more detailed discussion of the implementation and construction of high speed, mixed signal printed circuit boards, refer to Analog Devices' application notes AN-280 and AN-333.

AD9760

APPLICATIONS

Using the AD9760 for QAM Modulation

QAM is one of the most widely used digital modulation schemes in digital communication systems. This modulation technique can be found in both FDM spread spectrum (i.e., CDMA) based systems. A QAM signal is a carrier frequency that is both modulated in amplitude (i.e., AM modulation) and in phase (i.e., PM modulation). It can be generated by independently modulating two carriers of identical frequency but with a 90° phase difference. This results in an in-phase (I) carrier component and a quadrature (Q) carrier component at a 90° phase shift with respect to the I component. The I and Q components are then summed to provide a QAM signal at the specified carrier frequency.

A common and traditional implementation of a QAM modulator is shown in Figure 56. The modulation is performed in the analog domain in which two DACs are used to generate the baseband I and Q components, respectively. Each component is then typically applied to a Nyquist filter before being applied to a quadrature mixer. The matching Nyquist filters shape and limit each component's spectral envelope while minimizing intersymbol interference. The DAC is typically updated at the QAM symbol rate or possibly a multiple of it if an interpolating filter precedes the DAC. The use of an interpolating filter typically eases the implementation and complexity of the analog filter, which can be a significant contributor to mismatches in gain and phase between the two baseband channels. A quadrature mixer modulates the I and Q components with in-phase and quadrature phase carrier frequency and sums the two outputs to provide the QAM signal.

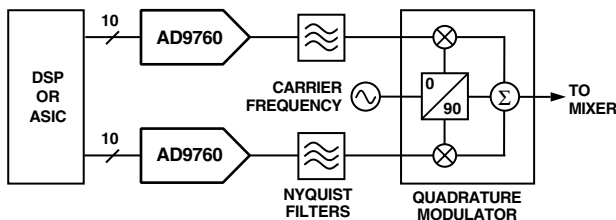


Figure 56. Typical Analog QAM Architecture

In this implementation, it is much more difficult to maintain proper gain and phase matching between the I and Q channels. The circuit implementation shown in Figure 57 helps improve on the matching and temperature stability characteristics between the I and Q channels. Using a single voltage reference derived from U1 to set the gain for both the I and Q channels will improve the gain matching and stability. Further enhancements in gain matching and stability are achieved by using separate matching resistor networks for both R_{SET} and R_{LOAD} . Additional trim capability via R_{CAL1} and R_{CAL2} can be added to compensate for any initial mismatch in gain between the two channels. This may be attributed to any mismatch between U1 and U2's gain setting resistor (R_{SET}), effective load resistance, (R_{LOAD}), and/or voltage offset of each DAC's control amplifier. The differential voltage outputs of U1 and U2 are fed into their respective differential inputs of a quadrature mixer via matching 50 Ω filter networks.

It is also possible to generate a QAM signal completely in the digital domain via a DSP or ASIC, in which case only a single DAC of sufficient resolution and performance is required to reconstruct the QAM signal. Also available from several vendors

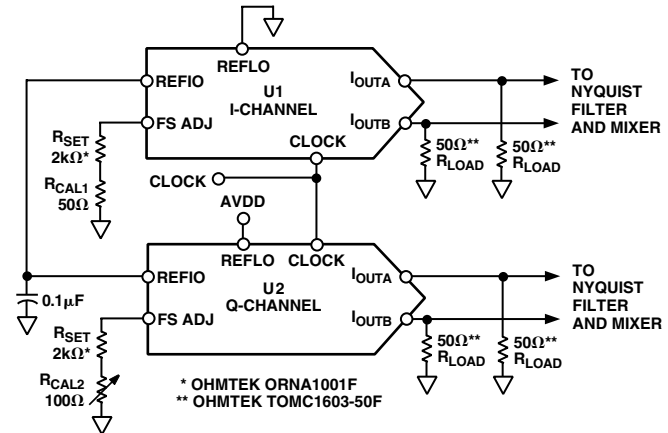


Figure 57. Baseband QAM Implementation Using Two AD9760s

are Digital ASICs which implement other digital modulation schemes such as PSK and FSK. This digital implementation has the benefit of generating perfectly matched I and Q components in terms of gain and phase, which is essential in maintaining optimum performance in a communication system. In this implementation, the reconstruction DAC must be operating at a sufficiently high clock rate to accommodate the highest specified QAM carrier frequency. Figure 58 shows a block diagram of such an implementation using the AD9760.

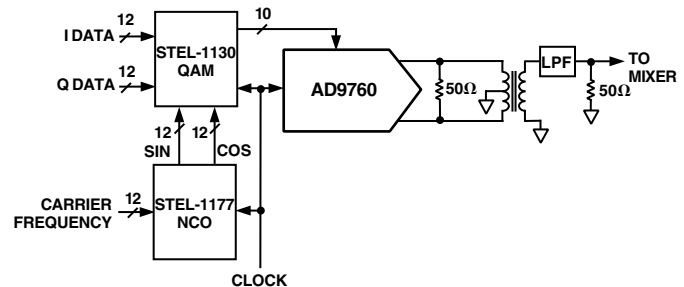


Figure 58. Digital QAM Architecture

AD9760 EVALUATION BOARD

General Description

The AD9760-EB is an evaluation board for the AD9760 10-bit D/A converter. Careful attention to layout and circuit design, combined with a prototyping area, allow the user to easily and effectively evaluate the AD9760 in any application where high resolution, high speed conversion is required.

This board allows the user the flexibility to operate the AD9760 in various configurations. Possible output configurations include transformer coupled, resistor terminated, inverting/noninverting and differential amplifier outputs. The digital inputs are designed to be driven directly from various word generators with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9760 with either the internal or external reference or to exercise the power-down feature.

Refer to the application note AN-420, "Using the AD9760/AD9760/AD9764-EB Evaluation Board," for a thorough description and operating instructions for the AD9760 evaluation board.

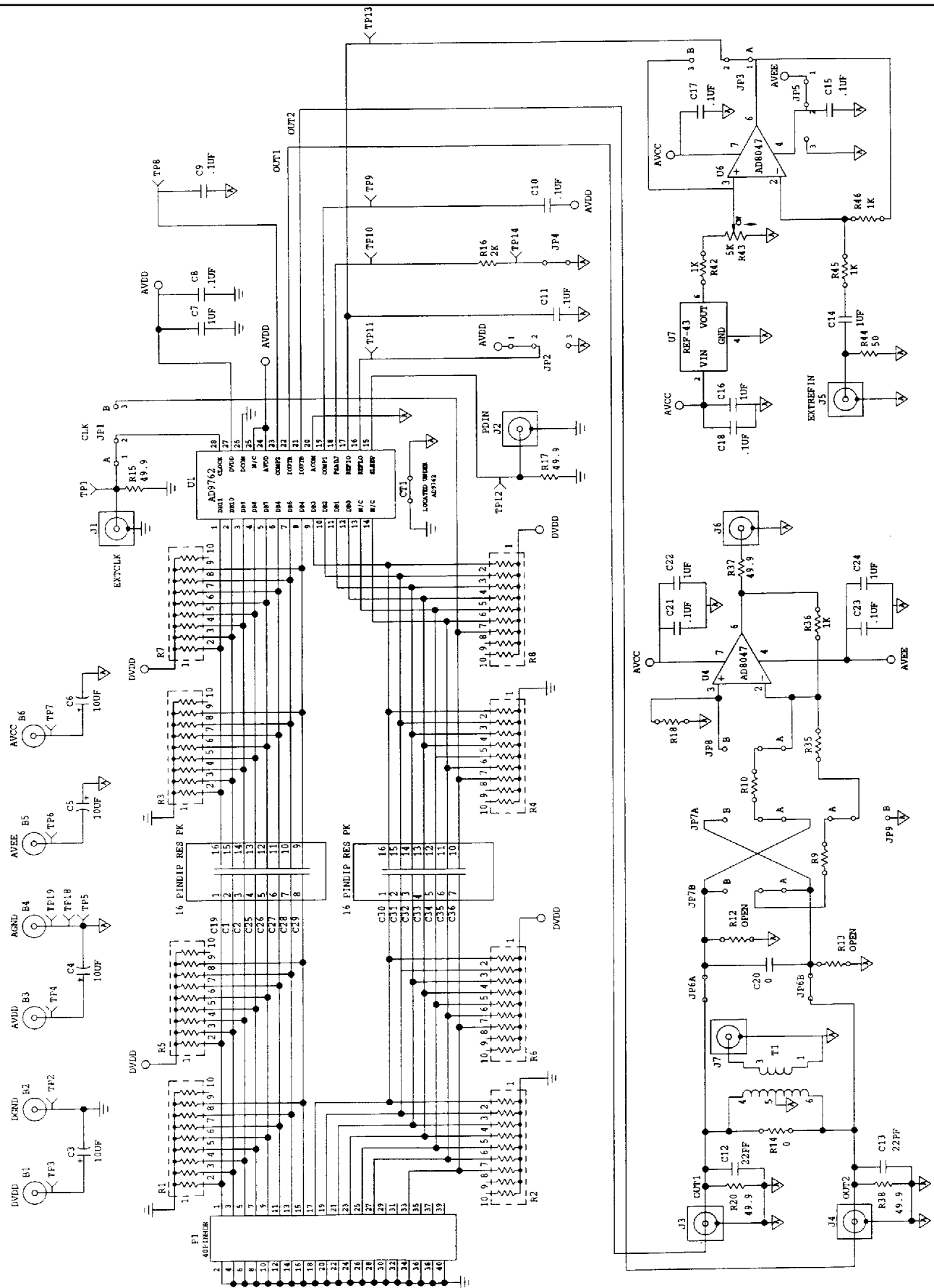


Figure 59. Evaluation Board Schematic

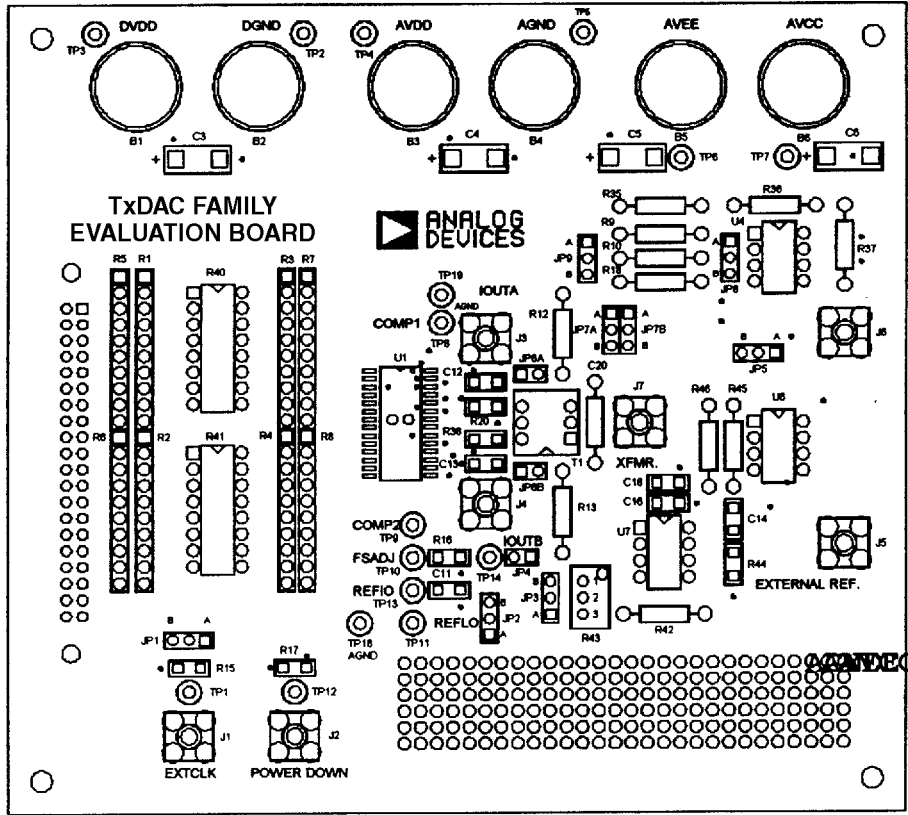


Figure 60. Silkscreen Layer—Top

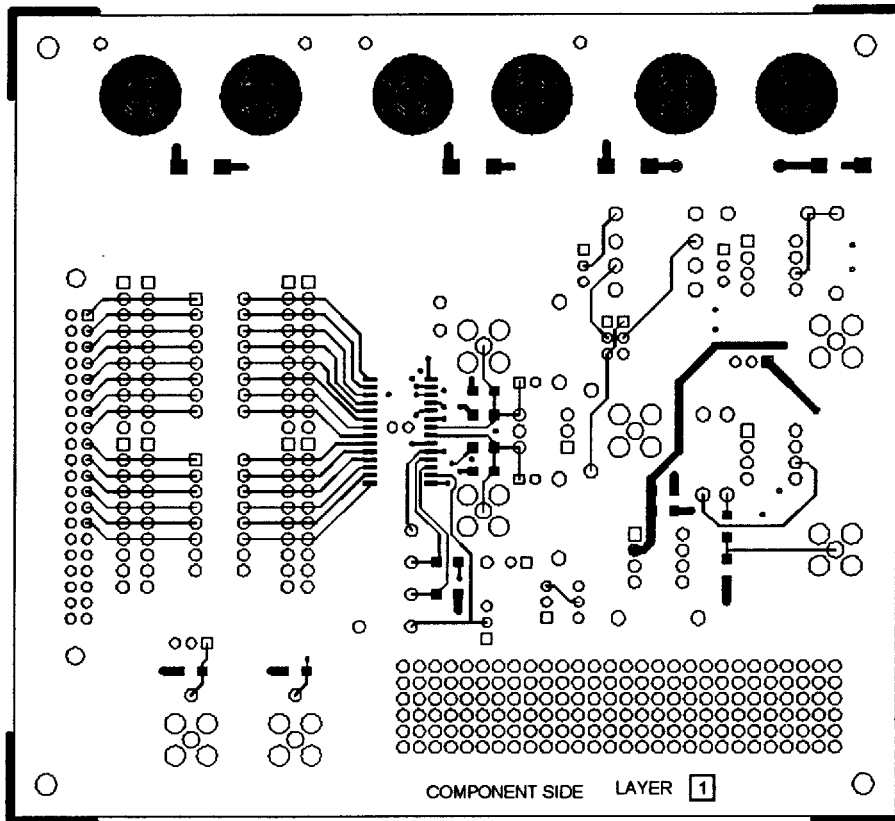


Figure 61. Component Side PCB Layout (Layer 1)

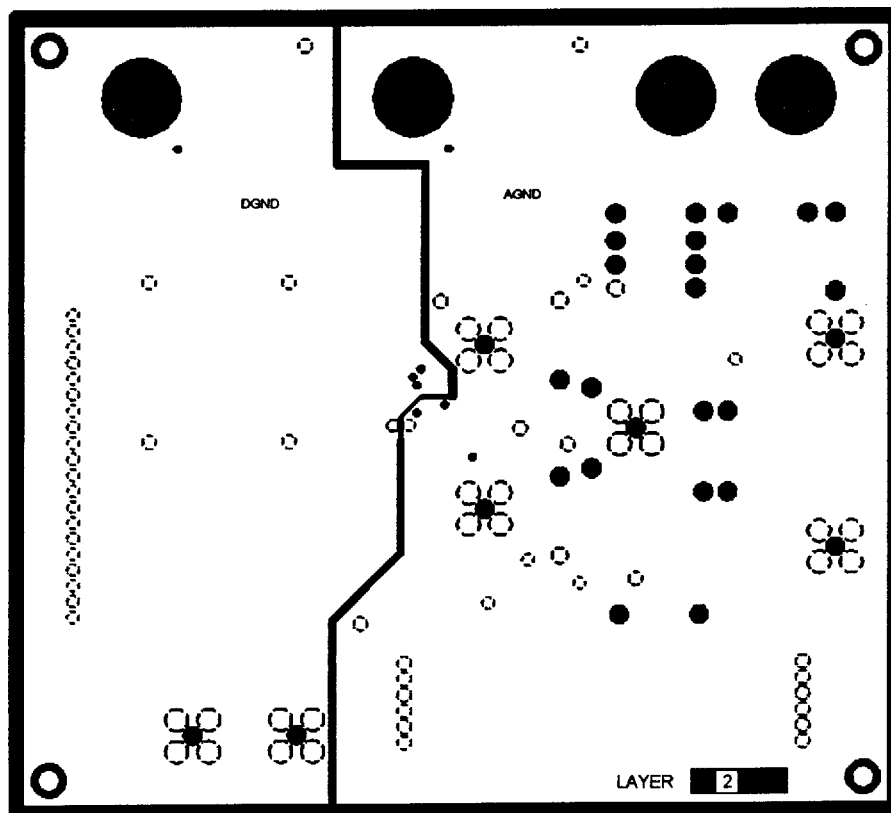


Figure 62. Ground Plane PCB Layout (Layer 2)

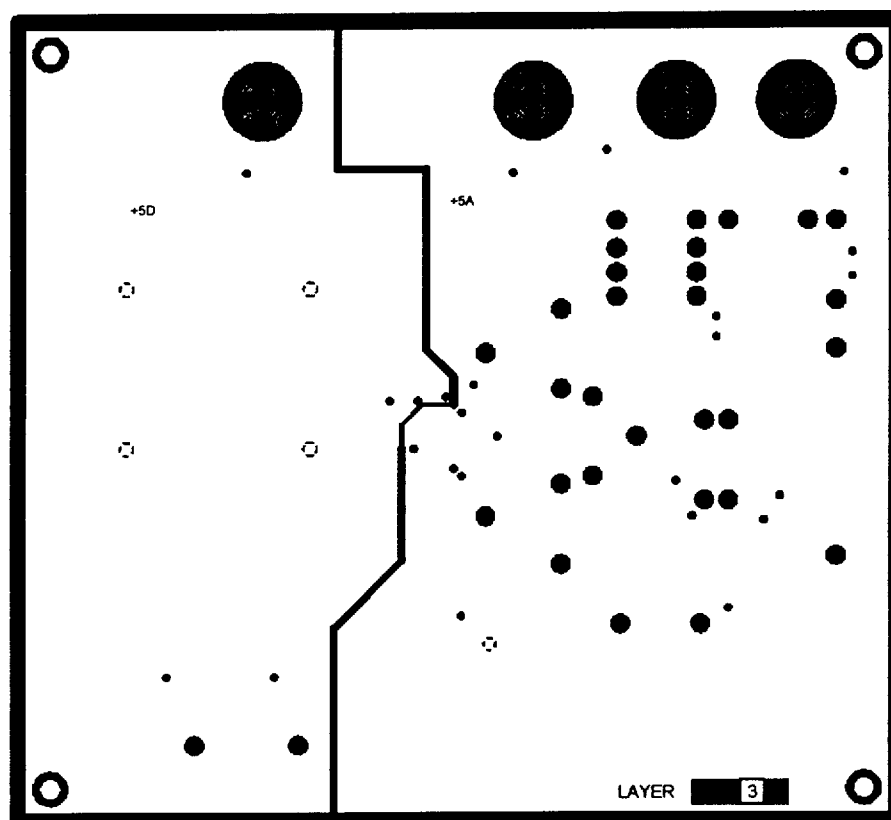


Figure 63. Power Plane PCB Layout (Layer 3)

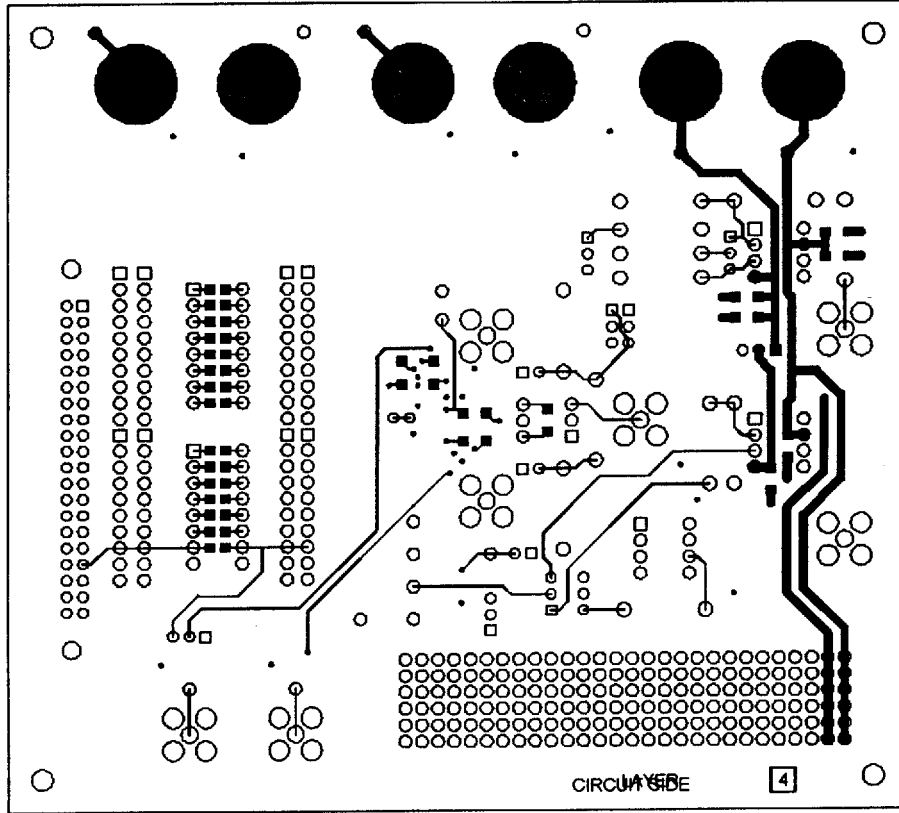


Figure 64. Solder Side PCB Layout (Layer 4)

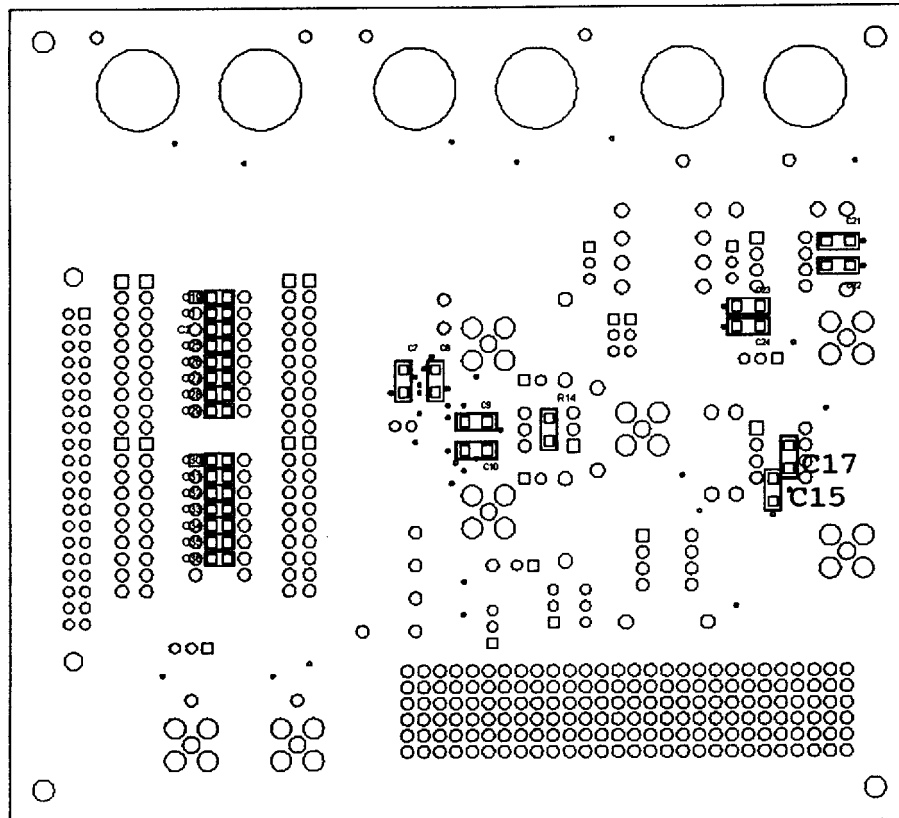
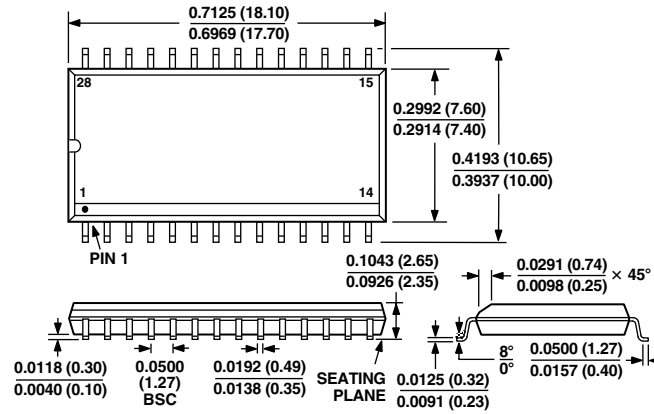


Figure 65. Silkscreen Layer—Bottom

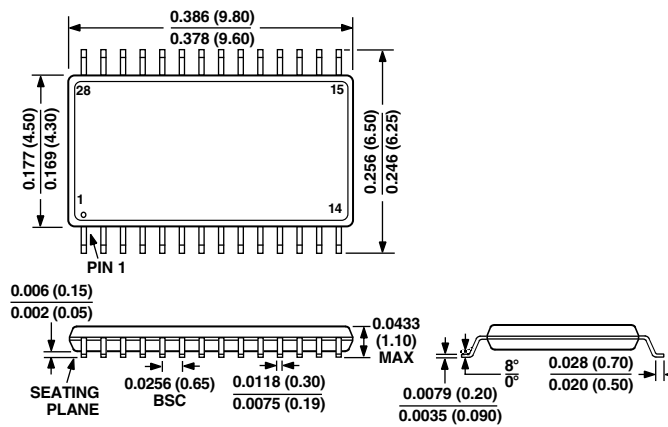
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**28-Lead, 300 Mil SOIC
(R-28)**



**28-Lead Thin Shrink Small Outline Package (TSSOP)
(RU-28)**



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