THE DATASHEET OF

LT8415IDDB#TRMPBF

Ultralow Power Boost Converter with Dual Half-Bridge Switches

FEATURES

- **High Voltage Switches Built In (Dual Half-Bridge)**
- **Ultralow Quiescent Current**
- **10.5µA in Active Mode**
- **0µA in Shutdown Mode**
- **Comparator Built into $\overline{SHDN}$ Pin**
- **Low Noise Control Scheme**
- **Adjustable FB Reference Voltage**
- **Wide Input Range: 2.5V to 16V**
- **Wide Output Range: Up to 40V**
- **Integrated Power NPN Switch (25mA Current Limit)**
- **Integrated Schottky Diode**
- **Integrated Output Disconnect**
- High Value (12.4M/0.4M) Feedback Resistor Integrated
- Built in Soft Start (Optional Capacitor from V_{REF} to GND)
- Over Voltage Protection for CAP, V_{OUT}, OUT1 and OUT2 Pins
- 12-Pin 3mm × 2mm DFN package

APPLICATIONS

- Sensor Power
- RF Mems Relay Power
- Low Power Actuator Bias/Control
- Liquid Lens Driver

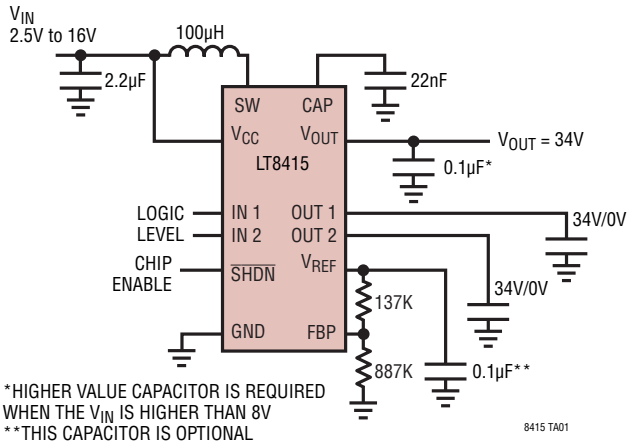
DESCRIPTION

The LT®8415 is an ultralow power boost converter with two integrated complementary MOSFET half-bridges (N- and P-channel), integrated power switch, Schottky diode and output disconnect circuitry. The N-channel and P-channel MOSFETs in each half-bridge are synchronously controlled by a single input pin, and never turn on at the same time in typical applications.

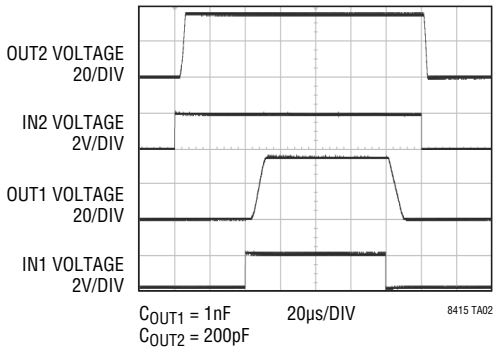
The boost regulator controls power delivery by varying both the peak inductor current and switch off-time. This control scheme results in low output voltage ripple as well as high efficiency over a wide load range. The quiescent current is a low 10.5µA, which is further reduced to 0µA in shutdown. The internal disconnect circuitry allows the output voltage to be blocked from the input during shutdown. High value (12.4M/0.4M) resistors are integrated on chip for output voltage detection, significantly reducing input referred quiescent current. The LT8415 also features a comparator built into the $\overline{SHDN}$ pin, overvoltage protection for the CAP, V_{OUT}, OUT1 and OUT2 pins, built in soft start and comes in a tiny 12-pin 3mm × 2mm DFN package.

TYPICAL APPLICATION

Drive External Capacitors to 34V/0V with the LT8415



Response Driving External Capacitors

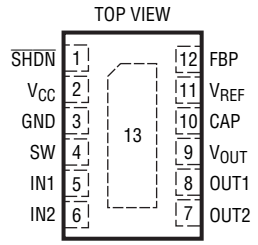


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} Voltage ..... –0.3V to 16V
CAP, V_{OUT} Voltage ..... –0.3V to 40V
SW ..... –0.3V to 41V
IN1,IN2 ..... –0.3V to 6V
OUT1,OUT2 ..... –0.3V to 40V
$\overline{SHDN}$ Voltage ..... –0.3V to 16V
V_{REF} Voltage ..... –0.3V to 2.5V
FBP Voltage ..... –0.3V to 2.5V
Maximum Junction Temperature ..... 125°C
Operating Temperature Range (Note 2).. –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DDB PACKAGE
12-PIN (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION (http://www.linear.com/product/LT8415#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8415EDDB#PBF	LT8415EDDB#TRPBF	LFDC	12-Pin (3mm × 2mm) Plastic DFN	–40°C to 125°C
LT8415IDDB#PBF	LT8415IDDB#TRPBF	LFDC	12-Pin (3mm × 2mm) Plastic DFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.0V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Operating Voltage				2.20	2.50	V
Maximum Operating Voltage					16	V
Reference Voltage		●	1.220	1.235	1.255	V
V_{REF} Current Limit	(Note 3)			10		µA
V_{REF} Discharge Time	(Note 3)			70		µS
V_{REF} Line Regulation				0.01		%/V
Quiescent Current	Not Switching	●		10.5	15.5	µA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V	●		0	1	µA
Quiescent Current from V_{OUT} and CAP	V_{OUT} = 16V			4		µA
Minimum Switch Off Time	After Start-Up (Note 4) During Start-Up (Note 4)			240 600		nS
Switch Current Limit		●	20	25	30	mA
Switch V_{CESAT}	I_{SW} = 10mA			150		mV
Switch Leakage Current	V_{SW} = 5V			0	1	µA
Schottky Forward Voltage	I_{DIODE} = 10mA			650	850	mV
Schottky Reverse Leakage	$V_{CAP} – V_{SW}$ = 5 $V_{CAP} – V_{SW}$ = 40			0 0	0.5 1	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are T_A = 25°C. V_{IN} = 3.0V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PMOS Disconnect Current Limit			14	19	25	mA
PMOS Disconnect V_{CAP} - V_{OUT}	I_{OUT} = 1mA			50		mV
Internal Resistor Divider Ratio		●	31.6	31.85	32.2	
FBP pin Bias Current	V_{FBP} = 0.5V, Current Flows Out of Pin	●		1.3	30	nA
$\overline{SHDN}$ Minimum Input Voltage High	$\overline{SHDN}$ Rising	●	1.20	1.30	1.45	V
$\overline{SHDN}$ Input Voltage High hysteresis				60		mV
$\overline{SHDN}$ Hysteresis Current	(Note 3)		0.08	0.1	0.14	µA
$\overline{SHDN}$ Input Voltage Low					0.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 16V			0 2	1 3	µA µA
IN1,IN2 Minimum Input Voltage High		●	1.1			V
IN1,IN2 Input Voltage Low		●			0.3	V
OUT1,OUT2 Rise Time	V_{OUT} = 34V, C_{LOAD} = 200pF (Note 5)			2.5		µs
OUT1,OUT2 Fall Time	V_{OUT} = 34V, C_{LOAD} = 200pF (Note 5)			3		µs
OUT1,OUT2 Rise Delay	V_{OUT} = 34V, C_{LOAD} = 200pF (Note 5)			4		µs
OUT1,OUT2 Fall Delay	V_{OUT} = 34V, C_{LOAD} = 200pF (Note 5)			2		µs
Half-bridge PMOS Voltage Drop V_{OUT} – $V_{OUT1,OUT2}$	IN1,IN2 = 2V, 0.1mA Load From OUT1,OUT2			70		mV
Half-bridge NMOS Voltage Drop $V_{OUT1,OUT2}$	IN1,IN2 = 0V, 0.1mA Current Into OUT1,OUT2			85		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT8415E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8415I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: See applications section for more information.

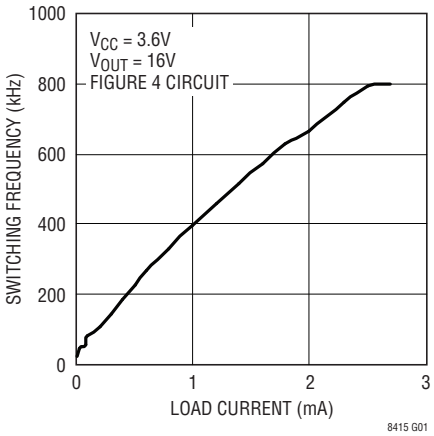
Note 4: Start-Up mode occurs when V_{OUT} is less than V_{FBP}*64/3.

Note 5: See Timing Diagram. Rise times are measured from 4V to 30V and fall times are measured from 30V to 4V. Delay times are measured from the IN1,IN2 transition to when the OUT1,OUT2 voltage has risen to 4V or decreased to 30V.

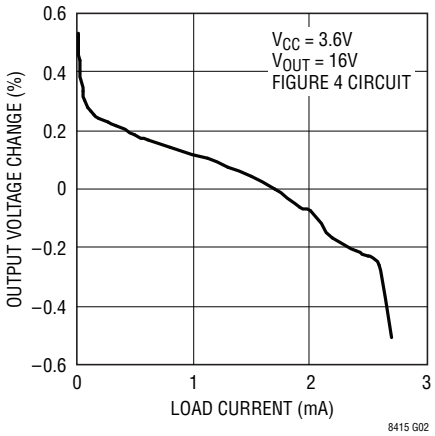
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

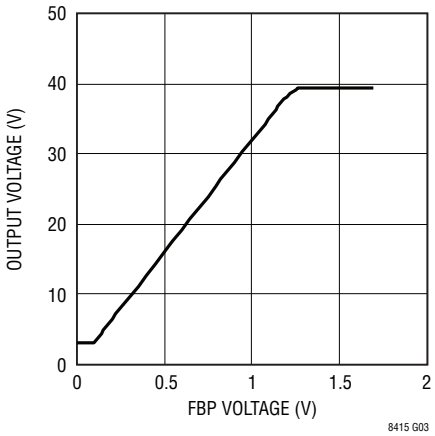
Switching Frequency vs Load Current



Load Regulation

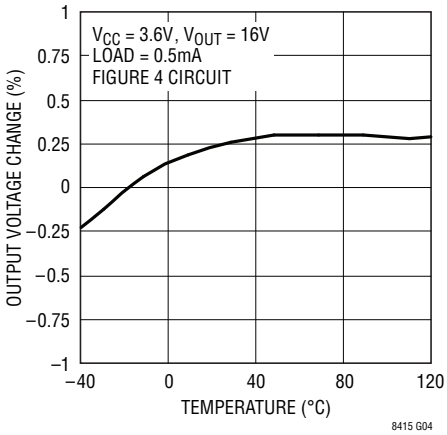


Vout vs FBP Voltage

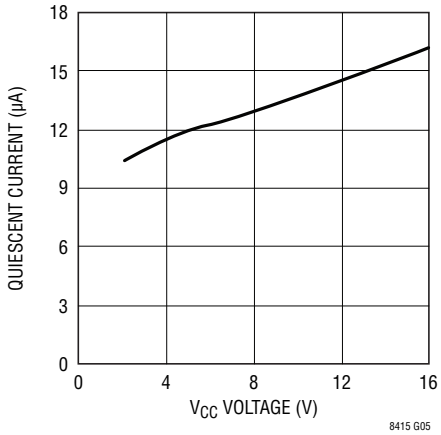


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

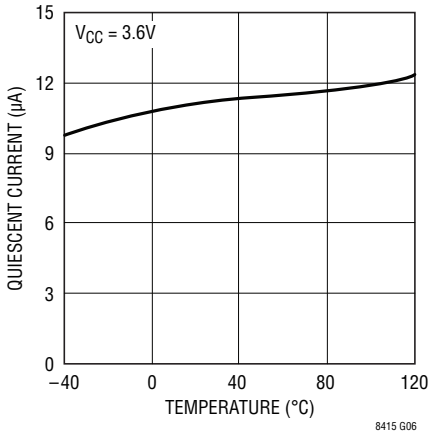
Output Voltage vs Temperature



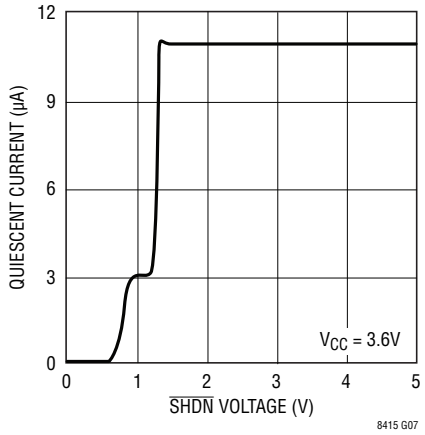
Quiescent Current – Not Switching



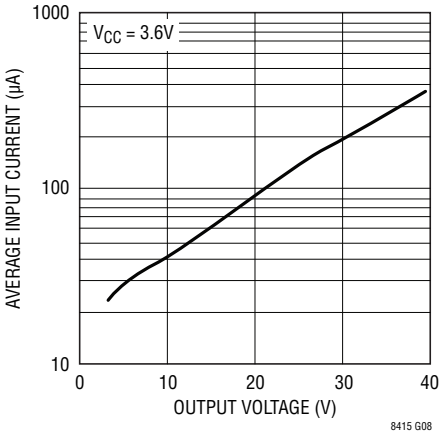
Quiescent Current vs Temperature



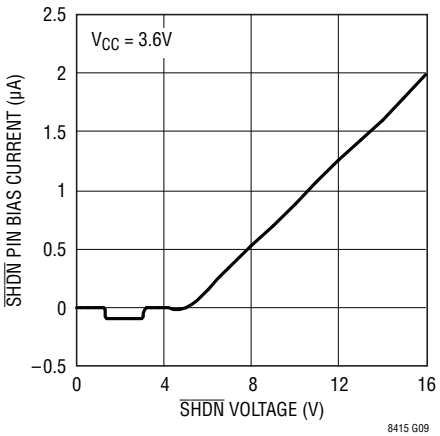
Quiescent Current vs $\overline{SHDN}$ Voltage



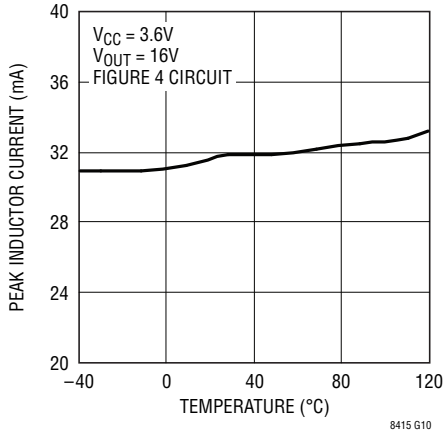
Average Input Current in Regulation with No Load



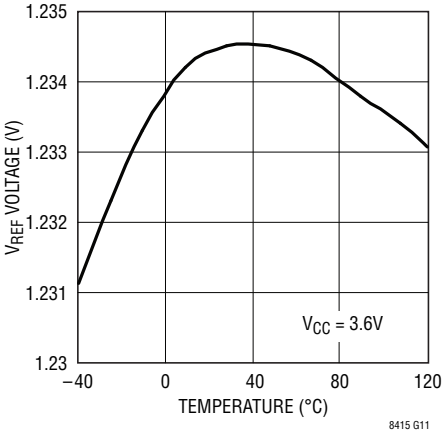
$\overline{SHDN}$ Current vs $\overline{SHDN}$ Voltage



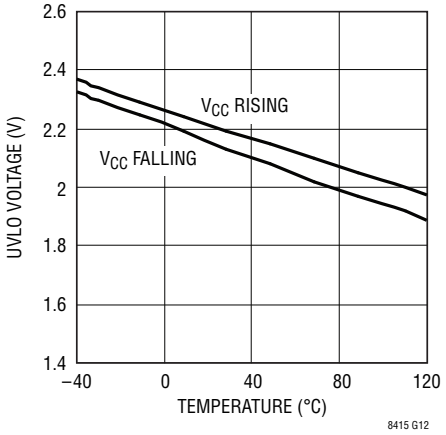
Peak Inductor Current vs Temperature



V_{REF} Voltage vs Temperature

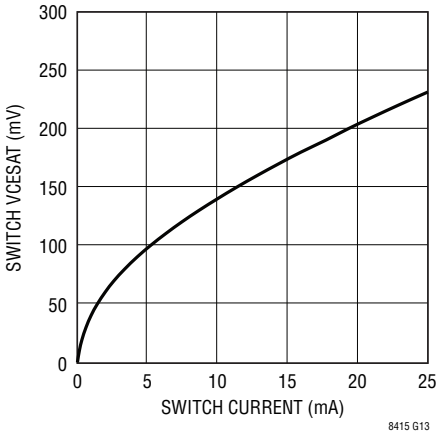


UVLO vs Temperature

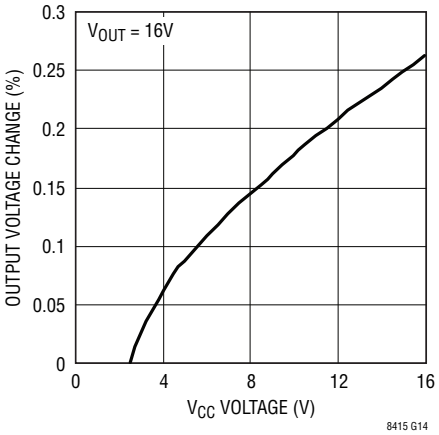


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

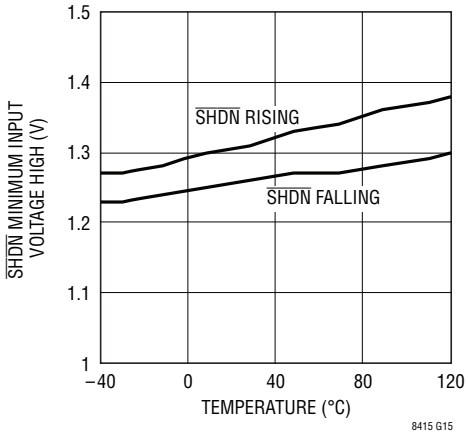
SW Saturation Voltage vs Switch Current



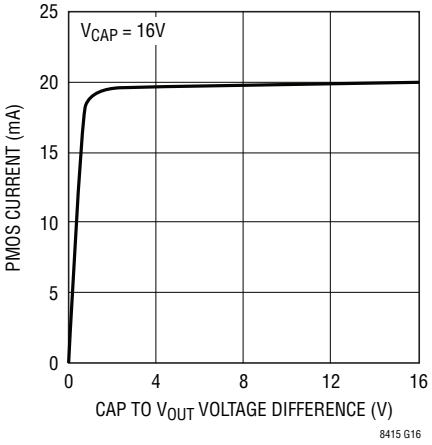
Line Regulation



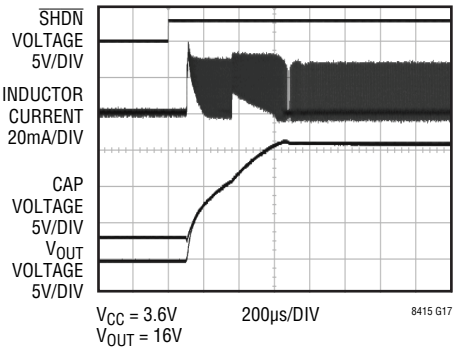
$\overline{SHDN}$ Minimum Input Voltage High vs Temperature



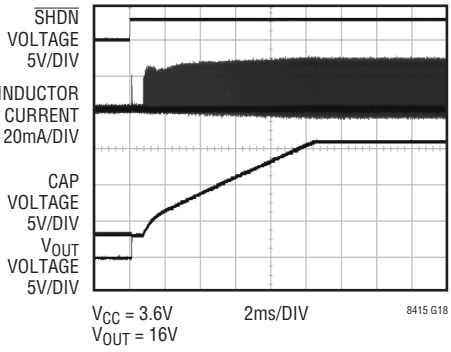
Output Disconnect PMOS current vs CAP to V_{OUT} Voltage Difference



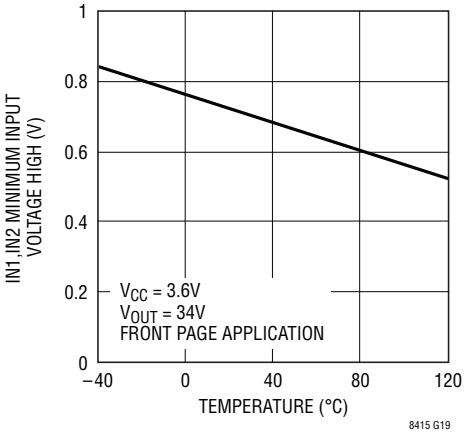
Start-Up Waveforms Without Capacitor at V_{REF} Pin



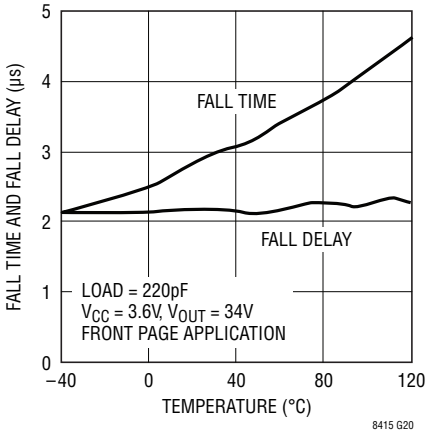
Start-Up Waveforms With 0.1µF Capacitor at V_{REF} pin



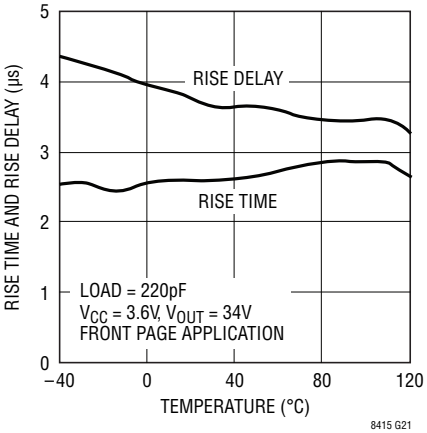
IN1,IN2 Minimum Input Voltage High vs Temperature



Half-Bridge Fall Time and Fall Delay vs Temperature



Half-Bridge Rise Time and Rise Delay vs Temperature



PIN FUNCTIONS

$\overline{SHDN}$ (Pin 1): Shutdown Pin. This pin is used to enable/disable the chip. Drive below 0.3V to disable the chip. Drive above 1.4V to activate the chip. Do not float this pin.

V_{CC} (Pin 2): Input Supply Pin. Must be locally bypassed to GND. See typical applications section.

GND (Pin 3 and Pin 13): Ground. Tie directly to local ground plane. Pin 13 is floating but must be grounded for proper shielding.

SW (Pin 4): Switch Pin. This is the collector of the internal NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI.

IN1 (Pin 5): First Half-Bridge Control Input. Do not float this pin.

IN2 (Pin 6): Second Half-Bridge Control Input. Do not float this pin.

OUT2 (Pin 7): Second Half-Bridge Output. This pin is controlled in phase by the voltage on IN2. The output level is either the voltage on V_{OUT} or GND.

OUT1 (Pin 8): First Half-Bridge Output. This pin is controlled in phase by the voltage on IN1. The output level is either the voltage on V_{OUT} or GND.

V_{OUT} (Pin 9): Drain of Output Disconnect PMOS. Place a bypass capacitor from this pin to GND.

CAP (Pin 10): This is the Cathode of the Internal Schottky Diode. Place a bypass capacitor from this pin to GND.

V_{REF} (Pin 11): Reference Pin. Soft start can be achieved by placing a capacitor from this pin to GND. This cap will be discharged for 70µs (typical) at the beginning of start-up and then be charged to 1.235V with a 10µA current source.

FBP(Pin 12): Positive Feedback Pin. This pin is the error amplifier's positive input terminal. To achieve the desired output voltage, choose the FBP pin voltage (V_{FBP}) according to the following formula:

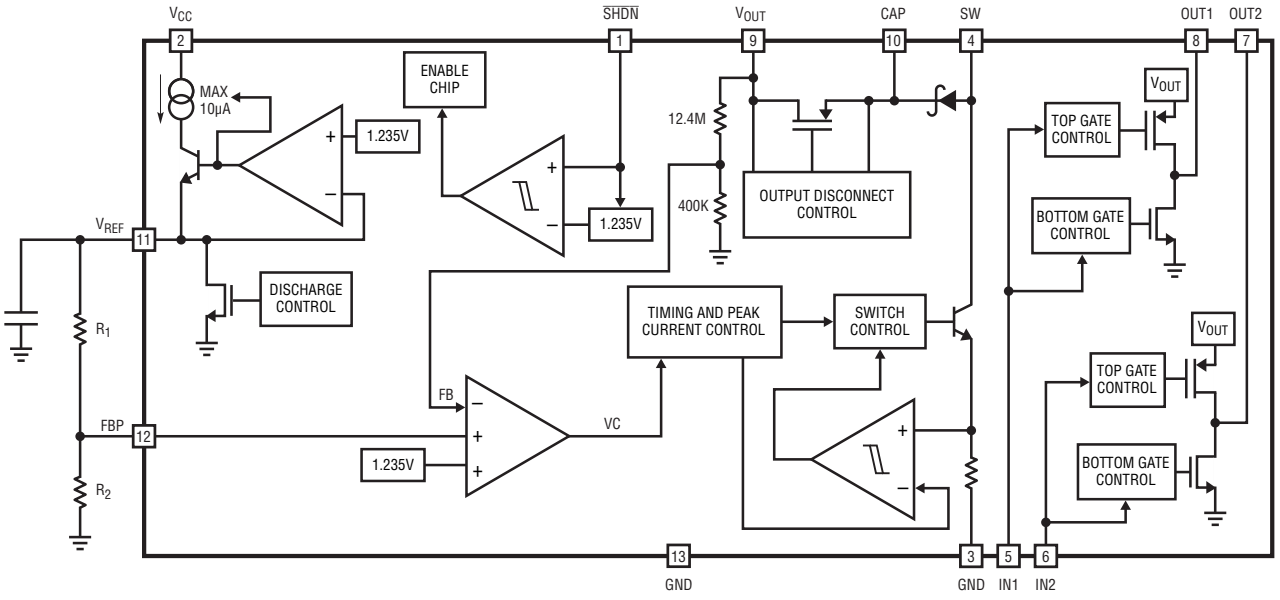
$$V_{FBP} = V_{OUT}/31.85$$

When resistor divider from the V_{REF} is used to set the FBP voltage, choose the resistor divider ratio according to the following formula:

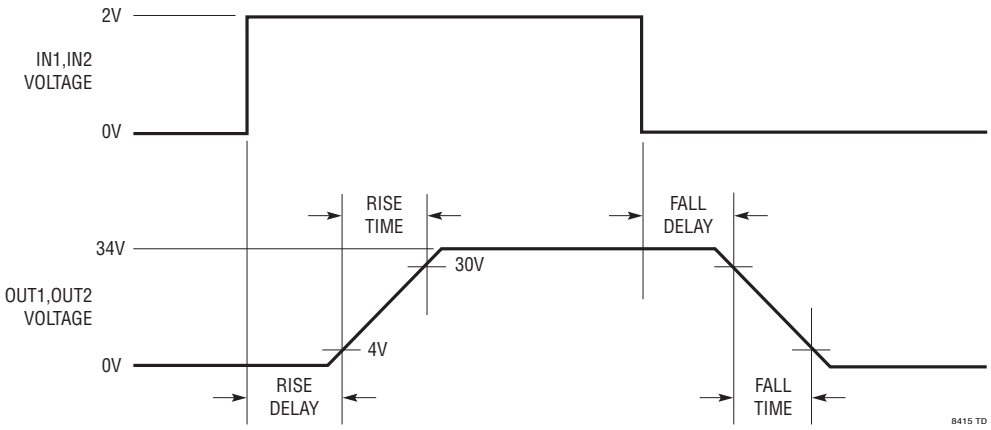
$$R1/R2 = (39.33 – V_{OUT})/V_{OUT}$$

For protection purposes, the output voltage can not exceed 40V even if V_{FBP} is driven higher than V_{REF}.

BLOCK DIAGRAM



TIMING DIAGRAM



OPERATION

Switching Regulator

The LT8415 utilizes a variable peak current, variable off-time control scheme to provide high efficiency over a wide output current range.

The operation of the part can be better understood by referring to the Block Diagram. The part senses the output voltage by monitoring the internal FB node, and servoing the FB node voltage to be equal to the FBP pin voltage. The chip integrates an accurate high value resistor divider (12.4MEG/0.4MEG) from the V_{OUT} pin. The output voltage is set by the FBP pin voltage, which in turn is set by an external resistor divider from the V_{REF} pin. The FBP pin voltage can also be directly biased with an external reference, allowing full control of the output voltage during operation.

The Switch Control block senses the output of the amplifier and adjusts the switching frequency as well as other parameters to achieve regulation. During the start-up of the circuit, special precautions are taken to ensure that the inductor current remains under control.

The LT8415 also has a PMOS output disconnect switch. The PMOS switch is turned on when the part is enabled via the $\overline{SHDN}$ pin. When the part is in shutdown, the PMOS switch turns off, allowing the V_{OUT} node to go to ground. This type of disconnect function is often required in power supplies.

Half-Bridge

The N-channel and P-channel MOSFETs in each half-bridge are synchronously controlled by a single input pin, and will never turn on at the same time in typical applications, protecting against shoot-through current. The OUT1 and OUT2 pins are the same polarity as the IN1 and IN2 pins respectively. When the part is disabled, both N-channel and P-channel MOSFETs turn off, and the OUT1 and OUT2 pins will become high impedance with a 20MΩ pull down resistor connected to ground.

APPLICATIONS INFORMATION

Inductor Selection

Several inductors that work well with the LT8415 are listed in Table 1. The tables are not complete, and there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, as many different sizes and shapes are available.

Inductors with a value of 47µH or higher are recommended for most LT8415 designs. Inductors with low core losses and small DCR (copper wire resistance) are good choices for LT8415 applications. For full output power, the inductor should have a saturation current rating higher than the peak inductor current. The peak inductor current can be calculated as:

$$I_{PK} = I_{LIMIT} + \frac{V_{IN} \bullet 150 \bullet 10^{-6}}{L} mA$$

where the worst case I_{LIMIT} is 30mA. L is the inductance value in Henrys and V_{IN} is the input voltage to the boost circuit.

Table 1. Recommended Inductors for LT8415

PART	L (µH)	DCR (µH)	SIZE (mm)	VENDOR
LQH2MCN680K02	68	6.6	2.0 × 1.6 × 0.9	Murata
LQH32CN101K53	100	3.5	3.2 × 2.5 × 2.0	www.murata.com
DO2010-683ML	68	8.8	2.0 × 2.0 × 1.0	Coilcraft
DO2010-104ML	100	15.7	2.0 × 2.0 × 1.0	www.coilcraft.com
LPS3015-104ML	100	3.4	3.0 × 3.0 × 1.4	
LPS3015-154ML	150	6.1	3.0 × 3.0 × 1.4	

Capacitor Selection

The small size and low ESR of ceramic capacitors make them suitable for most LT8415 applications. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 2.2µF or higher input capacitor and a 0.1µF to 1µF output capacitor are sufficient for most applications. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors rated at 0.1µF to 1µF have greatly reduced capacitance when bias voltages are applied. Be sure to check actual capacitance at the desired output voltage. Generally a 0603 or 0805 size capacitor will be adequate. A 0.1µF to 1µF capacitor placed on the CAP node is recommended to filter the inductor current while a 0.1µF to 1µF capacitor placed on the V_{OUT} node will give excellent transient response and stability. To make the V_{REF} pin less sensitive to noise, putting a capacitor on the V_{REF} pin is recommended, but not required. A 47nF to 220nF 0402 capacitor will be sufficient. See also Soft-Start section for more information about a capacitor across V_{REF}. Table 2 shows a list of several capacitor manufacturers. Consult the manufacturers for more detailed information and for their entire selection of related parts.

Table 2. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	PHONE	WEBSITE
Taiyo Yuden	(408) 573-4150	www.t-yuden.com
Murata	(814) 237-1431	www.murata.com
AVX	(843) 448-9411	www.avxcorp.com
Kemet	(408)986-0424	www.kemet.com
TDK	(847) 803-6100	www.tdk.com

Setting Output Voltage

The output voltage is set by the FBP pin voltage, and V_{OUT} is equal to 31.85 • V_{FBP} when the output is regulated, shown in Figure 1. Since the V_{REF} pin provides a good reference (~1.235V), the FBP voltage can be easily set by a resistor divider from the V_{REF} pin to ground. The series resistance of this resistor divider should be kept larger than 200KΩ to prevent loading down the V_{REF} pin. The FBP pin can also be biased directly by an external reference. For over voltage protection, the output voltage is limited to 40V. Therefore, if V_{FBP} is higher than 1.235V, the output voltage will stay at 40V.

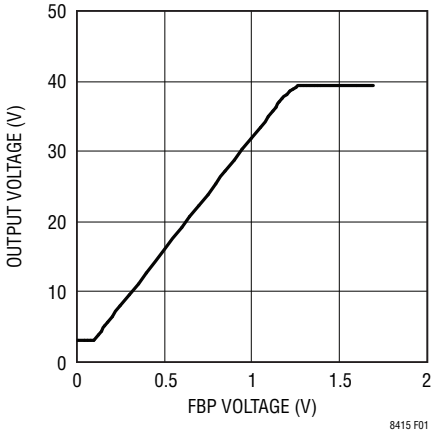


Figure 1. FBP to V_{OUT} Transfer Curve

APPLICATIONS INFORMATION

Maximum Output Load Current

The maximum output current of a particular LT8415 circuit is a function of several circuit variables. The following method can be helpful in predicting the maximum load current for a given circuit:

Step 1: Calculate the peak inductor current:

$$I_{PK} = I_{LIMIT} + \frac{V_{IN} \bullet 150 \bullet 10^{-6}}{L} mA$$

where I_{LIMIT} is 25mA. L is the inductance value in Henrys and V_{IN} is the input voltage to the boost circuit.

Step 2: Calculate the inductor ripple current:

$$I_{RIPPLE} = \frac{(V_{OUT} + 1 - V_{IN}) \bullet 200 \bullet 10^{-6}}{L} mA$$

where V_{OUT} is the desired output voltage. If the inductor ripple current is less than the peak current, then the circuit will only operate in discontinuous conduction mode. The inductor value should be increased so that $I_{RIPPLE} < I_{PK}$. An application circuit can be designed to operate only in discontinuous mode, but the output current capability will be reduced.

Step 3: Calculate the average input current:

$$I_{IN(AVG)} = I_{PK} - \frac{I_{RIPPLE}}{2} mA$$

Step 4: Calculate the nominal output current:

$$I_{OUT(NOM)} = \frac{I_{IN(AVG)} \bullet V_{IN} \bullet 0.7}{V_{OUT}} mA$$

Step 5: Derate output current:

$$I_{OUT} = I_{OUT(NOM)} \bullet 0.8$$

For low output voltages the output current capability will be increased. When using output disconnect (load current taken from V_{OUT}), these higher currents will cause the drop in the PMOS switch to be higher resulting in lower output current capability than predicted by the preceding equations.

Inrush Current

When V_{CC} is stepped from ground to the operating voltage while the output capacitor is discharged, a high level of inrush current may flow through the inductor and Schottky diode into the output capacitor. Conditions that increase inrush current include a larger more abrupt voltage step at V_{CC}, a larger output capacitor tied to the CAP pin and an inductor with a low saturation current. While the chip is designed to handle such events, the inrush current should not be allowed to exceed 0.3A. For circuits that use output capacitor values within the recommended range and have input voltages of less than 6V, inrush current remains low, posing no hazard to the device. In cases where there are large steps at V_{CC} (more than 6V) and/or a large capacitor is used at the CAP pin, inrush current should be measured to ensure safe operation.

Soft-Start

The LT8415 contains a soft-start circuit to limit peak switch currents during start-up. High start-up current is inherent in switching regulators in general since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible, which results in large peak current.

When the FBP pin voltage is generated by a resistor divider from the V_{REF} pin, the start-up current can be limited by connecting an external capacitor (typically 47nF to 220nF) to the V_{REF} pin. When the part is brought out of shutdown, this capacitor is first discharged for about 70µs (providing protection against pin glitches and slow ramping), then an internal 10µA current source pulls the V_{REF} pin slowly to 1.235V. Since the V_{OUT} voltage is set by the FBP pin voltage, the V_{OUT} voltage will also slowly increase to the regulated voltage, which results in lower peak inductor current. The voltage ramp rate on the pin can be set by the value of the V_{REF} pin capacitor.

Output Disconnect

The LT8415 has an output disconnect PMOS that blocks the load from the input during shutdown. The maximum current through the PMOS is limited to 19mA by circuitry inside the chip, helping the chip survive output shorts.

APPLICATIONS INFORMATION

If the application doesn't require the output disconnect function, the CAP and V_{OUT} pin can be shorted, and higher power converter efficiency can be achieved.

$\overline{SHDN}$ Pin Comparator and Hysteresis Current

An internal comparator compares the $\overline{SHDN}$ pin voltage with an internal voltage reference (~1.3V) which gives a precise turn-on voltage level. The internal hysteresis of this turn-on voltage is about 60mV. When the chip is turned on, and the $\overline{SHDN}$ pin voltage is close to this turn-on voltage, 0.1µA current flows out of the $\overline{SHDN}$ pin. This current is called $\overline{SHDN}$ pin hysteresis current, and will go away when the chip is off. By connecting the external resistors as in Figure 2, a user-programmable enable voltage function can be realized.

The turn-on voltage for the configuration is:

$$1.30 \bullet (1 + R1/R2)$$

and the turn-off voltage is:

$$(1.24 – R3 \bullet 10^{-7}) \bullet (1 + R1/R2) – R1 \bullet 10^{-7}$$

where R1, R2 and R3 are resistance value in Ω.

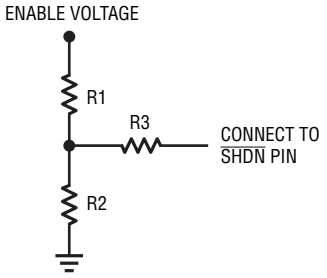


Figure 2. Programming Enable Voltage by Using External Resistors

Half-Bridge Control Signals

The half-bridge is controlled by the IN1 and IN2 pins. The IN1 and IN2 pins should be driven with a logic signal. When the chip is enabled, the OUT1 and OUT2 voltages are equal to V_{OUT} IN1 and IN2 are driven higher than 1V, and they are near GND when IN1 and IN2 are driven below 0.3V. Do not drive the IN1 or IN2 pins between 0.3V to 1V for more than 20µs since this will leave OUT1 or OUT2 in an uncertain state and may also cause shoot-through current.

Board Layout Considerations

As with all switching regulators, careful attention must be paid to the PCB layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signal of the SW pin has sharp rising and falling edges. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. In addition, the FBP pin and V_{REF} pin are sensitive to noise. Minimizing the length and area of all traces to these two pins is recommended. Recommended component placement is shown in Figure 3.

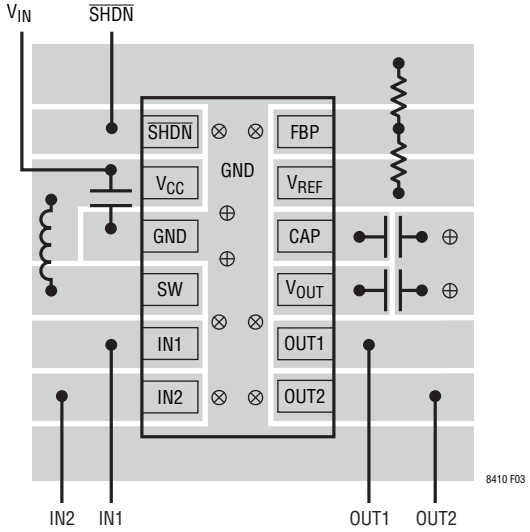
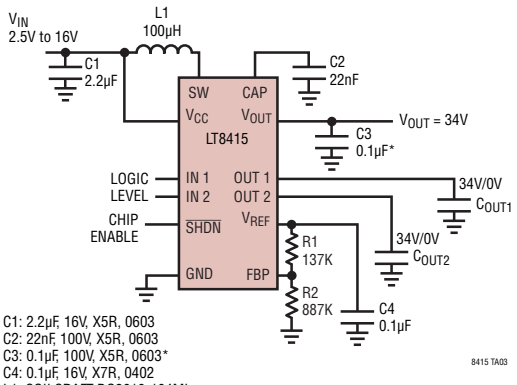


Figure 3. Recommended Board Layout

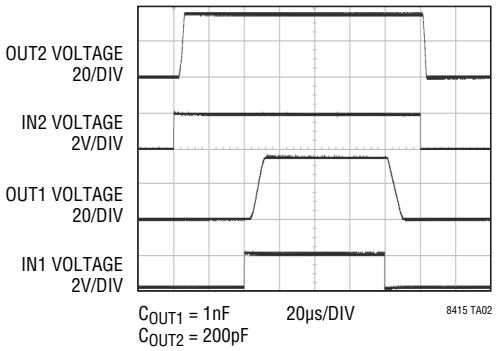
TYPICAL APPLICATIONS

Drive External Capacitors to 34V/0V with the LT8415



C1: 2.2µF, 16V, X5R, 0603
C2: 22nF, 100V, X5R, 0603
C3: 0.1µF, 100V, X5R, 0603*
C4: 0.1µF, 16V, X7R, 0402
L1: COILCRAFT DO2010-104ML
* HIGHER CAPACITANCE VALUE IS REQUIRED FOR C3 WHEN THE VIN IS HIGHER THAT 8V

Response Driving External Capacitors

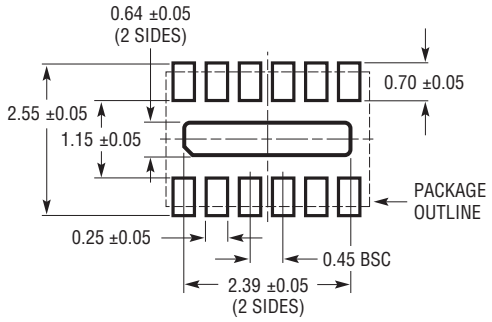


VOUT (V)	RESISTOR DIVIDER FROM VREF R1 (kΩ)/R2 (kΩ)	MAXIMUM OUTPUT CURRENT (mA)			
		VIN = 2.8V	VIN = 3.6V	VIN = 5.0V	VIN = 12V
40	NA	0.5	0.7	1.1	3.6
35	110/887	0.7	0.9	1.4	4.4
30	237/768	0.8	1.0	1.5	5.5
25	365/634	1.0	1.4	2.1	7.2
20	487/511	1.4	1.9	2.9	9.7
15	619/383	1.6	2.4	4.0	14
10	750/255	3.3	4.6	7.0	NA
5	866/127	8.0	11	17	NA

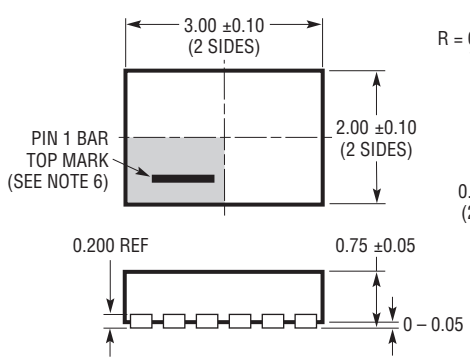
PACKAGE DESCRIPTION

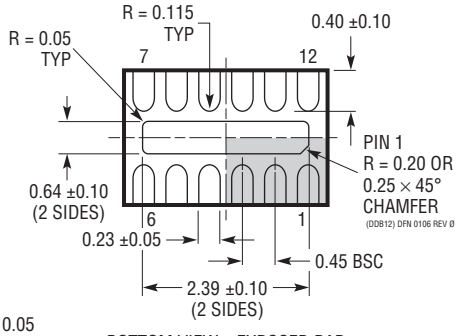
Please refer to http://www.linear.com/product/LT8415#packaging for the most recent package drawings.

DDB Package
12-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1723 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





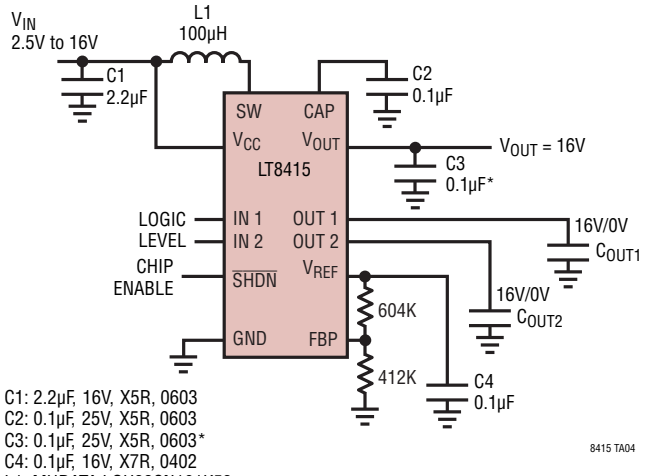
BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/15	Clarified Note 2	3
B	3/16	Corrected Switching Frequency vs Load Current graph, G01.	3

TYPICAL APPLICATION



C1: 2.2µF, 16V, X5R, 0603
C2: 0.1µF, 25V, X5R, 0603
C3: 0.1µF, 25V, X5R, 0603*
C4: 0.1µF, 16V, X7R, 0402
L1: MURATA LQH32CN101K53
* HIGHER CAPACITANCE VALUE IS REQUIRED FOR C3 WHEN THE V_{IN} IS HIGHER THAT 8V

Figure 4. Drive External Capacitors to 16V/0V with the LT8415

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1930/LT1930A	1A (I_{SW}), 1.2MHz/2.2MHz, High Efficiency Step-Up DC/DC Converters	V_{IN} = 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2mA/5.5mA, I_{SD} < 1µA, ThinSOT Package
LT1945 (Dual)	Dual Output, Boost/Inverter, 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN} = 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 40µA, I_{SD} < 1µA, 10-Lead MS Package
LT1946/LT1946A	1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converters	V_{IN} = 2.45V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} < 1µA, 8-Lead MS Package
LT3467/LT3467A	1.1A (I_{SW}), 1.3MHz/2.1MHz, High Efficiency Step-Up DC/DC Converters with Soft-Start	V_{IN} = 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} < 1µA, ThinSOT Package
LT3464	85mA (I_{SW}), High Efficiency Step-Up DC/DC Converter with Integrated Schottky and PNP Disconnect	V_{IN} = 2.3V to 10V, $V_{OUT(MAX)}$ = 34V, I_Q = 25µA, I_{SD} < 1µA, ThinSOT Package
LT3463/LT3463A	Dual Output, Boost/Inverter, 250mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converters with Integrated Schottkys	V_{IN} = 2.3V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} < 1µA, DFN Package
LT3471	Dual Output, Boost/Inverter, 1.3A (I_{SW}), High Efficiency Boost-Inverting DC/DC Converter	V_{IN} = 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} < 1µA, DFN Package
LT3473/LT3473A	1A (I_{SW}), 1.2MHz, High Efficiency Step-Up DC/DC Converter with integrated Schottky Diode and Output Disconnect	V_{IN} = 2.2V to 16V, $V_{OUT(MAX)}$ = 36V, I_Q = 100µA, I_{SD} < 1µA, DFN Package
LT3494/LT3494A	180mA/350mA (I_{SW}), High Efficiency, Low Noise Step-Up DC/DC Converter with Output Disconnect	V_{IN} = 2.1V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LT3580	2A, 40V, 2.5MHz Boost DC/DC Converter	V_{IN} = 2.5V to 32V, $V_{OUT(MAX)}$ = 40V, I_Q = 1mA, I_{SD} <1µA, MS8E 3mm × 3mm DFN-8 Package
LT3495/LT3495B/ LT3495-1/LT3495B-1	650mA/350mA (I_{SW}), High Efficiency, Low Noise Step-Up DC/DC Converter with Output Disconnect	V_{IN} = 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 60µA, I_{SD} < 1µA, DFN Package
LT8410/LT8410-1	25mA/8mA (I_{SW}), High Efficiency, Low Noise Step-Up DC/DC Converter with Output Disconnect	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 8.5µA, I_{SD} < 1µA, DFN Package

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