



THE DATASHEET OF SN65LVELT23DGKR



3.3-V Dual Differential LVPECL/LVDS Buffer to LVTTTL Translator

FEATURES

- Dual 3.3-V Differential LVPECL/LVDS to LVTTTL Buffer Translator
- 24-mA LVTTTL Outputs
- Operating Range
 - PECL $V_{CC} = 3\text{ V to }3.6\text{ V}$ With $GND = 0\text{ V}$
- Support for Clock Frequencies to >180 MHz
- 2-ns Typical Propagation Delay
- Internal Input Pullup and Pulldown Resistors
- Built-in Temperature Compensation
- Drop-In Compatible to MC100LVELT23

APPLICATIONS

- Data and Clock Transmission Over Backplane
- Signaling Level Conversion for Clock or Data

DESCRIPTION

The SN65LVELT23 is a low-power dual LVPECL/LVDS to LVTTTL translator device. The device includes circuitry to maintain inputs at $V_{CC}/2$ when left open. The SN65LVELT23 is housed in an industry-standard SOIC-8 package and is also available in a TSSOP-8 option.

PINOUT ASSIGNMENT

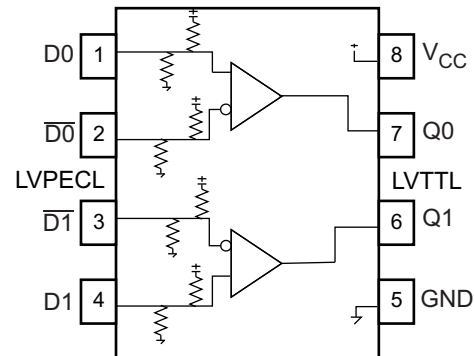


Table 1. PIN DESCRIPTION

PIN	FUNCTION
$D_0, \bar{D}_0, D_1, \bar{D}_1$	PECL inputs
Q_0, Q_1	TTL outputs
V_{CC}	Positive supply
GND	Ground

ORDERING INFORMATION⁽¹⁾

PART NUMBER	PART MARKING	PACKAGE	LEAD FINISH
SN65LVELT23D	LVEL23	SOIC	NiPdAu
SN65LVELT23DGK	SIMI	MSOP	NiPdAu

(1) Devices with lead (Pb)-bearing terminals not initially available; contact [TI sales representative](#) for further information.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	CONDITION	VALUE	UNIT
Absolute supply voltage, V_{CC}		3.8	V
Absolute input voltage, V_I	$GND = 0$ and $V_I \leq V_{CC}$	0 to 3.8	V
Output current	Continuous	50	mA
	Surge	100	
Operating temperature range		–40 to 85	°C
Storage temperature range		–65 to 150	°C

POWER DISSIPATION RATINGS

PACKAGE	CIRCUIT-BOARD MODEL	POWER RATING $T_A < 25^\circ\text{C}$ (mW)	THERMAL RESISTANCE, JUNCTION-TO-AMBIENT, NO AIRFLOW	DERATING FACTOR $T_A > 25^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
SOIC	Low-K	719	139	7	288
	High-K	840	119	8	336
MSOP	Low-K	469	213	5	188
	High-K	527	189	5	211

THERMAL CHARACTERISTICS

PARAMETER		PACKAGE	VALUE	UNIT
θ_{JB}	Junction-to-board thermal resistance	SOIC	79	°C/W
		MSOP	120	
θ_{JC}	Junction-to-case thermal resistance	SOIC	98	°C/W
		MSOP	74	

KEY ATTRIBUTES

CHARACTERISTICS	VALUE
Moisture sensitivity level	Level 1
Flammability rating (oxygen index: 28 to 34)	UL 94 V-0 at 0.125 in. (3.18 mm)
ESD human-body model	2 kV
ESD charged-device model	1.5 kV
Internal pulldown resistor	50 k Ω
Internal pullup resistor	50 k Ω
Meets or exceeds JEDEC Spec EIA/JESD78 latchup test	

LVTTTL OUTPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0\text{ V}$)⁽²⁾

PARAMETER	CONDITION	–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{OS} Output short-circuit current		–120		–30	–120	–30	–120	–30	–30	mA	
V_{OH} Output high voltage ⁽³⁾	$I_{OH} = -3.0\text{ mA}$	2.4			2.4		2.4			V	
V_{OL} Output low voltage	$I_{OL} = 24\text{ mA}$			0.5			0.5		0.5	V	

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) All values vary 1:1 with V_{CC} ; V_{CC} can vary $\pm 0.3\text{ V}$
- (3) LVTTTL output $R_L = 500\ \Omega$ to GND

LVPECL INPUT DC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$)⁽²⁾

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{CCH} Power-supply current (outputs set to high)		10	21	25	10	21	25	10	21	25	mA
I_{CCL} Power-supply current (outputs set to low)		15	21	27	15	21	27	15	21	27	mA
V_{IH} Input high voltage ⁽³⁾		2135		2420	2135		2420	2135		2420	mV
V_{IL} Input low voltage ⁽³⁾		1490		1825	1490		1825	1490		1825	mV
V_{IHCMR} Input high-voltage common-mode range (differential) ⁽⁴⁾		1.2		V_{CC}	1.2		V_{CC}	1.2		V_{CC}	V
I_{IH} Input high current				150			150			150	μA
I_{IL} Input low current		–150			–150			–150			μA

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input and output parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.
- (3) LVTTTL output $R_L = 500\ \Omega$ to GND
- (4) V_{IHCMR} minimum varies 1:1 with GND, V_{IHCMR} maximum varies 1:1 with V_{CC} .

AC CHARACTERISTICS⁽¹⁾ ($V_{CC} = 3.3\text{ V}$; $GND = 0.0\text{ V}$)⁽²⁾ (3)

PARAMETER		–40°C			25°C			85°C			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX} Maximum switching frequency ⁽⁴⁾		180	300		180	300		180	300		MHz
t_{PLH}/t_{PHL} Propagation delay to output at 1.5 V		1.2	1.6	2.2	1.2	1.7	2.2	1.2	1.8	2.2	ns
t_{SK++} Output-to-output skew++			30	160		30	150		30	150	ps
t_{SK--} Output to output skew--			45	180		45	160		45	135	ps
t_{SKPP} Part- to-part skew ⁽⁵⁾			60	200		60	200		70	200	ps
t_{JITTER} Random clock jitter (RMS)			4	10		4	10		4	10	ps
V_{PP} Input voltage swing ⁽⁶⁾		200	800	1000	200	800	1000	200	800	1000	mV
t_r/t_f Output rise/fall times (0.8 V – 2 V)		330	585	900	330	600	900	330	630	900	ps

- (1) Device meets the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm (2.54 m/s). Electrical parameters are assured only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.
- (2) Input parameters vary 1:1 with V_{CC} . V_{CC} can vary $\pm 0.3\text{ V}$.
- (3) TTL output $R_L = 500\ \Omega$ to GND and $C_L = 20\text{ pF}$ to GND; see [Figure 1](#).
- (4) f_{max} measured for $V_{OL} < 0.5\text{ V}$ and $V_{OH} > 2.4\text{ V}$. See [Figure 5](#).
- (5) Skews are measured between outputs under identical conditions.
- (6) 200-mV input assured full logic swing at the output.

Typical Output Loading Used for Device Evaluation

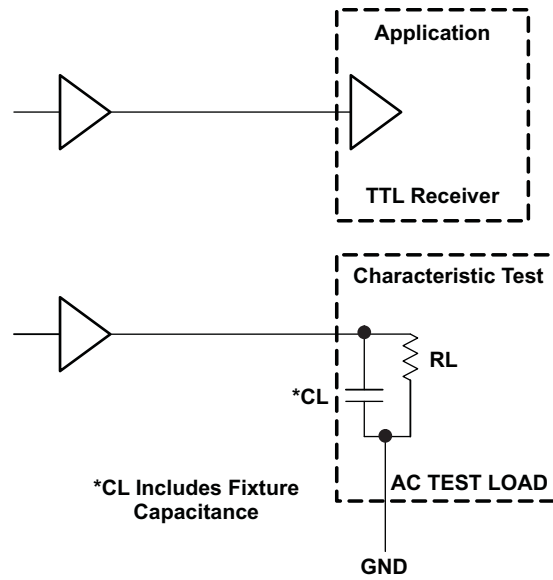


Figure 1. TTL Output Loading Used for Device Evaluation

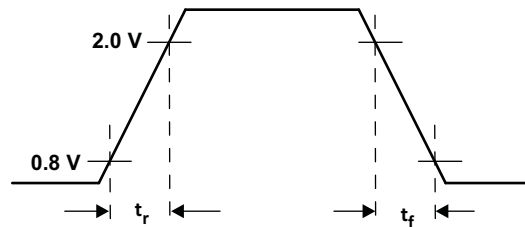


Figure 2. Output Rise and Fall Times

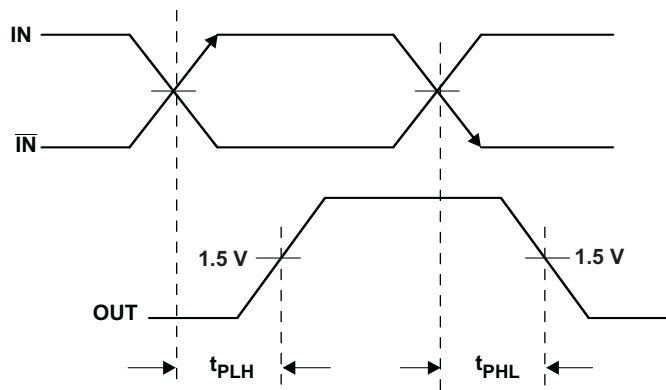


Figure 3. Output Propagation Delay

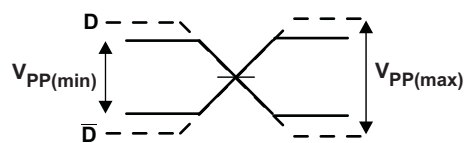


Figure 4. Input Voltage Swing

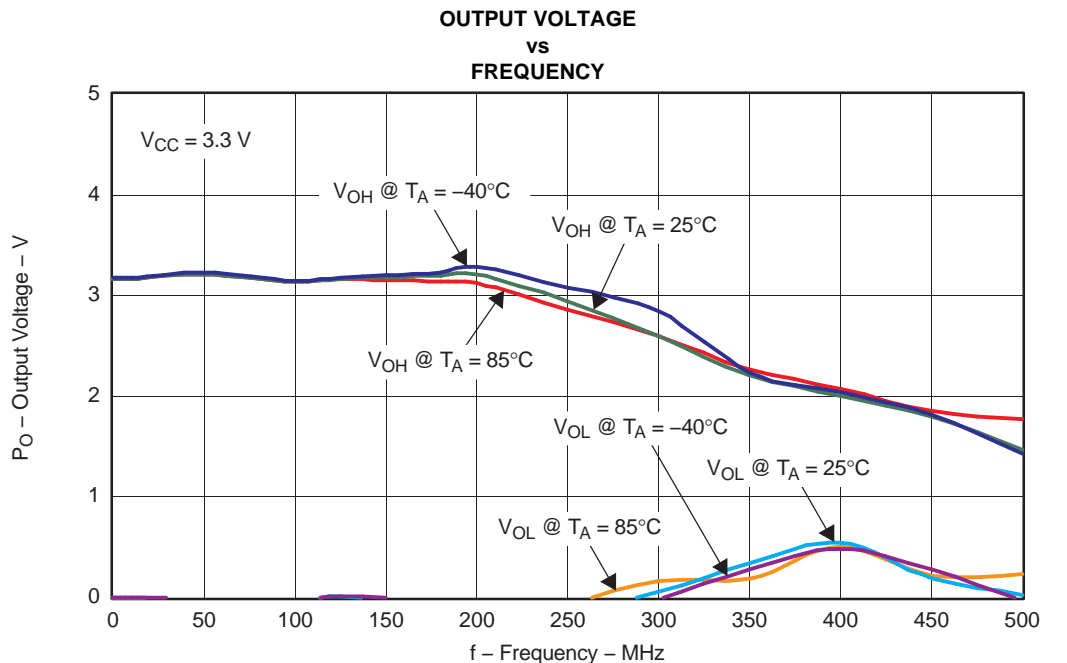


Figure 5.

G001

REVISION HISTORY

Changes from Revision Original (June 2009) to Revision A	Page
• Changed MIN and MAX values for t_{PLH}/t_{PHL} in AC CHARACTERISTICS table.....	3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVELT23D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23	Samples
SN65LVELT23DGK	ACTIVE	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	SIMI	Samples
SN65LVELT23DGKR	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU Call TI	Level-1-260C-UNLIM	-40 to 85	SIMI	Samples
SN65LVELT23DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVEL23	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

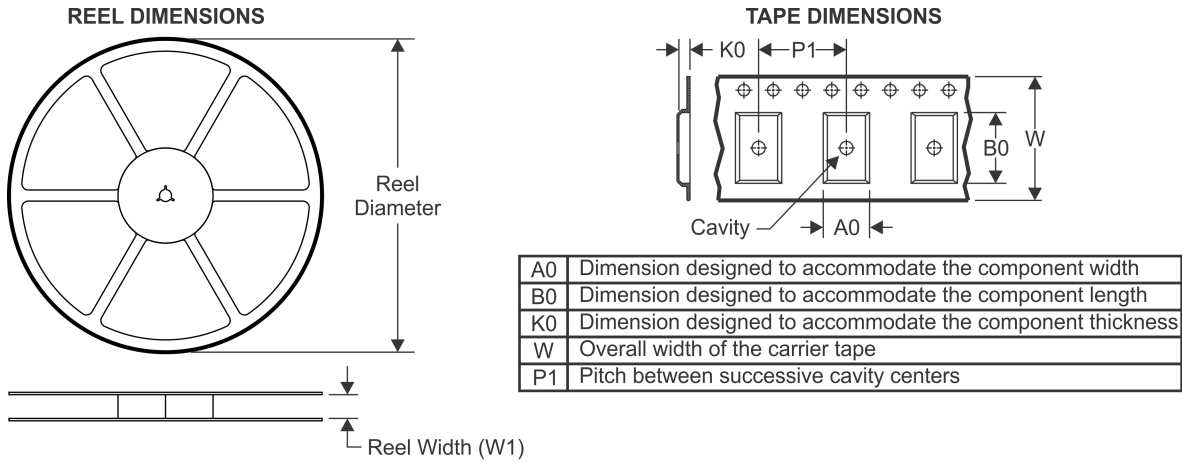
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

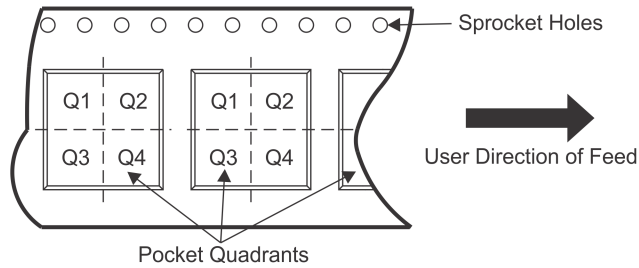
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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVELT23DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVELT23DR	SOIC	D	8	2500	367.0	367.0	35.0



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

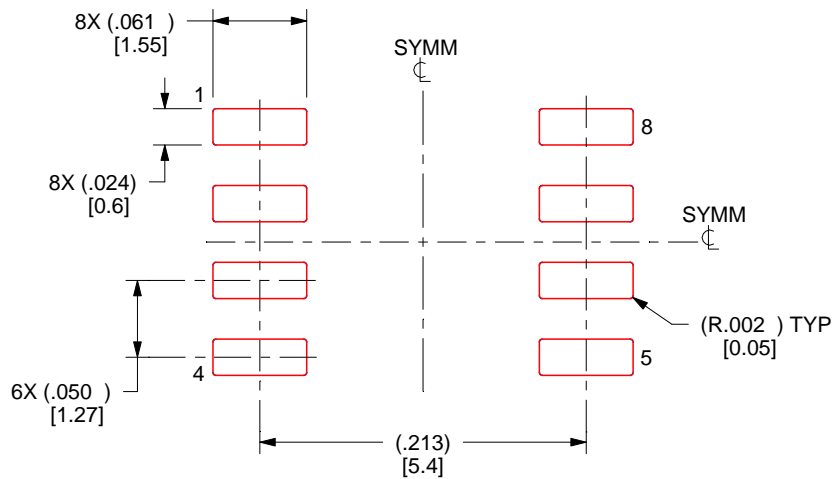
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

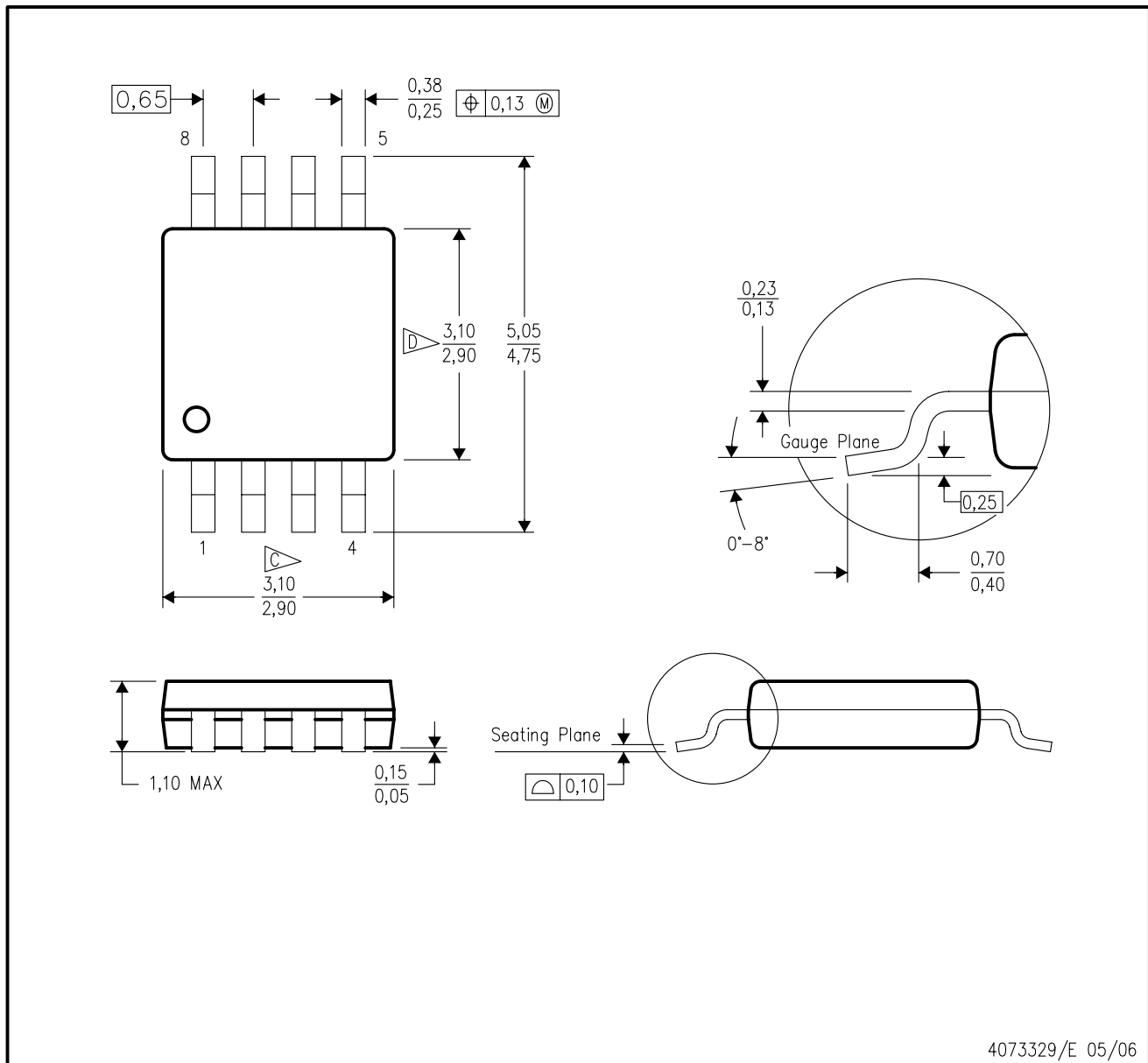
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NOTES: (continued)

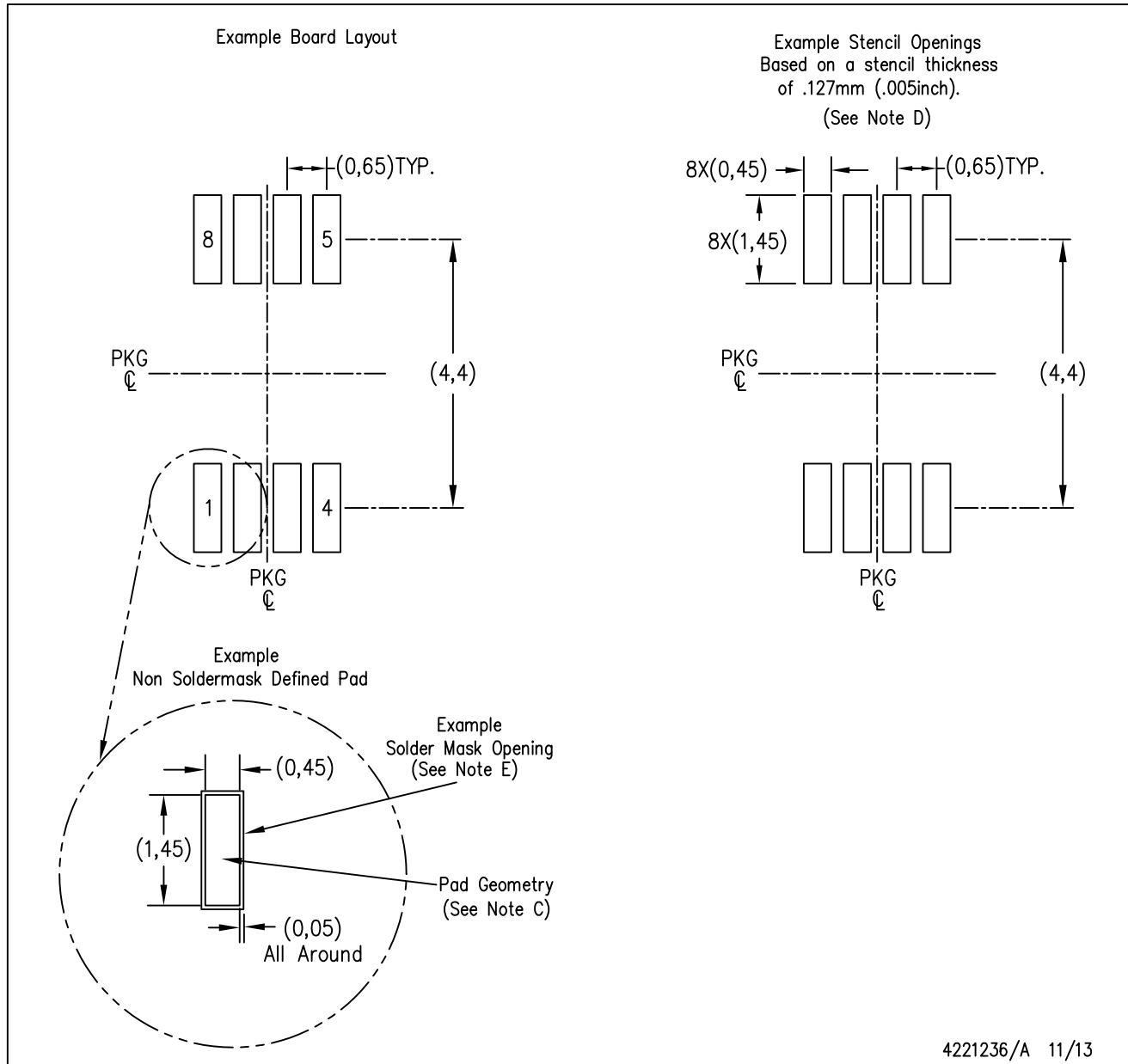
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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