



**THE DATASHEET OF
AON6906A**



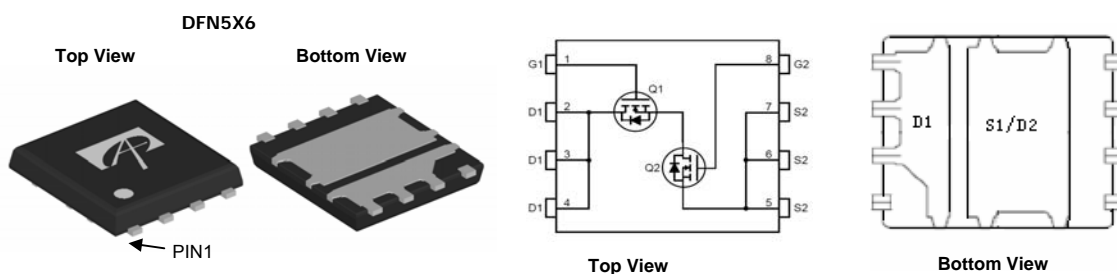
General Description

The AON6906A is designed to provide a high efficiency synchronous buck power stage with optimal layout and board space utilization. It includes two specialized MOSFETs in a dual Power DFN5x6A package. The Q1 "High Side" MOSFET is designed to minimize switching losses. The Q2 "Low Side" MOSFET is designed for low $R_{DS(ON)}$ to reduce conduction losses. Power losses are minimized due to an extremely low combination of $R_{DS(ON)}$ and C_{rss} . In addition, switching behavior is well controlled with a "Schottky style" soft recovery body diode.

Product Summary

| | Q1 | Q2 |
|------------------------------------|-----------------|-----------------|
| V_{DS} | 30V | 30V |
| I_D (at $V_{GS}=10V$) | 37A | 48A |
| $R_{DS(ON)}$ (at $V_{GS}=10V$) | <14.4m Ω | <11.7m Ω |
| $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) | <21.3m Ω | <17.5m Ω |

100% UIS Tested
 100% Rg Tested



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

| Parameter | Symbol | Max Q1 | Max Q2 | Units | |
|--|------------------|-------------------------|--------|------------------|---|
| Drain-Source Voltage | V_{DS} | 30 | | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | V | |
| Continuous Drain Current | I_D | $T_C=25^\circ\text{C}$ | 37 | 48 | A |
| | | $T_C=100^\circ\text{C}$ | 23 | 30 | |
| Pulsed Drain Current ^c | I_{DM} | 85 | 100 | | |
| Continuous Drain Current | I_{DSM} | $T_A=25^\circ\text{C}$ | 9.1 | 10 | A |
| | | $T_A=70^\circ\text{C}$ | 7.2 | 8.1 | |
| Avalanche Current ^c | I_{AS}, I_{AR} | 21 | 23 | A | |
| Avalanche Energy $L=0.1\text{mH}$ ^c | E_{AS}, E_{AR} | 22 | 26 | mJ | |
| Power Dissipation ^B | P_D | $T_C=25^\circ\text{C}$ | 31 | 45 | W |
| | | $T_C=100^\circ\text{C}$ | 12.5 | 18 | |
| Power Dissipation ^A | P_{DSM} | $T_A=25^\circ\text{C}$ | 1.9 | 2 | W |
| | | $T_A=70^\circ\text{C}$ | 1.2 | 1.3 | |
| Junction and Storage Temperature Range | T_J, T_{STG} | -55 to 150 | | $^\circ\text{C}$ | |

Thermal Characteristics

| Parameter | Symbol | Typ Q1 | Typ Q2 | Max Q1 | Max Q2 | Units | |
|--|-----------------|---------------------|--------|--------|--------|--------------------|--------------------|
| Maximum Junction-to-Ambient ^A | $R_{\theta JA}$ | $t \leq 10\text{s}$ | 29 | 27 | 35 | 32 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Ambient ^{A D} | | Steady-State | 56 | 51 | 67 | 61 | $^\circ\text{C/W}$ |
| Maximum Junction-to-Case | $R_{\theta JC}$ | 3.3 | 2.3 | 4 | 2.8 | $^\circ\text{C/W}$ | |

Q1 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|------------|------------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =30V, V _{GS} =0V T _J =55°C | | | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±20V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} I _D =250μA | 1.3 | 1.8 | 2.4 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 85 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =9.1A T _J =125°C | | 12 17.5 | 14.4 21 | mΩ |
| | | V _{GS} =4.5V, I _D =9.1A | | 17 | 21.3 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =9.1A | | 30 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.73 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 33 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | 400 | 510 | 670 | pF |
| C _{oss} | Output Capacitance | | 150 | 220 | 310 | pF |
| C _{rss} | Reverse Transfer Capacitance | | 13 | 22 | 38 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.9 | 1.8 | 2.7 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _g (10V) | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =9.1A | 5.9 | 7.4 | 9 | nC |
| Q _g (4.5V) | Total Gate Charge | | 2.6 | 3.3 | 4.0 | nC |
| Q _{gs} | Gate Source Charge | | 1.2 | 1.5 | 1.8 | nC |
| Q _{gd} | Gate Drain Charge | | 0.8 | 1.4 | 2 | nC |
| t _{D(on)} | Turn-On Delay Time | V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω | | 4.3 | | ns |
| t _r | Turn-On Rise Time | | | 8 | | ns |
| t _{D(off)} | Turn-Off Delay Time | | | 15.8 | | ns |
| t _f | Turn-Off Fall Time | | | 3.4 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =9.1A, dI/dt=500A/μs | 7.2 | 9 | 11 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =9.1A, dI/dt=500A/μs | 11.8 | 14.7 | 17.7 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

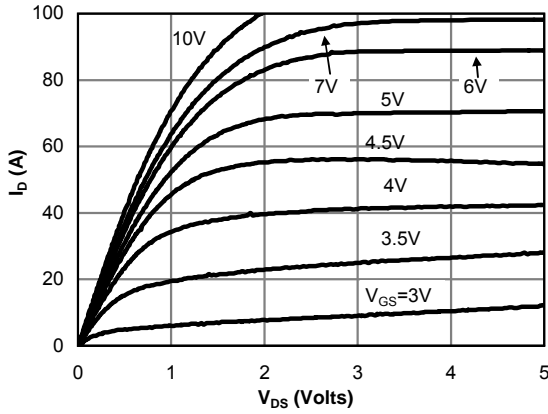


Fig 1: On-Region Characteristics (Note E)

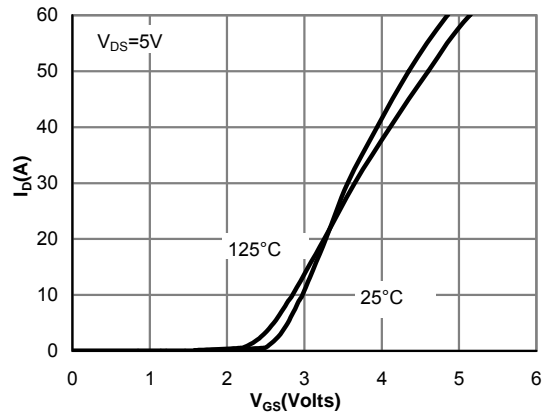


Figure 2: Transfer Characteristics (Note E)

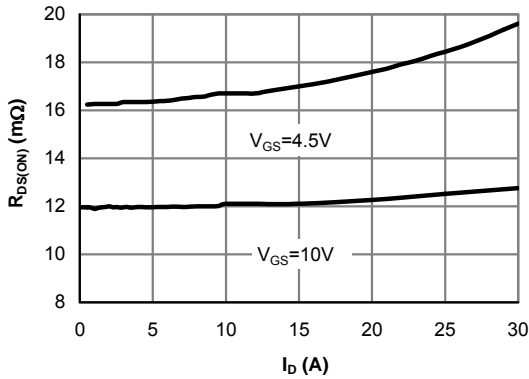


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

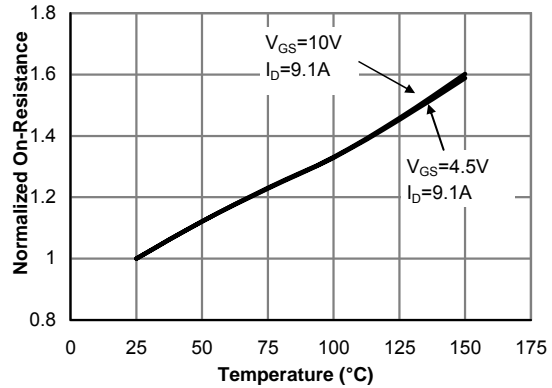


Figure 4: On-Resistance vs. Junction Temperature (Note E)

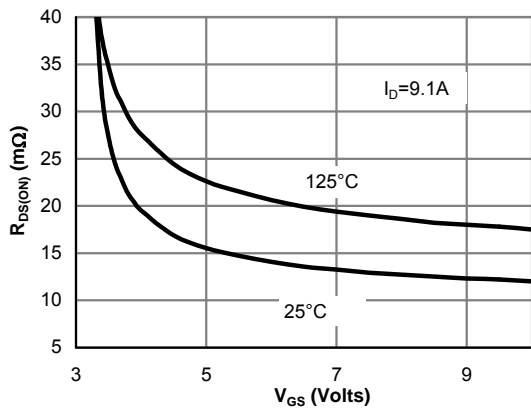


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

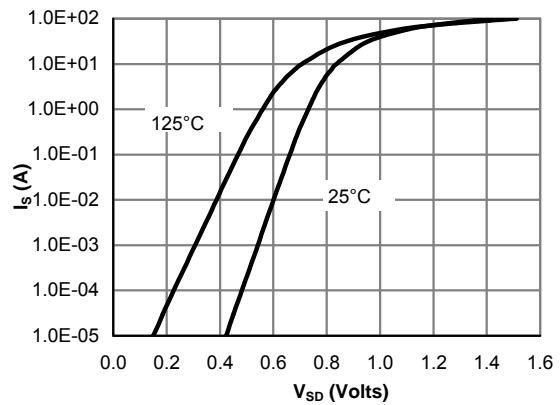


Figure 6: Body-Diode Characteristics (Note E)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

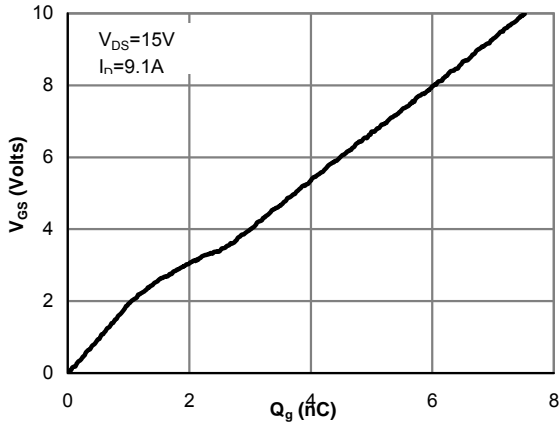


Figure 7: Gate-Charge Characteristics

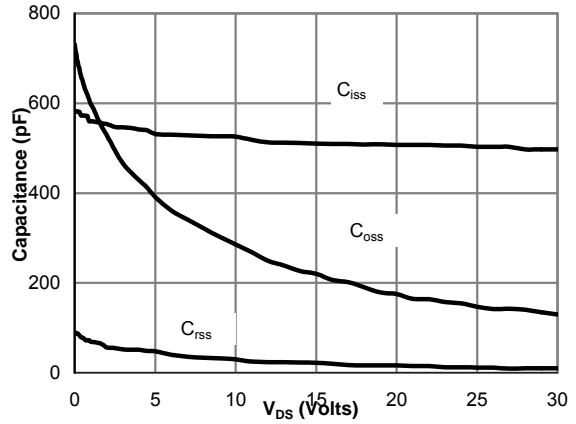


Figure 8: Capacitance Characteristics

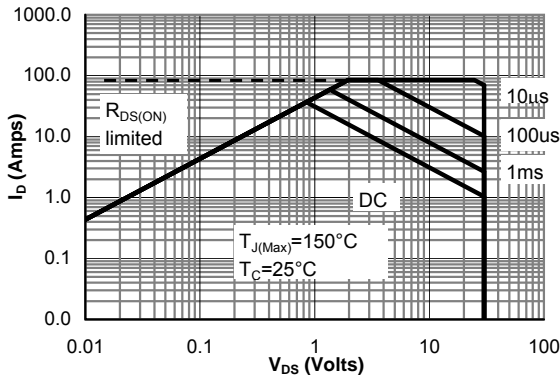


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

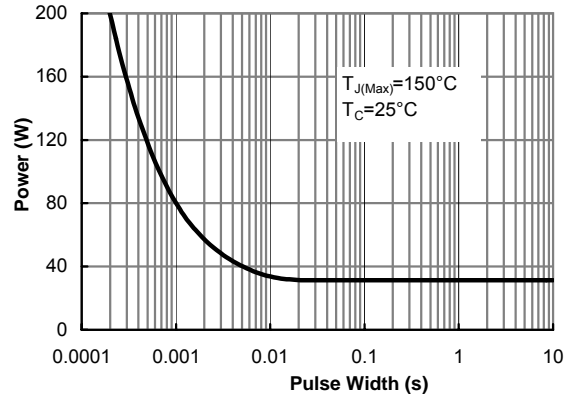


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

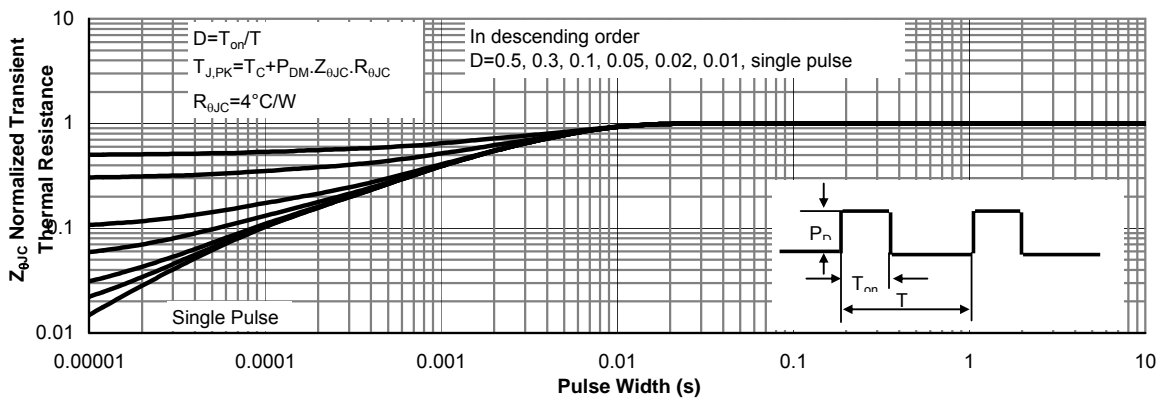


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q1-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

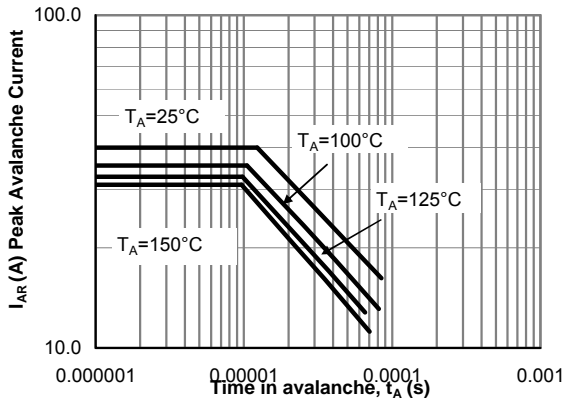


Figure 12: Single Pulse Avalanche capability (Note C)

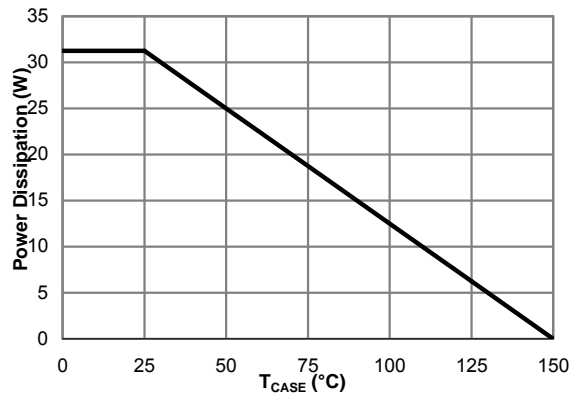


Figure 13: Power De-rating (Note F)

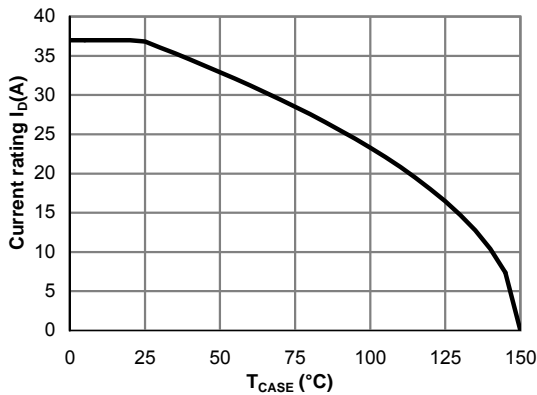


Figure 14: Current De-rating (Note F)

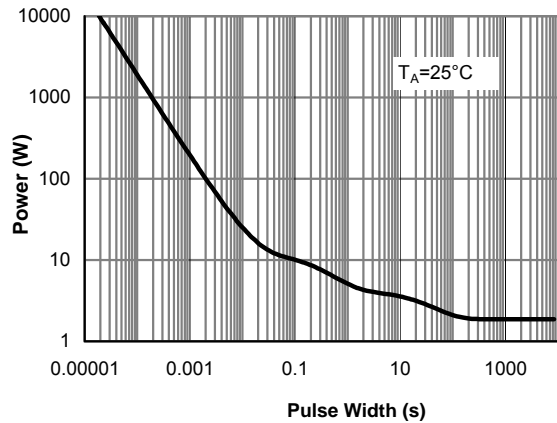


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

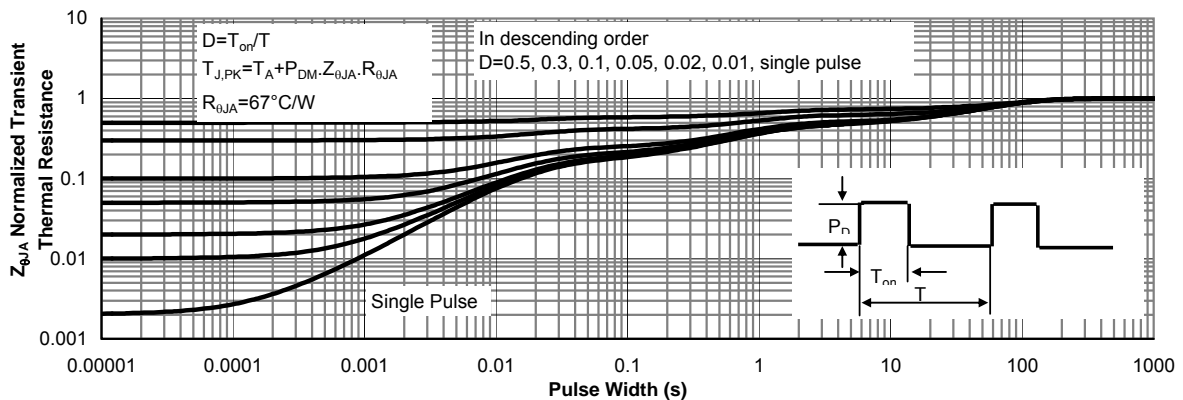


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

Q2 Electrical Characteristics (T_J=25°C unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-----------------------------|---------------------------------------|--|------|------|--------|-------|
| STATIC PARAMETERS | | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | I _D =250μA, V _{GS} =0V | 30 | | | V |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} =30V, V _{GS} =0V T _J =55°C | | | 1 5 | μA |
| I _{GSS} | Gate-Body leakage current | V _{DS} =0V, V _{GS} = ±20V | | | 100 | nA |
| V _{GS(th)} | Gate Threshold Voltage | V _{DS} =V _{GS} I _D =250μA | 1.3 | 1.8 | 2.3 | V |
| I _{D(ON)} | On state drain current | V _{GS} =10V, V _{DS} =5V | 100 | | | A |
| R _{DS(ON)} | Static Drain-Source On-Resistance | V _{GS} =10V, I _D =10A T _J =125°C | | 9.7 | 11.7 | mΩ |
| | | | | 15.1 | 18.2 | |
| | | V _{GS} =4.5V, I _D =10A | | 14 | 17.5 | mΩ |
| g _{FS} | Forward Transconductance | V _{DS} =5V, I _D =10A | | 25 | | S |
| V _{SD} | Diode Forward Voltage | I _S =1A, V _{GS} =0V | | 0.72 | 1 | V |
| I _S | Maximum Body-Diode Continuous Current | | | | 48 | A |
| DYNAMIC PARAMETERS | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} =0V, V _{DS} =15V, f=1MHz | 450 | 570 | 750 | pF |
| C _{oss} | Output Capacitance | | 180 | 260 | 370 | pF |
| C _{rss} | Reverse Transfer Capacitance | | 12 | 20 | 35 | pF |
| R _g | Gate resistance | V _{GS} =0V, V _{DS} =0V, f=1MHz | 0.9 | 1.8 | 2.7 | Ω |
| SWITCHING PARAMETERS | | | | | | |
| Q _{g(10V)} | Total Gate Charge | V _{GS} =10V, V _{DS} =15V, I _D =10A | 6.5 | 8.2 | 10 | nC |
| Q _{g(4.5V)} | Total Gate Charge | | 2.8 | 3.5 | 4.2 | nC |
| Q _{gs} | Gate Source Charge | | 1.2 | 1.6 | 2 | nC |
| Q _{gd} | Gate Drain Charge | | 0.8 | 1.4 | 2 | nC |
| t _{D(on)} | Turn-On Delay Time | V _{GS} =10V, V _{DS} =15V, R _L =0.75Ω, R _{GEN} =3Ω | | 4.1 | | ns |
| t _r | Turn-On Rise Time | | | 7.8 | | ns |
| t _{D(off)} | Turn-Off Delay Time | | | 15.2 | | ns |
| t _f | Turn-Off Fall Time | | | 3.3 | | ns |
| t _{rr} | Body Diode Reverse Recovery Time | I _F =10A, dI/dt=500A/μs | 6.8 | 8.6 | 10 | ns |
| Q _{rr} | Body Diode Reverse Recovery Charge | I _F =10A, dI/dt=500A/μs | 11.3 | 14.1 | 17 | nC |

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=150°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by package.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

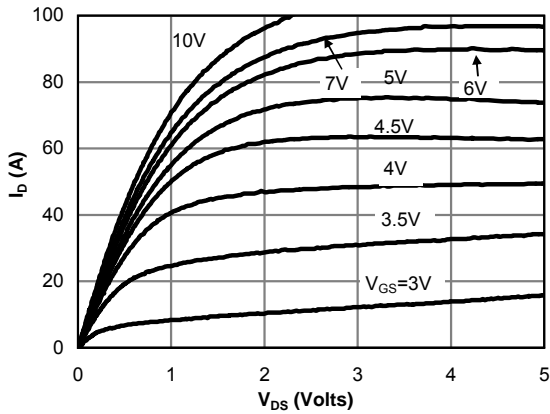


Fig 1: On-Region Characteristics (Note E)

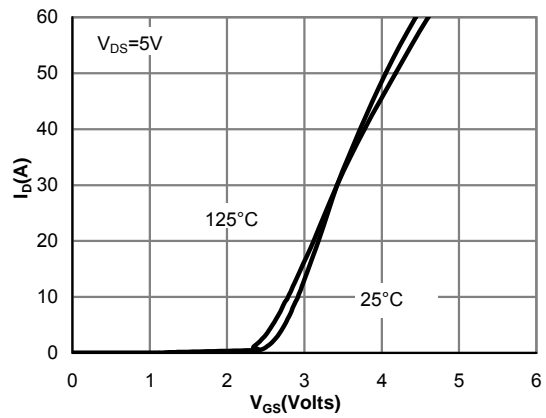


Figure 2: Transfer Characteristics (Note E)

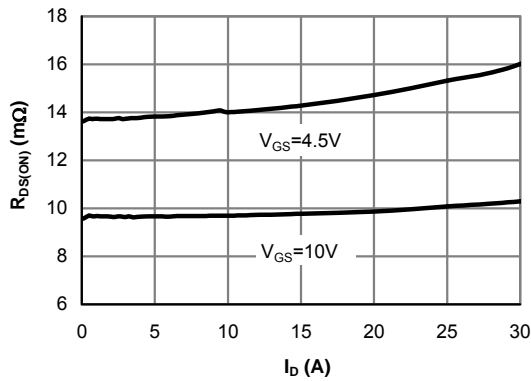


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

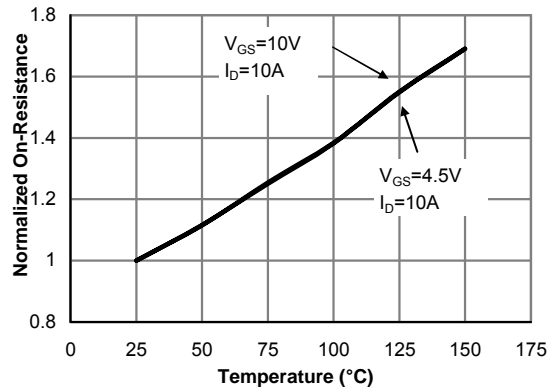


Figure 4: On-Resistance vs. Junction Temperature (Note E)

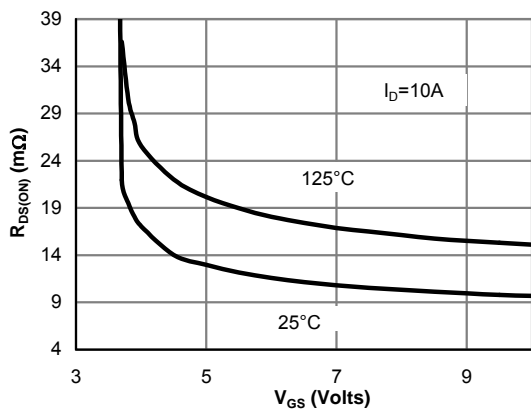


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

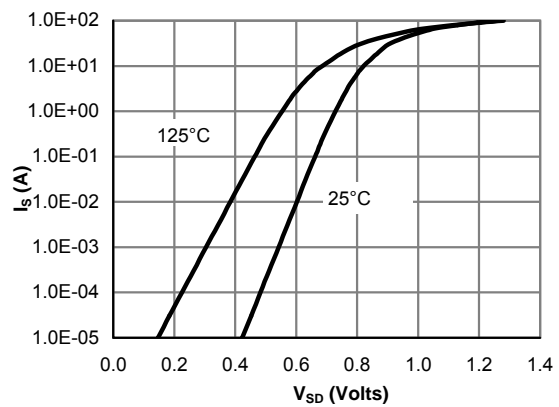


Figure 6: Body-Diode Characteristics (Note E)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

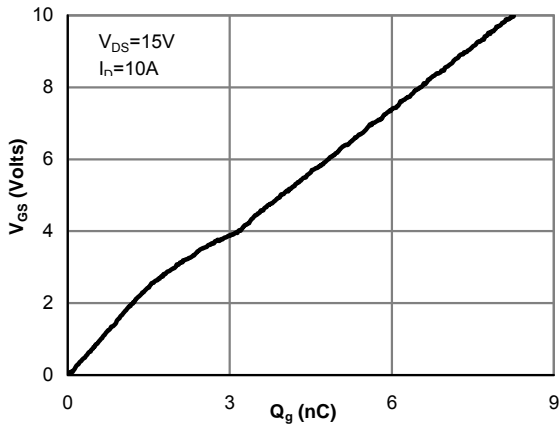


Figure 7: Gate-Charge Characteristics

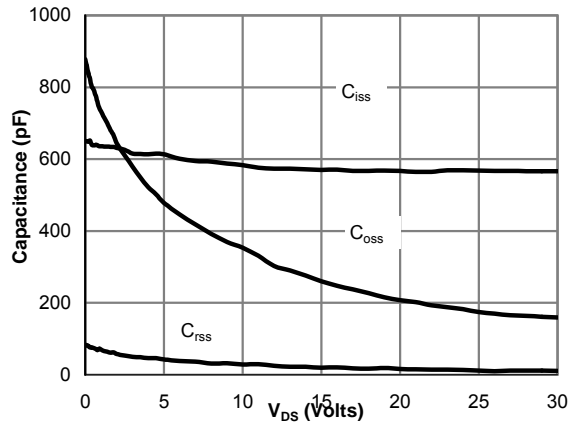


Figure 8: Capacitance Characteristics

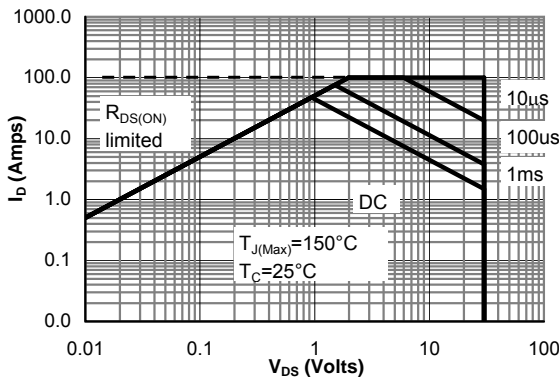


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

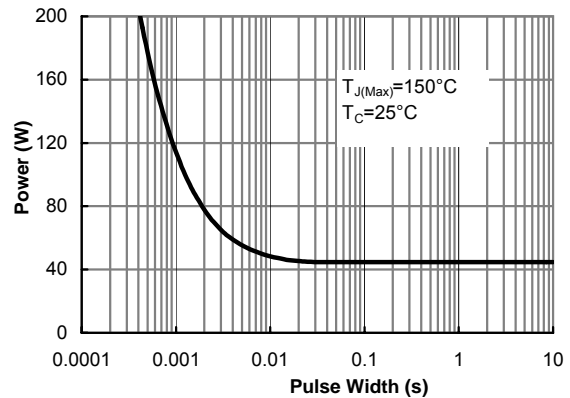


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

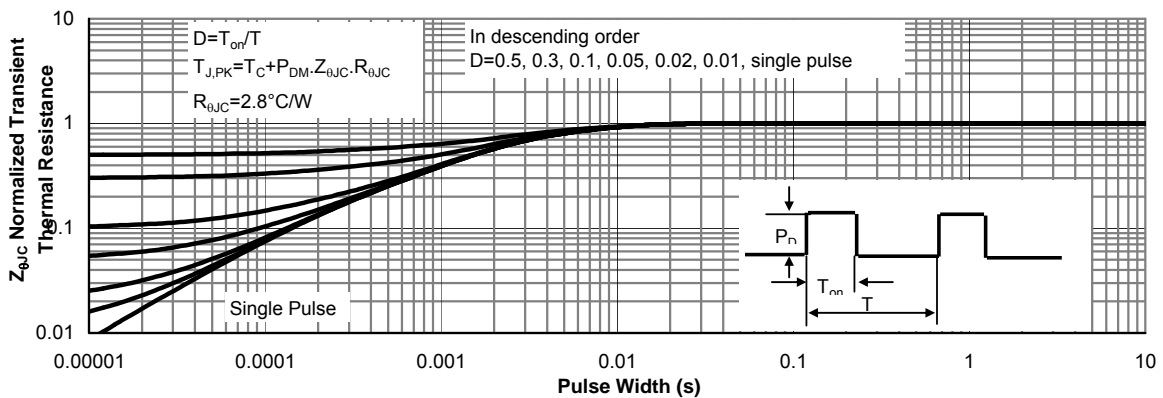


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

Q2-CHANNEL: TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

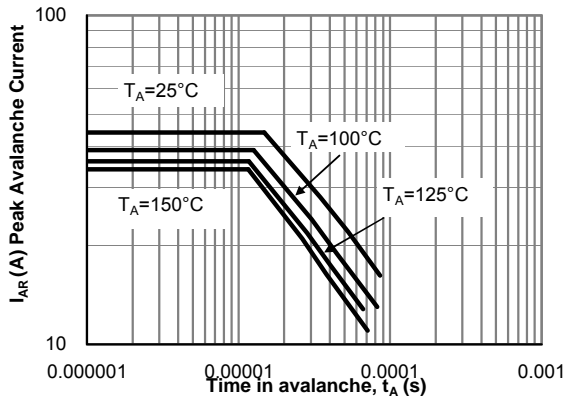


Figure 12: Single Pulse Avalanche capability (Note C)

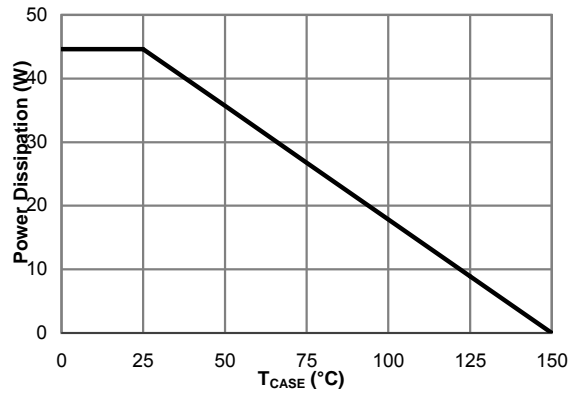


Figure 13: Power De-rating (Note F)

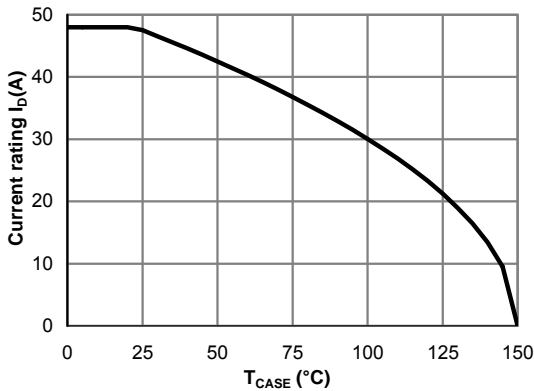


Figure 14: Current De-rating (Note F)

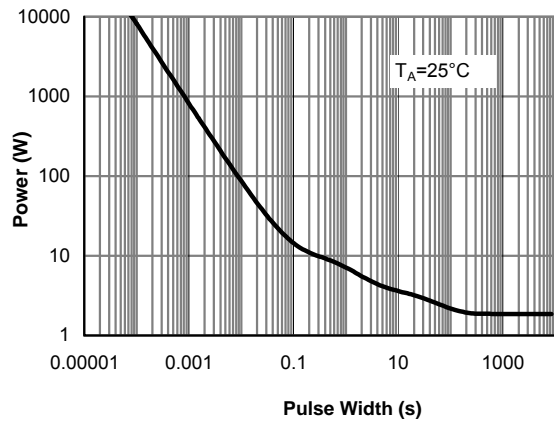


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

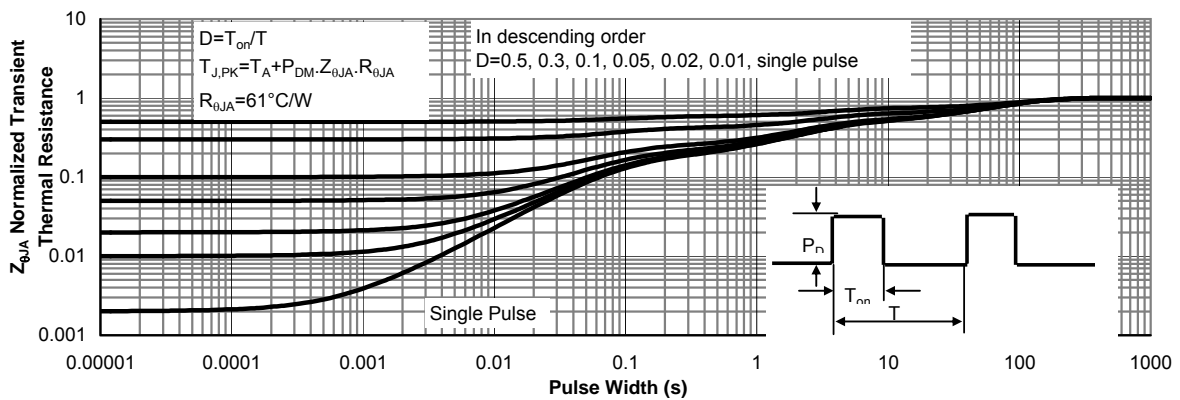
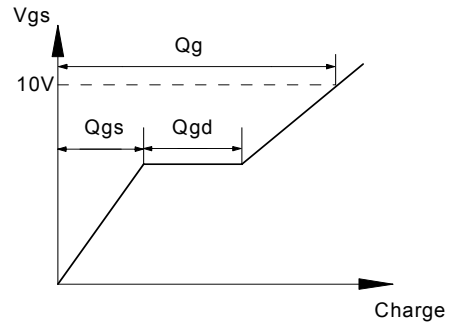
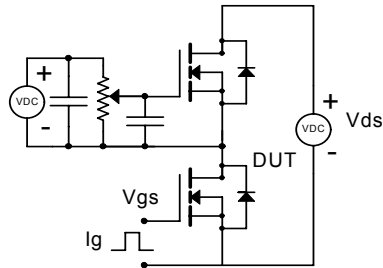
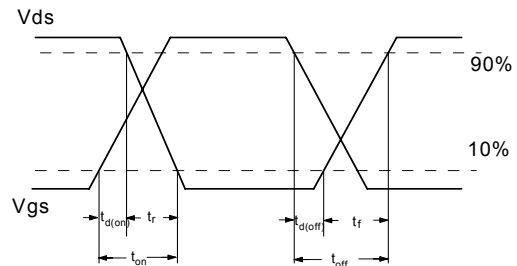
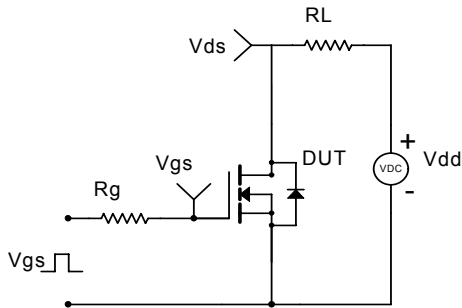


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

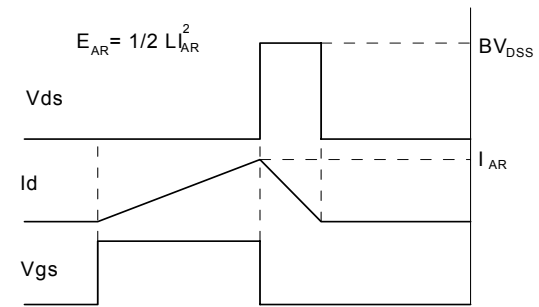
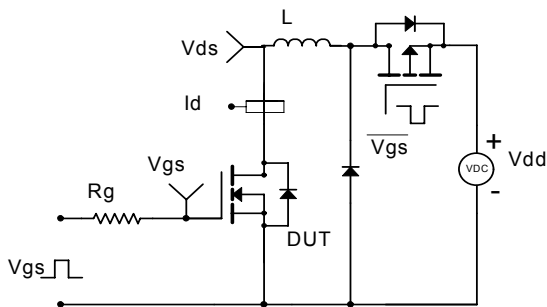
Gate Charge Test Circuit & Waveform



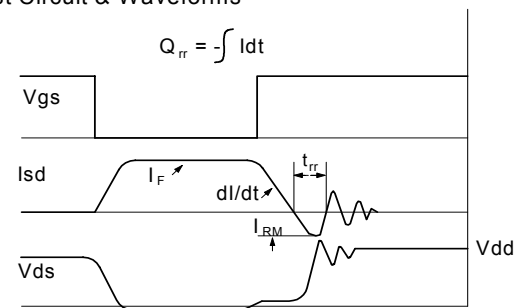
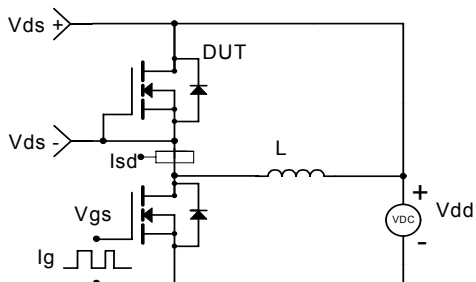
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management