WINSOURCE ELECTRONICS

THE DATASHEET OF

AD9882KSTZ-140

Dual Interface for Flat Panel Displays

AD9882A

FEATURES

Analog interface
- 140 MSPS maximum conversion rate
- Programmable analog bandwidth
- 0.5 V to 1.0 V analog input range
- 500 ps p-p PLL clock jitter at 140 MSPS
- 3.3 V power supply
- Full sync processing
- Midscale clamping
- 4:2:2 output format mode

Digital interface
- DVI 1.0 compatible interface
- 112 MHz operation
- High skew tolerance of 1 full input clock
- Sync detect for hot plugging
- Supports high bandwidth digital content protection

APPLICATIONS

- RGB graphics processing
- LCD monitors and projectors
- Plasma display panels
- Scan converter
- Microdisplays
- Digital TV

GENERAL DESCRIPTION

The AD9882A offers designers the flexibility of an analog interface and a digital visual interface (DVI) receiver integrated on a single chip. Also included is support for high bandwidth digital content protection (HDCP).

Analog Interface

The AD9882A is a complete, 8-bit, 140 MSPS monolithic analog interface optimized for capturing RGB graphics signals from personal computers and workstations. Its 140 MSPS encode rate capability and full power analog bandwidth of 300 MHz sup-ports resolutions up to SXGA (1280 × 1024 at 75 Hz).

The analog interface includes a 140 MHz triple ADC with internal 1.25 V reference, a phase-locked loop (PLL), programmable gain, offset, and clamp control. The user provides only a 3.3 V power supply, analog input, and Hsync. Three-state CMOS outputs can be powered from 2.2 V to 3.3 V.

The AD9882A's on-chip PLL generates a pixel clock from Hsync. Pixel clock output frequencies range from 12 MHz to 140 MHz. PLL clock jitter is typically 500 ps p-p at 140 MSPS.

FUNCTIONAL BLOCK DIAGRAM

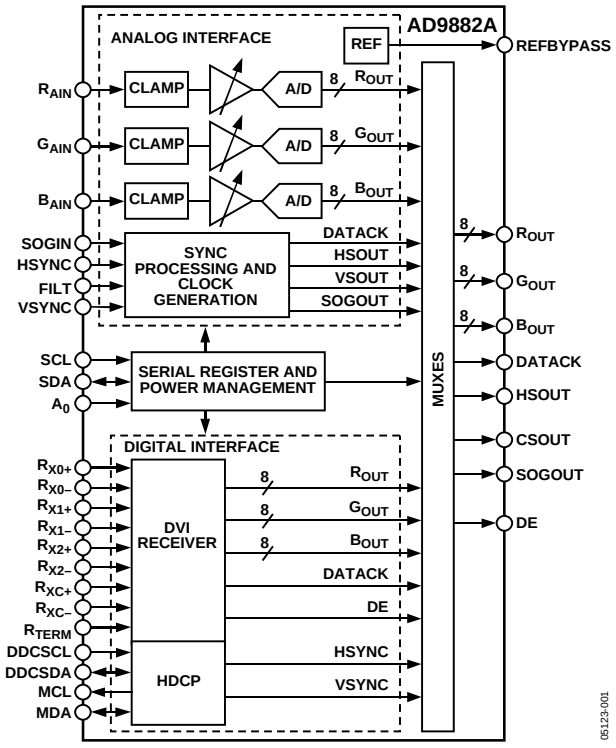

Figure 1.

The AD9882A also offers full sync processing for composite sync and sync-on-green (SOG) applications.

Digital Interface

The AD9882A contains a DVI 1.0 compatible receiver and supports display resolutions up to SXGA (1280 × 1024 at 60 Hz). The receiver features an intrapair skew tolerance of up to one full clock cycle.

With the inclusion of HDCP, displays can now receive encrypted video content. The AD9882A allows for authentication of a video receiver, decryption of encoded data at the receiver, and renewability of that authentication during transmission, as specified by the HDCP v1.0 protocol. It also has high tolerance of noncompliant HDCP sources.

Fabricated in an advanced CMOS process, the AD9882A is provided in a space-saving, 100-lead LQFP surface-mount plastic package and is specified over the 0°C to 70°C temperature range. It is available in a Pb-free package.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

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REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

V_D = 3.3 V, V_{DD} = 3.3 V, ADC clock = maximum conversion rate, unless otherwise noted.

Table 1. Analog Interface Electrical Characteristics

			AD9882AKSTZ-100			AD9882AKSTZ-140			
Parameter	**Temp**	**Test Level**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION				8			8		Bits
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.5	+1.25/–1.0		±0.5	+1.35/–1.0	LSB
	Full	VI			+1.35/–1.0			+1.45/–1.0	LSB
Integral Nonlinearity	25°C	I		±0.5	±1.85		±0.5	±2.0	LSB
	Full	VI			±2.0			±2.3	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		100			100		ppm/°C
Input Bias Current	Full	IV			1			1	µA
Input Full-Scale Matching	Full	VI		1.5	8.0		1.5	8.0	% FS
Offset Adjustment Range	Full	VI	45	49	56	45	49	56	% FS
REFERENCE OUTPUT									
Output Voltage	Full	VI		1.25			1.25		V
Temperature Coefficient	Full	V		±50			±50		ppm/°C
SWITCHING PERFORMANCE[1]									
Maximum Conversion Rate	Full	VI	100			140			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Clock to Data Skew, t_{SKEW}	Full	IV	–0.5		+2.0	–0.5		+2.0	ns
Serial Port Timing									
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	250			250			ns
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
Hsync Input Frequency	Full	IV	15		110	15		110	kHz
Maximum PLL Clock Rate	Full	VI	100			140			MHz
Minimum PLL Clock Rate	Full	IV			12			12	MHz
PLL Jitter	25°C	IV		500	700[2]		500	700	ps p-p
	Full	IV			1000			1000	ps p-p
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	2.6			2.6			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	IV			–1.0			–1.0	µA
Input Current, Low (I_{IL})	Full	IV			1.0			1.0	µA
Input Capacitance	25°C	V		3			3		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	IV	V_{DD} – 0.1			V_{DD} – 0.1			V
Output Voltage, Low (V_{OL})	Full	IV			0.4			0.4	V
Duty Cycle, DATACK	Full	IV	45	50	55	45	50	55	%

Parameter	Temp	Test Level	AD9882AKSTZ-100 Min	Typ	Max	AD9882AKSTZ-140 Min	Typ	Max	Unit
Output Coding				Binary			Binary		
POWER SUPPLY									
V_D Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	V
V_{DD} Supply Voltage	Full	IV	2.2	3.3	3.45	2.2	3.3	3.45	V
P_{VD} Supply Voltage	Full	IV	3.15	3.3	3.45	3.15	3.3	3.45	V
I_D Supply Current (V_D)	25°C	V		162			181		mA
I_{DD} Supply Current (V_{DD})[3]	25°C	V		47			63		mA
IPV_D Supply Current (PV_D)	25°C	V		19			21		mA
Total Supply Current	Full	VI		228	237		265	274	mA
Power-Down Supply Current	Full	VI		30	35		30	35	mA
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Signal-to-Noise Ratio (SNR) f_{IN} = 2.3 MHz	25°C	V		44			43		dB
Crosstalk	Full	V		55			55		dBc
THERMAL CHARACTERISTICS									
θ_{JA} Junction-to-Ambient[4]		V		43			43		°C/W

[1] Drive strength = 11.
[2] VCO range = 10, Charge pump current = 110, PLL divider = 1693.
[3] DATACK Load = 15 pF, Data load = 5 pF.
[4] Simulated typical performance with package mounted to a 4-layer board.

VD = 3.3 V, VDD = 3.3 V, clock = maximum, unless otherwise noted.

Table 2. Digital Interface Electrical Characteristics

Parameter	Conditions	Temp	Test Level	AD9882AKSTZ Min	Typ	Max	Unit
RESOLUTION					8		Bits
DC DIGITAL I/O Specifications							
High Level Input Voltage (V_{IH})		Full	VI	2.6			V
Low Level Input Voltage (V_{IL})		Full	VI			0.8	V
High Level Output Voltage (V_{OH})		Full	IV	2.4			V
Low Level Output Voltage (V_{OL})		Full	IV			0.4	V
Output Leakage Current (I_{OL})	High impedance	Full	IV	−10		+10	µA
DC SPECIFICATIONS							
Output High Drive	Output drive = high	Full	V		11		mA
(I_{OHD})(V_{OUT} = V_{OH})	Output drive = medium	Full	V		8		mA
	Output drive = low	Full	V		5		mA
Output Low Drive	Output drive = high	Full	V		−7		mA
(I_{OLD})(V_{OUT} = V_{OL})	Output drive = medium	Full	V		−6		mA
	Output drive = low	Full	V		−5		mA
DATACK High Drive	Output drive = high	Full	V		28		mA
(V_{OHC})(V_{OUT} = V_{OH})	Output drive = medium	Full	V		14		mA
	Output drive = low	Full	V		7		mA
DATACK Low Drive	Output drive = high	Full	V		−15		mA
(V_{OLC})(V_{OUT} = V_{OL})	Output drive = medium	Full	V		−9		mA
	Output drive = low	Full	V		−7		mA
Differential Input Voltage							
Single-Ended Amplitude		Full	IV	75		800	mV

Parameter	Conditions	Temp	Test Level	AD9882AKSTZ Min	Typ	Max	Unit
POWER SUPPLY							
V_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
V_{DD} Supply Voltage		Full	IV	2.2	3.3	3.45	V
PV_D Supply Voltage		Full	IV	3.15	3.3	3.45	V
I_D Supply Current (Typical Pattern)[1]		25°C	V		237		mA
I_{DD} Supply Current (Typical Pattern)[1, 2]		25°C	V		25		mA
IPV_D Supply Current (Typical Pattern)[1]		25°C	V		57		mA
Total Supply Current with HDCP (Typical Pattern)[1, 2]		Full	IV		340	367	mA
I_D Supply Current (Worst-Case Pattern)[3]		25°C	V		247		mA
I_{DD} Supply Current (Worst-Case Pattern)[2, 3]		25°C	V		61		mA
IPV_D Supply Current (Worst-Case Pattern)[3]		25°C	V		57		mA
Total Supply Current with HDCP (Worst-Case Pattern)[2, 3]		Full	IV		385	420	mA
Power-Down Supply Current (I_{PD})		Full	VI		30	35	mA
AC SPECIFICATIONS							
Intrapair (+ to –) Differential Input Skew (T_{DPS})		Full	IV			360	ps
Channel-to-Channel Differential Input Skew (T_{CCS})		Full	IV			1	Clock Period
Low-to-High Transition Time for Data (D_{LHT})	Output drive = high, C_L = 10 pF	Full	IV			2.2	ns
	Output drive = medium, C_L = 7 pF	Full	IV			2.5	ns
	Output drive = low, C_L = 5 pF	Full	IV			3.2	ns
Low-to-High Transition Time for DATACK (D_{LHT})	Output drive = high, C_L = 10 pF	Full	IV			1.0	ns
	Output drive = medium, C_L = 7 pF	Full	IV			1.6	ns
	Output drive = low, C_L = 5 pF	Full	IV			2.1	ns
High-to-Low Transition Time for Data (D_{HLT})	Output drive = high, C_L = 10 pF	Full	IV			2.2	ns
	Output drive = medium, C_L = 7 pF	Full	IV			1.9	ns
	Output drive = low, C_L = 5 pF	Full	IV			1.7	ns
High-to-Low Transition Time for DATACK (D_{HLT})	Output drive = high, C_L = 10 pF	Full	IV			1.0	ns
	Output drive = medium, C_L = 7 pF	Full	IV			1.0	ns
	Output drive = low, C_L = 5 pF	Full	IV			1.4	ns
Clock -to- Data Skew,[4] t_{SKEW}		Full	IV	–0.5		+2.0	ns
Duty Cycle, DATACK		Full	IV	40	46	50	%
DATACK Frequency (F_{CIP})		Full	VI	25		112	MHz

[1] The typical pattern contains a gray scale area. Output drive = high.
[2] DATACK load = 10 pF, data load = 10 pF.
[3] The worst-case pattern contains a black and white checkerboard pattern. Output drive = high.
[4] Drive strength = 11.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_D	3.6 V
V_{DD}	3.6 V
Analog Inputs	V_D to 0.0 V
V_{REF}	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature	–25°C to +85°C
Storage Temperature	–65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

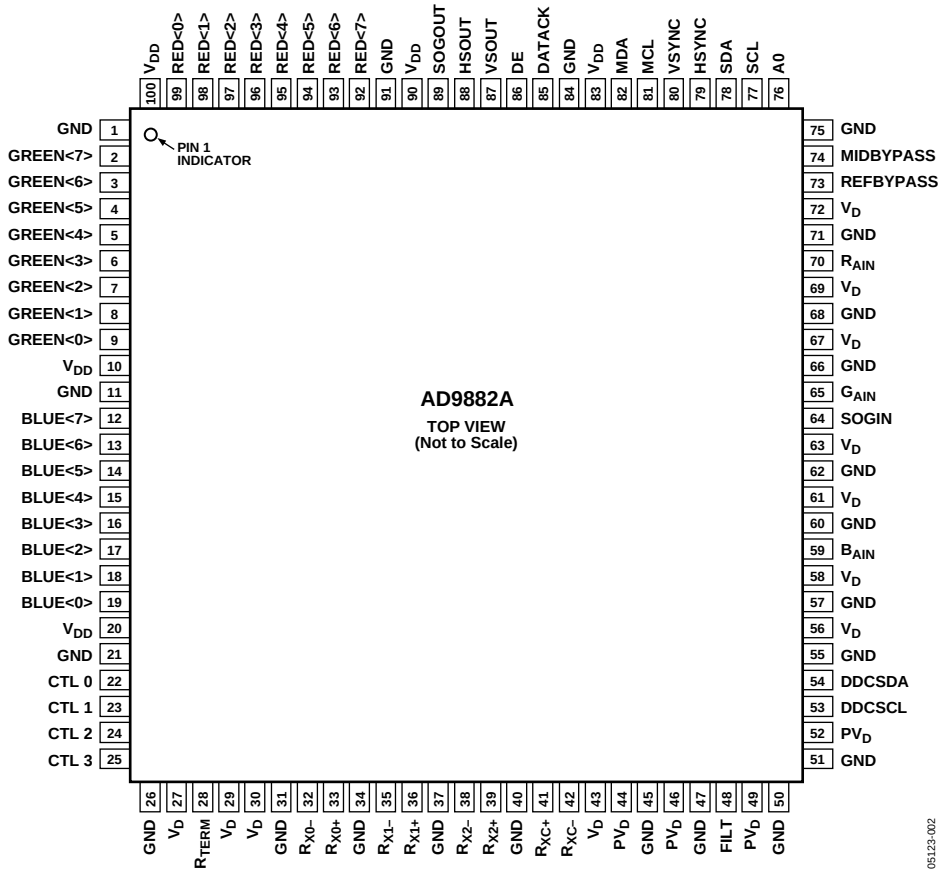

Figure 2. 100-Lead LQFP Pin Configuration

Table 4. Pin Function Descriptions

Pin Type	Mnemonic	Function	Value	Pin Number	Interface
Analog Video Inputs	R_{AIN}	Analog Input for Converter R	0.0 V to 1.0 V	70	Analog
	G_{AIN}	Analog Input for Converter G	0.0 V to 1.0 V	65	Analog
	B_{AIN}	Analog Input for Converter B	0.0 V to 1.0 V	59	Analog
External Sync/Clock	HSYNC	Horizontal Sync Input	3.3 V CMOS	79	Analog
	VSYNC	Vertical Sync Input	3.3 V CMOS	80	Analog
	SOGIN	Input for Sync-on-Green	0.0 V to 1.0 V	64	Analog
Sync Outputs	HSOUT	HSYNC Output Clock (Phase-Aligned with DATACK)	3.3 V CMOS	88	Both
	VSOUT	VSYNC Output Clock	3.3 V CMOS	87	Both
	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS	89	Analog
References	REFBYPASS	Internal Reference Bypass	1.25 V	73	Analog
	MIDBYPASS	Internal Midscale Voltage Bypass		74	Analog
PLL Filter	FILT	Connection for External Filter Components for Internal PLL		48	Analog
Power Supply	V_D	Analog Power Supply	3.15 V to 3.45 V		Both
	V_{DD}	Output Power Supply	2.2 V to 3.6 V		Both
	PV_D	PLL Power Supply	3.15 V to 3.45 V		Both
	GND	Ground	0 V		Both
Serial Port Control	SDA	Serial Port Data I/O	3.3 V CMOS	78	Both
	SCL	Serial Port Data Clock (100 kHz Maximum)	3.3 V CMOS	77	Both
	A0	Serial Port Address Input	3.3 V CMOS	76	Both

Pin Type	Mnemonic	Function	Value	Pin Number	Interface
Data Outputs	RED [7:0]	Outputs of Converter Red, Bit 7 is the MSB	3.3 V CMOS	92–99	Both
	GREEN [7:0]	Outputs of Converter Green, Bit 7 is the MSB	3.3 V CMOS	2–9	Both
	BLUE [7:0]	Outputs of Converter Bue, Bit 7 is the MSB	3.3 V CMOS	12–19	Both
Data Clock Output	DATACK	Data Output Clock for the Analog and Digital Interface	3.3 V CMOS	85	Both
Digital Video Data Inputs	R_{X0+}	Digital Input Channel 0 True		33	Digital
	R_{X0-}	Digital Input Channel 0 Complement		32	Digital
	R_{X1+}	Digital Input Channel 1 True		36	Digital
	R_{X1-}	Digital Input Channel 1 Complement		35	Digital
	R_{X2+}	Digital Input Channel 2 True		39	Digital
	R_{X2-}	Digital Input Channel 2 Complement		38	Digital
Digital Video Clock Inputs	R_{XC+}	Digital Data Clock True		41	Digital
	R_{XC-}	Digital Data Clock Complement		42	Digital
Data Enable	DE	Data Enable	3.3 V CMOS	86	Digital
Control Bits	CTL [0:3]	Decoded Control Bits	3.3 V CMOS	22–25	Digital
RTERM	R_{TERM}	Sets Internal Termination Resistance		28	Digital
HDCP	DDCSCL	HDCP Slave Serial Port Data Clock	3.3 V CMOS	53	Digital
	DDCSDA	HDCP Slave Serial Port Data I/O	3.3 V CMOS	54	Digital
	MCL	HDCP Master Serial Port Data Clock	3.3 V CMOS	81	Digital
	MDA	HDCP Master Serial Port Data I/O	3.3 V CMOS	82	Digital

PIN DESCRIPTIONS OF SHARED PINS BETWEEN ANALOG AND DIGITAL INTERFACES

HSOUT—Horizontal Sync Output

A reconstructed and phase-aligned version of the video Hsync. The polarity of this output can be controlled via a serial bus bit. In analog interface mode, the placement and duration are variable. In digital interface mode, the placement and duration are set by the graphics transmitter.

VSOUT—Vertical Sync Output

The separated Vsync from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes is set by the graphics transmitter.

SERIAL PORT (2-WIRE)

SDA—Serial Port Data I/O

SCL—Serial Port Data Clock

A0—Serial Port Address Input

For a full description of the 2-wire serial register, refer to the 2-Wire Serial Control Register Detail section.

DATA OUTPUTS

RED—Data Output, Red Channel

GREEN—Data Output, Green Channel

BLUE—Data Output, Blue Channel

The main data outputs. Bit 7 is the MSB. These outputs are shared between the two interfaces and behave in accordance with the active interface. Refer to the Analog Interface and Digital Interface sections.

DATACK—Data Output Clock

Just like the data outputs, the data clock output is shared between the two interfaces. It behaves differently depending on which interface is active. Refer to the **DATACK—Data Output Clock** section to determine how this pin behaves. .

Table 5. Analog Interface Pin List

Pin Type	Mnemonic	Function	Value	Pin Number
Analog Video Inputs	R_{AIN}	Analog input for Converter R	0.0 V to 1.0 V	70
	G_{AIN}	Analog input for Converter G	0.0 V to 1.0 V	65
	B_{AIN}	Analog input for Converter B	0.0 V to 1.0 V	59
External Sync/Clock	HSYNC	Horizontal SYNC input	3.3 V CMOS	79
	VSYNC	Vertical SYNC input	3.3 V CMOS	80
	SOGIN	Sync-on-green input	0.0 V to 1.0 V	64
Sync Outputs	HSOUT	Hsync output (phase-aligned with DATACK)	3.3 V CMOS	88
	VSOUT	Vsync output	3.3 V CMOS	87
	SOGOUT	Composite SYNC	3.3 V CMOS	89
Voltage Reference Clamp Voltages	REFBYPASS	Internal reference bypass	1.25 V	73
	MIDBYPASS	Internal midscale voltage bypass		74
PLL Filter	FILT	Connection for external filter components for internal PLL		48
Power Supply	V_D	Main power supply	3.15 V to 3.45 V	
	PV_D	PLL power supply (nominally 3.3 V)	3.15 V to 3.45 V	
	V_{DD}	Output power supply	2.2 V to 3.6 V	
	GND	Ground	0 V	

PIN FUNCTION DETAIL: ANALOG INTERFACE

Inputs

R_{AIN}—Analog Input for Red Channel

G_{AIN}—Analog Input for Green Channel

B_{AIN}—Analog Input for Blue Channel

High impedance inputs that accept the red, green, and blue channel graphics signals, respectively. For RGB, the three channels are identical and can be used for any colors, but colors are assigned for convenient reference.

For proper 4:2:2 formatting in a YPbPr application, the Y must be connected to the G_{AIN} input, the Pb must be connected to the B_{AIN} input, and the Pr must be connected to the R_{AIN} input.

They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation.

Hsync—Horizontal Sync Input

This input receives a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of this pin is controlled by Serial Register Bit 0x10, Bit 6 (Hsync polarity). Only the leading edge of Hsync is used by the PLL; the trailing edge is used for clamp timing. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync polarity = 1, the rising edge is active.

The input includes a Schmitt trigger for noise immunity, with a nominal input threshold of 1.5 V.

Electrostatic discharge (ESD) protection diodes conduct heavily if this pin is driven more than 0.5 V above the maximum tolerance voltage (3.3 V) or more than 0.5 V below ground.

VSYNC—Vertical Sync Input

This is the input for vertical sync.

SOGIN—Sync-on-Green Input

This input is provided to assist with processing signals with embedded sync, typically on the green channel. The pin is connected to a high speed comparator with an internally generated threshold, which is set by the value of Register 0x0F, Bits 7 to 3.

When connected to an ac-coupled graphics signal with embedded sync, it produces a noninverting digital output on SOGOUT.

When not used, this input should be left unconnected. For more details on this function and how it should be configured, refer to the Sync-on-Green (SOG) section.

SOGOUT—Sync-on-Green Slicer Output

This pin can be programmed to produce either the output from the sync-on-green slicer comparator or an unprocessed but delayed version of the Hsync input. See Figure 20, the sync processing block diagram, to view how this pin is connected. Note that the output from this pin is the composite sync without additional processing from the AD9882A.

FILT—External Filter Connection

For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter as shown in Figure 8 to this pin. For optimal performance, minimize noise and parasitics on this node.

REFBYPASS—Internal Reference Bypass

Bypass for the internal 1.25 V band gap reference. It should be connected to ground through a 0.1 µF capacitor.

The absolute accuracy of this reference is ±4%, and the temperature coefficient is ±50 ppm, which is adequate for most AD9882A applications. If higher accuracy is required, an external reference can be employed instead.

MIDBYPASS—Midscale Voltage Reference Bypass

Bypass for the internal midscale voltage reference. It should be connected to ground through a 0.1 µF capacitor. The exact voltage varies with the gain setting of the red channel.

HSOUT—Horizontal Sync Output

A reconstructed and phase-aligned version of the Hsync input. The duration of Hsync can be programmed only on the analog interface, not the digital.

DATACK—Data Output Clock

The data clock output signal is used to clock the output data and HSOUT into external logic. It is produced by the internal clock generator and is synchronous with the internal pixel sampling clock.

When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The data bits, DATACK, and HSOUT outputs are all moved, so the timing relationship among the signals is maintained.

VSOUT—Vertical Sync Output

The separated Vsync from a composite signal or a direct pass-through of the Vsync input. The polarity of this output can be controlled via Register 0x10, Bit 2. The placement and duration in all modes is set by the graphics transmitter.

RED—Data Output, Red Channel

GREEN—Data Output, Green Channel

BLUE—Data Output, Blue Channel

These are the main data outputs. Bit 7 is the MSB.

The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved, so the timing relationship among the signals is maintained. See the Timing Diagrams section for more information.

POWER SUPPLY

V_D—Main Power Supply

These pins supply power to the main elements of the circuit. They should be as quiet as possible.

V_{DD}—Digital Output Power Supply

A large number of output pins (up to 25) switching at high speed (up to 140 MHz) generates a lot of power supply transients. These supply pins are identified separately from the V_D pins, so special care must be taken to minimize output noise transferred into the sensitive analog circuitry.

If the AD9882A is interfacing with lower voltage logic, V_{DD} can be connected to a lower supply voltage (as low as 2.2 V) for compatibility.

PV_D—Clock Generator Power Supply

The most sensitive portion of the AD9882A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide noise-free power to these pins.

GND—Ground

The ground return for all circuitry on-chip. It is recommended that the AD9882A be assembled on a single solid ground plane, with careful attention to ground current paths.

Table 6. Interface Selection Controls

AIO (0xF Bit 2)	Analog Interface Detect	Digital Interface Detect	AIS (0x0F, Bit 1)	Active Interface	Description
1	X	X	0	Analog	Force the analog interface active.
			1	Digital	Force the digital interface active.
0	0	X	None	Neither interface was detected.	Both interfaces are powered down.
	0	1	X	Digital	The digital interface was detected. Power down the analog interface.
	1	0	X	Analog	The analog interface was detected. Power down the digital interface.
	1	1	0	Analog	Both interfaces were detected. The analog interface gets priority.
			1	Digital	Both interfaces were detected. The digital interface gets priority.

Table 7. Power-Down Modes, 4:2:2 and 4:4:4 Format Descriptions

Mode	Power-Down[1]	Analog Interface Detect[2]	Digital Interface Detect[3]	Active Interface Override	Active Interface Select	4:2:2 Formatting	Data Sheet Signals Powered On
Soft Power-Down (Seek Mode)	1	0	0	0	X	X	Serial bus, digital interface clock detect, analog interface clock detect, SOG
Digital Interface On	1	0	1	0	X	X	Serial bus; digital interface and analog interface activity detect; SOG, band gap reference; red, green, and blue outputs
Analog Interface On 4:4:4 Format	1	1	0	0	X	0	Serial bus; analog interface and digital interface clock detect; SOG, band gap reference; red, green, and blue outputs
Analog Interface On 4:2:2 Format	1	1	0	0	X	1	Serial bus; analog interface and digital interface clock detect; SOG, band gap reference; red and green outputs only
Serial Bus Arbitrated Interface	1	1	1	1	0	0	Same as the analog interface in 4:4:4 mode
Serial Bus Arbitrated Interface	1	1	1	1	0	1	Same as the analog interface in 4:2:2 mode
Serial Bus Arbitrated Interface	1	1	1	1	1	X	Same as digital interface mode
Override to Analog Interface	1	1	X	1	0	0	Same as the analog interface 4:4:4 mode
Override to Analog Interface	1	1	X	1	0	1	Same as the analog interface 4:2:2 mode
Override to Digital Interface	1	X	1	1	1	X	Same as digital interface mode
Absolute Power-Down	0	X	X	X	X	X	Serial bus

[1] Power-down is controlled via Bit 1 in Serial Bus Register 0x14.
[2] Analog interface detect is determined by OR'ing Bits 7, 6, and 5 in Serial Bus Register 0x15.
[3] Digital interface detect is determined by Bit 4 in Serial Bus Register 0x15.

THEORY OF OPERATION: INTERFACE DETECTION

ACTIVE INTERFACE DETECTION AND SELECTION

The AD9882A includes circuitry to detect whether an interface is active or not (see Table 6).

For detecting the analog interface, the circuitry monitors the presence of Hsync, Vsync, and sync-on-green. The result of the detection circuitry can be read from the 2-wire serial interface bus at Address 0x15, Bits 7, 5, and 6, respectively. If one of these sync signals disappears, the maximum time it takes for the circuitry to detect it is 100 ms.

For detecting the digital interface, there are two stages of detection. The first stage searches for the presence of the digital interface clock. The circuitry for detecting the digital interface clock is active even when the digital interface is powered down. The result of this detection stage can be read from the 2-wire serial interface bus at Address 0x15, Bit 4. If the clock disappears, the maximum time it takes for the circuitry to detect it is 100 ms. Once a digital interface clock is detected, the digital interface is powered up and the second stage of detection begins. During the second stage, the circuitry searches for 32 consecutive DEs. Once 32 DEs are found, the detection process is complete.

There is an override for the automatic interface selection. It is the AIO (Active Interface Override) bit, Register 0x0F, Bit 2. When the AIO bit is set to Logic 0, the automatic circuitry is used. When the AIO bit is set to Logic 1, the AIS (Active Interface Select) bit (Register 0x0F, Bit 1) is used to determine the active interface rather than the automatic circuitry.

POWER MANAGEMENT

The AD9882A is a dual interface device with shared outputs. Only one interface can be used at a time. For this reason, the chip automatically powers down the unused interface. When the analog interface is being used, most of the digital interface circuitry is powered down, and vice versa. This helps to minimize the AD9882A total power dissipation. In addition, if neither interface has activity on it, the chip powers down both interfaces. The AD9882A uses the activity detect circuits, the active interface bits in Serial Register 0x15, the active interface override bits in Register 0x0F, Bits 2 and 1, and the power-down bit in Register 0x14, Bit 1, to determine the correct power state. In a given power mode, not all circuitry in the inactive interface is powered down completely.

When the digital interface is active, the band gap reference Hsync, Vsync, and SOG detect circuitry remain powered-up. When the analog interface is active, the digital interface clock detect circuit is not powered-down. Table 7 summarizes how the AD9882A determines which power mode to be in and which circuitry is powered on/off in each of these modes. The power-down command has priority, then the active interface override, and then the automatic circuitry.

THEORY OF OPERATION AND DESIGN GUIDE: ANALOG INTERFACE

GENERAL DESCRIPTION

The AD9882A is a fully integrated solution for capturing analog RGB signals and digitizing them for display on flat panel monitors or projectors. The device is ideal for implementing a computer interface for HDTV monitors or as the front end to high performance video scan converters.

Implemented in a high performance CMOS process, the interface can capture signals with pixel rates of up to 140 MHz.

The AD9882A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface. Full integration of these sensitive analog functions makes the system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of only 875 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

INPUT SIGNAL HANDLING

The AD9882A has three high impedance analog input pins for the red, green, and blue channels. They will accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board via a DVI-I connector, a 15-pin D connector, or BNC connectors. The AD9882A should be located as close as practical to the input connector. Signals should be routed via matched-impedance traces (normally 75 Ω) to the IC input pins.

At that point, the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9882A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit (see Figure 9).

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9882A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next and digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. It has been shown that a small inductor in series with the input is effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a Fair-Rite #2508051217Z0 high speed signal chip bead inductor in the circuit of Figure 9 gives good results in most applications.

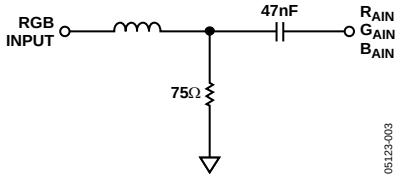

Figure 3. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The AD9882A receives a horizontal sync signal and uses it to generate the pixel clock and clamp timing. This can be either a sync signal directly from the graphics source or a preprocessed TTL or CMOS level signal.

The Hsync input includes a Schmitt trigger buffer and is capable of handling signals with long rise times, with superior noise immunity. In typical PC-based graphic systems, the sync signals are simply TTL level drivers, feeding unshielded wires in the monitor cable. As such, no termination is required.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic. If there are 5 V drivers on the bus, these pins should be protected with 150 Ω series resistors placed between the pull-up resistors and the input pins.

OUTPUT SIGNAL HANDLING

The digital outputs are designed and specified to operate from a 3.3 V power supply (V_{DD}). They can also work with a V_{DD} as low as 2.5 V for compatibility with other 2.5 V logic.

CLAMPING

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, and black is at 300 mV; white will be approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which is removed by clamping for proper capture by the AD9882A.

The key to clamping is to identify a portion (time) of the signal when the graphics system is known to be producing black. Originating from CRT displays, the electron beam is blanked by sending a black level during horizontal retrace to prevent disturbing the image. Most graphics systems maintain this format of sending a black level between active video lines.

An offset is then introduced, which results in the ADC producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In systems with embedded sync, a blacker-than-black signal (Hsync) is produced briefly to signal the CRT that it is time to begin a retrace. For obvious reasons, it is important to avoid clamping on the tip of Hsync. Fortunately, there is virtually always a period following Hsync called the back porch, in which a good black reference is provided. This is the time when clamping should be done.

The clamp timing is established by the AD9882A internal clamp timing generator. The clamp placement register (0x05) is programmed with the number of pixel times that should pass after the trailing edge of Hsync before clamping starts. A second register (clamp duration, 0x06) sets the duration of the clamp.

These are both 8-bit values, providing considerable flexibility in clamp generation. The clamp timing is referenced to the trailing edge of Hsync, because the back porch (black reference) always follows Hsync. A good starting point for establishing clamping is to set the clamp placement to 0x08 (providing eight pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x14 (giving the clamp 20 pixel periods to reestablish the black reference).

The value of the external input coupling capacitor affects the performance of the clamp. If the value is too small, there can be an amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, then it takes excessively long for the clamp to recover from a large change in incoming signal offset. The recommended value (47 nF) results in recovery from a step error of 100 mV to within one-half LSB in 30 lines, using a clamp duration of 20 pixel periods on a 75 Hz SXGA signal.

YUV Clamping

YUV signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) is at the midpoint of the U and V video. For these signals, it might be necessary to clamp to the midscale range of the ADC range (0x80) rather than the bottom of the ADC range (0x00).

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit, so that they can be clamped to either midscale or ground independently. These bits are located in Register 0x11 and are Bits 4 to 6. The midscale reference voltage that each ADC clamps to is provided on the MIDBYPASS pin (Pin 74). This pin should be bypassed to ground with a 0.1 µF capacitor (even if midscale clamping is not required).

GAIN AND OFFSET CONTROL

The AD9882A can accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The full-scale range is set in three 8-bit registers (red gain, green gain, and blue gain).

A code of 0 establishes a minimum input range of 0.5 V; a code of 255 corresponds with the maximum range of 1.0 V. Note that increasing the gain setting results in an image with less contrast.

The offset control shifts the entire input range, resulting in a change in image brightness. Three 7-bit registers (red offset, green offset, and blue offset) provide independent settings for each channel.

The offset controls provide a ±63 LSB adjustment range. This range is connected with the full-scale range, so if the input range is doubled (from 0.5 V to 1.0 V), the offset step size is also doubled (from 2 mV per step to 4 mV per step).

Figure 4 illustrates the interaction of gain and offset controls. The magnitude of an LSB in offset adjustment is proportional to the full-scale range, so changing the full-scale range also changes the offset. The change is minimal if the offset setting is near midscale. When changing the offset, the full-scale range is not affected, but the full-scale level is shifted by the same amount as the zero-scale level.

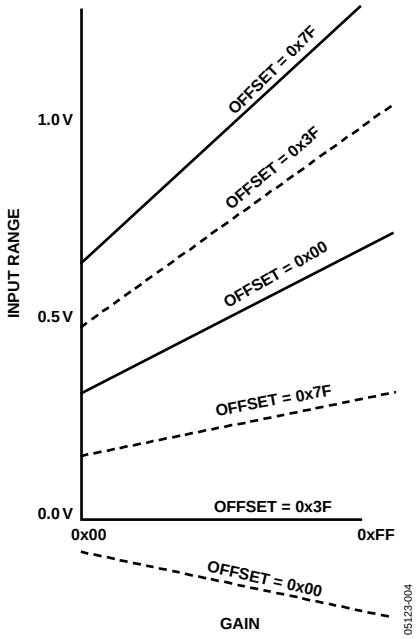

Figure 4. Gain and Offset Control

SYNC-ON-GREEN (SOG)

The sync-on-green input operates in two steps. First, it sets a baseline clamp level off of the incoming video signal with a negative peak detector. Second, it sets the sync trigger level (nominally 150 mV above the negative peak). The exact trigger level is variable and can be programmed via Register 0x0F, Bits 7 to 3. The sync-on-green input must be ac-coupled to the green analog input through its own capacitor as shown in Figure 5. The value of the capacitor must be 1 nF ±20%. If sync-on-green is not used, this connection is not required and SOGIN should be left unconnected. Note that the sync-on-green signal is always negative polarity. See the Sync Processing Engine section for further information.

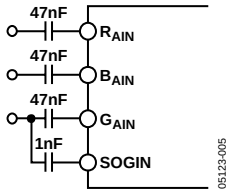

Figure 5. Typical Clamp Configuration

CLOCK GENERATION

A phase-locked loop (PLL) is employed to generate the pixel clock. The Hsync input provides a reference frequency for the PLL. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. This pixel clock is divided by the PLL divide value (Registers 0x01 and 0x02) and phase compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, there is a period during which the signal is slewing from the old pixel amplitude and settling at its new value. Then there is a time when the input voltage is stable, before the signal must slew to a new value (Figure 6). The ratio of the slewing time to the stable time is a function of the bandwidth of the graphics DAC and the bandwidth of the transmission system (cable and termination). It is also a function of the overall pixel rate. Clearly, if the dynamic characteristics of the system remain fixed, then the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter, and the stable pixel time becomes shorter as well.

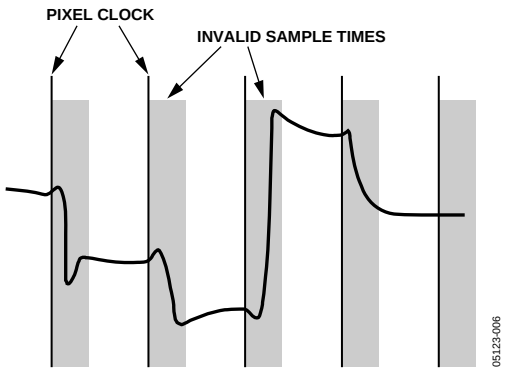

Figure 6. Pixel Sampling Times

Any jitter in the clock reduces the precision with which the sampling time can be determined and must also be subtracted from the stable pixel time.

Considerable care has been taken in the design of the AD9882A's clock generation circuit to minimize jitter. As indicated in Figure 7, the clock jitter of the AD9882A is less than 6% of the total pixel time in all operating modes, making negligible the reduction in the valid sampling time due to jitter.

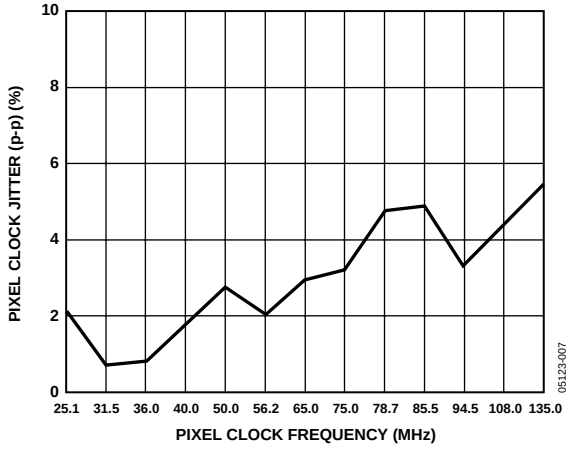

Figure 7. Pixel Clock Jitter vs. Frequency

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 8. Recommended settings of VCO range and charge pump current for VESA standard display modes are listed in Table 10.

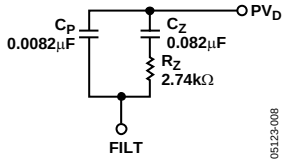

Figure 8. PLL Loop Filter Detail

Four programmable registers are provided to optimize the performance of the PLL. These registers are

1. The 12-bit divisor register (Registers 0x01 and 0x02). The input Hsync frequencies range from 15 kHz to 110 kHz. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 12 MHz to 140 MHz. The divisor register controls the exact multiplication factor. This register can be set to any value between 221 and 4095. The divide ratio that is actually used is the programmed divide ratio plus one.

2. The 2-bit VCO range register (Register 0x03, Bits 6 and 7). To improve the noise performance of the AD9882A, the VCO operating frequency range is divided into three overlapping regions. The VCO range register sets this operating range. The frequency ranges for the lowest and highest regions are shown in Table 8.

3. The 3-bit charge pump current register (Register 0x03, Bits 3 to 5). This register allows the current that drives the low-pass loop filter to be varied. The possible current values are listed in Table 9.

4. The 5-bit Phase Adjust Register (Register 0x04, Bits 3 to 7). The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin.

Table 8. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)
0	0	12–41
0	1	41–82
1	0	82–140

Table 9. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

The coast function allows the PLL to continue to run at the same frequency, in the absence of the incoming Hsync signal or during disturbances in Hsync (such as equalization pulses). This can be used during the vertical sync period, or any other time that the Hsync signal is unavailable. Also, the polarity of the Hsync signal can be set through the Hsync polarity bit (Register 0x10, Bit 6). If not using automatic polarity detection, the Hsync polarity bit should be set to match the polarity of the Hsync input signal.

Table 10. Recommended VCO Range and Charge Pump Current Settings for Standard Display Formats

Standard	Refresh Resolution	Horizontal Rate (Hz)	Frequency (kHz)	Pixel Rate (MHz)	VCORNGE	CURRENT
VGA	640 × 480	60	31.500	25.175	00	101
		72	37.700	31.500	00	101
		75	37.500	31.500	00	101
		85	43.300	36.000	00	110
SVGA	800 × 600	56	35.100	36.000	00	101
		60	37.900	40.000	00	110
		72	48.100	50.000	01	101
		75	46.900	49.500	01	101
		85	53.700	56.250	01	101
XGA	1024 × 768	60	48.400	65.000	01	101
		70	56.500	75.000	01	110
		75	60.000	78.750	01	110
		80	64.000	85.500	10	101
		85	68.300	94.500	10	101
SXGA	1280 × 1024	60	64.000	108.000	10	101
		75	80.000	135.000	10	110
TV Modes	480i	60	15.750	13.500	00	001
	480p	60	31.470	27.000	00	100
	720p	60	45.000	74.500	01	101
	1080i	60	33.750	74.500	01	101

TIMING: ANALOG INTERFACE

The following timing diagrams show the operation of the AD9882A. The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally.

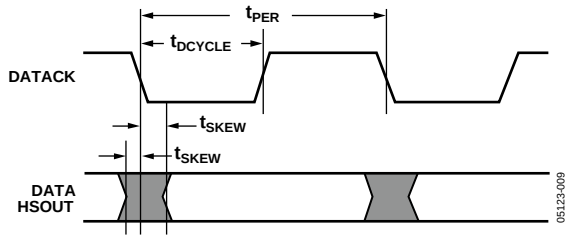

Figure 9. Output Timing

Hsync Timing

Horizontal sync (Hsync) is processed in the AD9882A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data. The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted, with respect to Hsync, through a full 360° in 32 steps via the phase adjust register (Register 0x04) to optimize the pixel sampling time. Display systems use Hsync to align memory and display write cycles, so it is important to have a stable timing relationship between Hsync output (HSOUT) and data clock (DATACK).

Three things happen to horizontal sync in the AD9882A. First, the polarity of Hsync input is determined and therefore has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x10, Bit 5). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x07. HSOUT is the sync signal that should be used to drive the rest of the display system.

Coast Timing

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the coast function is unnecessary and should be disabled using Register 0x11, Bits 1 to 3.

In some systems, however, Hsync is disturbed during the vertical sync period (Vsync). In other cases, Hsync pulses disappear. In other systems, such as those that employ composite sync (Csync) signals or embedded sync-on-green (SOG), Hsync includes equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to this new frequency and has changed frequency by the end of the Vsync period. It then takes a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The coast function is provided to eliminate this problem. It is an internally generated signal, created by the sync processing engine that disables the PLL input and allows the clock to free-run at its then-current frequency. The PLL can free-run for several lines without significant frequency drift.

TIMING DIAGRAMS

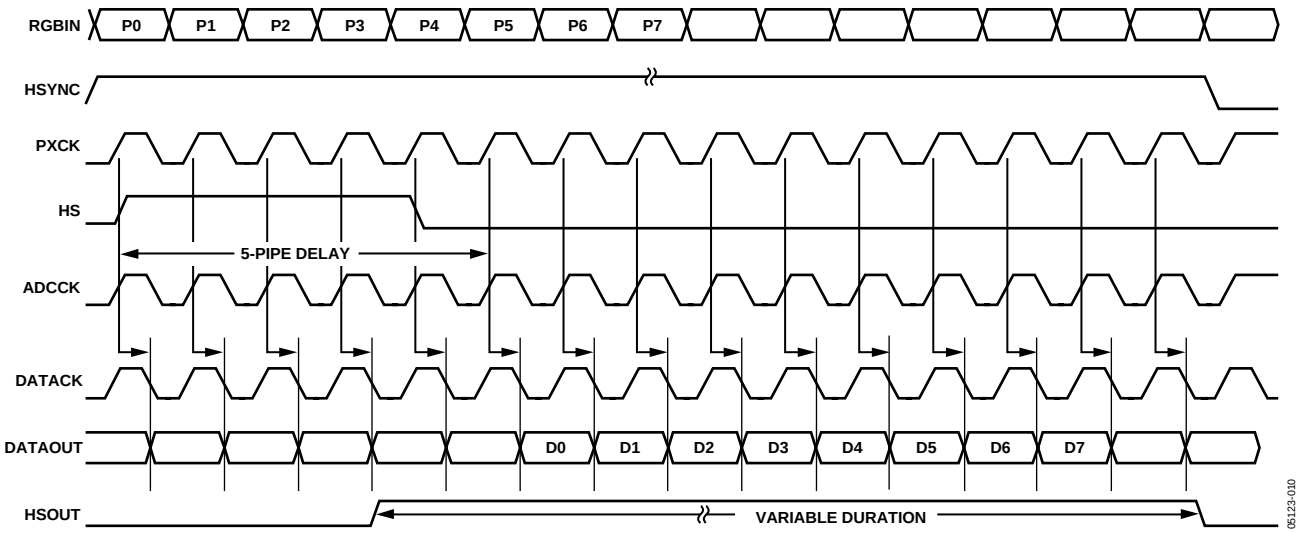

Figure 10. 4:4:4 Mode (for RGB and YPbPr)

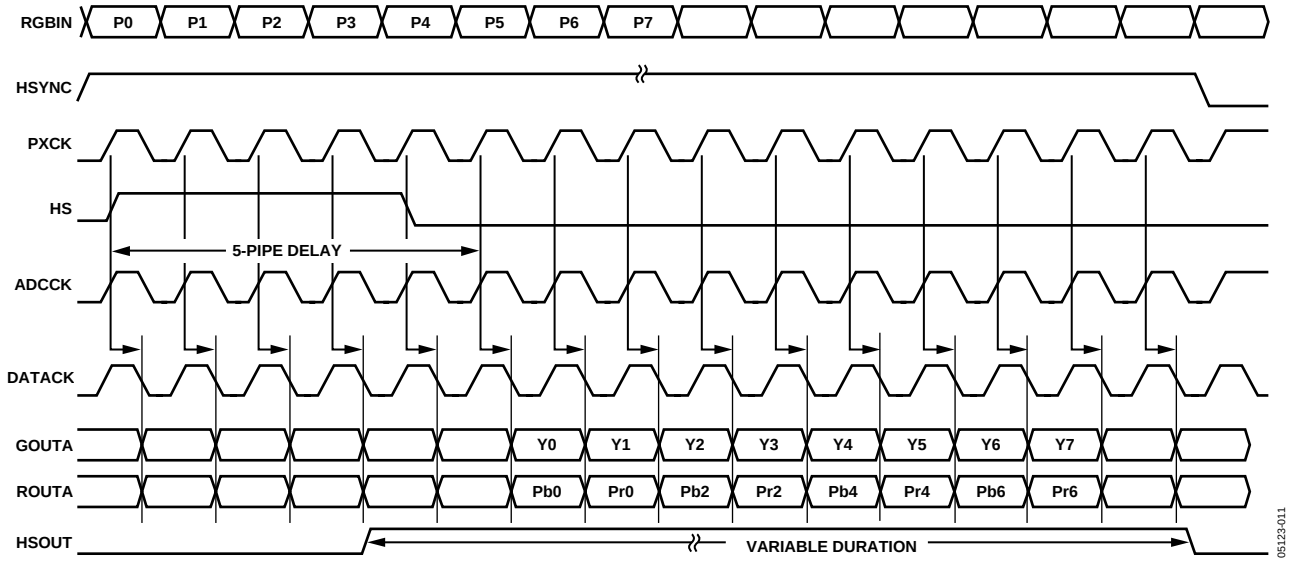

Figure 11. 4:4:2 Mode (for YPbPr Only)

THEORY OF OPERATION: DIGITAL INTERFACE

Table 11. Digital Interface Pin List

Pin Type	Mnemonic	Function	Value	Pin Number
Digital Video Data Inputs	R_{X0+}	Digital input Channel 0 true		33
	R_{X0-}	Digital input Channel 0 complement		32
	R_{X1+}	Digital input Channel 1 true		36
	R_{X1-}	Digital input Channel 1 complement		35
	R_{X2+}	Digital input Channel 2 true		39
	R_{X2-}	Digital input Channel 2 Complement		38
Digital Video Clock Inputs	R_{XC+}	Digital data clock true		41
	R_{XC-}	Digital data clock complement		42
Termination Control	R_{TERM}	Control pin for setting the internal termination resistance		28
Outputs	DE	Data enable	3.3 V CMOS	86
	HSOUT	Hsync output	3.3 V CMOS	88
	VSOUT	Vsync output	3.3 V CMOS	87
	CTL0, CTL1, CTL2, CTL3	Decoded control bit outputs	3.3 V CMOS	22–25
HDCP	DDCSCL	HDCP slave serial port data clock	3.3 V CMOS	53
	DDCSDA	HDCP slave serial port data I/O	3.3 V CMOS	54
	MCL	HDCP master serial port data clock	3.3 V CMOS	81
	MDA	HDCP master serial port data I/O	3.3 V CMOS	82
Power Supply	V_D	Main power supply	3.15 V to 3.45 V	
	PV_D	PLL power Supply	3.15 V to 3.45 V	
	V_{DD}	Output power supply	2.2 V to 3.6 V	
	GND	Ground supply	0 V	

DIGITAL INTERFACE PIN DESCRIPTIONS

Digital Data Inputs

R_{X0+} Positive Differential Input Data (Channel 0)

R_{X0-} Negative Differential Input Data (Channel 0)

R_{X1+} Positive Differential Input Data (Channel 1)

R_{X1-} Negative Differential Input Data (Channel 1)

R_{X2+} Positive Differential Input Data (Channel 2)

R_{X2-} Negative Differential Input Data (Channel 2)

These six pins receive three pairs of differential, low voltage swing input pixel data from a DVI transmitter.

Digital Clock Inputs

R_{XC+} Positive Differential Input Clock

R_{XC-} Negative Differential Input Clock

These two pins receive the differential, low voltage swing input pixel clock from a DVI transmitter.

Termination Control

R_{TERM}—Internal Termination Set Pin

This pin is used to set the termination resistance for all of the digital interface high speed inputs. To set, place a resistor of value equal to 10× the desired input termination resistance between this pin (Pin 28) and ground supply. Typically, the value of this resistor should be 500 Ω.

Outputs

DE—Data Enable Output

This pin outputs the state of data enable (DE). The AD9882A decodes DE from the incoming stream of data. The DE signal is high during active video and is low while there is no active video.

DDCSCL—HDCP Slave Serial Port Data Clock

Used for communicating with the HDCP-enabled DVI transmitter.

DDCSDA—HDCP Slave Serial Port I/O

For use in communicating with the HDCP-enabled DVI transmitter.

MCL—HDCP Master Serial Port Data Clock

Connects to the EEPROM for reading the encrypted HDCP keys.

MDA—HDCP Master Serial Port Data I/O

Connects to the EEPROM for reading the encrypted HDCP keys.

CTL—Digital Control Outputs

These pins output the control signals for the red and green channels. CTL0 and CTL1 correspond to the red channel's input, while CTL2 and CTL3 correspond to the green channel's input.

Power Supply

V_D—Main Power Supply

It should be as quiet as possible.

PV_D—PLL Power Supply

It should be as quiet as possible.

V_{DD}—Outputs Power Supply

The power for the data and clock outputs. It can run at 3.3 V or 2.5 V.

GND—Ground

The ground return for all circuitry on the device. It is recommended that the application circuit board have a single, solid ground plane.

CAPTURING THE ENCODED DATA

The first step in recovering the encoded data is to capture the raw data. To accomplish this, the AD9882A employs a high speed phase-locked loop (PLL) to generate clocks capable of over sampling the data at the correct frequency. The data capture circuitry continuously monitors the incoming data during horizontal and vertical blanking times (when DE is low) and selects the best sampling phase for each data channel independently. The phase information is stored and used until the next blanking period (one video line).

DATA FRAMES

The digital interface data is captured in groups of 10 bits each, which are called data frames. During the active data period, each frame is made up of the nine encoded video data bits and one dc-balancing bit. The data capture block receives this data serially but outputs each frame in parallel 10-bit words.

SPECIAL CHARACTERS

During periods of horizontal or vertical blanking time (when DE is low), the digital transmitter transmits special characters. The AD9882A receives these characters and uses them to set the video frame boundaries and the phase recovery loop for each channel. There are four special characters that can be received. They are used to identify the top, bottom, left side, and right side of each video frame. The data receiver can differentiate these special characters from active data because the special characters have a different number of transitions per data frame.

CHANNEL RESYNCHRONIZATION

The purpose of the channel resynchronization block is to resynchronize the three data channels to a single internal data clock. Coming into this block, all three data channels can be on different phases of the 3× oversampling PLL clock (0°, 120°, and 240°). This block can resynchronize the channels from a worst-case skew of one full input period (8.93 ns at 112 MHz).

DATA DECODER

The data decoder receives frames of data and sync signals from the data capture block (in 10-bit parallel words) and decodes them into groups of eight RGB bits, two control bits, and a data enable bit (DE).

HDCP

The AD9882A contains all the circuitry necessary for decryption of a high bandwidth digital content protection encoded DVI video stream. A typical HDCP implementation is shown in Figure 12. Several features of the AD9882A make this possible and add functionality to ease the implementation of HDCP.

The basic components of HDCP are included in the AD9882A. A slave serial bus connects to the DDC clock and DDC data pins on the DVI connector to allow the HDCP-enabled DVI transmitter to coordinate the HDCP algorithm with the AD9882A. A second serial port (MDA/MCL) allows the AD9882A to read the HDCP keys and key selection vector (KSV) stored in an external serial EEPROM. When transmitting encrypted video, the DVI transmitter enables HDCP through the DDC port. The AD9882A then decodes the DVI stream using information provided by the transmitter, HDCP keys, and KSV.

The AD9882A allows the MDA and MCL pins to be three-stated using the MDA/MCL three-state bit (Register 0x1B, Bit 7) in the configuration registers. The three-state feature allows the EEPROM to be programmed in-circuit. The MDA/MCL port must be three-stated before attempting to program the EEPROM using an external master. The keys will be stored in an $I^2C^®$ compatible 3.3 V serial EEPROM of at least 512 bytes in size. The EEPROM should have a device address of 0xA0.

Proprietary software licensed from Analog Devices encrypts the keys and creates properly formatted EEPROM images for use in a production environment. Encrypting the keys helps maintain

the confidentiality of the HDCP keys as required by the HDCP v. 1.0 specification. The AD9882A includes hardware for decrypting the keys in the external EEPROM.

ADI provides a royalty-free license for the proprietary software needed by customers to encrypt the keys between the AD9882A and the EEPROM only after customers provide evidence of a completed HDCP adopter's license agreement and sign ADI's software license agreement. The adopter's license agreement is maintained by Digital Content Protection, LLC, and can be downloaded from www.digital-cp.com. To obtain ADI's software license agreement, contact the Display Electronics Product Line directly by sending an email to flatpanel_apps@analog.com.

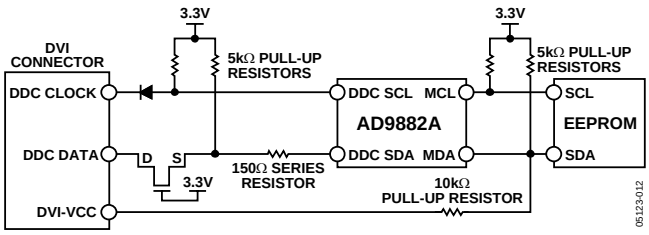

Figure 12. HDCP Implementation Using the AD9882A

GENERAL TIMING DIAGRAMS: DIGITAL INTERFACE

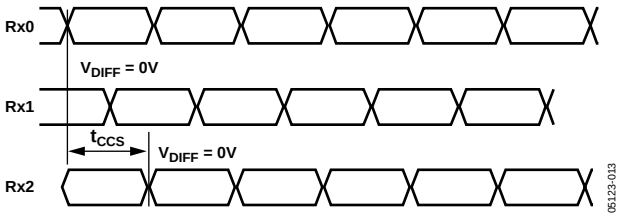

Figure 13. Digital Output Rise and Fall Times

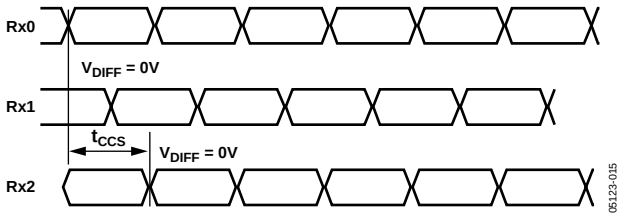

Figure 15. Channel-to-Channel Skew Timing

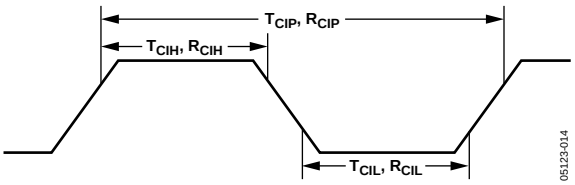

Figure 14. Clock Cycle High/Low Times

TIMING MODE DIAGRAMS: DIGITAL INTERFACE

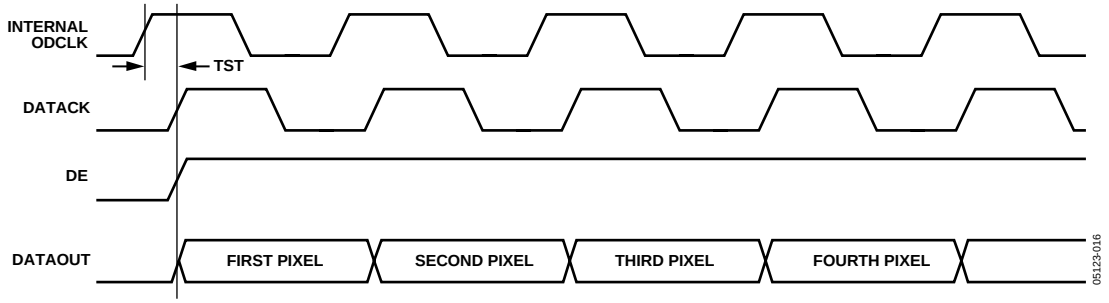

Figure 16. DVI CLK Invert = 1 (Register 14, Bit 4)

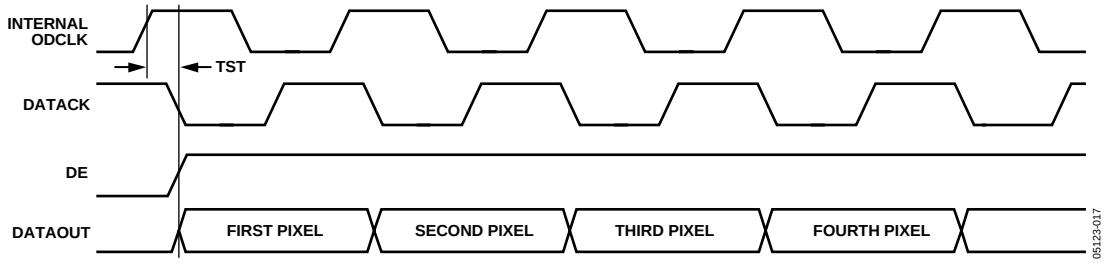

Figure 17. DVI CLK Invert = 0 (Register 14, Bit 4)

2-WIRE SERIAL REGISTER MAP

The AD9882A is initialized and controlled by a set of registers that determines the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 12. Control Register Map

Hexadecimal Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
0x00	RO	7–0		Chip Revisions	An 8-bit register that represents the silicon level.
0x01	R/W	7–0	0110 1001	PLL Div MSB	This register is for Bits [11:4] of the PLL divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first whenever a change is needed. (This will give the PLL more time to lock.)[1]
0x02	R/W	7–4	1101 ****	PLL Div LSB	Bits [3:0] LSBs of the PLL divider word. Links to PLL MSB to make a 12-bit register.[1]
0x03	R/W	7–6	01** ****	VCO Range	Selects VCO frequency range.
		5–3	**00 1***	Charge Pump	Varies the current that drives the PLL loop filter.
0x04	R/W	7–3	1000 0***	Phase Adjust	ADC clock phase adjustment. Larger values mean more delay (1 LSB = T/32).
0x05	R/W	7–0	0000 1000	Clamp Placement	Places the clamp signal an integer number of clock periods after the trailing edge of Hsync.
0x06	R/W	7–0	0001 0100	Clamp Duration	Number of clock periods that the clamp signal is actively clamping.
0x07	R/W	7–0	0010 0000	Hsync Output Pulse Width	Sets the number of pixel clocks that HSOUT will remain active.
0x08	R/W	7–0	1000 0000	Red Gain	Controls the ADC input range (contrast) of the red channel. Larger values give less contrast.
0x09	R/W	7–0	1000 0000	Green Gain	Controls the ADC input range (contrast) of the green channel. Larger values give less contrast.
0x0A	R/W	7–0	1000 0000	Blue Gain	Controls the ADC input range (contrast) of the blue channel. Larger values give less contrast.
0x0B	R/W	7–1	1000 000*	Red Offset	Controls the dc offset (brightness) of the red channel. Larger values decrease brightness.
0x0C	R/W	7–1	1000 000*	Green Offset	Controls the dc offset (brightness) of the green channel. Larger values decrease brightness.
0x0D	R/W	7–1	1000 000*	Blue Offset	Controls the dc offset (brightness) of the blue channel. Larger values decrease brightness.
0x0E	R/W	7–0	0010 0000	Sync Separator Threshold	Sets how many pixel clocks to count before toggling high or low. This should be set to some number greater than the maximum Hsync or equalization pulsewidth.
0x0F	R/W	7–3	0111 1***	Sync-on-Green Threshold	Sets the voltage level of the sync-on-green slicer's comparator.
		2	**** *0**	Active Interface Override	0 = No override. 1 = User overrides, interface set by 0x0F, Bit 1.
		1	**** **0*	Active Interface Select	0 = Analog interface active. 1 = Digital interface active. This interface is selected only if Register 0x0F, Bit 2 is set to 1, or if both interfaces are active.
0x10	R/W	7	0*** ****	Hsync Polarity Override	0 = Polarity determined by chip. 1 = Polarity set by 0x10, Bit 6.
		6	*1** ****	Input Hsync Polarity	0 = Active low polarity. 1 = Active high polarity.
		5	**0* ****	Output Hsync Polarity	0 = Active high sync signal. 1 = Active low sync signal.

Hexadecimal Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
		4	***0 ****	Active Hsync Override	0 = No override. 1 = User overrides, analog Hsync set by 0x10, Bit 3.
		3	**** 0***	Active Hsync Select	0 = Analog Hsync from the Hsync input pin. 1 = Analog Hsync from SOG. This bit is used if Register 0x10, Bit 4 is set to 1 or if both syncs are active.
		2	**** *0**	Output Vsync Polarity	0 = Invert. 1 = Not inverted.
		1	**** **0*	Active Vsync Override	0 = No override. 1 = User overrides, analog Vsync set by 0x10, Bit 0.
		0	**** ***0	Active Vsync Select	0 = Analog Vsync from the Vsync input pin. 1 = Analog Vsync from sync separator.
0x11	R/W	7	0*** ****	Clamp Function	0 = Clamping with internal clamp. 1 = Clamping disabled.
		6	*0** ****	Red Clamp Select	0 = Clamp to ground. 1 = Clamp to midscale for red channel.
		5	**0* ****	Green Clamp Select	0 = Clamp to ground. 1 = Clamp to midscale for green channel.
		4	***0 ****	Blue Clamp Select	0 = Clamp to ground. 1 = Clamp to midscale for blue channel.
		3	**** 1***	Coast Select	0 = Disabled coast. 1 = Coasting with internally generated coast signal.
		2	**** *0**	Coast Polarity Override	0 = Coast polarity determined by the chip. 1 = Coast polarity set by 0x11, Bit 1. This bit must be set to 1 to disable coast.
		1	**** **1*	Input Coast Polarity	0 = Active low coast signal. 1 = Active high coast signal. This bit must be set to 1 to disable coast.
0x12	R/W	7–0	0000 0000	Precoast	Number of Hsync periods that coast goes active prior to Vsync.
0x13	R/W	7–0	0000 0000	Postcoast	Number of Hsync periods before coast goes inactive following Vsync.
0x14	R/W	7–6	11** ****	Output Drive Select	Selects among high, medium, and low output drive strength.
		5	**1* ****	Programmable Bandwidth	0 = Low bandwidth of 10 MHz. 1 = High bandwidth of 300 MHz.
		4	***0 ****	DVI Clock Invert	0 = DVI data clock output not inverted. 1 = DVI data clock output inverted. For digital interface only.
		3	**** 0***	DVI PDO Three-State	0 = Normal outputs. 1 = High impedance outputs.
		2	**** *0**	HDCP Address	Address Bit 0 = 0 for HDCP slave port. Address Bit 1 = 1 for HDCP slave port.
		1	**** **1*	Power-Down	0 = Full chip power-down.
		0	**** ***0	Enable 4:2:2	0 = 4:4:4 mode. 1 = 4:2:2 mode.
0x15	RO	7		Analog Hsync Active	0 = Hsync not detected. 1 = Hsync detected.
		6		Analog SOG Active	0 = Sync signal not detected on green channel. 1 = Sync signal detected on green channel.
		5		Analog Vsync Active	0 = Vsync not detected. 1 = Vsync detected.
		4		DVI Active	0 = Digital interface clock not detected. 1 = Digital interface clock detected.
		3		Active Interface	0 = Analog interface active. 1 = DVI interface active.

Hexadecimal Address	Read and Write or Read Only	Bit	Default Value	Register Name	Function
0x16	RO	7		Active Hsync	0 = Hsync from the Hsync input pin. 1 = Hsync from the SOG input.
		6		Hsync Polarity Detected	0 = Active low polarity detected. 1 = Active high polarity detected.
		5		Active Vsync	0 = Vsync from the Vsync input pin. 1 = Vsync from SOG.
		4		Vsync Polarity Detected	0 = Active high polarity detected. 1 = Active low polarity detected.
		3		Coast Polarity Detected	0 = Active low polarity detected. 1 = Active high polarity detected. This function works only with internal coast.
		2		HDCP Keys Detected	0 = Not detected. 1 = Detected.
0x17	R/W	7–0	0000 0000	Test Register	Must be set to 1000 0000 for proper operation.
0x18	R/W	7–0	0000 000X	Test Register	Must be set to 1100 000x for proper operation.
0x19	R/W	7–0	0000 010X	Test Register	Must be set to 0111 110x for proper operation.
0x1A	R/W	7–0	0011 1111	Test Register	Must be set to default for proper operation.
0x1B	R/W	7	1*** ****	MDA and MCL	0 = MDA and MCL three-stated. 1 = MDA and MCL not three-stated.
		6–0	*111 0000	Test Register	Must be set to *110 0111 for proper operation.
0x1C	R/W	7–1	0000 111*	Test Register	Must be set to default for proper operation.
		0	**** ***1	RXC Connect	0 = RX clock lines disconnected. 1 = RX clock lines connected.
0x1D	RO	7–0		Test Register	Reserved for future use.
0x1E	RO	7–0		Test Register	Reserved for future use.

[1] The AD9882A updates the PLL divide ratio only when the LSBs are written to Register 0x02.

2-WIRE SERIAL CONTROL REGISTER DETAIL

CHIP IDENTIFICATION

0x00 7–0 Chip Revision

An 8-bit register that represents the silicon revision.

PLL DIVIDER CONTROL

0x01 7–0 PLL Divide Ratio MSBs

The eight most significant bits of the 12-bit PLL divide ratio PLLDIV. (The operational divide ratio is PLLDIV + 1.)

The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 221 to 4095. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications that can assist in determining the value for PLLDIV as a function of the horizontal and vertical display resolution and frame rate (see Table 10). However, many computer systems do not conform precisely to the recommendations, and these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9882A updates the full divide ratio only when the LSBs are changed. Writing to this register by itself does not trigger an update.

0x02 7–4 PLL Divide Ratio LSBs

The four least significant bits of the 12-bit PLL divide ratio PLLDIV. The operational divide ratio is PLLDIV + 1.

The power-up default value of PLLDIV is 1693 (PLLDIVM = 0x69, PLLDIVL = 0xDx).

The AD9882A updates the full divide ratio only when this register is written.

0x03 7–6 VCO Range Select

Two bits that establish the operating range of the clock generator. VCORNGE must be set to correspond with the desired operating frequency (incoming pixel rate).

The PLL VCO gives the best jitter performance while operating at high frequencies. For this reason, to output low pixel rates and still get good jitter performance, the PLL VCO actually operates at a higher frequency but then divides down the clock rate afterward. Table 13 shows the pixel rates for each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting.

Table 13. VCO Ranges

VCORNGE	Pixel Rate Range
00	12–41
01	41–82
10	82–140

The power-up default value is VCORNGE = 01.

0x03 5–3 CURRENT Charge Pump Current

Three bits that establish the current driving the loop filter in the clock generator.

Table 14. Charge Pump Currents

Charge Pump	Current (µA)
000	50
001	100
010	150
011	250
100	350
101	500
110	750
111	1500

Charge pump must be set to correspond with the desired operating frequency (incoming pixel rate). See Table 10 for the charge pump current for each register setting.

The power-up default value for current is 001.

0x04 7–3 Phase Adjust

A 5-bit value that adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase.

The power-up default phase adjust value is 0x10.

CLAMP TIMING

0x05 7–0 Clamp Placement

An 8-bit register that sets the position of the internally generated clamp.

When clamp function (Register 0x11, Bit 7) is 0, a clamp signal is generated internally at a position established by the clamp placement and for a duration set by the clamp duration. Clamping is started (clamp placement) an integral number of pixel periods after the trailing edge of Hsync. The clamp placement can be programmed to any value from 1 to 255.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image.

When clamp function is 1, this register is ignored.

0x06 7–0 Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp.

For the best results, the clamp duration should be set to include the majority of the black-reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen and a slow recovery from large changes in the average picture level (APL) or brightness.

When clamp function is 1, this register is ignored.

HSYNC OUTPUT PULSE WIDTH

0x07 7–0 Hsync Output Pulse Width

An 8-bit register that sets the duration of the Hsync output pulse.

The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted PLL feedback clock. The AD9882A then counts a number of pixel clocks equal to the value in this register minus one. This triggers the trailing edge of the Hsync output, which is also phase-adjusted.

INPUT GAIN

0x08 7–0 Red Gain Red Gain

An 8-bit word that sets the gain of the red channel. The AD9882A can accommodate input signals with a full-scale range of between 0.5 V and 1.0 V p-p. Setting red gain to 255 corresponds to an input range of 1.0 V. A red gain of 0 establishes an input range of 0.5 V. Note that increasing red gain results in the picture having less contrast (the input signal uses fewer of the available converter codes). See Figure 4.

0x09 7–0 Green Gain Green Gain

An 8-bit word that sets the gain of the green channel. See red gain (0x08).

0x0A 7–0 Blue Gain Blue Gain

An 8-bit word that sets the gain of the blue channel. See Red gain (0x08).

INPUT OFFSET

0x0B 7–1 Red Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the red channel. One LSB of offset adjustment equals approximately one LSB change in the ADC offset. Therefore, the absolute magnitude of the offset adjustment scales as the gain of the channel changes. A nominal setting of 64 results in the channel nominally clamping the back porch (during the clamping interval) to Code 00. An offset setting of 127 results in the channel clamping to Code 63 of the ADC. An offset setting of 0 clamps to Code –64 (off the bottom of the range). Increasing the value of the red offset decreases the brightness of the channel.

0x0C 7–1 Green Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the green channel. See the 0x0B 7–1 red channel offset adjust.

0x0D 7–1 Blue Channel Offset Adjust

A 7-bit offset binary word that sets the dc offset of the blue channel. 0x0B 7–1 Red channel offset adjust.

0x0E 7–0 Sync Separator Threshold

This register is used to set the responsiveness of the sync separator. It sets how many internal 5 MHz clock periods the sync separator must count to before toggling high or low. It works like a low-pass filter to ignore Hsync pulses in order to extract the Vsync signal. This register should be set to some number greater than the maximum Hsync pulse width. Note that the sync separator threshold uses an internal dedicated clock with a frequency of approximately 5 MHz.

The default for this register is 0x20.

0x0F 7–3 Sync-on-Green Slicer Threshold

This register allows the comparator threshold of the sync-on-green slicer to be adjusted. This register adjusts it in steps of 10 mV, with the minimum setting equaling 10 mV and the maximum setting equaling 330 mV.

The default setting is 15 decimal and corresponds to a threshold value of 170 mV.

0x0F 2 AIO Active Interface Override

This bit is used to override the automatic interface selection (Bit 3 in Register 0x15). To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 1 in this register.

Table 15. Active Interface Override Settings

AIO	Result
0	Autodetermines the active interface.
1	Override; Bit 1 determines the active interface.

The default for this register is 0.

0x0F 1 AIS Active Interface Select

This bit is used under two conditions. It is used to select the active interface when the override bit is set (Register 0x0F, Bit 2). Alternatively, it is used to determine the active interface when not overriding but both interfaces are detected.

Table 16. Active Interface Select Settings

AIS	Result
0	Analog interface
1	Digital interface

The default for this register is 0.

0x10 7 Hsync Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the Hsync signal going into the PLL.

Table 17. Hsync Input Polarity Override Settings

Override Bit	Result
0	Hsync polarity determined by chip.
1	Hsync polarity determined by Register 0x10, Bit 6.

The default for Hsync polarity override is 0. (Polarity determined by chip.)

0x10 6 HSPOL Hsync Input Polarity

A bit that must be set to indicate the polarity of the Hsync signal that is applied to the PLL Hsync input.

Table 18. Hsync Input Polarity Settings

HSPOL	Function
0	Active low
1	Active high

Active low means the leading edge of the Hsync pulse is negative-going. All PLL timing is based on the leading edge of Hsync, which is the falling edge. The rising edge is used to time the internal clamping.

Active high means the leading edge of the Hsync pulse is positive-going. This means that PLL timing is based on the leading edge of Hsync, which is now the rising edge.

The device operates if this bit is set incorrectly, but the internally generated clamp position, as established by clamp placement (Register 0x05), is not placed as expected, which might generate clamping errors.

The power-up default value for HSPOL is 1.

0x10 5 Hsync Output Polarity

This bit determines the polarity of the Hsync output and the SOG output. Table 19 shows the effect of this option. Sync indicates the logic state of the sync pulse.

Table 19. Hsync Output Polarity Settings

Setting	SYNC
0	Logic 1 (positive polarity)
1	Logic 0 (negative polarity)

The default setting for this register is 0.

0x10 4 Active Hsync Override

This bit is used to override the automatic Hsync selection. To override, set this bit to Logic 1. When overriding, the active Hsync is set via Bit 3 in this register.

Table 20. Active Hsync Override Settings

Override	Result
0	Autodetermines the active Hsync.
1	Override; Bit 3 determines the active Hsync.

The default for this register is 0.

0x10 3 Active Hsync Select

This bit is used under two conditions. It is used to select the active Hsync when the override bit is set (Bit 4). Alternatively, it is used to determine the active Hsync when not overriding, but both Hsyncs are detected.

Table 21. Active Hsync Select Settings

Select	Result
0	Hsync input
1	Sync-on-green input

The default for this register is 0.

0x10 2 Vsync Output Polarity

This bit determines the polarity of the Vsync output. Table 22 shows the effect of this option. SYNC indicates the logic state of the sync pulse.

Table 22. Vsync Output Polarity Settings

Setting	SYNC
1	Not inverted
0	Inverted

The default setting for this register is 0.

0x10 1 Active Vsync Override

This bit is used to override the automatic Vsync selection. To override, set this bit to Logic 1. When overriding, the active interface is set via Bit 0 in this register.

Table 23. Active Vsync Override Settings

Override	Result
0	Autodetermines the active Vsync
1	Override; Bit 0 determines the active Vsync.

The default for this register is 0.

0x10 0 Active Vsync Select

This bit is used to select the active Vsync when the override bit is set (Bit 1).

Table 24. Active Vsync Select Settings

Select	Result
0	Vsync input
1	Sync separator output

The default for this register is 0.

0x11 7 Clamp Function

This bit enables/disables clamping.

Table 25. Clamp Input Signal Source Settings

Clamp Function	Function
0	Internally generated clamp enabled
1	Clamping disabled

0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the trailing edge of Hsync.

1 disables clamping. The three channels are clamped when the clamp signal is active.

Power-up default value for clamp function is 0.

0x11 6 Red Clamp Select

A bit that determines whether the red channel is clamped to ground or to midscale. For RGB video, all three channels are referenced to ground. For YPbPr, the Y channel is referenced to ground, but the PbPr channels are referenced to midscale.

Clamping to midscale clamps to Pin 74.

Table 26. Red Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

0x11 5 Green Clamp Select

This bit determines whether the green channel is clamped to ground or to midscale.

Table 27. Green Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

0x11 4 Blue Clamp Select

This bit determines whether the blue channel is clamped to ground or to midscale.

Table 28. Blue Clamp Select Settings

Clamp	Function
0	Clamp to ground
1	Clamp to midscale (Pin 74)

The default setting for this register is 0.

0x11 3 Coast Select

This bit is used to enable or disable the coast signal. If coast is enabled, the additional decision of using the Vsync input pin or the output from the sync separator needs to be made (Register 0x10, Bits 1, 0). To disable coast, the user must set Register 0x11, Bit 2 to 1 and Register 0x11, Bit 1 to 1.

Table 29. Coast Enable Settings

Select	Result
0	Coast disabled
1	Internally generated coast signal

The default for this register is 1.

0x11 2 Coast Input Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL. When disabling coast, Register 11, Bit 2 must be set to 1 and Register 0x11, Bit 1 must be set to 1. This register works only when coast is disabled. It does not work with internal coast.

Table 30. Coast Input Polarity Override Settings

Override Bit	Result
0	Coast polarity determined by chip
1	Coast polarity determined by user

The default for coast polarity override is 0.

0x11 1 Coast Input Polarity

This bit indicates the polarity of the coast signal that is applied to the PLL coast input.

This register can be used only when coast is disabled and Register 0x11, Bit 2 is set to 1.

Table 31. Coast Input Polarity Settings

CSTPOL	Function
0	Active low
1	Active high

The power-up default value is CSTPOL = 1.

0x12 7–0 Precoast

This register allows the coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. This register defines the number of edges that are filtered before Vsync on a composite sync.

The default is 0.

0x13 7–0 Postcoast

This register allows the coast signal to be applied following the Vsync signal. This is necessary in cases where postequalization pulses are present. The step size for this control is one Hsync period. This register defines the number of edges that are filtered after Vsync on a composite sync.

The default is 0.

0x14 7–6 Output Drive

These two bits select the drive strength for the high speed digital outputs (all data output and clock output pins). Higher drive strength results in faster rise/fall times, and in general makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps reduce EMI and digitally generated power supply noise.

Table 32. Output Drive Strength Settings

Bit 7	Bit 6	Result
1	X	High drive strength
0	1	Medium drive strength
0	0	Low drive strength

The default for this register is 11, high drive strength. This option works on both the analog and digital interfaces.

0x14 5 Programmable Analog Bandwidth

These bits select the analog bandwidth.

Table 33. Analog Bandwidth Control

Bit 5	Analog Bandwidth
0	10 MHz
1	300 MHz

0x14 4 Clk Inv Data Output Clock Invert

A control bit for the inversion of the output data clock (Pin 85). This function works only for the digital interface. When not inverted, data is output on the falling edge of the data clock. See the Timing Diagrams sections, Figure 14 and Figure 15, to see how this affects timing.

Table 34. Clock Output Invert Settings

Clk Inv	Function
0	Not inverted
1	Inverted

The default for this register is 0 (not inverted).

0x14 3 PDO Power-Down Outputs

This bit is used to put the outputs in a high impedance mode. This applies to the 24 data output pins, HSOUT, VSOUT, and DE pins.

Table 35. Power-Down Output Settings

PDO	Function
0	Normal operation
1	Three-state

The default for this register is 0. (This option works on both the analog and digital interfaces.)

0x14 2 HDCP Address

This bit is used to set the HDCP slave port address.

Table 36. HDCP Address Settings

Address Bit	Result
0	0 for HDCP Slave Port
1	1 for HDCP Slave Port

The default for this register is 0.

0x14 1 PWRDN

This bit is used to control chip power-down. See the Power Management section for details about which blocks are actually powered down.

Table 37. Power-Down Settings

Select	Result
0	Power-down
1	Normal operation

The default for this register is 1.

0x14 0 4:2:2 Output Mode Select

This bit configures the output data in 4:2:2 mode. This mode can be used to reduce the number of data lines used from 24 to 16 for applications using YPbPr graphics signals. A timing diagram for this mode is shown in Figure 17. Recommended input and output configurations are shown in Table 39. In 4:2:2 mode, the red and blue channels can be interchanged to help satisfy board layout or timing requirements, but the green channel must be configured for Y.

Table 38. 4:2:2 Output Mode Select

Select	Output Mode
0	4:4:4
1	4:2:2

Table 39. 4:2:2 Input/Output Configuration

Channel	Input Connection	Output Format
Red	Pr	Pb/Pr
Green	Y	Y
Blue	Pr	High impedance

0x15 7 Hsync Detect

This bit is used to indicate when activity is detected on the HSYNC input pin (Pin 79). If Hsync is held high or low, activity is not detected.

Table 40. Hsync Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 20 shows where this function is implemented.

0x15 6 Sync-on-Green Detect

This bit is used to indicate when sync activity is detected on the sync-on-green input pin (Pin 64).

Table 41. Sync-on-Green Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 20 shows where this function is implemented.

Note that if no sync signal is presented on the green video input, normal video might still trigger activity.

0x15 5 Vsync Detect

This bit is used to indicate when activity is detected on the Vsync input pin (Pin 80). If Vsync is held high or low, activity is not detected.

Table 42. Vsync Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 20 shows where this function is implemented.

0x15 4 Digital Interface Clock Detect

This bit is used to indicate when activity is detected on the digital interface clock input.

Table 43. Digital Interface Clock Detection Results

Detect	Function
0	No activity detected
1	Activity detected

Figure 20 shows where this function is implemented.

0x15 3 Active Interface

This bit is used to indicate which interface should be active, analog or digital. It checks for activity on the analog interface and for activity on the digital interface, then determines which should be active according to Table 44. Specifically, analog interface detection is determined by OR'ing Bits 7, 6, and 5 in this register. Digital interface detection is determined by Bit 4 in this register. If both interfaces are detected, the user can determine which has priority via Bit 1 in Register 0x0F. The user can override this function via Bit 2 in Register 0x0F. If the override bit is set to Logic 1, then this bit will be forced to the same state as Bit 1 in Register 0x0F.

Table 44. Active Interface Results

Bits 7, 6, or 5 (Analog Detection)	Bit 4 (Digital Detection)	Override	AI
0	0	0	Soft power-down (seek mode)
0	1	0	1
1	0	0	0
1	1	0	Bit 1 in 0x0F
X	X	1	Bit 1 in 0x0F

AI = 0 means analog interface. AI = 1 means digital interface. The override bit is in Register 0x0F, Bit 2.

0x16 7 AHS Active Hsync

This bit indicates which Hsync input source is being used by the PLL (Hsync input or sync-on-green). Bits 6 and 7 in Register 0x15 determine which source is used. If both Hsync and SOG are detected, the user can determine which has priority via Bit 3 in Register 0x10. The user can override this function via Bit 4 in Register 0x10. If the override bit is set to Logic 1, then this bit will be forced to the same state as Bit 3 in Register 0x10.

Table 45. Active Hsync Results

Hsync Detect Register 0x15,Bit 7	SOG Detect Register 0x,10 Bit 4	Override Register 0x,15 Bit 6	AHS Register 0x16,Bit 7
0	0	0	Bit 3 in 0x10
0	1	0	1
1	0	0	0
1	1	0	Bit 3 in 0x10
X	X	1	Bit 3 in 0x10

AHS = 0 means use the Hsync pin input for Hsync. AHS = 1 means use the SOG pin input for Hsync. The override bit is in Register 0x10, Bit 4.

0x16 6 Detected Hsync Input Polarity Status

This bit reports the status of the Hsync input polarity detection circuit. It can be used to determine the polarity of the Hsync input. The detection circuit's location is shown Figure 20.

Table 46. Detected Hsync Input Polarity Status

Hsync Polarity Status	Result
0	Hsync polarity is negative/active low.
1	Hsync polarity is positive/active high.

0x16 5 AVS Active Vsync

This bit indicates which Vsync source is being used for the analog interface, the Vsync input or output from the sync separator. If the override bit (0x10, Bit 1) is set to Logic 1, then this bit will be forced to the same state as Bit 0 in Register 0x10.

Table 47. Active Vsync Results

Vsync Detect Register 0x16 Bit 5	Override Register 0x10 Bit 1	AVS
0	0	0
1	0	1
X	1	Bit 0 in 0x10

AVS = 0 means Vsync input. AVS = 1 means sync separator. The override bit is in Register 0x10, Bit 1.

0x16 4 Detected Vsync Output Polarity Status

This bit reports the status of the Vsync output polarity detection circuit. It can be used to determine the polarity of the Vsync output. The detection circuit's location is shown in Figure 20.

Table 48. Detected Vsync Input Polarity Status

Vsync Polarity Status	Result
0	Vsync polarity is active high.
1	Vsync polarity is active low.

0x16 3 Detected Coast Polarity Status

This bit reports the status of the coast input polarity detection circuit. The detection circuit's location is shown in Figure 20. This bit applies only to the internal coast and does not apply when coast is disabled.

Table 49. Detected Coast Input Polarity Status

Hsync Polarity Status	Result
0	Coast polarity is negative/active low.
1	Coast polarity is positive/active high.

0x16 2 Key Read Verification

This bit reports wherever HDCP keys are detected.

Table 50. Key Read Verification

Detect	Function
0	Not detected
1	Detected

0x1B 7 MDA and MCL Three-State

The MDA and MCL three-state feature allows the EEPROM to be programmed in-circuit. The MDA/MCL port must be three-stated before attempting to program the EEPROM using an external master. The keys are stored in an I^2C compatible 3.3 V serial EEPROM of at least 512 bytes. The EEPROM should have a device address of 0xA0.

0x1C 0 RxC Connect

The RxC (DVI differential clock pair) can be disconnected via software if the HDCP specified hot plug detect does not work to resynchronize the HDCP transmitter engine. To use this function, write this bit to 0 (0xR1C to 0x0E) then back to 1 (0xR1C to 0x0F). This signals to the DVI transmitter to restart the HDCP protocol. It is recommended that the user perform this toggle of the bit whenever switching from analog to digital inputs.

Table 51. DVI Clock Connect

Set	Function
0	RxC lines disconnected (open).
1	RxC lines connected internally.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial control interface is provided. Two AD9882A devices can be connected to the 2-wire serial interface, with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bidirectional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must

change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

The five components to serial bus operation are

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communications are initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first eight bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer: read from (1) or write to (0) the slave device. If the transmitted slave address matches the address of the device (set by the state of the SA input pin listed in Table 52), the AD9882A acknowledges by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9882A does not acknowledge.

Table 52. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A6 (MSB)	A5	A4	A3	A2	A1	A0 (LSB)
1	0	0	1	1	0	0
1	0	0	1	1	0	1

Data Transfer via Serial Interface

For each byte of data read or written, the MSB is the first bit of the sequence. If the AD9882A does not acknowledge the master device during a write sequence, the SDA remains high so the master can gen-erate a stop signal. If the master device does not acknowledge the AD9882A during a read sequence, the AD9882A interprets this as end of data. The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9882A requires that the 8-bit address of the control register of interest be written after the slave address has been established. This control register address is the base address for subsequent write operations. The base address autoincrements by one for each byte of data written after the data byte intended for the base address. If there are more bytes transferred than there are available addresses, the address does not increment and remains at its maximum value of 0x1E. Any base address higher than 0x1E does not produce an acknowledge signal.

Data is read from the control registers of the AD9882A in a similar manner. Reading requires two data transfer operations:

- The base address must be written with the R/$\overline{W}$ bit of the slave address byte low to set up a sequential read operation.
- Reading (the R/$\overline{W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register autoincrements after each byte is transferred.

To terminate a read/write sequence to the AD9882A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high. The timing for the read/write is shown in Figure 18, and a typical byte transfer is shown in Figure 19.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

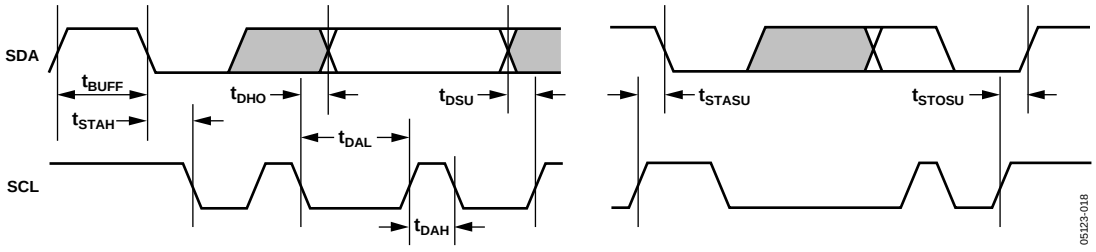

Figure 18. Serial Port Read/Write Timing

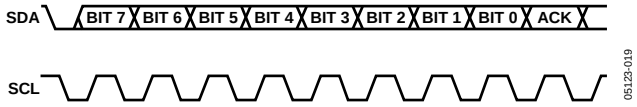

Figure 19. Serial Interface, Typical Byte Transfer

Serial Interface Read/Write Examples

Example 1. Write to one control register

- Start signal
- Slave address byte (R/$\overline{W}$ bit = LOW)
- Base address byte
- Data byte to base address
- Stop signal

Example 2. Write to four consecutive control registers

- Start signal
- Slave address byte (R/$\overline{W}$ bit = LOW)
- Base address byte
- Data byte to base address
- Data byte to (base address + 1)
- Data byte to (base address + 2)
- Data byte to (base address + 3)
- Stop signal

Example 3. Read from one control register

- Start signal
- Slave address byte (R/$\overline{W}$ bit = LOW)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = HIGH)
- Data byte from base address
- Stop signal

Example 4. Read from four consecutive control registers

- Start signal
- Slave address byte (R/$\overline{W}$ bit = LOW)
- Base address byte
- Start signal
- Slave address byte (R/$\overline{W}$ bit = HIGH)
- Data byte from base address
- Data byte from (base address + 1)
- Data byte from (base address + 2)
- Data byte from (base address + 3)
- Stop signal

Table 53. Control of the Sync Block Muxes via the Serial Register

Mux Number(s)	Serial Bus Control Bit	Control Bit State	Result
1 and 2	0x10: Bit 3	0	Pass Hsync
		1	Pass sync-on-green
3	0x10: Bit 0	0	Pass Vsync
		1	Pass sync separator signal
4, 5, and 6	0x0F: Bit 1	0	Pass analog interface signals
		1	Pass digital interface signals

SYNC PROCESSING ENGINE

SYNC SLICER

This section describes the basic operation of the sync processing engine (see Figure 20).

The purpose of the sync slicer is to extract the sync signal from the green graphics channel. A sync signal is not present on all graphics systems (only those with sync-on-green). The sync signal is extracted from the green channel in a two-step process.

1. SOG input is clamped to its negative peak (typically 0.3 V below the black level).
2. The signal goes to a comparator with a variable trigger level, nominally 0.15 V above the clamped level. The output signal is typically a composite sync signal containing both Hsync and Vsync.

SYNC SEPARATOR

A sync separator extracts the Vsync signal from a composite sync signal. It does this through a low-pass filter-like or integrator-like operation. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. So, it rejects any signal shorter than a threshold value, which is somewhere between an Hsync pulse width and a Vsync pulse width.

The sync separator on the AD9882A is an 8-bit digital counter with a 5 MHz clock. It works independently of the polarity of the composite sync signal. Polarities are determined elsewhere on the chip. The counter counts up when Hsync pulses are present. But since Hsync pulses are relatively short in width, the counter reaches only a value of N before the pulse ends. It then starts counting down, eventually reaching 0 before the next Hsync pulse arrives. The specific value of N varies for different video modes, but is always less than 255. For example, with a 1 ms width Hsync, the counter only reaches 5 (1 µs/200 ns = 5). When Vsync is present on the composite sync, the counter also counts up. However, because the Vsync signal is much longer, it counts to a higher number, M. For most video modes, M is at least 255. So, Vsync can be detected on the composite sync signal by detecting when the counter counts to higher than N. The specific count that triggers detection (t) can be programmed through the serial register (0x0E).

Once Vsync has been detected, a similar process detects when it goes inactive. At detection, the counter first resets to 0, then starts counting up when Vsync goes away. In a way similar to the previous case, it detects the absence of Vsync when the counter reaches the threshold count (T). In this way, it rejects noise and/or serration pulses. Once Vsync is determined to be absent, the counter resets to 0 and begins the cycle again.

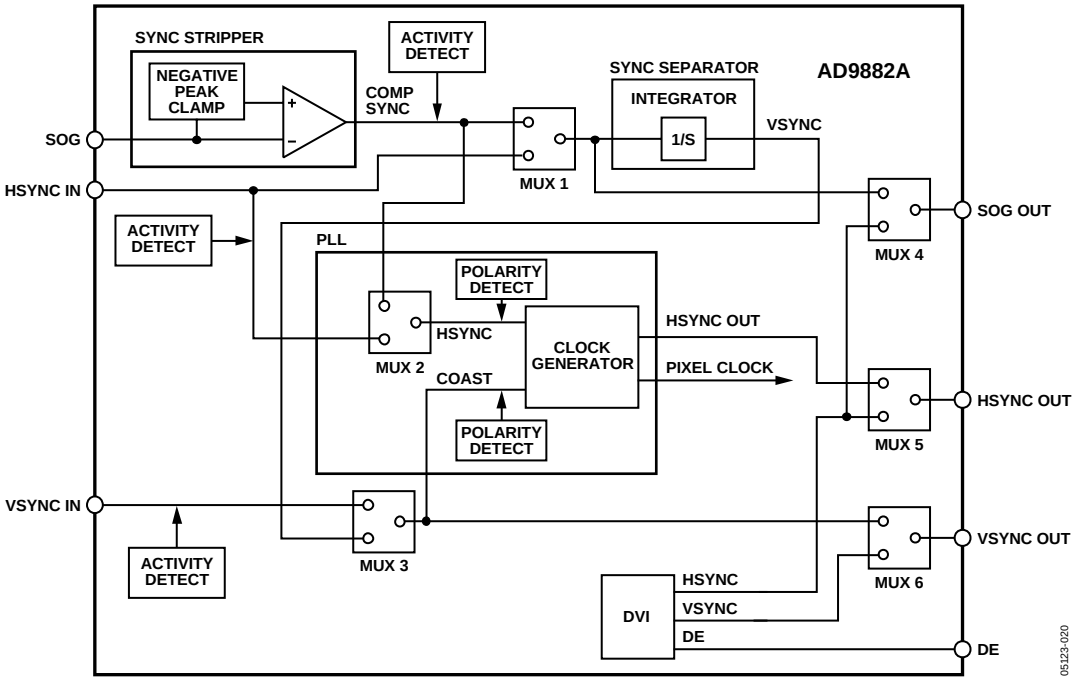

Figure 20. Sync Processing Block Diagram

PCB LAYOUT RECOMMENDATIONS

The AD9882A is a high precision, high speed analog device. To derive the maximum performance from the part, it is important to have a well laid out board. The following is a guide for designing a board using the AD9882A.

ANALOG INTERFACE INPUTS

Using the following layout techniques on the graphics inputs is extremely important.

Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9882A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they will pick up more noise from the board and other external sources.

Place the 75 Ω termination resistors (see Figure 9) as close to the AD9882A chip as possible. Any additional trace length between the termination resistors and the input of the AD9882A increases the magnitude of reflections, which corrupts the graphics signal.

Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω also increase the chance of reflections.

The AD9882A has a very high input bandwidth (300 MHz). While this is desirable for acquiring a high resolution PC graphics signal with fast edges, it means that it captures any high frequency noise present. Therefore, it is important to reduce the amount of noise that gets coupled to the inputs. Avoid running any digital traces near the analog inputs.

Due to the high bandwidth of the AD9882A, sometimes low-pass filtering the analog inputs can help to reduce noise. (For many applications, filtering is unnecessary.) Experiments have shown that placing a series ferrite bead prior to the 75 Ω termination resistor is helpful in filtering out excess noise. Specifically, the part used was the #2508051217Z0 from Fair-Rite, but different applications may work best with different bead values. Alternatively, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor can also be beneficial.

DIGITAL INTERFACE INPUTS

Many of the same techniques that are recommended for the analog interface inputs should also be used for the digital interface inputs. It is important to minimize trace lengths, then make the input trace impedances match the input termination (typically 50 Ω). Each differential input pair (R_{X0+}, R_{X0-}, R_{XC+}, R_{XC-}, and so on) should be routed together using 50 Ω strip line routing techniques and should be kept as short as possible. No other components, such as clamping diodes, should be placed on these inputs. Every effort should be made to route these signals on a single layer (component layer) with no vias.

POWER SUPPLY BYPASSING

Bypassing each power supply pin with a 0.1 µF capacitor is recommended. The exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the side of the PC board opposite the AD9882A, as that interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane ->to the capacitor ->to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of PV_D (the clock generator supply). Abrupt changes in PV_D can result in similarly abrupt changes in sampling clock phase and frequency. This can be avoided by careful attention to regulation, filtering, and bypassing. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use levels of power when active (during active picture time) that are substantially different from those used when they are idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner, power source (for example, from a 12 V supply).

Using a single ground plane for the entire board is also recommended. Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental, because each separate ground plane is smaller than one common ground plane, and can result in long ground loops.

In some cases, using separate ground planes is unavoidable. When they must be used, it is recommended that at least a single ground plane be placed under the AD9882A. The location of the split should be at the receiver of the digital outputs. In this case, it is even more important to place components wisely, because the current loops are much longer (current takes the path of least resistance). The following is an example of a current loop: power plane -> AD9882A -> digital output trace -> digital data receiver -> digital ground plane -> analog ground plane.

PLL

Place the PLL loop filter components as close to the FILT pin as possible.

Do not place any digital or other high frequency traces near these components.

Use the values suggested in the data sheet with 10% or smaller tolerances.

OUTPUTS: DATA AND CLOCKS

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance and require more current, which causes more internal digital noise.

Shorter traces reduce the possibility of reflections.

Adding a series resistor with a value of 22 Ω to 100 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9882A. However, if 50 Ω traces are used on the PCB, the data output should not need these resistors.

A 22 Ω resistor on the DATACK output should provide good impedance matching that can reduce reflections. If EMI or current spiking is a concern, use a lower drive strength setting by adjusting Register 0x14. If series resistors are used, place them as close as possible to the AD9882A pins but avoid adding vias or extra length to the output trace to get the resistors closer.

If possible, limit the capacitance that each of the digital outputs drives to less than 10 pF by keeping traces short and connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the AD9882A, creating more digital noise on its power supplies.

DIGITAL INPUTS

The digital inputs on the AD9882A were designed to work with 3.3 V signals, but are tolerant of 5.0 V signals. No extra components need to be added, if 5.0 V logic is used.

Any noise that gets onto the Hsync input trace adds jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

VOLTAGE REFERENCE

Bypass with a 0.1 µF capacitor. Place as close as possible to the AD9882A pin. Make the ground connection as short as possible.

OUTLINE DIMENSIONS

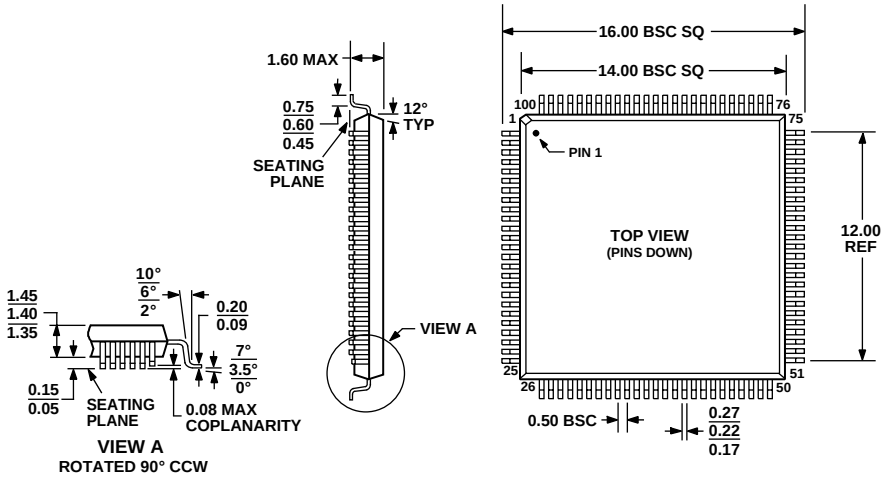

Figure 21. 100-Lead Quad Flatpack [LQFP]
(ST-100)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Option
AD9882AKSTZ-100[1]	0°C to 70°C	ST-100
AD9882AKSTZ-140[1]	0°C to 70°C	ST-100
AD9882A/PCB		Evaluation Kit

[1] Z = Pb-free part.

NOTES

NOTES

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