THE DATASHEET OF

AD9992BBCZRL

www.win-source.net 0086-755-83957316

12-Bit CCD Signal Processor with *Precision Timing* Generator

AD9992

FEATURES

1.8 V AFETG core
Internal LDO regulator and charge pump circuitry
Compatibility with 3 V or 1.8 V systems
24 programmable vertical clock outputs
Correlated double sampler (CDS) with −3 dB, 0 dB, +3 dB, and +6 dB gain
6 dB to 42 dB, 10-bit variable gain amplifier (VGA)
12-bit, 40 MHz ADC
Black level clamp with variable level control
Complete on-chip timing generator
***Precision Timing* core with 400 ps resolution**
On-chip 3 V horizontal and RG drivers
General-purpose outputs (GPOs) for shutter and system support
On-chip driver for external crystal
On-chip sync generator with external sync input
105-lead CSP_BGA package, 8 mm × 8 mm, 0.65 mm pitch

APPLICATIONS

Digital still cameras

GENERAL DESCRIPTION

The AD9992 is a highly integrated CCD signal processor for digital still camera applications. It includes a complete analog front end with analog to digital conversion combined with a full-function programmable timing generator. The timing generator is capable of supporting up to 24 vertical clock signals to control advanced CCDs. A *Precision Timing*™ core allows adjustment of high speed clocks with approximately 400 ps resolution at 40 MHz operation. The AD9992 also contains eight general-purpose inputs/outputs that can be used for shutter and system functions.

The AD9992 is specified at pixel rates of up to 40 MHz. The analog front end includes black level clamping, CDS, VGA, and a 12-bit analog-to-digital converter (ADC). The timing generator provides all the necessary CCD clocks: RG, H-clocks, V-clocks, sensor gate pulses, substrate clock, and substrate bias control. Operation is programmed using a 3-wire serial interface.

The AD9992 is specified over an operating temperature range of −25°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

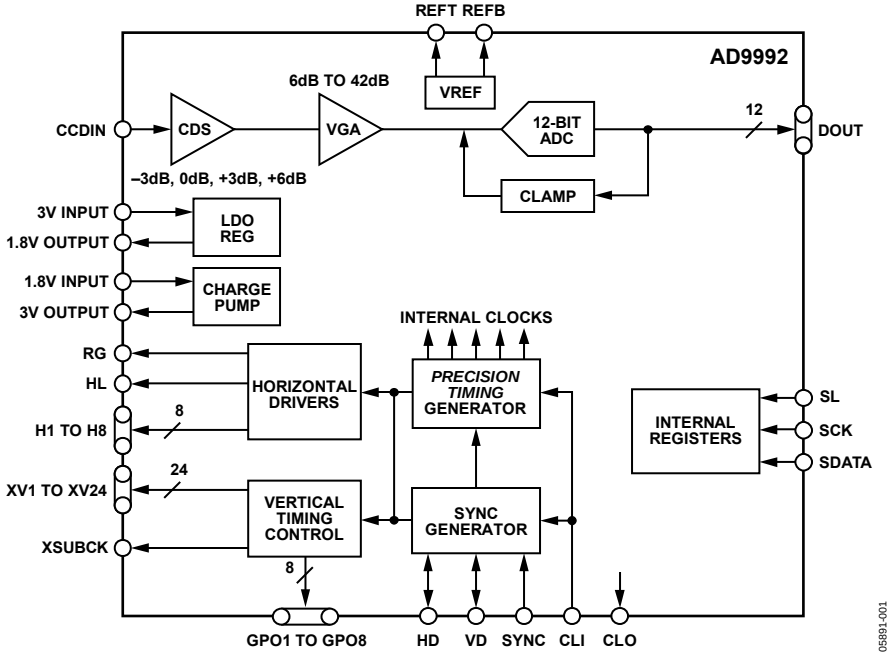

Figure 1.

Rev. C

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REVISION HISTORY

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9/07—Rev. A to Rev. B

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7/07—Rev. 0 to Rev. A

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1/06—Revision 0: Initial Version

SPECIFICATIONS

Table 1.

Parameter	Min	Typ	Max	Unit
TEMPERATURE RANGE				
Operating	−25		+85	°C
Storage	−65		+150	°C
POWER SUPPLY VOLTAGE INPUTS				
AVDD (AFE Analog Supply)	1.6	1.8	2.0	V
TCVDD (Timing Core Supply)	1.6	1.8	2.0	V
CLIVDD (CLI Input Supply)	1.6	3.0	3.6	V
RGVDD (RG, HL Driver)	2.7	3.0	3.6	V
HVDD1/HVDD2 (H1 to H8 Drivers)[1]	2.7	3.0	3.6	V
DVDD (Digital Logic)	1.6	1.8	2.0	V
DRVDD (Parallel Data Output Drivers)	1.6	3.0	3.6	V
IOVDD (Digital I/O)	1.6	3.0	3.6	V
XVVDD (Vertical Output Drivers)	1.6	3.0	3.6	V
CP1P8 (CP Supply Input)	1.6	1.8	2.0	V
LDOIN (LDO Supply Input)	2.25	3.0	3.6	V
POWER SUPPLY CURRENTS—40 MHz OPERATION				
AVDD (1.8 V)		27		mA
TCVDD (1.8 V)		5		mA
CLIVDD (3 V)		1.5		mA
RGVDD (3.3 V, 20 pF RG Load, 20 pF HL Load)		10		mA
HVDD1/HVDD2 (3.3 V, 480 pF Total Load on H1 to H8)[1]		59		mA
DVDD (1.8 V)		9.5		mA
DRVDD (3 V, 10 pF Load on Each DOUT Pin)		6		mA
IOVDD (3 V, Depends on Load and Output Frequency of Digital I/O)		2		mA
XVVDD (3 V, Depends on Load and Output Frequency of XV Signals)		2		mA
POWER SUPPLY CURRENTS—STANDBY MODE OPERATION				
Standby1 Mode		12		mA
Standby2 Mode		5		mA
Standby3 Mode		1.5		mA
MAXIMUM CLOCK RATE (CLI)	40			MHz

[1] The total power dissipated by the HVDD (or RGVDD) supply can be approximated using the equation

Total HVDD Power = [$C_L \times HVDD \times Pixel\ Frequency$] × *HVDD*

Reducing the capacitive load and/or reducing the HVDD supply reduces the power dissipation. C_L is the total capacitance seen by all H-outputs.

DIGITAL SPECIFICATIONS

IOVDD = 1.6 V to 3.6 V, RGVDD = HVDD = 2.7 V to 3.6 V, C_L = 20 pF, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit
LOGIC INPUTS (IOVDD)					
High Level Input Voltage	V_{IH}	V_{DD} – 0.6			V
Low Level Input Voltage	V_{IL}			0.6	V
High Level Input Current	I_{IH}		10		µA
Low Level Input Current	I_{IL}		10		µA
Input Capacitance	C_{IN}		10		pF
LOGIC OUTPUTS (IOVDD, XVDD)					
High Level Output Voltage @ I_{OH} = 2 mA	V_{OH}	V_{DD} – 0.5			V
Low Level Output Voltage @ I_{OL} = 2 mA	V_{OL}			0.5	V
RG and H-DRIVER OUTPUTS (HVDD, RGVDD)					
High Level Output Voltage @ Maximum Current	V_{OH}	V_{DD} – 0.5			V
Low Level Output Voltage @ Maximum Current	V_{OL}			0.5	V
Maximum Output Current (Programmable)		18			mA
Maximum Load Capacitance (for Each Output)		60			pF

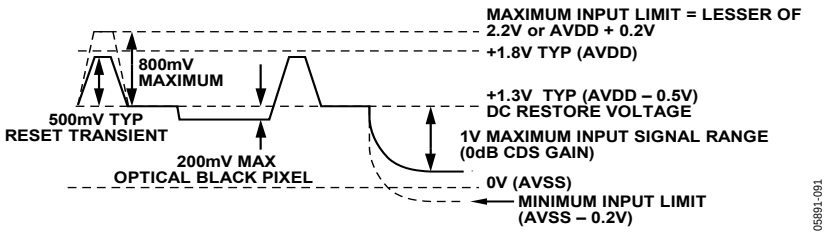


Figure 2. Input Signal Characteristics
(See Allowable OB Pixel Amplitude in Table 3)

ANALOG SPECIFICATIONS

AVDD = 1.8 V, f_{CLI} = 40 MHz, typical timing specifications, T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
CDS					
Allowable CCD Reset Transient		0.5	0.8	V	The limit is the lower of AVDD + 0.2 V or 2.2 V.
CDS Gain Accuracy					VGA gain = 6.3 dB (Code 15, default value).
−3.0 dB CDS Gain	−3.3	−2.8	−2.3	dB	
0 dB CDS Gain	−0.5	0	+0.5	dB	
+3 dB CDS Gain	2.4	2.9	3.4	dB	
+6 dB CDS Gain	5.0	5.5	6.0	dB	
Maximum Input Range Before Saturation					VGA gain = 6.3 dB (Code 15, default value).
−3 dB CDS Gain		1.4		V p-p	
0 dB CDS Gain		1.0		V p-p	
+3 dB CDS Gain		0.7		V p-p	
+6 dB CDS Gain		0.5		V p-p	
Allowable OB Pixel Amplitude (See Figure 2)					
0 dB CDS Gain (Default)	−100		+200	mV	
+6 dB CDS Gain	−50		+100	mV	
VARIABLE GAIN AMPLIFIER (VGA)					
Gain Control Resolution		1024		Steps	
Gain Monotonicity		Guaranteed			
Gain Range					
Low Gain (VGA Code 15, Default)		6.3		dB	
Maximum Gain (VGA Code 1023)		42.4		dB	
BLACK LEVEL CLAMP					
Clamp Level Resolution		1024		Steps	
Clamp Level					Measured at ADC output.
Minimum Clamp Level (Code 0)		0		LSB	
Maximum Clamp Level (Code 1023)		255		LSB	
ADC					
Resolution	12			Bits	
Differential Nonlinearity (DNL)	−1.0	±0.5	+1.0	LSB	
No Missing Codes		Guaranteed			
Integral Nonlinearity (INL)		1	4	LSB	
Full-Scale Input Voltage		2.0		V	
VOLTAGE REFERENCE					
Reference Top Voltage (REFT)		1.4		V	
Reference Bottom Voltage (REFB)		0.4		V	
SYSTEM PERFORMANCE					Includes entire signal chain.
Gain Accuracy					0 dB CDS gain.
Low Gain (VGA Code 15)	5.8	6.3	6.8	dB	Gain = (0.0358 × Code) + 5.76 dB.
Maximum Gain (VGA Code 1023)	41.9	42.4	42.9	dB	
Peak Nonlinearity, 1.0 V Input Signal		0.1	0.2	%	6 dB VGA gain, 0 dB CDS gain applied.
Total Output Noise		0.5		LSB rms	AC-grounded input, 6 dB VGA gain applied.
Power Supply Rejection (PSR)		50		dB	Measured with step change on supply.

TIMING SPECIFICATIONS

C_L = 20 pF, AVDD = DVDD = TCVDD = 1.8 V, DRVDD = 3.0 V, f_{CLI} = 40 MHz, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit
MASTER CLOCK (See Figure 15)					
CLI Clock Period	t_{CONV}	25			ns
CLI High/Low Pulse Width		10	12.5	15	ns
Delay from CLI Rising Edge to Internal Pixel Position 0	t_{CLIDLY}		6		ns
SLAVE MODE SPECIFICATIONS (See Figure 76)					
VD Falling Edge to HD Falling Edge in Slave Mode	t_{VDHD}	0		VD period − 5 × t_{CONV}	ns
HD Edge to CLI Rising Edge (Only Valid if OSC_RSTB = LO)	t_{HDCLI}	3		t_{CONV} − 2	ns
HD Edge to CLO Rising Edge (Only Valid if OSC_RSTB = HI)	t_{HDCLO}	3		t_{CONV} − 2	ns
Inhibit Region for SHP Edge Location	t_{SHPINH}	48		63	Edge location
AFE CLPOB PULSE WIDTH (See Figure 22 and Figure 32)[1, 2]		2	20		Pixels
AFE SAMPLE LOCATION (See Figure 16 and Figure 19)[1]					
SHP Sample Edge to SHD Sample Edge	t_{S1}	11	12.5		ns
DATA OUTPUTS (See Figure 20 and Figure 21)					
Output Delay from DCLK Rising Edge	t_{OD}		1		ns
Inhibited Area for DOUTPHASE Edge Location	$t_{DOUTINH}$	SHDLOC + 1		SHDLOC + 15	Edge location
Pipeline Delay from SHP/SHD Sampling to DOUT			16		Cycles
SERIAL INTERFACE (See Figure 83)					
Maximum SCK Frequency (Must Not Exceed CLI Frequency)	f_{SCLK}	40			MHz
SL to SCK Setup Time	t_{LS}	10			ns
SCK to SL Hold Time	t_{LH}	10			ns
SDATA Valid to SCK Rising Edge Setup	t_{DS}	10			ns
SCK Falling Edge to SDATA Valid Hold	t_{DH}	10			ns
INHIBIT REGION FOR SHP AND SHD WITH RESPECT TO H-CLOCK EDGE PLACEMENT (see Figure 19) for H*POL = 1					
RETIME = 0, MASK = 0	t_{SHDINH}	H*NEGLOC − 15		H*NEGLOC − 0	Edge location
RETIME = 0, MASK = 1	t_{SHDINH}	H*POSLOC − 15		H*POSLOC − 0	Edge location
RETIME = 1, MASK = 0	t_{SHPINH}	H*NEGLOC − 15		H*NEGLOC − 0	Edge location
RETIME = 1, MASK = 1	t_{SHPINH}	H*POSLOC − 15		H*POSLOC − 0	Edge location

[1] Parameter is programmable.
[2] Minimum CLPOB pulse width is for functional operation only. Wider typical pulses are recommended to achieve good clamp performance.

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	With Respect To	Rating
AVDD	AVSS	−0.2 V to +2.2 V
TCVDD	TCVSS	−0.2 V to +2.2 V
HVDD1/HVDD2	HVSS1/HVSS2	−0.3 V to +3.9 V
RGVDD	RGVSS	−0.3 V to +3.9 V
DVDD	DVSS	−0.2 V to +2.2 V
DRVDD	DRVSS	−0.3 V to +3.9 V
IOVDD	DVSS	−0.3 V to +3.9 V
XVVDD	DVSS	−0.3 V to +3.9 V
CLIVDD	TCVSS	−0.3 V to +3.9 V
CP1P8	CPVSS	−0.2 V to +2.2 V
RG Output	RGVSS	−0.3 V to RGVDD + 0.3 V
H1 to H8, HL Output	HVSS1/HVSS2	−0.3 V to HVDD + 0.3 V
Digital Outputs	DVSS	−0.3 V to IOVDD + 0.3 V
Digital Inputs	DVSS	−0.3 V to IOVDD + 0.3 V
SCK, SL, SDATA	DVSS	−0.3 V to IOVDD + 0.3 V
REFT, REFB, CCDIN	AVSS	−0.2 V to AVDD + 0.2 V
Junction Temperature		150°C
Lead Temperature, 10 sec		350°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
106-Lead CSP_BGA	40.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

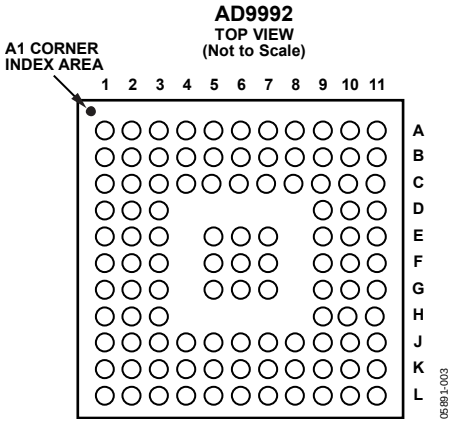


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	GPO8	DIO	General-Purpose Output 8
B2	GPO7	DIO	General-Purpose Output 7
C2	GPO6	DIO	General-Purpose Output 6
B1	GPO5	DIO	General-Purpose Output 5
B4	GPO4	DIO	General-Purpose Output 4
C1	GPO3	DIO	General-Purpose Output 3
D2	GPO2	DIO	General-Purpose Output 2
C3	GPO1	DIO	General-Purpose Output 1
D3	SYNC	DI	External System Sync Input
E2	VD	DIO	Vertical Sync Pulse (input for slave mode, output for master mode)
D1	HD	DIO	Horizontal Sync Pulse (input for slave mode, output for master mode)
E7	RSTB	DI	External Reset Input (active low pulse to reset, internal pull-up resistor)
E6	IOVDD	P	Digital I/O Supply: 1.8 V, 3.0 V (GPO, SUBCK, HD/VD, SL, SCK, SDATA, SYNC, RSTB)
E5	IOVSS	P	Digital I/O Ground
E3	XVVDD	P	XV Output Supply: 1.8 V, 3.0 V
E1	XSUBCK	DO	CCD Substrate Clock
F2	XV1	DO	CCD Vertical Clock 1
F3	XV2	DO	CCD Vertical Clock 2
F7	XV3	DO	CCD Vertical Clock 3
G3	XV4	DO	CCD Vertical Clock 4
F5	XV5	DO	CCD Vertical Clock 5
F6	XV6	DO	CCD Vertical Clock 6
G2	XV7	DO	CCD Vertical Clock 7
F1	XV8	DO	CCD Vertical Clock 8
G1	XV9	DO	CCD Vertical Clock 9
G5	XV10	DO	CCD Vertical Clock 10
H2	XV11	DO	CCD Vertical Clock 11
H1	XV12	DO	CCD Vertical Clock 12
G6	XV13	DO	CCD Vertical Clock 13
G7	XV14	DO	CCD Vertical Clock 14
J2	XV15	DO	CCD Vertical Clock 15
J1	XV16	DO	CCD Vertical Clock 16
L1	XV17	DO	CCD Vertical Clock 17
L2	XV18	DO	CCD Vertical Clock 18

Pin No.	Mnemonic	Type[1]	Description
L3	XV19	DO	CCD Vertical Clock 19
K1	XV20	DO	CCD Vertical Clock 20
K2	XV21	DO	CCD Vertical Clock 21
K3	XV22	DO	CCD Vertical Clock 22
J3	XV23	DO	CCD Vertical Clock 23
H3	XV24	DO	CCD Vertical Clock 24
L4	DVDD	P	Digital Logic Supply: 1.8 V
K4	DVSS	P	Digital Logic Ground
L6	D0	DO	Data Output 0 (LSB)
K6	D1	DO	Data Output 1
J6	D2	DO	Data Output 2
L7	D3	DO	Data Output 3
K7	D4	DO	Data Output 4
J7	D5	DO	Data Output 5
L8	D6	DO	Data Output 6
K8	D7	DO	Data Output 7
J8	D8	DO	Data Output 8
L9	D9	DO	Data Output 9
K9	D10	DO	Data Output 10
J9	D11	DO	Data Output 11 (MSB)
L10	DCLK	DO	Data Clock Output
K10	DRVSS	P	Data Driver Ground
L11	DRVDD	P	Data Driver Supply: 1.8 V, 3.0 V
K11	CP3P3	P	Charge Pump 3.3 V Output
J10	CPFCT	AO	Charge Pump Flying Capacitor Top
J11	CPFCB	AO	Charge Pump Flying Capacitor Bottom
H10	CPVSS	P	Charge Pump Ground
H11	CP1P8	P	Charge Pump 1.8 V Input
H9	CPCLI	DI	Charge Pump Clock Input
G11	LDO3P2EN	DI	LDO 3.2 V Output Enable
G9	LDOVSS	P	LDO Ground
F10	LDO1P8EN	DI	LDO 1.8 V Output Enable
F11	SENSE	AI	LDO Output Sense
E11	LDOOUT	AO	LDO Output Voltage
E10	LDOIN	P	LDO 3.3 V Input
F9	H1	DO	CCD Horizontal Clock 1
E9	H2	DO	CCD Horizontal Clock 2
D11	HVSS1	P	H-Driver Ground 1
C11	HVDD1	P	H-Driver Supply 1: 3.3 V
D10	H3	DO	CCD Horizontal Clock 3
C10	H4	DO	CCD Horizontal Clock 4
D9	H5	DO	CCD Horizontal Clock 5
C9	H6	DO	CCD Horizontal Clock 6
B11	HVSS2	P	H-Driver Ground 2
A11	HVDD2	P	H-Driver Supply 2: 3.3 V
B10	H7	DO	CCD Horizontal Clock 7
A10	H8	DO	CCD Horizontal Clock 8
B9	HL	DO	CCD Last Horizontal Clock
B8	RGVSS	P	RG Driver Ground
A8	RGVDD	P	RG Driver Supply: 3.3 V
C8	RG	DO	CCD Reset Gate Clock
B7	TCVSS	P	Analog Ground for Timing Core
A7	TCVDD	P	Timing Core Supply: 1.8 V

Pin No.	Mnemonic	Type[1]	Description
C7	CLIVDD	P	CLI Input Supply: 3.0 V
C6	CLO	DO	Clock Output for Crystal
C5	CLI	DI	Reference Clock Input
B6	AVDD	P	AFE Supply: 1.8 V
A6	CCDIN	AI	CCD Signal Input
B5, A5	AVSS	P	Analog Supply Ground
A4	REFT	AO	Voltage Reference Top Bypass
A3	REFB	AO	Voltage Reference Bottom Bypass
C4	SL	DI	3-Wire Serial Load Pulse (internal pull-up resistor)
A2	SDATA	DI	3-Wire Serial Data Input
B3	SCK	DI	3-Wire Serial Clock
A9, G10, K5, J4, J5, L5	NC		Not Internally Connected

[1] DIO = digital input/output, DI = digital input, P = power, DO = digital output, AI = analog input, AO = analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

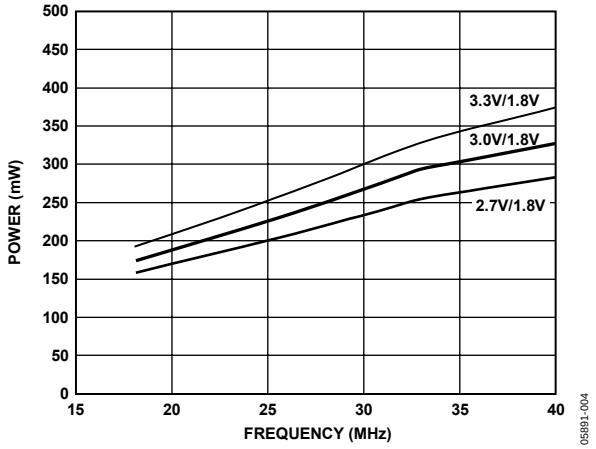


Figure 4. Power vs. Frequency
(AVDD = TCVDD = DVDD = 1.8 V, All Other Supplies at 2.7 V, 3.0 V, or 3.3 V)

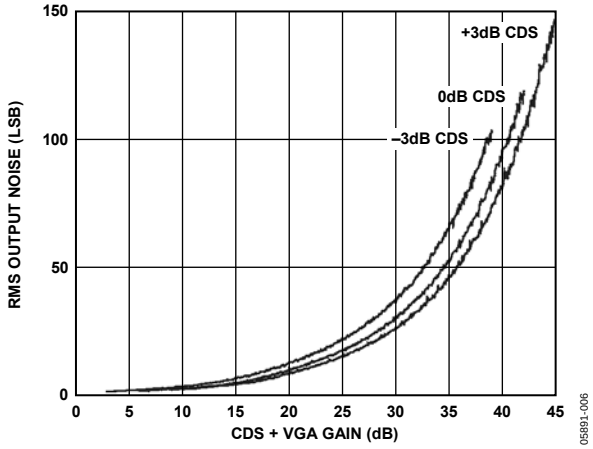


Figure 6. Output Noise vs. Total Gain (CDS + VGA)

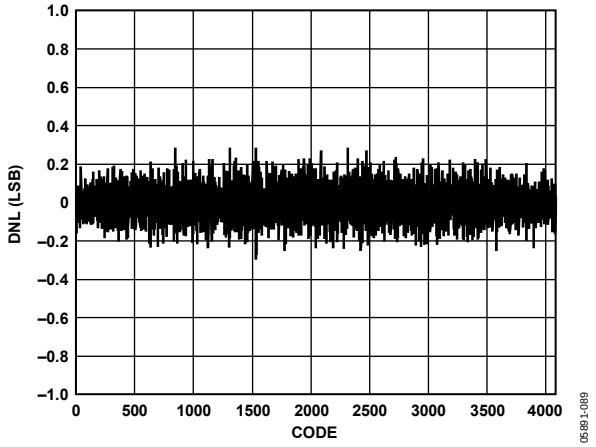


Figure 5. Typical Differential Nonlinearity (DNL) Performance

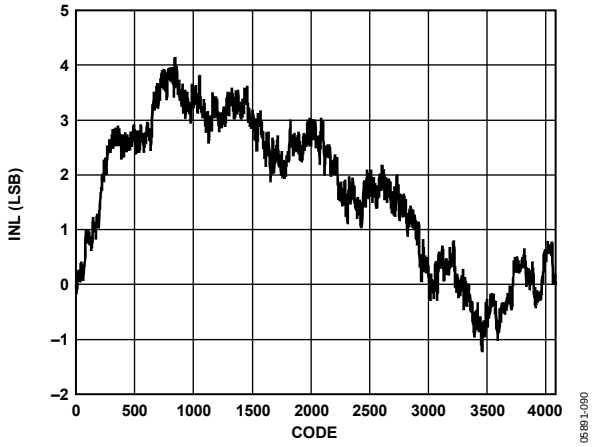


Figure 7. Typical Integral Nonlinearity (INL) Performance

EQUIVALENT CIRCUITS

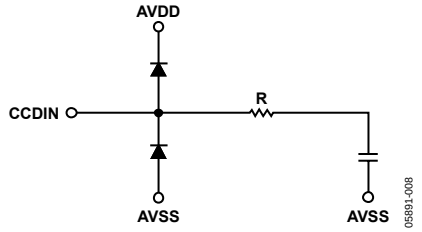


Figure 8. CCDIN

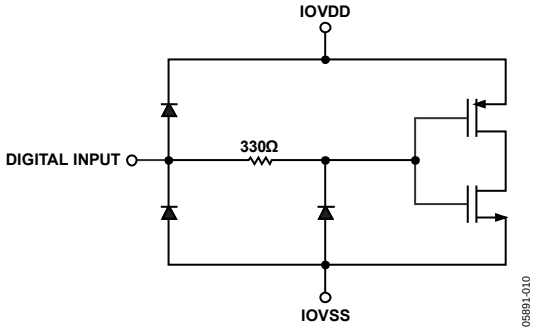


Figure 10. Digital Inputs

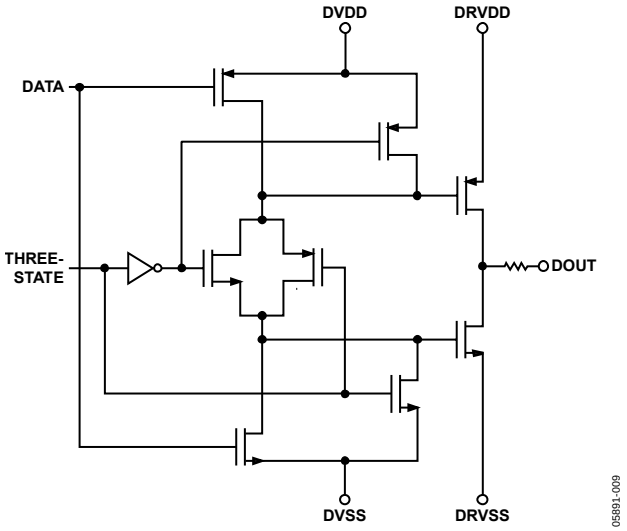


Figure 9. Digital Data Outputs

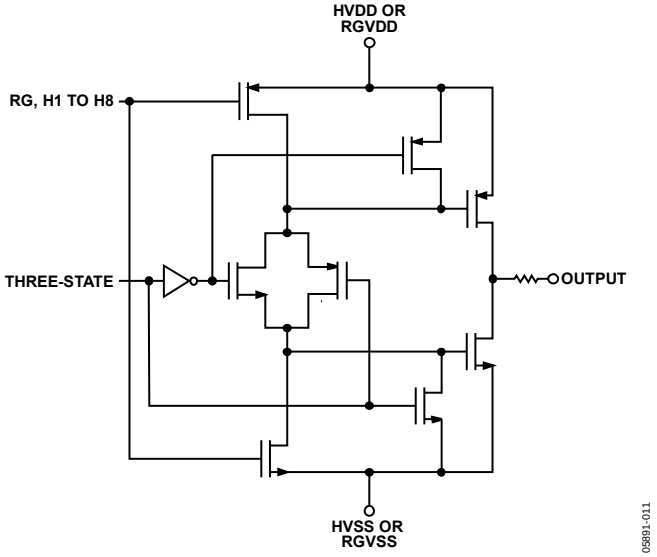


Figure 11. H1 to H8, HL, RG Drivers

TERMINOLOGY

Differential Nonlinearity (DNL)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. Therefore, every code must have a finite width. No missing codes guaranteed to 12-bit resolution indicates that all 4096 codes must be present over all operating conditions.

Peak Nonlinearity
Peak nonlinearity, a full signal chain specification, refers to the peak deviation of the output of the AD9992 from a true straight line. The point used as zero scale occurs 0.5 LSB before the first code transition. Positive full scale is defined as a level 1 LSB and 0.5 LSB beyond the last code transition. The deviation is measured from the middle of each particular output code to the true straight line. The error is then expressed as a percentage of the 2 V ADC full-scale signal. The input signal is always appropriately amplified to fill the full-scale range of the ADC.

Total Output Noise
The rms output noise is measured using histogram techniques. The standard deviation of the ADC output codes is calculated in LSB and represents the rms noise level of the total signal chain at the specified gain setting. The output noise can be converted to an equivalent voltage using the relationship

$$1\ \text{LSB} = (\textit{ADC Full Scale}/2^{n}\ \textit{Codes})$$

where n is the bit resolution of the ADC. For the AD9992, 1 LSB is 0.488 mV.

Power Supply Rejection (PSR)
The PSR is measured with a step change applied to the supply pins. The PSR specification is calculated from the change in data outputs for a given step change in the supply voltage.

SYSTEM OVERVIEW

Figure 12 shows the typical system block diagram for the AD9992 in master mode. The CCD output is processed by AD9992 AFE circuitry, which consists of a CDS, VGA, black level clamp, and ADC. The digitized pixel information is sent to the digital image processor chip, which performs the postprocessing and compression. To operate the CCD, all CCD timing parameters are programmed into the AD9992 from the system microprocessor through the 3-wire serial interface. The AD9992 generates the CCD's horizontal and vertical clocks and internal AFE clocks from the master clock, CLI, which is provided by the image processor or external crystal,. External synchronization is provided by a sync pulse from the microprocessor, which resets the internal counters and resyncs the VD and HD outputs.

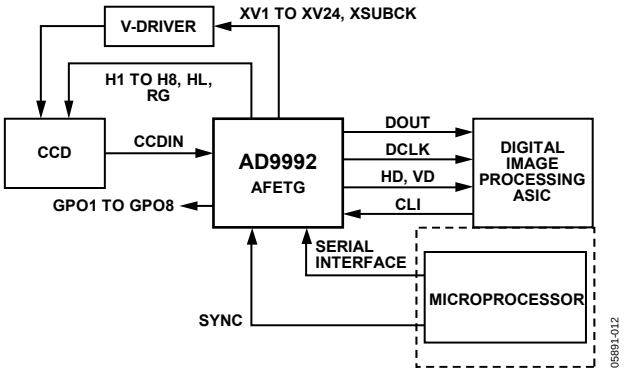


Figure 12. Typical System Block Diagram, Master Mode

Alternatively, the AD9992 can operate in slave mode. In slave mode, the VD and HD are provided externally from the image processor, and all AD9992 timing synchronizes with VD and HD.

H-drivers for H1 to H8, HL, and RG are included in the AD9992, allowing these clocks to be directly connected to the CCD. An H-driver voltage of up to 3.3 V is supported. An external V-driver is required for the vertical transfer clocks, the sensor gate pulses, and the substrate clock.

The AD9992 includes programmable general-purpose outputs (GPO), which can trigger mechanical shutter and strobe (flash) circuitry.

Figure 13 and Figure 14 show the maximum horizontal and vertical counter dimensions for the AD9992. All internal horizontal and vertical clocking is controlled by these counters, which specify line and pixel locations. Maximum HD length is 8192 pixels per line; maximum VD length is 8192 lines per field.

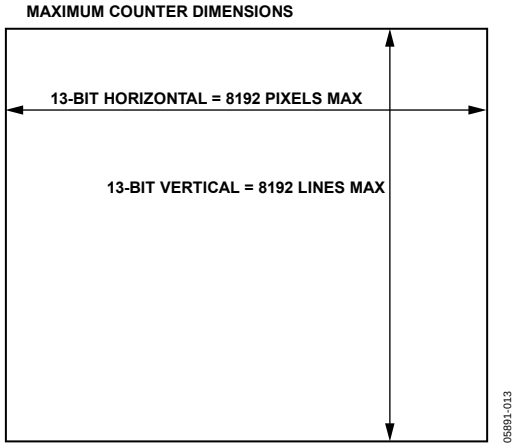


Figure 13. Vertical and Horizontal Counters

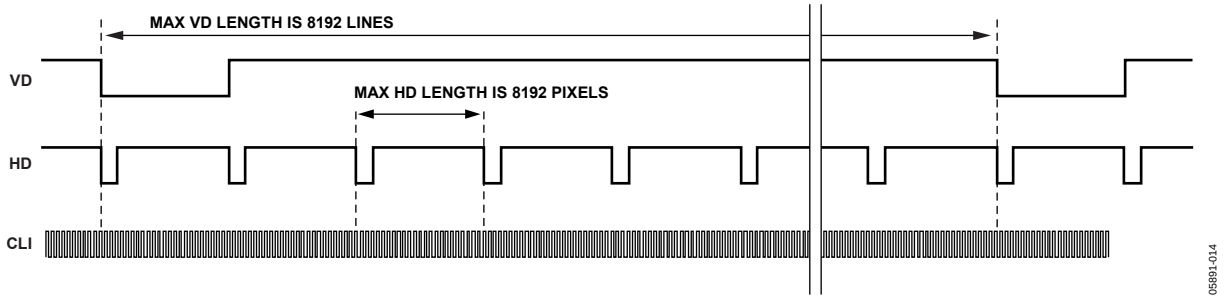


Figure 14. Maximum VD/HD Dimensions

HIGH SPEED *PRECISION TIMING* CORE

The AD9992 generates high speed timing signals using the flexible *Precision Timing* core. This core is the foundation for generating timing used for both the CCD and the AFE; it includes the reset gate RG, horizontal drivers H1 to H8, HL, and SHP/SHD sample clocks. A unique architecture makes it routine for the system designer to optimize image quality by providing precise control over the horizontal CCD readout and the AFE correlated double sampling.

The high speed timing of the AD9992 operates the same way in either master or slave mode configuration. For more information on synchronization and pipeline delays, see the Power-Up Sequence for Master Mode section.

Timing Resolution

The *Precision Timing* core uses a 1× master clock input (CLI) as a reference. This clock should be the same as the CCD pixel clock frequency. Figure 15 illustrates how the internal timing core divides the master clock period into 64 steps or edge positions. Using a 40 MHz CLI frequency, the edge resolution of the *Precision Timing* core is approximately 0.4 ns. If a 1× system clock is not available, it is possible to use a 2× reference clock by programming the CLIDIVIDE register (AFE Register Address 0x0D). The AD9992 then internally divides the CLI frequency by 2.

The AD9992 includes a master clock output (CLO) which is the inverse of CLI. This output should be used as a crystal driver. A crystal can be placed between the CLI and CLO pins to generate the master clock for the AD9992.

High Speed Clock Programmability

Figure 16 shows when the high speed clocks RG, H1 to H8, SHP, and SHD are generated. The RG pulse has programmable rising and falling edges and can be inverted using the polarity control. Horizontal Clock H1 has programmable rising and falling edges and polarity control. In HCLK Mode 1, H3, H5, and H7 are equal to H1. H2, H4, H6, and H8 are always inverses of H1.

The edge location registers are each six bits wide, allowing selection of all 64 edge locations. Figure 19 shows the default timing locations for all high speed clock signals.

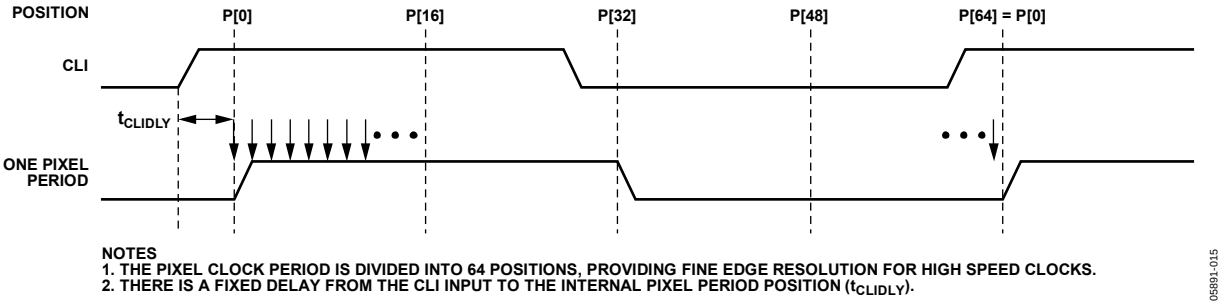


Figure 15. High Speed Clock Resolution from CLI, Master Clock Input

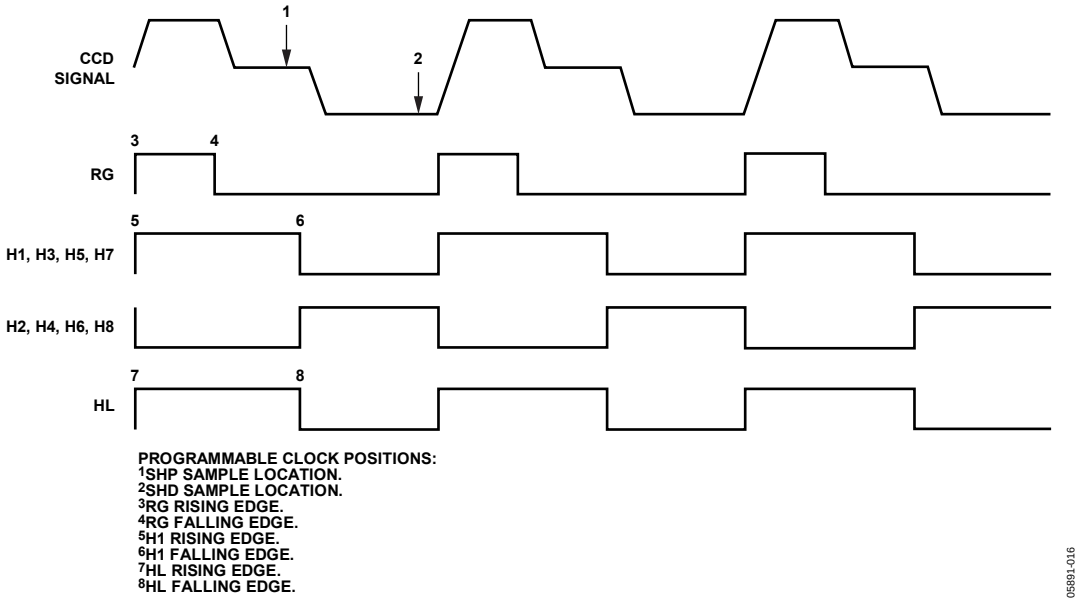


Figure 16. High Speed Clock Programmable Locations (HCLKMODE = 001)

H-Driver and RG Outputs

In addition to the programmable timing positions, the AD9992 features on-chip output drivers for the RG, HL, and H1 to H8 outputs. These drivers are powerful enough to drive the CCD inputs directly. The H-driver and RG current can be adjusted for optimum rise/fall time for a particular load by using the drive strength control registers (Address 0x35 and Address 0x36). The 3-bit drive setting for each output is adjustable in 4.3 mA increments: 0 = three-state; 1 = 4.3 mA; 2 = 8.6 mA; 3 = 12.9 mA; and 4, 5, 6, 7 = 17.2 mA.

As shown in Figure 16, when HCLK Mode 1 is used, the H2, H4, H6, and H8 outputs are inverses of the H1, H3, H5, and H7 outputs, respectively. Using the HCLKMODE register (Address 0x23, Bits [9:7]), it is possible to select a different configuration. Table 9 shows a comparison of the different programmable settings for each HCLK mode. Figure 17 and Figure 18 show the settings for HCLK Mode 2 and HCLK Mode 3, respectively.

It is recommended that all H1 to H8 outputs on the AD9992 be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs should only have the AD9992 H1, H3, H5, and H7 outputs connected together to drive the CCD's H1, and the H2, H4, H6, and H8 outputs connected together to drive the CCD's H2. Similarly, a CCD with H1, H2, H3, and H4 inputs should have

- H1 and H3 connected to the CCD's H1.
- H2 and H4 connected to the CCD's H2.
- H5 and H7 connected to the CCD's H3.
- H6 and H8 connected to the CCD's H4.

Table 8. Timing Core Register Parameters for H1, H2, HL, RG, SHP, SHD

Parameter	Length	Range	Description
Polarity	1b	High/low	Polarity control for H1, H2, HL, and RG (0 = inversion, 1 = no inversion)
Positive Edge	6b	0 to 63 edge location	Positive edge location for H1, H2, HL, and RG
Negative Edge	6b	0 to 63 edge location	Negative edge location for H1, H2, HL, and RG
Sampling Location	6b	0 to 63 edge location	Sampling location for internal SHP and SHD signals
Drive Strength	3b	0 to 4 current steps	Drive current for H1 to H8 , HL, and RG outputs (4.3 mA per step)

Table 9. HCLK Modes, Selected by Address 0x23, Bits[9:7]

HCLKMODE	Register Value	Description
Mode 1	001	H1 edges are programmable, with H3 = H5 = H7 = H1, H2 = H4 = H6 = H8 = inverse of H1
Mode 2	010	H1 edges are programmable, with H3 = H5 = H7 = H1 H2 edges are programmable, with H4 = H6 = H8 = H2
Mode 3	100	H1 edges are programmable, with H3 = H1 and H2 = H4 = inverse of H1 H5 edges are programmable, with H7 = H5 and H6 = H8 = inverse of H5
Invalid Selection	000, 011, 101, 110, 111	Invalid register settings

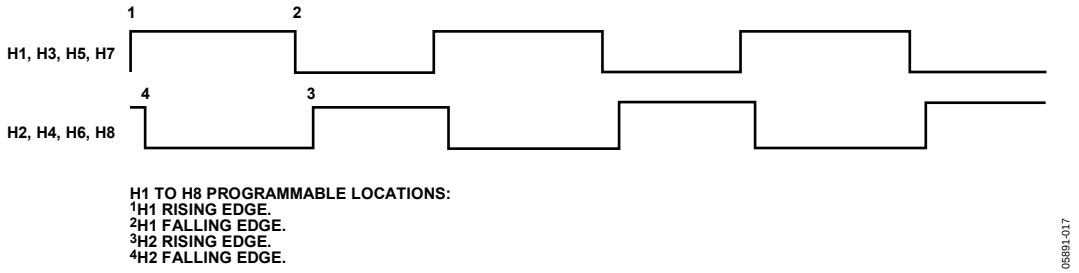


Figure 17. HCLK Mode 2 Operation

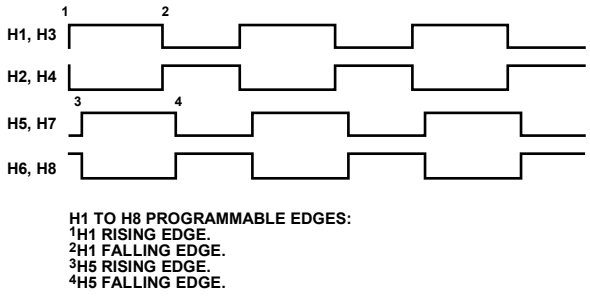


Figure 18. HCLK Mode 3 Operation

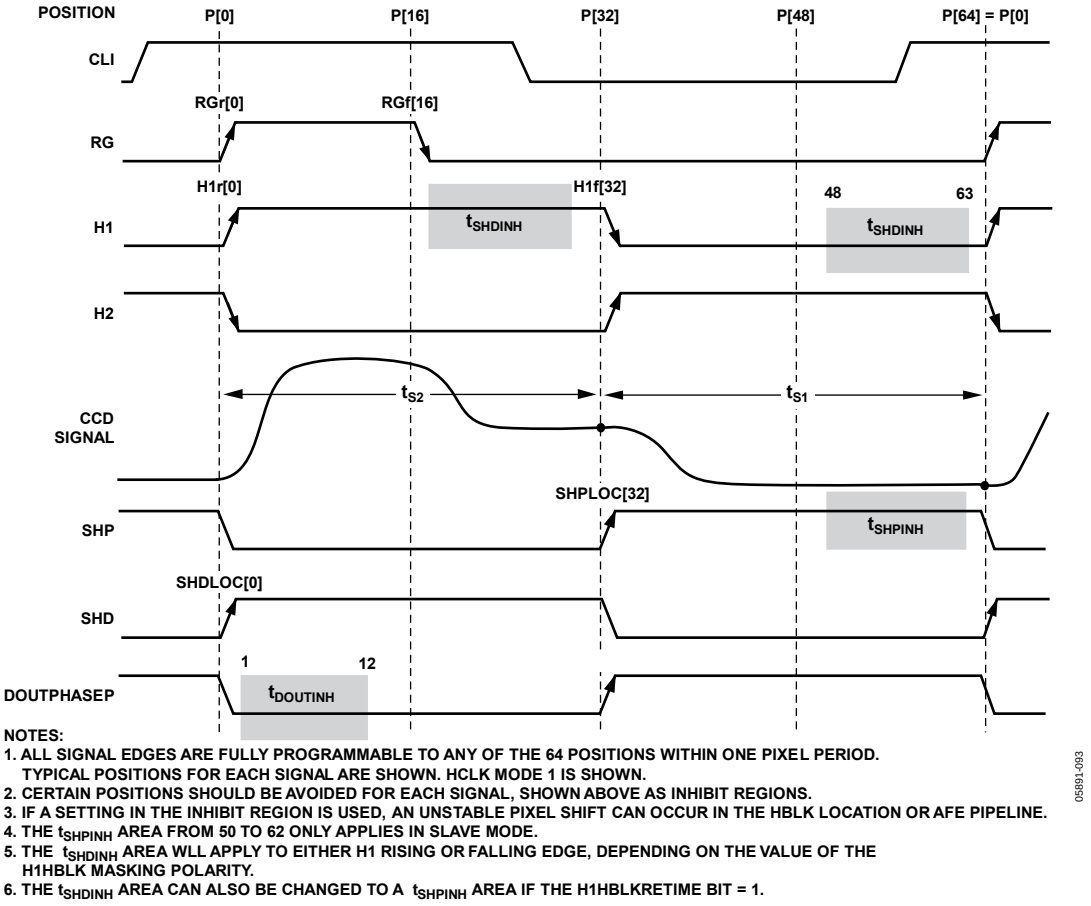


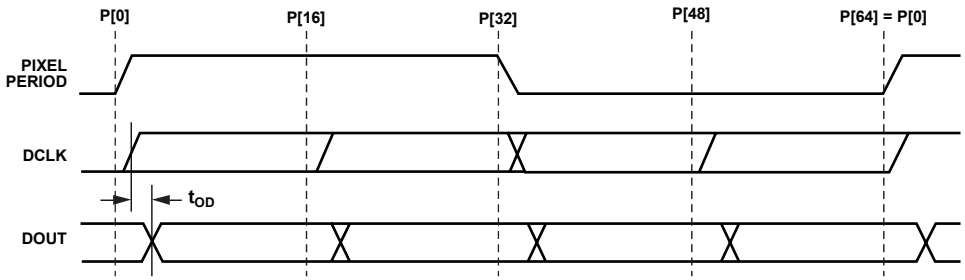
Figure 19. High Speed Timing Default Locations

Digital Data Outputs

The AD9992 data output and DCLK phase are programmable using the DOUTPHASE registers (Address 0x38, Bits [11:0]). DOUTPHASEP (Bits [5:0]) selects any edge location from 0 to 63, as shown in Figure 20. DOUTPHASEN (Bits [11:6]) does not actually program the phase of the data outputs but is used internally and should always be programmed to a value of DOUTPHASEP plus 32 edges. For example, if DOUTPHASEP is set to 0, DOUTPHASEN should be set to 32 (0x20).

Normally, the DOUT and DCLK signals track in phase, based on the contents of the DOUTPHASE registers. The DCLK output phase can also be held fixed with respect to the data outputs by changing the DCLKMODE register high (Address 0x38, Bit 12). In this mode, the DCLK output remains at a fixed phase equal to a delayed version of CLI while the data output phase is still programmable.

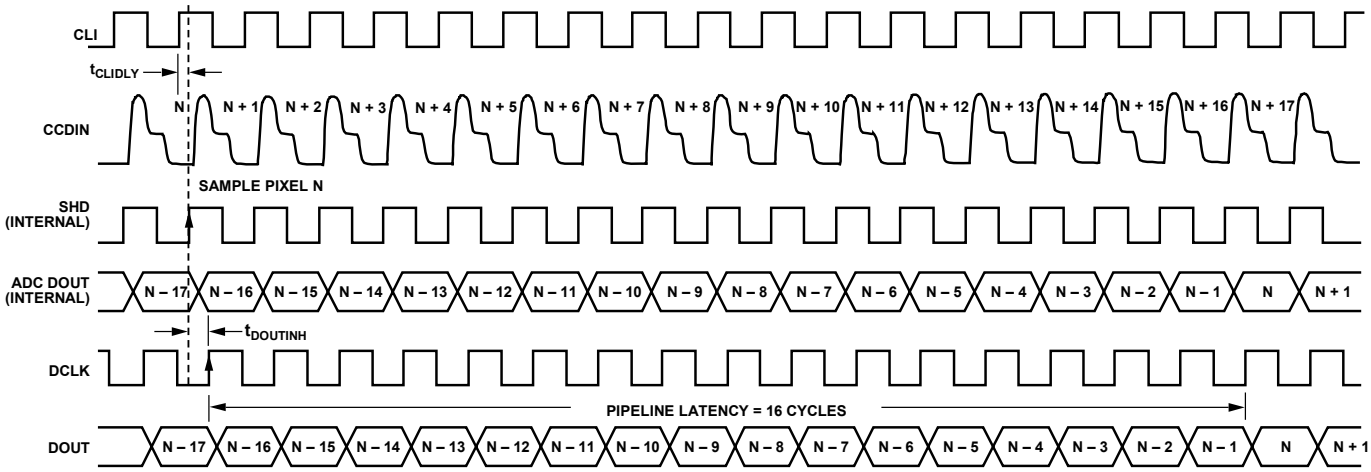
The pipeline delay through the AD9992 is shown in Figure 21. After the CCD input is sampled by SHD, there is a 16-cycle delay until the data is available.



NOTES
1. DATA OUTPUT (DOUT) AND DCLK PHASE ARE ADJUSTABLE WITH RESPECT TO THE PIXEL PERIOD.
2. WITHIN ONE CLOCK PERIOD, THE DATA TRANSITION CAN BE PROGRAMMED TO 64 DIFFERENT LOCATIONS.
3. DCLK CAN BE INVERTED WITH RESPECT TO DOUT BY USING THE DCLKINV REGISTER.

05891-020

Figure 20. Digital Output Phase Adjustment Using DOUTPHASEP Register



NOTES
1. TIMING VALUES SHOWN ARE SHDLOC = 0, WITH DCLKMODE = 0.
2. HIGHER VALUES OF SHD AND/OR DOUT PHASE SHIFTS DOUT TRANSITION TO THE RIGHT, WITH RESPECT TO CLI LOCATION.
3. RECOMMENDED VALUE FOR DOUT PHASE IS TO USE SHPLOC OR UP TO 15 EDGES FOLLOWING SHPLOC.

05891-021

Figure 21. Digital Data Output Pipeline Delay

HORIZONTAL CLAMPING AND BLANKING

The horizontal clamping and blanking pulses of the AD9992 are fully programmable to suit a variety of applications. Individual control is provided for CLPOB, PBLK, and HBLK in the different regions of each field. This allows the dark pixel clamping and blanking patterns to be changed at each stage of the readout to accommodate different image transfer timing and high speed line shifts.

Individual CLPOB and PBLK Patterns

The AFE horizontal timing consists of CLPOB and PBLK, as shown in Figure 22. These two signals are programmed independently using the registers listed in Table 10. The start polarity for the CLPOB (and PBLK) signal is CLPOBPOL (PBLKPOL), and the first and second toggle positions of the pulse are CLPOBTOG1 (PBLKTOG1) and CLPOBTOG2 (PBLKTOG2). Both signals are active low and should be programmed accordingly.

A separate pattern for CLPOB and PBLK can be programmed for each vertical sequence. As described in the Vertical Timing Generation section, several V-sequences can be created, each containing a unique pulse pattern for CLPOB and PBLK. Figure 48 shows how the sequence change positions divide the readout field into different regions. By assigning a different V-sequence to each region, the CLPOB and PBLK signals can change with each change in the vertical timing.

CLPOB and PBLK Masking Areas

Additionally, the AD9992 allows the CLPOB and PBLK signals to be disabled in certain lines in the field without changing any of the existing CLPOB pattern settings.

To use CLPOB (or PBLK) masking, the CLPMASKSTART (PBLKMASKSTART) and CLPMASKEND (PBLKMASKEND) registers are programmed to specify the start and end lines in the field where the CLPOB (PBLK) patterns are ignored. The three sets of start and end registers allow up to three CLPOB (PBLK) masking areas to be created.

The CLPOB and PBLK masking registers are not specific to a certain V-sequence; they are always active for any existing field of timing. During operation, to disable the CLPOB masking feature, these registers must be set to the maximum value of 0x1FFF or a value greater than the programmed VD length.

Note that to disable CLPOB (and PBLK) masking during power-up, it is recommended to set CLPMASKSTART (PBLKMASKSTART) to 8191 and CLPMASKEND (PBLKMASKEND) to 0. This prevents any accidental masking caused by register update events.

Table 10. CLPOB and PBLK Pattern Registers

Register	Length	Range	Description
CLPOBPOL	1b	High/low	Starting polarity of CLPOB for each V-sequence.
PBLKPOL	1b	High/low	Starting polarity of PBLK for each V-sequence.
CLPOBTOG1	13b	0 to 8191 pixel locations	First CLPOB toggle position within line for each V-sequence.
CLPOBTOG2	13b	0 to 8191 pixel locations	Second CLPOB toggle position within line for each V-sequence.
PBLKTOG1	13b	0 to 8191 pixel locations	First PBLK toggle position within line for each V-sequence.
PBLKTOG2	13b	0 to 8191 pixel locations	Second PBLK toggle position within line for each V-sequence.
CLPMASKSTART	13b	0 to 8191 line locations	CLPOB masking area—starting line within field (maximum of three areas).
CLPMASKEND	13b	0 to 8191 line locations	CLPOB masking area—ending line within field (maximum of three areas).
PBLKMASKSTART	13b	0 to 8191 line locations	PBLK masking area—starting line within field (maximum of three areas).
PBLKMASKEND	13b	0 to 8191 line locations	PBLK masking area—ending line within field (maximum of three areas).

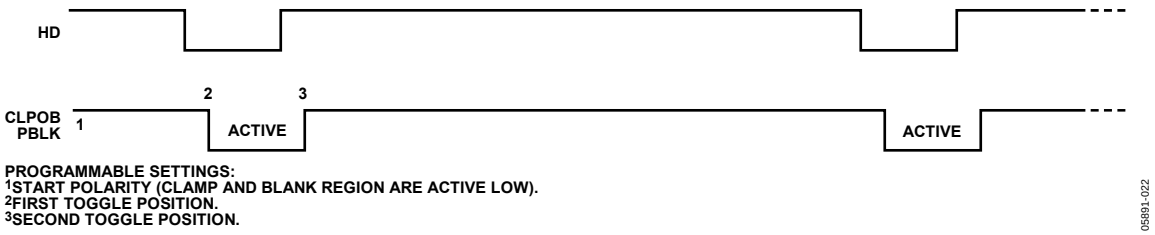


Figure 22. Clamp and Preblank Pulse Placement

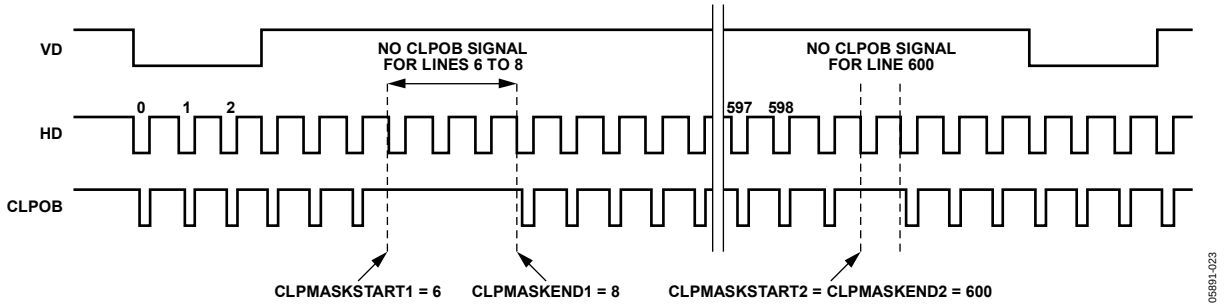


Figure 23. CLPOB Masking Example

Individual HBLK Patterns

The HBLK programmable timing shown in Figure 24 is similar to CLPOB and PBLK; however, there is no start polarity control. Only the toggle positions are used to designate the start and stop positions of the blanking period. Additionally, there are separate masking polarity controls for H1, H2, and HL that designate the polarity of the horizontal clock signals during the blanking period. Setting HBLKMASK_H1 high sets H1, and therefore H3, H5, and H7, low during the blanking, as shown in Figure 25. As with the CLPOB and PBLK signals, HBLK registers are available in each V-sequence, allowing different blanking signals to be used with different vertical timing sequences.

The AD9992 supports three modes of HBLK operation. HBLK Mode 0 supports basic operation and some support for special HBLK patterns. HBLK Mode 1 supports pixel mixing HBLK operation. HBLK Mode 2 supports advanced HBLK operation. The following sections describe each mode in detail. Register parameters are described in detail in Table 11.

HBLK Mode 0 Operation

There are six toggle positions available for HBLK. Normally, only two of the toggle positions are used to generate the standard HBLK interval. However, the additional toggle positions can be used to generate special HBLK patterns, as shown in Figure 26. The pattern in this example uses all six toggle positions to generate two extra groups of pulses during the HBLK interval. By changing the toggle positions, different patterns can be created.

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

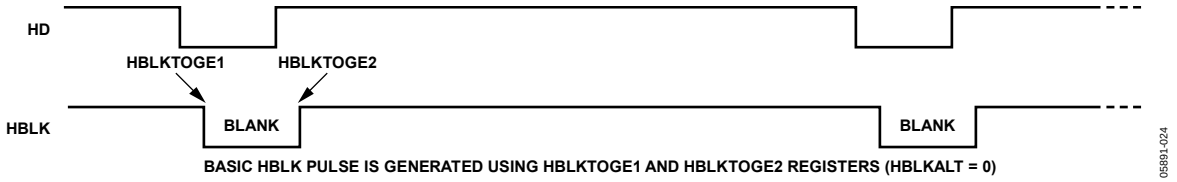


Figure 24. Typical Horizontal Blanking Pulse Placement (HBLKMODE = 0)

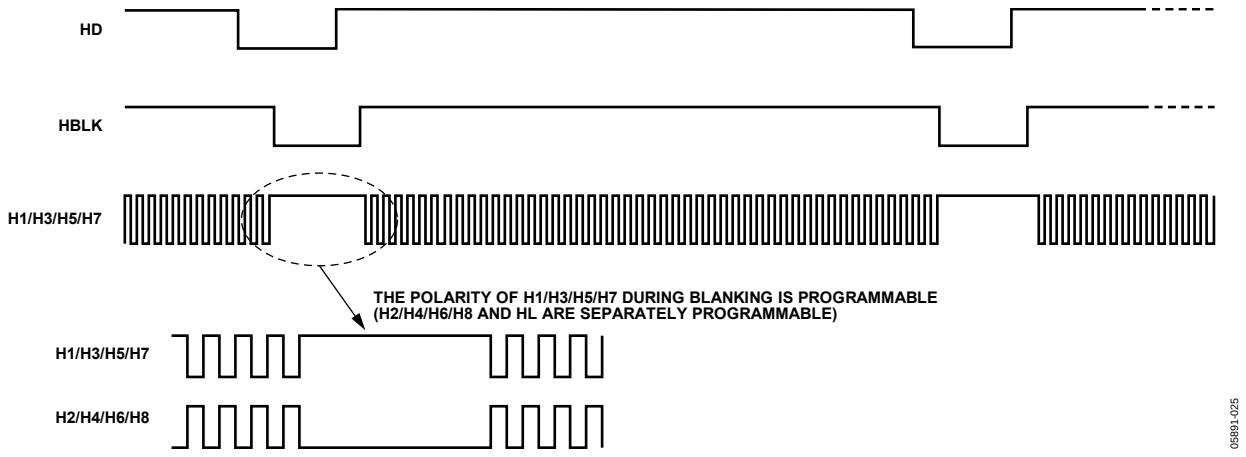


Figure 25. HBLK Masking Polarity Control

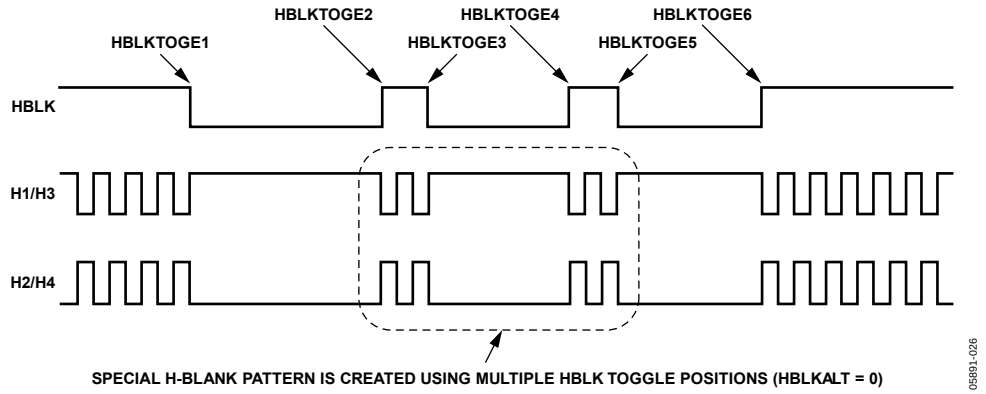


Figure 26. Using Multiple Toggle Positions for HBLK (HBLKMODE = 0)

Table 11. HBLK Pattern Registers

Register	Length	Range	Description
HBLKMODE	2b	0 to 2 HBLK modes	Enables different HBLK toggle position operation. 0: Normal mode. Six toggle positions available for even and odd lines. If even/odd alternation is not needed, set toggles for even/odd the same. 1: Pixel mixing mode. In addition to the six toggle positions, the HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP registers can be used to generate HBLK patterns. If even/odd alternation is not need, set toggles for even/odd the same. 2: Advanced HBLK mode. Divides HBLK interval into six repeat areas. Uses HBLKSTARTA/B/C and RA*H*REPA/B/C registers. 3: Test mode only. Do not access.
HBLKSTART	13b	0 to 8191 pixel location	Start location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKEND	13b	0 to 8191 pixel location	End location for HBLK in HBLK Mode 1 and HBLK Mode 2.
HBLKLEN	13b	0 to 8191 pixels	HBLK length in HBLK Mode 1 and HBLK Mode 2.
HBLKREP	13b	0 to 8191 repetitions	Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2.
HBLKMASK_H1	1b	High/low	Masking polarity for H1, H3, H5, H7 during HBLK.
HBLKMASK_H2	1b	High/low	Masking polarity for H2, H4, H6, H8 during HBLK.
HBLKMASK_HL	1b	High/low	Masking polarity for HL during HBLK.
HBLKTOGO1	13b	0 to 8191 pixel location	First HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO2	13b	0 to 8191 pixel location	Second HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO3	13b	0 to 8191 pixel location	Third HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO4	13b	0 to 8191 pixel location	Fourth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO5	13b	0 to 8191 pixel location	Fifth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGO6	13b	0 to 8191 pixel location	Sixth HBLK toggle position for odd lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE1	13b	0 to 8191 pixel location	First HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE2	13b	0 to 8191 pixel location	Second HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE3	13b	0 to 8191 pixel location	Third HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE4	13b	0 to 8191 pixel location	Fourth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE5	13b	0 to 8191 pixel location	Fifth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
HBLKTOGE6	13b	0 to 8191 pixel location	Sixth HBLK toggle position for even lines in HBLK Mode 0 and HBLK Mode 1.
RA0H1REPA/B/C	12b	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H1 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H1REPA. Number of H1 pulses following HBLKSTARTA. [7:4] RA0H1REPB. Number of H1 pulses following HBLKSTARTB. [11:8] RA0H1REPC. Number of H1 pulses following HBLKSTARTC.
RA1H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H1 repetitions for HBLKSTARTA/B/C.
RA2H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H1 repetitions for HBLKSTARTA/B/C.
RA3H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H1 repetitions for HBLKSTARTA/B/C.
RA4H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H1 repetitions for HBLKSTARTA/B/C.
RA5H1REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H1 repetitions for HBLKSTARTA/B/C.
RA0H2REPA/B/C	12b	0 to 15 HCLK pulses for each A, B, and C	HBLK Repeat Area 0. Number of H2 repetitions for HBLKSTARTA/B/C in HBLK Mode 2 for even lines; odd lines defined using HBLKALT_PAT. [3:0] RA0H2REPA. Number of H2 pulses following HBLKSTARTA. [7:4] RA0H2REPB. Number of H2 pulses following HBLKSTARTB. [11:8] RA0H2REPC. Number of H2 pulses following HBLKSTARTC.
RA1H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 1. Number of H2 repetitions for HBLKSTARTA/B/C.
RA2H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 2. Number of H2 repetitions for HBLKSTARTA/B/C.
RA3H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 3. Number of H2 repetitions for HBLKSTARTA/B/C.
RA4H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 4. Number of H2 repetitions for HBLKSTARTA/B/C.
RA5H2REPA/B/C	12b	0 to 15 HCLK pulses	HBLK Repeat Area 5. Number of H2 repetitions for HBLKSTARTA/B/C.
HBLKSTARTA	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position A for HBLK Mode 2. Set to 8191 if not used.
HBLKSTARTB	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position B for HBLK Mode 2. Set to 8191 if not used.
HBLKSTARTC	13b	0 to 8191 pixel location	HBLK Repeat Area Start Position C for HBLK Mode 2. Set to 8191 if not used.
HBLKALT_PAT1	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 0 pattern, selected from even field repeat areas previously defined.

Register	Length	Range	Description
HBLKALT_PAT2	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 1 pattern.
HBLKALT_PAT3	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 2 pattern.
HBLKALT_PAT4	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 3 pattern.
HBLKALT_PAT5	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 4 pattern.
HBLKALT_PAT6	3b	0 to 5 even repeat area	HBLK Mode 2, Odd Field Repeat Area 5 pattern.

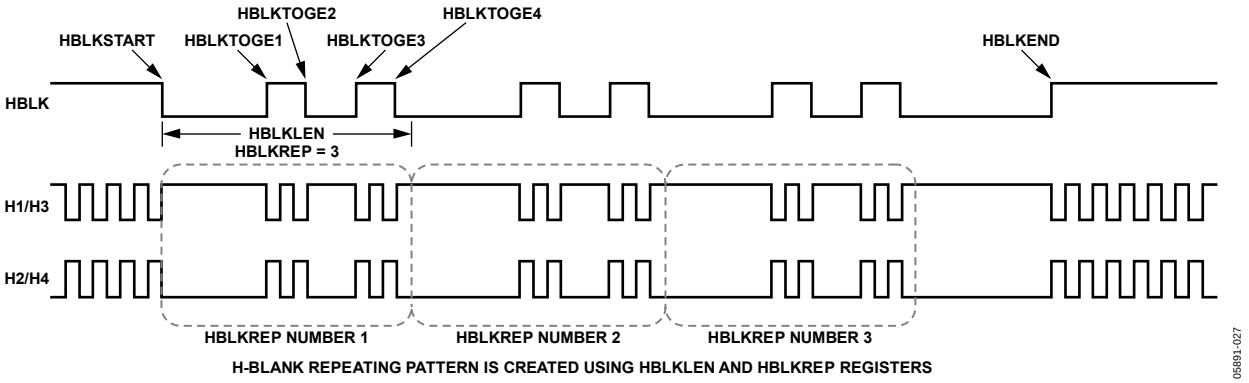


Figure 27. HBLK Repeating Pattern Using HBLKMODE = 1

HBLK Mode 1 Operation

Multiple repeats of the HBLK signal are enabled by setting HBLKMODE to 1. In this mode, the HBLK pattern can be generated using a different set of registers: HBLKSTART, HBLKEND, HBLKLEN, and HBLKREP, along with the six toggle positions (see Figure 27).

Separate toggle positions are available for even and odd lines. If alternation is not needed, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Generating HBLK Line Alternation

HBLK Mode 0 and HBLK Mode 1 provide the ability to alternate different HBLK toggle positions on even and odd lines. HBLK line alternation can be used in conjunction with V-pattern odd/even alternation or on its own. Separate toggle positions are available for even and odd lines. If even/odd line alternation is not required, the same values should be loaded into the registers for even (HBLKTOGE) and odd (HBLKTOGO) lines.

Increasing H-Clock Width During HBLK

HBLK Mode 0 and HBLK Mode 1 allow the H1 to H8 pulse widths to be increased during the HBLK interval. As shown in Figure 28, the H-clock frequency can be reduced by a factor of 1/2, 1/4, 1/6, 1/8, 1/10, 1/12, and so on, up to 1/30. To enable this feature, the HCLK_WIDTH register (Address 0x34, Bits [7:4]) is set to a value between 1 and 15. When this register is set to 0, the wide HCLK feature is disabled. The reduced frequency occurs only for H1 to H8 pulses that are located within the HBLK area.

The HCLK_WIDTH register is generally used in conjunction with special HBLK patterns to generate vertical and horizontal mixing in the CCD.

Note that the wide HCLK feature is available only in HBLK Mode 0 and HBLK Mode 1. HBLK Mode 2 does not support wide HCLKs.

Table 12. HCLK Width Register

Register	Length	Description
HCLK_WIDTH	4b	Controls H1 to H8 pulse widths during HBLK as a fraction of pixel rate 0: Same frequency as pixel rate 1: 1/2 pixel frequency, that is, doubles the HCLK pulse width 2: 1/4 pixel frequency 3: 1/6 pixel frequency 4: 1/8 pixel frequency 5: 1/10 pixel frequency … 15: 1/30 pixel frequency

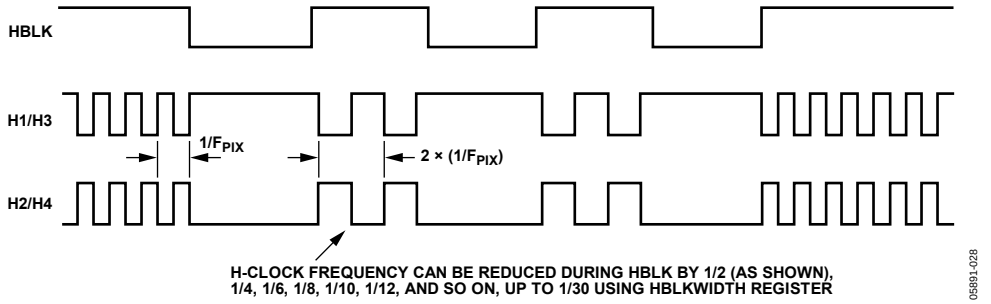


Figure 28. Generating Wide H-Clock Pulses During HBLK Interval

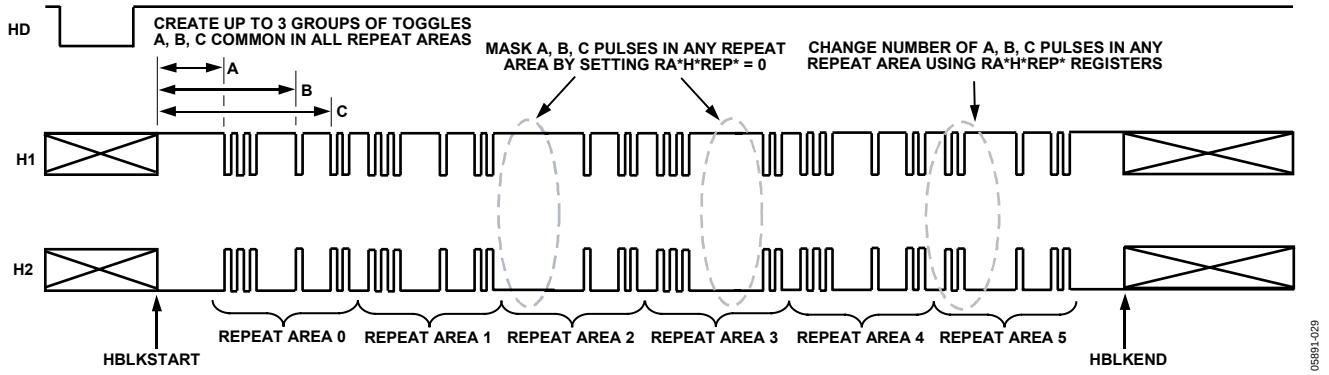


Figure 29. HBLK Mode 2 Operation

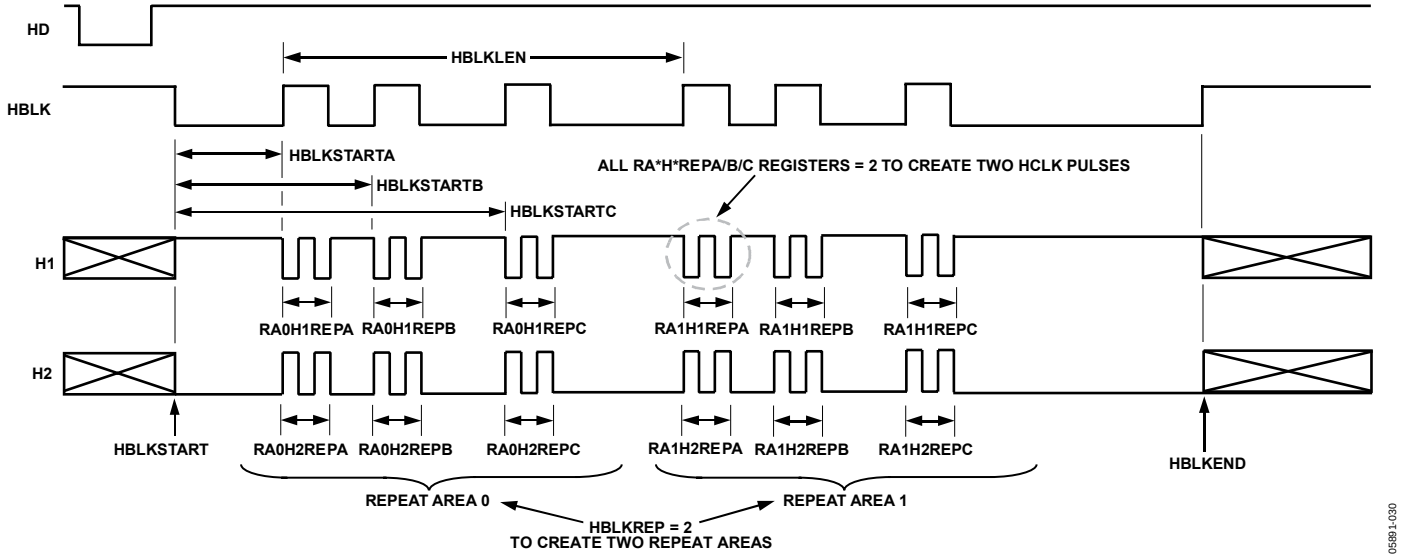


Figure 30. HBLK Mode 2 Registers

HBLK Mode 2 Operation

HBLK Mode 2 allows more advanced HBLK pattern operation. If multiple areas of HCLK pulses that are unevenly spaced apart from one another are needed, HBLK Mode 2 can be used. Using a separate set of registers, HBLK Mode 2 can divide the HBLK region into up to six repeat areas (see Table 11). As shown in Figure 30, each repeat area shares a common group of toggle positions, HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC. However, the number of toggles following each start position can be unique in each repeat area by using the RA*H1REP* and RA*H2REP* registers. As shown in Figure 29, setting the RA*H1REPA/RA*H1REPB/RA*H1REPC or RA*H2REPA/ RA*H2REPB/RA*H2REPC registers to 0 masks HCLK groups from appearing in a particular repeat area. Figure 30 shows only two repeat areas being used, although six are available. It is possible to program a separate number of repeat area repetitions for H1 and H2, but generally the same value is used for both H1 and H2. Figure 30 shows an example of RA0H1REPA/RA0H1REPB/ RA0H1REPC = RA0H2REPA/RA0H2REPB/RA0H2REPC = RA1H1REPA/RA1H1REPB/RA1H1REPC = RA1H2REPA/ RA1H2REPB/RA1H2REPC = 2.

Furthermore, HBLK Mode 2 allows a different HBLK pattern on even and odd lines. The HBLKSTARTA, HBLKSTARTB, and HBLKSTARTC registers, as well as the RA*H1REPA/RA*H1REPB /RA*H1REPC and RA*H2REPA/ RA*H2REPB/RA*H2REPC registers, define operation for the even lines. For separate control of the odd lines, the HBLKALT_PAT registers specify up to six repeat areas on the odd lines by reordering the repeat areas used for the even lines. New patterns are not available, but the order of the previously defined repeat areas on the even lines can be changed for the odd lines to accommodate advanced CCD operation.

HORIZONTAL TIMING SEQUENCE EXAMPLE

Figure 31 shows an example CCD layout. The horizontal register contains 28 dummy pixels, which occur on each line clocked from the CCD. In the vertical direction, there are 10 optical black (OB) lines at the front of the readout and two at the back of the readout. The horizontal direction has four OB pixels in the front and 48 in the back.

Figure 32 shows the basic sequence layout to be used during the effective pixel readout. The 48 OB pixels at the end of each line are used for the CLPOB signals. PBLK is optional and is often used to blank the digital outputs during the HBLK time. HBLK is used during the vertical shift interval.

Because PBLK is used to isolate the CDS input (see the Analog Preblanking section), the PBLK signal should not be used during CLPOB operation. The change in the offset behavior that occurs during PBLK impacts the accuracy of the CLPOB circuitry.

The HBLK, CLPOB, and PBLK parameters are programmed in the V-sequence registers. More elaborate clamping schemes, such as adding in a separate sequence to clamp in the entire shield OB lines, can be used. This requires configuring a separate V-sequence for clocking out the OB lines.

The CLPMASK registers are also useful for disabling the CLPOB on a few lines without affecting the setup of the clamping sequences. It is important that CLPOB be used only during valid OB pixels. During other portions on the frame timing, such as vertical blanking or SG line timing, the CCD does not output valid OB pixels. Any CLPOB pulse that occurs during this time causes errors in clamping operation and changes in the black level of the image.

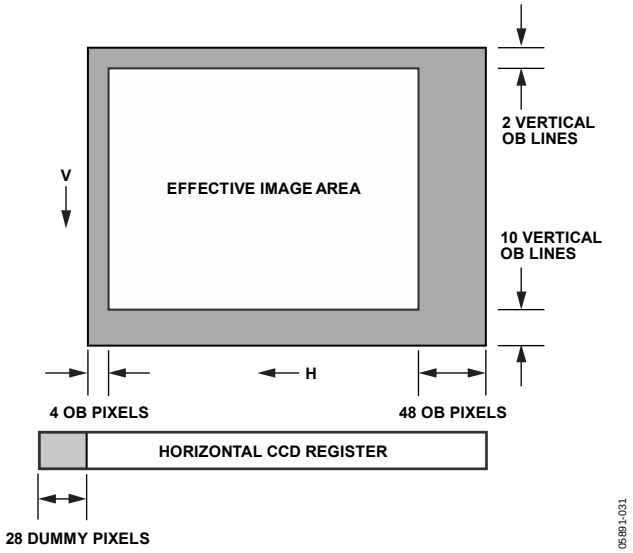


Figure 31. Example CCD Configuration

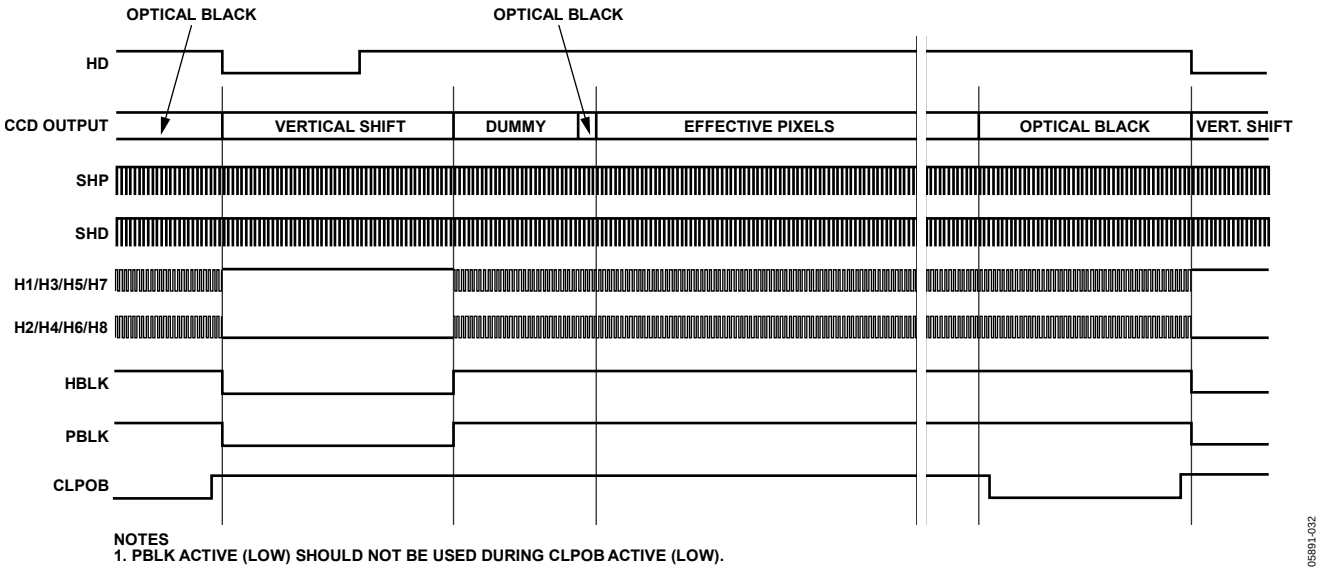


Figure 32. Horizontal Sequence Example

VERTICAL TIMING GENERATION

The AD9992 provides a flexible solution for generating vertical CCD timing and can support multiple CCDs and different system architectures. The vertical transfer clocks are used to shift each line of pixels into the horizontal output register of the CCD. The AD9992 allows these outputs to be individually programmed into various readout configurations by using a 4-step process.

Figure 33 shows an overview of how the vertical timing is generated in four steps.

1. The individual pulse patterns for XV1 to XV24 are created by using the vertical pattern group registers.
2. The V-pattern groups are used to build the sequences, which is when additional information is added.
3. The readout for an entire field is constructed by dividing the field into different regions and then assigning a sequence to each region.

   Each field can contain up to nine different regions to accommodate different steps of the readout, such as high speed line shifts and unique vertical line transfers. The total number of V-patterns, V-sequences, and fields is programmable but limited by the number of registers.
4. The MODE registers allow the different fields to be combined in any order for various readout configurations.

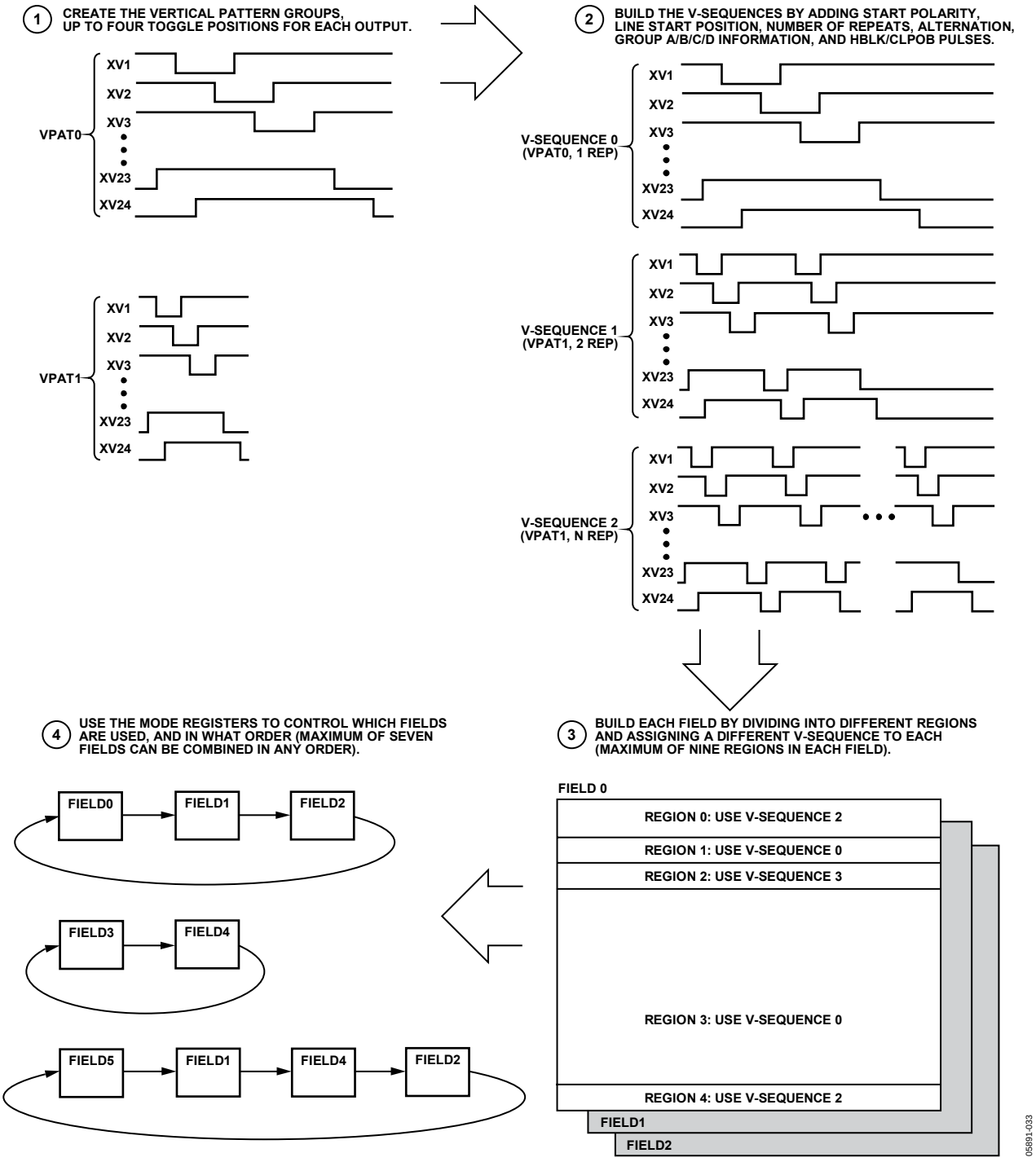


Figure 33. Summary of Vertical Timing Generation

Vertical Pattern Groups (VPAT)

The vertical pattern groups define the individual pulse patterns for each XV1 to XV24 output signal. Table 13 summarizes the registers available for generating each of the V-pattern groups. The first, second, third, and fourth toggle positions (XVTOG1, XVTOG2, XVTOG3, and XVTOG4) are the pixel locations within the line where the pulse transitions. All toggle positions are 13-bit values, allowing their placement anywhere in the horizontal line.

More registers are included in the vertical sequence registers to specify the output pulses. VPOL specifies the start polarity for each signal; VSTART specifies the start position of the V-pattern group within the line; VLEN designates the total length of the V-pattern group, which determines the number of pixels between each of the pattern repetitions when repetitions are used.

The VSTART position is actually an offset value for each toggle position. The actual pixel location for each toggle, measured from the HD falling edge (Pixel 0), is equal to the VSTART value plus the toggle position.

When the selected V-output is designated as a VSG pulse, either the XVTOG1/XVTOG2 or XVTOG3/XVTOG4 pair is selected using V-Sequence Address 0x02, VSGPATSEL. All four toggle positions are not simultaneously available for VSG pulses.

Unused V-channels must have their toggle positions programmed to either 0 or maximum value. This prevents unpredictable behavior because the default values of the V-pattern group registers are unknown.

Table 13. Vertical Pattern Group Registers

Register	Length	Description
XVTOG1	13b	First toggle position within line for each XV1 to XV24 output, relative to VSTART value.
XVTOG2	13b	Second toggle position, relative to VSTART value
XVTOG3	13b	Third toggle position, relative to VSTART value
XVTOG4	13b	Fourth toggle position, relative to VSTART value

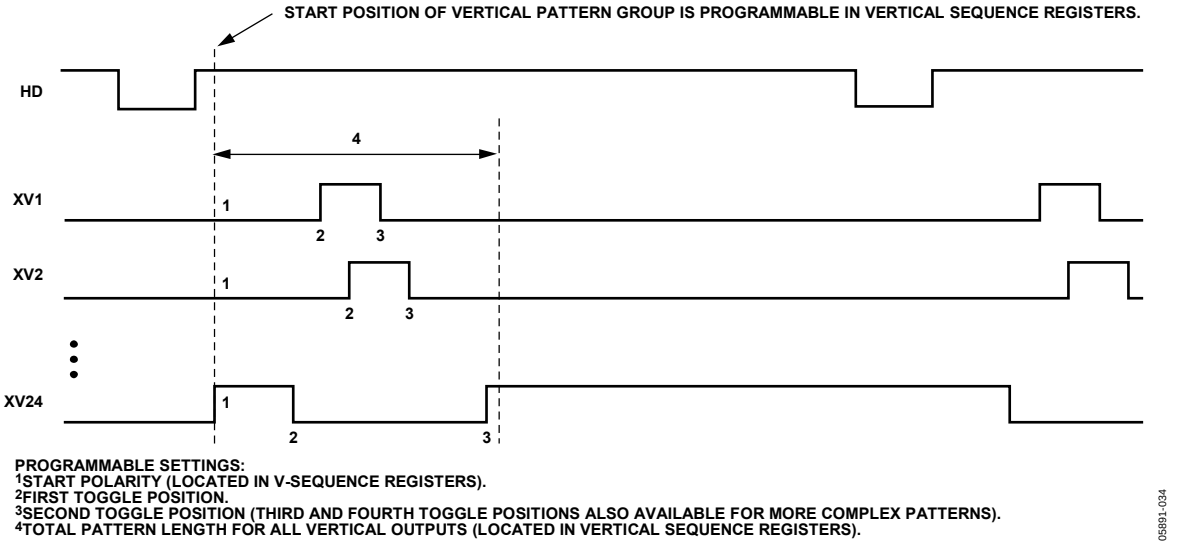


Figure 34. Vertical Pattern Group Programmability

VERTICAL SEQUENCES (VSEQ)

The vertical sequences are created by selecting one of the V-pattern groups and adding repeats, start position, horizontal clamping, and blanking information. The V-sequences are programmed using the registers shown in Table 14. Figure 35 shows how the different registers are used to generate each V-sequence.

The VPATSELA, VPATSELB, VPATSELC, and VPATSELD registers select which V-pattern is used in a given V-sequence. Having four groups available allows different vertical outputs to be mapped to different V-patterns. The selected V-pattern group can have repetitions added for high speed line shifts or for line binning by using the VREP registers for odd and even lines. Generally, the same number of repetitions is programmed into both registers. If a different number of repetitions is required on odd and even lines, separate values can be used for each register (see the Generating Line Alternation for V-Sequences and HBLK section). The VSTARTA and VSTARTB registers specify where in the line the V-pattern group starts. The VMASK_EN register is used with the FREEZE/RESUME registers to enable optional masking of the V-outputs. Either or both of the FREEZE1/RESUME1 and FREEZE2/RESUME2 registers can be enabled.

The line length (in pixels) is programmable using the HDLEN registers. Each V-sequence can have a different line length to accommodate various image readout techniques. The maximum number of pixels per line is 8192. The last line of the field is programmed separately using the HDLASTLEN register, which is located in the field register section.

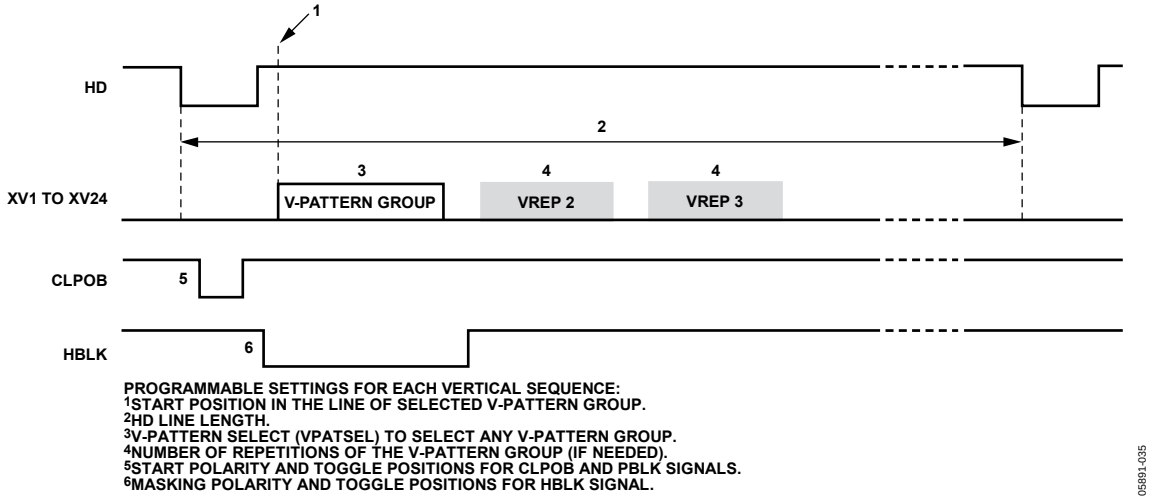


Figure 35. V-Sequence Programmability

Table 14. Summary of V-Sequence Registers (see Table 10 and Table 11 for the CLPOB, PBLK, and HBLK Pattern Registers)

Register	Length	Description
HOLD	4b	Use in conjunction with VMASK_EN. 1: HOLD function instead of FREEZE/RESUME function.
VMASK_EN	4b	Enables the masking of XV1 to XV24 outputs at the locations specified by the FREEZE/RESUME registers. 1: Enable masking for all groups. One bit for each set of Freeze and Resume Positions 1 to 4.
CONCAT_GRP	4b	Combines toggle positions of Groups A/B/C/D when enabled. Only Group A settings for start, polarity, length, and repetition are used when this mode is selected. 0: Disable. 1: Enable the addition of all toggle positions from VPATSELA/B/C/D. 2: Test mode only. Do not use. … 15: Test mode only. Do not use.
VREP_MODE	2b	Selects line alternation for V-output repetitions. Note separate controls for Group A and Groups B/C/D. 0: Disable alternation. Group A uses VREPA_1, Groups B/C/D use VREP _EVEN for all lines. 1: 2-line. Group A alternates VREPA_1 and VREPA_2. Groups B/C/D alternate VREP_EVEN and VREP_ODD. 2: 3-line. Group A alternates VREPA_1, VREPA_2, and VREPA_3. Groups B/C/D follow a VREP_EVEN, VREP_ODD, VREP_ODD, VREP_EVEN, VREP_ODD, VREP_ODD pattern. 3: 4-line. Group A alternates VREPA_1, VREPA_2, VREPA_3, VREPA_4. Groups B/C/D follow 2-line alternation.
LASTREPLEN_EN	4b	Enables a separate pattern length to be used during the last repetition of the V-sequence. One bit for each group (A, B, C, and D). Set bit high to enable. Group A is the LSB. Recommended value is enabled.
LASTTOG_EN	4b	Enables a final toggle position to be added at the end of the V-sequence. The toggle position is shared by all V-outputs in the same group. One bit for each group. Set bit high to enable. Group A is the LSB.
HDLENE	13b	HD line length for even lines in the V-sequence.
HDLENO	13b	HD line length for odd lines in the V-sequence.
VPOL_A	24b	Group A start polarity bits for each XV1 to XV24 output.
VPOL_B	24b	Group B start polarity bits for each XV1 to XV24 output.
VPOL_C	24b	Group C start polarity bits for each XV1 to XV24 output.
VPOL_D	24b	Group D start polarity bits for each XV1 to XV24 output.
GROUPSEL_0	24b	Assigns each XV1 to XV12 output to either Group A/B/C/D. Two bits for each signal. Bits [1:0] are for XV1, Bits [3:2] are for XV2 … Bits [23:22] are for XV12. 0: Assign to Group A 1: Assign to Group B 2: Assign to Group C 3: Assign to Group D
GROUPSEL_1	24b	Assigns each XV13 to XV24 output to either Group A/B/C/D. Two bits for each signal. Bits [1:0] are for XV13, Bits [3:2] are for XV14 … Bits [23:22] are for XV24. 0: Assign to Group A. 1: Assign to Group B. 2: Assign to Group C. 3: Assign to Group D.
VPATSELA	5b	Selected V-pattern for Group A.
VPATSELB	5b	Selected V-pattern for Group B.
VPATSELC	5b	Selected V-pattern for Group C.
VPATSELD	5b	Selected V-pattern for Group D.
VSTARTA	13b	Start position for the selected V-Pattern Group A.
VSTARTB	13b	Start position for the selected V-Pattern Group B.
VSTARTC	13b	Start position for the selected V-Pattern Group C.
VSTARTD	13b	Start position for the selected V-Pattern Group D.
VLENA	13b	Length of selected V-Pattern Group A.
VLENB	13b	Length of selected V-Pattern Group B.
VLENC	13b	Length of selected V-Pattern Group C.
VLEND	13b	Length of selected V-Pattern Group D.
VREPA_1	13b	Number of repetitions for the V-Pattern Group A for first lines (even).
VREPA_2	13b	Number of repetitions for the V-Pattern Group A for second lines (odd).

Register	Length	Description
VREPA_3	13b	Number of repetitions for the V-Pattern Group A for third lines.
VREPA_4	13b	Number of repetitions for the V-Pattern Group A for fourth lines.
VREPB_ODD	13b	Number of repetitions for the V-Pattern Group B for odd lines.
VREPC_ODD	13b	Number of repetitions for the V-Pattern Group C for odd lines.
VREPD_ODD	13b	Number of repetitions for the V-Pattern Group D for odd lines.
VREPB_EVEN	13b	Number of repetitions for the V-Pattern Group B for even lines.
VREPC_EVEN	13b	Number of repetitions for the V-Pattern Group C for even lines.
VREPD_EVEN	13b	Number of repetitions for the V-Pattern Group D for even lines.
FREEZE1	13b	Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL0_EVEN [12:0] register when special VSEQALT_EN mode is enabled.
FREEZE2	13b	Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL1_EVEN [12:0] register when special VSEQALT_EN mode is enabled.
FREEZE3	13b	Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL0_ODD [12:0] register when special VSEQALT_EN mode is enabled.
FREEZE4	13b	Pixel location where the V-outputs freeze or hold (see VMASK_EN). Also used as VALTSEL1_ODD [12:0] register when special VSEQALT_EN mode is enabled.
RESUME1	13b	Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL0_EVEN [17:13] register when S within line for each XV1 to XV24 output when special VSEQALT_EN mode is enabled.
RESUME2	13b	Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL1_EVEN [17:13] register when special VSEQALT_EN mode is enabled.
RESUME3	13b	Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL0_ODD [17:13] register when special VSEQALT_EN mode is enabled.
RESUME4	13b	Pixel location where the V-outputs resume operation (see VMASK_EN). Also used as VALTSEL1_ODD [17:13] register when special VSEQALT_EN mode is enabled.
LASTREPLEN_A	13b	Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENA register.
LASTREPLEN_B	13b	Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENB register.
LASTREPLEN_C	13b	Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLENC register.
LASTREPLEN_D	13b	Separate length for last repetition of vertical pulses. Must be enabled using LASTREPLEN_EN. Should be programmed to a value equal to the VLEND register.
LASTTOG_A	13b	Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals.
LASTTOG_B	13b	Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals.
LASTTOG_C	13b	Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals.
LASTTOG_D	13b	Optional fifth toggle position for the vertical signals. Must be enabled using LASTTOG_EN. Note that the toggle position is common for all vertical signals.
VSEQALT_EN	1b	Special V-sequence alternation mode is enabled when this register is programmed high.
VALT_MAP	1b	Enables the use of FREEZE/RESUME register locations to specify the VALTSEL0 and VALTSEL1 registers. Must be enabled if VSEQALT mode is enabled.
VALTSEL0_EVEN	18b	Select lines for special V-sequence alternation mode for even lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments.
VALTSEL1_EVEN	18b	Select lines for special V-sequence alternation mode for even lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments.
VALTSEL0_ODD	18b	Select lines for special V-sequence alternation mode for odd lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments.
VALTSEL1_ODD	18b	Select lines for special V-sequence alternation mode for odd lines. Used to concatenate VPAT Groups A/B/C/D into unique merged patterns. Setting is used to specify one segment, with up to a maximum of 18 segments.
SPC_PAT_EN	1b	Enable special V-pattern to be inserted into one repetition of a VPATA series. SPC_PAT_EN [0]: Set to 1 to enable VPATB to be used as special pattern insertion. SPC_PAT_EN [1]: Set to 1 to enable VPATC to be used as special pattern insertion. SPC_PAT_EN [2]: Set to 1 to enable VPATD to be used as special pattern insertion.

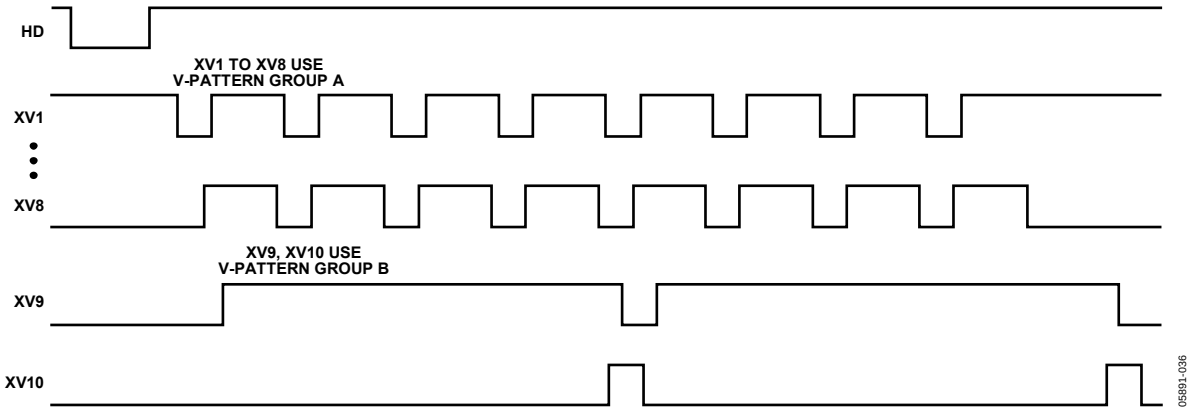


Figure 36. Using Separate Group A and Group B V-Patterns

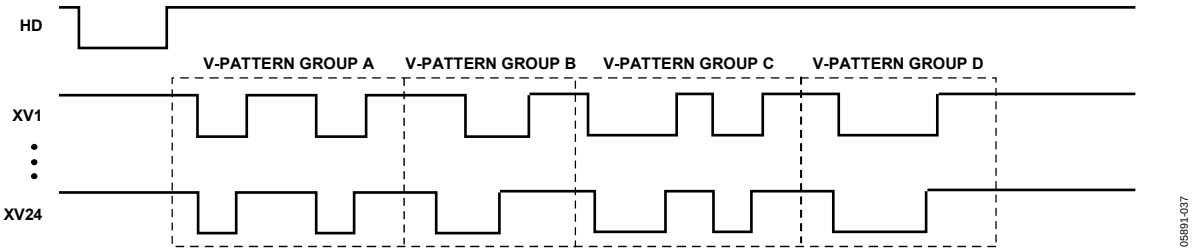


Figure 37. Combining Multiple V-Patterns Using CONCAT_GRP = 1

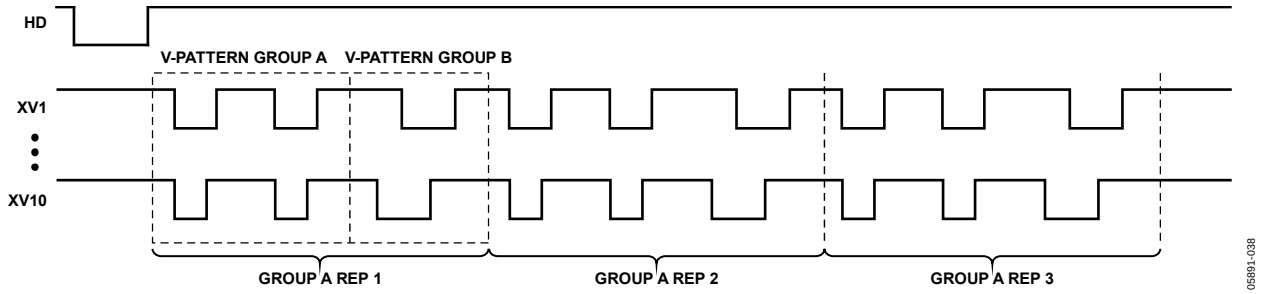


Figure 38. Combining Group A and Group B V-Patterns with Repetition

Group A/Group B/Group C/Group D Selection

The AD9992 has the flexibility to use four different V-pattern groups in a vertical sequence. In general, the vertical outputs use the same V-pattern group during a particular sequence. It is possible to assign some of the outputs to a different V-pattern group, which can be useful in certain CCD readout modes.

The GROUPSEL registers are used to select Group A, Group B, Group C, or Group D for each V-output. In general, only a single V-pattern group is needed for the vertical outputs; therefore, Group A should be selected for all outputs by default (GROUPSEL_0, GROUPSEL_1 = 0x00). In this configuration, all outputs use the V-pattern group specified by the VPATSELA register.

If additional flexibility is needed, some outputs can be set to Group B, Group C, or Group D in the GROUPSEL registers. In this case, those selected outputs use the V-pattern group specified by the VPATSELB, VPATSELC, or VPATSELD registers. Figure 36 shows an example where outputs XV9 and XV10 are using a separate V-Pattern Group B to perform special CCD timing.

Another application of the Group A, Group B, Group C, and Group D registers is to combine up to four different V-pattern groups together for more complex patterns. This is accomplished by setting the CONCAT_GRP register (Address 0x00, Bits [13:10]) equal to 0x01. This setting combines the toggle positions from the V-pattern groups specified by the VPATSELA, VPATSELB, VPATSELC, and VPATSELD registers for a maximum of up to 16 toggle positions. Example timing for the CONCAT_GRP = 1 feature is shown in Figure 37.

If only two groups are needed (up to eight toggle positions) for the specified timing, the VPATSELB, VPATSELC, and VPATSELD registers can be programmed to the same value. If only three groups are needed, VPATSELC and VPATSELD can be programmed to the same value. Following this approach

conserves register memory if the four separate V-patterns are not needed.

Note that when CONCAT_GRP is enabled, Group A settings are used only for start position, polarity, length, and repetitions. All toggle positions for Group A, Group B, Group C, and Group D are combined together and applied using the settings in the VSTARTA, VPOL_A, VLENA, and VREPA registers.

Special Vertical Sequence Alternation (SVSA) Mode

The AD9992 has additional flexibility for combining four different V-pattern groups in a random sequence that can be programmed for specific CCD requirements. This mode of operation allows custom vertical sequences for CCDs that require more complex vertical timing patterns. For example, using the special vertical sequence alternation mode, it is possible to support random pattern concatenation, with additional support for odd/even line alternation.

Figure 39 illustrates four common and repetitive vertical pattern segments, A through D, that are derived from the complete vertical pattern. Figure 40 illustrates how each group can be concatenated in an arbitrary order.

To enable the SVSA mode, write the VSEQALT_EN bit, Address 0x20 Bit 13, equal to 0x01. The location of the VALTSEL registers is shared with the VPAT registers for XV24. When SVSA mode is enabled, the VALTSEL register function is selected.

To create SVSA timing, divide the complete vertical timing pattern into four common and repetitive segments. Identify the related segments as VPATA, VPATB, VPATC, or VPATD. Up to four toggle positions for each segment can be programmed using the V-pattern registers.

Table 15 shows how the segments are specified using a 2-bit representation. Each bit from VALTSEL0 and VALTSEL1 is combined to produce four values, corresponding to Pattern A, Pattern B, Pattern C, and Pattern D.

Table 15. VALTSEL Bit Settings for Even and Odd Lines

Parameter	VALTSEL Bit Settings			
VALTSEL0_EVEN	0	0	1	1
VALTSEL1_EVEN	0	1	0	1
VALTSEL0_ODD	0	0	1	1
VALTSEL1_ODD	0	1	0	1
Resulting pattern for even lines	A	B	C	D
Resulting pattern for odd lines	A	B	C	D

When the entire pattern is divided, program VALTSEL0 (even and odd) [17:0] and VALTSEL1 (even and odd) [17:0] so that the segments are concatenated in the desired order. If separate odd and even lines are not required, set the odd and even registers to the same value. Figure 41 illustrates the process of using six vertical pattern segments that have been concatenated into a small, merged pattern.

Program the register VREPA_1 to specify the number of segments to concatenate into each merged pattern. The maximum number of segments that can be concatenated to create a merged pattern is 18. Program VLENA, VLENB, VLENC, VLEND to be of equal length. Finally, program HBLK to generate the proper H-clock timing using the procedure for HBLK Mode 2 described in the HBLK Mode 2 Operation section.

It is important to note that because the FREEZE/RESUME registers are used to specify the VALTSEL registers, the VALT_MAP register must be enabled when using the special VALT mode.

Table 16. VALTSEL Register Locations[1]

Register Function When VSEQALT_EN = 1	Register Location
VALTSEL0_EVEN [12:0]	VSEQ register FREEZE1 [12:0]
VALTSEL0_EVEN [17:13]	VSEQ register RESUME1 [17:13]
VALTSEL1_EVEN [12:0]	VSEQ register FREEZE2 [12:0]
VALTSEL1_EVEN [17:13]	VSEQ register RESUME2 [17:13]
VALTSEL0_ODD [12:0]	VSEQ register FREEZE3 [12:0]
VALTSEL0_ODD [17:13]	VSEQ register RESUME3 [17:13]
VALTSEL1_ODD [12:0]	VSEQ register FREEZE4 [12:0]
VALTSEL1_ODD [17:13]	VSEQ register RESUME4 [17:13]

[1] The VALT_MAP register must be set to 1 to enable the use of VALTSEL registers.

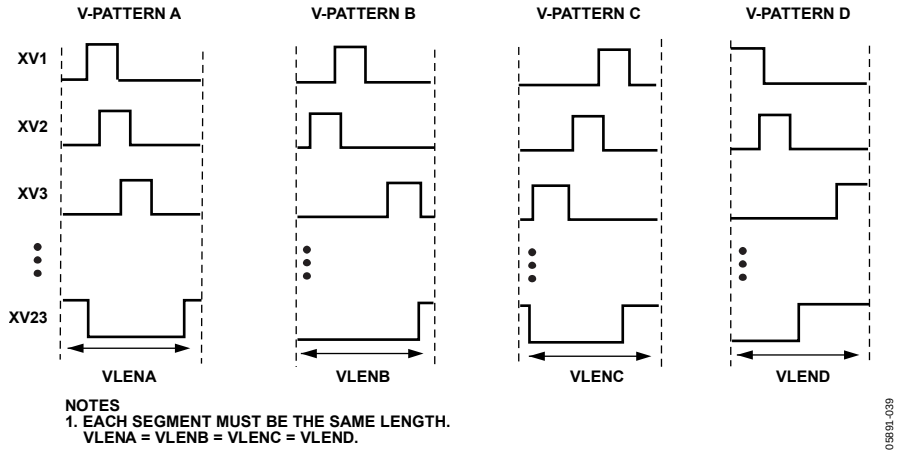


Figure 39. Vertical Timing Divided Into Four Segments: VPATA, VPATB, VPATC, and VPATD

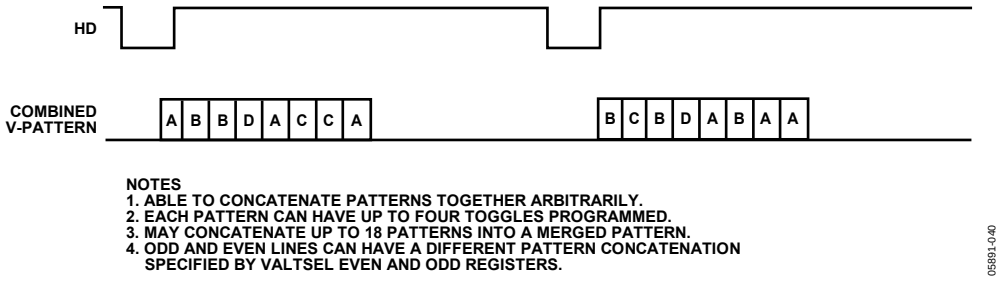


Figure 40. Concatenating Each VPAT Group in Arbitrary Order

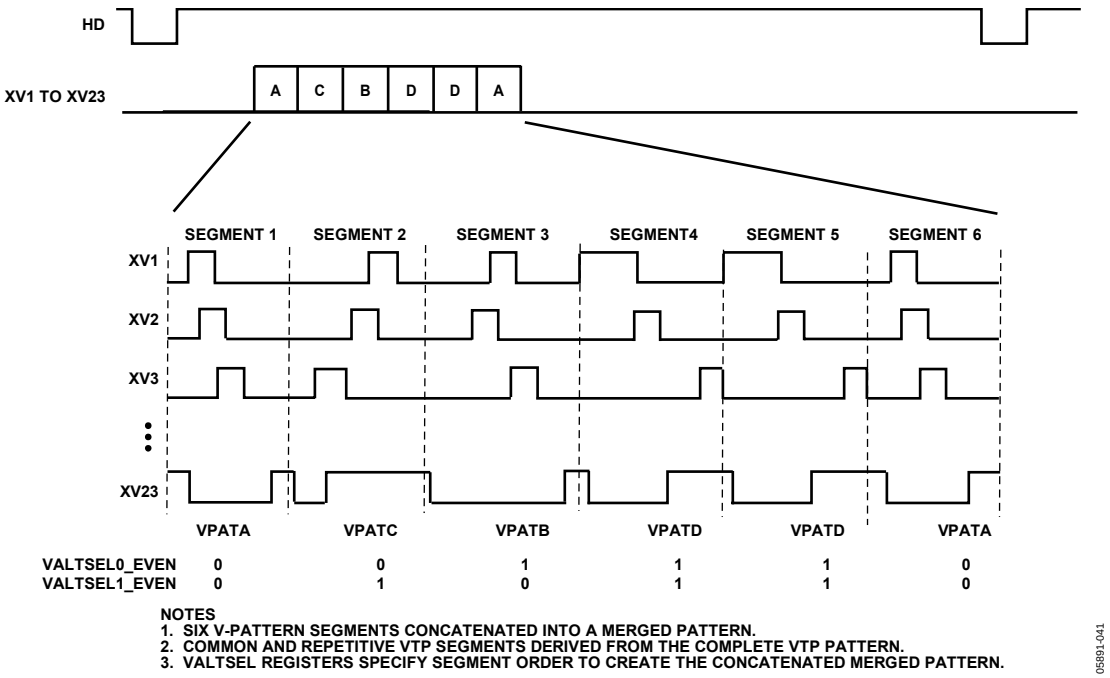


Figure 41. Special V-Sequence Alternation Mode Using VALTSEL Registers to Specify Segment Order

Using the LASTREPLEN_EN

The LASTREPLEN_EN register (Address 0x00, Bits [19:16] in the sequence registers) is used to enable a separate pattern length to be used in the final repetition of several pulse repetitions. It is recommended that the LASTREPLEN_EN register bits be set high (enabled) and the LASTREPLEN_A, LASTREPLEN_B, LASTREPLEN_C, and LASTREPLEN_D registers be set to a value equal to the VLENA, VLENB, VLENC, and VLEND register values, respectively.

Generating Line Alternation for V-Sequences and HBLK

During low resolution readout, some CCDs require a different number of vertical clocks on alternate lines. The AD9992 can support this by using the VREP registers. This allows a different number of V-pattern group repetitions to be programmed on odd and even lines. Only the number of repeats can be different in odd and even lines, while the V-pattern group remains the same. There are separate controls for the assigned Group A, Group B, Group C, and Group D patterns. All groups can support odd and even line alternation. Group A uses the VREPA_1 register and the VREPA_2 register; Group B, Group C, and Group D use the corresponding VREP_ODD register and VREP_EVEN register. With the additional VREPA_3 register and VREPA_4 register, Group A can also support 3-line and 4-line alternation.

As discussed in the Generating HBLK Line Alternation section, the HBLK signal can be alternated for odd and even lines. Figure 42 shows an example of V-pattern group repetition alternation and HBLK Mode 0 alternation used together.

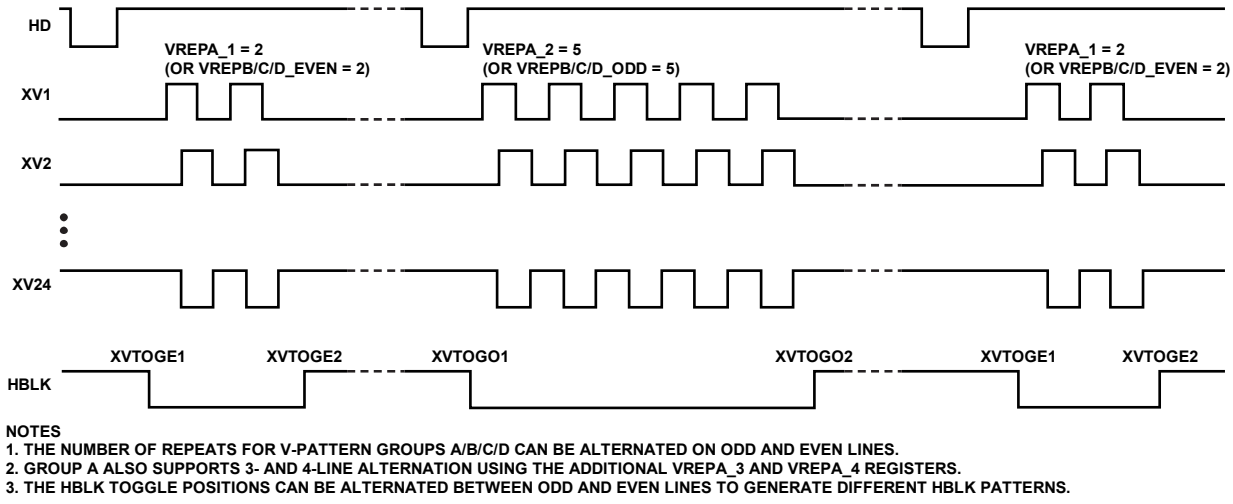


Figure 42. Odd/Even Line Alternation of V-Pattern Group Repetitions and HBLK Toggle Positions

Vertical Masking Using FREEZE/RESUME Registers

As shown in Figure 43 and Figure 44, the FREEZE/RESUME registers are used to temporarily mask the V-outputs. The pixel locations to begin the masking (FREEZE) and end the masking (RESUME) create an area in which the vertical toggle positions are ignored. At the pixel location specified in the FREEZE register, the V-outputs are held static at their current dc state, high or low. The V-outputs are held until the pixel location that is specified by the RESUME register is reached, at which point the signals continue with any remaining toggle positions, if any exist.

Four sets of FREEZE/RESUME registers are provided, allowing the vertical outputs to be interrupted up to four times in the same line. The FREEZE and RESUME Position 1 to Position 4 are enabled independently and applied to all groups (Group A, Group B, Group C, and Group D) using the VMASK_EN register.

Note that when masking is enabled, Group A, Group B, Group C, and Group D use the same FREEZE/RESUME positions.

Note that the FREEZE/RESUME registers are also used as the VALTSEL0 and VALTSEL1 registers during special vertical alternation mode.

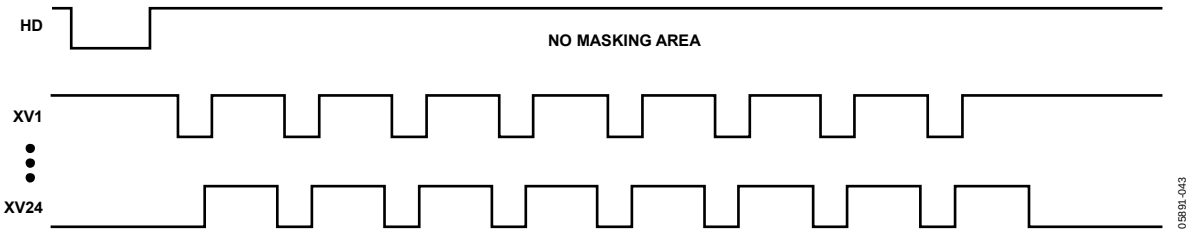


Figure 43. No FREEZE/RESUME

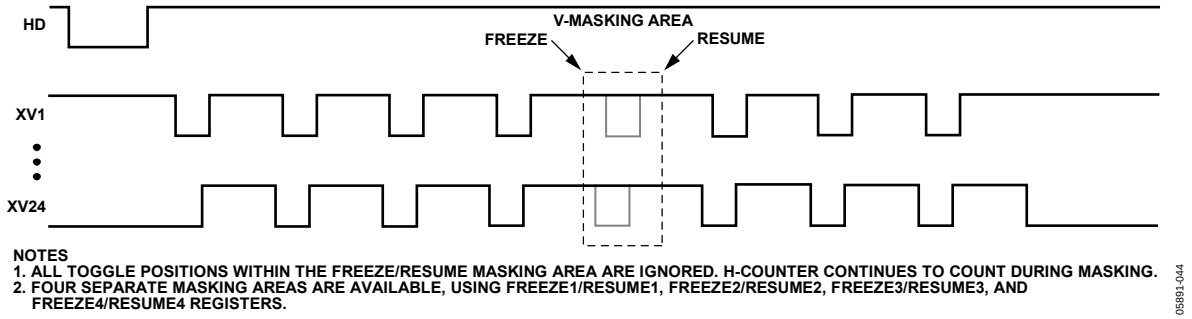


Figure 44. Using FREEZE/RESUME

Hold Area Using FREEZE/RESUME Registers

The FREEZE/RESUME registers can also be used to create a hold area in which the V-outputs are temporarily held and later continued, starting at the point where they were held. As shown in Figure 45, this is different from the VMASK_EN register because the V-outputs continue from where they stopped rather than from where they would have been. The hold area temporarily stops the pixel counter for the V-outputs, while the V-masking allows the counter to continue in the masking area.

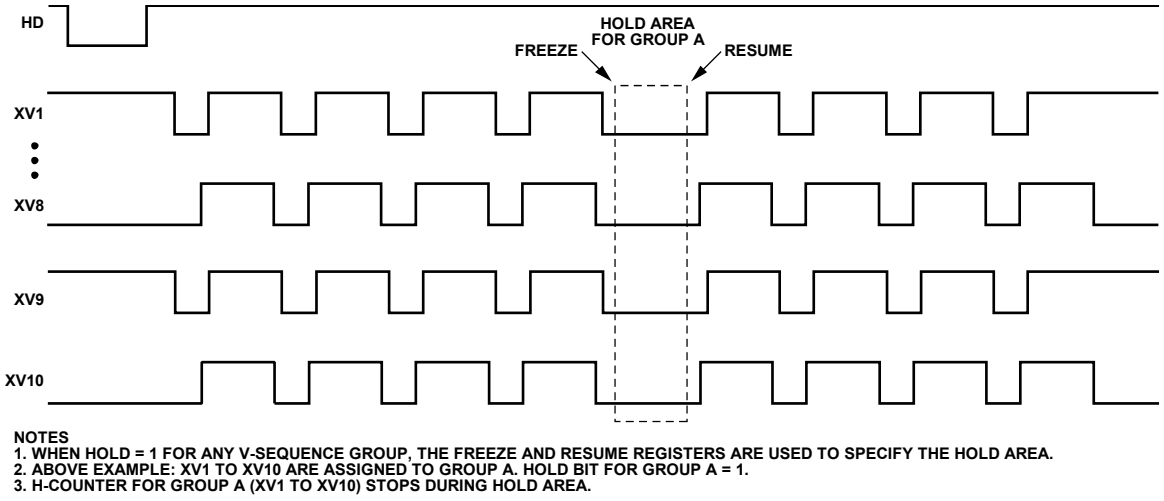


Figure 45. Hold Area for Group A

Special Pattern Insertion

Additional flexibility is available using the SPC_PAT_EN registers, which allows a Group B, Group C, or Group D pattern to be inserted into a series of Group A repetitions. This feature is useful when a different pattern is needed at the start, end, or middle of a sequence.

Figure 46 shows an example of a sweep region using VPATA with multiple repetitions where a single repetition of VPATB has been added into the middle of the sequence. Figure 47 shows more detail on how to set the registers to achieve the desired timing.

Note that VREPB is used to specify which repetition number has the special pattern inserted instead of VPATA. VPATB always has priority over VPATC or VPATD if more than one SPC_PAT_EN bit is enabled (SPC_PAT_EN [0] has priority).

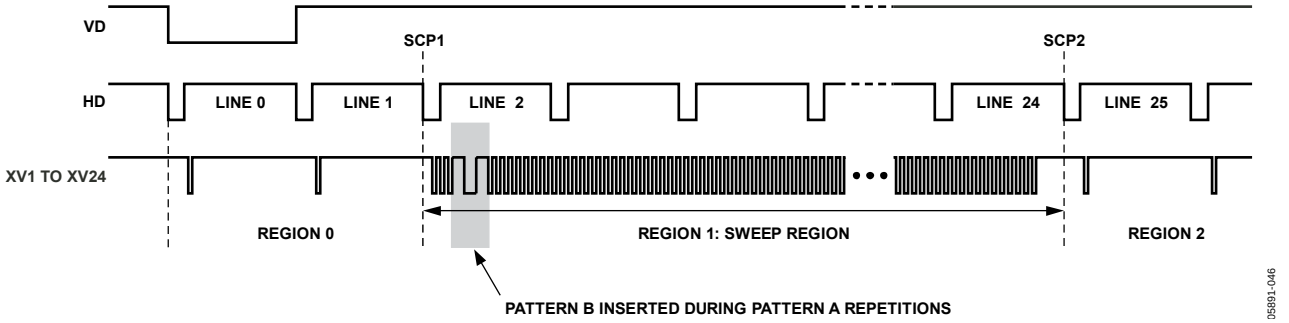


Figure 46. Example of Special Pattern Insertion

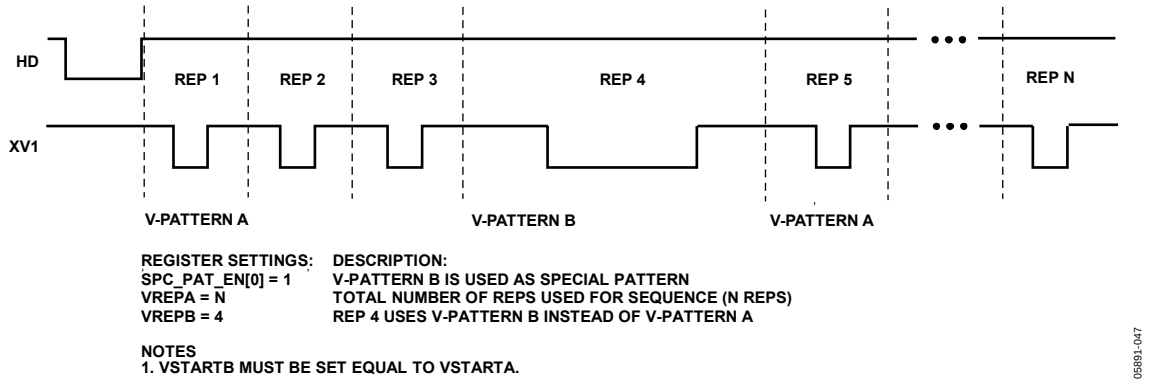


Figure 47. Example of Special Pattern Insertion, Detail

Complete Field: Combining V-Sequences

After the V-sequences are created, they are combined to create different readout fields. A field consists of up to nine regions, and within each region, a different V-sequence can be selected. Figure 48 shows how the sequence change positions (SCP) designate the line boundary for each region and how the SEQ registers then select which V-sequence is used in each region. Registers to control the VSG outputs are also included in the field registers. Table 17 summarizes the registers used to create the fields.

The SEQ registers, one for each region, select which V-sequences are active in each region. The MULT_SWEEP registers, one for each region, are used to enable sweep mode and/or multiplier mode in any region. The SCP registers create the line boundaries for each region. The VDLEN register specifies the total number of lines in the field. The HDLEN register specifies the total number of pixels per line, and the HDLASTLEN register specifies the number of pixels in the last line of the field.

The VPATSECOND register is used to add a second V-pattern group to the XV1 to XV10 outputs in the vertical sensor gate (VSG) line. The SGMASK register is used to enable or disable each individual VSG output. There are two bits for each VSG output to enable separate masking in SGACTLINE1 and SGACTLINE2.

Setting a masking bit high masks the output; setting it low enables the output. The VSGPATSEL register assigns one of the eight SG patterns to each VSG output. Individual SG patterns are created separately using the SG pattern registers. The SGACTLINE1 register specifies which line in the field contains the VSG outputs. The optional SGACTLINE2 register allows the same VSG pulses to be repeated on a different line. Separate masking is not available for SGACTLINE1 and SGACTLINE2.

Table 17. Field Registers (CLPOB, PBLK Masking Shown in Table 10)

Register	Length	Range	Description
SEQx	5b	0 to 31 V-sequence number	Selected V-sequence for each region in the field.
MULT_SWEEP	2b	0 to 3	Enables multiplier mode and/or sweep mode for each region. 0: Multiplier off, sweep off. 1: Multiplier off, sweep on. 2: Multiplier on, sweep off. 3: Multiplier on, sweep on.
SCP	13b	0 to 8191 line number	Sequence change position for each region.
VDLEN	13b	0 to 8191 lines	Total number of lines in each field.
HDLASTLEN	13b	0 to 8191 pixels	Length in pixels of the last HD line in each field.
VSGPATSEL	24b	High/low	VSGPATSEL selects which V-pattern toggle positions are used. When set to 0, Toggle 1 and Toggle 2 are used. When set to 1, Toggle 3 and Toggle 4 are used. [0]: XV1 selection (0 = use XVTOG1, XVTOG2; 1 = use XVTOG3, XVTOG4). … [23]: XV24 selection.
SGMASK	24b	High/low, each VSG	Set high to mask each individual VSG output. [0]: XV1 mask. … [23]: XV24 mask.
SGACTLINE1	13b	0 to 8191 line number	Selects the line in the field where the VSG signals are active.
SGACTLINE2	13b	0 to 8191 line number	Selects a second line in the field to repeat the VSG signals. If not used, set this equal to SGACTLINE1 or to the maximum value.

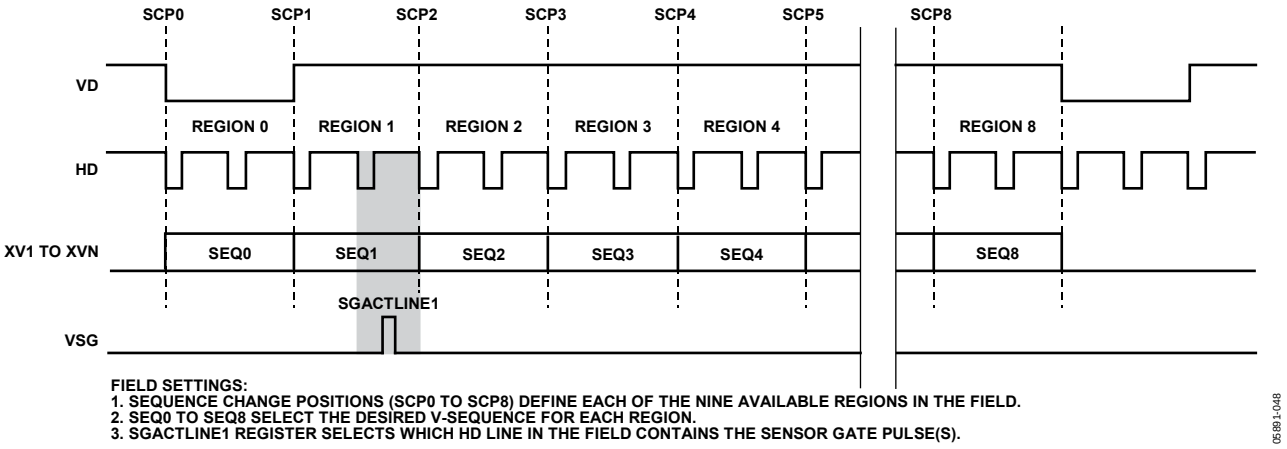


Figure 48. Complete Field Divided into Regions

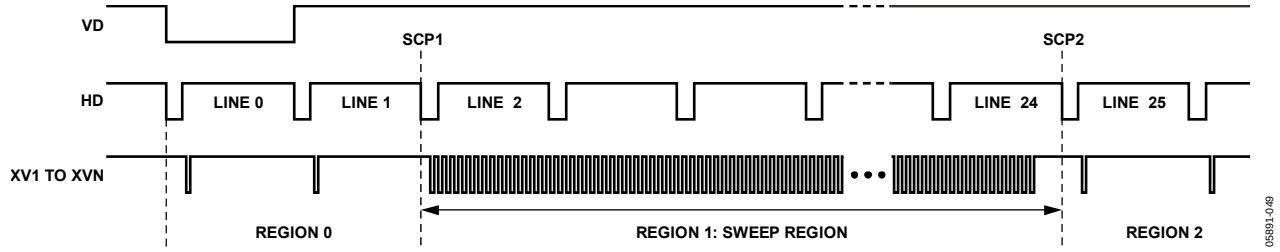


Figure 49. Example of Sweep Region for High Speed Vertical Shift

Sweep Mode Operation

The AD9992 contains an additional mode of vertical timing operation called sweep mode. This mode is used to generate a large number of repetitive pulses that span across multiple HD lines. An example of where this mode is needed is at the start of the CCD readout operation. At the end of the image exposure before the image is transferred by the sensor gate pulses, the vertical interline CCD registers should be free of all charge. This can be accomplished by quickly shifting out any charge using a long series of pulses from the vertical outputs. Depending on the vertical resolution of the CCD, up to 3000 clock cycles may be needed to shift the charge out of each vertical CCD line. This operation spans across multiple HD line lengths. Normally, the AD9992 vertical timing must be contained within one HD line length, but when sweep mode is enabled, the HD boundaries are ignored until the region is finished. To enable sweep mode within any region, program the appropriate SWEEP register to high.

Figure 49 shows an example of the sweep mode operation. The number of vertical pulses needed depends on the vertical resolution of the CCD. The toggle positions for the XV1 to XV24 signals are generated using the V-pattern registers (shown in Table 13). A single pulse is created using the polarity and toggle position registers. The number of repetitions is then programmed to match the number of vertical shifts required by the CCD. Repetitions are programmed into the V-sequence registers (shown in Table 14) by using the VREP registers. This produces a pulse train of the appropriate length. Normally, the pulse train is truncated at the end of the HD line length, but when sweep mode is enabled for this region, the HD boundaries are ignored. In Figure 49, the sweep region occupies 23 HD lines. After the sweep mode region is complete, normal sequence operation resumes in the next region. When using sweep mode, be sure to set the region boundaries (using the sequence change positions) to the appropriate lines to prevent the sweep operation from overlapping the next V-sequence.

Multiplier Mode

To generate very wide vertical timing pulses, a vertical region can be configured into a multiplier region. This mode uses the V-pattern registers in a slightly different manner. Multiplier mode can be used to support unusual CCD timing requirements, such as vertical pulses that are wider than the 13-bit V-pattern toggle position counter. In general, the 13-bit toggle position counter can be used with the sweep mode feature to support very wide pulses; however, multiplier mode can be used to generate even wider pulses.

The start polarity and toggle positions are still used in the same manner as the standard V-pattern group programming, but VLEN is used differently. Instead of using the pixel counter (HD counter) to specify the toggle position locations (XVTOG1, XVTOG2, XVTOG3, and XVTOG4) of the V-pattern group, the VLEN is multiplied with the XVVTOG position to allow very long pulses to be generated. To calculate the exact toggle position, which is counted in pixels after the start position, use the following equation:

Multiplier Mode Toggle Position = XVTOG × VLEN

Because the XVTOG register is multiplied by VLEN, the resolution of the toggle position placement is reduced. If VLEN = 4, the toggle position precision is reduced to 4-pixel increments instead of to single-pixel increments. Table 18 summarizes how the V-pattern group registers are used in multiplier mode operation. In multiplier mode, the VREP registers must always be programmed to the same value as the highest toggle position.

Figure 50 illustrates this operation. The first toggle position is 2, and the second toggle position is 9. In nonmultiplier mode, this causes the V-sequence to toggle at Pixel 2 and then at Pixel 9 within a single HD line. However, in multiplier mode, toggle positions are multiplied by the value of VLEN (in this case, 4); therefore, the first toggle occurs at Pixel 8, and the second toggle occurs at Pixel 36. Sweep mode has also been enabled to allow the toggle positions to cross the HD line boundaries.

Table 18. Multiplier Mode Register Parameters

Register	Length	Range	Description
MULTI	1b	High/low	High enables multiplier mode.
VPOL	1b	High/low	Starting polarity of XV1 to XV10 signals in each V-pattern group.
XVTOG	13b	0 to 8191 pixel location	Toggle positions for XV1 to XV10 signals in each V-pattern group.
VLEN	13b	0 to 8191 pixels	Used as multiplier factor for toggle position counter.
VREP	13b	0 to 8191 pixel location	VREP_EVEN/VREP_ODD must be set to the same value as the highest XVTOG value.

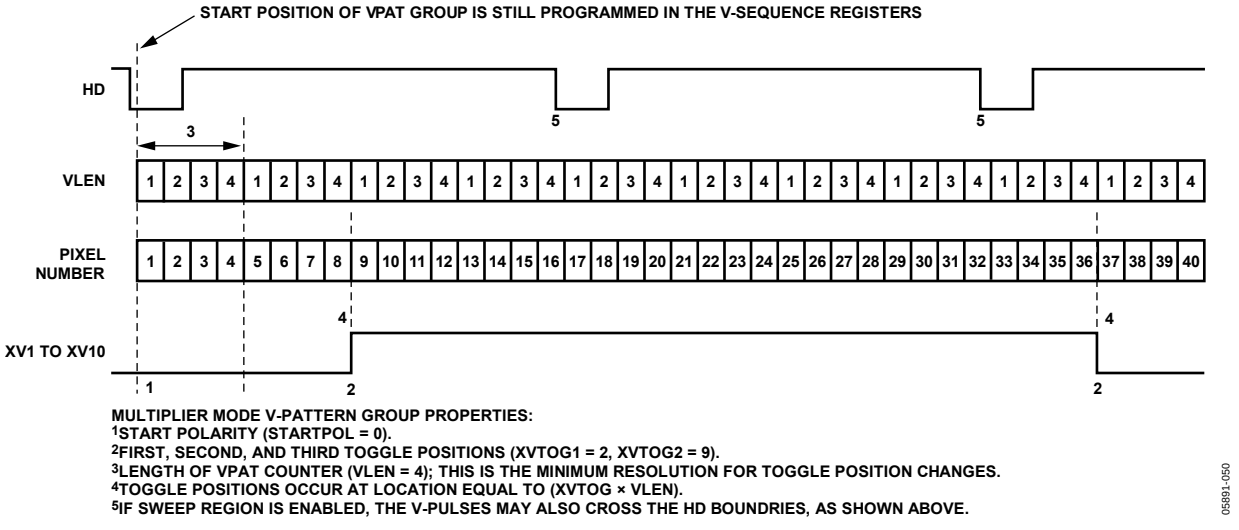


Figure 50. Example of Multiplier Region for Wide Vertical Pulse Timing

Vertical Sensor Gate (Shift Gate) Patterns

In an interline CCD, the vertical sensor gate (VSG) pulses are used to transfer the pixel charges from the light-sensitive image area into light-shielded vertical registers. From the light-shielded vertical registers, the image is clocked out line-by-line using the vertical transfer pulses (XV signals) in conjunction with the high speed horizontal clocks. The AD9992 has 24 vertical signals, and each signal can be assigned as a VSG pulse instead of an XV pulse.

Table 19 summarizes the VSG control registers, which are mostly located in the field registers space (see Table 17). The VSGSELECT register (Address 0x1C in the fixed address space) determines which vertical outputs are assigned as VSG pulses. When a signal is selected to be a VSG pulse, only the starting polarity and two of the V-pattern toggle positions are used. The VSGPATSEL register in the sequence registers is used to assign either XVTOG1 and XVTOG2 or XVTOG3 and XVTOG4 to the VSG signal.

Note that only two of the four V-pattern toggle positions are available when a vertical signal is selected to be a VSG pulse.

The SGACTLINE1 and SGACTLINE2 registers are used to select which line in the field is the VSG line. The VSG active line location is used to reference when the substrate clocking (SUBCK) signal begins to operate in each field. For more information, see the Substrate Clock Operation (SUBCK) section.

Also located in the field registers, the SGMASK register selects which individual VSG pulses are active in a given field. Therefore, all SG patterns to be preprogrammed into the V-pattern registers and the appropriate pulses for the different fields can be enabled separately.

Table 19. VSG Control Registers (Also see Field Registers in Table 17)

Register	Length	Range	Description
VSGSELECT (Located in Fixed Address Space, 0x1C)	24b	High/low	Selection of VSG signals from XV signals. Set to 1 to make signal a VSG. [0]: XV1 selection (0 = XV pulse; 1 = VSG pulse). [1]: XV2 selection. … [23]: XV24 selection.
VSGPATSEL	24b	High/low	When VSG signal is selected using the VSGSELECT register, VSGPATSEL selects which V-pattern toggle positions are used. When set to 0, Toggle 1 and Toggle 2 are used. When set to 1, Toggle 3 and Toggle 4 are used. [0]: XV1 selection (0 = use XVTOG1, XVTOG2; 1 = use XVTOG3, XVTOG4). [1]: XV2 selection. … [23]: XV24 selection.
SGMASK	24b	High/low, each VSG	Set high to mask each individual VSG output. [0]: XV1 mask. … [23]: XV24 mask.
SGACTLINE1	13b	0 to 8191 line number	Selects the line in the field where the VSG signals are active.
SGACTLINE2	13b	0 to 8191 line number	Selects a second line in the field to repeat the VSG signals. If not used, set this equal to SGACTLINE1 or to the maximum value.

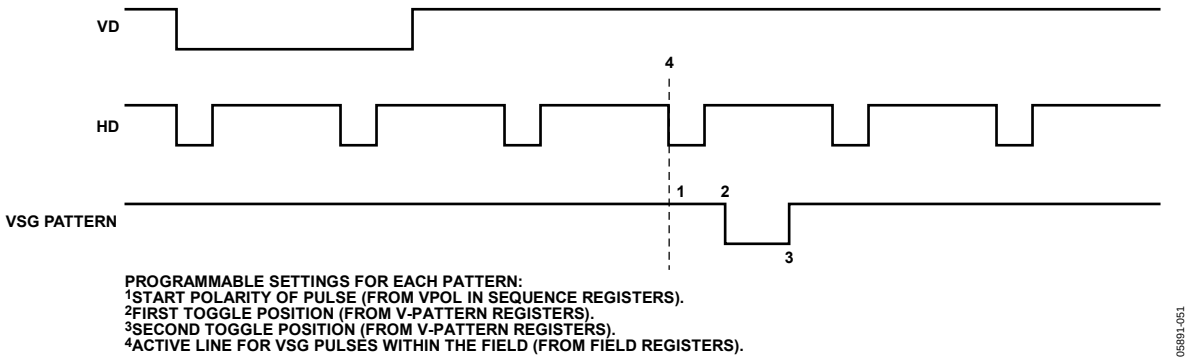


Figure 51. Vertical Sensor Gate Pulse Placement

MODE Registers

The MODE registers are used to select the field timing of the AD9992. Typically, all of the field, V-sequence, and V-pattern information is programmed into the AD9992 at startup. During operation, the MODE registers allow the user to select any combination of field timing to meet the requirements of the system. The advantage of using the MODE registers in conjunction with preprogrammed timing is that it greatly reduces the system programming requirements during camera operation. Only a few register writes are required when the camera operating mode is changed, rather than having to program all of the vertical timing information with each camera mode change.

A basic still camera application can require six fields of vertical timing—one for draft mode operation, one for autofocusing, and four for still image readout. All of the register timing information for the six fields is loaded at startup. Then, during camera operation, the MODE registers select which field timing is active, depending on how the camera is being used.

Table 20 shows how the MODE registers are used. The MODE register (Address 0x2A) specifies how many total fields are used. Any value from 1 to 7 can be selected using these three bits. The other two registers (0x2B and 0x2C) are used to select which of the programmed fields are used and in which order. Up to seven fields can be used in a single MODE write. The AD9992 starts with the field timing specified by FIELD0 and, on the next VD, switches to the timing specified by FIELD1 and so on. After completing the total number of fields specified by MODE, the AD9992 repeats by starting at the first field. This continues until a new write to the MODE register occurs. Figure 54 shows example MODE register settings for different field configurations.

Note that only a write to Address 0x2C properly resets the field counter. Therefore, when changing the values in any of the mode registers, it is recommended that all three registers be updated together in the same field (VD period).

Caution

The MODE registers are SCK updated by default. If they are configured as VD-updated registers by writing Address 0xB4 = 0x03FF and Address 0xB5 = 0xFC00, the new MODE information is updated on the second VD falling edge after the write occurs, rather than on the first VD falling edge (see Figure 53).

Table 20. MODE Registers—VD Updated

Address	Name	Length	Description
2A	MODE	3b	Total number of fields to cycle through. Set from 1 to 7.
2B	FIELD0	5b	Selected FIELD (from FIELD registers in configurable memory) for the first field to cycle through.
	FIELD1	5b	Selected FIELD (from FIELD registers in configurable memory) for the second field to cycle through.
	FIELD2	5b	Selected FIELD (from FIELD registers in configurable memory) for the third field to cycle through.
	FIELD3	5b	Selected FIELD (from FIELD registers in configurable memory) for the fourth field to cycle through.
	FIELD4	5b	Selected FIELD (from FIELD registers in configurable memory) for the fifth field to cycle through.
2C	FIELD5	5b	Selected FIELD (from FIELD registers in configurable memory) for the sixth field to cycle through.
	FIELD6	5b	Selected FIELD (from FIELD registers in configurable memory) for the seventh field to cycle through.

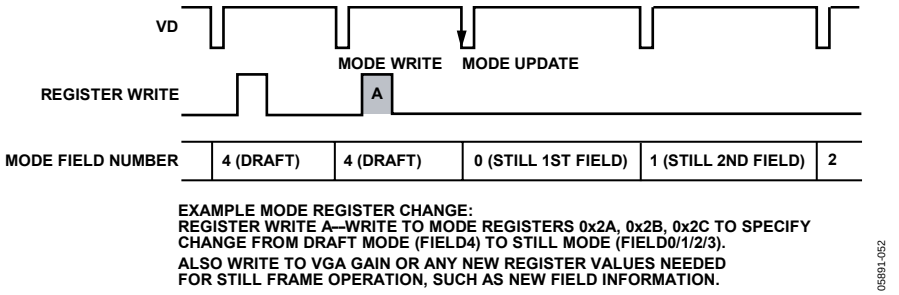


Figure 52. Update of MODE Register, SCK Updated (Default Setting)

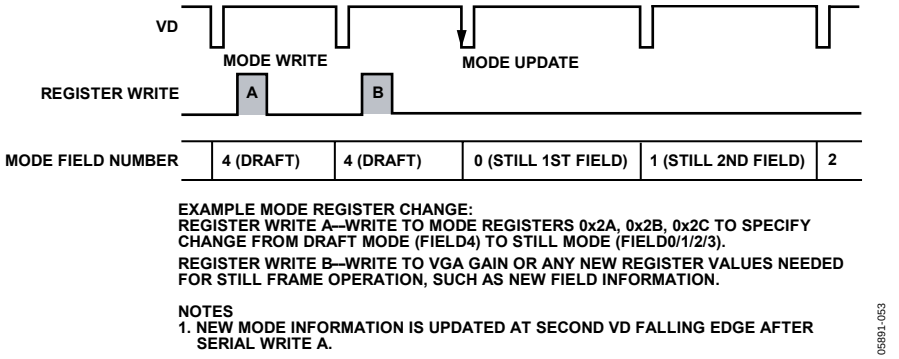


Figure 53. Update of MODE Register if Changed to VD-Updated Register

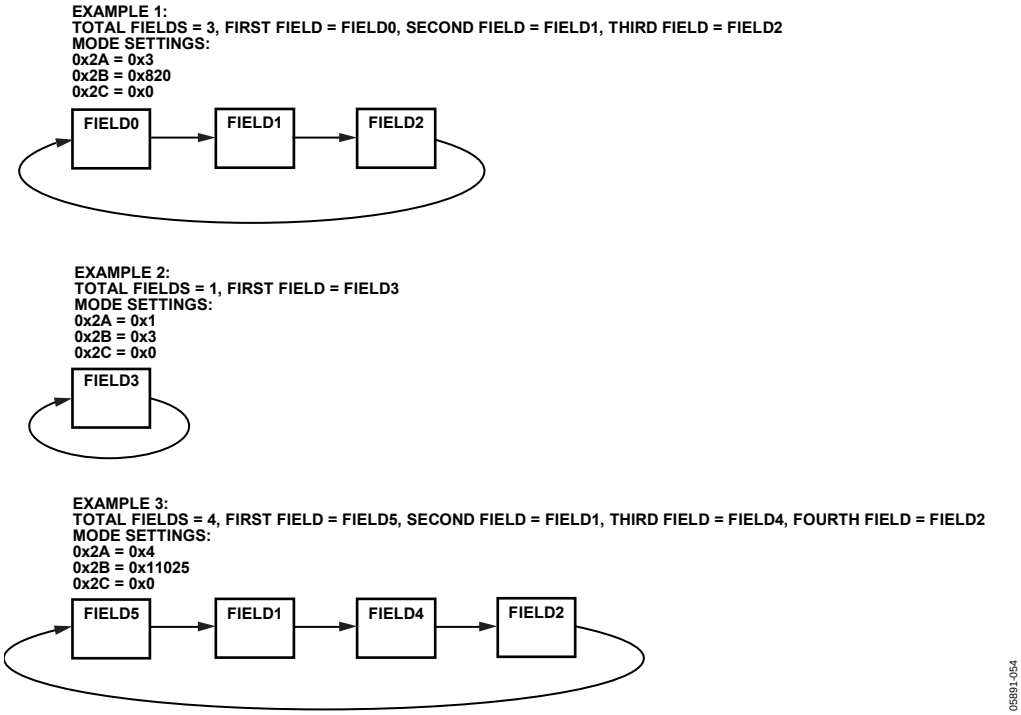


Figure 54. Using the MODE Registers to Select Field Timing

VERTICAL TIMING EXAMPLE

To better understand how AD9992 vertical timing generation is used, consider the example CCD timing chart in Figure 55. This example illustrates a CCD using a general 3-field readout technique. As described in the Complete Field: Combining V-Sequences section, each readout field must be divided into separate regions to perform each step of the readout. The sequence change positions (SCP) determine the line boundaries for each region, and the SEQx registers assign a particular V-sequence to each region. The V-sequences contain the specific timing information required in each region: XV1 to XV6 pulses (using V-pattern groups), HBLK/CLPOB timing, and VSG patterns for the SG active lines.

This timing example requires four regions for each of the three fields, labeled Region 0, Region 1, Region 2, and Region 3. Because the AD9992 allows many individual fields to be programmed, FIELD0, FIELD1, and FIELD2 can be used to meet the requirements of this timing example. The four regions for each field are very similar in this example, but the individual registers for each field allow flexibility to accommodate other timing charts.

Region 0 is a high speed, vertical shift region. Sweep mode can be used to generate this timing operation with the desired number of high speed vertical pulses needed to clear any charge from the CCD vertical registers.

Region 1 consists of only two lines and uses standard single-line, vertical shift timing. The timing of this region is the same as the timing in Region 3.

Region 2 is the sensor gate line where the VSG pulses transfer the image into the vertical CCD registers. This region may require the use of the second V-pattern group for the SG active line.

Region 3 also uses the standard single-line, vertical shift timing, the same timing as Region 1. Four regions are required in each of the three fields.

The timing for Region 1 and Region 3 is essentially the same, reducing the complexity of the register programming. Other registers need to be used during the actual readout operation. These include the MODE registers, shutter control registers (PRIMARY_ACTION, SUBCK, GPO for MSHUT, and VSUB control), and AFE gain register.

Important Note Regarding Signal Polarities

When programming the AD9992 to generate the XV1 to XV24 and SUBCK signals, the external V-driver circuit usually inverts these signals. Carefully check the required timing signals needed at the input and the output of the V-driver circuit being used and adjust the polarities of the AD9992 outputs accordingly.

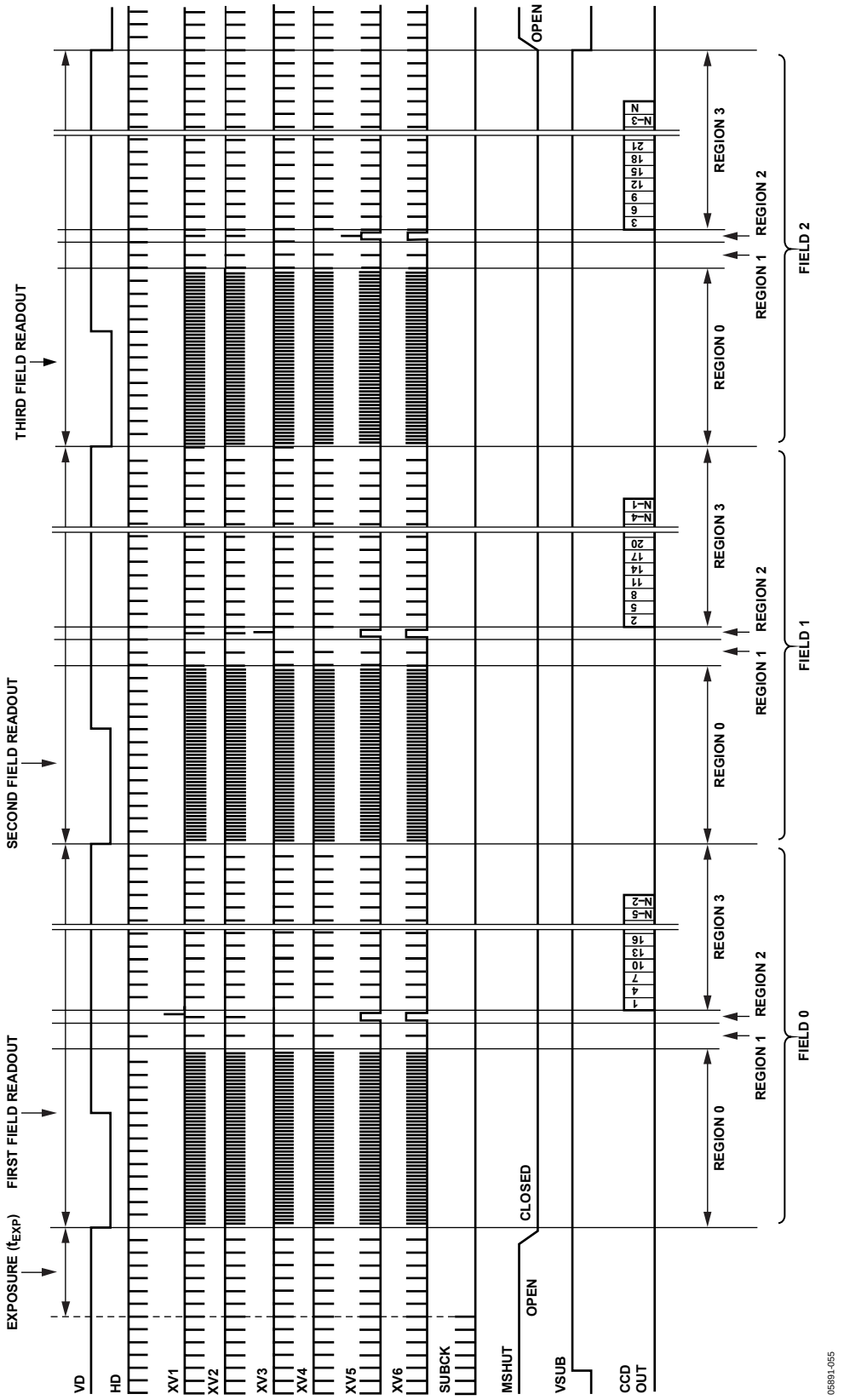


Figure 55. CCD Timing Example—Dividing Each Field into Regions

SHUTTER TIMING CONTROL

The AD9992 supports the generation of electronic shuttering (SUBCK) and also features flexible general-purpose outputs (GPO) to control mechanical shuttering, CCD substrate bias switching, and strobe circuitry. In the following documentation, the terms sense gate (SG) and vertical sense gate (VSG) are used interchangeably.

SUBSTRATE CLOCK OPERATION (SUBCK)

The CCD image exposure time is controlled by the substrate clock signal (SUBCK), which pulses the CCD substrate to clear out accumulated charge. The AD9992 supports three types of electronic shuttering: normal, high precision, and low speed. Along with the SUBCK pulse placement, the AD9992 can accommodate different readout configurations to further suppress the SUBCK pulses during multiple field readouts.

The SUBCK signal is a programmable string of pulses, each occupying a line following the primary sense gate active line, SGACTLINE1 (registers are shown in Table 21). The SUBCK signal has programmable pulse width, line placement, and number of pulses to accurately control the exposure time.

SUBCK: Normal Operation

By default, the AD9992 operates in the normal SUBCK configuration, in which the SUBCK signal is pulsing in every VD field (see Figure 56). The SUBCK pulse occurs once per line, and the total number of repetitions within the field determines the length of the exposure time. The SUBCK pulse polarity and toggle positions within a line are programmable using the SUBCK_POL and SUBCK_TOG1 registers (see Table 21). The number of SUBCK pulses per field is programmed in the SUBCKNUM register (Address 0x75).

As shown in Figure 56, the SUBCK pulses always begin in the line following the SG-active line, which is specified in the SGACTLINE registers for each field. The SUBCK_POL, SUBCK_TOG1, SUBCK_TOG2, SUBCKNUM, and SUBCKSTARTLINE registers are updated at the start of the line after the sensor gate line, as described in the Updating New Register Values section.

SUBCK: High Precision Operation

High precision shuttering is used in the same manner as normal shuttering but uses an additional register to control the last SUBCK pulse. In this mode, the SUBCK still pulses once per line, but the last SUBCK in the field has an additional SUBCK pulse, whose location is determined by the SUBCKHP_TOG registers, as shown in Figure 57. Finer resolution of the exposure time is possible using this mode. Leaving the SUBCKHP_TOG registers set to its maximum value (0xFFFFFF) disables the last SUBCK pulse (default setting).

SUBCK: Low Speed Operation

Normal and high precision shutter operations are used when the exposure time is less than 1 field. For exposure times greater than 1 field, the low speed (LS) shutter features can be used. The AD9992 includes a field counter (primary field counter) to regulate long exposure times. The primary field counter must be activated (Address 0x70) to serve as the trigger for the LS operation. The durations of the LS exposure and read are specified by the SGMASK_NUM and SUBCKMASK_NUM register (Address 0x74), respectively. As shown in Figure 58, this mode suppresses the SUBCK and VSG outputs for up to 8192 fields (VD periods).

To activate an LS shutter operation, trigger the start of the exposure by writing to the PRIMARY_ACTION register bits according to the desired effect. When the primary counter is activated, the next VD period becomes the first active period of the exposure for which the VSG and SUBCK masks are applied.

Optionally, if the SUBCKMASK_SKIP1 register is enabled, the AD9992 ignores the first VSG and SUBCK masks in subsequent fields. This is generally desired so that the exposure time begins in the field after the exposure operation is initiated. Figure 58 shows operation with SUBCKMASK_SKIP1 = 1.

If the PRIMARY_ACTION register is used while the SUBCKMASK_NUM and SGMASK_NUM registers are set to 0, the behavior of the SUBCK and VSG signals are not different from the normal shutter or high precision shutter operations. Therefore, the primary field counter can be used for other tasks (described in the General-Purpose Outputs (GPOs) section) without disrupting the normal activity. In addition, there exists a secondary field counter that has no effect on the SUBCK and VSG signals. These counters are described in detail in the Field Counters section.

SUBCK Start Line

By default, the SUBCK pulses begin in the line following SGACTLINE1. For applications where the SUBCK pulse should be suppressed for one or more lines following the VSG line, the SUBCKSTARTLINE register can be programmed. This register setting delays the start of the SUBCK pulses until the specified number of lines following SGACTLINE1.

Caution

A value of 1 should not be used in the SUBCKSTARTLINE register. A value of 0 is used to specify the SUBCK pulses to begin in the next line after the SG line. A value of 2 is used to specify the SUBCK pulses to begin two lines after the SG line, and so on.

Read After Exposure

To read the CCD data after exposure, the SG should resume normal activity while the SUBCK remains null. By default, the AD9992 generates the VSG pulses in every field. When only a single exposure and a single frame read are desired, such as is the case in the preview mode, the VSG and SUBCK pulses can operate in every field.

Other applications require that more frames are read, in which case SUBCK must be masked until the readout is finished.

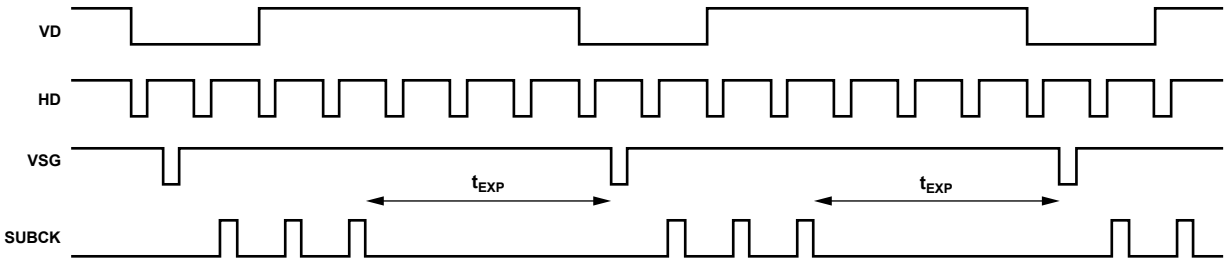
The SUBCKMASK_NUM register specifies the total number of fields (exposure and read) to mask SUBCK. A 2-field CCD frame read mode typically requires two additional fields of SUBCK masking (SUBCKMASK_NUM = 2). A 3-field, 6-phase CCD requires three additional fields of SUBCK masking after the read begins (SUBCKMASK_NUM = 3).

Note that the SUBCKMASK_SKIP1 register setting allows SUBCK pulses at the beginning of the field of exposure.

Table 21. SUBCK and Exposure/Read Register Parameters

Register	Length	Range	Description
SGMASK_NUM	13b	0 to 8191 fields	Exposure duration (number of fields to suppress VSG) for LS operation.
SUBCKMASK_NUM	13b	0 to 8191 fields	Exposure plus readout duration (number of fields to suppress SUBCK) for LS.
SUBCKMASK_SKIP1	1b	On/off	Suppress SG/SUBCK masks for one field (default = 0). Typically set to 1.
SUBCKSTARTLINE[1]	13b	0, 2 to 8191 line locations	Line location to start the SUBCK pulses, relative to SGLINE location. A value of 1 is invalid. See the SUBCK Start Line section.
SUBCKNUM[1]	13b	1 to 8191 pulses	Total number of SUBCKs per field, at 1 pulse per line. Must be <VDLEN.
SG_SUPPRESS[1]	1b	On/off	Suppress the SG and allow SUBCK to finish at SUBCKNUM.
SUBCK_TOG1	13b	0 to 8191 pixel locations	SUBCK Toggle Position 1.
SUBCK_TOG2	13b	0 to 8191 pixel locations	SUBCK Toggle Position 2.
SUBCK_POL	1b	Low/high	SUBCK start polarity.
SUBCKHP_TOG1	13b	0 to 8191 pixel locations	High precision SUBCK Toggle Position 1. Selectable as SG or VD updated.
SUBCKHP_TOG2	13b	0 to 8191 pixel locations	High precision SUBCK Toggle Position 2. Selectable as SG or VD updated.

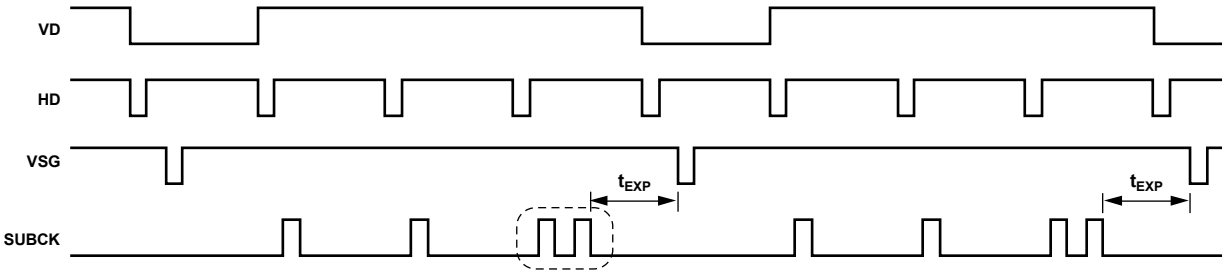
[1] Register is not VD updated but is updated at the start of the line after the sensor gate line.



SUBCK PROGRAMMABLE SETTINGS:
1. PULSE POLARITY USING THE SUBCK_POL REGISTER.
2. NUMBER OF PULSES WITHIN THE FIELD USING THE SUBCKNUM REGISTER (SUBCKNUM = 3 IN THE ABOVE EXAMPLE).
3. PIXEL LOCATION OF PULSE WITHIN THE LINE AND PULSE WIDTH PROGRAMMED USING THE SUBCK1 TOGGLE POSITION REGISTERS.

05891-056

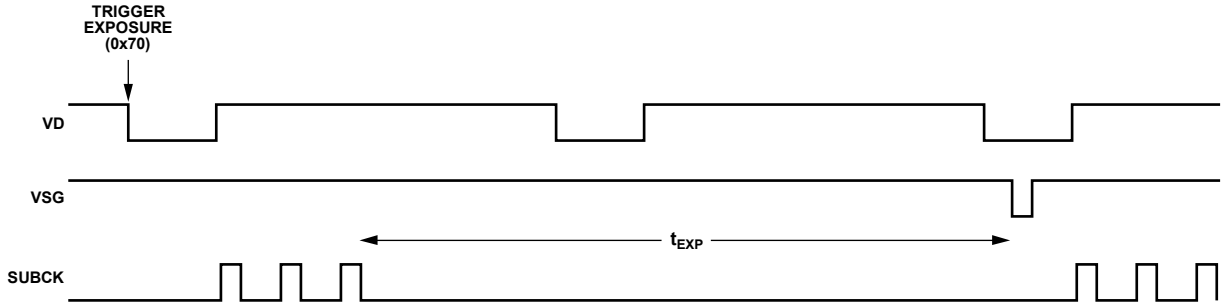
Figure 56. Normal SUBCK Operation



NOTES
1. SECOND SUBCK PULSE IS ADDED IN THE LAST SUBCK LINE.
2. LOCATION OF SECOND PULSE IS FULLY PROGRAMMABLE USING THE SUBCKHP TOGGLE POSITION REGISTERS.

05891-057

Figure 57. High Precision SUBCK Operation



NOTES
1. SUBCK CAN BE SUPPRESSED FOR MULTIPLE FIELDS BY PROGRAMMING THE EXPOSURE REGISTER TO BE GREATER THAN 0.
2. ABOVE EXAMPLE USES EXPOSURE = 1.
3. TRIGGER REGISTER MUST ALSO BE USED TO START THE LOW SPEED EXPOSURE.
4. VD/HD OUTPUTS CAN ALSO BE SUPPRESSED USING THE VDHDOFF REGISTER = 1.

05891-058

Figure 58. Low Speed SUBCK Operation

FIELD COUNTERS

The AD9992 contains three field counters (primary, secondary, and mode). When these counters are active, they increment with each VD cycle. The mode counter is the field counter used with the mode register to control the vertical timing signals (see the MODE Registers section. The primary and secondary counters are more flexible and are generally used for shuttering signal applications. Both the primary and secondary counters have several modes of operation that are dictated by Address 0x70, including

- Normal (single count)
- RapidShot (repeating count)
- ShotDelay (delayed count)
- ShotDelay with RapidShot
- Manual exposure
- Manual readout
- Force to idle

The primary counter regulates the expose and read actions by regulating the SUBCK and VSG signals. If the RapidShot feature is used with the primary counter, the SUBCK and VSG masking automatically repeats as necessary for multiple expose/read cycles. The secondary counter has no effect on the SUBCK or VSG signal. Both counters can be used to regulate the general-purpose signals described in the General-Purpose Outputs (GPOs) section.

Table 22. Primary/Secondary Field Counter Registers (Address 0x70, Address 0x71, and Address 0x72)

Register	Length	Description
PRIMARY_ACTION	3b	0: Idle, no counter action. GPO signals can still be controlled using polarity or GP_PROTOCOL = 1.
SECOND_ACTION	3b	1: Activate counter. Single cycle of counter from 1 to counter maximum value, and then returns to idle state.
		2: RapidShot. After reaching maximum counter value, counter wraps and repeats until reset.
		3: ShotTimer. Active single cycle of counter after added delay of N fields (use the corresponding DELAY register).
		4: ShotTimer with RapidShot. Same as 2, with added delay of N fields between each repetition.
		5: Manual exposure. Primary counter stays in exposure until manual readout or reset to idle. This mode keeps the SUBCK and VSG pulses masked indefinitely.
		6: Manual readout. Primary counter switches to readout (VSG pulses becomes active).
		7: Force to idle.
PRIMARY_MAX	13b	Primary counter maximum value.
SECOND_MAX	12b	Secondary counter maximum value.
VDHD_MASK	3b	Mask VD/HD during counter operation.
PRIMARY_DELAY	13b	ShotTimer. Number of fields to delay before the next primary count (exposure) starts. If using ShotTimer with RapidShot, delay value is used between each repeat.
PRIMARY_SKIP	1b	When using ShotTimer with RapidShot, use primary delay value only before first count (exposure).
SECOND_DELAY	13b	ShotTimer. Number of fields to delay before the next secondary count starts. If using ShotTimer with RapidShot, delay value is used between each repeat.
SECOND_SKIP	1b	When using ShotTimer with RapidShot, use secondary delay value only before first count.

GENERAL-PURPOSE OUTPUTS (GPOS)

The AD9992 provides programmable outputs to control a mechanical shutter, strobe/flash, the CCD bias select signal, or any other external component with general-purpose (GP) signals. Eight GP signals, with up to four toggles each, are available that can be programmed and assigned to special GPO pins. These pins are bidirectional and allow visibility (as an output) and external control (as an input) of HBLK, PBLK, CLPOB, and OUTCONTROL. The registers introduced in this section are described in Table 23.

GP Toggles

When configured as an output, each GPO1 to GPO8 output can deliver a signal that is the result of programmable toggle positions. The GP signals are independent and can be linked to either a specific VD period or over a range of VD periods via the primary or secondary field counters through the GP protocol registers (Address 0x73). As a result of their associations with the field counters, the GP toggles inherit the characteristics of the field counters, such as RapidShot and ShotDelay.

To use the GP toggles,

1. Program the toggle positions (Address 0x7A to Address 0xA9).
2. Program the protocol (Address 0x73).
3. Program the counter parameters (Address 0x71 to Address 0x72).
4. Activate the counter (Address 0x70).

For Protocol 1 (no counter association), skip Step 3 and Step 4.

With these four steps, the GP signals can be programmed to accomplish many common tasks. Careful protocol selection and application of the field counters yields efficient results to allow the GP signals smooth integration with concurrent operations.

Note that the SUBCK and VSG masks are linked to the primary counter; however, if their parameters are 0, the GPO can use the primary counter without expose/read activity.

The secondary counter is independent and can be used simultaneously with the primary counter. Some applications may require the use of both primary and secondary field counters with different GPO protocols, start times, and durations. Such operations are easily handled by the AD9992.

Several simple examples of GPO applications using only one GPO and one field counter follow. These examples can be used as building blocks for more complex GPO activity. In addition, specific GPO signals can be passed through a 4-input LUT to realize combinational logic between them. For example, GP1 and GP2 can be sent through an XOR look-up table, and the result can be delivered on GP1, GP2, or both. Also, either GP1 or GP2 can deliver their original toggles.

Table 23. GPO Registers

Register	Length	Range	Description
GP1_PROTOCOL	3b	0 to 7	0: Idle.
GP2_PROTOCOL	3b	0 to 7	1: No counter association, use MANUAL_TRIG bits to enable each GP signal.
GP3_PROTOCOL	3b	0 to 7	2: Link to primary counter.
GP4_PROTOCOL	3b	0 to 7	3: Link to secondary counter.
GP5_PROTOCOL	3b	0 to 7	4: Link to mode counter (from vertical timing generation).
GP6_PROTOCOL	3b	0 to 7	5: Primary repeat (allows GP signals to repeat with RapidShot).
GP7_PROTOCOL	3b	0 to 7	6: Secondary repeat (allows GP signals to repeat with RapidShot).
GP8_PROTOCOL	8b	0 to 7	7: Keep on.
MANUAL_TRIG	8b	Off/on	Manual trigger for each GP signal, for use with Protocol 1.
GP<1:8>_POL	8b	Low/high	Starting polarity for GP signals, only updated during PROTOCOL = 0.
SEL_GP<1:8>	8b	Off/on	1: Select GP toggles visible at GPO1 to GPO8 when output is enabled (default); 0: Select vertical signals visible at GPO4 to GPO8 when output is enabled. GPO4: SUBCK. GPO5: XV21. GPO6: XV22. GPO7: XV23. GPO8: XV24.
GPO_OUTPUT_EN	8b	Off/on	1: Enable GPO1 to GPO8 outputs (one bit per output). 0: Disable GPO1 to GPO8 outputs, pins will be high-Z state (default).
GP*_USE_LUT	8b	Off/on	Send GP signals through a programmable look-up table (LUT).
LUT_FOR_GP12	4b	Logic setting	Desired logic to be realized on GP1 combined with GP2.
LUT_FOR_GP34	4b	Logic setting	Desired logic to be realized on GP3 combined with GP4.
LUT_FOR_GP56	4b	Logic setting	Desired logic to be realized on GP5 combined with GP6.
LUT_FOR_GP78	4b	Logic setting	Desired logic to be realized on GP7 combined with GP8. Example logic settings for LUT_FOR_GPxy: 0x6: GPy XOR GPx (see Figure 64). 0x7: GPy NAND GPx. 0x8: GPy AND GPx. 0xE: GPy OR GPx.
GP*_TOG*_FD	13b	0 to 8191 field	Field of activity, relative to primary and secondary counter for corresponding toggle.
GP*_TOG*_LN	13b	0 to 8191 line	Line of activity for corresponding toggle.
GP*_TOG*_PX	13b	0 to 8191 pixel	Pixel of activity for corresponding toggle.
GPO_INT_EN	1b	Off/on	When set to 1, internal signals are viewable on GPO5 to GPO8. GPO5: OUTCONTROL. GPO6: HBLK. GPO7: CLPOB. GPO8: PBLK.

Single-Field Toggles

Single-field toggles occur in the next field only. There can be up to four toggles in the field. The mode is set with GP_PROTOCOL equal to 1, and then the toggles are triggered in the next field by writing to the MANUAL_TRIG register (0x70 [13:6]). In this mode, the field toggle settings must be set to a value of 1. Two consecutive fields do not have activity. If toggles are required to repeat in the next field, the MANUAL_TRIG register can be written to in consecutive fields.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x7D ← 0x00C4002
0x7E ← 0x0004000
0x7F ← 0x00000B3

Details

A) Field 0: 0x70 ← 0x0000040
0x73 ← 0x0000001

B) Field 1: 0x73 ← 0x0000000

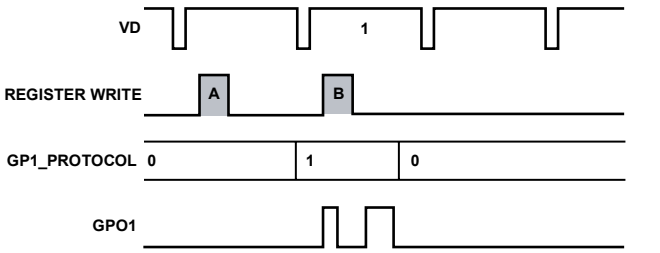


Figure 59. Single-Field Toggles Using GP1_PROTOCOL = 1

Scheduled Toggles

Scheduled toggles are programmed to occur during any upcoming field. For example, there can be one toggle in Field 1, two toggles in Field 3, and a last toggle in Field 4. The mode is set with GP_PROTOCOL = 2 or GP_PROTOCOL = 3. Mode 2 tells the GPO to obey the primary field counter, and Mode 3 tells the GPO to obey the secondary field counter.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

0x7A ← 0x00C4002
0x7B ← 0x0004000
0x7C ← 0x00000B3

Details

A) Field 0: 0x70 ← 0x0000008
0x73 ← 0x0000003

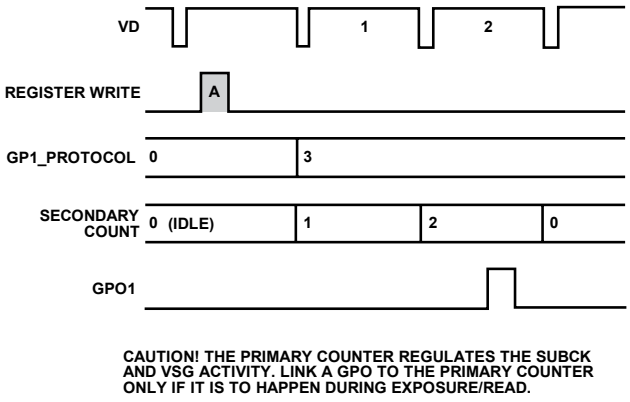


Figure 60. Scheduled Toggles Using GP1_PROTOCOL = 3

RapidShot Sequences

RapidShot technology provides continuous repetition of scheduled toggles.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

0x71 ← 0x0004000
0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x7D ← 0x00C4002
0x7E ← 0x0004000
0x7F ← 0x00000B3
0x73 ← 0x0000006

Details

A) Field 0: 0x70 ← 0x0000010

B) Field 2: 0x70 ← 0x0000007

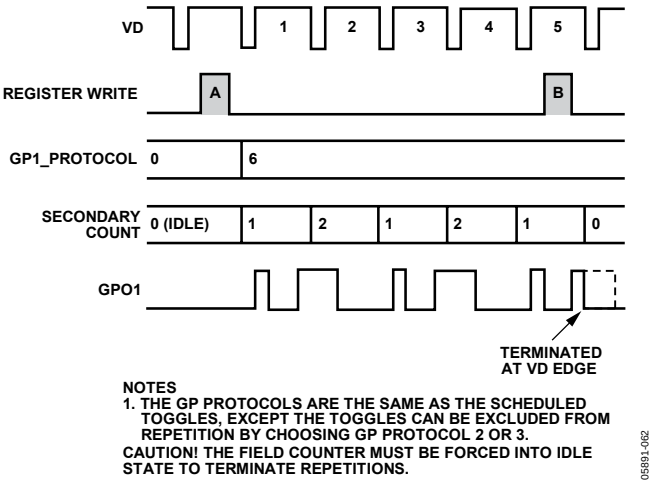


Figure 61. RapidShot Toggle Operation Using GP1_PROTOCOL = 6

ShotDelay Sequences

ShotDelay technology provides internal delay of scheduled toggles. The delay is in terms of fields.

Preparation

The GP toggle positions can be programmed any time prior to use. For example,

0x71 ← 0x0004000
0x72 ← 0x000C000
0x7A ← 0x000A001
0x7B ← 0x0002000
0x7C ← 0x000000F
0x73 ← 0x0000003

Details

A) Field 0: 0x70 ← 0x0000018

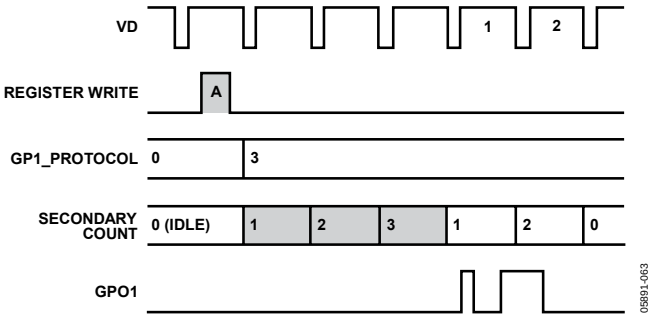


Figure 62. ShotDelay Toggle Operation Using GP1_PROTOCOL = 3

GP LOOK-UP TABLES (LUT)

The AD9992 is equipped with a look-up table for each pair of consecutive GP signals when configured as outputs. GP1 is always combined with GP2, GP3 is always combined with GP4, GP5 is always combined with GP6, and GP7 is always combined with GP8. The external GPO outputs from each pair can output the result of the LUT or the original GP internal signal.

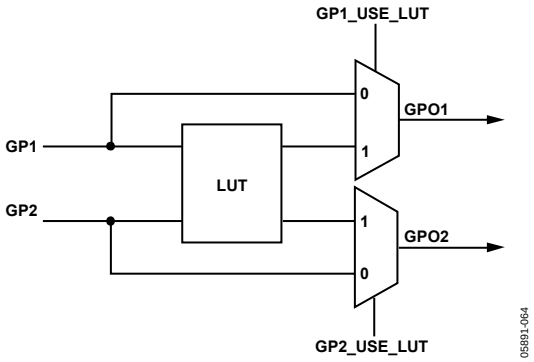


Figure 63. Internal LUT for GP1 and GP2 Signals

Address 0x79 dictates the behavior of the LUT and which signals receive the result. Each 4-bit LUT_FOR_GPxy register can realize any logic combination of GPx and GPy. For example, Table 24 shows how the register values of LUT_FOR_GP12 [11:8] are determined. XOR, NAND, AND, and OR results are shown, but any 4-bit combination is possible. A simple example of XOR gating is shown in Figure 64.

Table 24. LUT Results Based on GP1 and GP2 Values

GP2	GP1	LUT: XOR	LUT: NAND	LUT: AND	LUT: OR
0	0	0	1	0	0
0	1	1	1	0	1
1	0	1	1	0	1
1	1	0	0	1	1

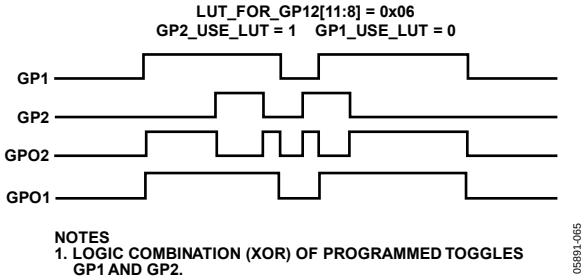


Figure 64. LUT Example for GP1 XOR GP2

Field Counter and GPO Limitations

The following is a summary of the known limitations of the field counters and GPO signals that dictate usability:

- The field counter trigger (PRIMARY_ACTION and SECONDARY_ACTION registers, Address 0x70) is self-reset at the start of every VD period. Therefore, there must be one VD period between sequential programming to that address.
- If GP*_PROTOCOL = 1, it must be manually reset to GP*_PROTOCOL = 0 one VD period before it can be used again. If manual toggles are desired in sequential fields, the MANUAL_TRIG register should be used in conjunction with GP*_PROTOCOL = 1.

COMPLETE EXPOSURE/READOUT OPERATION USING PRIMARY COUNTER AND GPO SIGNALS

Figure 65 demonstrates a typical expose/read cycle while exercising the GPO signals. Using a 3-field CCD with an exposure time that is greater than one field but less than two fields in duration requires a total of five fields for the entire exposure/readout operation. Other exposure times and other CCD field configurations require modification of these example settings.

Note that, if the MODE registers are changed to VD updated, as shown in the MODE Registers section and in Figure 53, the MODE update is delayed by one additional field. This should be accounted for in selecting the number of fields to cycle and the VD location to write to the MODE registers.

1. The primary counter is used to control the masking of VSG and SUBCK during exposure/readout. The PRIMARY_MAX register should be set equal to the total number of fields used for exposure and readout. In this example, PRIMARY_MAX = 5.

   The SUBCK masking should not occur immediately at the next VD edge (Step 2) because this would define an exposure time that begins in the previous field. Write to the PRIMARY_DELAY register to delay the masking of VSG and SUBCK pulses in the first exposure field. In this example, MASKDELAY = 1.

   Write to the SUBCKMASK_NUM register (Address 0x74) to specify the number of fields to mask SUBCK while the CCD data is read. In this example, SUBCKMASK_NUM = 4.

   Write to the SGMASK_NUM register (Address 0x74) to specify the number of fields to mask VSG outputs during exposure. In this example, SGMASK_NUM = 1.

   Write to the PRIMARY_ACTION register (Address 0x70) to trigger the GP1 (STROBE), GP2 (MSHUT), and GP3 (VSUB) signals and to start the expose/read operation.

   Write to the MODE registers to configure the next five fields. The first two fields during exposure are the same as the current draft mode fields, and the following three fields are the still-frame readout fields. The register settings for the draft mode field and the three readout fields are previously programmed. Note that if the MODE registers are changed to VD updated, only one field of exposure should be included (the second one) because the MODE settings will be delayed an extra field.
2. VD/HD falling edge updates the serial writes from 1.
3. GP3 (VSUB) output turns on at the field/line/pixel specified. VSUB Example 1 and Example 2 use GP3TOG1_FD = 1.
4. GP1 (STROBE) output turns on and off at the location specified.
5. GP2 (MSHUT) output turns off at the location specified.
6. The next VD falling edge automatically starts the first read field.
7. The next VD falling edge automatically starts the second read field.
8. The next VD falling edge automatically starts the third read field.
9. Write to the MODE register to reconfigure the single draft mode field timing. Note that if the MODE registers are changed to VD updated, this write should occur one field earlier.
10. VD/HD falling edge updates the serial writes from Step 9. VSG outputs return to draft mode timing. SUBCK output resumes operation. GP2 (MSHUT) output returns to the on position (active or open). GP3 (VSUB) output returns to the off position (inactive)

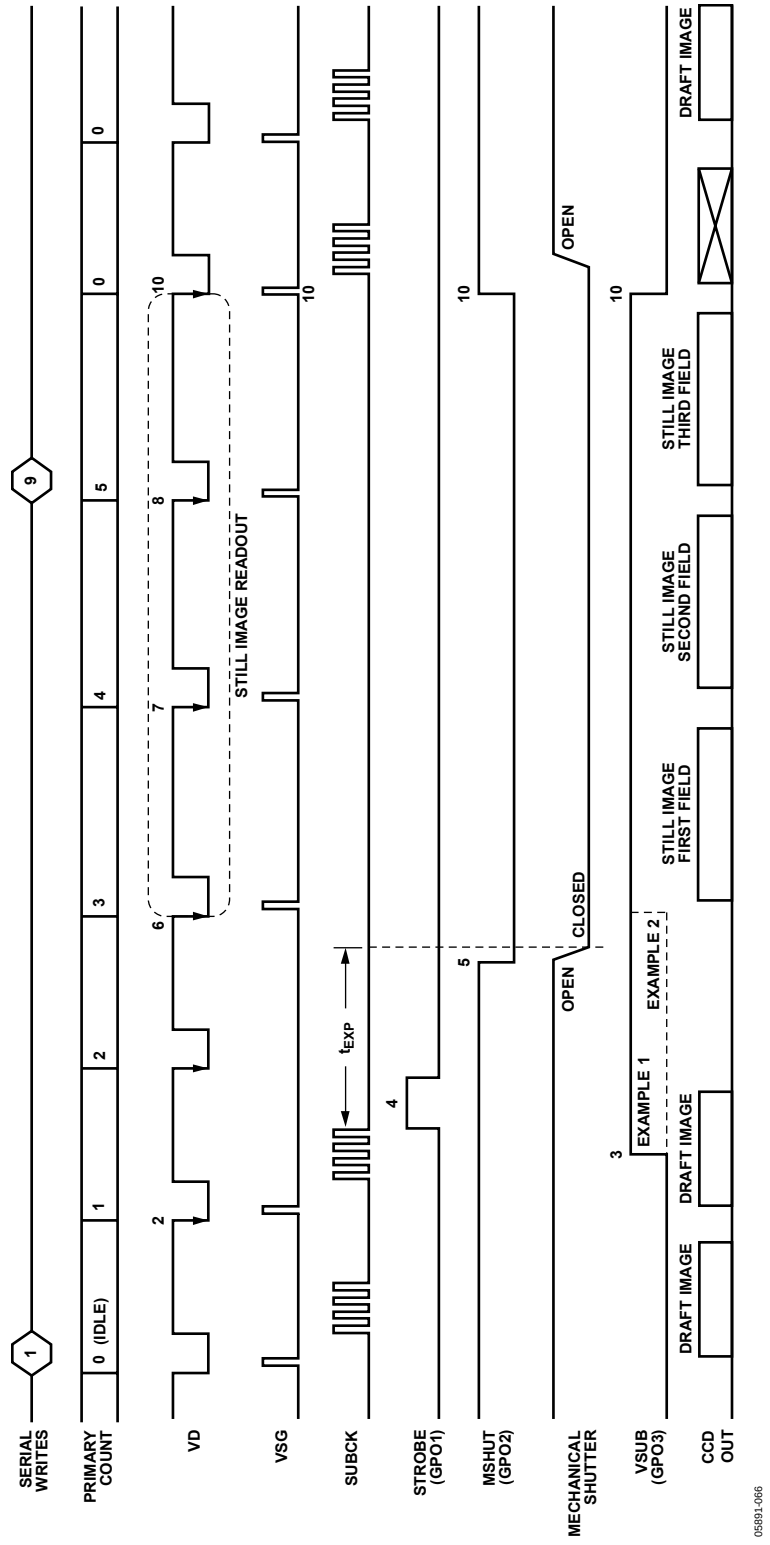


Figure 65. Complete Exposure/Readout Operation Using Primary Counter and GPO Signals

MANUAL SHUTTER OPERATION USING ENHANCED SYNC MODES

The AD9992 also supports an external signal to control exposure, using the SYNC input. Generally, the SYNC input is used as an asynchronous reset signal during master mode operation. When the enhanced SYNC mode is enabled, the SYNC input provides additional control of the exposure operation.

Normal SYNC Mode (Mode 1)

By default, the SYNC input is used in master mode for synchronizing the internal counters of the AD9992 with external timing. The SYNC During Master Mode Operation section describes how horizontal, vertical, and field designator signals are reset by the rising edge of the SYNC pulse. Figure 66 also shows how this mode operates, highlighting the behavior of the mode field designator.

Enhanced SYNC Modes (Mode 2 and Mode 3)

The enhanced SYNC modes can be used to accommodate unique synchronization requirements during exposure operations. In SYNC Mode 2, the V and VSG outputs are suspended and the VD output is masked. The V-outputs are held at the dc value established by the Sequence 0 start polarities. There is no SCP operation, but the H-counter is still enabled. Finally, the AFE sampling clocks HD, H/RG, CLPOB, and HBLK are operational and use Sequence 0 behavior. See Figure 67 for more details.

Set Register ENH_ SYNC_EN (Address 0x13 Bit 3) to 1 to enable the enhanced SYNC modes

Mode 3 uses all of these features, but the V-outputs are continuous through the SYNC pulse interval. VD control pulses are masked during the SYNC interval, and the HD pulse can also be masked if required (see Figure 68).

It is important to note that in both of these enhanced modes, the SYNC pulse resets the counters at both the falling edge and the rising edge of the SYNC pulse.

Register Update and Field Designator

When using special SYNC Mode 2 or SYNC Mode 3, the VD-updated registers, such as PRIMARY_ACTION, are not updated during the SYNC interval, and the SCP0 function is ignored and held at 0 (see Figure 69).

When using SYNC Mode 2 or SYNC Mode 3, both the rising and falling edges increment the internal field designator; therefore, the new register data takes effect and VTP information is updated to new SEQ0 data. However, this does not occur if the MODE register creates an output of one field. In that case, the region, sequence, and group information does not change (see Figure 70).

Shutter Operation in SLR Mode

Referring to Figure 71,

1. To turn on VSUB, write to the appropriate GP registers to start VSUB and manual exposure [PRIMARY_ACTION = 5]. This change takes effect after the next VD. SUBCK is suppressed during the exposure and readout phases.
2. To turn on MSHUT during the interval between the next VD and SYNC, write to the appropriate GP register. When MSHUT is in the on position, it has line and pixel control. This change takes effect on the SYNC falling edge because there is an internal VD.
3. If the MODE register is programmed to cycle through multiple fields (5, 7, 3, 5, 7, 3, …, in this example), the internal field designator increments. If the MODE register is not required to increment, set up the MODE register such that it outputs only one field. This prevents the MODE counter from incrementing during the SYNC interval.
4. Write to the manual readout trigger to begin the manual readout [PRIMARY_ACTION = 6]. Write to the appropriate GP registers to trigger MSHUT to toggle low at the end of the exposure. This change takes effect on the SYNC rising edge during readout. Because VD register update is disabled, the trigger takes effect on the SYNC rising edge. The MSHUT falling edge is aligned to the SYNC rising edge. Because the MSHUT falling edge is aligned with VD, it may be necessary to insert a dummy VD to delay the readout.

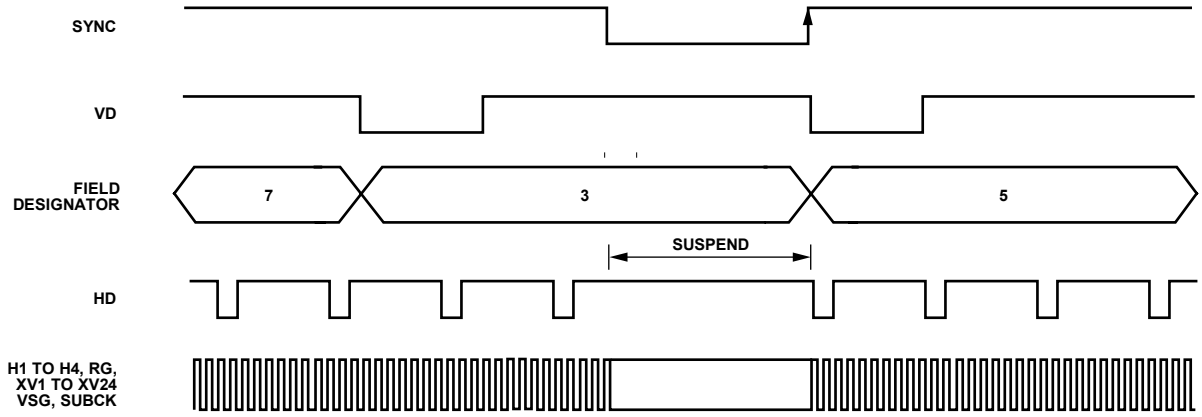
Note that because the internal exposure counter (PRIMARY counter) is not used during manual SYNC mode operation and the VD register update is disabled, control is lost on the fine placement of the GP signals for VSUB, MSHUT, and STROBE edges while SYNC is low.

New Serial Registers

SYNC Mode 2 and SYNC Mode 3 are controlled using the registers listed in Table 25. Note that registers for enhanced SYNC modes are located at Address 0x13 Bits [6:3].

Table 25. Registers for Enhanced SYNC Modes

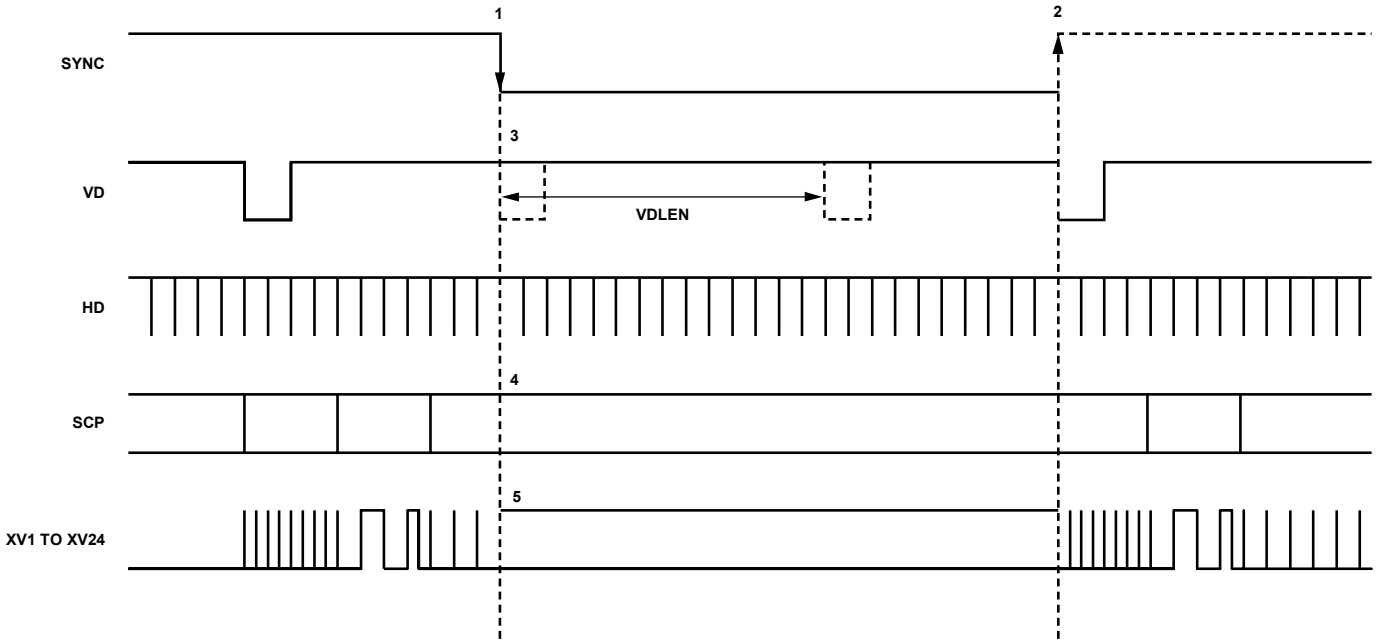
Register	Length	Description
ENH_SYNC_EN	1b	HI active to enable (default LO)
SYNC_MASK_V	1b	HI active to enable masking (default LO)
SYNC_MASK_VD	1b	HI active to enable masking (default HI)
SYNC_MASK_HD	1b	HI active to enable masking (default HI)



NOTES
1. THE SYNC RISING EDGE RESETS VD/HD AND COUNTERS TO 0.
2. SYNC POLARITY IS PROGRAMMABLE USING SYNCPOL REGISTER (ADDR 0x13).
3. DURING SYNC LOW, ALL INTERNAL COUNTERS ARE RESET AND VD/HD CAN BE SUSPENDED USING THE SYNCSUSPEND REGISTER (ADDR 0x13).
4. THE SYNC RISING EDGE CAUSES THE INTERNAL FIELD DESIGNATOR TO INCREMENT.
5. IF SYNCSUSPEND = 1, VERTICAL CLOCKS, H1 TO H4, AND RG ARE HELD AT THE SAME POLARITY SPECIFIED BY OUTCONTROL = LOW.
6. IF SYNCSUSPEND = 0, ALL CLOCK OUTPUTS CONTINUE TO OPERATE NORMALLY UNTIL SYNC RESET EDGE.

05891-083

Figure 66. Default Mode 1



[1]FALLING EDGE RESYNCS THE CIRCUIT TO THE LINE/PIXEL NUMBER 0. VD AND HD INTERNALLY RESYNC.
[2]RISING EDGE RESETS COUNTERS.
[3]VD IS DISABLED DURING SYNC. THE REGISTER IS PROGRAMMABLE.
[4]SCP, HBLK, AND CLPOB ARE HELD AT SEQ0 VALUE.
[5]XV1 TO XV24 SIGNALS ARE HELD AT THE V-OUTPUT START POLARITY.

05891-084

Figure 67. Enhanced SYNC Mode 2 with Vertical Signals Held at VTP Start Value

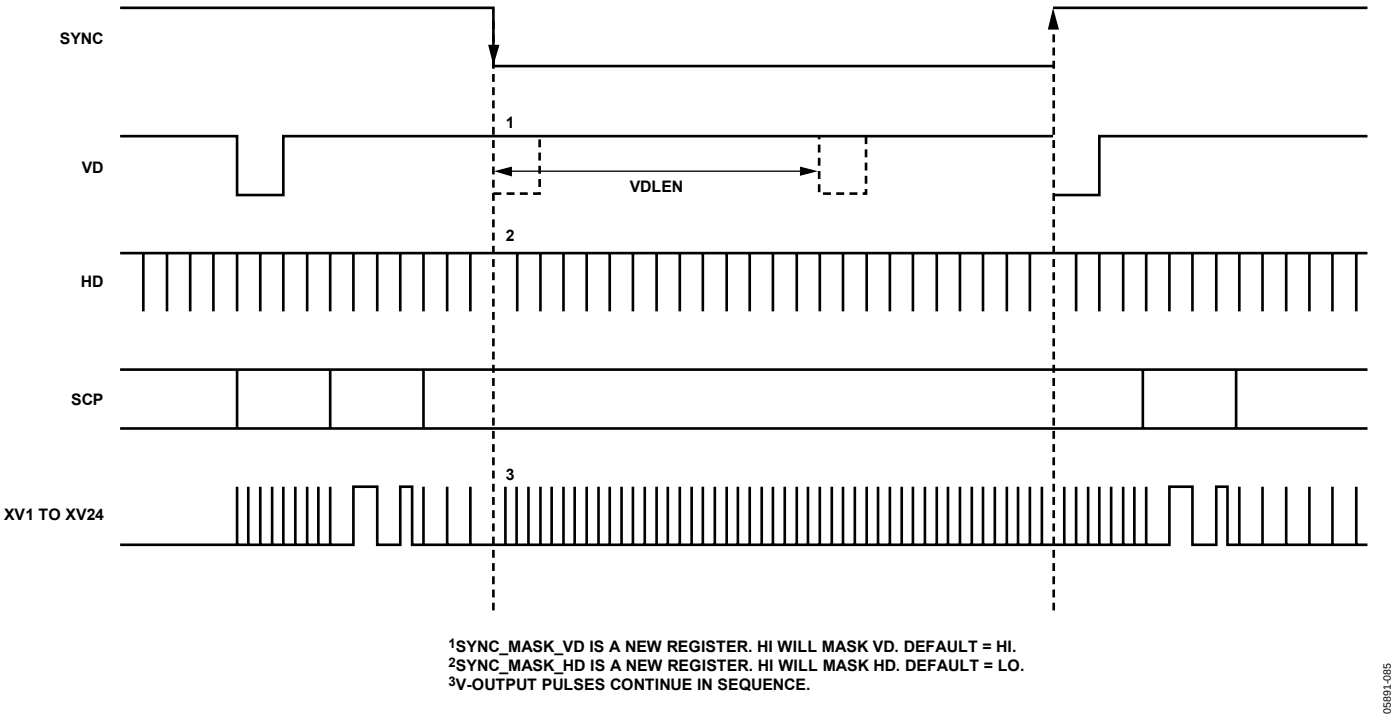


Figure 68. Enhanced SYNC Mode 3

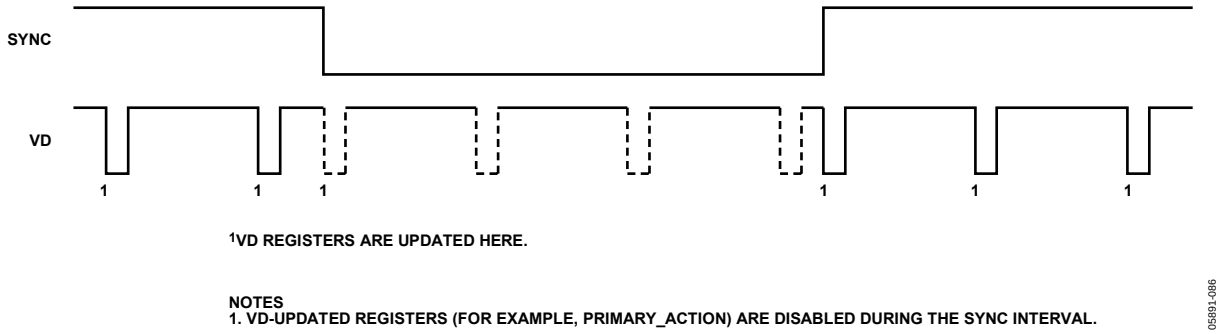


Figure 69. Register Update Behavior

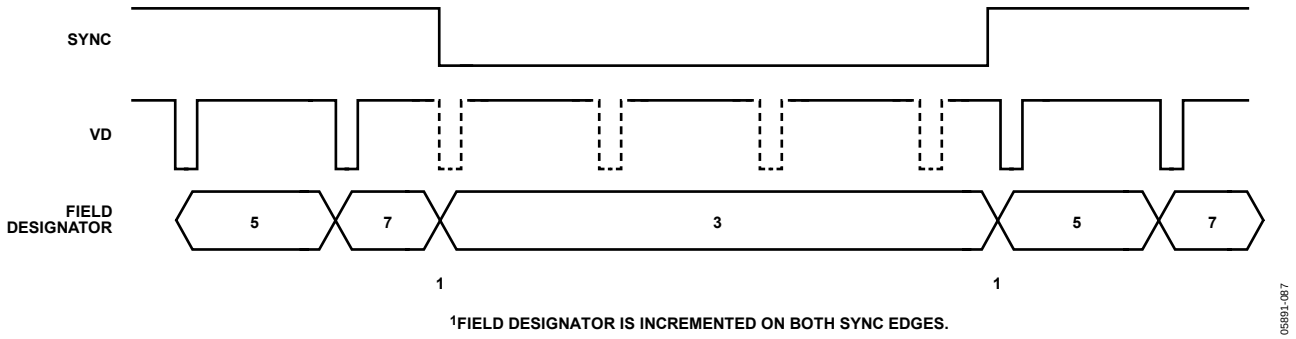
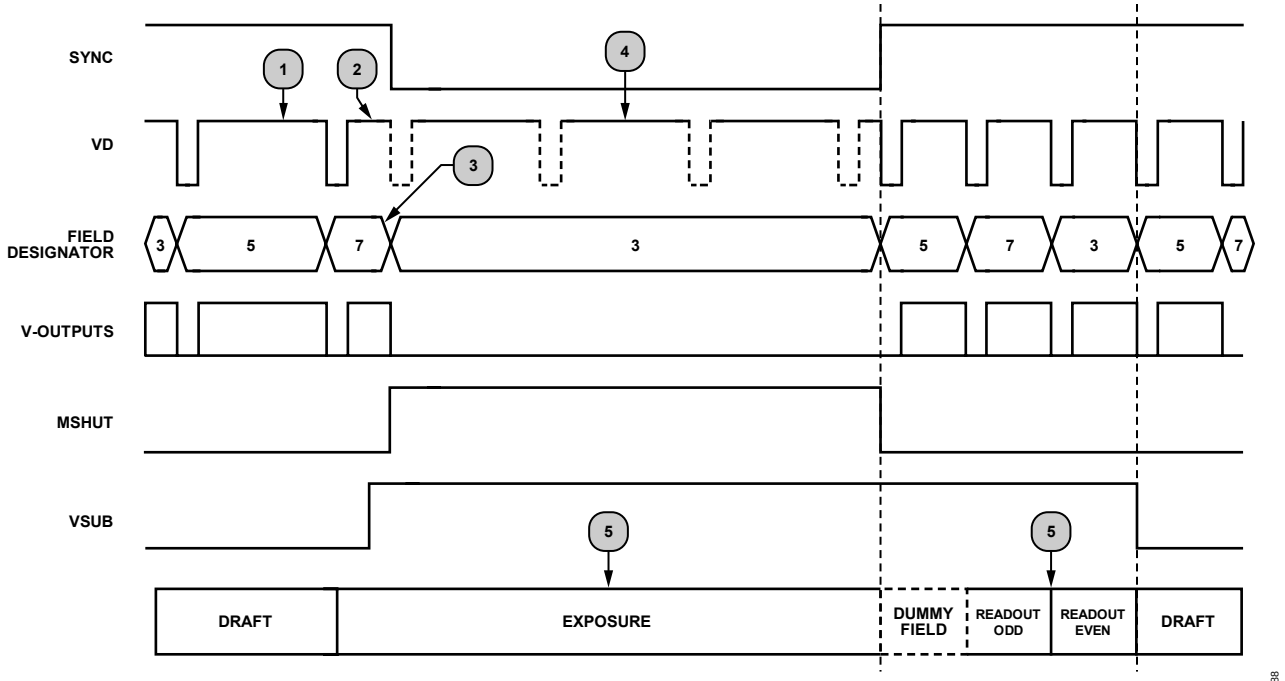


Figure 70. Special SYNC Mode Effect on Field Designator



[1]SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
[2]SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
[3]SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
[4]SEE THE SHUTTER OPERATION IN SLR MODE SECTION.
[5]SUBCK OUTPUT IS SUPPRESSED DURING EXPOSURE AND READOUT WHEN EXPOSURE TRIGGER IS USED.

Figure 71. Enhanced SYNC Mode—Manual Shutter Operation, SLR Mode

ANALOG FRONT END DESCRIPTION AND OPERATION

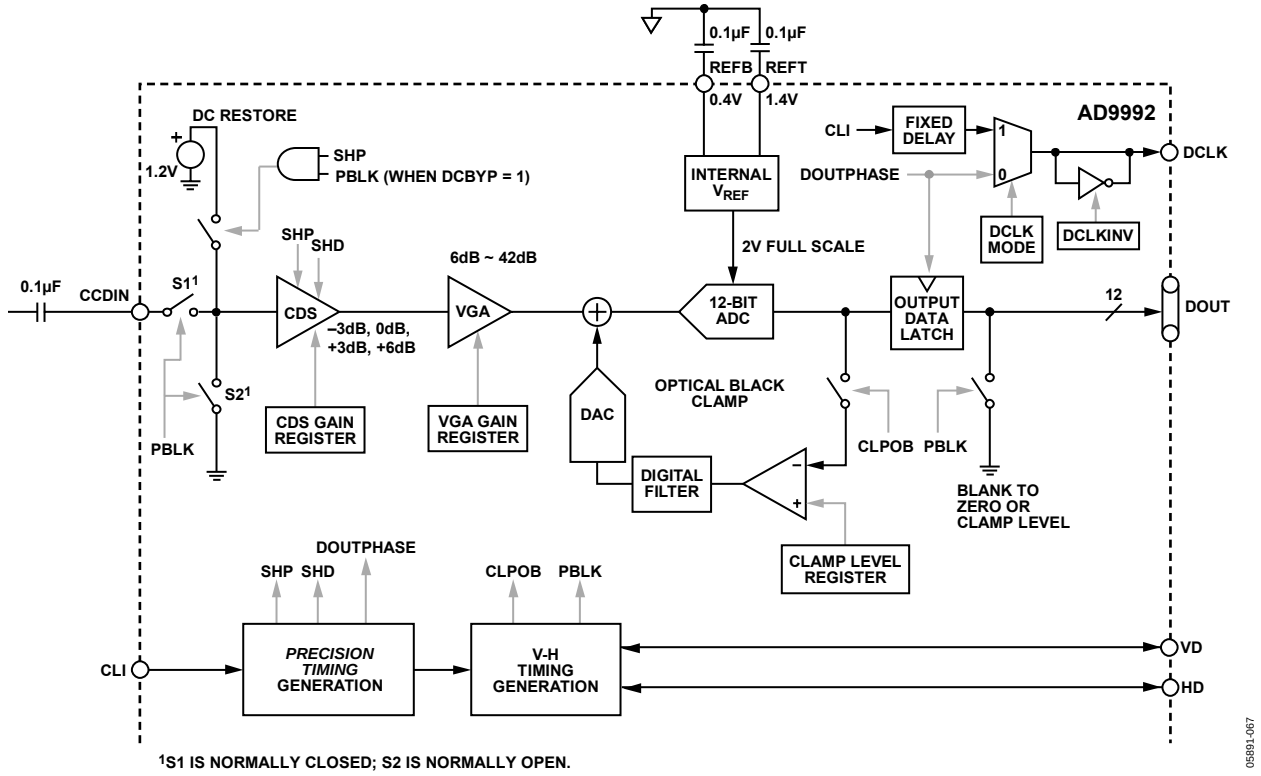


Figure 72. Analog Front-End Functional Block Diagram

The AD9992 signal processing chain is shown in Figure 72. Each processing step is essential for achieving a high quality image from the raw CCD pixel data.

DC Restore

To reduce the large dc offset of the CCD output signal, a dc restore circuit is used with an external 0.1 µF series coupling capacitor. This restores the dc level of the CCD signal to approximately 1.2 V, making it compatible with the 1.8 V core supply voltage of the AD9992. The dc restore switch is active during the SHP sample pulse time.

The dc restore circuit can be disabled when the optional PBLK signal is used to isolate large-signal swings from the CCD input (see the Analog Preblanking section). Bit 6 of AFE Register Address 0x00 controls whether the dc restore is active during the PBLK interval.

Analog Preblanking

During certain CCD blanking or substrate clocking intervals, the CCD input signal to the AD9992 can increase in amplitude beyond the recommended input range. The PBLK signal can be used to isolate the CDS input from large-signal swings. While PBLK is active (low), the CDS input is internally shorted to ground. Note that, because the CDS input is shorted during PBLK, the CLPOB pulse should not be used during the same active time as the PBLK pulse.

Correlated Double Sampler (CDS)

The CDS circuit samples each CCD pixel twice to extract the video information and to reject low frequency noise. The timing shown in Figure 19 illustrates how the two internally generated CDS clocks, SHP and SHD, are used to sample the reference level and data level of the CCD signal, respectively. The placement of the SHP and SHD sampling edges is determined by the setting of the SHPLOC and SHDLOC registers located at Address 0x37. Placement of these two clock signals is critical for achieving the best performance from the CCD.

The CDS gain is variable in three steps by using the AFE Address 0x04: −3 dB, 0 dB (default), and +3 dB. Improved noise performance results from using the +3 dB setting, but the input range is reduced (see the Analog Specifications section).

Variable Gain Amplifier

The VGA stage provides a gain range of approximately 6 dB to 42 dB, programmable with 10-bit resolution through the serial digital interface. A gain of 6 dB is needed to match a 1 V input signal with the ADC full-scale range of 2 V. When compared to 1 V full-scale systems, the equivalent gain range is 0 dB to 36 dB.

The VGA gain curve follows a linear-in-dB characteristic. The exact VGA gain is calculated for any gain register value by

$$Gain\ (\text{dB}) = (0.0358 \times Code) + 5.75$$

where *Code* is the range of 0 to 1023.

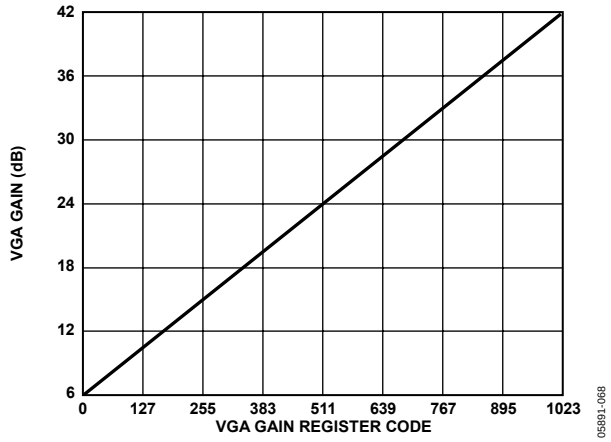


Figure 73. VGA Gain Curve

ADC

The AD9992 uses a high performance ADC architecture optimized for high speed and low power. Differential nonlinearity (DNL) performance is typically better than 0.5 LSB. The ADC uses a 2 V input range. See Figure 5 and Figure 7 for typical linearity and noise performance plots for the AD9992.

Optical Black Clamp

The optical black clamp loop is used to remove residual offsets in the signal chain and to track low frequency variations in the CCD's black level. During the optical black (shielded) pixel interval on each line, the ADC output is compared with a fixed black level reference, selected by the user in the clamp level register. The value can be programmed between 0 LSB and 255 LSB in 1023 steps. The resulting error signal is filtered to reduce noise; the correction value is applied to the ADC input through a DAC. Normally, the optical black clamp loop is turned on once per horizontal line, but this loop can be updated more slowly to suit a particular application. If external digital clamping is used during post-processing, the AD9992 optical black clamping can be disabled using Bit D2 in the AFE Register Address 0x00. When the loop is disabled, the clamp level register can still be used to provide fixed offset adjustment.

If the CLPOB loop is disabled, higher VGA gain settings reduce the dynamic range because the uncorrected offset in the signal path is amplified.

The CLPOB pulse should be aligned with the CCD's optical black pixels. It is recommended that the CLPOB pulse duration be at least 20 pixels wide. Shorter pulse widths can be used, but the ability for the loop to track low frequency variations in the black level will be reduced. See the Horizontal Clamping and Blanking section for timing examples.

Digital Data Outputs

The AD9992 digital output data is latched using the rising edge of the DOUTPHASE register value, as shown in Figure 72. Output data timing is shown in Figure 20 and Figure 21. It is also possible to leave the output latches transparent so that the data outputs are valid immediately from the ADC. Programming the AFE Register Address 0x01, Bit D1, to 1 sets the output latches to transparent. The data outputs can also be disabled (three-stated) by setting the AFE Register Address 0x01, Bit D0, to 1.

The DCLK output can be used for external latching of the data outputs. By default, the DCLK output tracks the values of the DOUTPHASE registers. By changing the DCLKMODE register, the DCLK output can be held at a fixed phase, and DOUTPHASE register values are ignored. The DCLK output can also be inverted with respect to DOUT, using the DCLKINV register bit.

The switching of the data outputs can couple noise back into the analog signal path. To minimize switching noise, it is recommended that the DOUTPHASE registers be set to the same edge as the SHP sampling location, or up to 15 edges after the SHP sampling location. Other settings can produce good results, but experimentation is necessary. It is recommended that the DOUTPHASE location not occur between the SHD sampling location and 15 edges after the SHD location. For example, if SHDLOC = 0, DOUTPHASE should be set to an edge location of 16 or greater. If adjustable phase is not required for the data outputs, the output latch can be left transparent by using Address 0x01, Bit D1.

The data output coding is normally straight binary, but the coding can be changed to gray coding by setting the AFE Register Address 0x01, Bit D2, to 1.

POWER-UP SEQUENCE FOR MASTER MODE

When the AD9992 is powered up, the following sequence is recommended (refer to Figure 74 for each step). A SYNC signal is required for master mode operation. If an external SYNC pulse is not available, it is possible to generate an internal SYNC event by writing to the SWSYNC register.

1. Turn on the power supplies for AD9992 and start the master clock, CLI.
2. Reset the internal AD9992 registers by writing 1 to the SW_RST register (Address 0x10).
3. By default, Vertical Output XV1 to Vertical Output XV24 are low. If necessary, write to the Standby3 output polarity (Address 0x26) to set different polarities for the vertical outputs in order to avoid damage to the V-driver and CCD. Write to Address 0x1C to configure each V-output as a vertical transfer clock (XV) or sensor pulse (VSG).
4. If using an external V-driver in conjunction with the AD9992, power up the V-driver supplies, VH and VL, anytime after Step 3 is complete to set the proper polarities.
5. Load the required registers to configure the necessary vertical timing, horizontal timing, high speed timing, and shutter timing. Set the recommended start-up address, 0xD8, to 0x888.
6. To place the part into normal power operation, write 0x04 to Register Address 0x00. This sets the STANDBY register (AFE Register Address 0x00, Bits [1:0]) to normal operation and enables the OB clamp (AFE Register Address 0x00, Bit 2). If the CLO output is being used to drive a crystal, also power up the CLO oscillator by writing 1 to Address 0x15.
7. By default, the internal timing core is held in a reset state, with TGCORE_RSTB register = 0. Write 1 to the TGCORE_RSTB register (Address 0x14) to start the internal timing core operation. Note that, if a 2× clock is used for the CLI input, the CLIDIVIDE register (0x0D) should be set to 1 before resetting the timing core.
8. Configure the AD9992 for master mode timing by writing 1 to the MASTER register (Address 0x20).
9. Write 1 to the OUTCONTROL register (Address 0x11). This allows the outputs to become active after the next SYNC rising edge. Normally OUTCONTROL takes effect after the next VD edge; however, because the part is just being powered up, there is no VD edge until the rising edge of the SYNC signal.
10. Generate a SYNC event. If SYNC is high at power-up, bring the SYNC input low for a minimum of 100 ns, and then bring SYNC high again. This causes the internal counters to reset and starts VD/HD operation. The first VD/HD edge allows VD-updated register updates to occur, including OUTCONTROL to enable all outputs. If a hardware SYNC is not available, the SWSYNC register (Address 0x13, Bit 14) can be used to initiate a SYNC event.

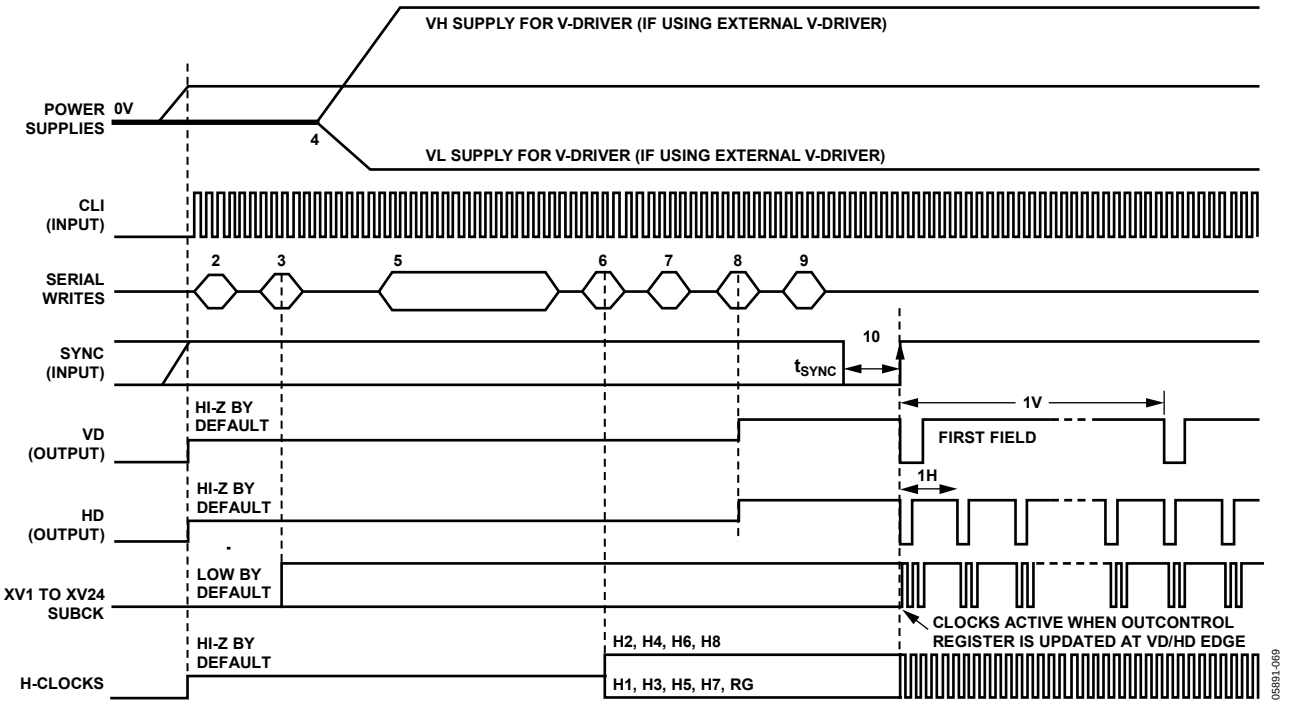


Figure 74. Recommended Power-Up Sequence and Synchronization, Master Mode

Table 26. Power-Up Register Write Sequence

Address	Data	Description
0x10	0x01	Resets all registers to default values
0x26	User-defined	Standby3 vertical output polarities
0x20 to 0xFFF	User-defined	Horizontal, vertical, shutter timing
0xD8	0x888	Configures start-up register
0x00	0x04	Powers up the AFE, enables OB clamp
0x15	0x01	Starts CLO oscillator (if using crystal)
0x14	0x01	Starts internal timing core
0x20	0x01	Configures for master mode
0x11	0x01	Enables all outputs after SYNC
0x13	0x4XX1	SWSYNC (if using software SYNC)

Using the SWSYNC Register

If an external SYNC pulse is not available, it is possible to generate an internal SYNC in the AD9992 by writing 1 to the SWSYNC register (Address 0x13, Bit 14). If the software SYNC option is used, the SYNC input (Pin D3) should be low (V_{SS}) during power-up. The SYNCENABLE register (Address 0x13, Bit 0) should be set high.

SYNC During Master Mode Operation

The hardware SYNC input can be used anytime during operation to synchronize the AD9992 counters with external timing, as shown in Figure 75. The operation of the digital outputs can be suspended during the SYNC operation by setting the SYNCSUSPEND register (Address 0x13, Bit 2) to 1. If SYNCSUSPEND = 1, the polarities of the outputs are held at the same state as OUTCONTROL = low, as shown in Table 27.

Power-Up and Synchronization in Slave Mode

The power-up procedure for slave mode operation is the same as the procedure for master mode operation with two exceptions:

- Eliminate Step 8. Do not write the part into master mode.
- No SYNC pulse is required in slave mode. Substitute Step 10 with starting the external VD and HD signals. This synchronizes the part, allows the register updates, and starts the timing operation.

When the AD9992 is used in slave mode, the VD/HD inputs are used to synchronize the internal counters. After a falling edge of VD, there is a latency of 36 master clock CLI edges after the falling edge of HD until the internal H-counter is reset. The reset operation is shown in Figure 76.

Additional Restrictions in Slave Mode

When operating in slave mode, the following restrictions should be noted:

- The HD falling edge should be located in the same CLI clock cycle as the VD falling edge or later than the VD falling edge. The HD falling edge should not be located within five cycles prior to the VD falling edge.
- If possible, all start-up serial writes should be performed with VD and HD disabled. This prevents unknown behavior caused by partial updating of registers before all information is loaded.

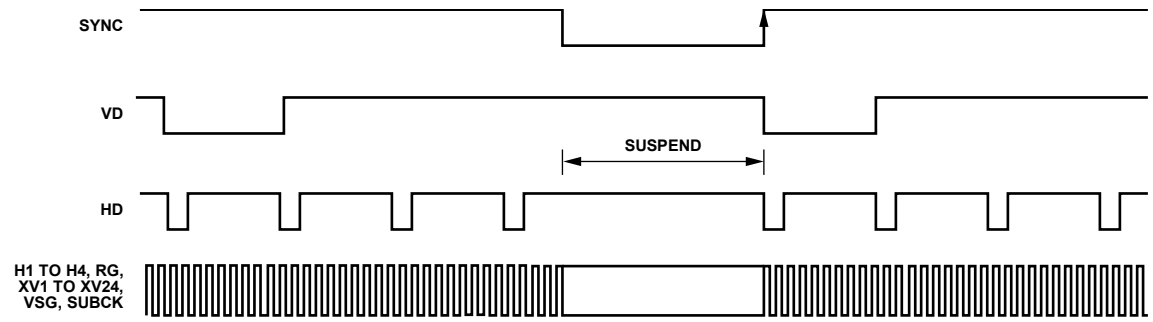
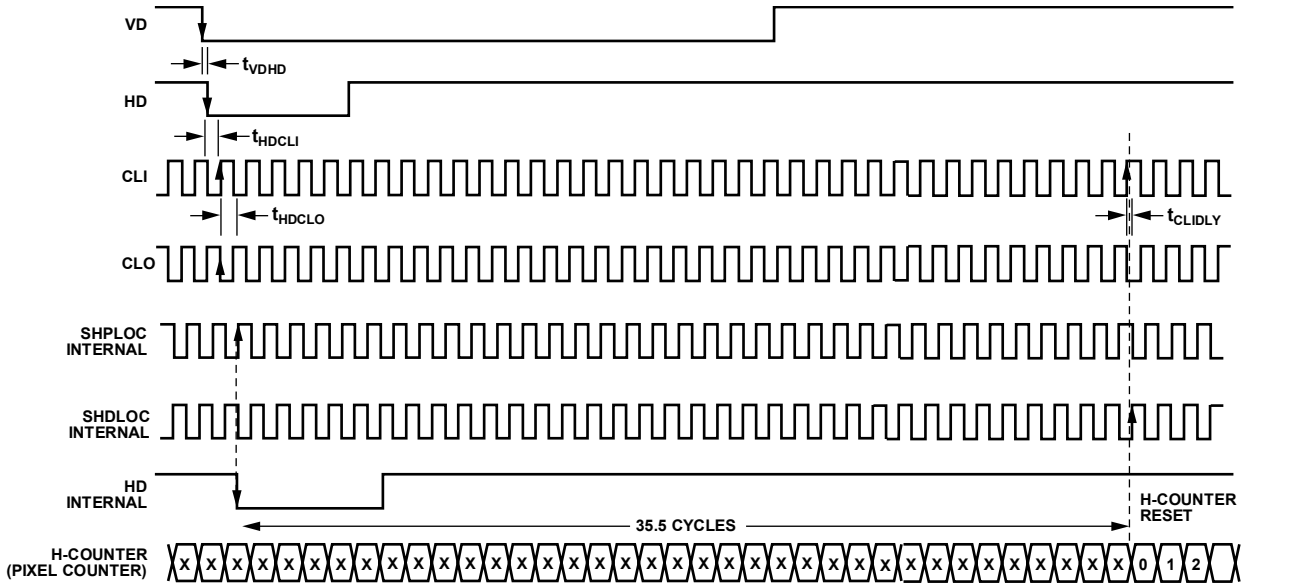


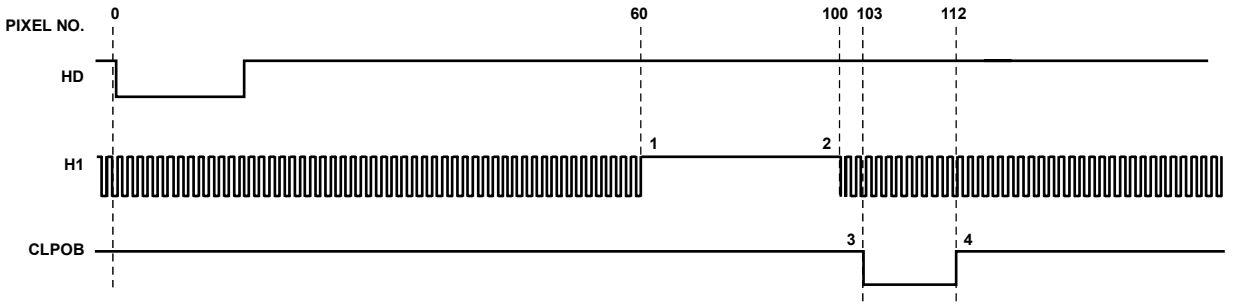
Figure 75. SYNC Timing to Synchronize the AD9992 with External Timing



NOTES:
1. EXTERNAL HD FALLING EDGE IS LATCHED BY CLI RISING EDGE, THEN LATCHED AGAIN BY SHPLOC (INTERNAL SAMPLING EDGE).
2. INTERNAL H-COUNTER IS ALWAYS RESET 35.5 CLOCK CYCLES AFTER THE INTERNAL HD FALLING EDGE, AT SHDLOC (INTERNAL SAMPLING EDGE).
3. DEPENDING ON THE VALUE OF SHPLOC, H-COUNTER RESET CAN OCCUR 36 OR 37 CLI CLOCK EDGES AFTER THE EXTERNAL HD FALLING EDGE.
4. SHPLOC = 32, SHDLOC = 0 IS SHOWN IN ABOVE EXAMPLE. IN THIS CASE, THE H-COUNTER RESET OCCURS 36 CLI RISING EDGES AFTER HD FALLING EDGE.
5. HD FALLING EDGE SHOULD OCCUR COINCIDENT WITH VD FALLING EDGE (WITHIN SAME CLI CYCLE) OR AFTER VD FALLING EDGE. HD FALLING EDGE SHOULD NOT OCCUR WITHIN 1 CYCLE IMMEDIATELY BEFORE VD FALLING EDGE.

05891-094

Figure 76. External VD/HD and Internal H-Counter Synchronization, Slave Mode



	MASTER MODE	SLAVE MODE
[1]HBLKTOG1	60	(60 – 36) = 24
[2]HBLKTOG2	100	(100 – 36) = 64
[3]CLPOB_TOG1	103	(103 – 36) = 67
[4]CLPOB_TOG2	112	(112 – 36) = 76

05891-072

Figure 77. Example of Slave Mode Register Setting to Obtain Desired Toggle Positions

Vertical Toggle Position Placement Near Counter Reset

An additional consideration during the reset of the internal counters is the vertical toggle position placement. Before the internal counters are reset, there is a region of 36 pixels during which no toggle positions should be programmed.

As shown in Figure 78 for master mode, the last 36 pixels before the HD falling edge must not be used for toggle position placement of the V, VSG, SUBCK, HBLK, PBLK, or CLPOB pulses.

Figure 79 shows the same example for slave mode. The same restriction applies: the last 36 pixels before the counters are reset cannot be used. However, in slave mode, the counter reset is delayed with respect to VD/HD placement, so the inhibited area is different than it is in master mode.

It is recommended that Pixel Location 0 not be used for any of the toggle positions for the VSG and SUBCK pulses.

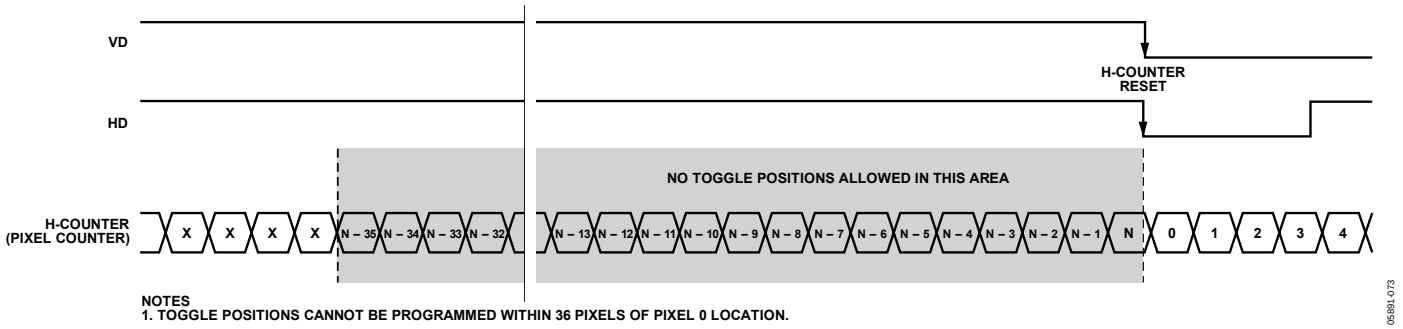


Figure 78. Toggle Position Inhibited Area—Master Mode

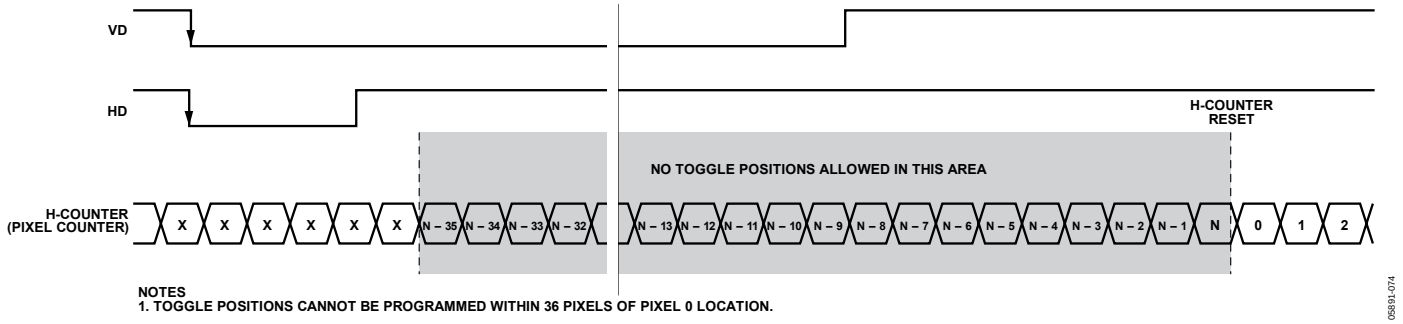


Figure 79. Toggle Position Inhibited Area—Slave Mode

STANDBY MODE OPERATION

The AD9992 contains three standby modes to optimize the overall power dissipation in a particular application. Bits [1:0] of Address 0x00 control the power-down state of the device:

- STANDBY [1:0] = 0 = normal operation (full power)
- STANDBY [1:0] = 1 = Standby1 mode
- STANDBY [1:0] = 2 = Standby2 mode
- STANDBY [1:0] = 3 = Standby3 mode (lowest power)

Table 27 summarizes the operation of each power-down mode. The OUTCONTROL register takes priority over the Standby1 and Standby2 modes in determining the digital output states, but Standby3 mode takes priority over OUTCONTROL. Standby3 has the lowest power consumption and even shuts down the crystal oscillator circuit between CLI and CLO. Therefore, if CLI and CLO are being used with a crystal to generate the master clock, this circuit is powered down and there is no clock signal. When returning from Standby3 mode to normal operation, the timing core must be reset at least 500 µs after the STANDBY register is written to. This allows sufficient time for the crystal circuit to settle.

The vertical outputs can also be programmed to hold a specific value during the Standby3 mode by using Address 0x26. This register is useful during power-up if different polarities are required by the V-driver and CCD to prevent damage when VH and VL areas are applied. The polarities for Standby1 mode and Standby2 mode are also programmable, using Address 0x25. OUTCONTROL = low also uses the same polarities programmed for Standby1 and Standby2 modes in Address 0x25. The GPO polarities are programmable using Address 0x27.

Note that the GPO outputs are high-Z by default at power-up until Address 0x78 is used to select them as outputs.

CLI FREQUENCY CHANGE

If the input clock CLI is interrupted or changed to a different frequency, the timing core must be reset for proper operation. After the CLI clock settles to the new frequency, or the previous frequency is resumed, write 0 and then 1 to the TGCORE_RSTB register (Address 0x14). This guarantees that the timing core operates properly.

Table 27. Standby Mode Operation (Standby Polarities for XV, XSUBCK, GPO Outputs Are Programmable)

I/O Block	Standby3 (Default)[1, 2]	OUTCONTROL = Low[2]	Standby2[3, 4]	Standby1[3, 4]
AFE	Off	No change	Off	Only REFT, REFB on
Timing Core	Off	No change	Off	On
CLO Oscillator	Off	No change	Off	On
CLO	Low	No change	Low	Running
H1	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H2	High-Z	High	High (4.3 mA)	High (4.3 mA)
H3	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H4	High-Z	High	High (4.3 mA)	High (4.3 mA)
H5	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H6	High-Z	High	High (4.3 mA)	High (4.3 mA)
H7	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
H8	High-Z	High	High (4.3 mA)	High (4.3 mA)
HL	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
RG	High-Z	Low	Low (4.3 mA)	Low (4.3 mA)
VD	Low	$\overline{\text{VDHDPOL}}$ value	$\overline{\text{VDHDPOL}}$ value	Running
HD	Low	$\overline{\text{VDHDPOL}}$ value	$\overline{\text{VDHDPOL}}$ value	Running
DCLK	Low	Running	Low	Running
DOUT	Low	Low	Low	Low
XV1 to XV24	Low	Low	Low	Low
XSUBCK	Low	Low	Low	Low
GPO1 to GPO8	Low	Low	Low	Low

[1] To exit Standby3, write 00 to STANDBY (Address 0x00, Bits [1:0]), and then reset the timing core after 500 µs to guarantee proper settling of the oscillator and external crystal.
[2] Standby3 mode takes priority over OUTCONTROL for determining the output polarities.
[3] These polarities assume OUTCONTROL = high because OUTCONTROL = low takes priority over Standby1 and Standby2.
[4] Standby1 and Standby2 set H and RG drive strength to minimum value (4.3 mA).

CIRCUIT LAYOUT INFORMATION

The PCB layout is critical in achieving good image quality from the AD9992. All of the supply pins, particularly the AVDD, TCVDD, RGVDD, and HVDD supplies, must be decoupled to ground with good quality high frequency chip capacitors. The decoupling capacitors should be located as close as possible to the supply pins and should have a very low impedance path to a continuous ground plane. If possible, there should be a 4.7 µF or larger value bypass capacitor for each main supply—AVDD, HVDD, and DRVDD—although this is not necessary for each individual pin. In most applications, the supply for RGVDD and HVDD is shared, which can be done as long as the individual supply pins are separately bypassed with 0.1 µF capacitors. A separate 3 V supply can also be used for DRVDD, but this supply pin should still be decoupled to the same ground plane as the rest of the chip. A separate ground for DRVSS is not recommended.

The analog bypass pins (REFT and REFB) should be carefully decoupled to ground as close as possible to their respective pins. The analog input (CCDIN) capacitor should be located close to the CCDIN pin.

The H1 to H8, HL, and RG traces should be designed to have low inductance to minimize distortion of the signals. The complementary signals, H1/H3/H5/H7 and H2/H4/H6/H8, should be routed as close together and as symmetrically as possible to minimize mutual inductance. Heavier PCB traces are recommended because of the large transient current demand on H1 to H8 by the CCD. If possible, physically locating the AD9992 closer to the CCD reduces the inductance on these lines. As usual, the routing path should be as direct as possible from the AD9992 to the CCD.

It is recommended that all H1 to H8 outputs on the AD9992 be used together for maximum flexibility in drive strength settings. A typical CCD with H1 and H2 inputs only should have the AD9992 H1, H3, H5, and H7 outputs connected together to drive the CCD's H1, and H2, H4, H6, and H8 outputs connected together to drive the CCD's H2. Similarly, a CCD with H1, H2, H3, and H4 inputs should have the following:

- H1 and H3 connected to the CCD's H1.
- H2 and H4 connected to the CCD's H2.
- H5 and H7 connected to the CCD's H3.
- H6 and H8 connected to the CCD's H4.

TYPICAL 3 V SYSTEM

The AD9992 typical circuit connections for a 3 V system are shown in Figure 80. This application uses an external 3.3 V supply, which is connected to the AD9992 LDO input. The LDO is configured to output 1.8 V for the AD9992 core supply by connecting the LDO1P8EN pin to 3.3 V and the LDO3P2EN pin to ground. The LDOOUT and SENSE pins are shorted together and used to supply 1.8 V to the AVDD, TCVDD, and DVDD pins.

TYPICAL 1.8 V SYSTEM

The internal LDO can be disabled by tying the LDO pins to ground (LDOIN, LDO1P8EN, LDO3P2EN, LDOOUT, and SENSE). In this case, an external 1.8 V regulator is required to supply 1.8 V to the AVDD, TCVDD, and DVDD pins.

All of the AD9992 remaining supplies can be directly supplied with 1.8 V. The internal charge pump (CP) can be used to generate 3.3 V for the H and RG supplies.

The AD9992 typical circuit connections for a 1.8 V system are shown in Figure 81.

EXTERNAL CRYSTAL APPLICATION

The AD9992 contains an on-chip oscillator for driving an external crystal. Figure 82 shows an example application using a typical 27 MHz crystal. For the exact values of the external resistors and capacitors, it is best to consult the crystal manufacturer's data sheet.

Note that a 2× crystal is not recommended for use with the CLO oscillator circuit. The crystal frequency should not exceed 40 MHz.

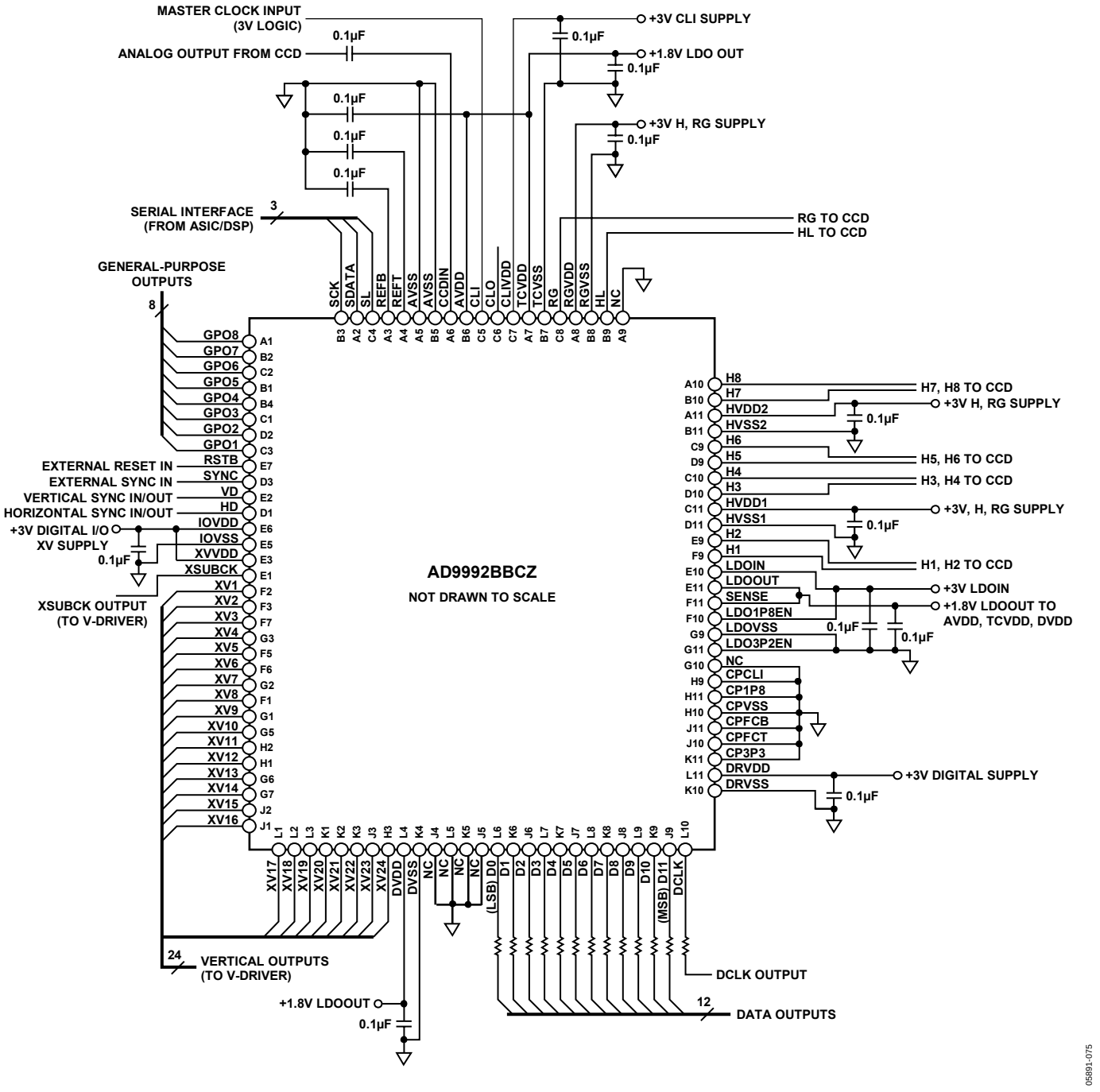


Figure 80. Typical 3 V Circuit Configuration

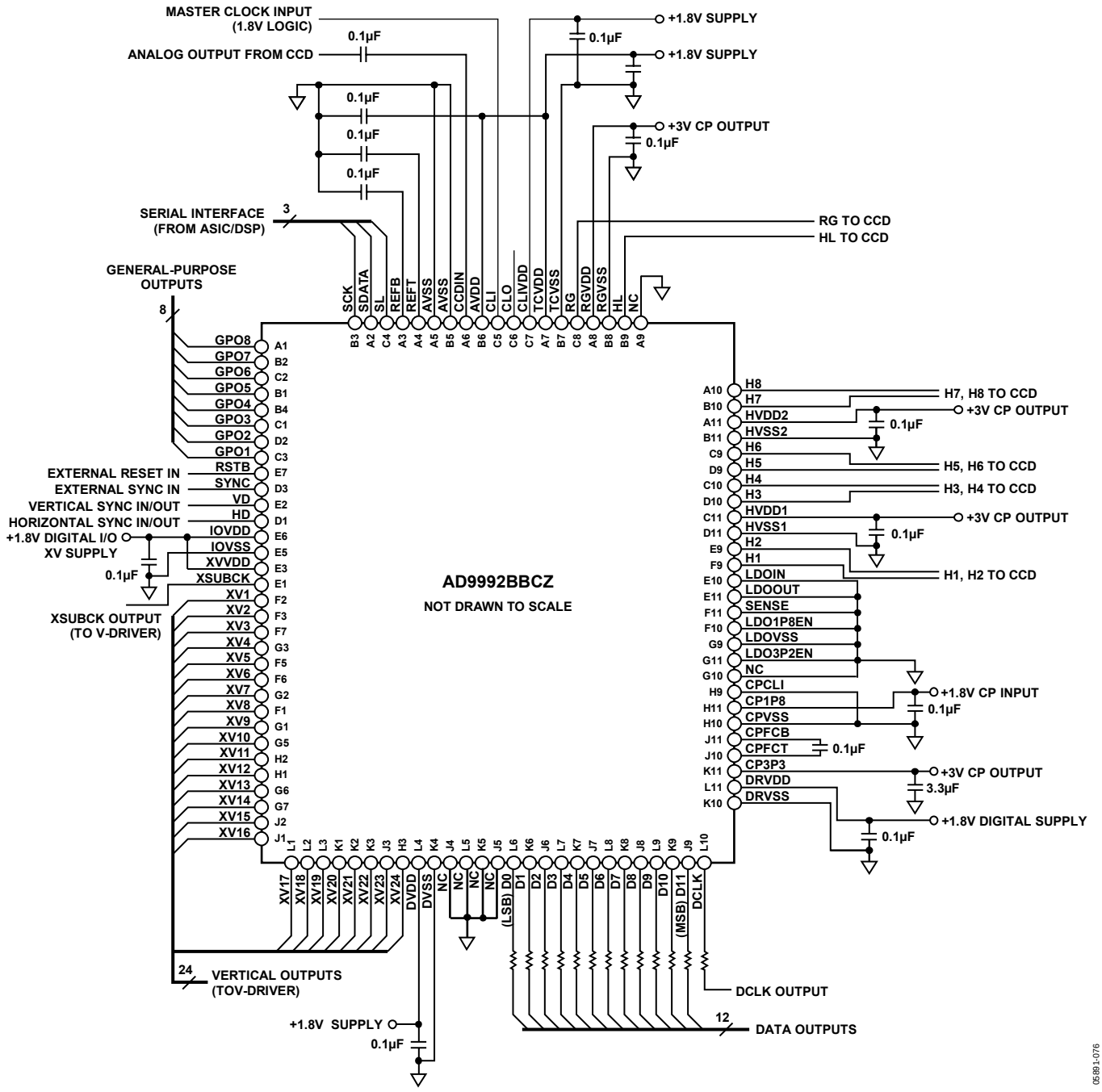


Figure 81. Typical 1.8 V Circuit Configuration Using Charge Pump for HVDD and RGVDD

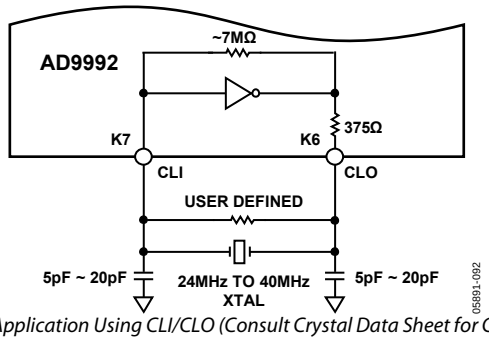


Figure 82. Crystal Application Using CLI/CLO (Consult Crystal Data Sheet for Component Values)

SERIAL INTERFACE TIMING

The internal registers of the AD9992 are accessed through a 3-wire serial interface. Each register consists of a 12-bit address and a 28-bit data-word. Both the 12-bit address and 28-bit data-word are written starting with the LSB. To write to each register, a 40-bit operation is required, as shown in Figure 83. Although many registers are fewer than 28 bits wide, all 28 bits must be written for each register. For example, if the register is only 20 bits wide, the upper eight bits are don't cares and must be filled with 0s during the serial write operation. If fewer than 28 data bits are written, the register is not updated with new data.

Figure 84 shows a more efficient way to write to the registers, using the AD9992 address autoincrement capability. Using this method, the lowest desired address is written first, followed by multiple 28-bit data-words. Each new 28-bit data-word is automatically written to the next highest register address. By eliminating the need to write each 12-bit address, faster register loading is achieved. Continuous write operations can be used starting with any register location.

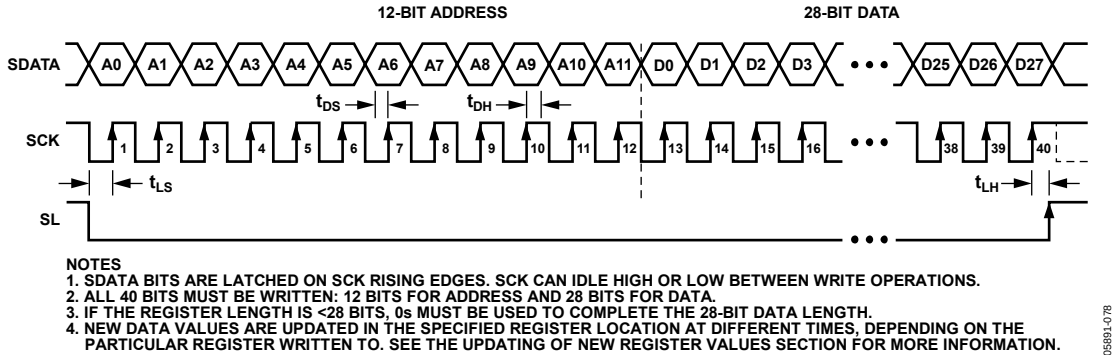


Figure 83. Serial Write Operation

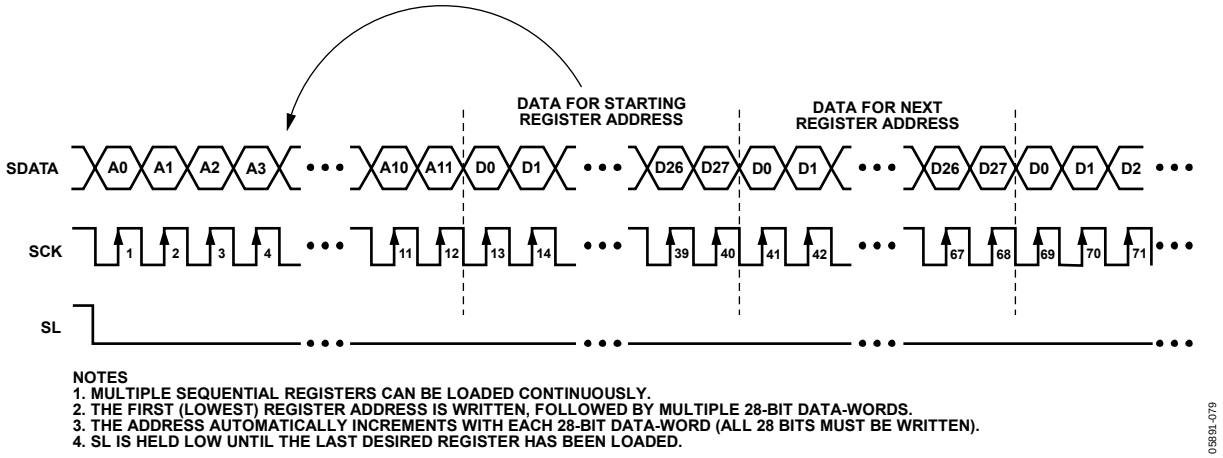


Figure 84. Continuous Serial Write Operation

LAYOUT OF INTERNAL REGISTERS

The AD9992 address space is divided into two register areas, as illustrated in Figure 85. In the first address space, Address 0x00 to Address 0xFF contain the registers for the AFE, miscellaneous, VD/HD, I/O and CP, timing core, shutter and GPO, mode, and update control functions. The second address space, beginning at Address 0x800, consists of the V-pattern groups, V-sequences, and field registers. This is a configurable set of registers; the user can decide how many V-pattern groups, V-sequences, and fields are used in a particular design. Therefore, the addresses for these registers vary, depending on the number of V-patterns and V-sequences chosen.

Address 0x28 specifies the total number of V-pattern groups and V-sequences used. The starting address for the V-pattern groups is always 0x800. The starting address for the V-sequences is based on the number of V-pattern groups used, with each V-pattern group occupying 48 register addresses. The starting address for the field registers depends on both the number of V-pattern groups and the number of V-sequences. Each V-sequence occupies 40 register addresses, and each field occupies 16 register addresses.

The starting address for the V-sequences is equal to 0x800 plus the number of V-pattern groups times 48. The starting address for the fields is equal to the starting address of the V-sequences plus the number of V-sequences times 40. The V-pattern, V-sequence and field registers must always occupy a continuous block of addresses.

Figure 86 shows an example in which three V-pattern groups, four V-sequences, and two fields are used. The starting address for the V-pattern groups is always 0x800. Because VPATNUM = 3, the V-pattern groups occupies 144 address locations. The start of the V-sequence registers is 0x890 (that is, 0x800 + 144). With VSEQNUM = 4, the V-sequences occupy 160 address locations. Therefore, the field registers begin at 0x930 (that is, 0x890 + 160).

The AD9992 address space contains many unused addresses. Undefined addresses between Address 0x00 and Address 0xFF should not be written to; otherwise, the AD9992 may operate incorrectly. Continuous register writes should be performed carefully so that undefined registers are not written to.

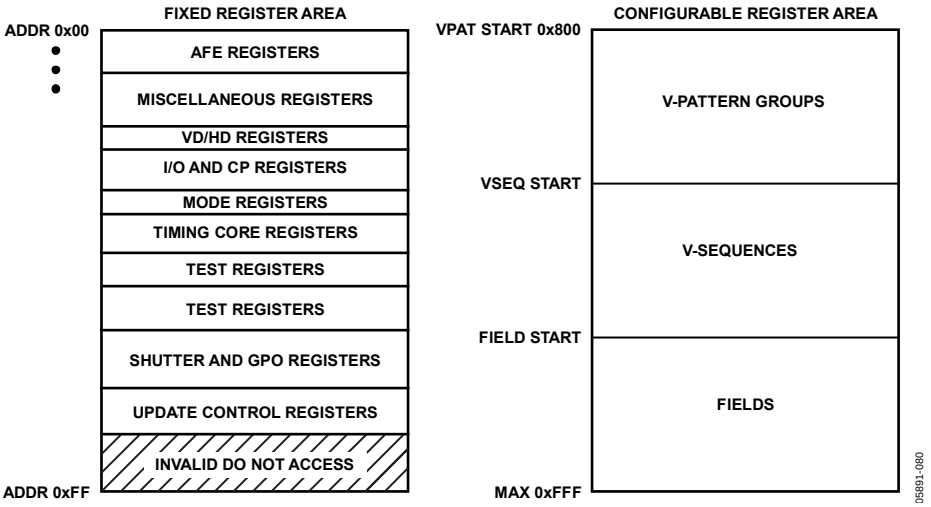


Figure 85. Layout of AD9992 Registers

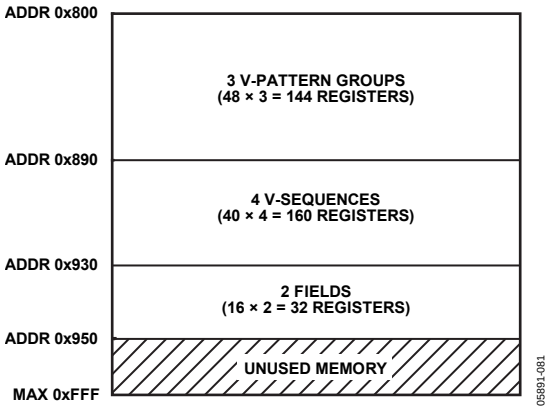


Figure 86. Example Register Configuration

UPDATING NEW REGISTER VALUES

The AD9992 internal registers are updated at different times, depending on the particular register. Table 28 summarizes the four register update types: SCK, VD, SG-Line, and SCP. Tables in the Complete Register Listing section also contain an Update Type column that identifies when each register is updated.

- SCK Updated—As soon as the 28th data bit (D27) is clocked in, some registers are immediately updated. These registers are used for functions that do not require gating with the next VD boundary, such as power-up and reset functions.
- VD Updated—More registers are updated at the next VD falling edge. By updating these values at the next VD edge, the current field is not corrupted and the new register values are applied to the next field. The VD update can be further delayed past the VD falling edge by using the UPDATE register (Address 0x17). This delays the VD-updated register updates to any HD line in the field. Note that the field registers are not affected by the UPDATE register.
- SG-Line Updated—A few of the shutter registers are updated at the HD falling edge at the start of the SG active line. These registers control the SUBCK signal so that the SUBCK output is not updated until the SG line occurs.
- SCP Updated—At the next SCP where they are used, the V-pattern group and V-sequence registers are updated. For example, in Figure 87 this field has selected Region 1 to use VSEQ3 for the vertical outputs. This means that a write to any of the VSEQ3 registers, or any of the V-pattern group registers, which are referenced by VSEQ3, updates at SCP1. If multiple writes are made to the same register, the last one done before SCP1 is the one that is updated. Likewise, register writes to any VSEQ5 registers are updated at SCP2; register writes to any VSEQ8 registers are updated at SCP3.

Caution

It is recommended that the registers in the configurable address area not be written within 36 pixels of any HD falling edge where a sequence change position (SCP) occurs. See Figure 78 and Figure 79 for examples of what this inhibit area looks like in master and slave modes. This restriction applies to the V-pattern, V-sequence, and field registers. As shown in Figure 87, writing to these registers before the VD falling edge typically avoids loading these registers during SCP locations.

Table 28. Register Update Locations

Update Type	Description
SCK	When the 28th data bit (D27) is clocked in, the register is immediately updated.
VD	Register is updated at the VD falling edge. VD-updated registers can be delayed further by using the UPDATE register at Address 0x17. FIELD registers are not affected by the UPDATE register.
SG-Line	Register is updated at the HD falling edge at the start of the SG-active line.
SCP	Register is updated at the next SCP when the register is used.

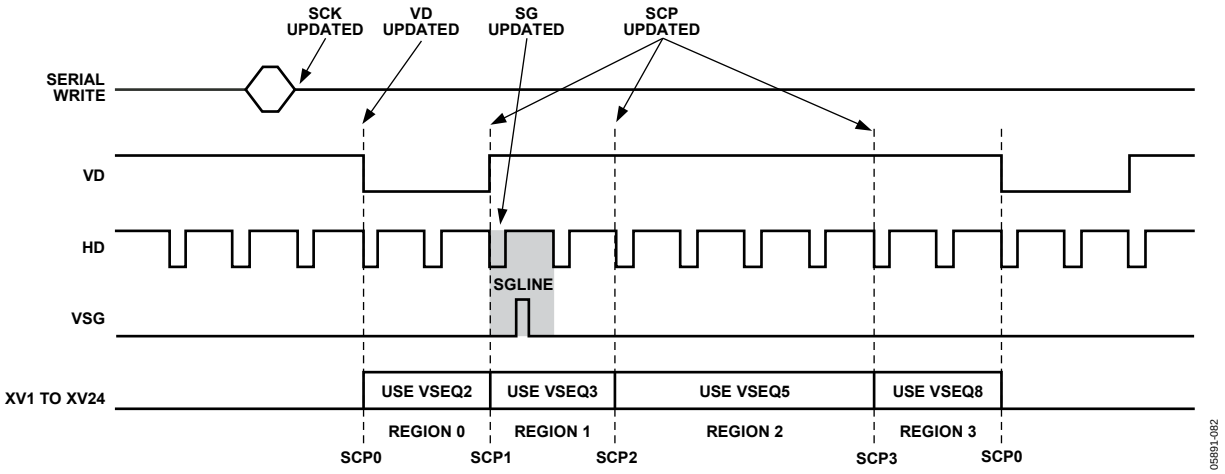


Figure 87. Register Update Locations (See Table 28 for Definitions)

COMPLETE REGISTER LISTING

When an address contains fewer than 28 data bits, all remaining bits must be written as 0s.

Table 29. AFE Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x00	[1:0]	3	SCK	STANDBY	Standby modes: 0: Normal operation. 1: Standby1 mode. 2: Standby2 mode. 3: Standby3 mode.
	[2]	1		CLPENABLE	0: Disable OB clamp. 1: Enable OB clamp.
	[3]	0		CLPSPEED	0: Select normal OB clamp settling. 1: Select fast OB clamp settling.
	[4]	0		FASTUPDATE	0: Ignore CDS gain. 1: Very fast clamping when CDS gain is updated.
	[5]	0		PBLK_LVL	0: Blank data outputs to 0 during PBLK. 1: Blank data outputs to programmed clamp level during PBLK.
	[6]	0		DCBYP	0: Enable input dc restore circuit during PBLK. 1: Disable input dc restore circuit during PBLK.
0x01	[0]	0	SCK	DOUTDISABLE	0: Data outputs are driven. 1: Data outputs are three-stated.
	[1]	0		DOUTLATCH	0: Latch data outputs using the rising edge of DOUTPHASEP (DOUTPHASEP register setting). 1: Output latch is transparent.
	[2]	0		GRAY_EN	1: Enable gray encoding of the digital data outputs.
	[3]	1		TEST	Set to 0.
0x02	[0]	0	SCK	TEST	Do not access, or set to 0.
0x03	[23:0]	FFFFFF	SCK	TEST	Do not access, or set to 0xFFFFFF.
0x04	[2:0]	0	VD	CDSGAIN	CDS gain setting: 0: −3 dB. 4: 0 dB. 6: +3 dB. 7: +6 dB. All other values are invalid.
0x05	[9:0]	F	VD	VGAGAIN	VGA gain, 6 dB to 42 dB (0.035 dB per step).
0x06	[9:0]	1EC	VD	CLAMPLEVEL	Optical black clamp level, 0 to 1023 LSB (1 LSB per step).
0x0D	[0]	0	VD	CLIDIVIDE	0: No division of CLI. 1: Divide CLI input frequency by 2.

Table 30. Miscellaneous Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x10	[0]	0	SCK	SW_RST	Software reset. Bit self-clears to 0 when a reset occurs. 1: Reset Address 0x00 to Address 0xFF to default values.
0x11	[0]	0	VD	OUTCONTROL	0: Make all outputs dc inactive. 1: Enable outputs at next VD edge.
0x12	[0]	0	SCK	RSTB_EN	1: Configure SYNC pin as RSTB input signal.
	[4:1]	0		TEST	Test mode only. Must be set to 0.
0x13	[0]	1	SCK	SYNCENABLE	1: External synchronization enable (configures Pin D3 as an input).
	[1]	0		SYNCPOL	SYNC active polarity.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
	[2]	0		SYNCSUSPEND	Suspend clocks during SYNC active pulse: 0: Do not suspend. 1: Suspend.
	[3]	0		ENH_SYNC_EN	1: Enable enhanced sync/shutter operations.
	[4]	0		SYNC_MASK_HD	1: Mask HD during SYNCSUSPEND.
	[5]	1		SYNC_MASK_VD	1: Mask VD during SYNCSUSPEND.
	[6]	1		SYNC_MASK_V	1: Mask XV outputs during SYNCSUSPEND.
	[7]	0		SHADOW_EN	1: Enable use of shadow registers.
	[12:8]	0		TEST	Test mode only. Must be set to 0.
	[13]	0		UPDATE_SHADOW	1: Writes to shadow bits affect shadow registers, not primary.
	[14]	0		SWSYNC	1: Initiate software SYNC event (self-clears to 0 after SYNC).
0x14	[0]	0	SCK	TGCORE_RSTB	Timing core reset bar. 0: reset TG core; 1: resume operation.
0x15	[0]	0	SCK	OSC_RSTB	CLO oscillator reset bar: 0: Oscillator in power-down state. 1: Resume oscillator operation.
0x16	[27:0]	0	SCK	TEST	Test mode only. Must be set to 0.
0x17	[12:0]	0	SCK	UPDATE	Serial update line. Sets the line (HD) within the field to update the VD-updated registers.
	[13]	0		PREVENTUP	Prevents the update of the VD-updated registers: 0: Normal update. 1: Prevent update of VD-updated registers.
	[14]	0		SYNC_RST_SHUTEN	1: Enable reset of the shutter control after SYNC operation occurs.
	[15]	0		REG_RST_SHUT	1: Forces shutter control to reset.
	[16]	0		GPO_RST_SYNC	1: Reset shutter and GPO control at SYNC operation.
	[17]	0		GPO_LINE_COUNT_OFFSET	0: First line in a field is considered Line 1 for GPOs. 1: First line in a field is considered Line 0 for GPOs.
0x18	[27:0]	0	SCK	TEST	Test mode only. Must be set to 0.
0x19	[27:0]	0	SCK	TEST	Test mode only. Must be set to 0.
0x1A	[27:0]	0	SCK	TEST	Test mode only. Must be set to 0.
0x1B	[27:0]	A	SCK	TEST	Test mode only. Must be set to 0xA.
0x1C	[23:0]	FF0000	SCK	VSGSELECT	Each bit selects XV pulses for use as VSG pulses.
0x1D	[23:0]	0	SCK	VSGMASK_CTL	VSG masking. Overrides settings in field registers when enabled.
	[24]	0		VSGMASK_CTL_EN	0: Disable VSGMAK_CTL bits. VSG masking is controlled by field registers. 1: Enable VSGMASK_CTL bits to control VSG masking.
0x1F	[0]	1	SCK	HCNT14_EN	1: Enable 14-bit H-counter.
	[1]	1		PBLK_MASK_EN	1: Disable clamp operation if PBLK is active at the same time as CLPOB.

Table 31. VD/HD Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x20	[0]	0	SCK	MASTER	VD/HD master or slave mode: 0: Slave mode. 1: Master mode.
0x21	[0]	0	VD	VDHDPOL	VD/HD active polarity: 0: Low. 1: High.
0x22	[12:0]	0	VD	HDRISE	Rising edge location for HD. Minimum value is 36 pixels.
	[25:13]	0		VDRISE	Rising edge location for VD.

Table 32. I/O and Charge Pump Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x23	[0]	0	SCK	OSC_NVR	Oscillator normal voltage range. Set to match CLIVDD supply voltage. 0: 1.8 V. 1: 3.3 V.
	[1]	0		XV_NVR	XV output normal voltage range. Set to match XVVDD supply voltage. 0: 1.8 V. 1: 3.3 V.
	[2]	0		IO_NVR	I/O normal voltage range. Set the match IOVDD supply voltage. 0: 1.8 V. 1: 3.3 V.
	[3]	0		DATA_NVR	Data pin normal voltage range. Set to match DRVDD supply voltage. 0: 1.8 V I/O. 1: 3.3 V I/O.
	[4]	0		TEST	Test mode only. Set to 0.
	[5]	0		TEST	Test mode only. Set to 0.
	[6]	0		LDO_32_EN	1: Internal regulator enable for 3.2 V output.
	[9:7]	1		HCLKMODE	Selects HCLK output configuration. Should be written to desired value. 001: Mode 1. 010: Mode 2. 100: Mode 3. All other values are invalid.
0x24	[0]	0	SCK	SEL_VCO	1: Internal CP clock select VCO.
	[1]	1		SEL_DIV	1: Internal CP clock select divided-down version of CLI (default).
	[2]	0		SEL_CLI	1: Internal CP clock select CLI.
	[3]	0		O31V	1: CP output voltage is 3.1 V.
	[4]	0		O32V	1: CP output voltage is 3.2 V.
	[5]	1		O33V	1: CP output voltage is 3.3 V.
	[6]	0		O34V	1: CP output voltage is 3.4 V.
	[7]	1		TEST	Test mode only. Use default values only.
	[8]	1		TEST	Test mode only. Use default values only.
	[9]	1		TEST	Test mode only. Use default values only.
	[10]	1		TEST	Test mode only. Use default values only.
	[11]	0		TEST	Test mode only. Use default values only.
	[12]	0		TEST	Test mode only. Use default values only.
	[13]	0		TEST	Test mode only. Use default values only.
	[14]	1		CP_PDN	Charge pump power-down. 1: Power-down. 0: CP is running.
0x25	[24:0]	0	SCK	VT_STBY12	[23:0] Standby1 and Standby2 polarity for XV [23:0]. [24] Standby1 and Standby2 polarity for XSUBCK. Settings also apply when OUTCONTROL = low.
0x26	[24:0]	0	SCK	VT_STBY3	[23:0] Standby3 polarity for XV [23:0]. [24] Standby3 polarity for XSUBCK.
0x27	[7:0]	0	SCK	GP_STDBY12	Standby1 and Standby2 polarity for GPO [7:0]. Settings also apply when OUTCONTROL = low.
	[15:8]			GP_STDBY3	Standby3 polarity for GPO [7:0].

Table 33. Memory Configuration and MODE Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x28	[4:0]	0	SCK	VPATNUM	Total number of V-pattern groups.
	[9:5]	0		SEQNUM	Total number of V-sequences.
0x2A	[2:0]	0	SCK	MODE	Total number of fields in MODE.
0x2B	[4:0]	0	SCK	FIELD0	Selected first field in MODE.
	[9:5]	0		FIELD1	Selected second field in MODE.
	[14:10]	0		FIELD2	Selected third field in MODE.
	[19:15]	0		FIELD3	Selected fourth field in MODE.
	[24:20]	0		FIELD4	Selected fifth field in MODE.
0x2C	[4:0]	0	SCK	FIELD5	Selected sixth field in MODE.
	[9:5]	0		FIELD6	Selected seventh field in MODE.

Table 34. Timing Core Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x30	[5:0]	0	SCK	H1POSLOC	H1 rising edge location.
	[13:8]	20		H1NEGLOC	H1 falling edge location.
	[16]	1		H1POL	H1 polarity control: 0: Inverse of Figure 19. 1: No inversion.
0x31	[5:0]	0	SCK	H2POSLOC	H2 rising edge location (H5 in HCLK Mode 3).
	[13:8]	20		H2NEGLOC	H2 falling edge location (H5 in HCLK Mode 3).
	[16]	1		H2POL	H2 polarity (H5 in HCLK Mode 3): 0: Inverse of Figure 19. 1: No inversion.
0x32	[5:0]	0	SCK	HLPOSLOC	HL rising edge location.
	[13:8]	20		HLNEGLOC	HL falling edge location.
	[16]	1		HLPOL	HL polarity control: 0: Inverse of Figure 19. 1: No inversion.
0x33	[5:0]	0	SCK	RGPOSLOC	RG rising edge location.
	[13:8]	10		RGNEGLOC	RG falling edge location.
	[16]	1		RGH2POL	RG polarity control: 0: Inverse of Figure 19. 1: No inversion.
0x34	[0]	0	SCK	H1HBLKRETIME	Retime H1, H2, HL HBLK to the internal clock: 0: No retime. 1: Retime.
	[1]	0		H2HBLKRETIME	Recommended setting is retime enabled (1). Setting to 1 adds one cycle delay to programmed HBLK positions.
	[2]	0		HLHBLKRETIME	
	[3]	0		HL_HBLK_EN	Enable HBLK for HL output: 0: Disable. 1: Enable.
	[7:4]	4		HCLK_WIDTH	Enables wide H-clocks during HBLK interval. Set to 0 to disable.
0x35	[2:0]	1	SCK	H1DRV	H1 drive strength: 0: Off. 1: 4.3 mA. 2: 8.6 mA. 3: 12.9 mA. 4: 4.3 mA. 5: 8.6 mA. 6: 12.9 mA. 7: 17.2 mA.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
	[6:4]	1		H2DRV	H2 drive strength (same range as H1DRV).
	[10:8]	1		H3DRV	H3 drive strength (same range as H1DRV).
	[14:12]	1		H4DRV	H4 drive strength (same range as H1DRV).
	[18:16]	1		HLDRV	HL drive strength (same range as H1DRV).
	[22:20]	1		RGDRV	RG drive strength (same range as H1DRV).
0x36	[2:0]	1	SCK	H5DRV	H5 drive strength (same range as H1DRV).
	[6:4]	1		H6DRV	H6 drive strength (same range as H1DRV).
	[10:8]	1		H7DRV	H7 drive strength (same range as H1DRV).
	[14:12]	1		H8DRV	H8 drive strength (same range as H1DRV).
0x37	[5:0]	0	SCK	SHDLOC	SHD sampling edge location.
	[11:6]	20		SHPLOC	SHP sampling edge location.
	[17:12]	10		SHPWIDTH	SHP width (controls input dc restore switch active time).
0x38	[5:0]	0	SCK	DOUTPHASEP	DOUT phase control, positive edge. Specifies location of DOUT.
	[11:6]	20		DOUTPHASEN	DOUT phase control, negative edge. Always set to DOUTPHASEP plus 32 edges to maintain 50% duty cycle of internal DOUTPHASE clocking.
	[12]	0		DCLKMODE	DCLK mode. 0: DCLK tracks DOUT; 1: DCLK phase is fixed.
	[14:13]	0		DOUTDELAY	Data output delay (t_{OD}) with respect to DCLK rising edge: 0: No delay. 1: ~3 ns. 2: ~6 ns. 3: ~9 ns.
	[15]	0		DCLKINV	Invert DCLK output: 0: No inversion. 1: Inversion of DCLK.
0x39	[2:0]	7	SCK	CPHMASK	Enable H-masking during CP operation.

Table 35. Test Registers—Do Not Access

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x3E to 0x4F					Test registers only. Do not access.

Table 36. Test Registers—Do Not Access

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x50 to 0x6F					Test registers only. Do not access.

Table 37. Shutter and GPO Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x70	[2:0]	0	VD	PRIMARY_ACTION	Selects action for primary and secondary counters.
	[5:3]	0		SECOND_ACTION	0: Idle (do nothing) autoreset on VD. 1: Activate counter (primary: auto exposure/readout). 2: RapidShot, wrap/repeat counter. 3: ShotTimer, delay start of count. 4: ShotTimer with RapidShot. 5: SLR exposure (manual). 6: SLR read (manual). 7: Force to idle.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
	[13:6]	0		MANUAL_TRIG	1: Manual trigger for GP signals, when Protocol 1 is selected. Bit 6: GP1 manual trigger. … Bit 13: GP8 manual trigger.
0x71	[12:0]	0	VD	PRIMARY_MAX	Primary counter maximum value.
	[24:13]	0		SECOND_MAX	Secondary counter maximum value.
	[27:25]	0		VDHD_MASK	Mask VD/HD during counter operation.
0x72	[12:0]	0	VD	PRIMARY_DELAY	Number of fields to delay before the next count (exposure) starts. ShotTimer with RapidShot, skip delay before first count (exposure).
	[13]	0		PRIMARY_SKIP	Number of fields to delay before the next count starts. ShotTimer with RapidShot, skip delay before first count.
	[26:14]	0		SECOND_DELAY	
	[27]	0		SECOND_SKIP	
0x73	[2:0]	0	VD	GP1_PROTOCOL	Selects protocol for each general-purpose signal.
	[5:3]	0		GP2_PROTOCOL	Idle = 0.
	[8:6]	0		GP3_PROTOCOL	No counter association = 1.
	[11:9]	0		GP4_PROTOCOL	Link to primary = 2.
	[14:12]	0		GP5_PROTOCOL	Link to secondary = 3.
	[17:15]	0		GP6_PROTOCOL	Link to mode = 4.
	[20:18]	0		GP7_PROTOCOL	Primary repeat = 5.
	[23:21]	0		GP8_PROTOCOL	Secondary repeat = 6. Keep on = 7.
0x74	[12:0]	0	VD	SGMASK_NUM	Exposure: number of fields to mask SGs.
	[25:13]	0		SUBCKMASK_NUM	Exposure plus readout: number of fields to mask SUBCK.
	[26]	1		SUBCKTOG_UPDATE	0: SUBCK toggles (Register 0x77) updated on SG line. 1: SUBCK toggles (Register 0x77) updated on UPDATE line (VD-updated).
	[27]	0		SUBCKMASK_SKIP1	Skip the SUBCK mask for the first exposure field only. Typically set to 1.
0x75	[0]	0	SG	TEST	Reserved for test purpose. Must be set to 0.
	[13:1]	0		SUBCKSTARTLINE	Line location after VSG line to begin SUBCK pulses. Must not be set to 1.
	[26:14]	0		SUBCKNUM	Number of SUBCK pulses per field. Must be set less than VDLEN.
	[27]	0		SG_SUPPRESS	Suppress the SG and allow SUBCK to finish at SUBCKNUM.
0x76	[12:0]	1FFF	VD	SUBCK_TOG1	SUBCK Toggle Position 1.
	[25:13]	1FFF		SUBCK_TOG2	SUBCK Toggle Position 2.
	[26]	0		SUBCK_POL	SUBCK start polarity.
0x77	[12:0]	1FFF	VD/SG	SUBCKHP_TOG1	High precision SUBCK Toggle Position 1.
	[25:13]	1FFF		SUBCKHP_TOG2	High precision SUBCK Toggle Position 2.
0x78	[0]	0	VD	GP1_POL	GP1 low/high start polarity.
	[1]	0		GP2_POL	GP2 low/high start polarity.
	[2]	0		GP3_POL	GP3 low/high start polarity.
	[3]	0		GP4_POL	GP4 low/high start polarity.
	[4]	0		GP5_POL	GP5 low/high start polarity.
	[5]	0		GP6_POL	GP6 low/high start polarity.
	[6]	0		GP7_POL	GP7 low/high start polarity.
	[7]	0		GP8_POL	GP8 low/high start polarity.
	[8]	1		SEL_GP1	1: GP1 signal is selected for GPO1 output.
	[9]	1		SEL_GP2	1: GP2 signal is selected for GPO2 output.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
	[10]	1		SEL_GP3	1: GP3 signal is selected for GPO3 output.
	[11]	1		SEL_GP4	1: GP4 signal is selected for GPO4 output. 0: SUBCK is selected.
	[12]	1		SEL_GP5	1: GP5 signal is selected for GPO5 output. 0: XV21 is selected.
	[13]	1		SEL_GP6	1: GP6 signal is selected for GPO6 output. 0: XV22 is selected.
	[14]	1		SEL_GP7	1: GP7 signal is selected for GPO7 output. 0: XV23 is selected.
	[15]	1		SEL_GP8	1: GP8 signal is selected for GPO8 output. 0: XV24 is selected.
	[23:16]	0		GPO_OUTPUT_EN	1: GPO outputs enabled. 0: GPO is input high-Z state (default).
	[24]	0		GPO5_OVERRIDE	1: When GPO5 configured as input, overrides internal OUT_CONT.
	[25]	0		GPO6_OVERRIDE	1: When GPO6 configured as input, overrides internal HBLK.
	[26]	0		GPO7_OVERRIDE	1: When GPO7 configured as input, overrides internal CLPOB.
	[27]	0		GPO8_OVERRIDE	1: When GPO8 configured as input, overrides internal PBLK.
0x79	[7:0]	0	VD	GP*_USE_LUT	Use result from LUT, or else GP* is unaltered.
	[11:8]	{0, 0, 0, 0}		LUT_FOR_GP12	Two-input look-up table results.
	[15:12]	{0, 0, 0, 0}		LUT_FOR_GP34	Examples: {LUT_FOR_GP12} ← [GP2:GP1].
	[19:16]	{0, 0, 0, 0}		LUT_FOR_GP56	{0, 1, 1, 0} = GP2 XOR GP1; {1, 1, 1, 0} = GP2 OR GP1.
	[23:20]	{0, 0, 0, 0}		LUT_FOR_GP78	{0, 1, 1, 1} = GP2 NAND GP1; {1, 0, 0, 0} = GP2 AND GP1.
0x7A	[12:0]	0	VD	GP1_TOG1_FD	General-Purpose Signal 1, first toggle position, field location.
	[25:13]	0		GP1_TOG1_LN	General-Purpose Signal 1, first toggle position, line location.
0x7B	[12:0]	0	VD	GP1_TOG1_PX	General-Purpose Signal 1, first toggle position, pixel location.
	[25:13]	0		GP1_TOG2_FD	General-Purpose Signal 1, second toggle position, field location.
0x7C	[12:0]	0	VD	GP1_TOG2_LN	General-Purpose Signal 1, second toggle position, line location.
	[25:13]	0		GP1_TOG2_PX	General-Purpose Signal 1, second toggle position, pixel location.
0x7D	[12:0]	0	VD	GP1_TOG3_FD	General-Purpose Signal 1, third toggle position, field location.
	[25:13]	0		GP1_TOG3_LN	General-Purpose Signal 1, third toggle position, line location.
0x7E	[12:0]	0	VD	GP1_TOG3_PX	General-Purpose Signal 1, third toggle position, pixel location.
	[25:13]	0		GP1_TOG4_FD	General-Purpose Signal 1, fourth toggle position, field location.
0x7F	[12:0]	0	VD	GP1_TOG4_LN	General-Purpose Signal 1, fourth toggle position, line location.
	[25:13]	0		GP1_TOG4_PX	General-Purpose Signal 1, fourth toggle position, pixel location.
0x80	[12:0]	0	VD	GP2_TOG1_FD	General-Purpose Signal 2, first toggle position, field location.
	[25:13]	0		GP2_TOG1_LN	General-Purpose Signal 2, first toggle position, line location.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x81	[12:0]	0	VD	GP2_TOG1_PX	General-Purpose Signal 2, first toggle position, pixel location.
	[25:13]	0		GP2_TOG2_FD	General-Purpose Signal 2, second toggle position, field location.
0x82	[12:0]	0	VD	GP2_TOG2_LN	General-Purpose Signal 2, second toggle position, line location.
	[25:13]	0		GP2_TOG2_PX	General-Purpose Signal 2, second toggle position, pixel location.
0x83	[12:0]	0	VD	GP2_TOG3_FD	General-Purpose Signal 2, third toggle position, field location.
	[25:13]	0		GP2_TOG3_LN	General-Purpose Signal 2, third toggle position, line location.
0x84	[12:0]	0	VD	GP2_TOG3_PX	General-Purpose Signal 2, third toggle position, pixel location.
	[25:13]	0		GP2_TOG4_FD	General-Purpose Signal 2, fourth toggle position, field location.
0x85	[12:0]	0	VD	GP2_TOG4_LN	General-Purpose Signal 2, fourth toggle position, line location.
	[25:13]	0		GP2_TOG4_PX	General-Purpose Signal 2, fourth toggle position, pixel location.
0x86	[12:0]	0	VD	GP3_TOG1_FD	General-Purpose Signal 3, first toggle position, field location.
	[25:13]	0		GP3_TOG1_LN	General-Purpose Signal 3, first toggle position, line location.
0x87	[12:0]	0	VD	GP3_TOG1_PX	General-Purpose Signal 3, first toggle position, pixel location.
	[25:13]	0		GP3_TOG2_FD	General-Purpose Signal 3, second toggle position, field location.
0x88	[12:0]	0	VD	GP3_TOG2_LN	General-Purpose Signal 3, second toggle position, line location.
	[25:13]	0		GP3_TOG2_PX	General-Purpose Signal 3, second toggle position, pixel location.
0x89	[12:0]	0	VD	GP3_TOG3_FD	General-Purpose Signal 3, third toggle position, field location.
	[25:13]	0		GP3_TOG3_LN	General-Purpose Signal 3, third toggle position, line location.
0x8A	[12:0]	0	VD	GP3_TOG3_PX	General-Purpose Signal 3, third toggle position, pixel location.
	[25:13]	0		GP3_TOG4_FD	General-Purpose Signal 3, fourth toggle position, field location.
0x8B	[12:0]	0	VD	GP3_TOG4_LN	General-Purpose Signal 4, fourth toggle position, line location.
	[25:13]	0		GP3_TOG4_PX	General-Purpose Signal 4, fourth toggle position, pixel location.
0x8C	[12:0]	0	VD	GP4_TOG1_FD	General-Purpose Signal 4, first toggle position, field location.
	[25:13]	0		GP4_TOG1_LN	General-Purpose Signal 4, first toggle position, line location.
0x8D	[12:0]	0	VD	GP4_TOG1_PX	General-Purpose Signal 4, first toggle position, pixel location.
	[25:13]	0		GP4_TOG2_FD	General-Purpose Signal 4, second toggle position, field location.
0x8E	[12:0]	0	VD	GP4_TOG2_LN	General-Purpose Signal 4, second toggle position, line location.
	[25:13]	0		GP4_TOG2_PX	General-Purpose Signal 4, second toggle position, pixel location.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x8F	[12:0]	0	VD	GP4_TOG3_FD	General-Purpose Signal 4, third toggle position, field location.
	[25:13]	0		GP4_TOG3_LN	General-Purpose Signal 4, third toggle position, line location.
0x90	[12:0]	0	VD	GP4_TOG3_PX	General-Purpose Signal 4, third toggle position, pixel location.
	[25:13]	0		GP4_TOG4_FD	General-Purpose Signal 4, fourth toggle position, field location.
0x91	[12:0]	0	VD	GP4_TOG4_LN	General-Purpose Signal 4, fourth toggle position, line location.
	[25:13]	0		GP4_TOG4_PX	General-Purpose Signal 4, fourth toggle position, pixel location.
0x92	[12:0]	0	VD	GP5_TOG1_FD	General-Purpose Signal 5, first toggle position, field location.
	[25:13]	0		GP5_TOG1_LN	General-Purpose Signal 5, first toggle position, line location.
0x93	[12:0]	0	VD	GP5_TOG1_PX	General-Purpose Signal 5, first toggle position, pixel location.
	[25:13]	0		GP5_TOG2_FD	General-Purpose Signal 5, second toggle position, field location.
0x94	[12:0]	0	VD	GP5_TOG2_LN	General-Purpose Signal 5, second toggle position, line location.
	[25:13]	0		GP5_TOG2_PX	General-Purpose Signal 5, second toggle position, pixel location.
0x95	[12:0]	0	VD	GP5_TOG3_FD	General-Purpose Signal 5, third toggle position, field location.
	[25:13]	0		GP5_TOG3_LN	General-Purpose Signal 5, third toggle position, line location.
0x96	[12:0]	0	VD	GP5_TOG3_PX	General-Purpose Signal 5, third toggle position, pixel location.
	[25:13]	0		GP5_TOG4_FD	General-Purpose Signal 5, fourth toggle position, field location.
0x97	[12:0]	0	VD	GP5_TOG4_LN	General-Purpose Signal 5, fourth toggle position, line location.
	[25:13]	0		GP5_TOG4_PX	General-Purpose Signal 5, fourth toggle position, pixel location.
0x98	[12:0]	0	VD	GP6_TOG1_FD	General-Purpose Signal 6, first toggle position, field location.
	[25:13]	0		GP6_TOG1_LN	General-Purpose Signal 6, first toggle position, line location.
0x99	[12:0]	0	VD	GP6_TOG1_PX	General-Purpose Signal 6, first toggle position, pixel location.
	[25:13]	0		GP6_TOG2_FD	General-Purpose Signal 6, second toggle position, field location.
0x9A	[12:0]	0	VD	GP6_TOG2_LN	General-Purpose Signal 6, second toggle position, line location.
	[25:13]	0		GP6_TOG2_PX	General-Purpose Signal 6, second toggle position, pixel location.
0x9B	[12:0]	0	VD	GP6_TOG3_FD	General-Purpose Signal 6, third toggle position, field location.
	[25:13]	0		GP6_TOG3_LN	General-Purpose Signal 6, third toggle position, line location.
0x9C	[12:0]	0	VD	GP6_TOG3_PX	General-Purpose Signal 6, third toggle position, pixel location.
	[25:13]	0		GP6_TOG4_FD	General-Purpose Signal 6, fourth toggle position, field location.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x9D	[12:0]	0	VD	GP6_TOG4_LN	General-Purpose Signal 6, fourth toggle position, line location.
	[25:13]	0		GP6_TOG4_PX	General-Purpose Signal 6, fourth toggle position, pixel location.
0x9E	[12:0]	0	VD	GP7_TOG1_FD	General-Purpose Signal 7, first toggle position, field location.
	[25:13]	0		GP7_TOG1_LN	General-Purpose Signal 7, first toggle position, line location.
0x9F	[12:0]	0	VD	GP7_TOG1_PX	General-Purpose Signal 7, first toggle position, pixel location.
	[25:13]	0		GP7_TOG2_FD	General-Purpose Signal 7, second toggle position, field location.
0xA0	[12:0]	0	VD	GP7_TOG2_LN	General-Purpose Signal 7, second toggle position, line location.
	[25:13]	0		GP7_TOG2_PX	General-Purpose Signal 7, second toggle position, pixel location.
0xA1	[12:0]	0	VD	GP7_TOG3_FD	General-Purpose Signal 7, third toggle position, field location.
	[25:13]	0		GP7_TOG3_LN	General-Purpose Signal 7, third toggle position, line location.
0xA2	[12:0]	0	VD	GP7_TOG3_PX	General-Purpose Signal 7, third toggle position, pixel location.
	[25:13]	0		GP7_TOG4_FD	General-Purpose Signal 7, fourth toggle position, field location.
0xA3	[12:0]	0	VD	GP7_TOG4_LN	General-Purpose Signal 7, fourth toggle position, line location.
	[25:13]	0		GP7_TOG4_PX	General-Purpose Signal 7, fourth toggle position, pixel location.
0xA4	[12:0]	0	VD	GP8_TOG1_FD	General-Purpose Signal 8, first toggle position, field location.
	[25:13]	0		GP8_TOG1_LN	General-Purpose Signal 8, first toggle position, line location.
0xA5	[12:0]	0	VD	GP8_TOG1_PX	General-Purpose Signal 8, first toggle position, pixel location.
	[25:13]	0		GP8_TOG2_FD	General-Purpose Signal 8, second toggle position, field location.
0xA6	[12:0]	0	VD	GP8_TOG2_LN	General-Purpose Signal 8, second toggle position, line location.
	[25:13]	0		GP8_TOG2_PX	General-Purpose Signal 8, second toggle position, pixel location.
0xA7	[12:0]	0	VD	GP8_TOG3_FD	General-Purpose Signal 8, third toggle position, field location.
	[25:13]	0		GP8_TOG3_LN	General-Purpose Signal 8, third toggle position, line location.
0xA8	[12:0]	0	VD	GP8_TOG3_PX	General-Purpose Signal 8, third toggle position, pixel location.
	[25:13]	0		GP8_TOG4_FD	General-Purpose Signal 8, fourth toggle position, field location.
0xA9	[12:0]	0	VD	GP8_TOG4_LN	General-Purpose Signal 8, fourth toggle position, line location.
	[25:13]	0		GP8_TOG4_PX	General-Purpose Signal 8, fourth toggle position, pixel location.
0xAA	[0]	0	VD	SUBCK_TOG1_13	Bit 13 for SUBCK Toggle Position 1. For 14-bit H-counter mode.
	[1]	0	VD	SUBCK_TOG2_13	Bit 13 for SUBCK Toggle Position 2. For 14-bit H-counter mode.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
	[2]	0	VD/SG	SUBCKHP_TOG1_13	Bit 13 for SUBCK HP Toggle 1. For 14-bit H-counter mode.
	[3]	0	VD/SG	SUBCKHP_TOG2_13	Bit 13 for SUBCK HP Toggle 2. For 14-bit H-counter mode.

Table 38. Update Control Registers

Address	Data Bits	Default Value	Update	Mnemonic	Description
0xB0	[15:0]	1803	SCK	AFE_UPDT_SCK	Each bit corresponds to one address location. AFE_UPDT_SCK [0] = 1, update Address 0x00 on SL rising edge. AFE_UPDT_SCK [1] = 1, update Address 0x01 on SL rising edge. … AFE_UPDT_SCK [15] = 1, update Address 0x0F on SL rising edge.
0xB1	[15:0]	E7FC	SCK	AFE_UPDT_VD	Each bit corresponds to one address location. AFE_UPDT_VD [0] = 1, update Address 0x00 on VD rising edge. AFE_UPDT_VD [1] = 1, update Address 0x01 on VD rising edge. … AFE_UPDT_VD [15] = 1, update Address 0x0F on VD rising edge.
0xB2	[15:0]	F8FD	SCK	MISC_UPDT_SCK	Enable SCK update of miscellaneous registers, Address 0x10 to Address 0x1F.
0xB3	[15:0]	0702	SCK	MISC_UPDT_VD	Enable VD update of miscellaneous registers, Address 0x10 to Address 0x1F.
0xB4	[15:0]	FFF9	SCK	VDHD_UPDT_SCK	Enable SCK update of VDHD registers, Address 0x20 to Address 0x2F.
0xB5	[15:0]	0006	SCK	VDHD_UPDT_VD	Enable VD update of VDHD registers, Address 0x20 to Address 0x2F.

Table 39. Extra Registers

Address	Data Bits	Default Value	Update	Mnemonic	Description
0xD4	[0]	0	SCK	TEST	Test mode only. Set to 0.
	[1]	0		GPO_INT_EN	Allow observation of internal signals at GPO5 to GPO8 outputs: GPO5: OUTCONTROL. GPO6: HBLK. GPO7: CLPOB. GPO8: PBLK.
	[9:2]	0		TEST	Test mode only. Set to 0.
0xD7	[0]	0	SCK	TEST	Test mode only. Set to 0.
	[1]	0		XV24_SWAP	Set to 1 to change the V-driver output configuration so that XV15 is output on the XV24 output pin. Useful with special vertical sequence alternation mode when the XV24 register is reserved for pattern selection.
0xD8	[27:0]	0	SCK	START	Recommended start-up register. Should be set to 0x888.

Table 40. V-Pattern Group (VPAT) Register Map

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x00	[12:0]	X	SCP	XV1TOG1	XV1 Toggle Position 1.
	[25:13]	X		XV1TOG2	XV1 Toggle Position 2.
0x01	[12:0]	X	SCP	XV1TOG3	XV1 Toggle Position 3.
	[25:13]	X		XV1TOG4	XV1 Toggle Position 4.
0x02	[12:0]	X	SCP	XV2TOG1	XV2 Toggle Position 1.
	[25:13]	X		XV2TOG2	XV2 Toggle Position 2.
0x03	[12:0]	X	SCP	XV2TOG3	XV2 Toggle Position 3.
	[25:13]	X		XV2TOG4	XV2 Toggle Position 4.
0x04	[12:0]	X	SCP	XV3TOG1	XV3 Toggle Position 1.
	[25:13]	X		XV3TOG2	XV3 Toggle Position 2.
0x05	[12:0]	X	SCP	XV3TOG3	XV3 Toggle Position 3.
	[25:13]	X		XV3TOG4	XV3 Toggle Position 4.
0x06	[12:0]	X	SCP	XV4TOG1	XV4 Toggle Position 1.
	[25:13]	X		XV4TOG2	XV4 Toggle Position 2.
0x07	[12:0]	X	SCP	XV4TOG3	XV4 Toggle Position 3.
	[25:13]	X		XV4TOG4	XV4 Toggle Position 4.
0x08	[12:0]	X	SCP	XV5TOG1	XV5 Toggle Position 1.
	[25:13]	X		XV5TOG2	XV5 Toggle Position 2.
0x09	[12:0]	X	SCP	XV5TOG3	XV5 Toggle Position 3.
	[25:13]	X		XV5TOG4	XV5 Toggle Position 4.
0x0A	[12:0]	X	SCP	XV6TOG1	XV6 Toggle Position 1.
	[25:13]	X		XV6TOG2	XV6 Toggle Position 2.
0x0B	[12:0]	X	SCP	XV6TOG3	XV6 Toggle Position 3.
	[25:13]	X		XV6TOG4	XV6 Toggle Position 4.
0x0C	[12:0]	X	SCP	XV7TOG1	XV7 Toggle Position 1.
	[25:13]	X		XV7TOG2	XV7 Toggle Position 2.
0x0D	[12:0]	X	SCP	XV7TOG3	XV7 Toggle Position 3.
	[25:13]	X		XV7TOG4	XV7 Toggle Position 4.
0x0E	[12:0]	X	SCP	XV8TOG1	XV8 Toggle Position 1.
	[25:13]	X		XV8TOG2	XV8 Toggle Position 2.
0x0F	[12:0]	X	SCP	XV8TOG3	XV8 Toggle Position 3.
	[25:13]	X		XV8TOG4	XV8 Toggle Position 4.
0x10	[12:0]	X	SCP	XV9TOG1	XV9 Toggle Position 1.
	[25:13]	X		XV9TOG2	XV9 Toggle Position 2.
0x11	[12:0]	X	SCP	XV9TOG3	XV9 Toggle Position 3.
	[25:13]	X		XV9TOG4	XV9 Toggle Position 4.
0x12	[12:0]	X	SCP	XV10TOG1	XV10 Toggle Position 1.
	[25:13]	X		XV10TOG2	XV10 Toggle Position 2.
0x13	[12:0]	X	SCP	XV10TOG3	XV10 Toggle Position 3.
	[25:13]	X		XV10TOG4	XV10 Toggle Position 4.
0x14	[12:0]	X	SCP	XV11TOG1	XV11 Toggle Position 1.
	[25:13]	X		XV11TOG2	XV11 Toggle Position 2.
0x15	[12:0]	X	SCP	XV11TOG3	XV11 Toggle Position 3.
	[25:13]	X		XV11TOG4	XV11 Toggle Position 4.
0x16	[12:0]	X	SCP	XV12TOG1	XV12 Toggle Position 1.
	[25:13]	X		XV12TOG2	XV12 Toggle Position 2.
0x17	[12:0]	X	SCP	XV12TOG3	XV12 Toggle Position 3.
	[25:13]	X		XV12TOG4	XV12 Toggle Position 4.
0x18	[12:0]	X	SCP	XV13TOG1	XV13 Toggle Position 1.
	[25:13]	X		XV13TOG2	XV13 Toggle Position 2.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x19	[12:0]	X	SCP	XV13TOG3	XV13 Toggle Position 3.
	[25:13]	X		XV13TOG4	XV13 Toggle Position 4.
0x1A	[12:0]	X	SCP	XV14TOG1	XV14 Toggle Position 1.
	[25:13]	X		XV14TOG2	XV14 Toggle Position 2
0x1B	[12:0]	X	SCP	XV14TOG3	XV14 Toggle Position 3.
	[25:13]	X		XV14TOG4	XV14 Toggle Position 4.
0x1C	[12:0]	X	SCP	XV15TOG1	XV15 Toggle Position 1.
	[25:13]	X		XV15TOG2	XV15 Toggle Position 2.
0x1D	[12:0]	X	SCP	XV15TOG3	XV15 Toggle Position 3.
	[25:13]	X		XV15TOG4	XV15 Toggle Position 4.
0x1E	[12:0]	X	SCP	XV16TOG1	XV16 Toggle Position 1.
	[25:13]	X		XV16TOG2	XV16 Toggle Position 2.
0x1F	[12:0]	X	SCP	XV16TOG3	XV16 Toggle Position 3.
	[25:13]	X		XV16TOG4	XV16 Toggle Position 4.
0x20	[12:0]	X	SCP	XV17TOG1	XV17 Toggle Position 1.
	[25:13]	X		XV17TOG2	XV17 Toggle Position 2.
0x21	[12:0]	X	SCP	XV17TOG3	XV17 Toggle Position 3.
	[25:13]	X		XV17TOG4	XV17 Toggle Position 4.
0x22	[12:0]	X	SCP	XV18TOG1	XV18 Toggle Position 1.
	[25:13]	X		XV18TOG2	XV18 Toggle Position 2.
0x23	[12:0]	X	SCP	XV18TOG3	XV18 Toggle Position 3.
	[25:13]	X		XV18TOG4	XV18 Toggle Position 4.
0x24	[12:0]	X	SCP	XV19TOG1	XV19 Toggle Position 1.
	[25:13]	X		XV19TOG2	XV19 Toggle Position 2.
0x25	[12:0]	X	SCP	XV19TOG3	XV19 Toggle Position 3.
	[25:13]	X		XV19TOG4	XV19 Toggle Position 4.
0x26	[12:0]	X	SCP	XV20TOG1	XV20 Toggle Position 1.
	[25:13]	X		XV20TOG2	XV20 Toggle Position 2.
0x27	[12:0]	X	SCP	XV20TOG3	XV20 Toggle Position 3.
	[25:13]	X		XV20TOG4	XV20 Toggle Position 4.
0x28	[12:0]	X	SCP	XV21TOG1	XV21 Toggle Position 1.
	[25:13]	X		XV21TOG2	XV21 Toggle Position 2.
0x29	[12:0]	X	SCP	XV21TOG3	XV21 Toggle Position 3.
	[25:13]	X		XV21TOG4	XV21 Toggle Position 4.
0x2A	[12:0]	X	SCP	XV22TOG1	XV22 Toggle Position 1.
	[25:13]	X		XV22TOG2	XV22 Toggle Position 2.
0x2B	[12:0]	X	SCP	XV22TOG3	XV22 Toggle Position 3.
	[25:13]	X		XV22TOG4	XV22 Toggle Position 4.
0x2C	[12:0]	X	SCP	XV23TOG1	XV23 Toggle Position 1.
	[25:13]	X		XV23TOG2	XV23 Toggle Position 2.
0x2D	[12:0]	X	SCP	XV23TOG3	XV23 Toggle Position 3.
	[25:13]	X		XV23TOG4	XV23 Toggle Position 4.
0x2E	[12:0]	X	SCP	XV24TOG1	XV24 Toggle Position 1.
	[25:13]	X		XV24TOG2	XV24 Toggle Position 2.
0x2F	[12:0]	X	SCP	XV24TOG3	XV24 Toggle Position 3.
	[25:13]	X		XV24TOG4	XV24 Toggle Position 4.

Table 41. V-Sequence (VSEQ) Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x00	[0]	X	SCP	CLPOBPOL	CLPOB start polarity.
	[1]	X		PBLKPOL	PBLK start polarity.
	[5:2]	X		HOLD	1: Enable HOLD function for each VPAT group (A, B, C, D).
	[9:6]	X		VMASK_EN	1: Enable FREEZE/RESUME for each VPAT group (A, B, C, D).
	[13:10]	X		CONCAT_GRP	Combine multiple VPAT groups together in one sequence. Set register equal to 0x01 to enable.
	[15:14]	X		VREP_MODE	Defines V-alternation repetition mode. 00: Single pattern alternation for all groups. 01: Two pattern alternation for all groups. 10: Three-pattern alternation for Group A. Groups B, C, and D follow pattern {0, 1, 1, 0, 1, 1…}. 11: Four-pattern alternation for Group A. Two-pattern alternation for Groups B, C, and D.
	[19:16]	X		LASTREPLEN_EN	Enable use of last repetition counter for last repetition length of each group.
	[23:20]	X		LASTTOG_EN	Enable the fifth toggle position for all V-signals in each group.
	[25:24]	X		HBLK_MODE	Selection of HBLK modes: 00: HBLK Mode 0 (normal six-toggle operation). 01: HBLK Mode 1. 10: HBLK Mode 2. (Address 0x19 to Address 0x1E operate differently.) 11: Test only, do not access.
0x01	[12:0]	X	SCP	HDLENE	HD line length for even lines.
	[25:13]	X		HDLENO	HD line length for odd lines.
0x02	[23:0]	X	SCP	VSGPATSEL	Selects which two toggle positions are used by each V-output when they are configured as VSG pulses (Miscellaneous Register Address 0x1C, fixed register area): 0: Use Toggle 1, Toggle 2. 1: Use Toggle 3, Toggle 4.
	[24]			HDLENE_13	HD length Bit 13 for even lines when 14-bit H-counter is enabled.
	[25]			HDLENO_13	HD length Bit 13 for odd lines when 14-bit H-counter is enabled.
0x03	[23:0]	X	SCP	VPOL_A	Starting polarities for each V-output signal (Group A).
0x04	[23:0]	X	SCP	VPOL_B	Starting polarities for each V-output signal (Group B).
0x05	[23:0]	X	SCP	VPOL_C	Starting polarities for each V-output signal (Group C).
0x06	[23:0]	X	SCP	VPOL_D	Starting polarities for each V-output signal (Group D).
0x07	[23:0]	X	SCP	GROUPSEL_0	Select which group each XV1 to XV12 signal is assigned to: 00: Group A. 01: Group B. 10: Group C. 11: Group D. [1:0]: XV1. [3:2]: XV2. … [23:22]: XV12.
0x08	[23:0]	X	SCP	GROUPSEL_1	Select which group each XV13 to XV24 signal is assigned to: 00: Group A. 01: Group B. 10: Group C. 11: Group D. [1:0]: XV13. [3:2]: XV14. … [23:22]: XV24.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x09	[4:0]	X	SCP	VPATSELA	Selected VPAT group for Group A, from VPAT Group 0 to Group 31.
	[9:5]	X		VPATSELB	Selected VPAT group for Group B, from VPAT Group 0 to Group 31.
	[14:10]	X		VPATSELC	Selected VPAT group for Group C, from VPAT Group 0 to Group 31.
	[19:15]	X		VPATSELD	Selected VPAT group for Group D, from VPAT Group 0 to Group 31.
0x0A	[12:0]	X	SCP	VSTARTA	Start position of selected V-Pattern Group A.
	[25:13]	X		VLENA	Length of selected V-Pattern Group A.
0x0B	[12:0]	X	SCP	VREPA_1	Number of repetitions for V-Pattern Group A for first lines.
	[25:13]	X		VREPA_2	Number of repetitions for V-Pattern Group A for second lines.
0x0C	[12:0]	X	SCP	VREPA_3	Number of repetitions for V-Pattern Group A for third lines.
	[25:13]	X		VREPA_4	Number of repetitions for V-Pattern Group A for fourth lines.
0x0D	[12:0]	X	SCP	VSTARTB	Start position of selected V-Pattern Group B.
	[25:13]	X		VLENB	Length of selected V-Pattern Group B.
0x0E	[12:0]	X	SCP	VREPB_ODD	Number of repetitions for V-Pattern Group B for odd lines.
	[25:13]	X		VREPB_EVEN	Number of repetitions for V-Pattern Group B for even lines.
0x0F	[12:0]	X	SCP	VSTARTC	Start position of selected V-Pattern Group C.
	[25:13]	X		VLENC	Length of selected V-Pattern Group C.
0x10	[12:0]	X	SCP	VREPC_ODD	Number of repetitions for V-Pattern Group C for odd lines.
	[25:13]	X		VREPC_EVEN	Number of repetitions for V-Pattern Group C for even lines.
0x11	[12:0]	X	SCP	VSTARTD	Start position of selected V-Pattern Group D.
	[25:13]	X		VLEND	Length of selected V-Pattern Group D.
0x12	[12:0]	X	SCP	VREPD_ODD	Number of repetitions for V-Pattern Group D for odd lines.
	[25:13]	X		VREPD_EVEN	Number of repetitions for V-Pattern Group D for even lines.
0x13	[12:0]	X	SCP	FREEZE1	Holds the V-outputs at their current levels.
	[25:13]	X		RESUME1	Resumes the operation of V-outputs to finish the pattern.
0x14	[12:0]	X	SCP	FREEZE2	Holds the V-outputs at their current levels.
	[25:13]	X		RESUME2	Resumes the operation of V-outputs to finish the pattern.
0x15	[12:0]	X	SCP	FREEZE3	Holds the V-outputs at their current levels.
	[25:13]	X		RESUME3	Resumes the operation of V-outputs to finish the pattern.
0x16	[12:0]	X	SCP	FREEZE4	Holds the V-outputs at their current levels.
	[25:13]	X		RESUME4	Resumes the operation of V-outputs to finish the pattern.
0x17	[12:0]	X	SCP	HBLKSTART	Start location for HBLK in HBLK Mode 1 and HBLK Mode 2.
	[25:13]	X		HBLKEND	End location for HBLK in HBLK Mode 1 and HBLK Mode 2.
0x18	[12:0]	X	SCP	HBLKLEN	HBLK length in HBLK Mode 1 and HBLK Mode 2.
	[20:13]	X		HBLKREP	Number of HBLK repetitions in HBLK Mode 1 and HBLK Mode 2.
	[21]	X		HBLKMASK_H1	Masking polarity for H1/H3/H5/H7 during HBLK.
	[22]	X		HBLKMASK_H2	Masking polarity for H2/H4/H6/H8 during HBLK.
	[23]	X		HBLKMASK_HL	Masking polarity for HL during HBLK.
	[25:24]	X		TEST	Test mode only. Set to 0.
0x19	[12:0]	X	SCP	HBLKTOGO1	First HBLK toggle position for odd lines, or RA0H1REPA/B/C in HBLK Mode 2 (see the HBLK Mode 2 Operation section for more information).
	[25:13]	X		HBLKTOGO2	Second HBLK toggle position for odd lines, or RA1H1REPA/B/C.
0x1A	[12:0]	X	SCP	HBLKTOGO3	Third HBLK toggle position for odd lines, or RA2H1REPA/B/C.
	[25:13]	X		HBLKTOGO4	Fourth HBLK toggle position for odd lines, or RA3H1REPA/B/C.
0x1B	[12:0]	X	SCP	HBLKTOGO5	Fifth HBLK toggle position for odd lines, or RA4H1REPA/B/C.
	[25:13]	X		HBLKTOGO6	Sixth HBLK toggle position for odd lines, or RA5H1REPA/B/C.
0x1C	[12:0]	X	SCP	HBLKTOGE1	First HBLK toggle position for even lines, or RA0H2REPA/B/C.
	[25:13]	X		HBLKTOGE2	Second HBLK toggle position for even lines, or RA1H2REPA/B/C.
0x1D	[12:0]	X	SCP	HBLKTOGE3	Third HBLK toggle position for even lines, or RA2H2REPA/B/C.
	[25:13]	X		HBLKTOGE4	Fourth HBLK toggle position for even lines, or RA3H2REPA/B/C.
0x1E	[12:0]	X	SCP	HBLKTOGE5	Fifth HBLK toggle position for even lines, or RA4H2REPA/B/C.
	[25:13]	X		HBLKTOGE6	Sixth HBLK toggle position for even lines, or RA5H2REPA/B/C.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x1F	[12:0]	X	SCP	HBLKSTARTA	HBLK Repeat Area Start Position A for HBLK Mode 2. Set to 8191 if not used.
	[25:13]	X		HBLKSTARTB	HBLK Repeat Area Start Position B for HBLK Mode 2. Set to 8191 if not used.
0x20	[12:0]	X	SCP	HBLKSTARTC	HBLK Repeat Area Start Position C for HBLK Mode 2. Set to 8191 if not used.
	[13]	X		VSEQALT_EN	Special V-sequence alternation enable.
	[14]	X		VALT_MAP	1: Enables operation of VALTSEL0_EVEN/ODD, VALTSEL1_EVEN/ODD registers in FREEZE/RESUME registers. Must be enabled if special VALT mode is used.
	[17:15]	X		SPC_PAT_EN	1: Enables use of special vertical pattern insertion into VPATA sequence. [0]: Use VPATB as the special pattern. [1]: Use VPATC as the special pattern. [2]: Use VPATD as the special pattern.
0x21	[2:0]	X	SCP	HBLKALT_PAT1	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
	[6:4]	X		HBLKALT_PAT2	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
	[10:8]	X		HBLKALT_PAT3	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
	[14:12]	X		HBLKALT_PAT4	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
	[18:16]	X		HBLKALT_PAT5	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
	[22:20]	X		HBLKALT_PAT6	HBLK Mode 2, Repeat Area 0 pattern for odd lines.
0x22	[12:0]	X	SCP	CLPOBTOG1	CLPOB Toggle Position 1.
	[25:13]	X		CLPOBTOG2	CLPOB Toggle Position 2.
0x23	[12:0]	X	SCP	PBLKTOG1	PBLK Toggle Position 1.
	[25:13]	X		PBLKTOG2	PBLK Toggle Position 2.
0x24	[12:0]	X	SCP	LASTREPLEN_A	Last repetition length for Group A. Set equal to VLENA.
	[25:13]	X		LASTREPLEN_B	Last repetition length for Group B. Set equal to VLENB.
0x25	[12:0]	X	SCP	LASTREPLEN_C	Last repetition length for Group C. Set equal to VLENC.
	[25:13]	X		LASTREPLEN_D	Last repetition length for Group D. Set equal to VLEND.
0x26	[12:0]	X	SCP	LASTTOG_A	Optional fifth toggle position for Group A.
	[25:13]	X		LASTTOG_B	Optional fifth toggle position for Group B.
0x27	[12:0]	X	SCP	LASTTOG_C	Optional fifth toggle position for Group C.
	[25:13]	X		LASTTOG_D	Optional fifth toggle position for Group D.

Table 42. Field Registers

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x00	[4:0]	X	VD	SEQ0	Selected V-sequence for first region in the field.
	[9:5]	X		SEQ1	Selected V-sequence for second region in the field.
	[14:10]	X		SEQ2	Selected V-sequence for third region in the field.
	[19:15]	X		SEQ3	Selected V-sequence for fourth region in the field.
	[24:20]	X		SEQ4	Selected V-sequence for fifth region in the field.
0x01	[4:0]	X	VD	SEQ5	Selected V-sequence for sixth region in the field.
	[9:5]	X		SEQ6	Selected V-sequence for seventh region in the field.
	[14:10]	X		SEQ7	Selected V-sequence for eighth region in the field.
	[19:15]	X		SEQ8	Selected V-sequence for ninth region in the field.
	[21:20]			MULT_SWEEP0	Enables multiplier mode and/or sweep mode for Region 0: 0: Multiplier off/sweep off. 1: Multiplier off/sweep on. 2: Multiplier on/sweep off. 3: Multiplier on/sweep on.
	[23:22]			MULT_SWEEP1	Enables multiplier mode and/or sweep mode for Region 2.
	[25:24]			MULT_SWEEP2	Enables multiplier mode and/or sweep mode for Region 1.

Address	Data Bits	Default Value	Update Type	Mnemonic	Description
0x02	[12:0]	X	VD	HDLASTLEN	HD last line length. Line length of last line in the field.
	[14:13]	X		MULT_SWEEP3	Enables multiplier mode and/or sweep mode for Region 3.
	[16:15]	X		MULT_SWEEP4	Enables multiplier mode and/or sweep mode for Region 4.
	[18:17]	X		MULT_SWEEP5	Enables multiplier mode and/or sweep mode for Region 5.
	[20:19]	X		MULT_SWEEP6	Enables multiplier mode and/or sweep mode for Region 6.
	[22:21]	X		MULT_SWEEP7	Enables multiplier mode and/or sweep mode for Region 7.
	[24:23]	X		MULT_SWEEP8	Enables multiplier mode and/or sweep mode for Region 8.
	[25]			HDLASTLEN_13	HD last line length Bit 13 when 14-bit H-counter is enabled.
0x03	[12:0]	X	VD	SCP0	V-Sequence Change Position 0.
	[25:13]	X		SCP1	V-Sequence Change Position 1.
0x04	[12:0]	X	VD	SCP2	V-Sequence Change Position 2.
	[25:13]	X		SCP3	V-Sequence Change Position 3.
0x05	[12:0]	X	VD	SCP4	V-Sequence Change Position 4.
	[25:13]	X		SCP5	V-Sequence Change Position 5.
0x06	[12:0]	X	VD	SCP6	V-Sequence Change Position 6.
	[25:13]	X		SCP7	V-Sequence Change Position 7.
0x07	[12:0]	X	VD	SCP8	V-Sequence Change Position 8.
	[25:13]			VDLEN	VD field length (number of lines in the field).
0x08	[12:0]	X	VD	SGACTLINE1	SG Active Line 1.
	[25:13]	X		SGACTLINE2	SG Active Line 2 (set to SG Active Line 1 or maximum if not used).
0x09	[23:0]	X	VD	SGMASK	Masking of VSG outputs during SG active line.
0x0A	[12:0]	X	VD	CLPMASKSTART1	CLPOB Mask Region 1 start position. Set to 8191 to disable.
	[25:13]	X		CLPMASKEND1	CLPOB Mask Region 1 end position. Set to 0 to disable.
0x0B	[12:0]	X	VD	CLPMASKSTART2	CLPOB Mask Region 2 start position. Set to 8191 to disable.
	[25:13]	X		CLPMASKEND2	CLPOB Mask Region 2 end position. Set to 0 to disable.
0x0C	[12:0]	X	VD	CLPMASKSTART3	CLPOB Mask Region 3 start position. Set to 8191 to disable.
	[25:13]	X		CLPMASKEND3	CLPOB Mask Region 3 end position. Set to 0 to disable.
0x0D	[12:0]	X	VD	PBLKMASKSTART1	PBLK Mask Region 1 start position. Set to 8191 to disable.
	[25:13]	X		PBLKMASKEND1	PBLK Mask Region 1 end position. Set to 0 to disable.
0x0E	[12:0]	X	VD	PBLKMASKSTART2	PBLK Mask Region 2 start position. Set to 8191 to disable.
	[25:13]	X		PBLKMASKEND2	PBLK Mask Region 2 end position. Set to 0 to disable.
0x0F	[12:0]	X	VD	PBLKMASKSTART3	PBLK Mask Region 3 start position. Set to 8191 to disable.
	[25:13]	X		PBLKMASKEND3	PBLK Mask Region 3 end position. Set to 0 to disable.

OUTLINE DIMENSIONS

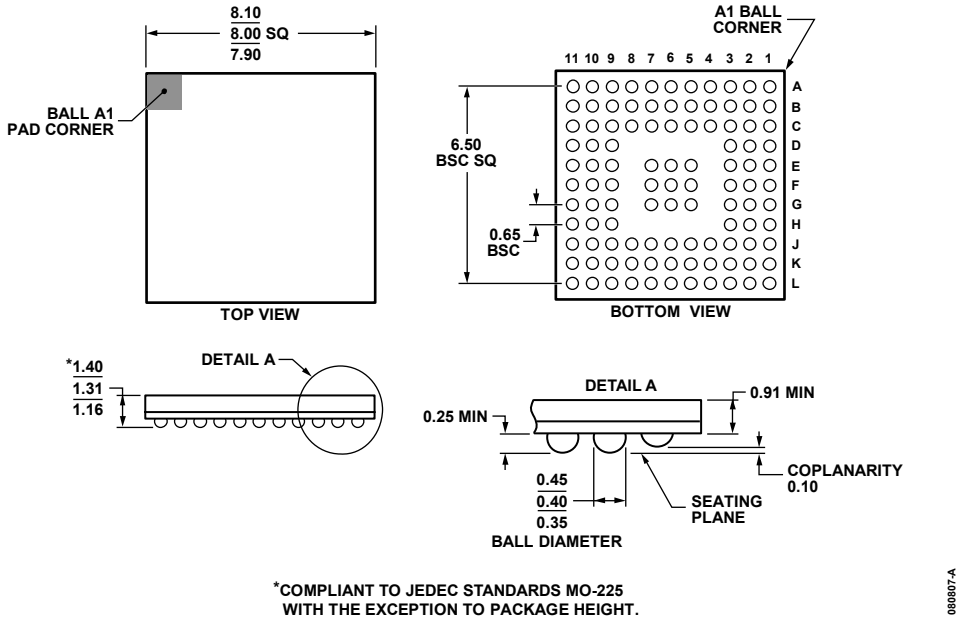


Figure 88. 105-Lead Chip Scale Package Ball Grid Array [CSP_BGA]
8 mm × 8 mm Body
(BC-105-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9992BBCZ[1]	–25°C to +85°C	105-Lead CSP_BGA	BC-105-1
AD9992BBCZRL[1]	–25°C to +85°C	105-Lead CSP_BGA	BC-105-1

[1] Z = RoHS Compliant Part.

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