THE DATASHEET OF

ADE7754ARZRL

Polyphase Multifunction Energy Metering IC with Serial Port

ADE7754

FEATURES

High Accuracy, Supports IEC 687/61036
Compatible with 3-Phase/3-Wire, 3-Phase/4-Wire and any Type of 3-Phase Services
Less than 0.1% Error in Active Power Measurement over a Dynamic Range of 1000 to 1
Supplies Active Energy, Apparent Energy, Voltage RMS, Current RMS, and Sampled Waveform Data
Digital Power, Phase, and Input Offset Calibration
On-Chip Temperature Sensor (±4°C Typical after Calibration)
On-Chip User Programmable Thresholds for Line Voltage SAG and Overdrive Detections
SPI Compatible Serial Interface with Interrupt Request Line (IRQ)
Pulse Output with Programmable Frequency
Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time
Single 5 V Supply

GENERAL DESCRIPTION

The ADE7754 is a high accuracy polyphase electrical energy measurement IC with a serial interface and a pulse output. The ADE7754 incorporates second order Σ-Δ ADCs, reference circuitry, temperature sensor, and all the signal processing required to perform active, apparent energy measurements, and rms calculation.

The ADE7754 provides different solutions for measuring active and apparent energy from the six analog inputs, thus enabling the use of the ADE7754 in various power meter services such as 3-phase/4-wire, 3-phase/3-wire, and 4-wire delta.

In addition to rms calculation, active and apparent power information, the ADE7754 provides system calibration features for each phase (i.e., channel offset correction, phase calibration, and gain calibration). The CF logic output provides instantaneous active power information.

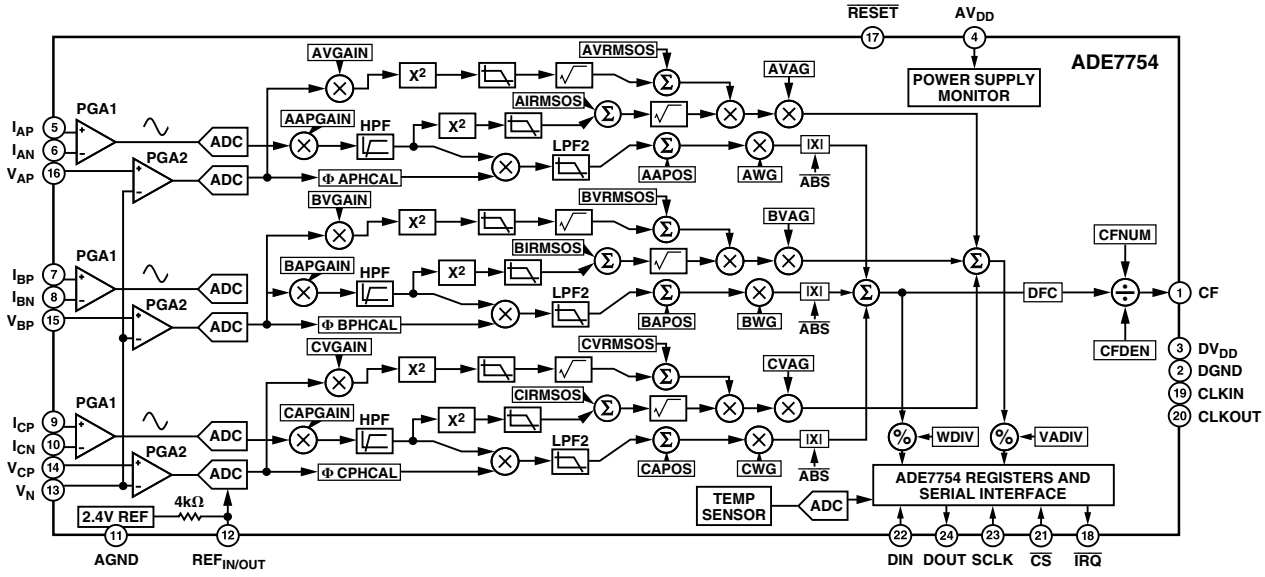
The ADE7754 has a waveform sample register that enables access to ADC outputs. The part also incorporates a detection circuit for short duration low or high voltage variations. The voltage threshold levels and the duration (number of half line cycles) of the variation are user programmable.

A zero-crossing detection is synchronized with the zero-crossing point of the line voltage of each of the three phases. The information collected is used to measure each line's period. It is also used internally to the chip in the line active energy and line apparent energy accumulation modes. This permits faster and more accurate calibration of the power calculations. This signal is also useful for synchronization of relay switching.

Data is read from the ADE7754 via the SPI serial interface. The interrupt request output ($\overline{IRQ}$) is an open-drain, active low logic output. The $\overline{IRQ}$ output goes active low when one or more interrupt events have occurred in the ADE7754. A status register indicates the nature of the interrupt.

The ADE7754 is available in a 24-lead SOIC package.

FUNCTIONAL BLOCK DIAGRAM



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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
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ADE7754—SPECIFICATIONS

(AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 10 MHz, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameters	Spec	Unit	Test Conditions/Comments
ACCURACY			
Active Power Measurement Error	0.1	% typ	Over a dynamic range 1000 to 1
Phase Error between Channels			
(PF = 0.8 Capacitive)	±0.05	° max	Phase lead 37°
(PF = 0.5 Inductive)	±0.05	° max	Phase lag 60°
AC Power Supply Rejection[1]			
Output Frequency Variation	0.01	% typ	IAP/N = IBP/N = ICP/N = ±100 mV rms
DC Power Supply Rejection[1]			
Output Frequency Variation	0.01	% typ	IAP/N = IBP/N = ICP/N = ±100 mV rms
Active Power Measurement Bandwidth	14	kHz typ	
V_{rms} Measurement Error	0.5	% typ	Over dynamic range of 20 to 1
V_{rms} Measurement Bandwidth	260	Hz typ	
I_{rms} Measurement Error	2	% typ	Over dynamic range of 100 to 1
I_{rms} Measurement Bandwidth	14	kHz	
ANALOG INPUTS			
Maximum Signal Levels	±500	mV peak max	Differential input: V_{AP}–V_N, V_{BP}–V_N, V_{CP}–V_N, I_{AP}–I_{AN}, I_{BP}–I_{BN}, I_{CP}–I_{CN}
Input Impedance (DC)	370	kΩ min	
Bandwidth (–3 dB)	14	kHz typ	
ADC Offset Error[1]	25	mV max	Uncalibrated error; See Terminology for details.
Gain Error[1]	±8	% typ	External 2.5 V reference
Gain Error Match[1]	±3	% typ	External 2.5 V reference
REFERENCE INPUT			
$REF_{IN/OUT}$ Input Voltage Range	2.6	V max	2.4 V + 8%
	2.2	V min	2.4 V – 8%
Input Impedance	3.7	kΩ max	
Input Capacitance	10	pF max	
TEMPERATURE SENSOR	±4	°C	Calibrated dc offset
ON-CHIP REFERENCE			
Reference Error	±200	mV max	
Temperature Coefficient	30	ppm/°C typ	
CLKIN			
Input Clock Frequency	10	MHz typ	
LOGIC INPUTS			
$\overline{RESET}$, DIN, SCLK, CLKIN, and $\overline{CS}$			
Input High Voltage, V_{INH}	2.4	V min	DV_{DD} = 5 V ± 5%
Input Low Voltage, V_{INL}	0.8	V max	DV_{DD} = 5 V ± 5%
Input Current, I_{IN}	±3	μA max	Typical 10 nA, V_{IN} = 0 V to DV_{DD}
Input Capacitance, C_{IN}	10	pF max	
LOGIC OUTPUTS			
CF, IRQ, DOUT, and CLKOUT			
Output High Voltage, V_{OH}	4	V min	DV_{DD} = 5 V ± 5%
Output Low Voltage, V_{OL}	1	V max	DV_{DD} = 5 V ± 5%
POWER SUPPLY			For specified performance
AV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
DV_{DD}	4.75	V min	5 V – 5%
	5.25	V max	5 V + 5%
AI_{DD}	7	mA max	At 5.25 V
DI_{DD}	18	mA max	At 5.25 V

NOTES

[1]See Terminology section for explanation of specifications.

[2]See plots in the Typical Performance Characteristics section.

Specifications subject to change without notice.

TIMING CHARACTERISTICS[1, 2]

(AV_{DD} = DV_{DD} = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 10 MHz XTAL, T_{MIN} to T_{MAX} = –40°C to +85°C, unless otherwise noted.)

Parameter	Spec	Unit	Test Conditions/Comments
Write Timing			
t_1	50	ns (min)	$\overline{CS}$ Falling Edge to First SCLK Falling Edge
t_2	50	ns (min)	SCLK Logic High Pulsewidth
t_3	50	ns (min)	SCLK Logic Low Pulsewidth
t_4	10	ns (min)	Valid Data Setup Time before Falling Edge of SCLK
t_5	5	ns (min)	Data Hold Time after SCLK Falling Edge
t_6	400	ns (min)	Minimum Time between the End of Data Byte Transfers
t_7	50	ns (min)	Minimum Time between Byte Transfers during a Serial Write
t_8	100	ns (min)	$\overline{CS}$ Hold Time after SCLK Falling Edge
Read Timing			
t_9[3]	4	µs (min)	Minimum Time between Read Command (i.e., a Write to Communication Register) and Data Read
t_{10}	50	ns (min)	Minimum Time between Data Byte Transfers during a Multibyte Read
t_{11}[4]	30	ns (min)	Data Access Time after SCLK Rising Edge following a Write to the Communications Register
t_{12}[5]	100	ns (max)	Bus Relinquish Time after Falling Edge of SCLK
	10	ns (min)	
t_{13}[5]	100	ns (max)	Bus Relinquish Time after Rising Edge of $\overline{CS}$
	10	ns (min)	

NOTES

[1]Sample tested during initial release and after any redesign or process change that may affect this parameter. All input signals are specified with tr = tf = 5 ns (10% to 90%) and timed from a voltage level of 1.6 V.

[2]See timing diagrams below and Serial Interface section of this data sheet.

[3]Minimum time between read command and data read for all registers except wavmode register, which is t_9 = 500 ns min.

[4]Measured with the load circuit in Figure 1 and defined as the time required for the output to cross 0.8 V or 2.4 V.

[5]Derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 1. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. The time quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

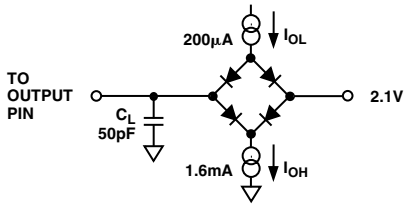


Figure 1. Load Circuit for Timing Specifications

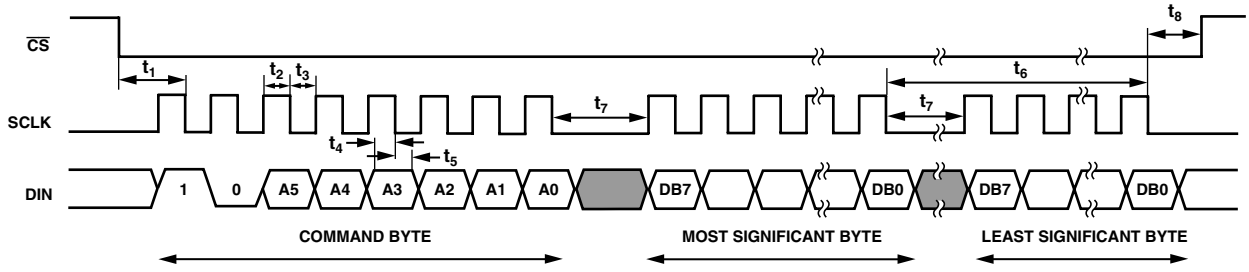


Figure 2. Serial Write Timing

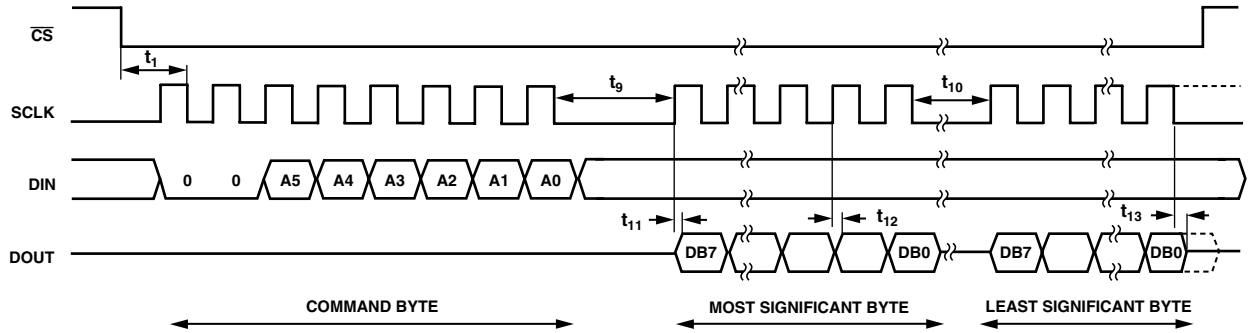


Figure 3. Serial Read Timing

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C, unless otherwise noted.)

AV_{DD} to AGND ..... –0.3 V to +7 V
DV_{DD} to DGND ..... –0.3 V to +7 V
DV_{DD} to AV_{DD} ..... –0.3 V to +0.3 V
Analog Input Voltage to AGND
I_{AP}, I_{AN}, I_{BP}, I_{BN}, I_{CP}, I_{CN}, V_{AP}, V_{BP}, V_{CP}, V_N .. –6 V to +6 V
Reference Input Voltage to AGND . –0.3 V to AV_{DD} + 0.3 V
Digital Input Voltage to DGND ... –0.3 V to DV_{DD} + 0.3 V
Digital Output Voltage to DGND .. –0.3 V to DV_{DD} + 0.3 V
Operating Temperature Range
Industrial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... 150°C
24-Lead SOIC, Power Dissipation ..... 88 mW
θ_{JA} Thermal Impedance ..... 53°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

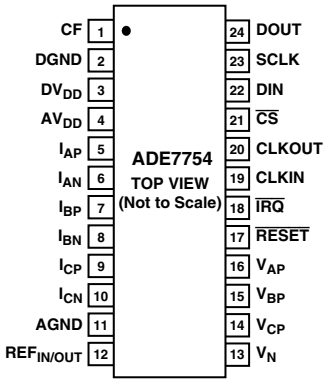
Model	Package Description	Package Option*
ADE7754AR	24-Lead SOIC	RW-24
ADE7754ARRL	24-Lead SOIC	RW-24 in Reel
EVAL-ADE7754EB		ADE7754 Evaluation Board

*RW = Small Outline (Wide Body Package in Tubes)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7754 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

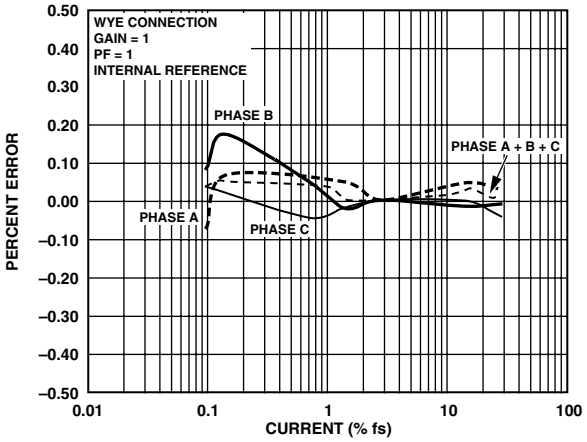


PIN FUNCTION DESCRIPTIONS

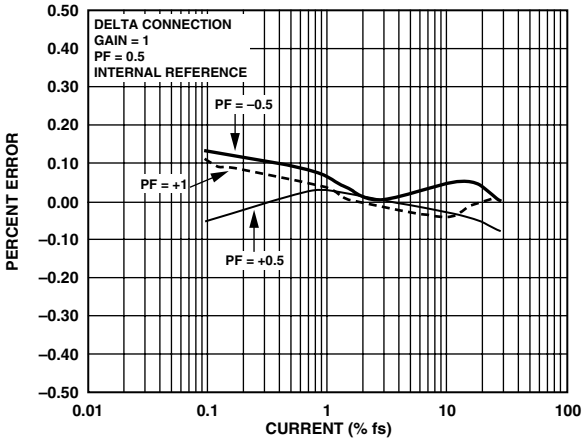
Pin No.	Mnemonic	Description
1	CF	Calibration Frequency Logic Output. This pin provides active power information. This output is intended to be used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CFNUM and CFDEN registers. See the Energy to Frequency Conversion section.
2	DGND	This pin provides the ground reference for the digital circuitry in the ADE7754 (i.e. multiplier, filters, and a digital-to-frequency converter). Because the digital return currents in the ADE7754 are small, this pin can be connected to the analog ground plane of the whole system. However high bus capacitance on the DOUT pin may result in noisy digital current, which could affect performance.

PIN FUNCTION DESCRIPTIONS (continued)

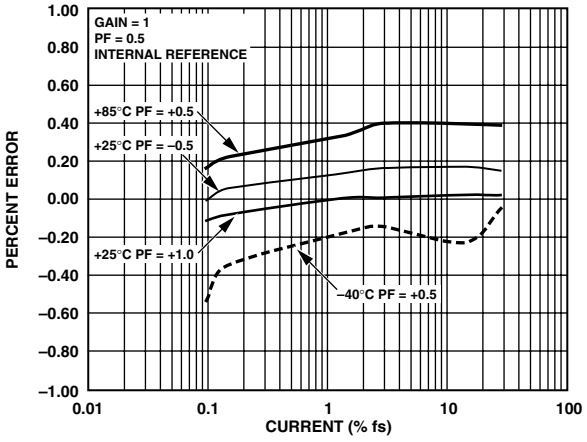
Pin No.	Mnemonic	Description
3	DV_{DD}	Digital Power Supply. The supply voltage should be maintained at 5 V ± 5% for specified operation. This pin should be decoupled to DGND with a 10 μF capacitor in parallel with a ceramic 100 nF capacitor.
4	AV_{DD}	Analog Power Supply. The supply should be maintained at 5 V ± 5% for specified operation. Every effort should be made to minimize power supply ripple and noise at this pin through the use of proper decoupling. The TPCs chart the power supply rejection performance. This pin should be to decoupled AGND with a 10 μF capacitor in parallel with a ceramic 100 nF capacitor.
5, 6; 7, 8; 9, 10	I_{AP}, I_{AN}; I_{BP}, I_{BN}; I_{CP}, I_{CN}	Analog Inputs for Current Channel. This channel is intended for use with the current transducer is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the gain selections of the internal PGA. See the Analog Inputs section. All inputs have internal ESD protection circuitry. An overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
11	AGND	Analog Ground Reference. Used for ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry such as anti-aliasing filters and current and voltage transducers. To keep ground noise around the ADE7754 to a minimum, the quiet ground plane should be connected only to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane.
12	$REF_{IN/OUT}$	This pin provides access to the on-chip voltage reference, which has a nominal value of 2.4 V ± 8% and a typical temperature coefficient of 30 ppm/°C. An external reference source may also be connected at this pin. In either case, this pin should be decoupled to AGND with a 1 μF ceramic capacitor.
13, 14; 15, 16	V_N, V_{CP}; V_{BP}, V_{AP}	Analog Inputs for the Voltage Channel. This channel is intended for use with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with maximum signal level of ±0.5 V with respect to V_N for specified operation. These inputs are voltage inputs with maximum differential input signal levels of ±0.5 V, ±0.25 V, and ±0.125 V, depending on the gain selections of the internal PGA. See the Analog Inputs section. All inputs have internal ESD protection circuitry. An overvoltage of ±6 V can be sustained on these inputs without risk of permanent damage.
17	$\overline{RESET}$	Reset. A logic low on this pin holds the ADCs and digital circuitry (including the serial interface) in a reset condition.
18	$\overline{IRQ}$	Interrupt Request Output. This is an active low, open-drain logic output. Maskable interrupts include active energy register at half level, apparent energy register at half level, and waveform sampling at up to 26 kSPS. See the Interrupts section.
19	CLKIN	Master Clock for ADCs and Digital Signal Processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7754. The clock frequency for specified operation is 10 MHz. Ceramic load capacitors of 22 pF to 33 pF should be used with the gate oscillator circuit. Refer to the crystal manufacturer's data sheet for load capacitance requirements.
20	CLKOUT	A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7754. The CLKOUT pin can drive one CMOS load when an external clock is supplied at CLKIN, or a crystal is used.
21	$\overline{CS}$	Chip Select. Part of the 4-wire serial interface. This active low logic input allows the ADE7754 to share the serial bus with several other devices. See the Serial Interface section.
22	DIN	Data Input for the Serial Interface. Data is shifted in at this pin on the falling edge of SCLK. See the Serial Interface section.
23	SCLK	Serial Clock Input for the Synchronous Serial Interface. All serial data transfers are synchronized to this clock. See the Serial Interface section. The SCLK has a Schmidt-trigger input for use with a clock source that has a slow edge transition time (e.g., opto-isolator outputs).
24	DOUT	Data Output for the Serial Interface. Data is shifted out at this pin on the rising edge of SCLK. This logic output is normally in a high impedance state unless it is driving data onto the serial data bus. See the Serial Interface section.



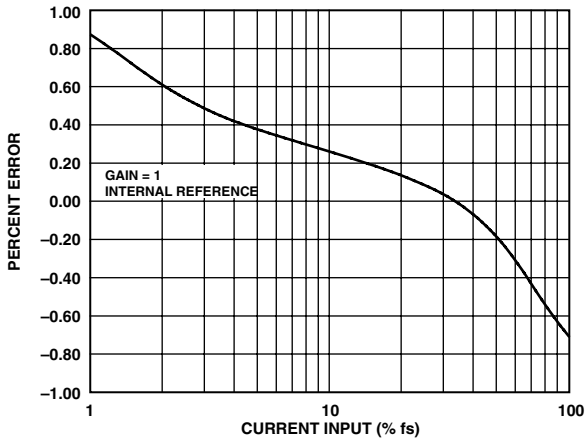
TPC 1. Real Power Error as a Percentage of Reading with Gain = 1 and Internal Reference (WYE Connection)



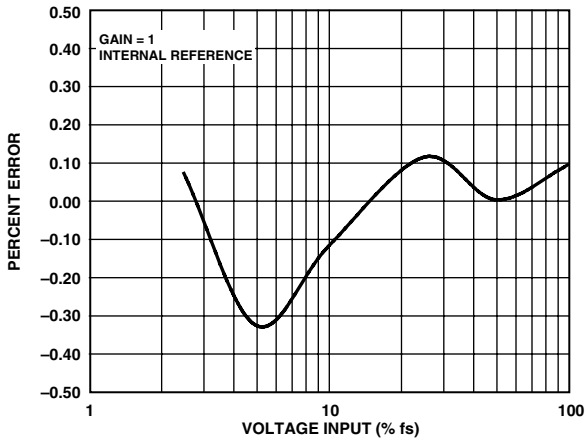
TPC 2. Real Power Error as a Percentage of Reading over Power Factor with Internal Reference (DELTA Connection)



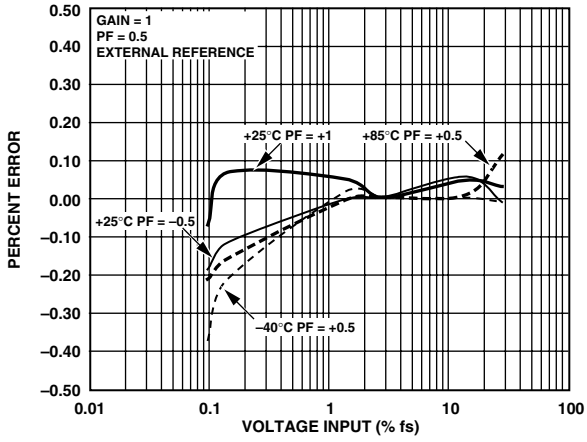
TPC 3. Real Power Error as a Percentage of Reading over Power Factor with Internal Reference (Gain = 1)



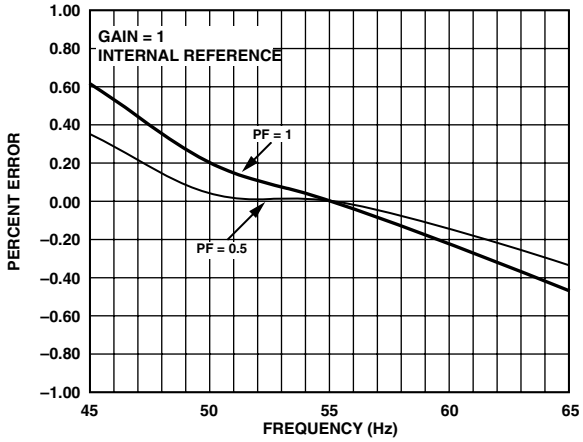
TPC 4. Current RMS Error as a Percentage of Reading with Internal Reference (Gain = 1)



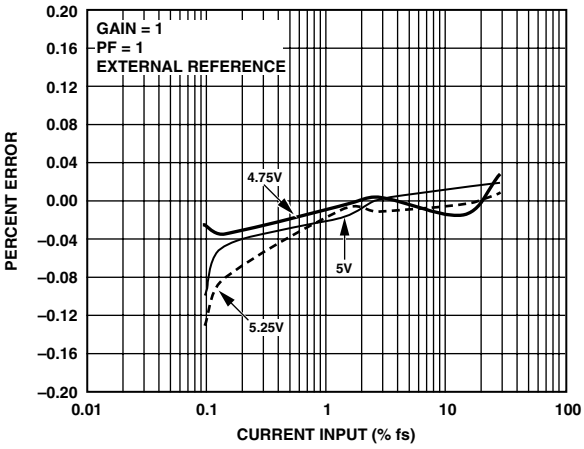
TPC 5. Voltage RMS Error as a Percentage of Reading with Internal Reference (Gain = 1)



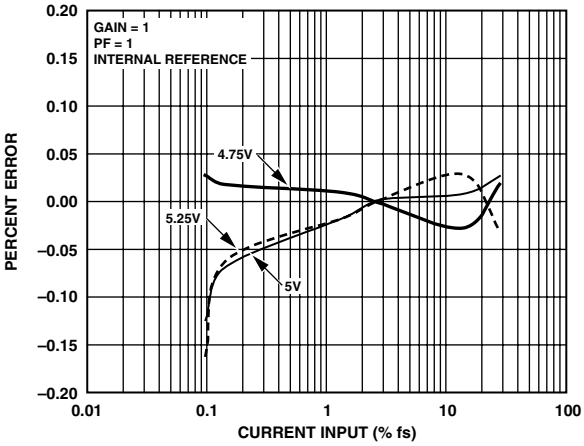
TPC 6. Real Power Error as a Percentage of Reading over Power Factor with External Reference (Gain = 1)



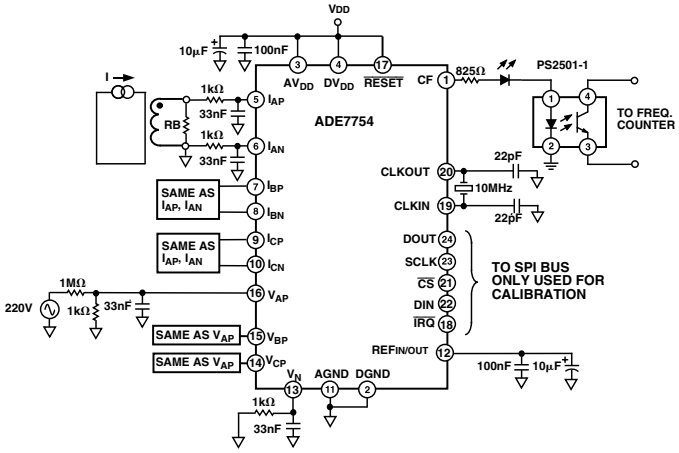
TPC 7. Real Power Error as a Percentage of Reading over Input Frequency with Internal Reference



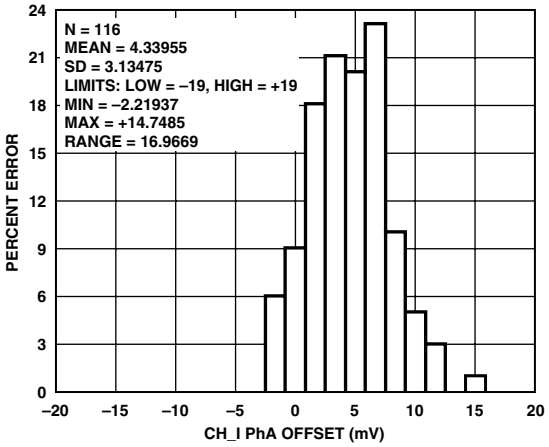
TPC 8. Real Power Error as a Percentage of Reading over Power Supply with External Reference (Gain = 1)



TPC 9. Real Power Error as a Percentage of Reading over Power Supply with Internal Reference (Gain = 1)



TPC 10. Test Circuit for Performance Curves



TPC 11. Current Channel Offset Distribution (Gain = 1)

TERMINOLOGY

Measurement Error
The error associated with the energy measurement made by the ADE7754 is defined by the formula

$$Percentage\ Error = \left(\frac{Energy\ Registered\ by\ ADE7754 - True\ Energy}{True\ Energy} \times 100\% \right)$$

Phase Error Between Channels
The HPF (high-pass filter) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels, a phase correction network is placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45 Hz to 65 Hz and ±0.2° over a range of 40 Hz to 1 kHz. This phase mismatch between the voltage and the current channels can be reduced further with the phase calibration register in each phase.

Power Supply Rejection
This quantifies the ADE7754 measurement error as a percentage of reading when power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained using the same input signal levels when an ac (175 mV rms/100 Hz) signal is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading. See the Measurement Error definition above.

For the dc PSR measurement, a reading at nominal supplies (5 V) is taken. A second reading is obtained using the same input signal levels when the power supplies are varied ±5%. Any error introduced is again expressed as a percentage of reading.

ADC Offset Error
This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection (see the TPCs). However, when HPFs are switched on, the offset is removed from the current channels and the power calculation is unaffected by this offset.

Gain Error
The gain error in the ADE7754 ADCs is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code. See the Current Channel ADC and the Voltage Channel ADC sections. The difference is expressed as a percentage of the ideal code.

Gain Error Match
Gain error match is defined as the gain error (minus the offset) obtained when switching between a gain of 1, 2, or 4. It is expressed as a percentage of the output ADC code obtained under a gain of 1.

POWER SUPPLY MONITOR

The ADE7754 contains an on-chip power supply monitor. The analog supply (AV_{DD}) is continuously monitored by the ADE7754. If the supply is less than 4 V ± 5%, the ADE7754 goes into an inactive state (i.e., no energy is accumulated when the supply voltage is below 4 V). This is useful to ensure correct device operation at power-up and during power-down. The power supply monitor has built-in hysteresis and filtering, providing a high degree of immunity to false triggering due to noisy supplies.

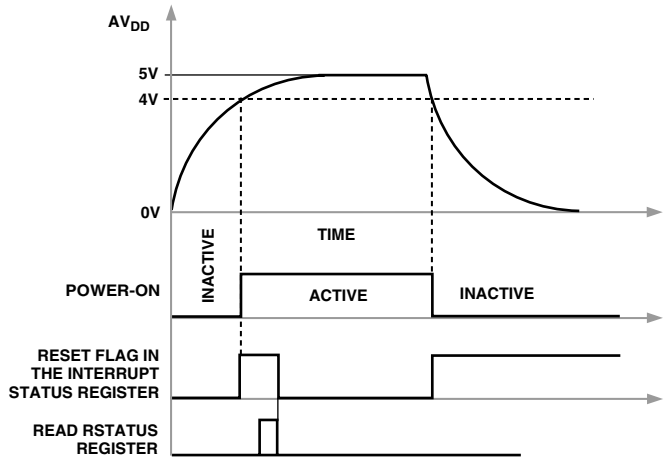


Figure 4. On-Chip Power Supply Monitoring

The RESET bit in the interrupt status register is set to Logic 1 when AV_{DD} drops below 4 V ± 5%. The RESET flag is always masked by the interrupt enable register and cannot cause the $\overline{IRQ}$ pin to go low. The power supply and decoupling for the part should ensure that the ripple at AV_{DD} does not exceed 5 V ± 5% as specified for normal operation.

ANALOG INPUTS

The ADE7754 has six analog inputs, divisible into two channels: current and voltage. The current channel consists of three pairs of fully differential voltage inputs: I_{AP}, I_{AN}; I_{BP}, I_{BN}; and I_{CP}, I_{CN}. The fully differential voltage input pairs have a maximum differential voltage of ±0.5 V. The voltage channel has three single-ended voltage inputs: V_{AP}, V_{BP}, and V_{CP}. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to V_N. Both the current channel and the voltage channel have a PGA (programmable gain amplifier) with possible gain selections of 1, 2, or 4. The same gain is applied to all the inputs of each channel.

The gain selections are made by writing to the gain register. Bits 0 and 1 select the gain for the PGA in the fully differential current channel. The gain selection for the PGA in the single-ended voltage channel is made via Bits 5 and 6. Figure 5 shows how a gain selection for the current channel is made using the gain register.

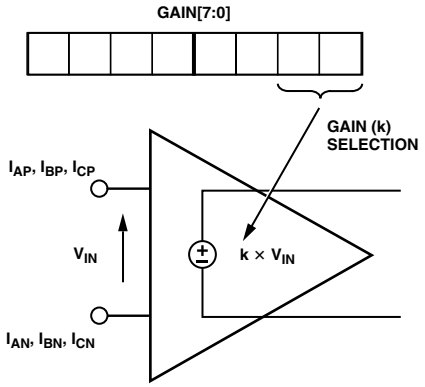


Figure 5. PGA in Current Channel

Figure 6 shows how the gain settings in PGA 1 (current channel) and PGA 2 (voltage channel) are selected by various bits in the gain register. The no-load threshold and sum of the absolute value can also be selected in the gain register. See Table X.

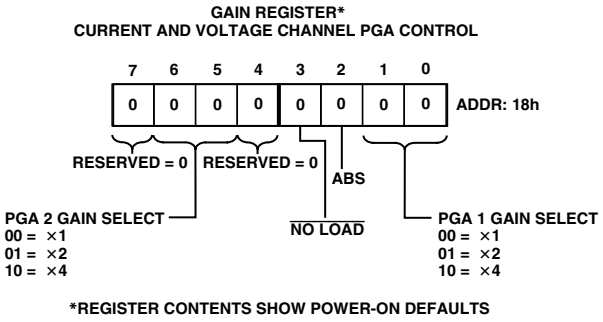


Figure 6. Analog Gain Register

ANALOG-TO-DIGITAL CONVERSION

The ADE7754 carries out analog-to-digital conversion using second order Σ-Δ ADCs. The block diagram in Figure 7 shows a first order (for simplicity) Σ-Δ ADC. The converter is made up of two parts, the Σ-Δ modulator and the digital low-pass filter.

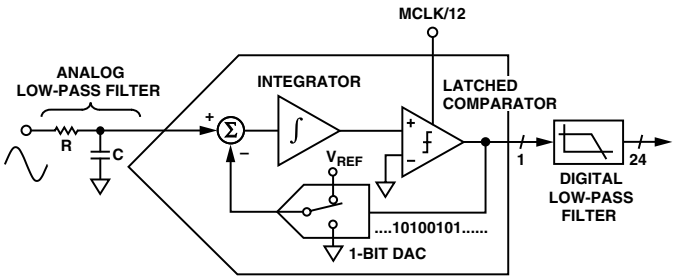


Figure 7. First Order (Σ-Δ) ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7754, the sampling clock is equal to CLKIN/12. The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and therefore the bit stream) will approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged will a meaningful result be obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. Averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling; the signal is sampled at a rate (frequency) many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7754 is CLKIN/12 (833 kHz), and the band of interest is 40 Hz to 2 kHz. Oversampling spreads the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered. See Figure 8.

Oversampling alone is not an efficient enough method to improve the signal to noise ratio (SNR) in the band of interest. For example, an oversampling ratio of 4 is required to increase the SNR by only 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, the quantization noise can be shaped so that most of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass type of response for the quantization noise. The result is that most of the noise is at the higher frequencies, where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 8.

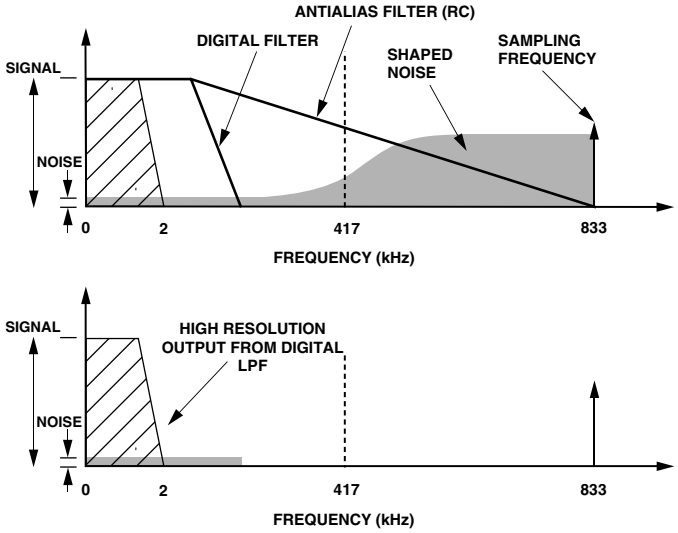


Figure 8. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialias Filter

Figure 7 shows an analog low-pass filter (RC) on the input to the modulator. This filter is used to prevent aliasing, an artifact of all sampled systems. Frequency components in the input signal to the ADC that are higher than half the sampling rate of the ADC appear in the sampled signal at a frequency below half the sampling rate. Figure 9 illustrates the effect; frequency components (arrows shown in black) above half the sampling frequency (also known as the Nyquist frequency), i.e., 417 kHz, get imaged or folded back down below 417 kHz (arrows shown in gray). This happens with all ADCs, regardless of the architecture. In the example shown, only frequencies near the sampling frequency, i.e., 833 kHz, will move into the band of interest for metering, i.e., 40 Hz to 2 kHz. This allows use of a very simple LPF (low-pass filter) to attenuate these high frequencies (near 900 kHz) and thus prevent distortion in the band of interest. A simple RC filter (single pole) with a corner frequency of 10 kHz produces an attenuation of approximately 40 dBs at 833 kHz. See Figure 9. This is sufficient to eliminate the effects of aliasing.

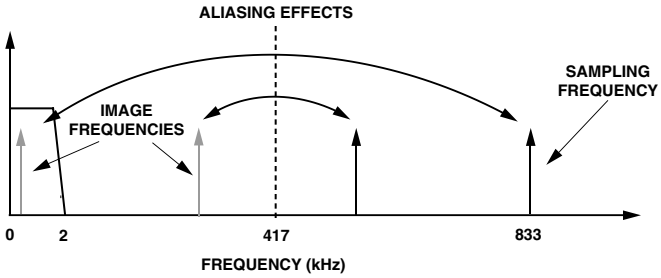


Figure 9. ADC and Signal Processing in Current Channel or Voltage Channel

CURRENT CHANNEL ADC

Figure 10 shows the ADC and signal processing chain for the input IA of the current channels (which are the same for IB and IC). In waveform sampling mode, the ADC outputs are signed twos complement 24-bit data-word at a maximum of 26 kSPS (kilo samples per second). The output of the ADC can be scaled by ±50% by using the APGAINs register. While the ADC outputs are 24-bit twos complement value, the maximum full-scale positive value from the ADC is limited to 400000h (+4,194,304d). The maximum full-scale negative value is limited to C00000h (–4,194,304d). If the analog inputs are overranged, the ADC output code clamps at these values. With the specified full-scale analog input signal of ±0.5 V, the ADC produces an output code between D70A3Eh (–2,684,354) and 28F5C2h (+2,684,354), as illustrated in Figure 10, which also shows a full-scale voltage signal being applied to the differential inputs I_{AP} and I_{AN}.

Current Channel ADC Gain Adjust

The ADC gain in each phase of the current channel can be adjusted using the multiplier and active power gain register (AAPGAIN[11:0], BAPGAIN, and CAPGAIN). The gain of the ADC is adjusted by writing a twos complement 12-bit word to the active power gain register. The following expression shows how the gain adjustment is related to the contents of that register:

$$Code = \left(ADC \times \left\{ 1 + \frac{AAPGAIN}{2^{12}} \right\} \right)$$

For example, when 7FFh is written to the active power gain register, the ADC output is scaled up by 50%: 7FFh = 2047d, 2047/212 = 0.5. Similarly, 800h = –2047d (signed twos complement) and ADC output is scaled by –50%. These two examples are illustrated in Figure 10.

Current Channel Sampling

The waveform samples of the current channel inputs may also be routed to the waveform register (wavmode register to select the speed and the phase) to be read by the system master (MCU). The active energy and apparent energy calculation remains uninterrupted during waveform sampling.

When in waveform sample mode, one of four output sample rates may be chosen using Bits 3 and 4 of the WAVMODE register (DTRT[1:0] mnemonic). The output sample rate may be 26.0 kSPS, 13.0 kSPS, 6.5 kSPS, or 3.3 kSPS. See the Waveform Mode Register section. By setting the WSMP bit in the interrupt enable register to Logic 1, the interrupt request output $\overline{IRQ}$ will go active low when a sample is available. The timing is shown in Figure 11. The 24-bit waveform samples are transferred from the ADE7754 one byte (eight bits) at a time, with the most significant byte shifted out first.

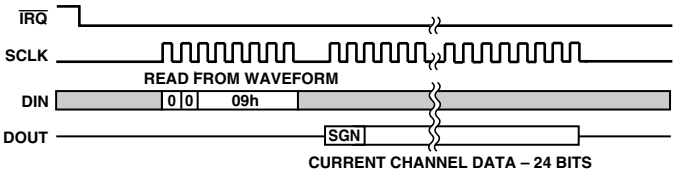


Figure 11. Waveform Sampling Current Channel

The interrupt request output $\overline{IRQ}$ stays low until the interrupt routine reads the reset status register. See the Interrupt section.

Note that if the WSMP bit in the interrupt enable register is not set to Logic 1, no data is available in the waveform register.

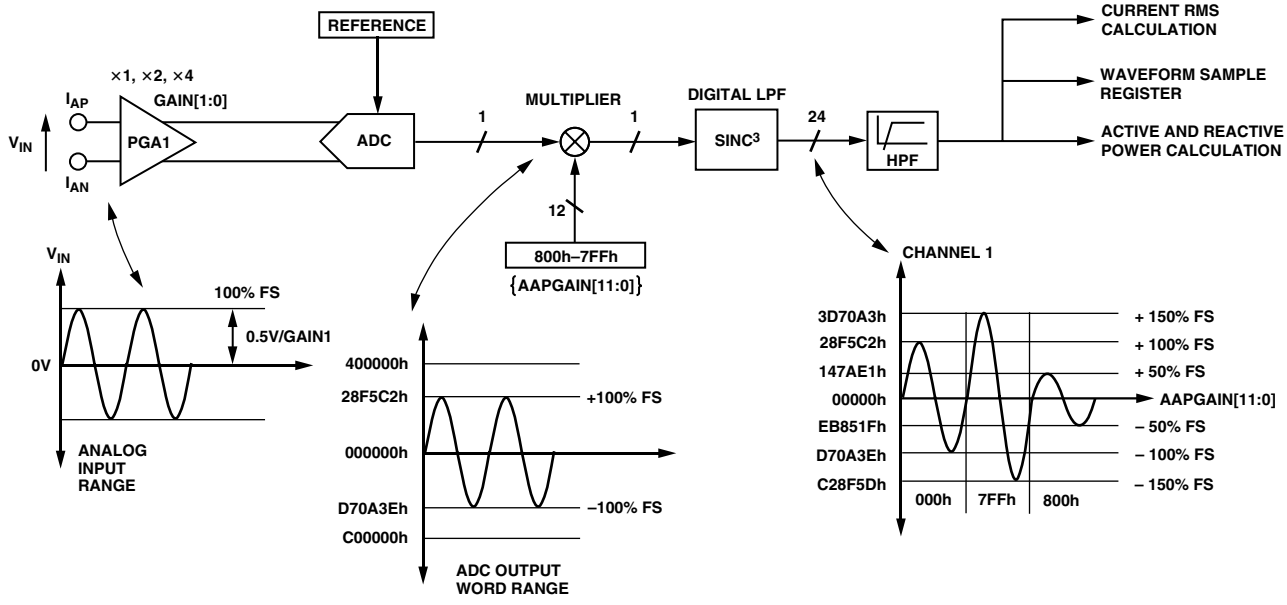


Figure 10. ADC and Signal Processing in Current Channel

VOLTAGE CHANNEL ADC

Figure 12 shows the ADC and signal processing chain for the input VA in voltage channel (which is the same for VB and VC).

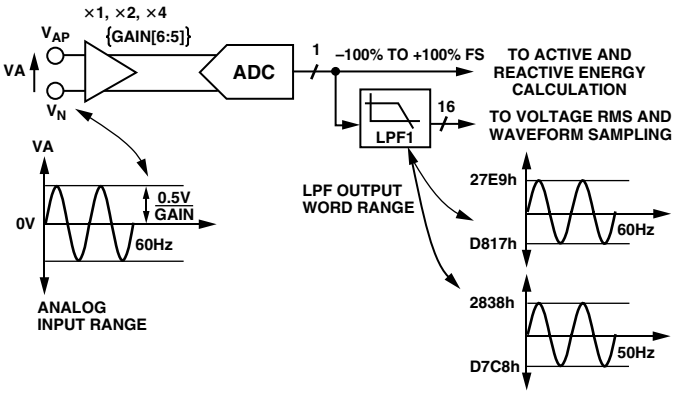


Figure 12. ADC and Signal Processing in Voltage Channel

For energy measurements, the output of the ADC (one bit) is passed directly to the multiplier and is not filtered. This solution avoids a wide-bits multiplier and does not affect the accuracy of the measurement. An HPF is not required to remove any dc offset since it is only required to remove the offset from one channel to eliminate errors in the power calculation.

In the voltage channel, the samples may also be routed to the WFORM register (WAVMODE to select VA, VB, or VC and sampling frequency). However, before being passed to the waveform register, the ADC output is passed through a single-pole, low-pass filter with a cutoff frequency of 260 Hz. The plots in Figure 13 show the magnitude and phase response of this filter. The filter output code of any inputs of the voltage channel swings between D70Bh (–10,485d) and 28F5h (+10,485d) for full-scale sine wave inputs. This has the effect of attenuating the signal. For example, if the line frequency is 60 Hz, the signal at the output of LPF1 will be attenuated by 3%.

$$|H(f)| = \frac{1}{\sqrt{1+\left(\frac{60\ Hz}{260\ Hz}\right)^2}} = 0.974 = -0.2\ dBs$$

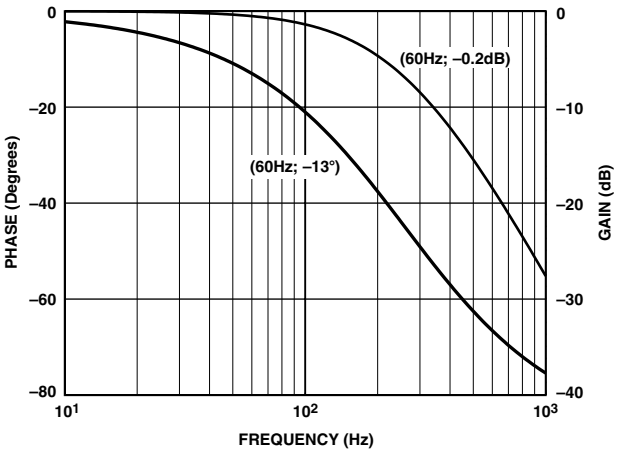


Figure 13. Magnitude and Phase Response of LPF1

Note that LPF1 does not affect the power calculation because it is used only in the waveform sample mode and rms calculation.

In waveform sample mode, one of four output sample rates can be chosen by using Bits 3 and 4 of the WAVMODE register. The available output sample rates are 26 kSPS, 13.5 kSPS, 6.5 kSPS, or 3.3 kSPS. The interrupt request output $\overline{IRQ}$ signals a new sample availability by going active low. The voltage waveform register is a twos complement 16-bit register. Because the waveform register is a 24-bit signed register, the waveform data from the voltage input is located in the 16 LSB of the waveform register. The sign of the 16-bit voltage input value is not extended to the upper byte of the waveform register. The upper byte is instead filled with zeros. 24-bit waveform samples are transferred from the ADE7754 one byte (eight bits) at a time, with the most significant byte shifted out first. The timing is the same as that for the current channels and is shown in Figure 11.

ZERO-CROSSING DETECTION

The ADE7754 has rising edge zero-crossing detection circuits for each of voltage channels (V_{AP}, V_{BP}, and V_{CP}). Figure 14 shows how the zero-cross signal is generated from the output of the ADC of the voltage channel.

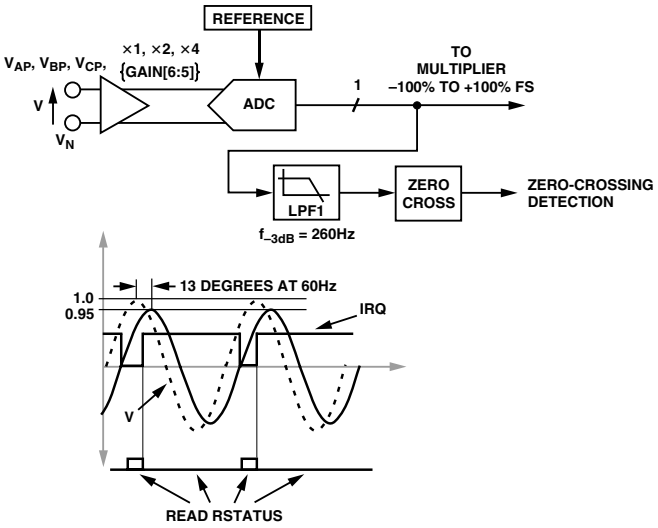


Figure 14. Zero-Crossing Detection on Voltage Channel

The zero-crossing interrupt is generated from the output of LPF1, which has a single pole at 260 Hz (CLKIN = 10 MHz). As a result, there is a phase lag between the analog input signal of the voltage channel and the output of LPF1. The phase response of this filter is shown in the Voltage Channel ADC section. The phase lag response of LPF1 results in a time delay of approximately 0.6 ms (@ 60 Hz) between the zero crossing on the analog inputs of voltage channel and the falling of IRQ.

When one phase crosses zero from negative to positive values (rising edge), the corresponding flag in the interrupt status register (Bits 7 to 9) is set Logic 1. An active low in the $\overline{IRQ}$ output also appears if the corresponding ZX bit in the interrupt enable register is set to Logic 1.

The flag in the interrupt status register is reset to 0 when the interrupt status register with reset (RSTATUS) is read. Each phase has its own interrupt flag and enable bit in the interrupt register.

In addition to the enable bits, the zero-crossing detection interrupt of each phase is enabled/disabled by setting the ZXSEL bits of the MMODE register (Address 0Bh) to Logic 1 or 0, respectively.

Zero-Crossing Timeout

Each zero-crossing detection has an associated internal timeout register (not accessible to the user). This unsigned, 16-bit register is decremented (1 LSB) every 384/CLKIN seconds. The registers are reset to a common user programmed value (i.e., zero cross timeout register—ZXTOUT, Address 12h) every time a zero crossing is detected on its associated input. The default value of ZXTOUT is FFFFh. If the internal register decrements to zero before a zero crossing at the corresponding input is detected, it indicates an absence of a zero crossing in the time determined by the ZXTOUT. The ZXTO detection bit of the corresponding phase in the interrupt status register is then switched on (Bits 4 to 6). An active low on the $\overline{IRQ}$ output also appears if the SAG enable bit for the corresponding phase in the interrupt enable register is set to Logic 1.

In addition to the enable bits, the zero-crossing timeout detection interrupt of each phase is enabled/disabled by setting the ZXSEL bits of the MMODE register (Address 0Bh) to Logic 1 or Logic 0, respectively. When the zero-crossing timeout detection is disabled by this method, the ZXTO flag of the corresponding phase is switched on all the time.

Figure 15 shows the mechanism of the zero-crossing timeout detection when the line voltage A stays at a fixed dc level for more than CLKIN/384 × ZXTOUT seconds.

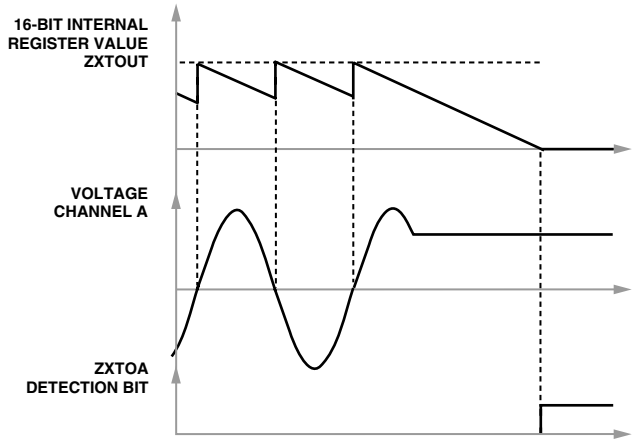


Figure 15. Zero-Crossing Timeout Detection

PERIOD MEASUREMENT

The ADE7754 also provides the period measurement of the line voltage. The period is measured on the phase specified by Bits 0 to 1 of the MMODE register. The period register is an unsigned 15-bit register and is updated every period of the selected phase. Bits 0 and 1 and Bits 4 to 6 of the MMODE register select the phase for the period measurement; both selections should indicate the same phase. The ZXSEL bits of the MMODE register (Bits 4 to 6) enable the phases on which the period measurement can be done. The PERDSEL bits select the phase for period measurement within the phases selected by the ZXSEL bits.

The resolution of this register is 2.4 μs/LSB when CLKIN = 10 MHz, which is 0.014% when the line frequency is 60 Hz. When the line frequency is 60 Hz, the value of the period register is approximately 6944d. The length of the register enables the measurement of line frequencies as low as 12.7 Hz.

LINE VOLTAGE SAG DETECTION

The ADE7754 can be programmed to detect when the absolute value of the line voltage of any phase drops below a certain peak value for a number of half cycles. All phases of the voltage channel are controlled simultaneously. This condition is illustrated in Figure 16.

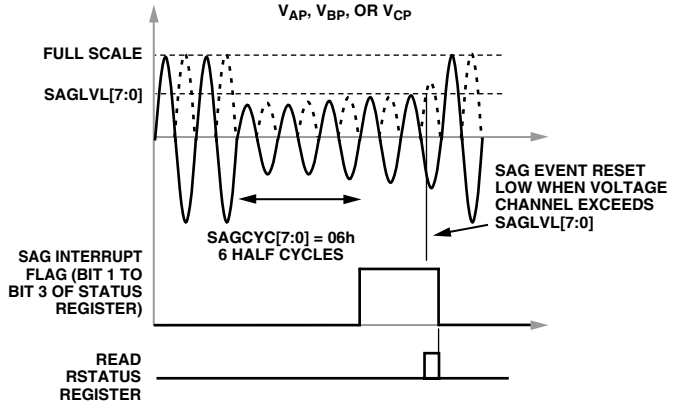


Figure 16. SAG Detection

Figure 16 shows a line voltage falling below a threshold set in the SAG level register (SAGLVL[7:0]) for nine half cycles. Since the SAG cycle register indicates a six half-cycle threshold (SAGCYC[7:0]=06h), the SAG event is recorded at the end of the sixth half-cycle by setting the SAG flag of the corresponding phase in the interrupt status register (Bits 1 to 3 in the interrupt status register). If the SAG enable bit is set to Logic 1 for this phase (Bits 1 to 3 in the interrupt enable register), the $\overline{IRQ}$ logic output goes active low. See the Interrupts section. All the phases are compared to the same parameters defined in the SAGLVL and SAGCYC registers.

SAG Level Set

The content of the SAG level register (one byte) is compared to the absolute value of the most significant byte output from the voltage channel ADC. Thus, for example, the nominal maximum code from the voltage channel ADC with a full-scale signal is 28F5h. See the Voltage Channel ADC section.

Therefore, writing 28h to the SAG level register puts the SAG detection level at full scale and sets the SAG detection to its most sensitive value.

Writing 00h puts the SAG detection level at 0. The detection of a decrease of an input voltage is in this case hardly possible. The detection is made when the content of the SAGLVL register is greater than the incoming sample.

PEAK DETECTION

The ADE7754 also can be programmed to detect when the absolute value of the voltage or the current channel of one phase exceeds a certain peak value. Figure 17 illustrates the behavior of the peak detection for the voltage channel.

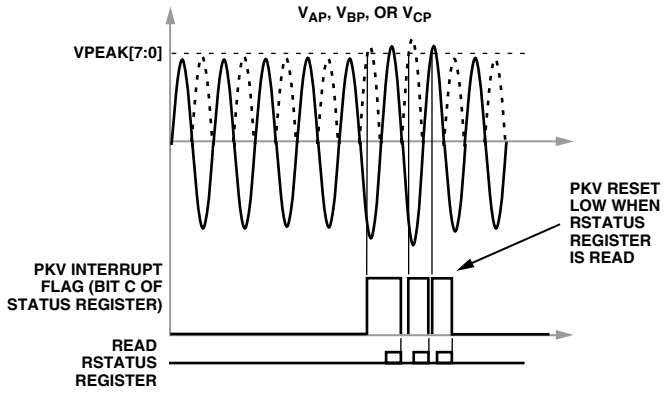


Figure 17. Peak Detection

Bits 2 and 3 of the measurement mode register define the phase supporting the peak detection. Current and voltage of this phase can be monitored at the same time. Figure 17 shows a line voltage exceeding a threshold set in the voltage peak register (VPEAK[7:0]). The voltage peak event is recorded by setting the PKV flag in the interrupt status register. If the PKV enable bit is set to Logic 1 in the interrupt enable register, the $\overline{\text{IRQ}}$ logic output goes active low. See the Interrupts section.

Peak Level Set

The contents of the VPEAK and IPEAK registers compare to the absolute value of the most significant byte output of the selected voltage and current channels, respectively. Thus, for example, the nominal maximum code from the current channel ADC with a full-scale signal is 28F5C2h. See the Current Channel Sampling section. Therefore, writing 28h to the IPEAK register will put the current channel peak detection level at full scale and set the current peak detection to its least sensitive value. Writing 00h puts the current channel detection level at zero. The detection is done when the content of the IPEAK register is smaller than the incoming current channel sample.

TEMPERATURE MEASUREMENT

The ADE7754 also includes an on-chip temperature sensor. A temperature measurement is made every 4/CLKIN seconds. The output from the temperature sensing circuit is connected to an ADC for digitizing. The resulting code is processed and placed into the temperature register (TEMP[7:0]) which can be read by the user and has an address of 08h. See the Serial Interface section. The contents of the temperature register are signed (twos complement) with a resolution of 4°C/LSB. The temperature register produces a code of 00h when the ambient temperature is approximately 129°C. The value of the register is temperature register = (temperature (°C) – 129)/4. The temperature in the ADE7754 has an offset tolerance of approximately ±5°C. The error can be easily calibrated out by an MCU.

PHASE COMPENSATION

When the HPFs are disabled, the phase difference between the current channel (IA, IB, and IC) and the voltage channel (VA, VB, and VC) is zero from dc to 3.3 kHz. When the HPFs are enabled, the current channels have a phase response as shown in Figure 18a and 18b. The magnitude response of the filter is shown in Figure 18c. As seen from in the plots, the phase response is almost zero from 45 Hz to 1 kHz. This is all that is required in typical energy measurement applications.

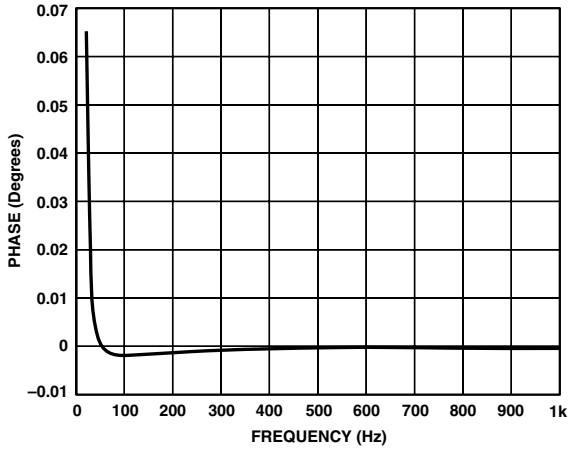


Figure 18a. Phase Response of the HPF and Phase Compensation (10 Hz to 1 kHz)

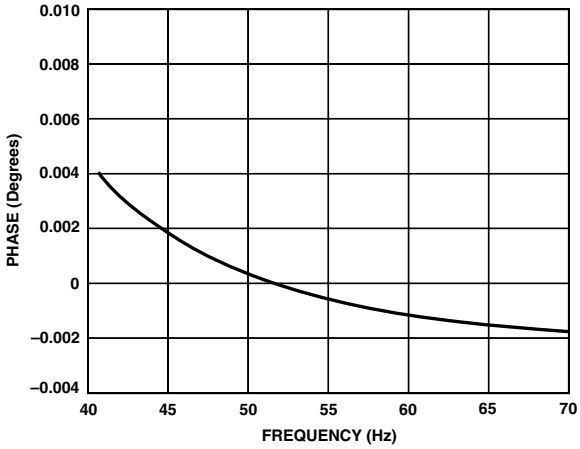


Figure 18b. Phase Response of the HPF and Phase Compensation (40 Hz to 70 Hz)

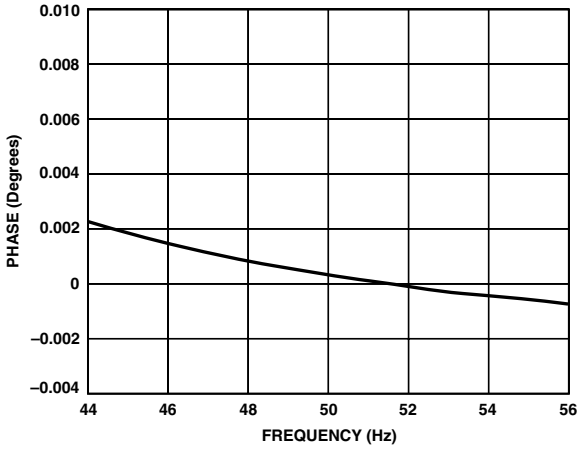


Figure 18c. Gain Response of HPF and Phase Compensation (Deviation of Gain as % of Gain at 54 Hz)

Despite being internally phase compensated, the ADE7754 must work with transducers that may have inherent phase errors. For example, a phase error of 0.1° to 0.3° is not uncommon for a CT (current transformer). These phase errors can vary from part to part, and they must be corrected in order to perform accurate power calculations. The errors associated with phase mismatch

are particularly noticeable at low power factors. The ADE7754 provides a means of digitally calibrating these small phase errors. The ADE7754 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for small phase errors. Because the compensation is in time, this technique should be used only for small phase errors in the range of 0.1° to 0.5°. Correcting large phase errors using a time shift technique can introduce significant phase errors at higher harmonics.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are twos complement, 5-bit signed registers that can vary the time delay in the voltage channel signal path from –19.2 µs to +19.2 µs (CLKIN = 10 MHz). One LSB is equivalent to 1.2 µs. With a line frequency of 50 Hz, this gives a phase resolution of 0.022° at the fundamental (i.e., 360° × 1.2 µs × 50 Hz).

Figure 19 illustrates how the phase compensation is used to remove a 0.091° phase lead in IA of the current channel caused by an external transducer. In order to cancel the lead (0.091°) in IA of the current channel, a phase lead must also be introduced into VA of the voltage channel. The resolution of the phase adjustment allows the introduction of a phase lead of 0.086°. The phase lead is achieved by introducing a time advance into VA. A time advance of 4.8 µs is made by writing –4 (1Ch) to the time delay block (APHCAL[4:0]), thus reducing the amount of time delay by 4.8 µs. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624.

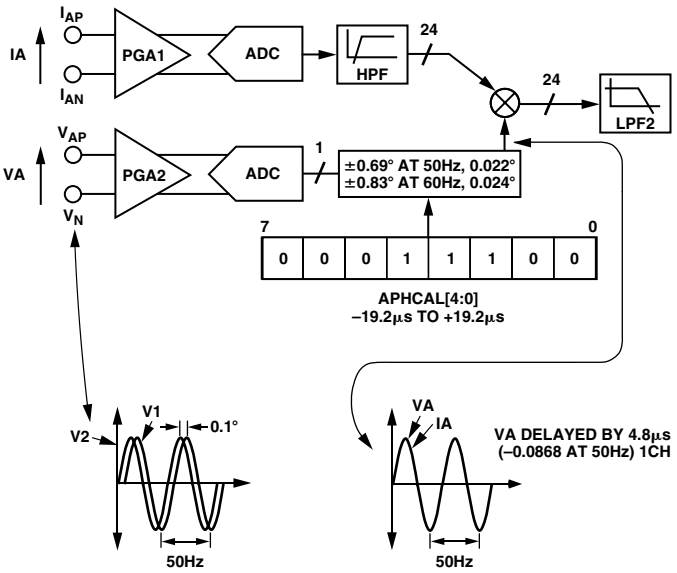


Figure 19. Phase Calibration

ROOT MEAN SQUARE MEASUREMENT

Root Mean Square (rms) is a fundamental measurement of the magnitude of an ac signal. Its definition can be practical or mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of heat in the same load. Mathematically the rms value of a continuous signal f(t) is defined as

$$F_{rms}=\sqrt{\frac{1}{T}\times\int_0^T f^2(t)dt} \quad (1)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root:

$$F_{rms}=\sqrt{\frac{1}{N}\times\sum_{i=1}^{N} f^2(i)} \quad (2)$$

The method used to calculate the rms value in the ADE7754 is to low-pass filter the square of the input signal (LPF3) and take the square root of the result.

With

$$V(t)=V_{rms}\times\sqrt{2}\times\sin(\omega t)$$

then

$$V(t)\times V(t)={V_{rms}}^2-{V_{rms}}^2\times\cos(2\omega t)$$

The rms calculation is simultaneously processed on the six analog input channels. Each result is available on separate registers.

Current RMS Calculation

Figure 20 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel waveform sampling mode. Note that the APGAIN adjustment affects the result of the rms calculation. See the Current RMS Gain Adjust section. The current rms values are stored in unsigned 24-bit registers (AIRMS, BIRMS, and CIRMS). One LSB of the current rms register is equivalent to 1 LSB of a current waveform sample. The update rate of the current rms measurement is CLKIN/12. With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code which is approximately ±2,684,354d. See the Current Channel ADC section. The equivalent rms values of a full-scale ac signal is 1,898,124d. With offset calibration, the current rms measurement provided in the ADE7754 is accurate within ±2% for signal input between full scale and full scale/100.

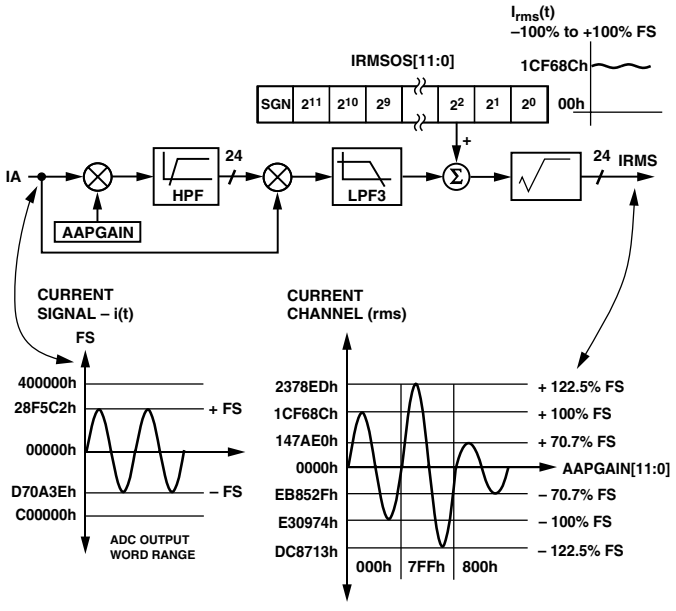


Figure 20. Current RMS Signal Processing

Note that a crosstalk between phases can appear in the ADE7754 current rms measurements. This crosstalk follows a specific

pattern. Current rms measurements of Phase A are corrupted by the signal on the Phase C current input, current rms measurements of Phase B are corrupted by the signal on the Phase A current input, and current rms measurements of Phase C are corrupted by the signal on the Phase B current input. This crosstalk is present only on the current rms measurements and does not affect the regular active power measurements. The level of the crosstalk is dependent on the level of the noise source and the phase angle between the noise source and the corrupted signal. The level of the crosstalk can be reduced by writing 01F7h to the address 3Dh. This 16-bit register is reserved for factory operation and should not be written to any other value. When the current inputs are 120° out of phase and the register 3Dh is set to 01F7h, the level of the current rms crosstalk is below 2%.

Current RMS Gain Adjust

The active power gain registers (AAPGAIN[11:0], BAPGAIN, and CAPGAIN) affect the active power and current rms values. Calibrating the current rms measurements with these registers is not recommended. The conversion of the current rms registers values to amperes has to be done in an external microcontroller with a specific ampere/LSB constant for each phase. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624. Due to gain mismatches between phases, the calibration of the ampere/LSB constant has to be done separately for each phase. One-point calibration is sufficient for this calibration. The active power gain registers ease the calibration of the active energy calculation in MODE 1 and 2 of the WATMODE register.

If the APGAIN registers are used for active power calibration (WATMOD bits in WATMode register = 1 or 2), the current rms values are changed by the active power gain register value as described in the expression

$$Current\ rms\ register\ Phase\ A = \left(rms \times \sqrt{1 + \frac{AAPGAIN}{2^{12}}} \right)$$

For example, when 7FFh is written to the active power gain register, the ADC output is scaled up by 22.5%. Similarly, 800h = –2047d (signed twos complement) and ADC output is scaled by 29.3%. These two examples are illustrated in Figure 20.

Current RMS Offset Compensation

The ADE7754 incorporates a current rms offset compensation for each phase (AIRMSOS, BIRMSOS, and CIRMSOS). These are 12-bit twos complement signed registers that can be used to remove offsets in the current rms calculations. An offset may exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The offset calibration will allow the contents of the I_{RMS} registers to be maintained at zero when no current is being consumed.

n LSB of the current rms offset are equivalent to 32768 × n LSB of the square of the current rms register. Assuming that the maximum value from the current rms calculation is 1,898,124 decimal with full-scale ac inputs, then 1 LSB of the current rms offset represents 0.0058% of measurement error at –40 dB below full scale.

$$I_{rms} = \sqrt{{I_{rms_0}}^2 + IRMSOS \times 32768}$$

where I_{rmso} is the rms measurement without offset correction.

The current rms offset compensation should be done by testing the rms results at two non-zero input levels. One measurement can be done close to full scale and the other at approximately full scale/100. The current offset compensation can then be derived using these measurements. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624.

Voltage RMS Calculation

Figure 21 shows the details of the signal processing chain for the rms calculation on one of the phases of the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel waveform sampling mode. The output of the voltage channel ADC can be scaled by ±50% by changing VGAIN registers to perform an overall apparent power calibration. See the Apparent Power Calculation section. The VGAIN adjustment affects the rms calculation because it is done before the rms signal processing. The voltage rms values are stored in unsigned 24-bit registers (AVRMS, BVRMS, and CVRMS). 256 LSB of the voltage rms register is approximately equivalent to one LSB of a voltage waveform sample. The update rate of the voltage rms measurement is CLKIN/12.

With the specified full-scale ac analog input signal of 0.5 V, the LPF1 produces an output code that is approximately ±10,217 decimal at 60 Hz. See the Voltage Channel ADC section. The equivalent rms value of a full-scale ac signal is approximately 7,221d (1C35h), which gives a voltage rms value of 1,848,772d (1C35C4h) in the V_{RMS} register. With offset calibration, the voltage rms measurement provided in the ADE7754 is accurate within ±0.5% for signal input between full scale and full scale/20.

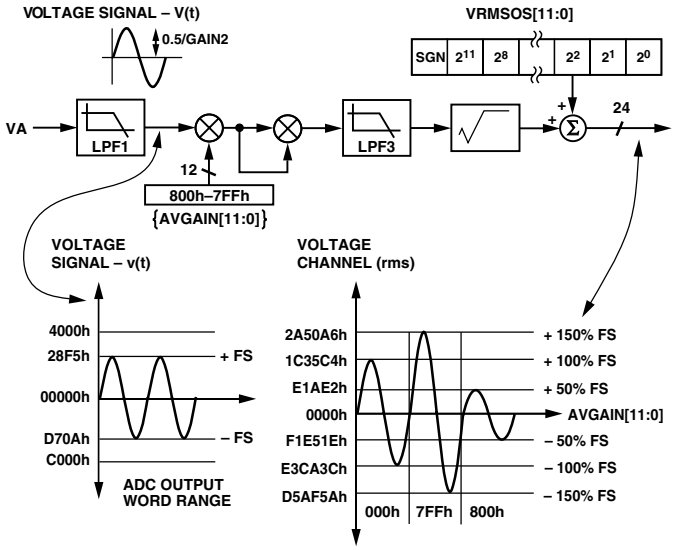


Figure 21. Voltage RMS Signal Processing

Voltage RMS Gain Adjust

The voltage gain registers (AVGAIN[11:0], BVGAIN, and CVGAIN) affect the apparent power and voltage rms values. Calibrating the voltage rms measurements with these registers is not recommended. The conversion of the voltage rms registers values to volts has to be done in an external microcontroller with a specific volt/LSB constant for each phase. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624. Due to gain mismatches between phases, the calibration of the volt/LSB constant has to be done separately for each phase. One point calibration is sufficient for this calibration. The voltage gain registers are aimed to ease the calibration of the apparent energy calculation in MODE 1 and MODE 2 of the VAMODE register.

If the VGAIN registers are used for apparent power calibration (WATMOD bits in VAMODE register = 1 or 2), the voltage rms values are changed by voltage gain register value as described in the expression

$$Voltage\ rms\ register\ Phase\ A = \left(rms \times \left\{ 1 + \frac{AVGAIN}{2^{12}} \right\} \right)$$

For example, when 7FFh is written to the voltage gain register, the ADC output is scaled up by +50%. 7FFh = 2047d, 2047/ 2^{12} = 0.5. Similarly, 800h = –2047d (signed twos complement) and ADC output is scaled by –50%. These two examples are illustrated in Figure 21.

Voltage RMS Offset Compensation

The ADE7754 incorporates a voltage rms offset compensation for each phase (AVRMSOS, BVRMSOS, and CVRMSOS). These are 12-bit twos complement signed registers that can be used to remove offsets in the voltage rms calculations. An offset may exist in the rms calculation due to input noises and offsets in the input samples. The offset calibration allows the contents of the V_{RMS} registers to be maintained at zero when no voltage is applied.

n LSB of the voltage rms offset are equivalent to 64 × n LSB of the voltage rms register. Assuming that the maximum value from the voltage rms calculation is 1,898,124 decimal with full-scale ac inputs, then 1 LSB of the voltage rms offset represents 0.07% of measurement error at –26 dB below full scale.

$$V_{rms} = V_{rms_0} + VRMSOS \times 64$$

where V_{rmso} is the rms measurement without offset correction.

The voltage rms offset compensation should be done by testing the rms results at two non-zero input levels. One measurement can be done close to full scale and the other at approximately full scale/10. The voltage offset compensation can then be derived from these measurements. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624.

ACTIVE POWER CALCULATION

Electrical power is defined as the rate of energy flow from source to load. It is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. Equation 5 gives an expression for the instantaneous power signal in an ac system.

$$v(t) = \sqrt{2}V \sin(\omega t) \quad (3)$$

$$i(t) = \sqrt{2}I \sin(\omega t) \quad (4)$$

where V = rms voltage and I = rms current.

$$p(t) = v(t) \times i(t)$$
$$p(t) = VI - VI \cos(2\omega t) \quad (5)$$

The average power over an integral number of line cycles (n) is given by the expression in Equation 6.

$$P = \frac{1}{nT} \int_0^{nT} p(t)dt = VI \quad (6)$$

where T is the line cycle period. P is referred to as the active or real power. Note that the active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 5 (i.e., VI). This is the relationship used to calculate active power in the ADE7754 for each phase. The instantaneous power signal $p(t)$ is generated by multiplying the current and voltage signals in each phase. The dc component of the instantaneous power signal in each phase (A, B, and C) is then extracted by LPF2 (low-pass filter) to obtain the active power information on each phase. This process is illustrated in Figure 22. In a polyphase system, the total electrical power is simply the sum of the real power in all active phases. The solutions available to process the total active power are discussed in the following section.

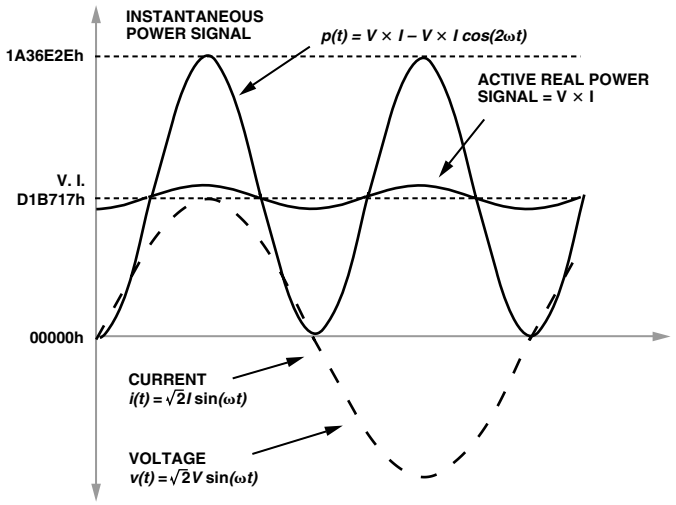


Figure 22. Active Power Calculation

Since LPF2 does not have an ideal brick wall frequency response (see Figure 23), the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Since the ripple is sinusoidal in nature, it is removed when the active power signal is integrated to calculate the energy. See the Energy Calculation section.

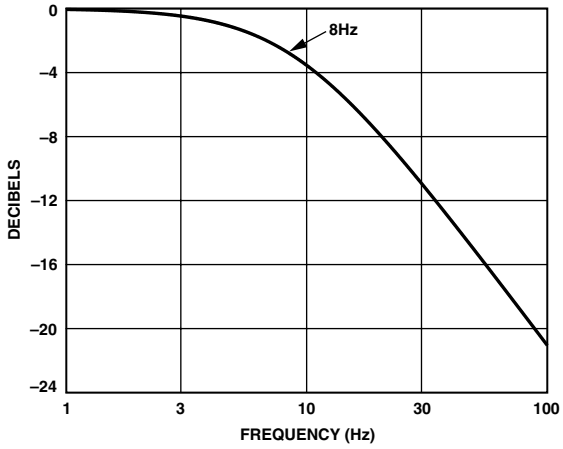


Figure 23. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase

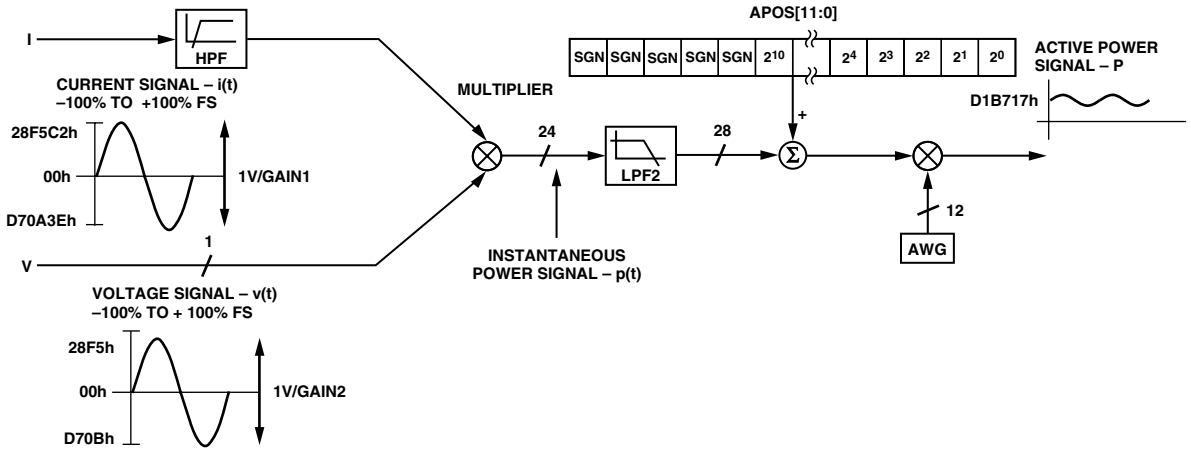


Figure 24. Active Power Signal Processing

Figure 24 shows the signal processing in each phase for the active power in the ADE7754.

Figure 25 shows the maximum code (hexadecimal) output range of the active power signal (after AWG). Note that the output range changes depending on the contents of the active power gain and watt gain registers. See the Current Channel ADC section. The minimum output range is given when the active power gain and watt gain registers contents are equal to 800h, and the maximum range is given by writing 7FFh to the active power gain and watt gain registers. These can be used to calibrate the active power (or energy) calculation in the ADE7754 for each phase and the total active energy. See the Total Active Power Calculation section.

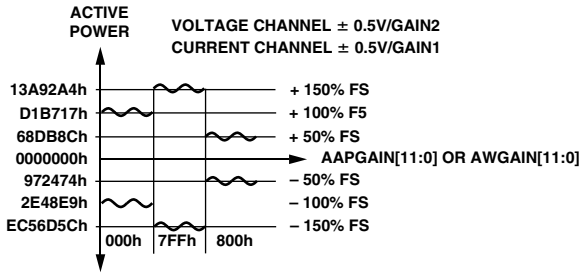


Figure 25. Active Power Calculation Output Range

Power Offset Calibration

The ADE7754 also incorporates an active offset register on each phase (AAPOS, BAPOS, and CAPOS). These are signed twos complement 12-bit registers that can be used to remove offsets in the active power calculations. An offset may exist in the power calculation because of crosstalk between channels on the PCB or in the IC itself. The offset calibration allows the contents of the active power register to be maintained at zero when no power is being consumed.

One LSB in the active power offset register is equivalent to one LSB in the 28-bit energy bus displayed in Figure 24. Each time power is added to the internal active energy register, the content of the active power offset register is added. See the Total Active Power Calculation section. Assuming the average value from LPF2 is 8637BCh (8,796,092d) with full ac scale inputs on current channel and voltage channel, then one LSB in the LPF2 output is equivalent to 0.011% of measurement error at –60 dB down of full scale. See the Calibration of a 3-Phase Meter Based on the ADE7754 Application Note AN-624.

Reverse Power Information

The ADE7754 detects when the current and voltage channels of any of the three phase inputs have a phase difference greater than 90° (i.e., $|\Phi_A|$ or $|\Phi_B|$ or $|\Phi_C| > 90°$). This mechanism can detect wrong connection of the meter or generation of active energy.

The reverse power information is available for Phase A, Phase B, and Phase C, respectively, by reading Bits 12 to 14 of the CFNUM register. See Table XI. The state of these bits represents the sign of the active power of the corresponding phase. Logic 1 corresponds to negative active power.

The AENERGY phase selection bits (WATSEL bits of the WATMode register) enable the negative power detection per phase. If Phase A is enabled in the AENERGY accumulation, Bit 5 of WATMode register sets to Logic 1 and the negative power detection for Phase A—Bit 12 of CFNUM register—indicates the direction of the active energy. If Phase A is disabled in the AENERGY register, the negative power bit for Phase A is set to Logic 0.

TOTAL ACTIVE POWER CALCULATION

The sum of the active powers coming from each phase provides the total active power consumption. Different combinations of the three phases can be selected in the sum by setting Bits 7 and 6 of the WATMode register (mnemonic WATMOD[1:0]). Figure 26 demonstrates the calculation of the total active power, which depends on the configuration of the WATMOD bits in the WATMode register. Each term of the formula can be disabled or enabled by setting WATSEL bits respectively to Logic 0 or Logic 1 in the WATMode register. The different configurations are described in Table I.

Table I. Total Active Power Calculation

WATMOD	WATSEL0	WATSEL1	WATSEL2
0d	$V_A \times I_A^*$	$+ V_B \times I_B^*$	$+ V_C \times I_C^*$
1d	$V_A \times (I_A^* – I_B^*)$	+ 0	$+ V_C \times (I_C^* – I_B^*)$
2d	$V_A \times (I_A^* – I_B^*)$	+ 0	$+ V_C \times I_C^*$

Note that I_A^*, I_B^*, and I_C^* represent the current channel samples after APGAIN correction and high-pass filtering.

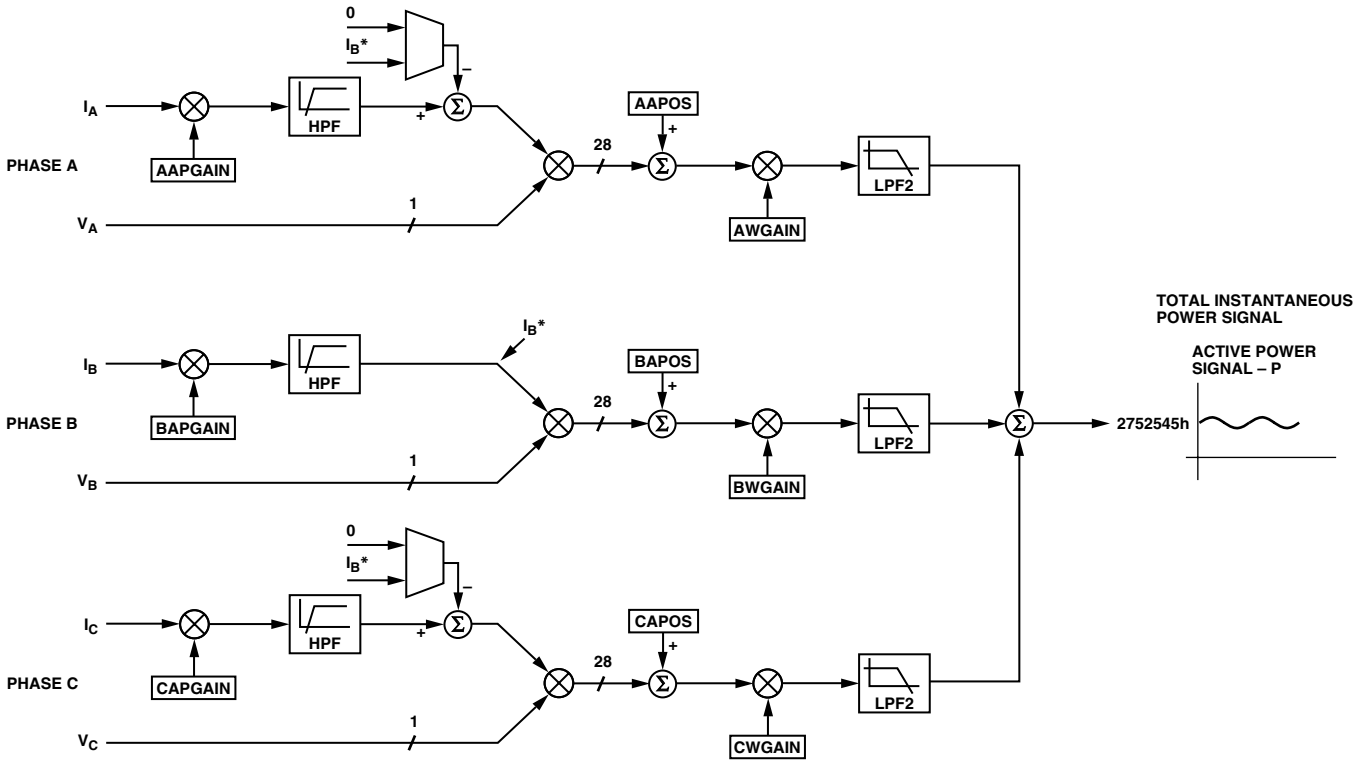


Figure 26. Total Active Power Consumption Calculation

For example, for WATMOD = 1, when all the gains and offsets corrections are taken into consideration, the formula that is used to process the active power is

Total Active Power =

$$\left(V_A \times \left(\left(1+\frac{AAPGAIN}{2^{12}}\right)\times I_A - \left(1+\frac{BAPGAIN}{2^{12}}\right)\times I_B\right) + AAPOS\right)\times\left(1+\frac{AWG}{2^{12}}\right)$$
$$+\left(V_C \times \left(\left(1+\frac{CAPGAIN}{2^{12}}\right)\times I_C - \left(1+\frac{BAPGAIN}{2^{12}}\right)\times I_B\right) + CAPOS\right)\times\left(1+\frac{CWG}{2^{12}}\right)$$

Depending on the polyphase meter service, an appropriate formula should be chosen to calculate the active power. The American ANSI C12.10 standard defines the different configurations of the meter. Table II describes which mode should be chosen for each configuration.

Table II. Meter Form Configuration

ANSI	Meter Form	WATMOD	WATSEL
5S/13S	3-wire Delta	0	3 or 5 or 6
6S/14S	4-wire Wye	1	5
8S/15S	4-wire Delta	2	5
9S/16S	4-wire Wye	0	7

Different gain calibration parameters are offered in the ADE7754 to cover the calibration of the meter in different configurations. Note that in Mode 0, the APGAIN and WGAIN registers have the same effect on the end result. In this case, APGAIN registers should be set at their default value and the gain adjustment should be made with the WGAIN registers.

ENERGY CALCULATION

As stated earlier, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$P = \frac{dE}{dt} \tag{7}$$

where P = power and E = energy.

Conversely energy is given as the integral of power.

$$E = \int P dt \tag{8}$$

The ADE7754 achieves the integration of the active power signal by continuously accumulating the active power signal in an internal non readable 54-bit energy register. The active energy register (AENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 9 expresses the relationship

$$E = \int p(t)dt = \underset{T\to 0}{Lim}\left\{\sum_{n=0}^{\infty} p(nT)\times T\right\} \tag{9}$$

where n is the discrete time sample number and T is the sample period.

The discrete time sample period (T) for the accumulation register in the ADE7754 is 0.4 µs (4/10 MHz). In addition to calculating the energy, this integration removes any sinusoidal component that may be in the active power signal. Figure 27 shows a graphical representation of this discrete time integration or accumulation. The active power signal is continuously added to the internal energy register. Because this addition is a signed addition, negative energy will be subtracted from the active energy contents.

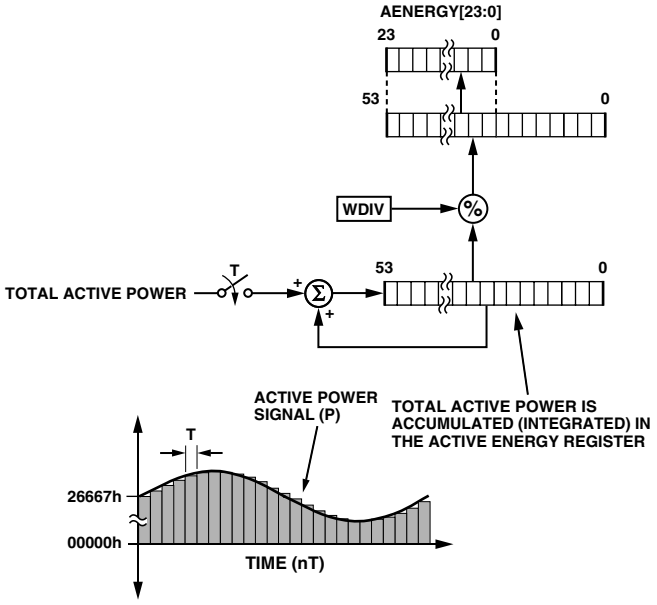


Figure 27. Active Energy Calculation

The 54-bit value of the internal energy register is divided by WDIV. If the value in the WDIV register is 0, then the internal active energy register is divided by 1. WDIV is an 8-bit unsigned register. The upper 24-bits of the result of the division are then available in the 24-bit active energy register. The AENERGY and RAENERGY registers read the same internal active energy register. They differ by the state in which they are leaving the internal active energy register after a read. Two operations are held when reading the RAENERGY register: read and reset to 0 the internal active energy register. Only one operation is held when reading the AENERGY register: read the internal active energy register.

Figure 28 shows the energy accumulation for full-scale (sinusoidal) signals on the analog inputs. The three displayed curves illustrate the minimum time it takes the energy register to roll over when the individual watt gain registers contents are all equal to 3FFh, 000h, and 800h. The watt gain registers are used to carry out a power calibration in the ADE7754. As shown, the fastest integration time occurs when the watt gain registers are set to maximum full scale, i.e., 3FFh.

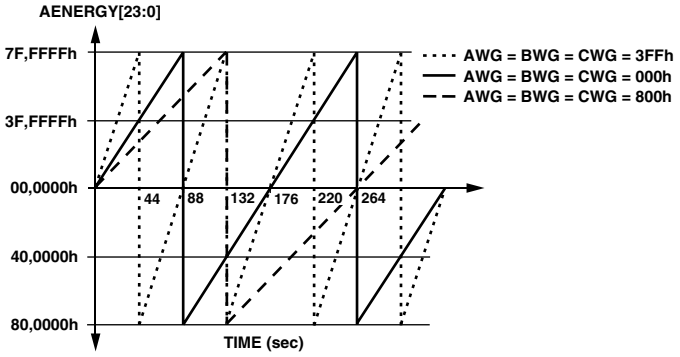


Figure 28. Energy Register Roll-Over Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the active energy register contents roll over to full-scale negative (80,0000h) and continue increasing in value when the power or energy flow is positive. See Figure 28.

Conversely, if the power is negative, the energy register would underflow to full scale positive (7F,FFFFh) and continue decreasing in value.

By using the interrupt enable register, the ADE7754 can be configured to issue an interrupt ($\overline{\text{IRQ}}$) when the active energy register is half full (positive or negative).

Integration Times Under Steady Load

As mentioned in the last section, the discrete time sample period (T) for the accumulation register is 0.4 µs (4/CLKIN). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 000h, the average word value from each LPF2 is D1B717h. See Figures 22 and 24. The maximum value that can be stored in the active energy register before it overflows is $2^{23} - 1$ or 7F,FFFFh. As the average word value is added to the internal register, which can store $2^{53} - 1$ or 1F,FFFF,FFFF,FFFFh before it overflows, the integration time under these conditions with WDIV = 0 is calculated as follows:

$$Time = \frac{1F,FFFF,FFFF,FFFFh}{3 \times D1B717h} \times 0.4\ \mu s = 88\ s$$

When WDIV is set to a value different from 0, the integration time varies as shown in Equation 10.

$$Time = Time_{WDIV=0} \times WDIV \quad (10)$$

The WDIV register can be used to increase the time before the active energy register overflows, thereby reducing the communication needs with the ADE7754.

Energy to Frequency Conversion

The ADE7754 also provides energy-to-frequency conversion for calibration purposes. After initial calibration at manufacture, the manufacturer or the customer will often verify the energy meter calibration. One convenient way to verify the meter calibration is for the manufacturer to provide an output frequency proportional to the energy or active power under steady load conditions. This output frequency can provide a simple single-wire, optically isolated interface to external calibration equipment. Figure 29 illustrates the energy to frequency conversion in the ADE7754.

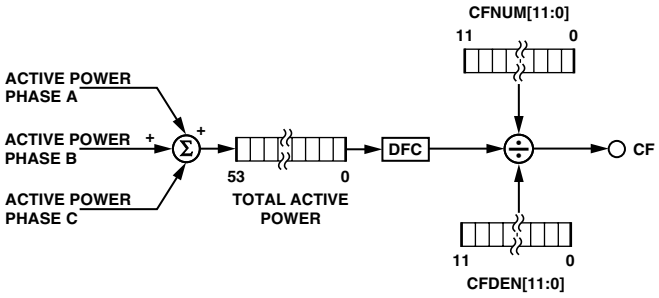


Figure 29. ADE7754 Energy to Frequency Conversion

A digital to frequency converter (DFC) is used to generate the CF pulsed output. The DFC generates a pulse each time one LSB in the active energy register is accumulated. An output pulse is generated when CFDEN/CFNUM pulses are generated at the DFC output. Under steady load conditions, the output frequency is proportional to the active power. The maximum output frequency (CFNUM = 00h and CFDEN = 00h) with full scale ac signals on the three phases (i.e., current channel and voltage channel is approximately 96 kHz).

The ADE7754 incorporates two registers to set the frequency of CF (CFNUM[11:0] and CFDEN[11:0]). These are unsigned 12-bit registers that can be used to adjust the frequency of CF to a wide range of values. These frequency scaling registers are 12-bit registers that can scale the output frequency by $1/2^{12}$ to 1 with a step of $1/2^{12}$.

If the value 0 is written to any of these registers, the value 1 would be applied to the register. The ratio CFNUM/CFDEN should be smaller than 1 to ensure proper operation. If the ratio of the registers CFNUM/CFDEN is greater than 1, the CF frequency can no longer be guaranteed to be a consistent value.

For example, if the output frequency is 18.744 kHz and the contents of CFDEN are zero (000h), then the output frequency can be set to 6.103 Hz by writing BFFh to the CFDEN register.

The output frequency will have a slight ripple at a frequency equal to twice the line frequency because of imperfect filtering of the instantaneous power signal used to generate the active power signal. See the Active Power Calculation section. Equation 5 gives an expression for the instantaneous power signal. This is filtered by LPF2, which has a magnitude response given by Equation 11.

$$|H(f)| = \frac{1}{\sqrt{1+\frac{f^2}{8^2}}} \tag{11}$$

The active power signal (output of the LPF2) can be rewritten as

$$p(t) = VI - \left\{ \frac{VI}{\sqrt{1+\left(\frac{2f_l}{8}\right)^2}} \right\} \times \cos(4\pi\ f_l\ t) \tag{12}$$

where f_l is the line frequency (e.g., 60 Hz).

From Equation 8

$$E(t) = VIt - \left\{ \frac{VI}{4\pi\ f_l \sqrt{1+\left(\frac{2f_l}{8}\right)^2}} \right\} \times \sin(4\pi\ f_l\ t) \tag{13}$$

Equation 13 shows that there is a small ripple in the energy calculation due to a sin(2ωt) component. This is graphically displayed in Figure 30. The ripple becomes larger as a percentage of the frequency at larger loads and higher output frequencies. Choosing a lower output frequency at CF for calibration can significantly reduce the ripple. Also, averaging the output frequency by using a longer gate time for the counter achieves the same results.

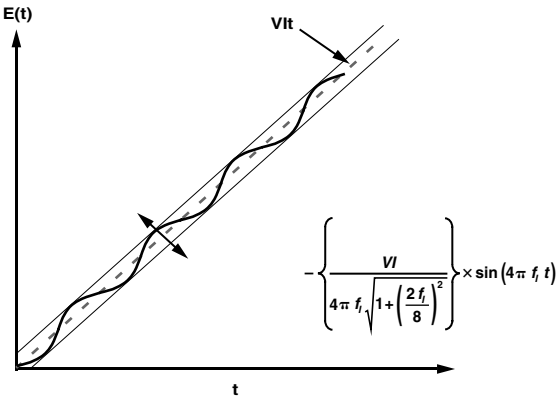


Figure 30. Output Frequency Ripple

No Load Threshold

The ADE7754 includes a selectable "no load threshold" or "startup current" feature that eliminates any creep effects in the active energy measurement of the meter. When enabled, this function is independently applied on each phase's active power calculation. This mode is selected by default and can be disabled

by setting to Logic 1 Bit 3 of the gain register (Address 18h). See Table X. Any load generating an active power amplitude lower than the minimum amplitude specified will not be taken into account when accumulating the active power from this phase.

The minimum instantaneous active power allowed in this mode is 0.005% of the full-scale amplitude. Because the maximum active power value is 13,743,895d with full-scale analog input, the no-load threshold is 687d. For example, an energy meter with maximum inputs of 220 V and 40 A and Ib = 10 A, the maximum instantaneous active power is 3,435,974d, assuming that both inputs represent half of the analog input full scale. As the no-load threshold represents 687d, the start-up current represents 8 mA or 0.08% of Ib.

Mode Selection of the Sum of the Three Active Energies

The ADE7754 can be configured to execute the arithmetic sum of the three active energies, $Wh = Wh_{\phi A} + Wh_{\phi B} + Wh_{\phi C}$, or the sum of the absolute value of these energies, $Wh = |Wh_{\phi A}| + |Wh_{\phi B}| + |Wh_{\phi C}|$. The selection between the two modes can be made by setting Bit 2 of the gain register (Address 18h). See Table X. Logic high and logic low of this bit correspond to the sum of absolute values and the arithmetic sum, respectively. This selection affects the active energy accumulation in the AENERGY, RAENERGY, and LAENERGY registers as well as the CF frequency output.

When the sum of the absolute values is selected, the active energy from each phase is always counted positive in the total active energy. It is particularly useful in a 3-phase, 4-wire installation where the sign of the active power should always be the same. If the meter is misconnected to the power lines (e.g., CT is connected in the wrong direction), the total active energy recorded without this solution can be reduced by two thirds. The sum of the absolute values ensures that the active energy recorded represents the actual active energy delivered. In this mode, the reverse power information available in the CFNUM register is still detecting when negative active power is present on any of the three phase inputs.

LINE ENERGY ACCUMULATION

The ADE7754 is designed with a special energy accumulation mode that simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7754 accumulates the active power signal in the LAENERGY register for an integer number of half cycles, as shown in Figure 31. The line active energy accumulation mode is always active.

Using this mode with only one phase selected is recommended. If several phases are selected, the amount accumulated may be smaller than it should be.

Each one of three phases zero-crossing detection can contribute to the accumulation of the half line cycles. Phase A, B, and C zero crossings, respectively, are taken into account when counting the number of half line cycles by setting Bits 4 to 6 of the MMODE register to Logic 1. Selecting phases for the zero-crossing counting also has the effect of enabling the zero-crossing detection, zero-crossing timeout and period measurement for the corresponding phase as described in the zero-crossing detection paragraph.

The number of half line cycles is specified in the LINCYC register. LINCYC is an unsigned 16-bit register. The ADE7754 can accumulate active power for up to 65535 combined half cycles. Because the active power is integrated on an integer number of line cycles, the sinusoidal component is reduced to zero. This eliminates any ripple in the energy calculation. Energy is calculated more accurately because of this precise timing control. At the end of an energy calibration cycle, the LINCYC flag in the interrupt status register is set. If the LINCYC enable bit in the interrupt enable register is set to Logic 1, the $\overline{IRQ}$ output also goes active low.

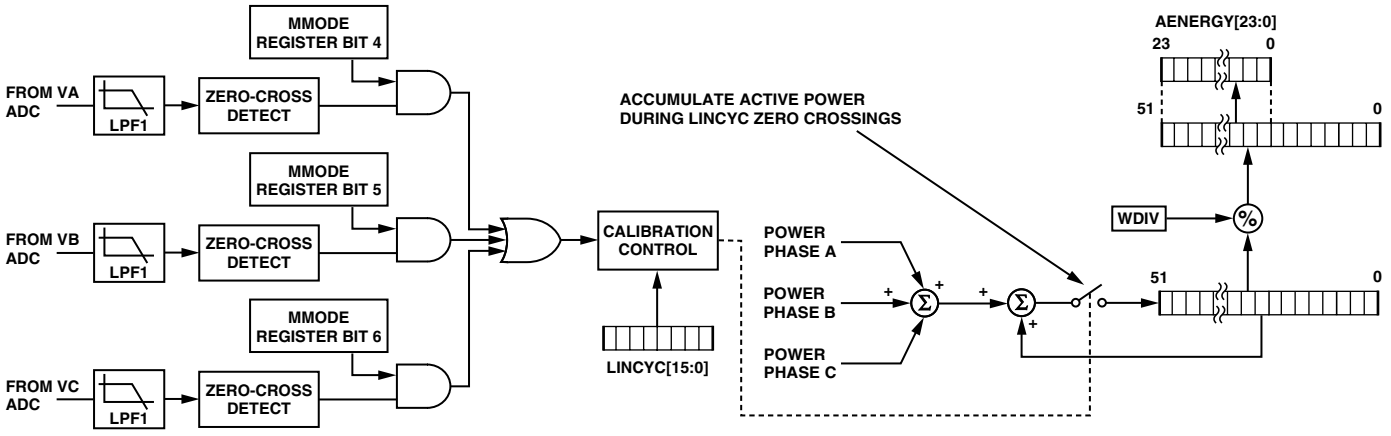


Figure 31. Active Energy Calibration

Thus the $\overline{IRQ}$ line can also be used to signal the end of a calibration. Equation 14 is derived from Equations 8 and 12.

$$E(t) = \int_0^{nT} VI\,dt - \left\{ \frac{VI}{\sqrt{1+\left(\frac{f}{8}\right)^2}} \right\} \times \int_0^{nT} \cos(2\pi\, f\, t)dt \quad (14)$$

where n is an integer and T is the line cycle period. Since the sinusoidal component is integrated over an integer number of line cycles, its value is always zero.

Therefore,

$$E(t) = \int_0^{nT} VI\,dt + 0 \quad (15)$$

$$E(t) = VInT \quad (16)$$

The total active power calculated by the ADE7754 in the line accumulation mode depends on the configuration of the WATMOD bits in the WATMode register. Each term of the formula can be disabled or enabled by the LWATSEL bits of the WATMode register. The different configurations are described in Table III.

Table III. Total Line Active Energy Calculation

WATMOD	LWATSEL0	LWATSEL1	LWATSEL2
0	$V_A \times I_A$*	+ $V_B \times I_B$*	+ $V_C \times I_C$*
1	$V_A \times (I_A$*– I_B*)	+ 0	+ $V_C \times (I_C$*– I_B*)
2	$V_A \times (I_A$*– I_B*)	+ 0	+ $V_C \times I_C$*

Note that I_A*, I_B*, and I_C* represent the current channels samples after APGAIN correction and high-pass filtering.

The line active energy accumulation uses the same signal path as the active energy accumulation; however, the LSB size of the two registers is different. If the line active energy register and active energy register are accumulated at the same time, the line active energy register will be four times bigger than the active energy register.

The LAENERGY register is also used to accumulate the reactive energy by setting to Logic 1 Bit 5 of the WAVMode register (Address 0Ch). See the Reactive Power Calculation section. When this bit is set to 1, the accumulation of the active energy over half line cycles in the LAENERGY register is disabled and is done instead in the LVAENERGY register. Because the LVAENERGY register is an unsigned value, the accumulation of the active energy in the LVAENERGY register is unsigned in this mode. The reactive energy is then accumulated in the LAENERGY register. See Figure 33. In this mode (reactive energy), selecting the phases accumulated in the LAENERGY and LVAENERGY registers is done by the LWATSEL selection bits of the WATTMode register.

In normal mode, Bit 5 of the WAVMODE register equals 0, and the type of active power summation in the LAENERGY register (sum of absolute active power or arithmetic sum) is selected by Bit 2 of the gain register.

In the mode where the active powers are accumulated in the LVAENERGY register, and Bit 5 of the WAVMODE register equals 1, note that the sum of several active powers is always done ignoring the sign of the active powers. This is due to the unsigned nature of the LVAENERGY register which does not allow signed addition.

REACTIVE POWER CALCULATION

Reactive power is defined as the product of the voltage and current waveforms when one of this signals is phase shifted by 90° at each frequency. It is defined mathematically in the IEEE Standards Dictionary 100 as

$$Reactive\ Power = \sum_{n=1}^{\infty} V_n \times I_n \times sin(\varphi_n)$$

where V_n and I_n are the voltage and current rms values of the n^{th} harmonics of the line frequency, respectively, and φ_n is the phase difference between the voltage and current nth harmonics. The resulting waveform is called the instantaneous reactive power signal (VAR).

Equation 19 gives an expression for the instantaneous reactive power signal in an ac system without harmonics when the phase of the current channel is shifted by –90°.

$$v(t) = \sqrt{2}\,V_1 \sin(\omega t - \varphi_1) \quad (17)$$

$$i(t) = \sqrt{2}\,I_1 \sin(\omega t)\; i'(t) = \sqrt{2}\,I_1 \sin\left(\omega t - \frac{\Pi}{2}\right) \quad (18)$$

$$VAR(t) = v(t) \times i'(t)$$
$$VAR(t) = V_1 I_1 \sin(\varphi_1) + V_1 I_1 \sin(2\omega t + \varphi_1) \quad (19)$$

The average power over an integral number of line cycles (n) is given in Equation 20.

$$VAR = \frac{1}{nT} \int_0^{nT} VAR(t)dt = V_1 I_1 \sin(\varphi_1) \quad (20)$$

where T is the line cycle period.

VAR is referred to as the reactive power. Note that the reactive power is equal to the dc component of the instantaneous reactive power signal $VAR(t)$ in Equation 19. This is the relationship used to calculate reactive power in the ADE7754 for each phase. The instantaneous reactive power signal VAR(t) is generated by multiplying the current and voltage signals in each phase. In this case, the phase of the current channel is shifted by –89°. The dc component of the instantaneous reactive power signal in each phase (A, B, and C) is then extracted by a low-pass filter to obtain the reactive power information on each phase. In a polyphase system, the total reactive power is simply the sum of the reactive power in all active phases. The different solutions available to process the total reactive power from the individual calculation are discussed in the following section.

Figure 32 shows the signal processing in each phase for the reactive power calculation in the ADE7754.

Since the phase shift applied on the current channel is not –90° as it should be ideally, the reactive power calculation done in the ADE7754 cannot be used directly for the reactive power calculation. Consequently, using the ADE7754 reactive power measurement only to get the sign of the reactive power is recommended. The reactive power can be processed using the power triangle method.

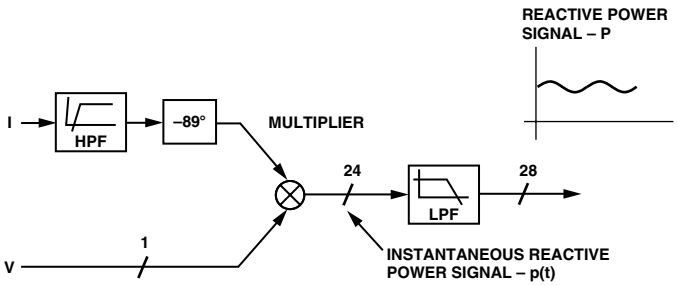


Figure 32. Reactive Power Signal Processing

TOTAL REACTIVE POWER CALCULATION

The sum of the reactive powers coming from each phase gives the total reactive power consumption. Different combinations of the three phases can be selected in the sum by setting Bits 7 to 6 of the WATMode register (mnemonic WATMOD[1:0]). Each term of the formula can be disabled or enabled by the LWATSEL bits of the WATMode register. Note that in this mode, the LWATSEL bits are also used to select the terms of the LVAENERGY register. The different configurations are described in Table III.

The accumulation of the reactive power in the LAENERGY register is different from the accumulation of the active power in the LAENERGY register. Under the same signal conditions (e.g., current and voltage channels at full scale), and if the accumulation of the active power with PF = 1 over one second is Wh_1, and the accumulation of the reactive power with PF = 0 during that time is $VARh_1$, then $Wh_1 = 9.546 \times VAR_1$.

Note that I_A*, I_B*, and I_C* represent the current channels samples after APGAIN correction, high-pass filtering, and –89° phase shift in the case of reactive energy accumulation.

Reactive Energy Accumulation Selection

The ADE7754 accumulates the total reactive power signal in the LAENERGY register for an integer number of half cycles, as shown in Figure 31. This mode is selected by setting Bit 5 of the WAVMode register (Address 0Ch) to Logic 1. When this bit is set, the accumulation of the active energy over half line cycles in the LAENERGY register is disabled and done instead in the LVAENERGY register. In this mode, the accumulation of the apparent energy over half line cycles in the LVAENERGY is no longer available. See Figure 33.

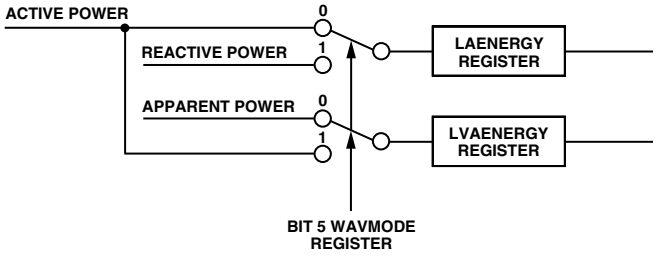


Figure 33. Selection of Reactive Energy Accumulation

The features of the reactive energy accumulation are the same as for the line active energy accumulation: each one of three phases zero-crossing detection can contribute to the accumulation of the half line cycles. Phase A, B, and C zero crossings, respectively, are taken into account when counting the number of half line cycles by setting to Logic 1 Bits 4 to 6 of the MMODE register. Selecting phases for the zero-crossing counting also has the effect of enabling the zero-crossing detection, zero-crossing timeout, and period measurement for the corresponding phase as described in the Zero-Crossing Detection section.

The number of half line cycles is specified in the LINCYC register. LINCYC is an unsigned 16-bit register. The ADE7754 can accumulate active power for up to 65535 combined half cycles. At the end of an energy calibration cycle, the LINCYC flag in the interrupt status register is set. If the LINCYC enable bit in the interrupt enable register is set to Logic 1, the $\overline{IRQ}$ output also goes active low. Thus the $\overline{IRQ}$ line can also be used to signal the end of a calibration.

As explained in the Reactive Power Calculation section, the purpose of the reactive energy calculation in the ADE7754 is not to give an accurate measurement of this value but to provide the sign of the reactive energy. The ADE7754 provides an accurate measurement of the apparent energy. Because the active energy is also measured in the ADE7754, a simple mathematical formula can be used to extract the reactive energy. The evaluation of the sign of the reactive energy makes up the calculation of the reactive energy.

$$Reactive\ Energy = sign(Reactive\ Power) \times \sqrt{Apparent\ Energy^2 - Active\ Energy^2}$$

APPARENT POWER CALCULATION

Apparent power is defined as the maximum active power that can be delivered to a load. $_{Vrm}$s and $_{Irm}$s are the effective voltage and current delivered to the load; the apparent power (AP) is defined as $V_{rms} \times I_{rms}$.

Note that the apparent power is equal to the multiplication of the rms values of the voltage and current inputs. For a polyphase system, the rms values of the current and voltage inputs of each phase (A, B, and C) are multiplied to obtain the apparent power information of each phase. The total apparent power is the sum of the apparent powers of all the phases. The different solutions available to process the total apparent power are discussed below.

Figure 34 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7754.

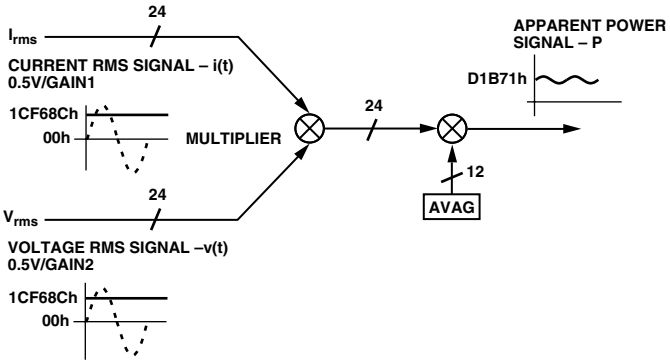


Figure 34. Apparent Power Signal Processing

The apparent power is calculated with the current and voltage rms values obtained in the rms blocks of the ADE7754. Figure 35 shows the maximum code (hexadecimal) output range of the apparent power signal for each phase. Note that the output range changes depending on the contents of the apparent power gain registers and also on the contents of the active power gain

and voltage gain registers. See the Current RMS Calculation and Voltage RMS Calculation sections. Only the effect of the apparent power gain is shown on Figure 35. The minimum output range is given when the apparent power gain register content is equal to 800h and the maximum range is given by writing 7FFh to the apparent power gain register. This can be used to calibrate the apparent power (or energy) calculation in the ADE7754 for each phase and the total apparent energy. See the Total Apparent Power Calculation section.

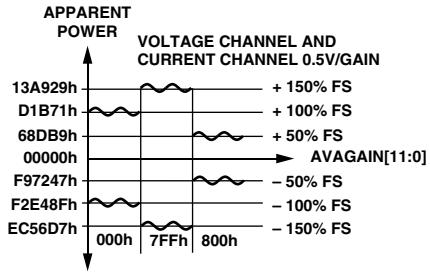


Figure 35. Apparent Power Calculation Output Range

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value. See the Current RMS Calculation and Voltage RMS Calculation sections. The voltage and current rms values are then multiplied in the apparent power signal processing. Because no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase is done by calibrating each individual rms measurement.

TOTAL APPARENT POWER CALCULATION

The sum of the apparent powers coming from each phase gives the total apparent power consumption. Different combinations of the three phases can be selected in the sum by setting Bits 7 and 6 of the VAMode register (mnemonic VAMOD[1:0]). Figure 36 demonstrates the calculation of the total apparent power.

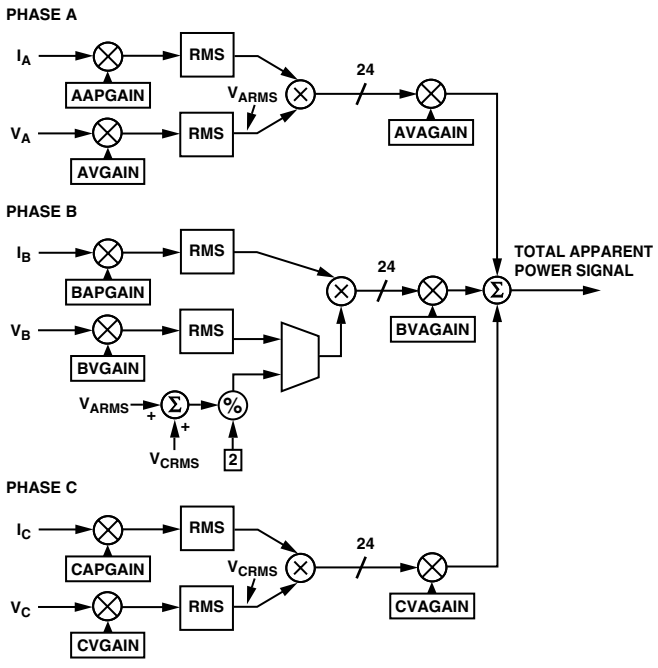


Figure 36. Total Apparent Power Calculation

The total apparent power calculated by the ADE7754 depends on the configuration of the VAMOD bits in the VAMode register. Each term of the formula used can be disabled or enabled by the setting VASEL bits, respectively, to Logic 0 or Logic 1 in the VAMode register. The different configurations are described in Table IV.

Table IV. Total Apparent Power Calculation

VAMOD	VASEL0	VASEL1	VASEL2
0d	$V_{ARMS} \times I_{ARMS}$	$+ V_{BRMS} \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$
1d	$V_{ARMS} \times I_{ARMS}$	$+(V_{ARMS} + V_{CRMS}) /2 \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$
2d	$V_{ARMS} \times I_{ARMS}$	$+ V_{ARMS} \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$

Note that V_{ARMS}, V_{BRMS}, V_{CRMS}, I_{ARMS}, I_{BRMS}, and I_{CRMS} represent the voltage and current channels RMS values of the corresponding registers.

For example, for VAMOD = 1, the formula used to process the apparent power is

$$Total\ Apparent\ Power = V_{ARMS} \times I_{ARMS} \times \left(1 + \frac{AVAG}{2^{12}}\right) + \frac{(V_{ARMS} + V_{CRMS})}{2} \times I_{BRMS} \times \left(1 + \frac{BVAG}{2^{12}}\right) + V_{CRMS} \times I_{CRMS} \times \left(1 + \frac{CVAG}{2^{12}}\right)$$

The polyphase meter configuration determines which formula should be used to calculate the apparent energy. The American ANSI C12.10 standard defines the different configurations of the meter. Table V describes which mode should be chosen for different configurations.

Table V. Meter Form Configuration

ANSI	Meter Form	VAMOD	VASEL
5S/13S	3-wire Delta	0	3 or 5 or 6
6S/14S	4-wire Wye	1	7
8S/15S	4-wire Delta	2	7
9S/16S	4-wire Wye	0	7

Different gain calibration parameters are offered in the ADE7754 to cover the calibration of the meter in different configurations. The APGAIN, VGAIN, and VAGAIN registers have different purposes in the signal processing of the ADE7754. APGAIN registers affect the apparent power calculation but should be used only for active power calibration. VAGAIN registers are used to calibrate the apparent power calculation. VGAIN registers have the same effect as VAGAIN registers when VAMOD = 0 or 2. They should be left at their default value in these modes. VGAIN registers should be used to compensate gain mismatches between channels in VAMOD = 1.

As mentioned previously, the offset compensation of the phase apparent power calculation is done in each individual rms measurement signal processing. See the Apparent Power Offset Calibration section.

APPARENT ENERGY CALCULATION

The apparent energy is given as the integral of the apparent power.

$$Apparent\ Energy = \int Apparent\ Power(t)\,dt \quad (21)$$

The ADE7754 achieves the integration of the apparent power signal by continuously accumulating the apparent power signal in an internal nonreadable 49-bit register. The apparent energy register (VAENERGY[23:0]) represents the upper 24 bits of this internal register. This discrete time accumulation or summation is equivalent to integration in continuous time. Equation 22 expresses the relationship, where n is the discrete time sample number and T is the sample period.

$$Apparent\ Energy = \underset{T\to 0}{Lim}\left\{\sum_{n=0}^{\infty} Apparent\ Power(nT)\times T\right\} \quad (22)$$

The discrete time sample period (T) for the accumulation register in the ADE7754 is 1.2 µs (12/10 MHz).

Figure 37 shows a graphical representation of this discrete time integration or accumulation. The apparent power signal is continuously added to the internal register. This addition is a signed addition even if the apparent energy theoretically always remains positive.

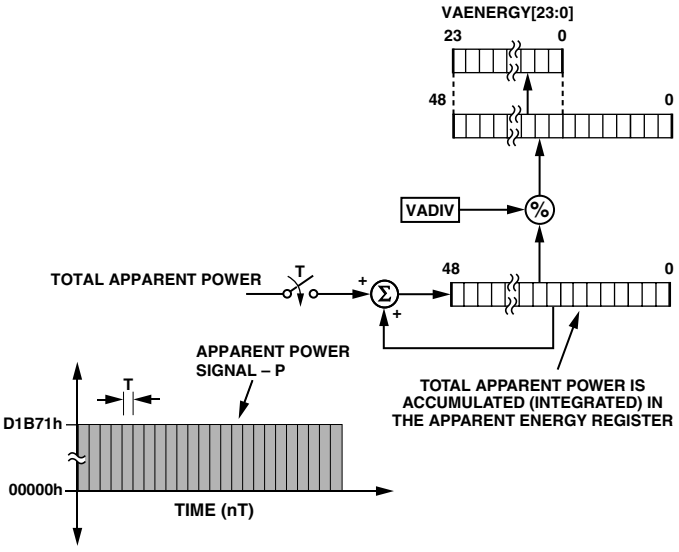


Figure 37. Apparent Energy Calculation

The upper 49-bit value of the internal register is divided by VADIV. If the value in the VADIV register is 0, then the internal active energy register is divided by 1. VADIV is an 8-bit unsigned register. The upper 24-bit values are then written in the 24-bit apparent energy register (VAENERGY[23:0]). RVAENERGY register (24 bits long) is provided to read the apparent energy. This register is reset to 0 after a read operation.

Figure 38 shows this apparent energy accumulation for full-scale (sinusoidal) signals on the analog inputs. The three curves illustrate the minimum time it takes the energy register to roll over when the individual VA gain registers contents all equal 3FFh, 000h, and 800h. The VA gain registers are used to carry out an apparent power calibration in the ADE7754. The fastest integration time occurs when the VA gain registers are set to maximum full scale (i.e., 3FFh).

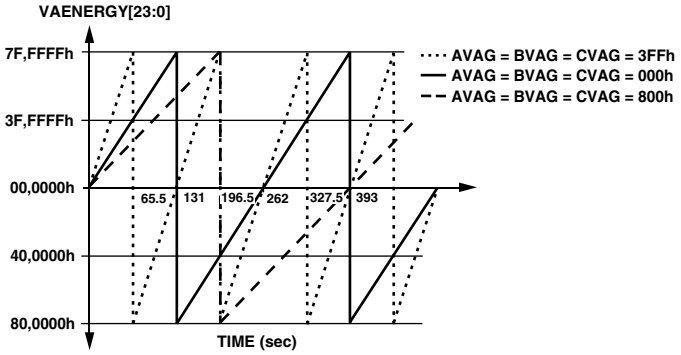


Figure 38. Energy Register Roll Over Time for Full-Scale Power (Minimum and Maximum Power Gain)

Note that the apparent energy register contents roll over to full-scale negative (80,0000h) and continue increasing in value when the power or energy flow is positive, as shown in Figure 38. By using the interrupt enable register, the ADE7754 can be configured to issue an interrupt ($\overline{IRQ}$) when the apparent energy register is half full (positive or negative).

Integration Times under Steady Load

As described in the preceding section, the discrete time sample period (T) for the accumulation register is 1.2 µs (12/CLKIN). With full-scale sinusoidal signals on the analog inputs and the VA gain registers set to 000h, the average word value from each apparent power stage is D1B71h. See the Apparent Power Calculation section. The maximum value that can be stored in the apparent energy register before it overflows is $22^3 - 1$ or FF,FFFFh. As the average word value is added to the internal register that can store $24^8 - 1$ or FFFF,FFFF,FFFFh before it overflows, the integration time under these conditions with VADIV = 0 is calculated as follows:

$$Time = \frac{FFFF,FFFF,FFFFh}{3\times D1B71h}\times 1.2\ \mu s = 131\ s = 2\ \min 11\ s$$

When VADIV is set to a value different from 0, the integration time varies as shown in Equation 23.

$$Time = Time_{WDIV=0}\times VADIV \quad (23)$$

LINE APPARENT ENERGY ACCUMULATION

The ADE7754 is designed with a special apparent energy accumulation mode that simplifies the calibration process. By using the on-chip zero-crossing detection, the ADE7754 accumulates the apparent power signal in the LVAENERGY register for an integral number of half cycles, as shown in Figure 39. The line apparent energy accumulation mode is always active.

Each of three zero-crossing detection phases can contribute to the accumulation of the half line cycles. Phase A, B, and C zero crossings are taken into account when counting the number of half line cycles by setting Bits 4 to 6 of the MMODE register to Logic 1. Selecting phases for the zero-crossing counting also has the effect of enabling the zero-crossing detection, zero-crossing timeout, and period measurement for the corresponding phase as described in the zero-crossing detection paragraph.

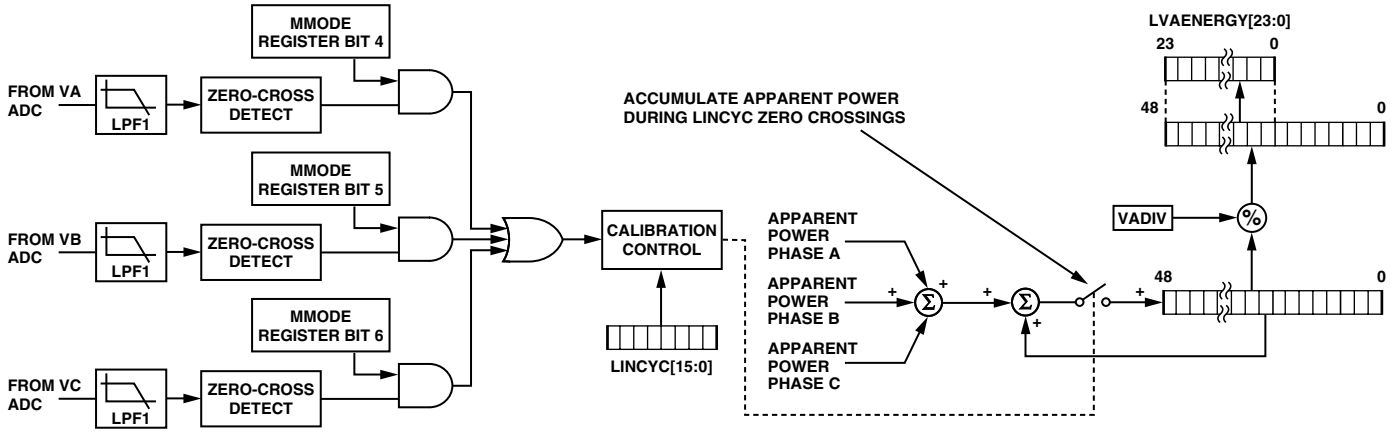


Figure 39. Apparent Energy Calibration

The number of half line cycles is specified in the LINCYC unsigned 16-bit register. The ADE7754 can accumulate apparent power for up to 65535 combined half cycles. Because the apparent power is integrated on the same integral number of line cycles as the line active energy register, these two values can be compared easily. See the Energies Scaling section. The active and apparent energy are calculated more accurately because of this precise timing control and provide all the information needed for reactive power and power factor calculation. At the end of an energy calibration cycle, the LINCYC flag in the interrupt status register is set. If the LINCYC enable bit in the interrupt enable register is set to Logic 1, the $\overline{\text{IRQ}}$ output also goes active low. Thus the $\overline{\text{IRQ}}$ line can also be used to signal the end of a calibration.

The total apparent power calculated by the ADE7754 in the line accumulation mode depends on the configuration of the VAMOD bits in the VAMode register. Each term of the formula used can be disabled or enabled by the LVASEL bits of the VAMode register. The different configurations are described in Table VI.

Table VI. Total Line Apparent Energy Calculation

VAMOD	VASEL0	VASEL1	VASEL2
0d	$V_{ARMS} \times I_{ARMS}$	$+ V_{BRMS} \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$
1d	$V_{ARMS} \times I_{ARMS}$	$+(V_{ARMS} + V_{CRMS}) /2 \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$
2d	$V_{ARMS} \times I_{ARMS}$	$+ V_{ARMS} \times I_{BRMS}$	$+ V_{CRMS} \times I_{CRMS}$

The line apparent energy accumulation uses the same signal path as the apparent energy accumulation. The LSB size of these two registers is equivalent.

The ADE7754 accumulates the total reactive power signal in the LAENERGY register. This mode is selected by setting to Logic 1 Bit 5 of the WAVMode register (Address 0Ch). When this bit is set, the accumulation of the active energy over half line cycles in the LAENERGY register is disabled and done instead in the LVAENERGY register. In this mode, the accumulation of the apparent energy over half line cycles in the LVAENERGY is no longer available. See Figure 33. Since the LVAENERGY register is an unsigned value, the accumulation of the active energy in the LVAENERGY register is unsigned. In this mode (reactive energy), the selection of the phases accumulated in the LAENERGY and LVAENERGY registers is done by the LWATSEL selection bits of the WATMode register.

ENERGIES SCALING

The ADE7754 provides measurements of the active, reactive, and apparent energies. These measurements do not have the same scaling and thus cannot be compared directly to each other.

Energy Type	PF = 1	PF = 0.707	PF = 0
Active	Wh	Wh × 0.707	0
Reactive	0	Wh × 0.707 / 9.546	Wh / 9.546
Apparent	Wh / 3.657	Wh / 3.657	Wh / 3.657

CHECK SUM REGISTER

The ADE7754 has a checksum register (CHECKSUM[5:0]) to ensure that the data bits received in the last serial read operation are not corrupted. The 6-bit checksum register is reset before the first bit (MSB of the register to be read) is put on the DOUT pin. During a serial read operation, when each data bit becomes available on the rising edge of SCLK, the bit is added to the checksum register. In the end of the serial read operation, the content of the checksum register will equal the sum of all ones in the register previously read. Using the checksum register, the user can determine whether an error has occurred during the last read operation. Note that a read to the checksum register also generates a checksum of the checksum register itself.

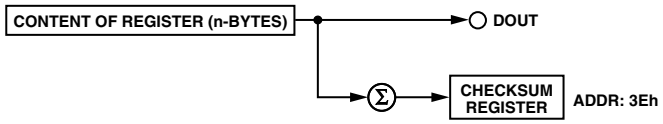


Figure 40. Checksum Register for Serial Interface Read

SERIAL INTERFACE

ADE7754 has a built-in SPI interface. The serial interface of the ADE7754 is made of four signals: SCLK, DIN, DOUT, and $\overline{CS}$. The serial clock for a data transfer is applied at the SCLK logic input, which has a Schmidt-trigger input structure that allows slow rising (and falling) clock edges to be used. All data transfer operations are synchronized to the serial clock. Data is shifted into the ADE7754 at the DIN logic input on the falling edge of SCLK. Data is shifted out of the ADE7754 at the DOUT logic output on a rising edge of SCLK. The $\overline{CS}$ logic input is the chip-select input. This input is used when multiple devices share the serial bus. A falling edge on $\overline{CS}$ also resets the serial interface and places the ADE7754 into communications mode. The $\overline{CS}$ input should be driven low for the entire data transfer operation. Bringing $\overline{CS}$ high during a data transfer operation will abort the transfer and place the serial bus in a high impedance state. The $\overline{CS}$ logic input may be tied low if the ADE7754 is the only device on the serial bus. However, with $\overline{CS}$ tied low, all initiated data transfer operations must be fully completed (i.e., the LSB of each register must be transferred because there is no other way to bring the ADE7754 back into communications mode without resetting the entire device, i.e., setting the $\overline{RESET}$ pin logic low).

All the ADE7754 functionality is accessible via several on-chip registers. See Figure 41. The contents of these registers can be updated or read using the on-chip serial interface. After power-on or toggling the $\overline{RESET}$ pin low, or a falling edge on $\overline{CS}$, the ADE7754 is placed into communications mode. In communications mode, the ADE7754 expects the first communication to be a write to the internal communications register. The data written to the communications register contains the address and specifies the next data transfer to be a read or a write command. Therefore all data transfer operations with the ADE7754, whether read or write types, must begin with a write to the communications register.

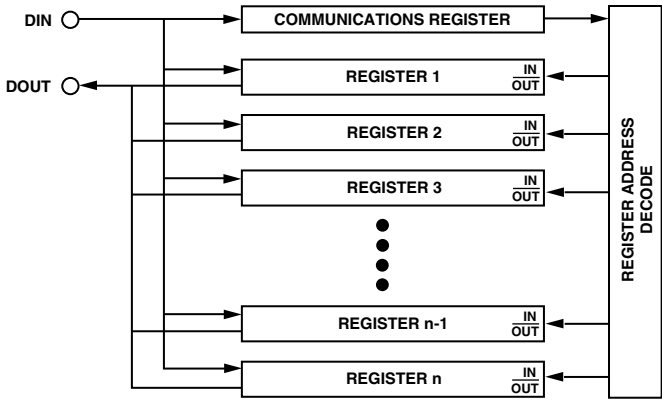


Figure 41. Addressing ADE7754 Registers via the Communications Register

The communications register is an 8-bit write-only register. The MSB determines whether the next data transfer operation is a read or a write. The six LSBs contain the address of the register to be accessed. See the Communications Register section for a more detailed description.

Figure 42 and Figure 43 show the data transfer sequences for a read and write operation, respectively. On completion of a data transfer (read or write), the ADE7754 once again enters communications mode (i.e., the next instruction followed must be a write to the communications register).

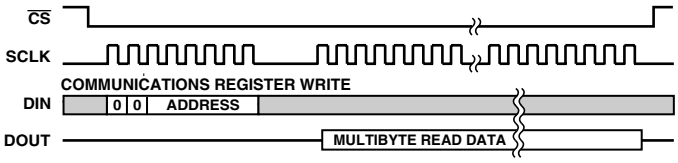


Figure 42. Reading Data from the ADE7754 via the Serial Interface

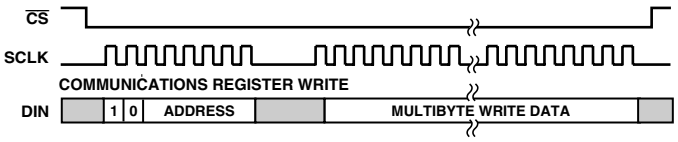


Figure 43. Writing Data to the ADE7754 via the Serial Interface

A data transfer is completed when the LSB of the ADE7754 register being addressed (for a write or a read) is transferred to or from the ADE7754.

Serial Write Operation

The serial write sequence requires the following steps. With the ADE7754 in communications mode and the $\overline{CS}$ input logic low, a write to the communications register takes place. The MSB of this byte transfer must be set to 1, indicating that the next data transfer operation is a write to the register. The six LSBs of this byte contain the address of the register to be written to. The ADE7754 starts shifting in the register data on the next falling edge of SCLK. All remaining bits of register data are shifted in on the falling edge of subsequent SCLK pulses. See Figure 44.

As explained previously, the data write is initiated by a write to the communications register, followed by the data. During a data write operation to the ADE7754, data is transferred to all on-chip registers one byte at a time. After a byte is transferred into the serial port, there is a finite amount of time before the content of the serial port buffer is transferred to one of the ADE7754 on-chip registers. Although another byte transfer to the serial port can start while the previous byte is being transferred to the destination register, this second byte transfer should not finish until at least 1 μs after the end of the previous byte transfer. This functionality is expressed in the timing specification t_6. See Figure 44. If a write operation is aborted during a byte transfer ($\overline{CS}$ brought high), then that byte will not be written to the destination register.

Destination registers may be up to 3 bytes wide. See the Register Descriptions section. Therefore, the first byte shifted into the serial port at DIN is transferred to the MSB (most significant byte) of the destination register. If the destination register is 12 bits wide, for example, a 2-byte data transfer must take place. The data is always assumed to be right justified; therefore, in this case, the four MSBs of the first byte would be ignored and the four LSBs of the first byte written to the ADE7754 would be the four MSBs of the 12-bit word. Figure 45 illustrates this example.

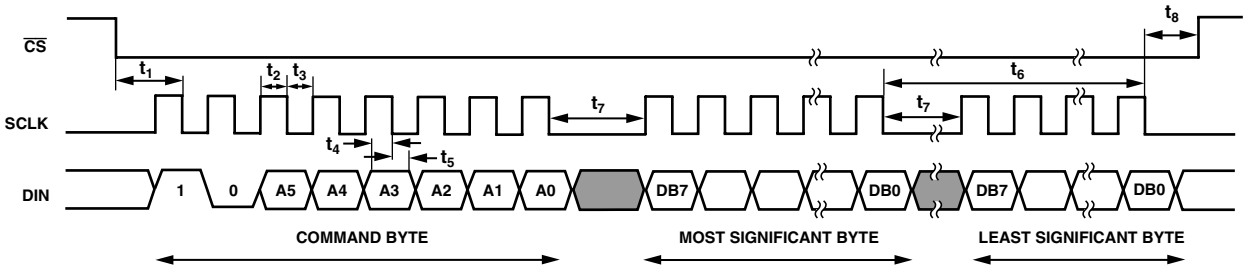


Figure 44. Serial Interface Write Timing Diagram

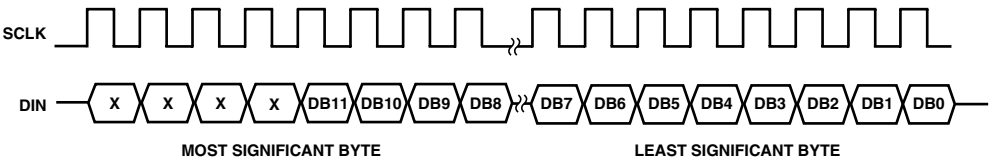


Figure 45. 12-Bit Serial Write Operation

Serial Read Operation

During a data read operation from the ADE7754, data is shifted out at the DOUT logic output on the rising edge of SCLK. As was the case with the data write operation, a data read must be preceded by a write to the communications register.

With the ADE7754 in communications mode and $\overline{CS}$ logic low, an 8-bit write to the communications register first takes place. The MSB of this byte transfer must be a 0, indicating that the next data transfer operation is a read. The six LSBs of this byte contain the address of the register to be read. The ADE7754 starts shifting out of the register data on the next rising edge of SCLK. See Figure 46. At this point, the DOUT logic output switches from high impedance state and starts driving the data bus. All remaining bits of register data are shifted out on subsequent SCLK rising edges. The serial interface enters communications mode again as soon as the read has been completed. The DOUT logic output enters a high impedance state on the falling edge of the last SCLK pulse. The read operation may be aborted by bringing the $\overline{CS}$ logic input high before the data transfer is completed. The DOUT output enters a high impedance state on the rising edge of $\overline{CS}$.

When an ADE7754 register is addressed for a read operation, the entire contents of that register are transferred to the serial port. This allows the ADE7754 to modify its on-chip registers without the risk of corrupting data during a multibyte transfer.

Note that when a read operation follows a write operation, the read command (i.e., write to communications register) should not happen for at least 1 µs after the end of the write operation. If the read command is sent within 1 µs of the write operation, the last byte of the write operation may be lost.

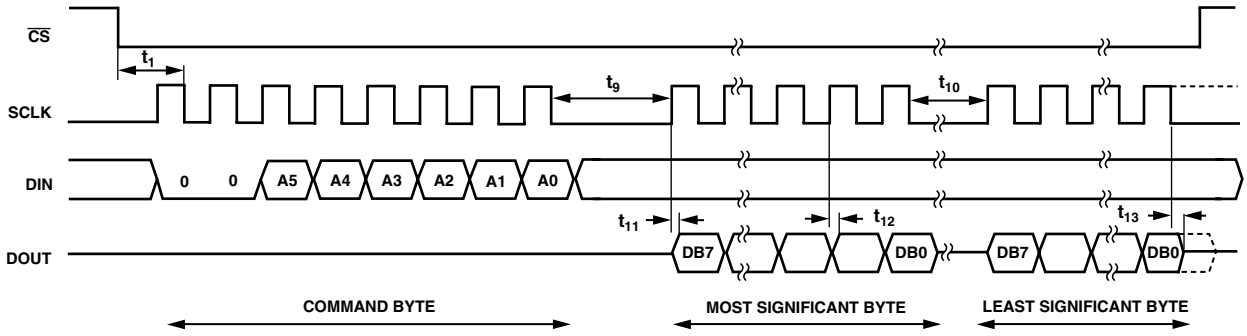


Figure 46. Serial Interface Read Timing Diagram

INTERRUPTS

ADE7754 interrupts are managed through the interrupt status register (STATUS[15:0], Address 10h) and the interrupt enable register (IRQEN[15:0], Address 0Fh). When an interrupt event occurs in the ADE7754, the corresponding flag in the interrupt status register is set to Logic 1. See the Interrupt Status Register section. If the enable bit for this interrupt in the interrupt enable register is Logic 1, then the $\overline{IRQ}$ logic output goes active low. The flag bits in the interrupt status register are set irrespective of the state of the enable bits. In order to determine the source of the interrupt, the system master (MCU) should perform a read from the reset interrupt status register with reset. This is achieved by carrying out a read from Address 11h. The $\overline{IRQ}$ output goes logic high on completion of the interrupt status register read command. See the Interrupt Timing section. When carrying out a read with reset, the ADE7754 is designed to ensure that no interrupt events are missed. If an interrupt event occurs just as the interrupt status register is being read, the event will not be lost and the $\overline{IRQ}$ logic output is guaranteed to go high for the duration of the interrupt status register data transfer before going logic low again to indicate the pending interrupt.

Using Interrupts with an MCU

The timing diagram in Figure 47 illustrates a suggested implementation of ADE7754 interrupt management using an MCU. At time t_1, the $\overline{IRQ}$ line goes active low indicating that one or more interrupt events have occurred. The $\overline{IRQ}$ logic output should be tied to a negative edge triggered external interrupt on the MCU. On detection of the negative edge, the MCU should be configured to start executing its interrupt service routine (ISR). On entering the ISR, all interrupts should be disabled using the global interrupt enable bit. At this point the MCU external interrupt flag can be cleared in order to capture interrupt events that occur during the current ISR. When the MCU interrupt flag is cleared, a read from the reset interrupt status register with reset is carried out. This causes the $\overline{IRQ}$ line to be reset logic high *(t_2)*. See the Interrupt Timing section. The reset interrupt status register contents are used to determine the source of the interrupt(s) and therefore the appropriate action to be taken. If a subsequent interrupt event occurs during the ISR *(t_3)*, that event will be recorded by the MCU external interrupt flag being set again. On returning from the ISR, the global interrupt enable bit will be cleared (same instruction cycle) and the external interrupt flag will cause the MCU to jump to its ISR once again. This will ensure that the MCU does not miss any external interrupts.

Interrupt Timing

The Serial Interface section should be reviewed first before reviewing interrupt timing. As previously described, when the $\overline{IRQ}$ output goes low, the MCU ISR must read the interrupt status register in order to determine the source of the interrupt. When reading the interrupt status register contents, the $\overline{IRQ}$ output is set high on the last falling edge of SCLK of the first byte transfer (read interrupt status register command). The $\overline{IRQ}$ output is held high until the last bit of the next 8-bit transfer is shifted out (interrupt status register contents). See Figure 48. If an interrupt is pending at this time, the $\overline{IRQ}$ output will go low again. If no interrupt is pending, the $\overline{IRQ}$ output will remain high.

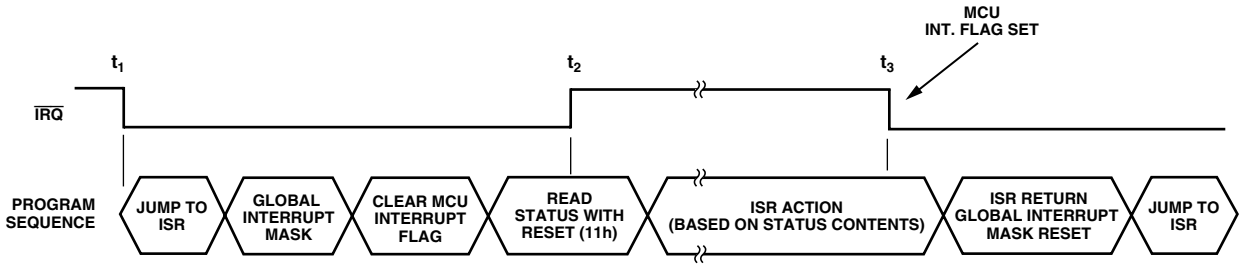


Figure 47. Interrupt Management

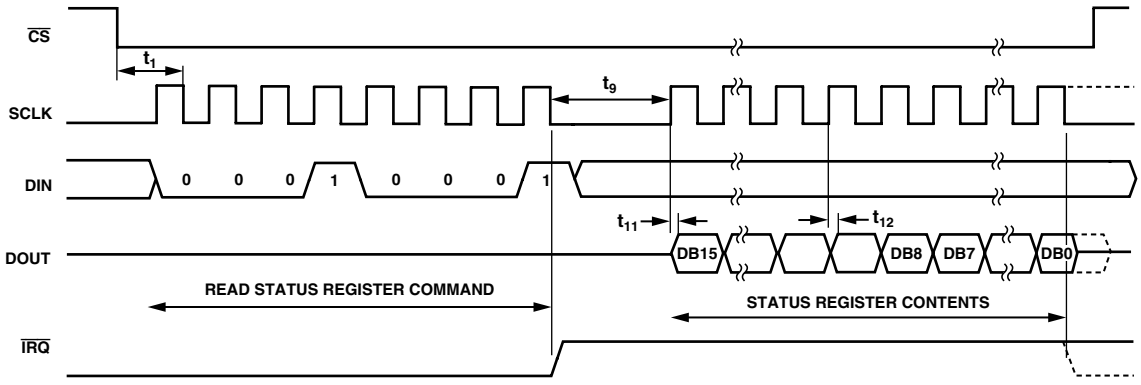


Figure 48. Interrupt Timing

ACCESSING THE ADE7754 ON-CHIP REGISTERS

All ADE7754 functionality is accessed via the on-chip registers. Each register is accessed by first writing to the communications register, then transferring the register data. For a full description of the serial interface protocol, see the Serial Interface section.

Communications Register

The communications register is an 8-bit, write-only register that controls the serial data transfer between the ADE7754 and the host processor. All data transfer operations must begin with a write to the communications register. The data written to the communications register determines whether the next operation is a read or a write and which register is being accessed. Table VII outlines the bit designations for the communications register.

Table VII. Communications Register

Bit Location	Bit Mnemonic	Description
0 to 5	A0 to A5	The six LSBs of the communications register specify the register for the data transfer operation. Table VIII lists the address of each ADE7754 on-chip register.
6	RESERVED	This bit is unused and should be set to 0.
7	W/$\overline{R}$	When this bit is a Logic 1, the data transfer operation immediately following the write to the communications register will be interpreted as a write to the ADE7754. When this bit is a Logic 0, the data transfer operation immediately following the write to the communications register will be interpreted as a read operation.

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W/$\overline{R}$	0	A5	A4	A3	A2	A1	A0

Table VIII. Register List

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
00h	Reserved				Reserved.
01h	AENERGY	R	24	0	Active Energy Register. Active power is accumulated over time in an internal register. The AENERGY register is a read-only register that reads this internal register and can hold a minimum of 88 seconds of active energy information with full-scale analog inputs before it overflows. See the Energy Calculation section. Bits 7 to 3 of the WATMODE register determine how the active energy is processed from the six analog inputs. See Table XIV.
02h	RAENERGY	R	24	0	Same as the AENERGY register, except that the internal register is reset to 0 following a read operation.
03h	LAENERGY	R	24	0	Line Accumulation Active Energy Register. The instantaneous active power is accumulated in this read-only register over the LINCYC number of half line cycles. Bits 2 to 0 of the WATMODE register determine how the line accumulation active energy is processed from the six analog inputs. See Table XIV.
04h	VAENERGY	R	24	0	VA Energy Register. Apparent power is accumulated over time in this read-only register. Bits 7 to 3 of the VAMODE register determine how the apparent energy is processed from the six analog inputs. See Table XV.
05h	RVAENERGY	R	24	0	Same as the VAENERGY register except that the register is reset to 0 following a read operation.
06h	LVAENERGY	R	24	0	Apparent Energy Register. The instantaneous apparent power is accumulated in this read-only register over the LINCYC number of half line cycles. Bits 2 to 0 of the VAMODE register determine how the apparent energy is processed from the six analog inputs. See Table XV.
07h	PERIOD	R	15	0	Period of the line input estimated by zero-crossing processing. Data Bit 0 and 1 and 4 to 6 of the MMODE register determine the voltage channel used for period calculation. See Table XII.
08h	TEMP	R	8	0	Temperature Register. This register contains the result of the latest temperature conversion. Refer to the Temperature Measurement section for details on how to interpret the content of this register.
09h	WFORM	R	24	0	Waveform Register. This register contains the digitized waveform of one of the six analog inputs. The source is selected by Data Bits 0 to 2 in the WAVMode register. See Table XIII.
0Ah	OPMODE	R/W	8	4	Operational Mode Register. This register defines the general configuration of the ADE7754. See Table IX.
0Bh	MMODE	R/W	8	70h	Measurement Mode Register. This register defines the channel used for period and peak detection measurements. See Table XII.
0Ch	WAVMODE	R/W	8	0	Waveform mode register. This register defines the channel and sampling frequency used in waveform sampling mode. See Table XIII.
0Dh	WATMODE	R/W	8	3Fh	This register configures the formula applied for the active energy and line active energy measurements. See Table XIV.
0Eh	VAMODE	R/W	8	3Fh	This register configures the formula applied for the apparent energy and line apparent energy measurements. See Table XV.
0Fh	IRQEN	R/W	16	0	IRQ Enable Register. It determines whether an interrupt event will generate an active low output at IRQ pin. See Table XVI.
10h	STATUS	R	16	0	IRQ Status Register. This register contains information regarding the source of ADE7754 interrupts. See Table XVII.
11h	RSTATUS	R	16	0	Same as the status register, except that its contents are reset to 0 (all flags cleared) after a read operation.
12h	ZXTOUT	R/W	16	FFFFh	Zero Cross Timeout Register. If no zero crossing is detected within a time period specified by this register, the interrupt request line (IRQ) will go active low for the corresponding line voltage. The maximum timeout period is 2.3 seconds. See the Zero-Crossing Detection section.

Table VIII. Register List (continued)

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
13h	LINCYC	R/W	16	FFFFh	Line Cycle Register. The content of this register sets the number of half line cycles while the active energy and the apparent energy are accumulated in the LAENERGY and LVAENERGY registers. See the Energy Calculation section.
14h	SAGCYC	R/W	8	FFh	SAG Line Cycle Register. This register specifies the number of consecutive half line cycles where voltage channel input falls below a threshold level. This register is common to the three-line voltage SAG detection. The detection threshold is specified by SAGLVL register. See the Line Voltage SAG Detection section.
15h	SAGLVL	R/W	8	0	SAG Voltage Level. This register specifies the detection threshold for SAG event. This register is common to the three-line voltage SAG detection. See the description of SAGCYC register for details.
16h	VPEAK	R/W	8	FFh	Voltage Peak Level. This register sets the level of the voltage peak detection. If the selected voltage phase exceeds this level, the PKV flag in the status register is set. See Table XII.
17h	IPEAK	R/W	8	FFh	Current Peak Level. This register sets the level of the current peak detection. If the selected current phase exceeds this level, the PKI flag in the status register is set. See Table XII.
18h	GAIN	R/W	8	0	PGA Gain Register. This register is used to adjust the gain selection for the PGA in current and voltage channels. See the Analog Inputs section and Table X. This register is also used to configure the active energy accumulation no-load threshold and sum of absolute values.
19h	AWG	R/W	12	0	Phase A Active Power Gain Register. The active power caluation for Phase A can be calibrated by writing to this register. The calibration range is 50% of the nominal full-scale active power. The resolution of the gain adjust is 0.0244%/LSB.
1Ah	BWG	R/W	12	0	Phase B Active Power Gain.
1Bh	CWG	R/W	12	0	Phase C Active Power Gain.
1Ch	AVAG	R/W	12	0	VA Gain Register. This register calculation can be calibrated by writing this register. The calibration range is 50% of the nominal full-scale real power. The resolution of the gain adjust is 0.02444%/LSB.
1Dh	BVAG	R/W	12	0	Phase B VA Gain.
1Eh	CVAG	R/W	12	0	Phase C VA Gain.
1Fh	APHCAL	R/W	5	0	Phase A Phase Calibration Register.
20h	BPHCAL	R/W	5	0	Phase B Phase Calibration Register.
21h	CPHCAL	R/W	5	0	Phase C Phase Calibration Register.
22h	AAPOS	R/W	12	0	Phase A Power Offset Calibration Register.
23h	BAPOS	R/W	12	0	Phase B Power Offset Calibration Register.
24h	CAPOS	R/W	12	0	Phase C Power Offset Calibration Register.
25h	CFNUM	R/W	12	0h	CF Scaling Numerator Register. The content of this register is used in the numerator of CF output scaling.
26h	CFDEN	R/W	12	3Fh	CF Scaling Denominator Register. The content of this register is used in the denominator of CF output scaling.
27h	WDIV	R/W	8	0	Active Energy Register Divider.
28h	VADIV	R/W	8	0	Apparent Energy Register Divider.
29h	AIrms	R	24	0	Phase A Current Channel RMS Register. The register contains the rms component of one input of the current channel. The source is selected by data bits in the mode register.
2Ah	BIrms	R	24	0	Phase B Current Channel RMS Register.
2Bh	CIrms	R	24	0	Phase C Current Channel RMS Register.
2Ch	AVrms	R	24	0	Phase A Voltage Channel RMS Register.
2Dh	BVrms	R	24	0	Phase B Voltage Channel RMS Register.
2Eh	CVrms	R	24	0	Phase C Voltage Channel RMS Register.
2Fh	AIrmsOS	R/W	12	0	Phase A Current RMS Offset Correction Register.
30h	BIrmsOS	R/W	12	0	Phase B Current RMS Offset Correction Register.

Table VIII. Register List (continued)

Address [A5:A0]	Name	R/W*	Length	Default Value	Description
31h	CIrmsOS	R/W	12	0	Phase C Current RMS Offset Correction Register.
32h	AVrmsOS	R/W	12	0	Phase A Voltage RMS Offset Correction Register.
33h	BVrmsOS	R/W	12	0	Phase B Voltage RMS Offset Correction Register.
34h	CVrmsOS	R/W	12	0	Phase C Voltage RMS Offset Correction Register.
35h	AAPGAIN	R/W	12	0	Phase A Active Power Gain Adjust. The active power accumulation of the Phase A can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale of the active power. The resolution of the gain is 0.0244%/LSB. See the Current Channel ADC Gain Adjust section.
36h	BAPGAIN	R/W	12	0	Phase B Active Power Gain Adjust.
37h	CAPGAIN	R/W	12	0	Phase C Active Power Gain Adjust.
38h	AVGAIN	R/W	12	0	Phase A Voltage RMS Gain. The apparent power accumulation of the Phase A can be calibrated by writing to this register. The calibration range is ±50% of the nominal full scale of the apparent power. The resolution of the gain is 0.0244% / LSB. See the Voltage RMS Gain Adjust section.
39h	BVGAIN	R/W	12	0	Phase B Voltage RMS Gain.
3Ah	CVGAIN	R/W	12	0	Phase C Voltage RMS Gain.
3Bh–3Dh					Reserved.
3Eh	CHKSUM	R	8		Check Sum Register. The content of this register represents the sum of all 1s of the latest register read from the SPI port.
3Fh	VERSION	R	8	1	Version of the Die.

*R/W: Read/Write capability of the register.
R: Read-only register.
R/W: Register that can be both read and written.

Operational Mode Register (0Ah)
The general configuration of the ADE7754 is defined by writing to the OPMODE register. Table IX summarizes the functionality of each bit in the OPMODE register.

Table IX. OPMODE Register

Bit Location	Bit Mnemonic	Default Value	Description
0	DISHPF	0	The HPFs (high-pass filters) in all current channel inputs are disabled when this bit is set.
1	DISLPF	0	The LPFs (low-pass filters) in all current channel inputs are disabled when this bit is set.
2	DISCF	1	The frequency output CF is disabled when this bit is set.
3-5	DISMOD	0	By setting these bits, ADE7754's A/D converters can be turned off. In normal operation, these bits should be left at Logic 0. DISMOD2 DISMOD1 DISMOD0 0 0 0 Normal operation. 1 0 0 Normal operation. By setting this bit to Logic 1, the analog inputs to current channel are connected to the ADC for voltage channel and the analog inputs to voltage channel are connected to the ADC for current channel. 0 0 1 Current channel A/D converters off. 1 0 1 Current channel A/D converters off + channels swapped. 0 1 0 Voltage Channel A/D converters off. 1 1 0 Voltage Channel A/D converters off + channels swapped. 0 1 1 ADE7754 in sleep mode. 1 1 1 ADE7754 powered down.
6	SWRST	0	Software Chip Reset. A data transfer to the ADE7754 should not take place for at least 18 µs after a software reset.
7	RESERVED		This is intended for factory testing only and should be left at 0.

Gain Register (18h)
The gain of the analog inputs and the mode of accumulation of the active energies in the ADE7754 are defined by writing to the gain register. Table X summarizes the functionality of each bit in the gain register.

Table X. GAIN Register

Bit Location	Bit Mnemonic	Default Value	Description
0-1	PGA1	0	These bits are used to select the gain of the current channels inputs. Bit 1 Bit 0 0 0 PGA1 = 1 0 1 PGA1 = 2 1 0 PGA1 = 4 0 0 Reserved
2	ABS	0	The sum of the absolute active energies is done in the ANERGY and LAENERGY registers when this bit is set to Logic 1. The regular sum is done when this bit is set to Logic 0—default mode.
3	$\overline{\text{NO LOAD}}$	0	The active energy of each phase is not accumulated in the total active energy registers if the instantaneous active power is lower than the no-load threshold when this bit is set to Logic 0; this mode is selected by default.
4	RESERVED		This is intended for factory testing only and should be left at 0.
5-6	PGA2	0	These bits are used to select the gain of the voltage channels inputs. Bit 6 Bit 5 0 0 PGA2 = 1 0 1 PGA2 = 2 1 0 PGA2 = 4 0 0 Reserved
7	RESERVED		This is intended for factory testing only and should be left at 0.

CFNUM Register (25h)
The CF scaling numerator and the sign of the active energy per phase are defined by writing/reading to the CFNUM register. Table XI summarizes the functionality of each bit in the CFNUM register.

Table XI. CFNUM Register

Bit Location	Bit Mnemonic	Default Value	Description
0-Bh	CFN	0	CF Scaling Numerator Register. The content of this register is used in the numerator of CF output scaling.
Ch	NEGA	0	The sign of the Phase A instantaneous active power is available in this bit. Logic 0 and Logic 1 correspond to positive and negative active power, respectively. The functionality of this bit is enabled by setting Bit 5 of the WATMode register to Logic 1. When disabled, NEGA is equal to its default value.
Dh	NEGB	0	The sign of the Phase B instantaneous active power is available in this bit. Logic 0 and Logic 1 correspond to positive and negative active power, respectively. The functionality of this bit is enabled by setting Bit 4 of the WATMode register to Logic 1. When disabled, NEGB is equal to its default value.
Eh	NEGC	0	The sign of the Phase C instantaneous active power is available in this bit. Logic 0 and Logic 1 correspond to positive and negative active power, respectively. The functionality of this bit is enabled by setting Bit 3 of the WATMode register to Logic 1. When disabled, NEGC is equal o its default value.
Fh	RESERVED		

Measurement Mode Register (0Bh)
The configuration of the period and peak measurements made by the ADE7754 are defined by writing to the MMODE register. Table XII summarizes the functionality of each bit in the MMODE register.

Table XII. MMODE Register

Bit Location	Bit Mnemonic	Default Value	Description
0-1	PERDSEL	0	These bits are used to select the source of the measurement of the voltage line period. Bit 1 Bit 0 Source 0 0 Phase A 0 1 Phase B 1 0 Phase C 1 1 Reserved
2-3	PEAKSEL	0	These bits select the line voltage and current phase used for the PEAK detection. If the selected line voltage is above the level defined in the PKVLVL register, the PKV flag in the interrupt status register is set. If the selected current input is above the level defined in the PKILVL register, the PKI flag in the interrupt status register is set. Bit 3 Bit 2 Source 0 0 Phase A 0 1 Phase B 1 0 Phase C 1 1 Reserved
4-6	ZXSEL	7	These bits select the phases used for counting the number of zero crossing in the line active and apparent accumulation modes as well as enabling these phases for the zero-crossing timeout detection, zero crossing, period measurement, and SAG detection. Bits 4, 5, and 6 select Phase A, Phase B, and Phase C, respectively.
7			Reserved.

Waveform Mode Register (0Ch)
The waveform sampling mode of the ADE7754 is defined by writing to the WAVMODE register. Table XIII summarizes the functionality of each bit in the WAVMODE register.

Table XIII. WAVMODE Register

Bit Location	Bit Mnemonic	Default Value	Description
0-2	WAVSEL	0	These bits are used to select the source of the waveform sample. Bit 2 Bit 1 Bit 0 Source 0 0 0 Voltage Phase A 0 0 1 Voltage Phase B 0 1 0 Voltage Phase C 0 1 1 Current Phase A 1 0 0 Current Phase B 1 0 1 Current Phase C 1 1 0 or 1 Reserved
3-4	DTRT	0	These bits are used to select the waveform sampling update rate. Bit 4 Bit 3 Update Rate 0 0 26.0 kSPS (CLKIN/3/128) 0 1 13.0 kSPS (CLKIN/3/256) 1 0 6.5 kSPS (CLKIN/3/512) 1 1 3.3 kSPS (CLKIN/3/1024)
5	LVARSEL	0	This bit is used to enable the accumulation of the line VAR energy into the LAENERGY register and of the line active energy into the LVAENERGY register.

Watt Mode Register (0Dh)
The phases involved in the active energy measurement of the ADE7754 are defined by writing to the WATMODE register. Table XIV summarizes the functionality of each bit in the WATMODE register.

Table XIV. WATMODE Register

Bit Location	Bit Mnemonic	Default Value	Description
0-2	LWATSEL	7	These bits are used to select each part of the formula separately, depending on the line active energy measurement method. The behavior of these bits is the same as WATSEL bits. Bit 2 selects the first term of the formula and so on.
3-5	WATSEL	7	These bits are used to select each part of the formula separately, depending on the active energy measurement method. These bits are also used to enable the negative power detection available in Bits 12 to 14 of CFNUM register. See Table XI. Setting Bit 5 to Logic 1 selects the first term of the formula (VA × IA or VA × (IA – IB)). Setting Bit 4 to Logic 1 selects the second term of the formula (VB × IB or 0 depending on WATMOD configuration). Setting Bit 3 to Logic 1 selects the last term of the formula (VC × IC or VC × (IC – IB)). Any combination of these bits can address calibration and operational needs.
6-7	WATM	0	These bits are used to select the formula used for active energy calculation.

WATM1	WAVM0	Active Energy Calculation
0	0	VA × IA + VB × IB + VC × IC
0	1	VA × (IA – IB) + 0 + VC × (IC – IB)
1	0	VA × (IA – IB) + 0 + VC × IC
1	1	Reserved.

VA Mode Register (0Eh)
The phases involved in the apparent energy measurement of the ADE7754 are defined by writing to the VAMODE register. Table XV summarizes the functionality of each bit in the VAMODE register.

Table XV. VAMODE Register

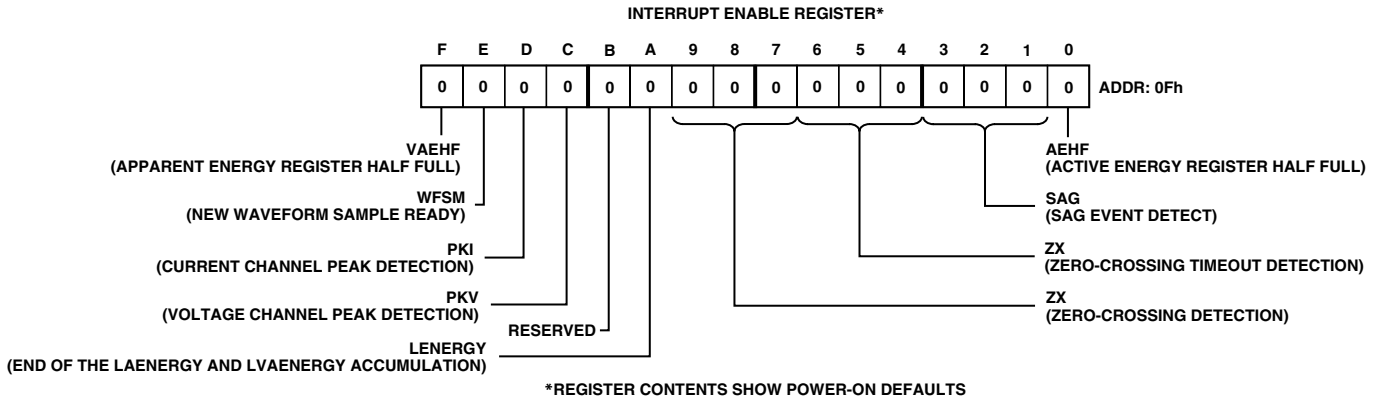
Bit Location	Bit Mnemonic	Default Value	Description
0-2	LVASEL	7	These bits are used to select each part of the formula separately, depending on the line apparent energy measurement method. The behavior of these bits is the same as VASEL bits. Bit 2 selects the first term of the formula, and so on.
3-5	VASEL	7	These bits are used to select separately each part of the formula, depending on the apparent energy measurement method. Setting Bit 5 to Logic 1 selects the first term of the formula ($VA_{rms} \times IA_{rms}$). Setting Bit 4 to Logic 1 selects the second term of the formula ($VB_{rms} \times IB_{rms}$ or $(VA_{rms}+VC_{rms})/2 \times IB_{rms}$ or $VA_{rms} \times IB_{rms}$ depending on VAMOD configuration). Setting Bit 3 to Logic 1 selects the first term of the formula ($VC_{rms} \times IC_{rms}$). Any combination of these bits can address calibration and operational needs.
6-7	VAMOD	0	These bits are used to select the formula used for active energy calculation.

VAMOD1	VAMOD0	Apparent Energy Calculation
0	0	$VA_{rms} \times IA_{rms} + VB_{rms} \times IB_{rms} + VC_{rms} \times IC_{rms}$
0	1	$VA_{rms} \times IA_{rms} + (VA_{rms} + VC_{rms})/2 \times IB_{rms} + VC_{rms} \times IC_{rms}$
1	0	$VA_{rms} \times IA_{rms} + VA_{rms} \times IB_{rms} + VC_{rms} \times IC_{rms}$
1	1	Reserved.

Interrupt Enable Register (0Fh)
When an interrupt event occurs in the ADE7754, the $\overline{\text{IRQ}}$ logic output goes active low if the enable bit for this event is Logic 1 in this register. The $\overline{\text{IRQ}}$ logic output is reset to its default collector open state when the RSTATUS register is read. Table XVI describes the function of each bit in the interrupt enable register.

Table XVI. IRQEN Register

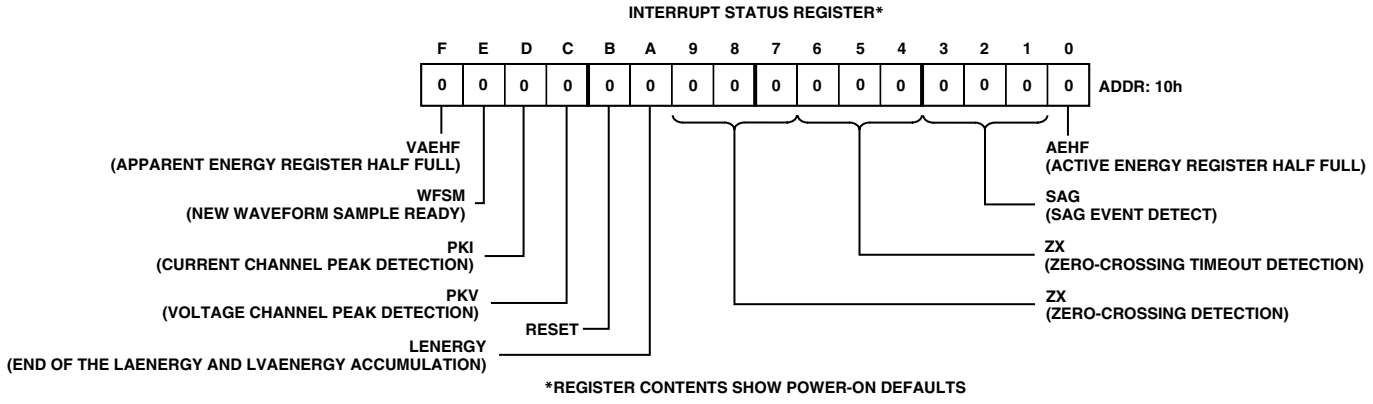
Bit Location	Interrupt Flag	Default Value	Description
0	AEHF	0	Enables an interrupt when there is a 0 to 1 transition of the MSB of the AENERGY register (i.e., the AENERGY register is half-full).
1	SAGA	0	Enables an interrupt when there is a SAG on the line voltage of the Phase A.
2	SAGB	0	Enables an interrupt when there is a SAG on the line voltage of the Phase B.
3	SAGC	0	Enables an interrupt when there is a SAG on the line voltage of the Phase C.
4	ZXTOA	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase A.
5	ZXTOB	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase B.
6	ZXTOC	0	Enables an interrupt when there is a zero-crossing timeout detection on Phase C.
7	ZXA	0	Enables an interrupt when there is a rising zero crossing in voltage channel of the Phase A—zero-crossing detection.
8	ZXB	0	Enables an interrupt when there is a rising zero crossing in voltage channel of the Phase B—zero-crossing detection.
9	ZXC	0	Enables an interrupt when there is a rising zero crossing in voltage channel of the Phase C—zero-crossing detection.
Ah	LENERGY	0	Enables an interrupt when the LAENERGY and LVAENERGY accumulations over LINCYC are finished.
Bh			Reserved.
Ch	PKV	0	Enables an interrupt when the voltage input selected in the MMODE register is above the value in the PKVLVL register.
Dh	PKI	0	Enables an interrupt when the current input selected in the MMODE register is above the value in the PKILVL register.
Eh	WFSM	0	Enables an interrupt when a data is present in the waveform register.
Fh	VAEHF	0	Enables an interrupt when there is a 0 to 1 transition of the MSB of the VAENERGY register (i.e., the VAENERGY register is half full).



Interrupt Status Register (10h)/Reset Interrupt Status Register (11h)
The interrupt status register is used to determine the source of an interrupt event. When an interrupt event occurs in the ADE7754, the corresponding flag in the interrupt status register is set logic high. The $\overline{IRQ}$ pin will go active low if the corresponding bit in the interrupt enable register is set logic high. When the MCU services the interrupt, it must first carry out a read from the interrupt status register to determine the source of the interrupt. All the interrupts in the interrupt status register stay at their logic high state after an event occurs. The state of the interrupt bit in the interrupt status register is reset to its default value once the reset interrupt status register is read.

Table XVII. STATUS Register

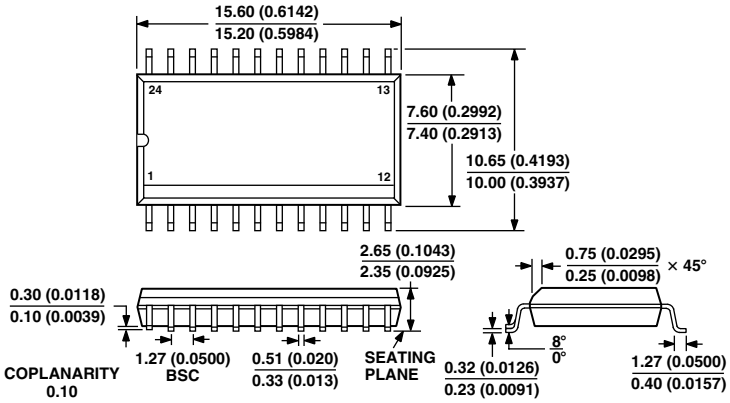
Bit Location	Interrupt Flag	Default Value	Event Description
0	AEHF	0	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the AENERGY register (i.e., the AENERGY register is half full).
1	SAGA	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase A.
2	SAGB	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase B.
3	SAGC	0	Indicates that an interrupt was caused by a SAG on the line voltage of the Phase C.
4	ZXTOA	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase A.
5	ZXTOB	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase B.
6	ZXTOC	0	Indicates that an interrupt was caused by a missing zero crossing on the line voltage of the Phase C.
7	ZXA	0	Indicates a detection of rising zero crossing in the voltage channel of the Phase A.
8	ZXB	0	Indicates a detection of rising zero crossing in the voltage channel of the Phase B.
9	ZXC	0	Indicates a detection of rising zero crossing in the voltage channel of the Phase C.
Ah	LENERGY	0	In line energy accumulation, it indicates the end of an integration over an integer number of half line cycles (LINCYC). See the Energy Calculation section.
Bh	RESET	0	Indicates that the ADE7754 has been reset.
Ch	PKV	0	Indicates that an interrupt was caused when the selected voltage input is above the value in the PKVLV register.
Dh	PKI	0	Indicates that an interrupt was caused when the selected current input is above the value in the PKILV register.
Eh	WFSM	0	Indicates that new data is present in the waveform register.
Fh	VAEHF	0	Indicates that an interrupt was caused by the 0 to 1 transition of the MSB of the VAENERGY register (i.e., the VAENERGY register is half full).



OUTLINE DIMENSIONS

24-Lead Standard Small Outline Package [SOIC]
Wide Body
(RW-24)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AD

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(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
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