THE DATASHEET OF

ADE7880ACPZ

www.win-source.net 0086-755-83957316

Polyphase Multifunction Energy Metering IC with Harmonic Monitoring

Data Sheet

ADE7880

FEATURES

- **Highly accurate; supports IEC 62053-21, IEC 62053-22, IEC 62053-23, EN 50470-1, EN 50470-3, ANSI C12.20, and IEEE1459 standards**
- **Supports IEC 61000-4-7 Class I and Class II accuracy specification**
- **Compatible with 3-phase, 3-wire or 4-wire (delta or wye), and other 3-phase services**
- **Supplies rms, active, reactive, and apparent powers, power factor, THD, and harmonic distortion of all harmonics within 2.8 kHz pass band on all phases**
- **Supplies rms and harmonic distortions of all harmonics within 2.8 kHz pass band on neutral current**
- **Less than 1% error in harmonic current and voltage rms, harmonic active and reactive powers over a dynamic range of 2000 to 1 at T_A = 25°C**
- **Supplies total (fundamental and harmonic) active and apparent energy and fundamental active/reactive energy on each phase and on the overall system**
- **Less than 0.1% error in active and fundamental reactive energy over a dynamic range of 1000 to 1 at T_A = 25°C**
- **Less than 0.2% error in active and fundamental reactive energy over a dynamic range of 5000 to 1 at T_A = 25°C**
- **Less than 0.1% error in voltage and current rms over a dynamic range of 1000 to 1 at T_A = 25°C**
- **Battery supply input for missing neutral operation**
- **Wide supply voltage operation: 2.4 V to 3.7 V**
- **Reference: 1.2 V (drift 20 ppm/°C typical) with external overdrive capability**
- **40-lead lead frame chip scale package (LFCSP), Pb-free, pin-for-pin compatible with ADE7854, ADE7858, ADE7868 and ADE7878**

APPLICATIONS

- **Energy metering systems**
- **Power quality monitoring**
- **Solar inverters**
- **Process monitoring**
- **Protective devices**

GENERAL DESCRIPTION

The ADE7880[1] is a high accuracy, 3-phase electrical energy measurement IC with serial interfaces and three flexible pulse outputs. The ADE7880 device incorporates second-order sigma-delta (Σ-Δ) analog-to-digital converters (ADCs), a digital integrator, reference circuitry, and all of the signal processing required to perform the total (fundamental and harmonic) active, and apparent energy measurements, rms calculations, as well as fundamental-only active and reactive energy measurements. In addition, the ADE7880 computes the rms of harmonics on the phase and neutral currents and on the phase voltages, together with the active, reactive and apparent powers, and the power factor and harmonic distortion on each harmonic for all phases. Total harmonic distortion (THD) is computed for all currents and voltages. A fixed function digital signal processor (DSP) executes this signal processing. The DSP program is stored in the internal ROM memory.

The ADE7880 is suitable for measuring active, reactive, and apparent energy in various 3-phase configurations, such as wye or delta services with, both, three and four wires. The ADE7880 provides system calibration features for each phase, that is, rms offset correction, phase calibration, and gain calibration. The CF1, CF2, and CF3 logic outputs provide a wide choice of power information: total active powers, apparent powers, or the sum of the current rms values, and fundamental active and reactive powers.

The ADE7880 contains waveform sample registers that allow access to all ADC outputs. The devices also incorporate power quality measurements, such as short duration low or high voltage detections, short duration high current variations, line voltage period measurement, and angles between phase voltages and currents. Two serial interfaces, SPI and I^2C, can be used to communicate with the ADE7880. A dedicated high speed interface, the high speed data capture (HSDC) port, can be used in conjunction with I^2C to provide access to the ADC outputs and real-time power information. The ADE7880 also has two interrupt request pins, $\overline{IRQ0}$ and $\overline{IRQ1}$, to indicate that an enabled interrupt event has occurred. Three specially designed low power modes ensure the continuity of energy accumulation when the ADE7880 is in a tampering situation. The ADE7880 is available in the 40-lead LFCSP, Pb-free package, pin-for-pin compatible with ADE7854, ADE7858, ADE7868, and ADE7878 devices.

[1] Protected by U.S. Patent 8,010,304 B2. Other patents pending.

Rev. C
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FUNCTIONAL BLOCK DIAGRAM

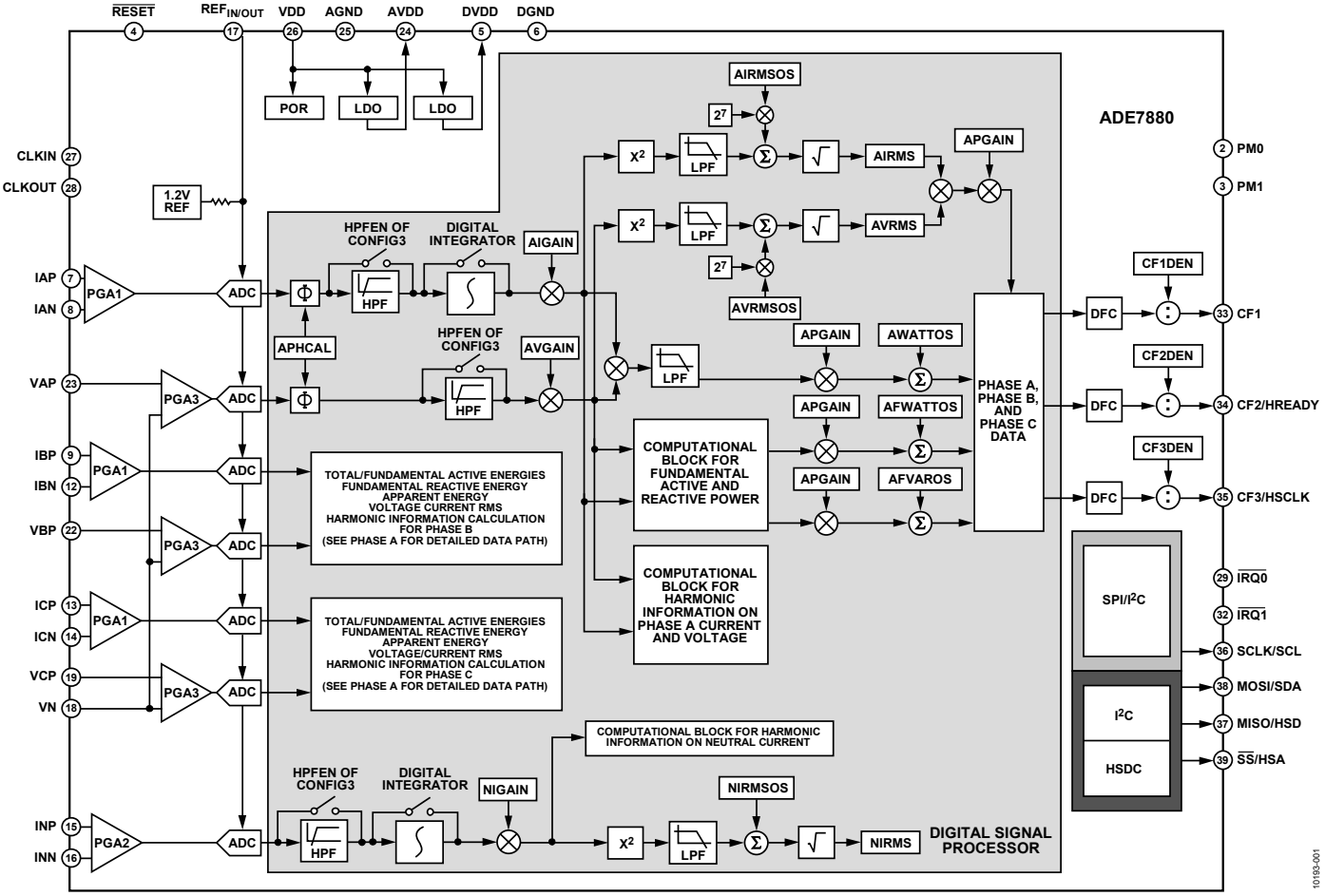

Figure 1. ADE7880 Functional Block Diagram

SPECIFICATIONS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C, T_{TYP} = 25°C.

Table 1.

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
ACTIVE ENERGY MEASUREMENT					
Active Energy Measurement Error (per Phase)					
Total Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
Fundamental Active Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 1
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 1, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 1
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ±100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Total Active Energy Measurement Bandwidth (−3 dB)		3.3		kHz	
REACTIVE ENERGY MEASUREMENT					
Reactive Energy Measurement Error (per Phase)					
Fundamental Reactive Energy		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1, 2, 4; integrator off, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 5000 to 1, PGA = 1, 2, 4; integrator off, pf = 0
		0.1		%	Over a dynamic range of 500 to 1, PGA = 8, 16; integrator on, pf = 0, gain compensation only
		0.2		%	Over a dynamic range of 2000 to 1, PGA = 8, 16; integrator on, pf = 0
AC Power Supply Rejection					VDD = 3.3 V + 120 mV rms/120 Hz, IPx = VPx = ± 100 mV rms
Output Frequency Variation		0.01		%	
DC Power Supply Rejection					VDD = 3.3 V ± 330 mV dc
Output Frequency Variation		0.01		%	
Fundamental Reactive Energy Measurement Bandwidth (−3 dB)		3.3		kHz	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
RMS MEASUREMENTS (PSM0 Mode)					
I RMS and V RMS Measurement Bandwidth (−3 dB)		3.3		kHz	
I RMS and V RMS Measurement Error		0.1		%	Over a dynamic range of 1000 to 1, PGA = 1
MEAN ABSOLUTE VALUE (MAV) MEASUREMENT (PSM1 Mode)					
I MAV Measurement Bandwidth		260		Hz	
I MAV Measurement Error		0.5		%	Over a dynamic range of 100 to 1, PGA = 1, 2, 4, 8
HARMONIC MEASUREMENTS					
Bandwidth (−3 dB)		3.3		kHz	
No attenuation Pass Band		2.8		kHz	
Fundamental Line Frequency, f_L	45		66	Hz	Voltage signal must have amplitudes greater than 100 mV peak at ADC stage. Set the SELFREQ bit of COMPMODE register based on the frequency. See the Managing Change in Fundamental Line Frequency section for details.
Maximum Number of Harmonics[3]			$\left[\frac{2800}{f_L}\right]$		
Absolute Maximum Number of Harmonics			63		
Harmonic RMS Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1 Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 10 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
Harmonic Active/Reactive Power Measurement Error		1		%	Instantaneous reading accuracy over a dynamic range of 1000 to 1 for harmonics of frequencies within the pass band; after the initial 750 ms settling time; PGA = 1 Accuracy over a dynamic range of 2000:1 for harmonics of frequencies within the pass band; average of 5 readings at 128 ms update rate, after the initial 750 ms setting time; PGA = 1
ANALOG INPUTS					
Maximum Signal Levels			±500	mV peak	PGA = 1, differential or single-ended inputs between the following pins: IAP and IAN, IBP and IBN, ICP and ICN, INP and INN; single-ended inputs between the following pins: VAP and VN, VBP and VN, VCP and VN
Input Impedance (DC)					
IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, and VCP Pins	490			kΩ	
VN Pin	170			kΩ	
ADC Offset		−35		mV	PGA = 1, uncalibrated error, see the Terminology section. Scales inversely proportional to the other PGA gains
Gain Error		±4		%	External 1.2 V reference

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
WAVEFORM SAMPLING					Sampling CLKIN/2048, 16.384 MHz/2048 = 8 kSPS
Current and Voltage Channels					See the Waveform Sampling Mode section
Signal-to-Noise Ratio, SNR		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Signal-to-Noise-and-Distortion Ratio, SINAD		72		dB	PGA = 1, fundamental frequency = 45 Hz to 65 Hz, see the Terminology section
Bandwidth (−3 dB)		3.3		kHz	
TIME INTERVAL BETWEEN PHASES					
Measurement Error		0.3		Degrees	Line frequency = 45 Hz to 65 Hz, HPF on
CF1, CF2, CF3 PULSE OUTPUTS					
Maximum Output Frequency		68.818		kHz	WTHR = VARTHR = VATHR = 3
Duty Cycle		50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is even and > 1
		(1 + 1/CFDEN) × 50		%	If CF1, CF2, or CF3 frequency > 6.25 Hz and CFDEN is odd and > 1
Active Low Pulse Width		80		ms	If CF1, CF2, or CF3 frequency < 6.25 Hz
Jitter		0.04		%	For CF1, CF2, or CF3 frequency = 1 Hz and nominal phase currents are larger than 10% of full scale
REFERENCE INPUT					
$REF_{IN/OUT}$ Input Voltage Range	1.1		1.3	V	Minimum = 1.2 V − 8%; maximum = 1.2 V + 8%
Input Capacitance			10	pF	
ON-CHIP REFERENCE					Nominal 1.2 V at the $REF_{IN/OUT}$ pin at T_A = 25°C
PSM0 and PSM1 Modes					
Temperature Coefficient	−50	±20	+50	ppm/°C	Drift across the entire temperature range of −40°C to +85°C is calculated with reference to 25°C; see the Reference Circuit section for more details
CLKIN					See the Crystal Circuit section for more details
Input Clock Frequency	16.22	16.384	16.55	MHz	
LOGIC INPUTS—MOSI/SDA, SCLK/SCL, $\overline{SS}$, $\overline{RESET}$, PM0, AND PM1					
Input High Voltage, V_{INH}	2.4			V	VDD = 3.3 V
Input Current, I_{IN}			82	nA	Input = VDD = 3.3 V
Input Low Voltage, V_{INL}			0.8	V	VDD = 3.3 V
Input Current, I_{IN}			−7.3	μA	Input = 0, VDD = 3.3 V
Input Capacitance, C_{IN}			10	pF	
LOGIC OUTPUTS—$\overline{IRQ0}$, $\overline{IRQ1}$, AND MISO/HSD					VDD = 3.3 V
Output High Voltage, V_{OH}	3.0			V	I_{SOURCE} = 800 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
CF1, CF2, CF3/HSCLK					
Output High Voltage, V_{OH}	2.4			V	I_{SOURCE} = 500 μA
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 8 mA
POWER SUPPLY					For specified performance
PSM0 Mode					
VDD Pin	2.97		3.63	V	Minimum = 3.3 V − 10%; maximum = 3.3 V + 10%
I_{DD}		25	28	mA	

Parameter[1, 2]	Min	Typ	Max	Unit	Test Conditions/Comments
PSM1 and PSM2 Modes					
VDD Pin	2.4		3.7	V	
I_{DD}					
PSM1 Mode		5.3	5.8	mA	
PSM2 Mode		0.2	0.27	mA	
PSM3 Mode					For specified performance
VDD Pin	2.4		3.7	V	
I_{DD} in PSM3 Mode		1.8	6	µA	

[1] See the Typical Performance Characteristics section.
[2] See the Terminology section for a definition of the parameters.
[3] $\left[\frac{2800}{f_L}\right]$ means the whole number of the division.

TIMING CHARACTERISTICS

VDD = 3.3 V ± 10%, AGND = DGND = 0 V, on-chip reference, CLKIN = 16.384 MHz, T_{MIN} to T_{MAX} = −40°C to +85°C. Note that dual function pin names are referenced by the relevant function only within the timing tables and diagrams (see the Pin Configuration and Function Descriptions section for full pin mnemonics and descriptions).

Table 2. I²C-Compatible Interface Timing Parameter

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**
SCL Clock Frequency	f_{SCL}	0	100	0	400	kHz
Hold Time (Repeated) Start Condition	$t_{HD;STA}$	4.0		0.6		µs
Low Period of SCL Clock	t_{LOW}	4.7		1.3		µs
High Period of SCL Clock	t_{HIGH}	4.0		0.6		µs
Set-Up Time for Repeated Start Condition	$t_{SU;STA}$	4.7		0.6		µs
Data Hold Time	$t_{HD;DAT}$	0.1	3.45	0.1	0.9	µs
Data Setup Time	$t_{SU;DAT}$	250		100		ns
Rise Time of Both SDA and SCL Signals	t_R		1000	20	300	ns
Fall Time of Both SDA and SCL Signals	t_F		300	20	300	ns
Setup Time for Stop Condition	$t_{SU;STO}$	4.0		0.6		µs
Bus Free Time Between a Stop and Start Condition	t_{BUF}	4.7		1.3		µs
Pulse Width of Suppressed Spikes	t_{SP}	N/A[1]			50	ns

[1] N/A means not applicable.

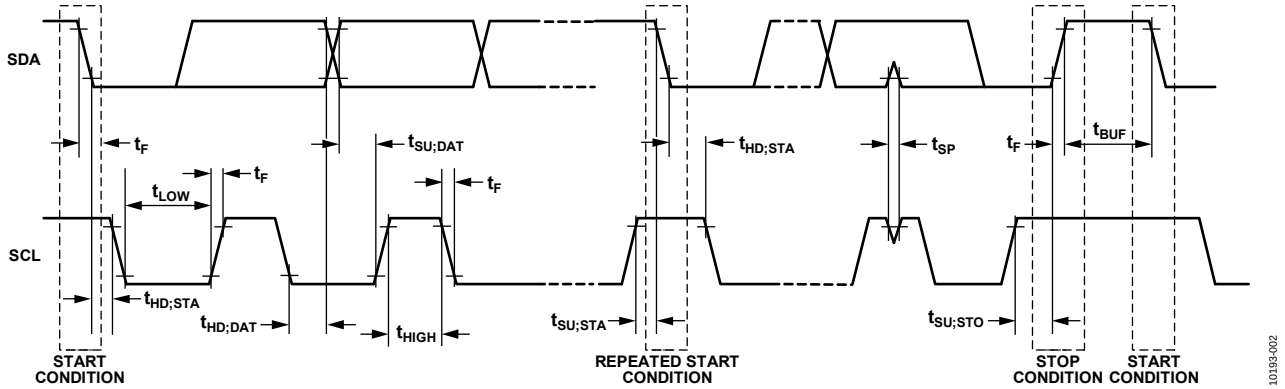

Figure 2. I²C-Compatible Interface Timing

Table 3. SPI Interface Timing Parameters

Parameter	Symbol	Min	Max	Unit
$\overline{SS}$ to SCLK Edge	t_{SS}	50		ns
SCLK Period		0.4	4000[1]	µs
SCLK Low Pulse Width	t_{SL}	175		ns
SCLK High Pulse Width	t_{SH}	175		ns
Data Output Valid After SCLK Edge	t_{DAV}		100	ns
Data Input Setup Time Before SCLK Edge	t_{DSU}	100		ns
Data Input Hold Time After SCLK Edge	t_{DHD}	5		ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
SCLK Rise Time	t_{SR}		20	ns
SCLK Fall Time	t_{SF}		20	ns
MISO Disable After $\overline{SS}$ Rising Edge	t_{DIS}		200	ns
$\overline{SS}$ High After SCLK Edge	t_{SFS}	0		ns

[1] Guaranteed by design.

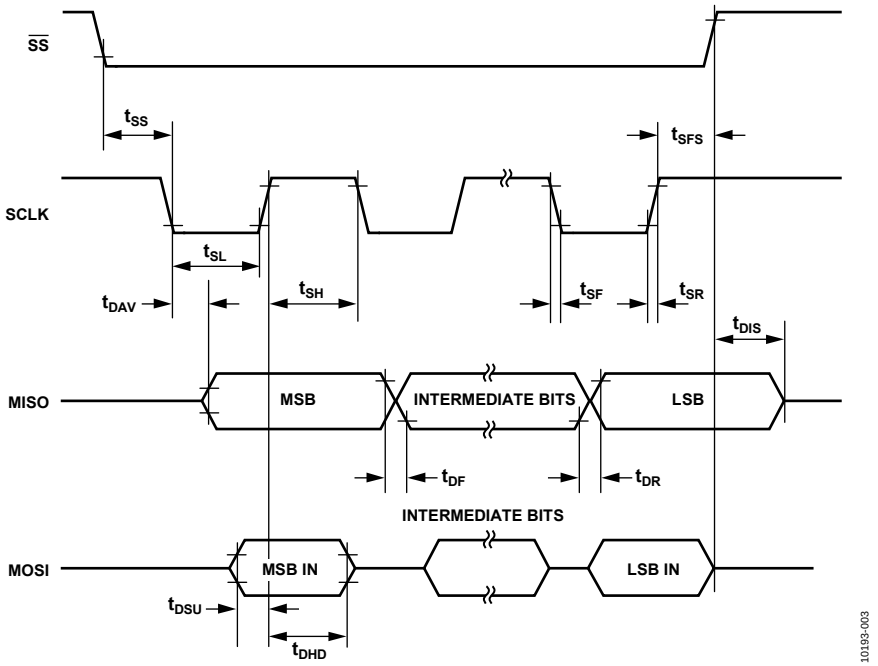

Figure 3. SPI Interface Timing

Table 4. HSDC Interface Timing Parameter

Parameter	Symbol	Min	Max	Unit
HSA to HSCLK Edge	t_{SS}	0		ns
HSCLK Period		125		ns
HSCLK Low Pulse Width	t_{SL}	50		ns
HSCLK High Pulse Width	t_{SH}	50		ns
Data Output Valid After HSCLK Edge	t_{DAV}		40	ns
Data Output Fall Time	t_{DF}		20	ns
Data Output Rise Time	t_{DR}		20	ns
HSCLK Rise Time	t_{SR}		10	ns
HSCLK Fall Time	t_{SF}		10	ns
HSD Disable After HSA Rising Edge	t_{DIS}	5		ns
HSA High After HSCLK Edge	t_{SFS}	0		ns

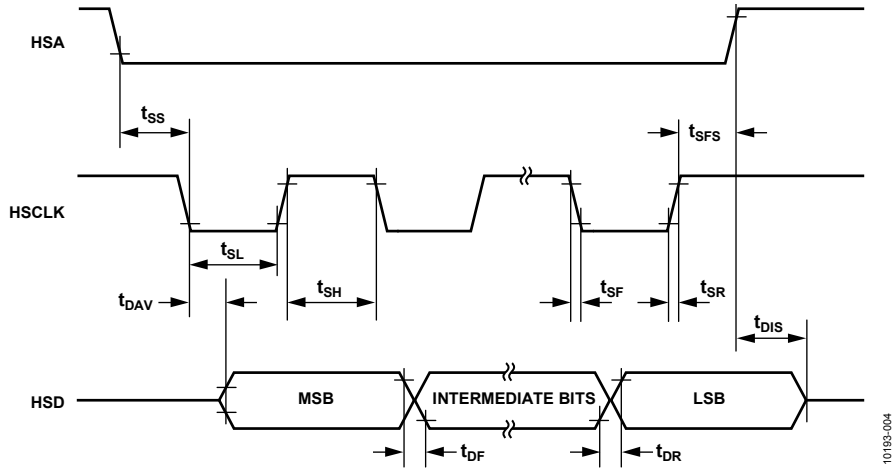

Figure 4. HSDC Interface Timing

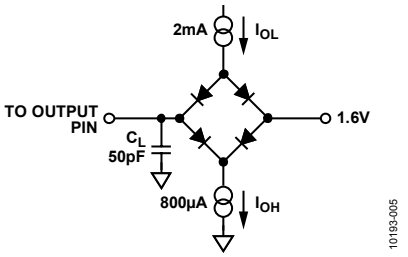

Figure 5. Load Circuit for Timing Specifications

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter[1]	Rating
VDD to AGND	−0.3 V to +3.7 V
VDD to DGND	−0.3 V to +3.7 V
Analog Input Voltage to AGND, IAP, IAN, IBP, IBN, ICP, ICN, VAP, VBP, VCP, VN	−2 V to +2 V
Analog Input Voltage to INP and INN	−2 V to +2 V
Reference Input Voltage to AGND	−0.3 V to VDD + 0.3 V
Digital Input Voltage to DGND	−0.3 V to VDD + 0.3 V
Digital Output Voltage to DGND	−0.3 V to VDD + 0.3 V
Operating Temperature	
Industrial Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	300°C

[1] Regarding the temperature profile used in soldering RoHS Compliant Parts, Analog Devices, Inc. advises that reflow profiles conform to J-STD 20 from JEDEC. Refer to JEDEC website for the latest revision.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified equal to 29.3°C/W; θ_{JC} is specified equal to 1.8°C/W.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
40-Lead LFCSP	29.3	1.8	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

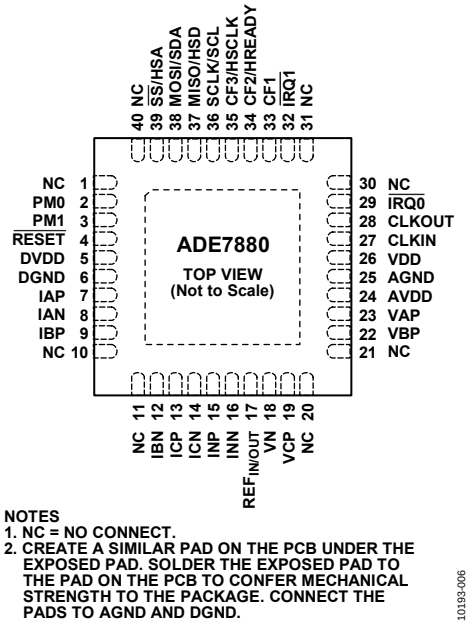

Figure 6. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20, 21, 30, 31, 40	NC	No Connect. Do not connect to these pins. These pins are not connected internally.
2	PM0	Power Mode Pin 0. This pin, combined with PM1, defines the power mode of the ADE7880, as described in Table 8.
3	PM1	Power Mode Pin 1. This pin defines the power mode of the ADE7880 when combined with PM0, as described in Table 8.
4	$\overline{\text{RESET}}$	Reset Input, Active Low. In PSM0 mode, this pin must stay low for at least 10 µs to trigger a hardware reset.
5	DVDD	2.5 V Output of the Digital Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
6	DGND	Ground Reference. This pin provides the ground reference for the digital circuitry.
7, 8	IAP, IAN	Analog Inputs for Current Channel A. This channel is used with the current transducers and is referenced in this data sheet as Current Channel A. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel B and Channel C.
9, 12	IBP, IBN	Analog Inputs for Current Channel B. This channel is used with the current transducers and is referenced in this data sheet as Current Channel B. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel C and Channel A.
13, 14	ICP, ICN	Analog Inputs for Current Channel C. This channel is used with the current transducers and is referenced in this data sheet as Current Channel C. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA equal to the ones on Channel A and Channel B.
15, 16	INP, INN	Analog Inputs for Neutral Current Channel N. This channel is used with the current transducers and is referenced in this data sheet as Current Channel N. These inputs are fully differential voltage inputs with a maximum differential level of ±0.5 V. This channel also has an internal PGA, different from the ones found on the A, B, and C channels.
17	$\text{REF}_{\text{IN/OUT}}$	This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 1.2 V. An external reference source with 1.2 V ± 8% can also be connected at this pin. In either case, decouple this pin to AGND with a 4.7 µF capacitor in parallel with a ceramic 100 nF capacitor. After reset, the on-chip reference is enabled.

Pin No.	Mnemonic	Description
18, 19, 22, 23	VN, VCP, VBP, VAP	Analog Inputs for the Voltage Channel. This channel is used with the voltage transducer and is referenced as the voltage channel in this data sheet. These inputs are single-ended voltage inputs with a maximum signal level of ±0.5 V with respect to VN for specified operation. This channel also has an internal PGA.
24	AVDD	2.5 V Output of the Analog Low Dropout (LDO) Regulator. Decouple this pin with a 4.7 µF capacitor in parallel with a ceramic 220 nF capacitor. Do not connect external active circuitry to this pin.
25	AGND	Ground Reference. This pin provides the ground reference for the analog circuitry. Tie this pin to the analog ground plane or to the quietest ground reference in the system. Use this quiet ground reference for all analog circuitry, for example, antialiasing filters, current, and voltage transducers.
26	VDD	Supply Voltage. This pin provides the supply voltage. In PSM0 (normal power mode), maintain the supply voltage at 3.3 V ± 10% for specified operation. In PSM1 (reduced power mode), PSM2 (low power mode), and PSM3 (sleep mode), when the ADE7880 is supplied from a battery, maintain the supply voltage between 2.4 V and 3.7 V. Decouple this pin to DGND with a 10 µF capacitor in parallel with a ceramic 100 nF capacitor.
27	CLKIN	Master Clock. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT-cut crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7880. The clock frequency for specified operation is 16.384 MHz. Use ceramic load capacitors of a few tens of picofarad with the gate oscillator circuit. Refer to the data sheet of the crystal manufacturer for load capacitance requirements.
28	CLKOUT	A crystal can be connected across this pin and CLKIN (as previously described with Pin 27 in this table) to provide a clock source for the ADE7880.
29, 32	$\overline{\text{IRQ0}}$, $\overline{\text{IRQ1}}$	Interrupt Request Outputs. These are active low logic outputs. See the Interrupts section for a detailed presentation of the events that can trigger interrupts.
33, 34, 35	CF1, CF2/HREADY, CF3/HSCLK	Calibration Frequency (CF) Logic Outputs. These outputs provide power information based on the CF1SEL[2:0], CF2SEL[2:0], and CF3SEL[2:0] bits in the CFMODE register. These outputs are used for operational and calibration purposes. The full-scale output frequency can be scaled by writing to the CF1DEN, CF2DEN, and CF3DEN registers, respectively (see the Energy-to-Frequency Conversion section). CF2 is multiplexed with the HREADY signal generated by the harmonic calculations block. CF3 is multiplexed with the serial clock output of the HSDC port.
36	SCLK/SCL	Serial Clock Input for SPI Port/Serial Clock Input for I^2C Port. All serial data transfers are synchronized to this clock (see the Serial Interfaces section). This pin has a Schmidt trigger input for use with a clock source that has a slow edge transition time, for example, optoisolator outputs.
37	MISO/HSD	Data Out for SPI Port/Data Out for HSDC Port.
38	MOSI/SDA	Data In for SPI Port/Data Out for I^2C Port.
39	$\overline{\text{SS}}$/HSA	Slave Select for SPI Port/HSDC Port Active.
EP	Exposed Pad	Create a similar pad on the PCB under the exposed pad. Solder the exposed pad to the pad on the PCB to confer mechanical strength to the package. Connect the pads to AGND and DGND.

TYPICAL PERFORMANCE CHARACTERISTICS

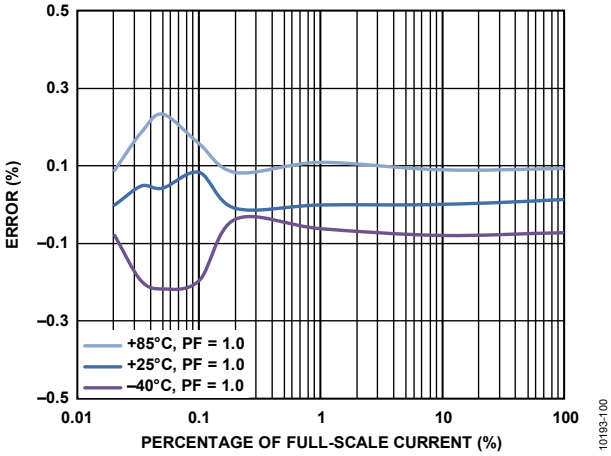

Figure 7. Total Active Energy Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

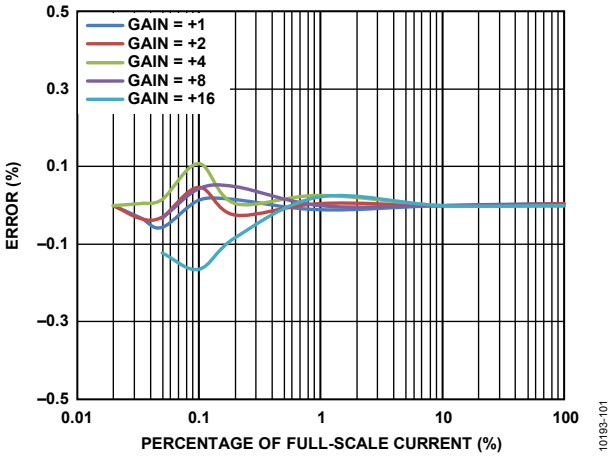

Figure 8. Total Active Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

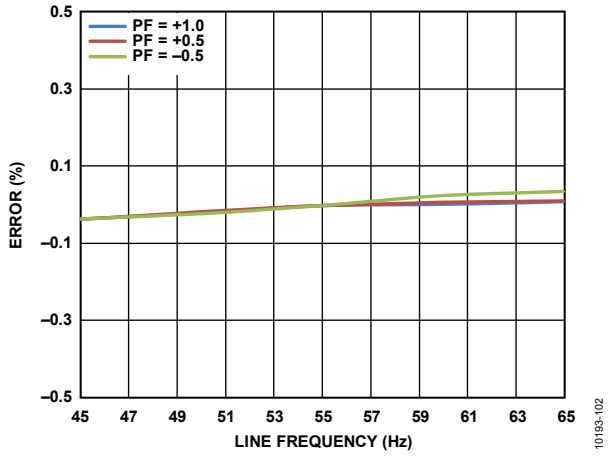

Figure 9. Total Active Energy Error as Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

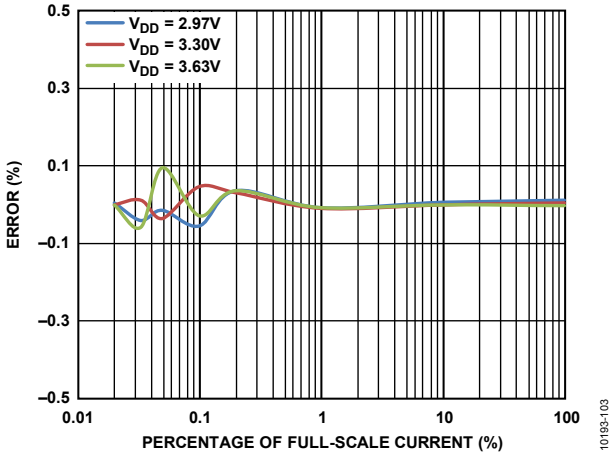

Figure 10. Total Active Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

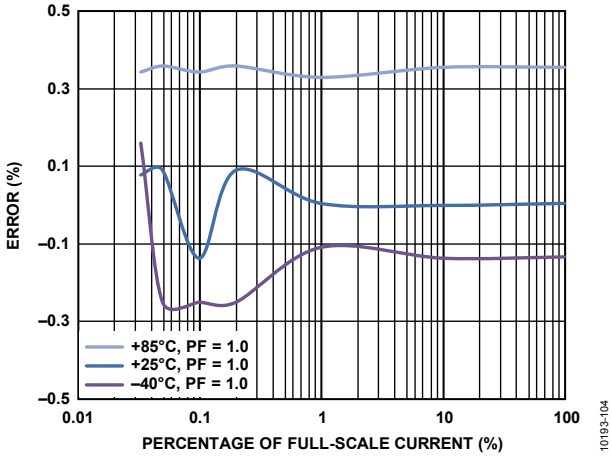

Figure 11. Total Active Energy Error as Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

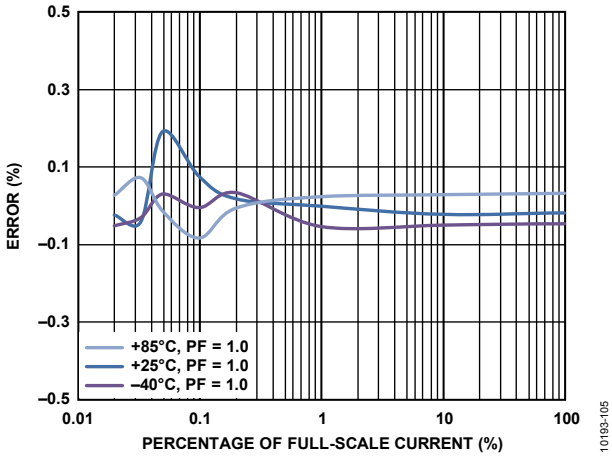

Figure 12. Fundamental Active Energy Error as Percentage of Reading (Gain = +1, Power Factor = 1) over Temperature with Internal Reference and Integrator Off

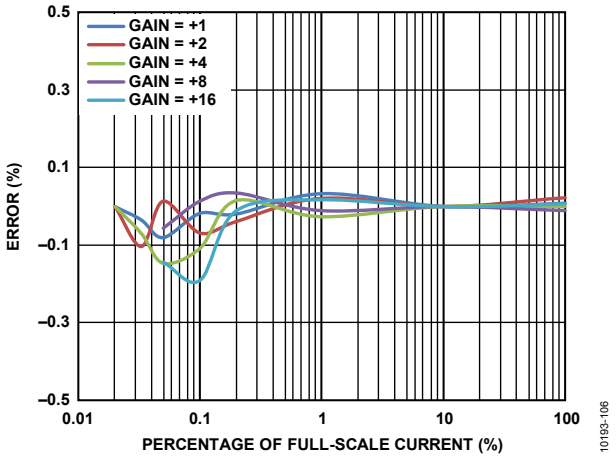

Figure 13. Fundamental Active Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

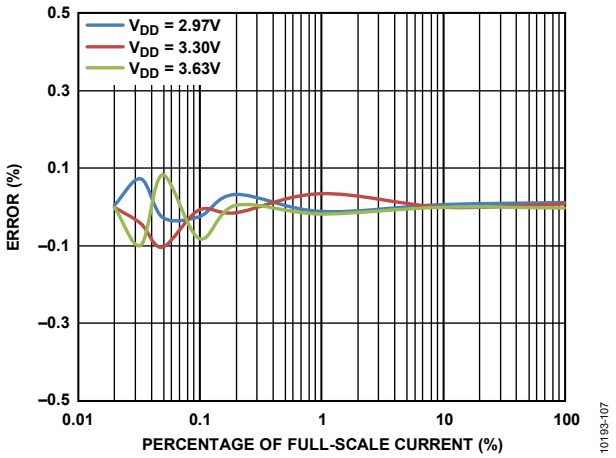

Figure 14. Fundamental Active Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

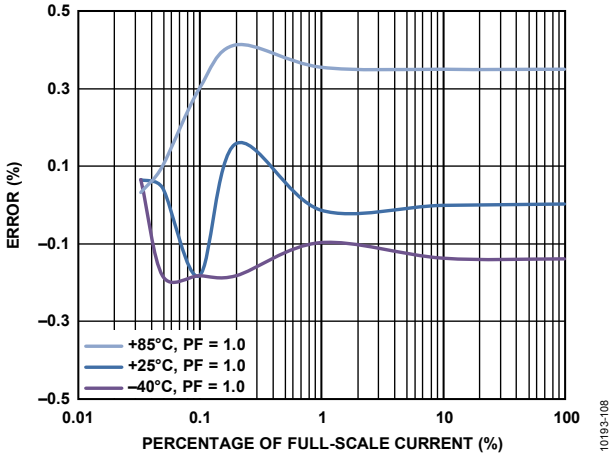

Figure 15. Fundamental Active Energy Error as Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator On

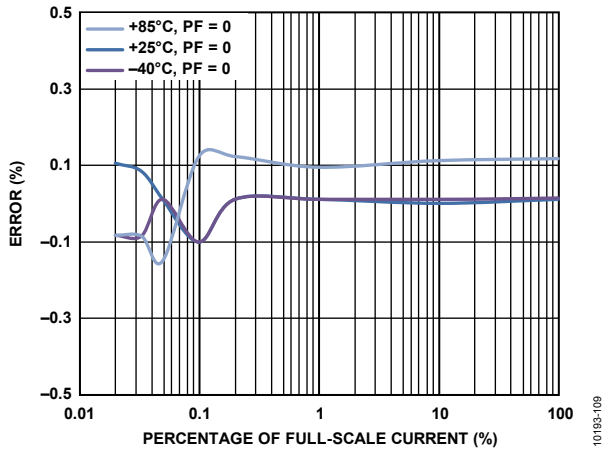

Figure 16. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1, Power Factor = 0) over Temperature with Internal Reference and Integrator Off

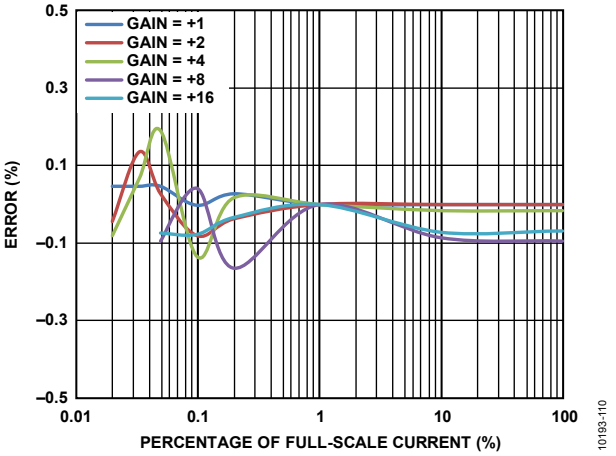

Figure 17. Fundamental Reactive Energy Error as Percentage of Reading over Gain with Internal Reference and Integrator Off

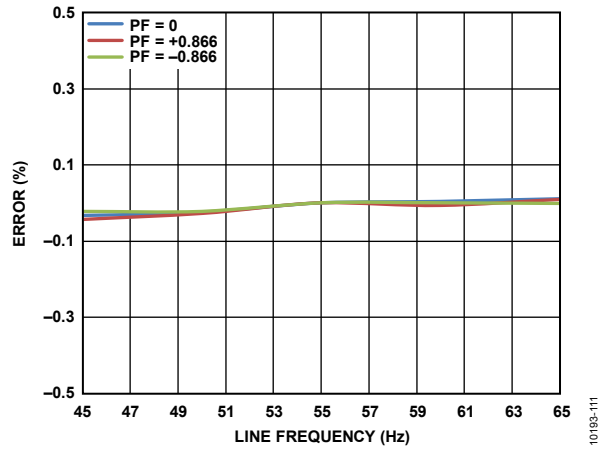

Figure 18. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1) over Frequency with Internal Reference and Integrator Off

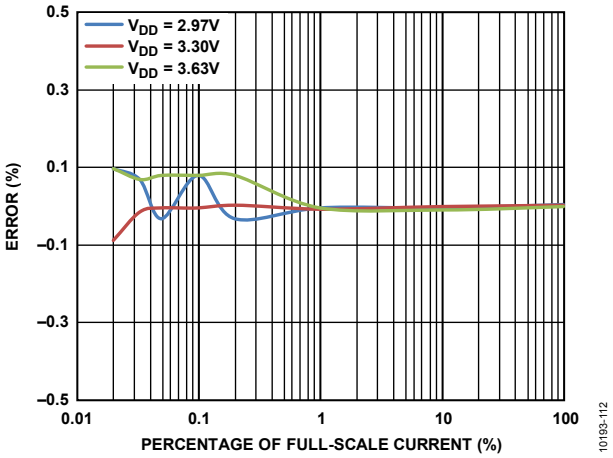

Figure 19. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +1) over Power Supply with Internal Reference and Integrator Off

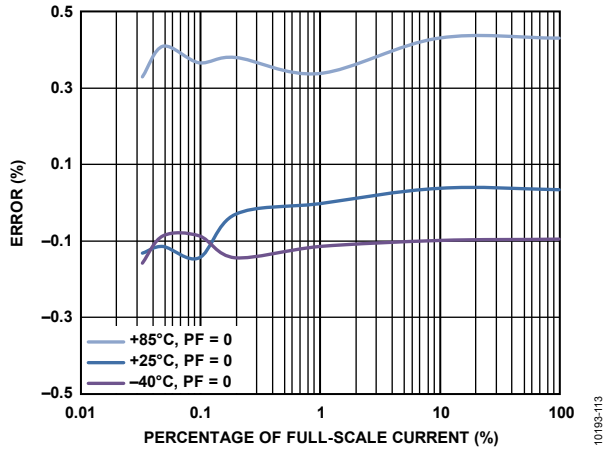

Figure 20. Fundamental Reactive Energy Error as Percentage of Reading (Gain = +16) over Temperature with Internal Reference and Integrator On

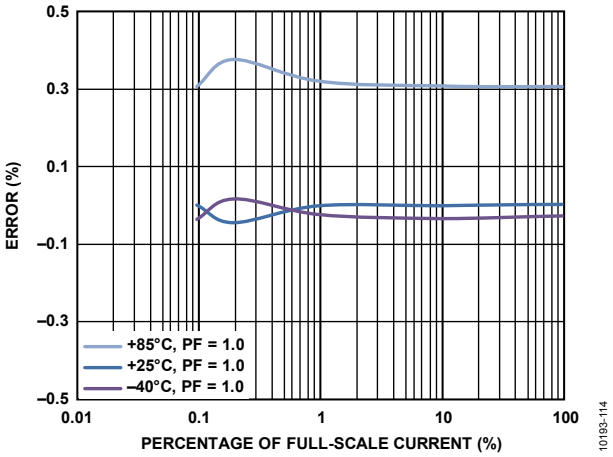

Figure 21. I RMS Error as Percentage of Reading (Gain = +1) over Temperature with Internal Reference and Integrator Off

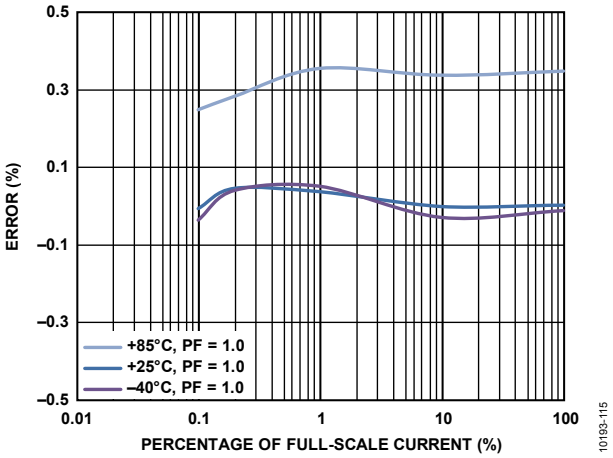

Figure 22. V RMS Error as a Percentage of Reading (Gain = +1) over Temperature with Internal Reference

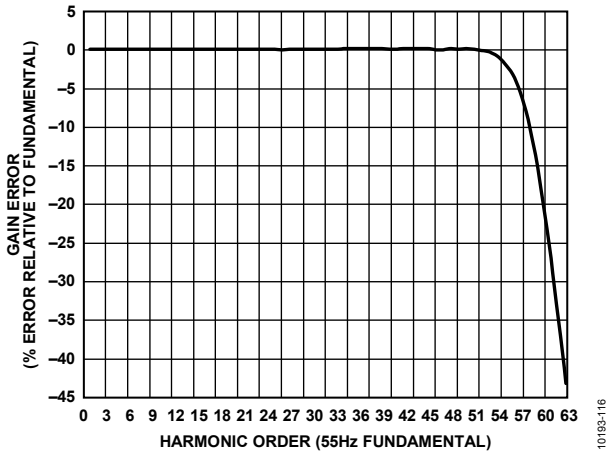

Figure 23. Harmonic I RMS Error as a Percentage of Reading over Harmonic Order, 63 Harmonics, 55 Hz Fundamental, 30 Averages per Reading, 750 ms Settling time, 125 µs Update Rate

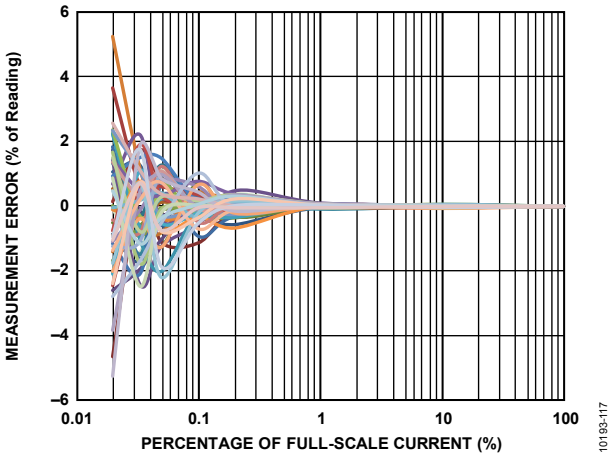

Figure 24. Harmonic I RMS Error as a Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time; 125 µs Update Rate

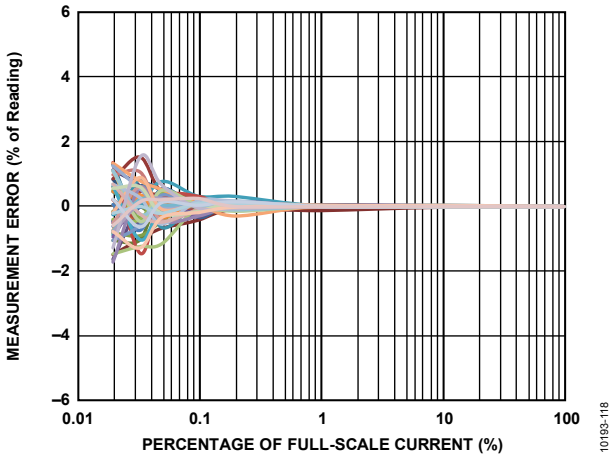

Figure 25. Harmonic I RMS Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

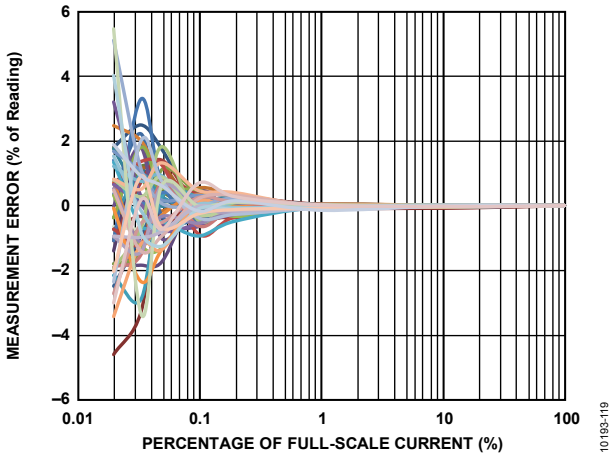

Figure 26. Harmonic Active Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

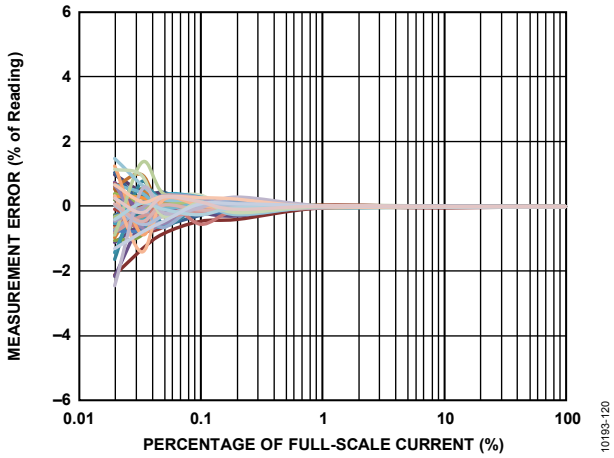

Figure 27. Harmonic Active Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

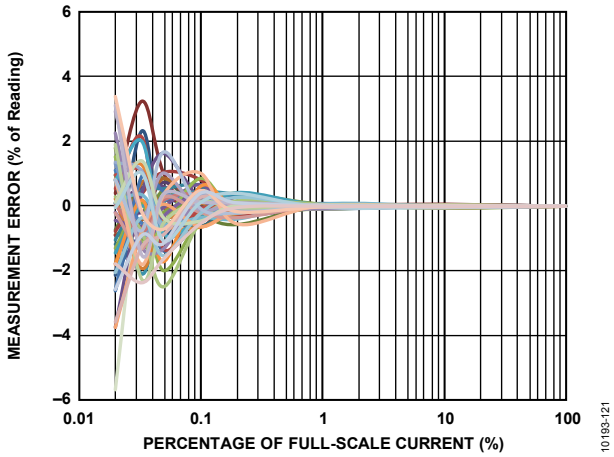

Figure 28. Harmonic Reactive Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

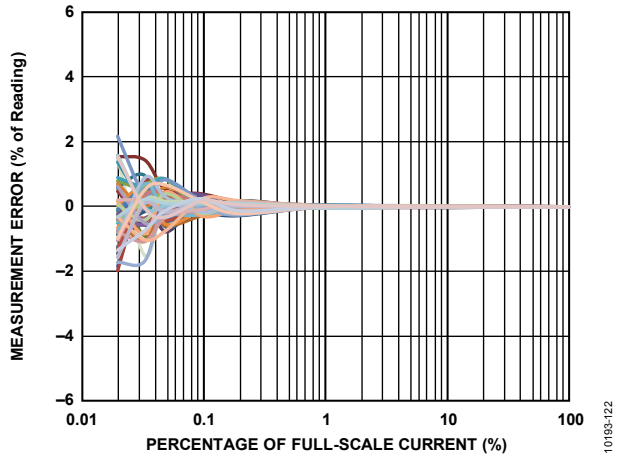

Figure 29. Harmonic Reactive Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

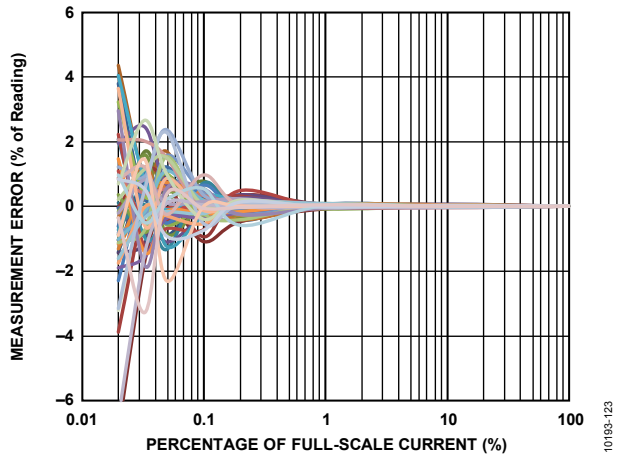

Figure 30. Harmonic Apparent Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, Single Reading, 750 ms Settling Time, 125 µs Update Rate

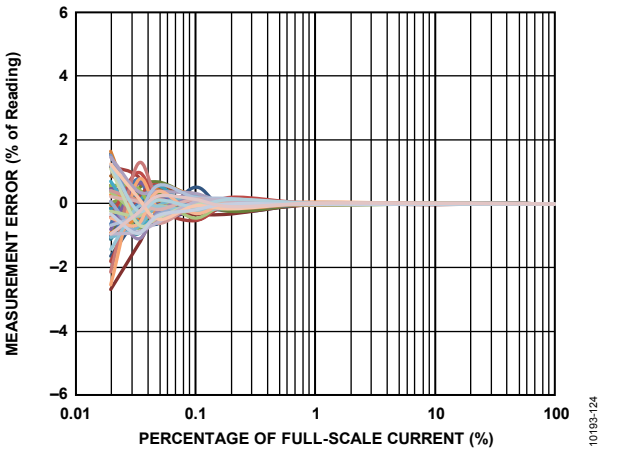

Figure 31. Harmonic Apparent Power Error as Percentage of Reading (Gain = +1), 51 Harmonics, 55 Hz Fundamental, 10 Averages per Reading, 750 ms Settling Time, 125 µs Update Rate

TEST CIRCUIT

In Figure 32, the PM1 and PM0 pins are pulled up internally to VDD. Select the mode of operation by using a microcontroller to programmatically change the pin values. See the Power Management section for details.

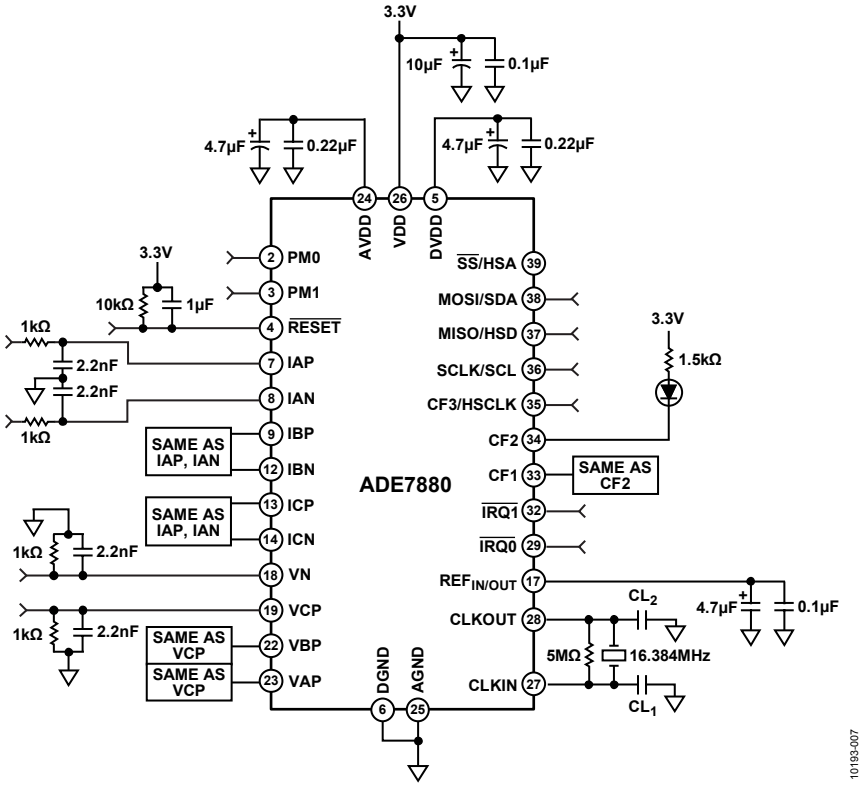

Figure 32. Test Circuit

TERMINOLOGY

Measurement Error

The error associated with the energy measurement made by the ADE7880 is defined by

$$Measurement\ Error = \frac{Energy\ Registered\ by\ ADE7880 - True\ Energy}{True\ Energy} \times 100\% \quad (1)$$

Power Supply Rejection (PSR)

This quantifies the ADE7880 measurement error as a percentage of reading when the power supplies are varied. For the ac PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when an ac signal (120 mV rms at 100 Hz) is introduced onto the supplies. Any error introduced by this ac signal is expressed as a percentage of reading (see the Measurement Error definition).

For the dc PSR measurement, a reading at nominal supplies (3.3 V) is taken. A second reading is obtained with the same input signal levels when the power supplies are varied ±10%. Any error introduced is expressed as a percentage of the reading.

ADC Offset

ADC offset refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND, the ADCs still see a dc analog input signal. The magnitude of the offset depends on the gain and input range selection. The high-pass filter (HPF) removes the offset from the current and voltage channels; therefore, the power calculation remains unaffected by this offset.

Gain Error

The gain error in the ADCs of the ADE7880 is defined as the difference between the measured ADC output code (minus the offset) and the ideal output code (see the Current Channel ADC section and the Voltage Channel ADC section). The difference is expressed as a percentage of the ideal code.

CF Jitter

The period of pulses at one of the CF1, CF2, or CF3 pins is continuously measured. The maximum, minimum, and average values of four consecutive pulses are computed as follows:

$$Maximum = max(Period_0, Period_1, Period_2, Period_3)$$

$$Minimum = min(Period_0, Period_1, Period_2, Period_3)$$

$$Average = \frac{Period_0 + Period_1 + Period_2 + Period_3}{4}$$

The CF jitter is then computed as

$$CF_{JITTER} = \frac{Maximum - Minimum}{Average} \times 100\% \quad (2)$$

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 3.3 kHz, excluding harmonics and dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SNR is expressed in decibels.

Signal-to-Noise-and-Distortion (SINAD) Ratio

SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below 3.3 kHz, including harmonics but excluding dc. The input signal contains only the fundamental component. The spectral components are calculated over a 2 sec window. The value for SINAD is expressed in decibels.

Harmonic Power Measurement Error

To measure the error in the harmonic active and reactive power calculations made by the ADE7880, the voltage channel is supplied with a signal comprising a fundamental and one harmonic component with amplitudes equal to 250 mV. The current channel is supplied with a signal comprising a fundamental with amplitude of 50 mV and one harmonic component of the same index as the one in the voltage channel. The amplitude of the harmonic is varied from 250 mV, down to 250 μV, 2000 times lower than full scale.

The error is defined by

$$Measurement\ Error = \frac{Power\ Registered\ by\ ADE7880 - True\ Power}{True\ Power} \times 100\% \quad (3)$$

POWER MANAGEMENT

The ADE7880 has four modes of operation, determined by the state of the PM0 and PM1 pins (see Table 8). These pins provide complete control of the ADE7880 operation and can easily be connected to an external microprocessor I/O. The PM0 and PM1 pins have internal pull-up resistors. See Table 10 and Table 11 for a list of actions that are recommended before and after setting a new power mode.

Table 8. Power Supply Modes

Power Supply Modes	PM1	PM0
PSM0, Normal Power Mode	0	1
PSM1, Reduced Power Mode	0	0
PSM2, Low Power Mode	1	0
PSM3, Sleep Mode	1	1

PSM0—NORMAL POWER MODE (ALL PARTS)

In PSM0 mode, the ADE7880 is fully functional. For the ADE7880 to enter this mode, the PM0 pin is set to high, and the PM1 pin is set to low. If the ADE7880 is in PSM1, PSM2, or PSM3 mode and is switched into PSM0 mode, then all control registers take the default values with the exception of the threshold register, LPOILVL, which is used in PSM2 mode, and the CONFIG2 register, both of which maintain their values.

The ADE7880 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition is finished. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with the corresponding bit set to 1. Bit 15 (RSTDONE) in the interrupt mask register does not have any functionality attached even if the $\overline{\text{IRQ1}}$ pin goes low when Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This makes the RSTDONE interrupt unmaskable.

PSM1—REDUCED POWER MODE

In the reduced power mode, PSM1, the ADE7880 measures the mean absolute values (mav) of the 3-phase currents and stores the results in the AIMAV, BIMAV, and CIMAV 20-bit registers. This mode is useful in missing neutral cases in which the voltage supply of the ADE7880 is provided by an external battery. The serial ports, I^2C or SPI, are enabled in this mode; the active port can be used to read the AIMAV, BIMAV, and CIMAV registers. Do not read any of the other registers as their values are not guaranteed in this mode. Similarly, the ADE7880 does not take a write operation into account by in this mode.

In summary, in this mode, it is not recommended to access any register other than AIMAV, BIMAV, and CIMAV. The circuit that computes the rms estimates is also active during PSM0; therefore, its calibration can be completed in either PSM0 mode or in PSM1 mode. Note that the ADE7880 does not provide any register to store or process the corrections resulting from the calibration process. The external microprocessor stores the gain values in connection with these measurements and uses them during PSM1 (see the Current Mean Absolute Value Calculation section for more details on the xIMAV registers).

The 20-bit mean absolute value measurements done in PSM1, although also available in PSM0, are different from the rms measurements of phase currents and voltages executed only in PSM0 and stored in the HxIRMS and HxVRMS 24-bit registers. See the Current Mean Absolute Value Calculation section for details.

If the ADE7880 is set in PSM1 mode after being in PSM0 mode, the ADE7880 begins the mean absolute value calculations without any delay. The xIMAV registers are accessible at any time; however, if the ADE7880 is set in PSM1 mode after being in PSM2 or PSM3 modes, the ADE7880 signals the start of the mean absolute value computations by triggering the $\overline{\text{IRQ1}}$ pin low. The xIMAV registers can be accessed only after this moment.

PSM2—LOW POWER MODE

In the low power mode, PSM2, the ADE7880 compares all phase currents against a threshold for a period of 0.02 × (LPLINE[4:0] + 1) seconds, independent of the line frequency. LPLINE[4:0] are Bits[7:3] of the LPOILVL register (see Table 9).

Table 9. LPOILVL Register

Bit	Mnemonic	Default	Description
[2:0]	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8
[7:3]	LPLINE[4:0]	00000	The measurement period is (LPLINE[4:0] + 1)/50 sec

The threshold is derived from Bits[2:0] (LPOIL[2:0]) of the LPOILVL register as LPOIL[2:0]/8 of full scale. Every time one phase current becomes greater than the threshold, a counter is incremented. If every phase counter remains below LPLINE[4:0] + 1 at the end of the measurement period, then the $\overline{\text{IRQ0}}$ pin is triggered low. If a single phase counter becomes greater or equal to LPLINE[4:0] + 1 at the end of the measurement period, the $\overline{\text{IRQ1}}$ pin is triggered low. Figure 33 illustrates how the ADE7880 behaves in PSM2 mode when LPLINE[4:0] = 2 and LPOIL[2:0] = 3. The test period is three 50 Hz cycles (60 ms), and the Phase A current rises above the LPOIL[2:0] threshold three times. At the end of the test period, the $\overline{\text{IRQ1}}$ pin is triggered low.

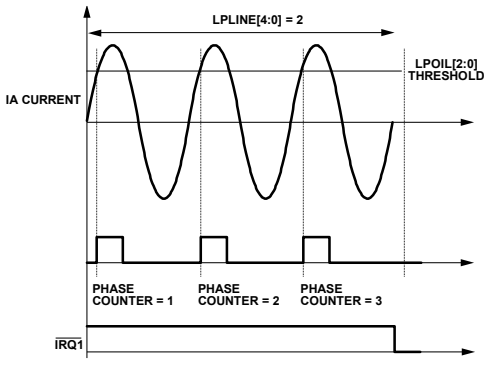

Figure 33. PSM2 Mode Triggering $\overline{\text{IRQ}}$ Pin for LPLINE[4:0] = 2 (50 Hz Systems)

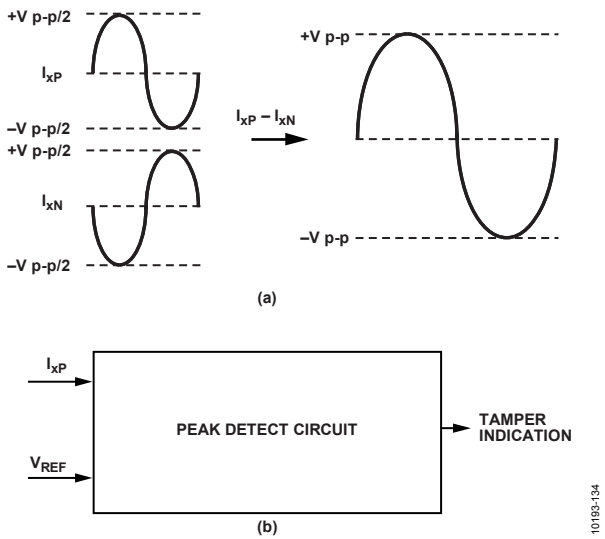

Figure 34. PSM2 Low Power Mode Peak Detection

The PSM2 level threshold comparison works based on a peak detection methodology. The peak detect circuit makes the comparison based on the positive terminal current channel input, I_{AP}, I_{BP}, and I_{CP} (see Figure 34). In case of differential inputs being applied to the current channels, Figure 34 shows the differential antiphase signals at each of the current input terminals, I_{xP} and I_{xN}, and the net differential current, $I_{xP} - I_{xN}$.

The I²C or SPI port is not functional during this mode. The PSM2 mode reduces the power consumption required to monitor the currents when there is no voltage input and the voltage supply of the ADE7880 is provided by an external battery. If the $\overline{\text{IRQ0}}$ pin is triggered low at the end of a measurement period, it signifies all phase currents stayed below threshold and, therefore, there is no current flowing through the system. At this point, the external microprocessor sets the ADE7880 into sleep mode PSM3. If the $\overline{\text{IRQ1}}$ pin is triggered low at the end of the measurement period, it signifies that at least one current input is above the defined threshold and current is flowing through the system, although no voltage is present at the ADE7880 pins. This situation is often called missing neutral and is considered a tampering situation, at which point the external microprocessor sets the ADE7880 into PSM1 mode, measures the mean absolute values of phase currents, and integrates the energy based on their values and the nominal voltage.

It is recommended to use the ADE7880 in PSM2 mode when Bits[2:0] (PGA1[2:0]) of the Gain register are equal to 1 or 2. These bits represent the gain in the current channel data path. It is not recommended to use the ADE7880 in PSM2 mode when the PGA1[2:0] bits are equal to 4, 8, or 16.

PSM3—SLEEP MODE (ALL PARTS)

In sleep mode, the ADE7880 has most of its internal circuits turned off and the current consumption is at its lowest level. The I²C, HSDC, and SPI ports are not functional during this mode, and the $\overline{\text{RESET}}$, SCLK/SCL, MOSI/SDA, and $\overline{\text{SS}}$/HSA pins must be set high.

Table 10. Power Modes and Related Characteristics

Power Mode	All Registers[1]	LPOILVL, CONFIG2	I²C/SPI	Functionality
PSM0				
State After Hardware Reset	Set to default	Set to default	I²C enabled	All circuits are active and DSP is in idle mode.
State After Software Reset	Set to default	Unchanged	Active serial port is unchanged if lock-in procedure has been previously executed	All circuits are active and DSP is in idle mode.
PSM1	Not available	PSM0 values retained	Enabled	Current mean absolute values are computed and the results are stored in the AIMAV, BIMAV, and CIMAV registers. The I²C or SPI serial port is enabled with limited functionality.
PSM2	Not available	PSM0 values retained	Disabled	Compares phase currents against the threshold set in LPOILVL. Triggers $\overline{\text{IRQ0}}$or $\overline{\text{IRQ1}}$ pins accordingly. The serial ports are not available.
PSM3	Not available	PSM0 values retained	Disabled	Internal circuits shut down and the serial ports are not available.

[1] Setting for all registers except the LPOILVL and CONFIG2 registers.

Table 11. Recommended Actions When Changing Power Modes

Initial Power Mode	Before Setting Next Power Mode	Next Power Mode			
		PSM0	PSM1	PSM2	PSM3
PSM0	Stop DSP by setting the Run register = 0x0000 Disable HSDC by clearing Bit 6 (HSDCEN) to 0 in the CONFIG register Mask interrupts by setting MASK0 = 0x0 and MASK1 = 0x0 Erase interrupt status flags in the STATUS0 and STATUS1 registers		Current mean absolute values (mav) computed immediately xIMAV registers can be accessed immediately	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM1	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1		Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	No action necessary
PSM2	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin triggered low Current mean absolute values compute at this moment xIMAV registers may be accessed from this moment		No action necessary
PSM3	No action necessary	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Poll the STATUS1 register until Bit 15 (RSTDONE) is set to 1	Wait until the $\overline{\text{IRQ1}}$ pin is triggered low Current mav circuit begins computations at this time xIMAV registers can be accessed from this moment	Wait until the $\overline{\text{IRQ0}}$ or $\overline{\text{IRQ1}}$ pin is triggered accordingly	

POWER-UP PROCEDURE

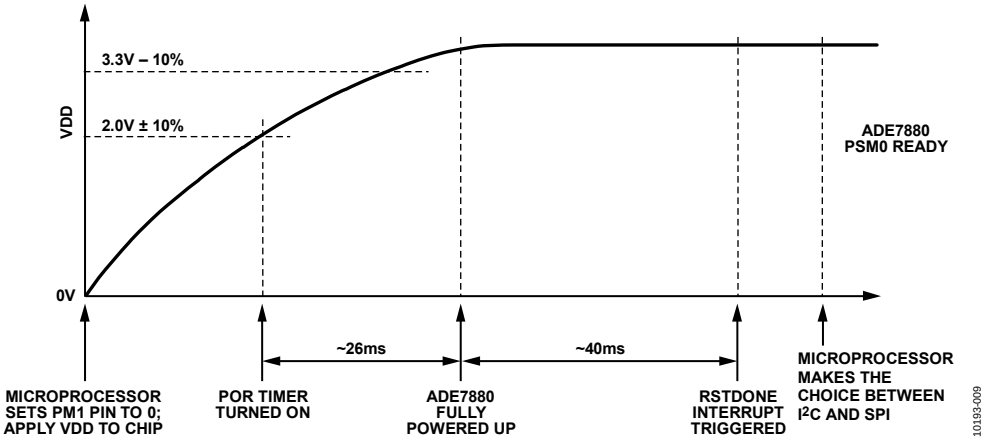

Figure 35. Power-Up Procedure

The ADE7880 contains an on-chip power supply monitor that supervises the power supply (VDD). At power-up, the device is inactive until VDD reaches 2.0 V ± 10%. When VDD crosses this threshold, the power supply monitor keeps the device in the inactive state for an additional 26 ms to allow VDD to rise to 3.3 V − 10%, the minimum recommended supply voltage.

The PM0 and PM1 pins have internal pull-up resistors, but it is necessary to set the PM1 pin to Logic 0, either through a microcontroller or by grounding the PM1 pin externally, before powering up the chip. The PM0 pin can remain open as it is held high, due to the internal pull-up resistor. This ensures that the ADE7880 always powers up in PSM0 (normal) mode. The time from the chip being powered up completely to all functionality being enabled is about 40 ms (see Figure 35). It is necessary to ensure that the $\overline{\text{RESET}}$ pin is held high during the entire power-up procedure.

If PSM0 mode is the only desired power mode, the PM1 pin can be tied to ground externally. When the ADE7880 enters PSM0 mode, the I²C port is the active serial port. To use the SPI port, toggle the $\overline{\text{SS}}$/HSA pin three times from high to low.

To lock I²C as the active serial port, set Bit 1 (I2C_LOCK) of the CONFIG2 register to 1. From this moment, the device ignores spurious toggling of the $\overline{\text{SS}}$/HSA pin, and a switch to the SPI port is no longer possible.

If SPI is the active serial port, any write to the CONFIG2 register locks the port, and a switch to the I²C port is no longer possible. To use the I²C port, the ADE7880 must be powered down or the device must be reset by setting the $\overline{\text{RESET}}$ pin low. After the serial port is locked, the serial port selection is maintained when the device changes from one PSMx power mode to another.

Immediately after entering PSM0 mode, all registers in the ADE7880 are set to their default values, including the CONFIG2 and LPOILVL registers.

The ADE7880 signals the end of the transition period by pulling the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is cleared to 0 during the transition period and is set to 1 when the transition ends. Writing the STATUS1 register with the RSTDONE bit set to 1 clears the status bit and returns the $\overline{\text{IRQ1}}$ pin high. Because RSTDONE is an unmaskable interrupt, Bit 15 (RSTDONE) in the STATUS1 register must be cancelled for the $\overline{\text{IRQ1}}$ pin to return high. Wait until the $\overline{\text{IRQ1}}$ pin goes low before accessing the STATUS1 register to test the state of the RSTDONE bit. At this point, as a good programming practice, cancel all other status flags in the STATUS1 and STATUS0 registers by writing the corresponding bits with 1.

Initially, the DSP is in idle mode and, therefore, does not execute any instructions. This is the moment to initialize all registers in the ADE7880. See the Digital Signal Processor section for the proper procedure to initialize all registers and start the metering.

If the supply voltage, VDD, falls lower than 2.0 V ± 10%, the ADE7880 enters an inactive state, which means that no measurements or computations are executed.

If the $\overline{\text{RESET}}$ pin is held low while the IC powers up or if the power-up sequence timing cannot be maintained as per Figure 35, perform the following sequence of write operations prior to starting the DSP (setting the RUN register to 0x01), to ensure that the modulators are reset properly.

1. 8-bit write: 0xAD is written at Address 0xE7FE.
2. 8-bit write: 0x14 is written at Address 0xE7E2.
3. Wait 200 µs.
4. 8-bit write: 0xAD is written at Address 0xE7FE.
5. 8-bit write: 0x04 is written at Address 0xE7E2.

HARDWARE RESET

The ADE7880 has a $\overline{\text{RESET}}$ pin. If the ADE7880 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is set low, then the ADE7880 enters the hardware reset state. The ADE7880 must be in PSM0 mode for a hardware reset to be considered. Setting the $\overline{\text{RESET}}$ pin low while the ADE7880 is in PSM1, PSM2, and PSM3 modes does not have any effect.

If the ADE7880 is in PSM0 mode and the $\overline{\text{RESET}}$ pin is toggled from high to low and then back to high after at least 10 µs, all the registers are set to their default values, including the CONFIG2 and LPOILVL registers. The ADE7880 signals the end of the transition period by triggering the $\overline{\text{IRQ1}}$ interrupt pin low and setting Bit 15 (RSTDONE) in the STATUS1 register to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned high by writing to the STATUS1 register with the corresponding bit set to 1.

After a hardware reset, the DSP is in idle mode, which means it does not execute any instruction.

Because the I²C port is the default serial port of the ADE7880, it becomes active after a reset state. If SPI is the port used by the external microprocessor, the procedure to enable it must be repeated immediately after the $\overline{\text{RESET}}$ pin is toggled back to high (see the Serial Interfaces section for details).

At this point, it is recommended to initialize all of the ADE7880 registers and then write 0x0001 into the Run register to start the DSP. See the Digital Signal Processor section for details on the Run register.

SOFTWARE RESET FUNCTIONALITY

Bit 7 (SWRST) in the CONFIG register manages the software reset functionality in PSM0 mode. The default value of this bit is 0. If this bit is set to 1, then the ADE7880 enters the software reset state. In this state, almost all internal registers are set to their default values. In addition, the choice of which serial port, I²C or SPI, is in use remains unchanged if the lock-in procedure has been executed previously (see the Serial Interfaces section for details). The registers that maintain their values despite the SWRST bit being set to 1 are the CONFIG2 and LPOILVL registers. When the software reset ends, Bit 7 (SWRST) in the CONFIG register is cleared to 0, the $\overline{\text{IRQ1}}$ interrupt pin is set low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1. This bit is 0 during the transition period and becomes 1 when the transition ends. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

After a software reset ends, the DSP is in idle mode, which means it does not execute any instruction. As a good programming practice, it is recommended to initialize all the ADE7880 registers and then write 0x0001 into the Run register to start the DSP (see the Digital Signal Processor section for details on the Run register).

Software reset functionality is not available in PSM1, PSM2, or PSM3 mode.

THEORY OF OPERATION

ANALOG INPUTS

The ADE7880 has seven analog inputs forming current and voltage channels. The current channels consist of four pairs of fully differential voltage inputs: IAP and IAN, IBP and IBN, ICP and ICN, and INP and INN. These voltage input pairs have a maximum differential signal of ±0.5 V.

The maximum signal level on analog inputs for the IxP/IxN pair is also ±0.5 V with respect to AGND. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 36 presents a schematic of the input for the current channels and their relation to the maximum common-mode voltage.

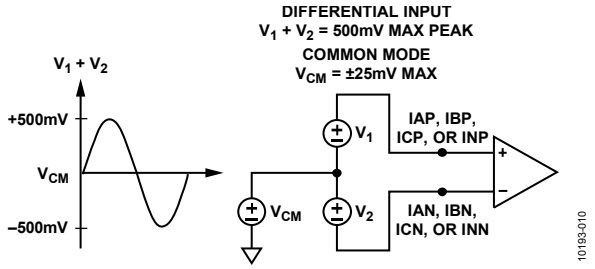

Figure 36. Maximum Input Level, Current Channels, Gain = 1

All inputs have a programmable gain amplifier (PGA) with a possible gain selection of 1, 2, 4, 8, or 16. The gain of IA, IB, and IC inputs is set in Bits[2:0] (PGA1[2:0]) of the Gain register. The gain of the IN input is set in Bits[5:3] (PGA2[2:0]) of the Gain register; thus, a different gain from the IA, IB, or IC inputs is possible. See Table 43 for details on the Gain register.

The voltage channel has three single-ended voltage inputs: VAP, VBP, and VCP. These single-ended voltage inputs have a maximum input voltage of ±0.5 V with respect to VN. The maximum signal level on analog inputs for VxP and VN is also ±0.5 V with respect to AGND. The maximum common-mode signal allowed on the inputs is ±25 mV. Figure 37 presents a schematic of the voltage channels inputs and their relation to the maximum common-mode voltage.

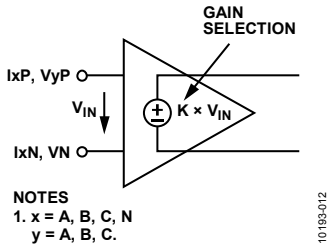

Figure 37. Maximum Input Level, Voltage Channels, Gain = 1

All inputs have a programmable gain with a possible gain selection of 1, 2, 4, 8, or 16. To set the gain, use Bits[8:6] (PGA3[2:0]) in the Gain register (see Table 43).

Figure 38 shows how the gain selection from the Gain register works in both current and voltage channels.

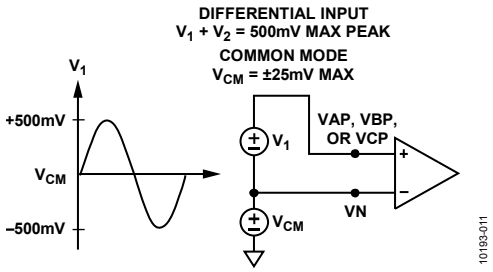

Figure 38. PGA in Current and Voltage Channels

ANALOG-TO-DIGITAL CONVERSION

The ADE7880 has seven sigma-delta (Σ-Δ) analog-to-digital converters (ADCs). In PSM0 mode, all ADCs are active. In PSM1 mode, only the ADCs that measure the Phase A, Phase B, and Phase C currents are active. The ADCs that measure the neutral current and the A, B, and C phase voltages are turned off. In PSM2 and PSM3 modes, the ADCs are powered down to minimize power consumption.

For simplicity, the block diagram in Figure 39 shows a first-order Σ-Δ ADC. The converter is composed of the Σ-Δ modulator and the digital low-pass filter.

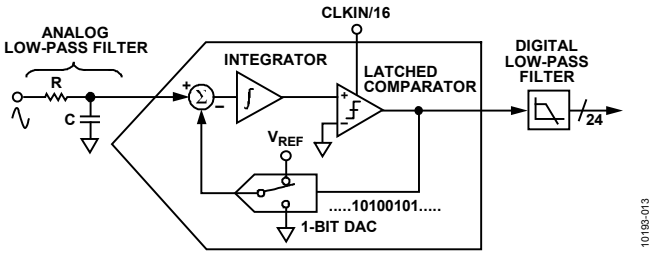

Figure 39. First-Order Σ-Δ ADC

A Σ-Δ modulator converts the input signal into a continuous serial stream of 1s and 0s at a rate determined by the sampling clock. In the ADE7880, the sampling clock is equal to 1.024 MHz (CLKIN/16). The 1-bit DAC in the feedback loop is driven by the serial data stream. The DAC output is subtracted from the input signal. If the loop gain is high enough, the average value of the DAC output (and, therefore, the bit stream) can approach that of the input signal level. For any given input value in a single sampling interval, the data from the 1-bit ADC is virtually meaningless. Only when a large number of samples are averaged is a meaningful result obtained. This averaging is carried out in the second part of the ADC, the digital low-pass filter. By averaging a large number of bits from the modulator, the low-pass filter can produce 24-bit data-words that are proportional to the input signal level.

The Σ-Δ converter uses two techniques to achieve high resolution from what is essentially a 1-bit conversion technique. The first is oversampling. Oversampling means that the signal is sampled at a rate (frequency) that is many times higher than the bandwidth of interest. For example, the sampling rate in the ADE7880 is 1.024 MHz, and the bandwidth of interest is 40 Hz to 3.3 kHz. Oversampling has the effect of spreading the quantization noise (noise due to sampling) over a wider bandwidth. With the noise spread more thinly over a wider bandwidth, the quantization noise in the band of interest is lowered, as shown in Figure 40. However, oversampling alone is not efficient enough to improve the signal-to-noise ratio (SNR) in the band of interest. For example, an oversampling factor of 4 is required just to increase the SNR by a mere 6 dB (1 bit). To keep the oversampling ratio at a reasonable level, it is possible to shape the quantization noise so that the majority of the noise lies at the higher frequencies. In the Σ-Δ modulator, the noise is shaped by the integrator, which has a high-pass-type response for the quantization noise. This is the second technique used to achieve high resolution. The result is that most of the noise is at the higher frequencies where it can be removed by the digital low-pass filter. This noise shaping is shown in Figure 40.

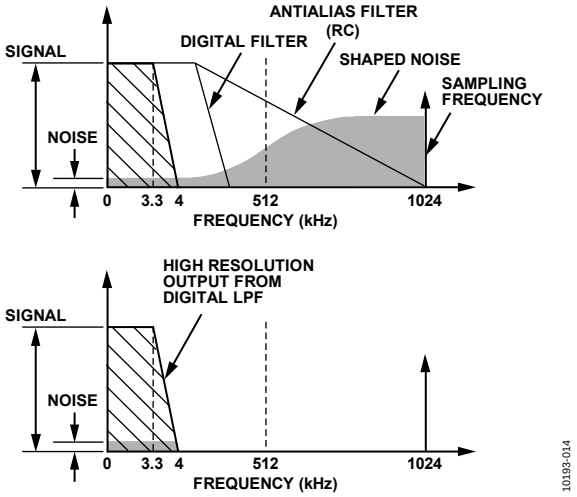

Figure 40. Noise Reduction Due to Oversampling and Noise Shaping in the Analog Modulator

Antialiasing Filter

Figure 39 also shows an analog low-pass filter (RC) on the input to the ADC. This filter is placed outside the ADE7880, and its role is to prevent aliasing. Aliasing is an artifact of all sampled systems as shown in Figure 41. Aliasing means that frequency components in the input signal to the ADC, which are higher than half the sampling rate of the ADC, appear in the sampled signal at a frequency below half the sampling rate. Frequency components above half the sampling frequency (also known as the Nyquist frequency, that is, 512 kHz) are imaged or folded back down below 512 kHz. This happens with all ADCs regardless of the architecture. In the example shown, only frequencies near the sampling frequency, that is, 1.024 MHz, move into the band of interest for metering, that is, 40 Hz to 3.3 kHz. To attenuate the high frequency (near 1.024 MHz) noise and prevent the distortion of the band of interest, a low-pass filter (LPF) must be introduced. For conventional current sensors, it is recommended to use one RC filter with a corner frequency of 5 kHz for the attenuation to be sufficiently high at the sampling frequency of 1.024 MHz. The 20 dB per decade attenuation of this filter is usually sufficient to eliminate the effects of aliasing for conventional current sensors. However, for a di/dt sensor such as a Rogowski coil, the sensor has a 20 dB per decade gain. This neutralizes the 20 dB per decade attenuation produced by the LPF. Therefore, when using a di/dt sensor, take care to offset the 20 dB per decade gain. One simple approach is to cascade one additional RC filter, thereby producing a −40 dB per decade attenuation.

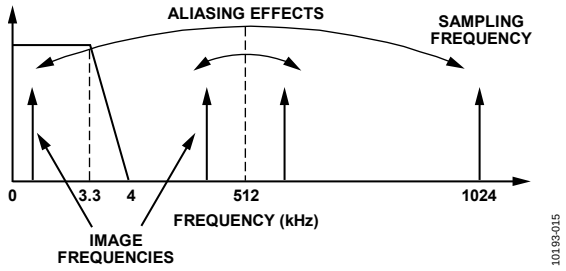

Figure 41. Aliasing Effects

ADC Transfer Function

All ADCs in the ADE7880 are designed to produce the same 24-bit signed output code for the same input signal level. With a full-scale input signal of 0.5 V and an internal reference of 1.2 V, the ADC output code is nominally 5,326,737 (0x514791) and usually varies for each ADE7880 around this value. The code from the ADC can vary between 0x800000 (−8,388,608) and 0x7FFFFF (+8,388,607); this is equivalent to an input signal level of ±0.787 V. However, for specified performance, do not exceed the nominal range of ±0.5 V; ADC performance is guaranteed only for input signals lower than ±0.5 V.

CURRENT CHANNEL ADC

Figure 42 shows the ADC and signal processing path for Input IA of the current channels (it is the same for IB and IC). The ADC outputs are signed twos complement 24-bit data-words and are available at a rate of 8 kSPS (thousand samples per second). With the specified full-scale analog input signal of ±0.5V, the ADC produces its maximum output code value. Figure 42 shows a full-scale voltage signal applied to the differential inputs (IAP and IAN). The ADC output swings between −5,326,737 (0xAEB86F) and +5,326,737 (0x514791). Note that these are nominal values and every ADE7880 varies around these values. The input, IN, corresponds to the neutral current of a 3-phase system. If no neutral line is present, connect this input to AGND. The data path of the neutral current is similar to the path of the phase currents as shown in Figure 43.

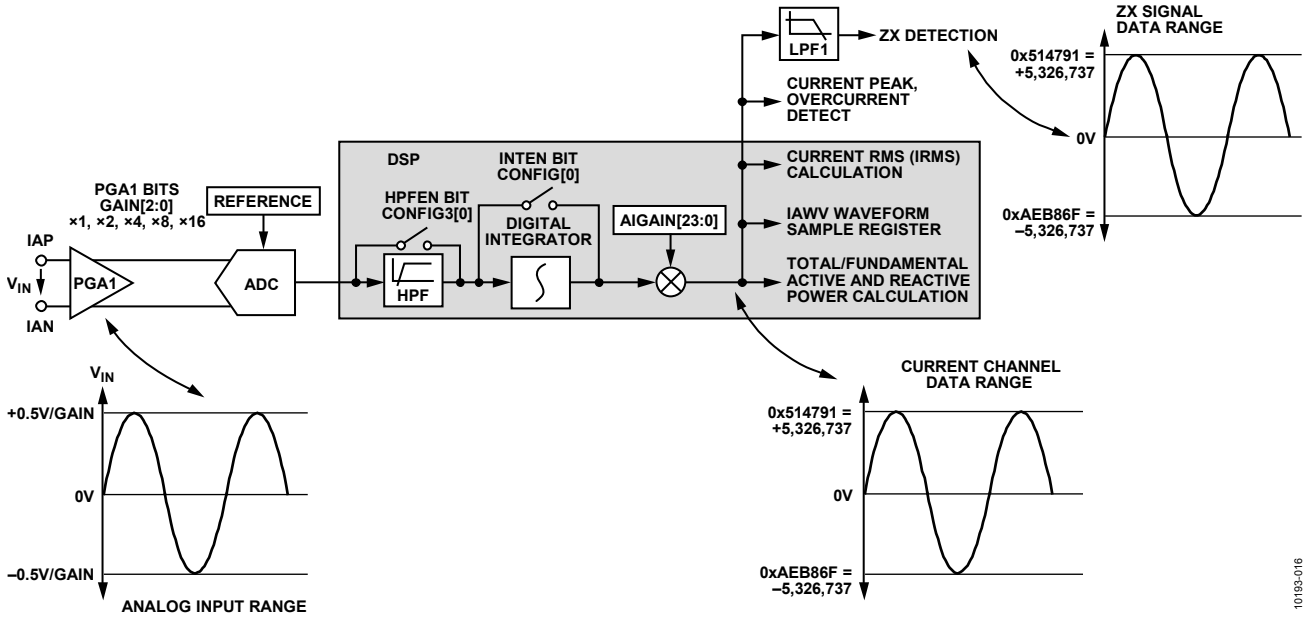

Figure 42. Current Channel Signal Path

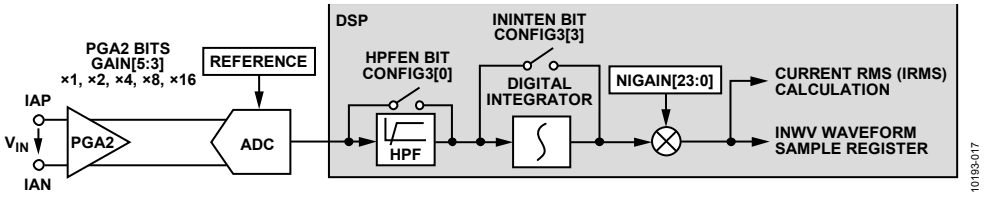

Figure 43. Neutral Current Signal Path

Current Waveform Gain Registers

There is a multiplier in the signal path of each phase and neutral current. The current waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed current waveform gain registers (AIGAIN, BIGAIN, CIGAIN, and NIGAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 4 describes mathematically the function of the current waveform gain registers.

$$Current\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Current\ Gain\ Register}{2^{23}}\right) \quad (4)$$

Changing the content of the AIGAIN, BIGAIN, CIGAIN, or INGAIN registers affects all calculations based on its current; that is, it affects the corresponding phase active/reactive/apparent energy and current rms calculation. In addition, waveform samples scale accordingly.

Note that the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. The 24-bit AIGAIN, BIGAIN, CIGAIN, and NIGAIN registers are accessed as 32-bit registers with the four most significant bits (MSBs) padded with 0s and sign extended to 28 bits. See Figure 44 for details.

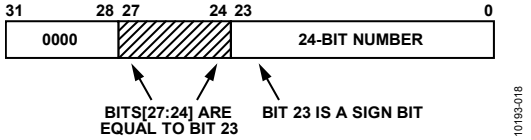

Figure 44. 24-Bit xIGAIN Transmitted as 32-Bit Words

Current Channel HPF

The ADC outputs can contain a dc offset. This offset can create errors in power and rms calculations. High-pass filters (HPFs) are placed in the signal path of the phase and neutral currents and of the phase voltages. If enabled, the HPF eliminates any dc offset on the current channel. All filters are implemented in the DSP and, by default, they are all enabled: Bit 0 (HPFEN) of the CONFIG3[7:0] register is set to 1. All filters are disabled by setting Bit 0 (HPFEN) to 0.

Current Channel Sampling

The waveform samples of the current channel are taken at the output of HPF and stored in the 24-bit signed registers, IAWV, IBWV, ICWV, and INWV at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the IAWV, IBWV, ICWV, and INWV registers are available to be read using the I²C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. When the IAWV, IBWV, ICWV, and INWV 24-bit signed registers are read from the ADE7880, they are transmitted sign extended to 32 bits. See Figure 45 for details.

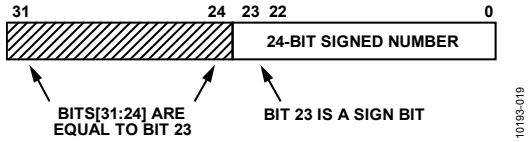

Figure 45. 24-Bit IxWV Register Transmitted as 32-Bit Signed Word

The ADE7880 contains a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

di/dt CURRENT SENSOR AND DIGITAL INTEGRATOR

The di/dt sensor detects changes in the magnetic field caused by the ac current. Figure 46 shows the principle of a di/dt current sensor.

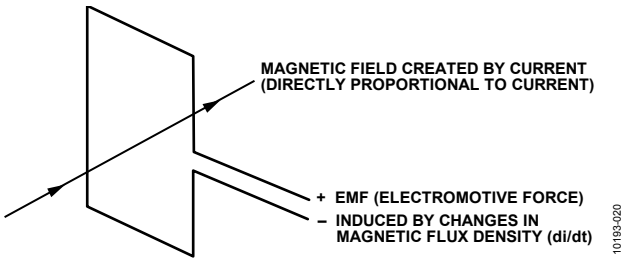

Figure 46. Principle of a di/dt Current Sensor

The flux density of a magnetic field induced by a current is directly proportional to the magnitude of the current. The changes in the magnetic flux density passing through a conductor loop generate an electromotive force (EMF) between the two ends of the loop. The EMF is a voltage signal that is proportional to the di/dt of the current. The voltage output from the di/dt current sensor is determined by the mutual inductance between the current carrying conductor and the di/dt sensor.

Due to the di/dt sensor, the current signal needs to be filtered before it can be used for power measurement. On each phase and neutral current data path, there are built-in digital integrators to recover the current signal from the di/dt sensor. The digital integrators placed on the phase currents data paths are independent of the digital integrator placed in the neutral current data path. This allows for using a different current sensor to measure the neutral current (for example a current transformer) from the current sensors used to measure the phase currents (for example di/dt sensors). The digital integrators are managed by Bit 0 (INTEN) of the CONFIG register and by Bit 3 (ININTEN) of the CONFIG3 register. Bit 0 (INTEN) of the CONFIG register manages the integrators in the phase current channels. Bit 3 (ININTEN) of the CONFIG3 register manages the integrator in the neutral current channel. When the INTEN bit is 0 (default), all integrators in the phase current channels are disabled. When INTEN bit is 1, the integrators in the phase currents data paths are enabled. When the ININTEN bit is 0 (default), the integrator in the neutral current channel is disabled. When the ININTEN bit is 1, the integrator in the neutral current channel is enabled.

Figure 47 and Figure 48 show the magnitude and phase response of the digital integrator.

Note that the integrator has a −20 dB/dec attenuation and approximately −90° phase shift. When combined with a di/dt sensor, the resulting magnitude and phase response is a flat gain over the frequency band of interest. However, the di/dt sensor has a 20 dB/dec gain associated with it and generates significant high frequency noise. At least a second order antialiasing filter is needed to avoid noise aliasing back in the band of interest when the ADC is sampling (see the Antialiasing Filter section).

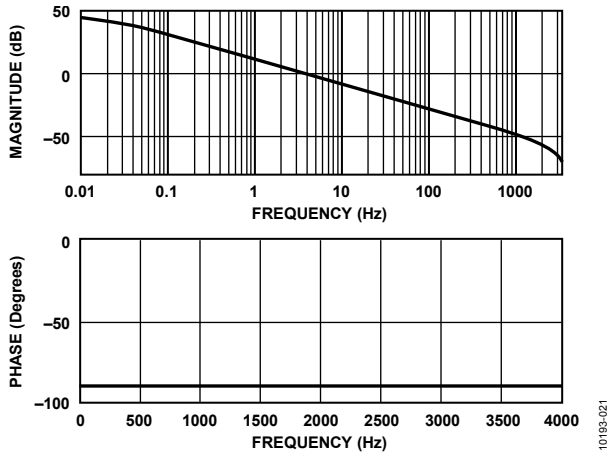

Figure 47. Combined Gain and Phase Response of the Digital Integrator

The DICOEFF 24-bit signed register is used in the digital integrator algorithm. At power-up or after a reset, its value is 0x000000. Before turning on the integrator, this register must be initialized with 0xFFF8000. DICOEFF is not used when the integrator is turned off and can remain at 0x000000 in that case.

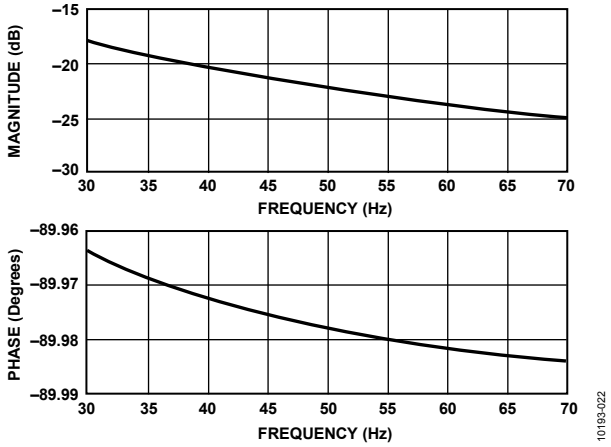

Figure 48. Combined Gain and Phase Response of the Digital Integrator (30 Hz to 70 Hz) when DICOEFF is Set to 0x00000000

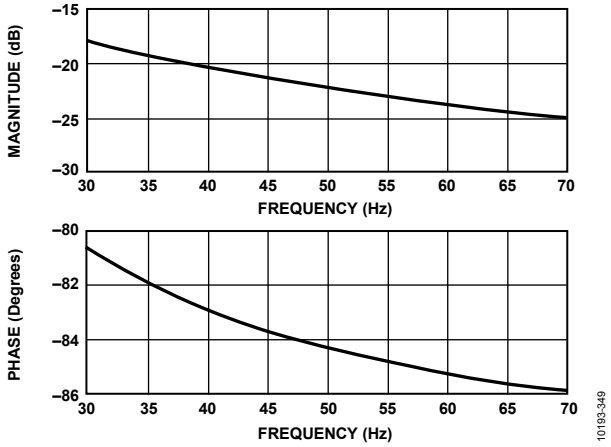

Figure 49. Combined Gain and Phase Response of the Digital Integrator (30 Hz to 70 Hz) when DICOEFF is Set to 0x0FFF8000

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to the registers shown in Figure 44, the DICOEFF 24-bit signed register is accessed as a 32-bit register with four MSBs padded with 0s and sign extended to 28 bits, which practically means it is transmitted equal to 0x0FFF8000.

When the digital integrator is switched off, the ADE7880 can be used directly with a conventional current sensor, such as a current transformer (CT).

VOLTAGE CHANNEL ADC

Figure 50 shows the ADC and signal processing chain for Input VA in the voltage channel. The VB and VC channels have similar processing chains. The ADC outputs are signed twos complement 24-bit words and are available at a rate of 8 kSPS. With the specified full-scale analog input signal of ±0.5 V, the ADC produces its maximum output code value. Figure 50 shows a full-scale voltage signal being applied to the differential inputs (VA and VN). The ADC output swings between −5,326,737 (0xAEB86F) and +5,326,737 (0x514791). Note these are nominal values and every ADE7880 varies around these values.

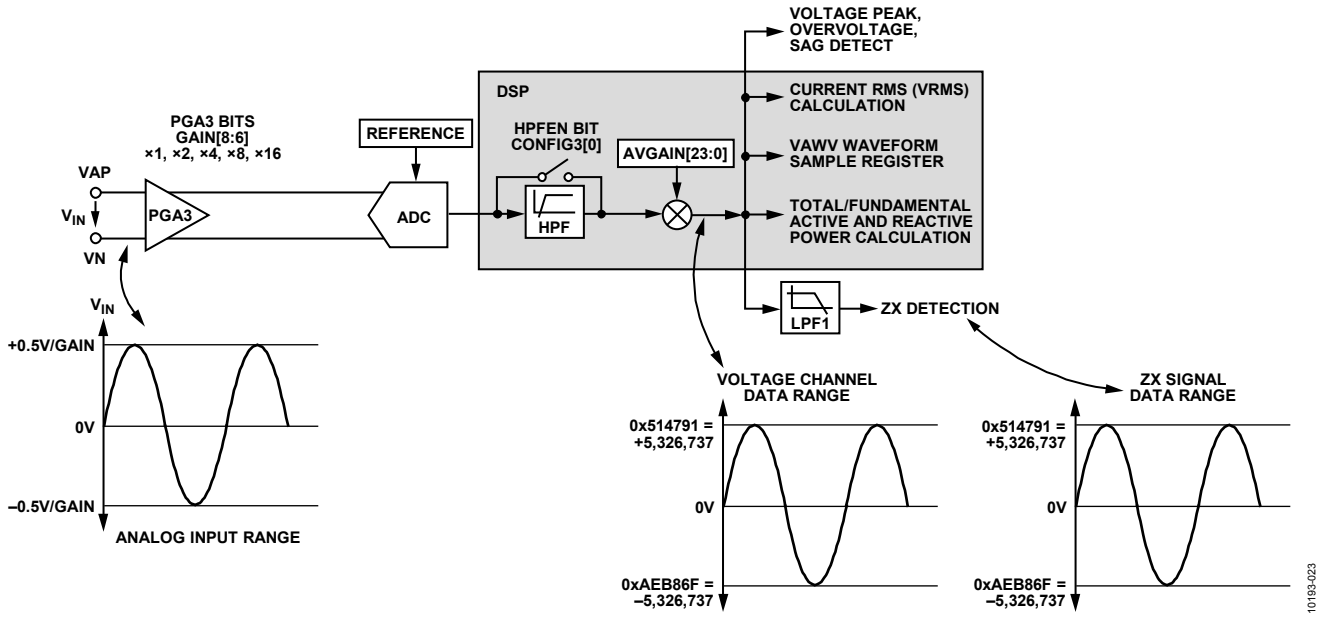

Figure 50. Voltage Channel Data Path

Voltage Waveform Gain Registers

There is a multiplier in the signal path of each phase voltage. The voltage waveform can be changed by ±100% by writing a corresponding twos complement number to the 24-bit signed voltage waveform gain registers (AVGAIN, BVGAIN, and CVGAIN). For example, if 0x400000 is written to those registers, the ADC output is scaled up by 50%. To scale the input by −50%, write 0xC00000 to the registers. Equation 5 describes mathematically the function of the current waveform gain registers.

$$Voltage\ Waveform = ADC\ Output \times \left(1 + \frac{Content\ of\ Voltage\ Gain\ Register}{2^{23}}\right) \quad (5)$$

Changing the content of the AVGAIN, BVGAIN, and CVGAIN registers affects all calculations based on its voltage; that is, it affects the corresponding phase active/reactive/apparent energy and voltage rms calculation. In addition, waveform samples are scaled accordingly.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. As presented in Figure 44, the AVGAIN, BVGAIN, and CVGAIN registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Voltage Channel HPF

As explained in the Current Channel HPF section, the ADC outputs can contain a dc offset that can create errors in power and rms calculations. HPFs are placed in the signal path of the phase voltages, similar to the ones in the current channels. Bit 0 (HPFEN) of CONFIG3 register can enable or disable the filters. See the Current Channel HPF section for more details.

Voltage Channel Sampling

The waveform samples of the voltage channel are taken at the output of HPF and stored into VAWV, VBWV, and VCWV 24-bit signed registers at a rate of 8 kSPS. All power and rms calculations remain uninterrupted during this process. Bit 17 (DREADY) in the STATUS0 register is set when the VAWV, VBWV, and VCWV registers are available to be read using the I²C or SPI serial port. Setting Bit 17 (DREADY) in the MASK0 register enables an interrupt to be set when the DREADY flag is set. See the Digital Signal Processor section for more details on Bit DREADY.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to registers presented in Figure 45, the VAWV, VBWV, and VCWV 24-bit signed registers are transmitted sign extended to 32 bits.

The ADE7880 contains an HSDC port especially designed to provide fast access to the waveform sample registers. See the HSDC Interface section for more details.

CHANGING PHASE VOLTAGE DATA PATH

The ADE7880 can direct one phase voltage input to the computational data path of another phase. For example, Phase A voltage can be introduced in the Phase B computational data path, which means all powers computed by the ADE7880 in Phase B are based on Phase A voltage and Phase B current.

Bits[9:8] (VTOIA[1:0]) of the CONFIG register manage which phase voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 00 (default value), the Phase A voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 01, the Phase B voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 10, the Phase C voltage is directed to the Phase A computational data path. If VTOIA[1:0] = 11, the ADE7880 behaves as if VTOIA[1:0] = 00.

Bits[11:10] (VTOIB[1:0]) of the CONFIG register manage which phase voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 00 (default value), the Phase B voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 01, the Phase C voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 10, the Phase A voltage is directed to the Phase B computational data path. If VTOIB[1:0] = 11, the ADE7880 behaves as if VTOIB[1:0] = 00.

Bits[13:12] (VTOIC[1:0]) of the CONFIG register manage which phase voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 00 (default value), the Phase C voltage is directed to the Phase C computational data path, if VTOIC[1:0] = 01, the Phase A voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 10, the Phase B voltage is directed to the Phase C computational data path. If VTOIC[1:0] = 11, the ADE7880 behaves as if VTOIC[1:0] = 00.

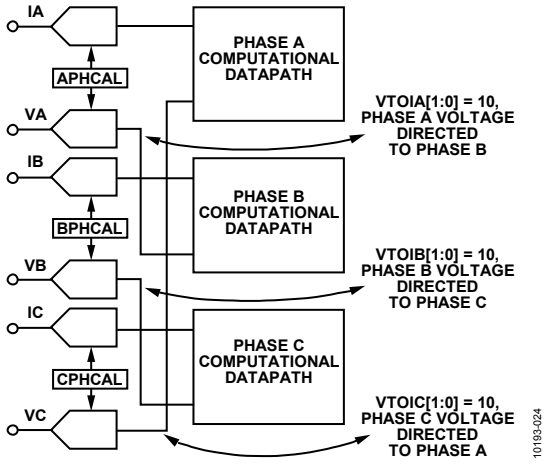

Figure 51. Phase Voltages Used in Different Data Paths

Figure 51 presents the case in which the Phase A voltage is used in the Phase B data path, the Phase B voltage is used in the Phase C data path, and the Phase C voltage is used in the Phase A data path.

POWER QUALITY MEASUREMENTS

Zero-Crossing Detection

The ADE7880 has a zero-crossing (ZX) detection circuit on the phase current and voltage channels. The neutral current data path does not contain a zero-crossing detection circuit. Zero-crossing events are used as a time base for various power quality measurements and in the calibration process.

The output of LPF1 is used to generate zero crossing events. The low-pass filter is intended to eliminate all harmonics of 50 Hz and 60 Hz systems, and to help identify the zero-crossing events on the fundamental components of both current and voltage channels.

The digital filter has a pole at 80 Hz and is clocked at 256 kHz. As a result, there is a phase lag between the analog input signal (one of IA, IB, IC, VA, VB, and VC) and the output of LPF1. The error in ZX detection is 0.0703° for 50 Hz systems (0.0843° for 60 Hz systems). The phase lag response of LPF1 results in a time delay of approximately 31.4° or 1.74 ms (at 50 Hz) between its input and output. The overall delay between the zero crossing on the analog inputs and ZX detection obtained after LPF1 is about 39.6° or 2.2 ms (at 50 Hz). The ADC and HPF introduce the additional delay. The LPF1 cannot be disabled to assure a good resolution of the ZX detection. Figure 52 shows how the zero-crossing signal is detected.

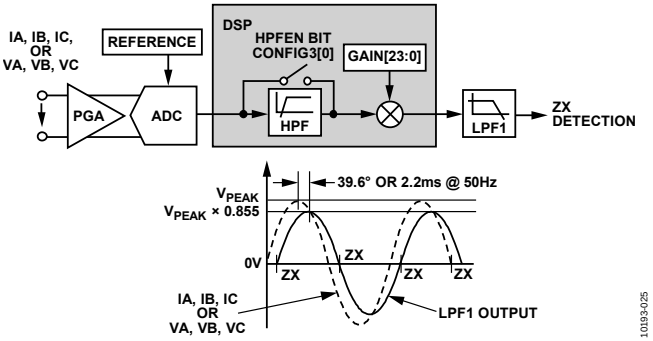

Figure 52. Zero-Crossing Detection on Voltage and Current Channels

To provide further protection from noise, input signals to the voltage channel with amplitude lower than 10% of full scale do not generate zero-crossing events at all. The Current Channel ZX detection circuit is active for all input signals independent of their amplitudes.

The ADE7880 contains six zero-crossing detection circuits, one for each phase voltage and current channel. Each circuit drives one flag in the STATUS1 register. If a circuit placed in the Phase A voltage channel detects one zero-crossing event, Bit 9 (ZXVA) in the STATUS1 register is set to 1.

Similarly, the Phase B voltage circuit drives Bit 10 (ZXVB), the Phase C voltage circuit drives Bit 11 (ZXVC), and circuits placed in the current channel drive Bit 12 (ZXIA), Bit 13 (ZXIB), and Bit 14 (ZXIC) in the STATUS1 register. If a ZX detection bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the corresponding status flag is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

Zero-Crossing Timeout

Every zero-crossing detection circuit has an associated timeout register. This register is loaded with the value written into the 16-bit ZXTOUT register and is decremented (1 LSB) every 62.5 µs (16 kHz clock). The register is reset to the ZXTOUT value every time a zero crossing is detected. The default value of this register is 0xFFFF. If the timeout register decrements to 0 before a zero crossing is detected, one of Bits[8:3] of the STATUS1 register is set to 1. Bit 3 (ZXTOVA), Bit 4 (ZXTOVB), and Bit 5 (ZXTOVC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the voltage channel; Bit 6 (ZXTOIA), Bit 7 (ZXTOIB), and Bit 8 (ZXTOIC) in the STATUS1 register refer to Phase A, Phase B, and Phase C of the current channel.

If a ZXTOIx or ZXTOVx bit is set in the MASK1 register, the $\overline{\text{IRQ1}}$ interrupt pin is driven low when the corresponding status bit is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

The resolution of the ZXOUT register is 62.5 µs (16 kHz clock) per LSB. Thus, the maximum timeout period for an interrupt is 4.096 sec: 2^{16}/16 kHz.

Figure 53 shows the mechanism of the zero-crossing timeout detection when the voltage or the current signal stays at a fixed dc level for more than 62.5 µs × ZXTOUT µs.

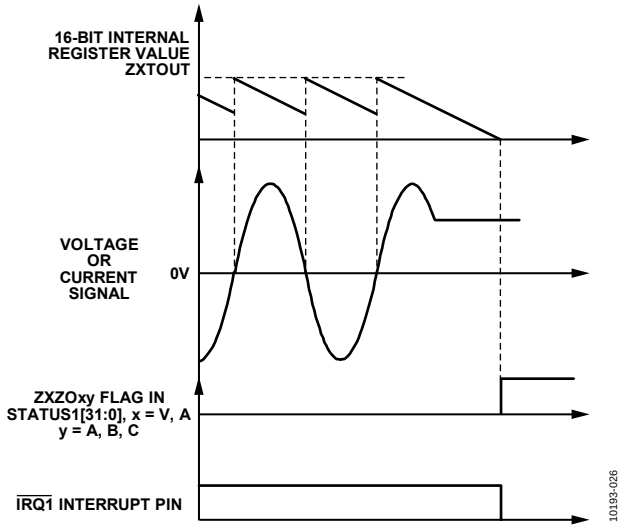

Figure 53. Zero-Crossing Timeout Detection

Phase Sequence Detection

The ADE7880 has on-chip phase sequence error detection circuits. This detection works on phase voltages and considers only the zero crossings determined by their negative-to-positive transitions. The regular succession of these zero-crossing events is Phase A followed by Phase B followed by Phase C (see Figure 55). If the sequence of zero-crossing events is, instead, Phase A followed by Phase C followed by Phase B, then Bit 19 (SEQERR) in the STATUS1 register is set.

If Bit 19 (SEQERR) in the MASK1 register is set to 1 and a phase sequence error event is triggered, the $\overline{\text{IRQ1}}$ interrupt pin is driven low. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set high by writing to the STATUS1 register with the Status Bit 19 (SEQERR) set to 1.

The phase sequence error detection circuit is functional only when the ADE7880 is connected in a 3-phase, 4-wire, three voltage sensors configuration (Bits[5:4], CONSEL[1:0] in the ACCMODE register, set to 00). In all other configurations, only two voltage sensors are used; therefore, it is not recommended to use the detection circuit. In these cases, use the time intervals between phase voltages to analyze the phase sequence (see the Time Interval Between Phases section for details).

Figure 54 presents the case in which Phase A voltage is not followed by Phase B voltage but by Phase C voltage. Every time a negative-to-positive zero crossing occurs, Bit 19 (SEQERR) in the STATUS1 register is set to 1 because such zero crossings on Phase C, Phase B, or Phase A cannot come after zero crossings from Phase A, Phase C, or respectively, Phase B zero crossings.

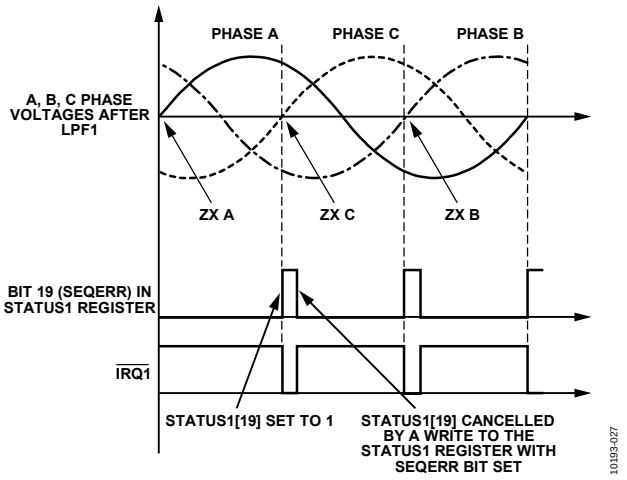

Figure 54. SEQERR Bit Set to 1 When Phase A Voltage Is Followed by Phase C Voltage

Once a phase sequence error is detected, the time measurement between various phase voltages (see the Time Interval Between Phases section) can help to identify which phase to consider with another phase current in the computational data path. Bits[9:8] (VTOIA[1:0]), Bits[11:10] (VTOIB[1:0]), and Bits[13:12] (VTOIC[1:0]) in the CONFIG register can be used to direct one phase voltage to the data path of another phase. See the Changing Phase Voltage Data Path section for details.

Time Interval Between Phases

The ADE7880 has the capability to measure the time delay between phase voltages, between phase currents, or between voltages and currents of the same phase. The negative-to-positive transitions identified by the zero-crossing detection circuit are used as start and stop measuring points. Only one set of such measurements is available at one time, based on Bits[10:9] (ANGLESEL[1:0]) in the COMPMODE register.

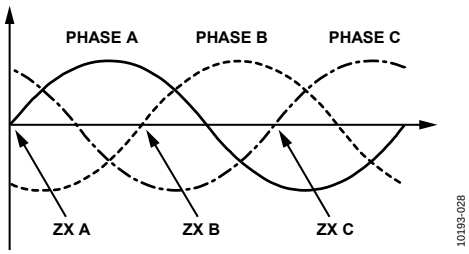

Figure 55. Regular Succession of Phase A, Phase B, and Phase C

When the ANGLESEL[1:0] bits are set to 00, the default value, the delays between voltages and currents on the same phase are measured. The delay between Phase A voltage and Phase A current is stored in the 16-bit unsigned ANGLE0 register (see Figure 56 for details). In a similar way, the delays between voltages and currents on Phase B and Phase C are stored in the ANGLE1 and ANGLE2 registers, respectively.

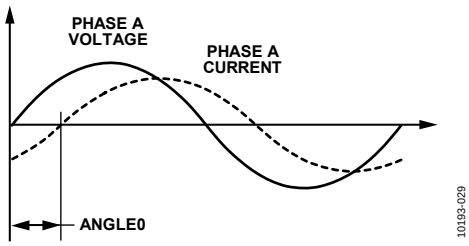

Figure 56. Delay Between Phase A Voltage and Phase A Current Is Stored in the ANGLE0 Register

When the ANGLESEL[1:0] bits are set to 01, the delays between phase voltages are measured. The delay between Phase A voltage and Phase C voltage is stored into the ANGLE0 register. The delay between Phase B voltage and Phase C voltage is stored in the ANGLE1 register, and the delay between Phase A voltage and Phase B voltage is stored in the ANGLE2 register (see Figure 57 for details).

When the ANGLESEL[1:0] bits are set to 10, the delays between phase currents are measured. Similar to delays between phase voltages, the delay between Phase A and Phase C currents is stored into the ANGLE0 register, the delay between Phase B and Phase C currents is stored in the ANGLE1 register, and the delay between Phase A and Phase B currents is stored into the ANGLE2 register (see Figure 57 for details).

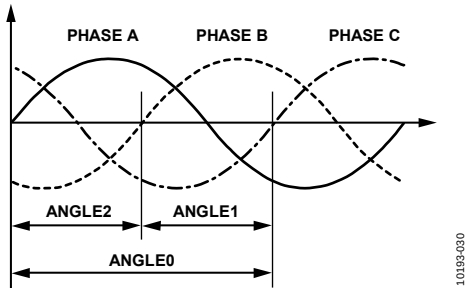

Figure 57. Delays Between Phase Voltages (Currents)

The ANGLE0, ANGLE1, and ANGLE2 registers are 16-bit unsigned registers with 1 LSB corresponding to 3.90625 µs (256 kHz clock), which means a resolution of 0.0703° (360° × 50 Hz/256 kHz) for 50 Hz systems and 0.0843° (360° × 60 Hz/

256 kHz) for 60 Hz systems. The delays between phase voltages or phase currents are used to characterize how balanced the load is. The delays between phase voltages and currents can be used to compute the power factor on each phase, as shown in the following Equation 6:

$$\cos\varphi_x = \cos\left[ANGLEx \times \frac{360^\circ \times f_{LINE}}{256\,\text{kHz}} \right] \quad (6)$$

where f_{LINE} = 50 Hz or 60 Hz.

However, the ADE7880 computes the power factor based on the powers as described in the Power Factor Calculation section.

Period Measurement

The ADE7880 provides the period measurement of the line in the voltage channel. The period of each phase voltage is measured and stored in three different registers, APERIOD, BPERIOD, and CPERIOD. The period registers are 16-bit unsigned registers and update every line period. Because of the LPF1 filter (see Figure 52), a settling time of 30 ms to 40 ms is associated with this filter before the measurement is stable.

The period measurement has a resolution of 3.90625 µs/LSB (256 kHz clock), which represents 0.0195% (50 Hz/256 kHz) when the line frequency is 50 Hz and 0.0234% (60 Hz/256 kHz) when the line frequency is 60 Hz. The value of the period registers for 50 Hz networks is approximately 5120 (256 kHz/50 Hz) and for 60 Hz networks is approximately 4267 (256 kHz/60 Hz). The length of the registers enables the measurement of line frequencies as low as 3.9 Hz (256 kHz/2^{16}). The period registers are stable at ±1 LSB when the line is established and the measurement does not change.

The following equations can be used to compute the line period and frequency using the period registers:

$$T_L = \frac{PERIOD[15:0]}{256\text{E}3}[\text{sec}] \quad (7)$$

$$f_L = \frac{256\text{E}3}{PERIOD[15:0]}[\text{Hz}] \quad (8)$$

Phase Voltage Sag Detection

The ADE7880 can be programmed to detect when the absolute value of any phase voltage drops below or grows above a certain peak value for a number of half-line cycles. The phase where this event takes place and the state of the phase voltage relative to the threshold is identified in Bits[14:12] (VSPHASE[x]) of the PHSTATUS register. An associated interrupt is triggered when any phase drops below or grows above a threshold. This condition is illustrated in Figure 58.

Figure 58 shows Phase A voltage falling below a threshold that is set in the sag level register (SAGLVL) for four half-line cycles (SAGCYC = 4). When Bit 16 (SAG) in the STATUS1 register is set to 1 to indicate the condition, Bit VSPHASE[0] in the PHSTATUS register is also set to 1 because the phase A voltage is below SAGLVL. The microcontroller then writes back STATUS1 register with Bit 16 (SAG) set to 1 to erase the bit and bring $\overline{\text{IRQ1}}$ interrupt pin back high. Then the phase A voltage stays above the SAGLVL threshold for four half-line cycles (SAGCYC = 4). The Bit 16 (SAG) in STATUS1 register is set to 1 to indicate the condition and the bit VSPHASE[0] in the PHSTATUS register is set back to 0.

Bits VSPHASE[1] and VSPHASE[2] relate to the sag events on Phase B and Phase C in the same way: when Phase B or Phase C voltage stays below SAGLVL, they are set to 1. When the phase voltages are above SAGLVL, they are set to 0.

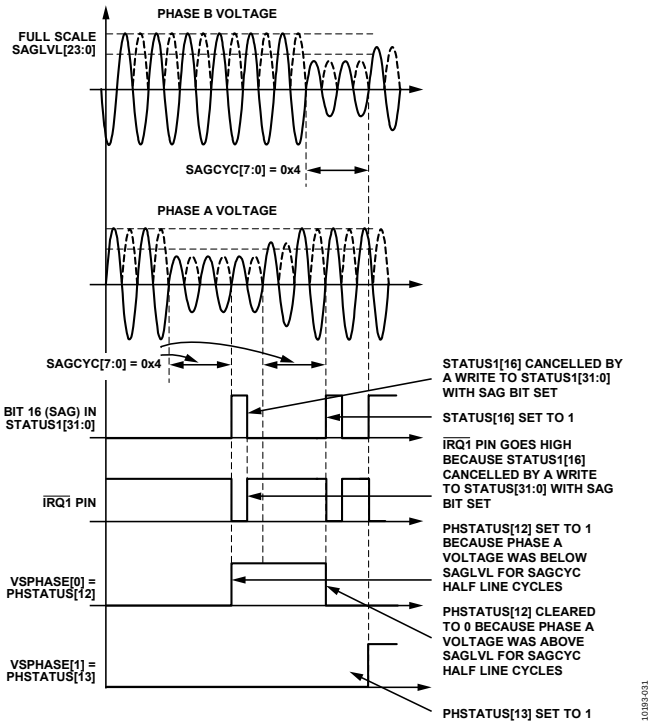

Figure 58. SAG Detection

The SAGCYC register represents the number of half-line cycles the phase voltage must remain below or above the level indicated in the SAGLVL register to trigger a SAG interrupt; 0 is not a valid number for SAGCYC. For example, when the sag cycle (SAGCYC[7:0]) contains 0x07, the SAG flag in the STATUS1 register is set at the end of the seventh half line cycle for which the line voltage falls below the threshold. If Bit 16 (SAG) in MASK1 is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low in case of a sag event in the same moment the Status Bit 16 (SAG) in STATUS1 register is set to 1. The SAG status bit in the STATUS1 register and the $\overline{\text{IRQ1}}$ pin is returned to high by writing to the STATUS1 register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting the SAGLVL register, the first sag detection result is, therefore, not executed across a full SAGCYC period. Writing to the SAGCYC register when the SAGLVL register is already initialized resets the zero-crossing counter, thus ensuring that the first sag detection result is obtained across a full SAGCYC period.

The recommended procedure to manage sag events is the following:

1. Enable sag interrupts in the MASK1 register by setting Bit 16 (SAG) to 1.
2. When a sag event happens, the $\overline{\text{IRQ1}}$ interrupt pin goes low and Bit 16 (SAG) in the STATUS1 is set to 1.
3. The STATUS1 register is read with Bit 16 (SAG) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases a sag event happened.
5. The STATUS1 register is written with Bit 16 (SAG) set to 1. Immediately, the sag bit is erased.

Sag Level Set

The content of the SAGLVL[23:0] sag level register is compared to the absolute value of the output from HPF. Writing 5,326,737 (0x5A7540) to the SAGLVL register puts the SAG detection level at full scale (see the Voltage Channel ADC section), thus; the sag event is triggered continuously. Writing 0x00 or 0x01 puts the sag detection level at 0, therefore, the sag event is never triggered.

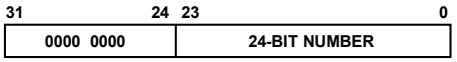

Figure 59. SAGLVL Register Transmitted as a 32-Bit Word

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. The SAGLVL register is accessed as a 32-bit register with eight MSBs padded with 0s. See Figure 59 for details.

Peak Detection

The ADE7880 records the maximum absolute values reached by the voltage and current channels over a certain number of half-line cycles and stores them into the less significant 24 bits of the VPEAK and IPEAK 32-bit registers.

The PEAKCYC register contains the number of half-line cycles used as a time base for the measurement. The circuit uses the zero-crossing points identified by the zero-crossing detection circuit. Bits[4:2] (PEAKSEL[2:0]) in the MMODE register select the phases upon which the peak measurement is performed. Bit 2 selects Phase A, Bit 3 selects Phase B, and Bit 4 selects Phase C. Selecting more than one phase to monitor the peak values decreases proportionally the measurement period indicated in the PEAKCYC register because zero crossings from more phases are involved in the process. When a new peak value is determined, one of Bits[26:24] (IPPHASE[2:0] or VPPHASE[2:0]) in the IPEAK and VPEAK registers is set to 1, identifying the phase that triggered the peak detection event. For example, if a peak value has been identified on Phase A current, Bit 24 (IPPHASE[0]) in the IPEAK register is set to 1. If next time a new peak value is measured on Phase B, Bit 24 (IPPHASE[0]) of the IPEAK register is cleared to 0, and Bit 25 (IPPHASE[1]) of the IPEAK register is set to 1. Figure 60 shows the composition of the IPEAK and VPEAK registers.

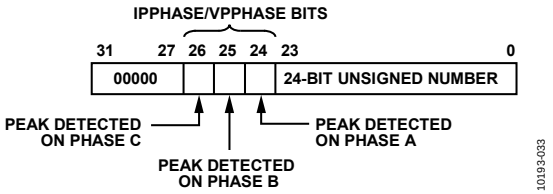

Figure 60. Composition of IPEAK[31:0] and VPEAK[31:0] Registers

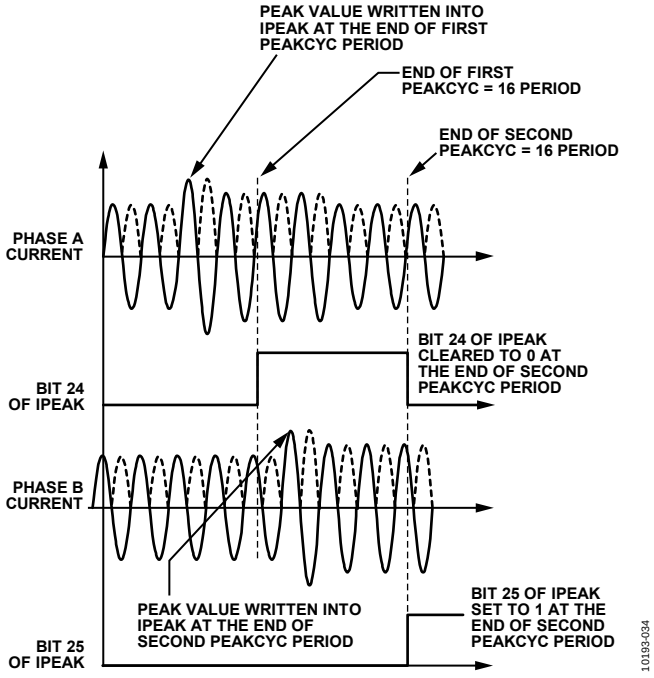

Figure 61. Peak Level Detection

Figure 61 shows how the ADE7880 records the peak value on the current channel when measurements on Phase A and Phase B are enabled (Bit PEAKSEL[2:0] in the MMODE register are 011). PEAKCYC is set to 16, meaning that the peak measurement cycle is four line periods. The maximum absolute value of Phase A is the greatest during the first four line periods (PEAKCYC = 16), so the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 24 (IPPHASE[0]) of the IPEAK register is set to 1 at the end of the period. This bit remains at 1 for the duration of the second PEAKCYC period of four line cycles. The maximum absolute value of Phase B is the greatest during the second PEAKCYC period; therefore, the maximum absolute value is written into the less significant 24 bits of the IPEAK register, and Bit 25 (IPPHASE[1]) in the IPEAK register is set to 1 at the end of the period.

At the end of the peak detection period in the current channel, Bit 23 (PKI) in the STATUS1 register is set to 1. If Bit 23 (PKI) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of the PEAKCYC period, and Status Bit 23 (PKI) in the STATUS1 register is set to 1. In a similar way, at the end of the peak detection period in the voltage channel, Bit 24 (PKV) in the STATUS1 register is set to 1. If Bit 24 (PKV) in the MASK1 register is set, the $\overline{\text{IRQ1}}$ interrupt pin is driven low at the end of PEAKCYC period and Status Bit 24 (PKV) in the STATUS1

register is set to 1. To find the phase that triggered the interrupt, one of either the IPEAK or VPEAK registers is read immediately after reading the STATUS1 register. Next, the status bits are cleared, and the IRQ1 pin is set to high by writing to the STATUS1 register with the status bit set to 1.

Note that the internal zero-crossing counter is always active. By setting Bits[4:2] (PEAKSEL[2:0]) in the MMODE register, the first peak detection result is, therefore, not executed across a full PEAKCYC period. Writing to the PEAKCYC register when the PEAKSEL[2:0] bits are set resets the zero-crossing counter, thereby ensuring that the first peak detection result is obtained across a full PEAKCYC period.

Overvoltage and Overcurrent Detection

The ADE7880 detects when the instantaneous absolute value measured on the voltage and current channels becomes greater than the thresholds set in the OVLVL and OILVL 24-bit unsigned registers. If Bit 18 (OV) in the MASK1 register is set, the IRQ1 interrupt pin is driven low in case of an overvoltage event. There are two status flags set when the IRQ1 interrupt pin is driven low: Bit 18 (OV) in the STATUS1 register and one of Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register to identify the phase that generated the overvoltage. The Status Bit 18 (OV) in the STATUS1 register and all Bits[11:9] (OVPHASE[2:0]) in the PHSTATUS register are cleared, and the IRQ1 pin is set to high by writing to the STATUS1 register with the status bit set to 1. Figure 62 presents overvoltage detection in the Phase A voltage.

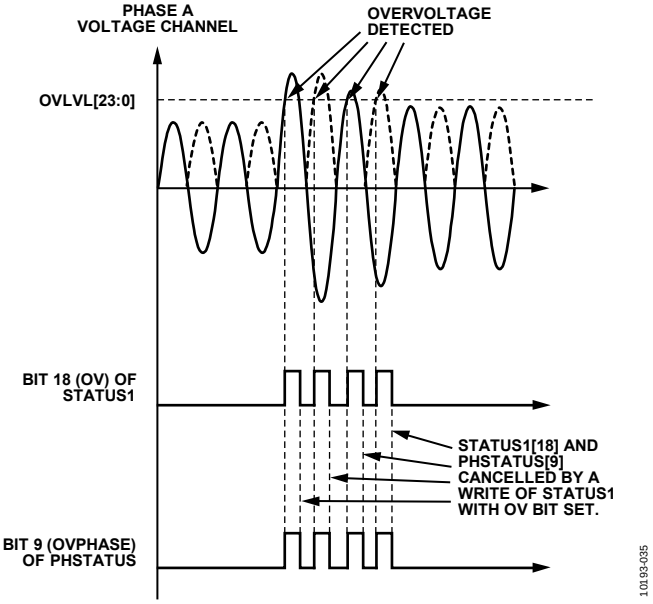

Figure 62. Overvoltage Detection

Whenever the absolute instantaneous value of the voltage goes above the threshold from the OVLVL register, Bit 18 (OV) in the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are set to 1. Bit 18 (OV) of the STATUS1 register and Bit 9 (OVPHASE[0]) in the PHSTATUS register are cancelled when the STATUS1 register is written with Bit 18 (OV) set to 1.

The recommended procedure to manage overvoltage events is the following:

1. Enable OV interrupts in the MASK1 register by setting Bit 18 (OV) to 1.
2. When an overvoltage event happens, the IRQ1 interrupt pin goes low.
3. The STATUS1 register is read with Bit 18 (OV) set to 1.
4. The PHSTATUS register is read, identifying on which phase or phases an overvoltage event happened.
5. The STATUS1 register is written with Bit 18 (OV) set to 1. In this moment, Bit OV is erased and also all Bits[11:9] (OVPHASE[2:0]) of the PHSTATUS register.

In case of an overcurrent event, if Bit 17 (OI) in the MASK1 register is set, the IRQ1 interrupt pin is driven low. Immediately, Bit 17 (OI) in the STATUS1 register and one of Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register, which identify the phase that generated the interrupt, are set. To find the phase that triggered the interrupt, the PHSTATUS register is read immediately after reading the STATUS1 register. Next, Status Bit 17 (OI) in the STATUS1 register and Bits[5:3] (OIPHASE[2:0]) in the PHSTATUS register are cleared and the IRQ1 pin is set to high by writing to the STATUS1 register with the status bit set to 1. The process is similar with overvoltage detection.

Overvoltage and Overcurrent Level Set

The content of the overvoltage (OVLVL), and overcurrent, (OILVL) 24-bit unsigned registers is compared to the absolute value of the voltage and current channels. The maximum value of these registers is the maximum value of the HPF outputs: +5,326,737 (0x514791). When the OVLVL or OILVL register is equal to this value, the overvoltage or overcurrent conditions are never detected. Writing 0x0 to these registers signifies the overvoltage or overcurrent conditions are continuously detected, and the corresponding interrupts are permanently triggered.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 59, OILVL and OVLVL registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

Neutral Current Mismatch

In 3-phase systems, the neutral current is equal to the algebraic sum of the phase currents

$$I_N(t) = I_A(t) + I_B(t) + I_C(t)$$

If there is a mismatch between these two quantities, then a tamper situation may have occurred in the system.

The ADE7880 computes the sum of the phase currents adding the content of the IAWV, IBWV, and ICWV registers, and storing the result into the ISUM 28-bit signed register: $I_{SUM}(t) = I_A(t) + I_B(t) + I_C(t)$. ISUM is computed every 125 µs (8 kHz frequency), the rate at which the current samples are available, and Bit 17 (DREADY) in the STATUS0 register is used to signal when the ISUM register can be read. See the Digital Signal Processor section for more details on Bit DREADY.

To recover $I_{SUM}(t)$ value from the ISUM register, use the following equation:

$$I_{SUM}(t) = \frac{ISUM[27:0]}{ADC_{MAX}} \times I_{FS}$$

where:
ADC_{MAX} = 5,326,737, the ADC output when the input is at full scale.
I_{FS} is the full-scale ADC phase current.

Note that the ADE7880 also computes the rms of ISUM and stores it into NIRMS register when Bit 2 (INSEL) in CONFIG3 register is set to 1 (see Current RMS Calculation section for details).

The ADE7880 computes the difference between the absolute values of ISUM and the neutral current from the INWV register, take its absolute value and compare it against the ISUMLVL threshold.

If

$$\left| |ISUM| - |INWV| \right| \le ISUMLVL ,$$

then it is assumed that the neutral current is equal to the sum of the phase currents, and the system functions correctly.

If

$$\left| |ISUM| - |INWV| \right| > ISUMLVL ,$$

a tamper situation may have occurred, and Bit 20 (MISMTCH) in the STATUS1 register is set to 1. An interrupt attached to the flag can be enabled by setting Bit 20 (MISMTCH) in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low when Status Bit MISMTCH is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back to high by writing to the STATUS1 register with Bit 20 (MISMTCH) set to 1.

If $\left| |ISUM| - |INWV| \right| \le ISUMLVL$, then $MISMTCH = 0$

If $\left| |ISUM| - |INWV| \right| > ISUMLVL$, then $MISMTCH = 1$

ISUMLVL, the positive threshold used in the process, is a 24-bit signed register. Because it is used in a comparison with an absolute value, always set ISUMLVL as a positive number, somewhere between 0x00000 and 0x7FFFFF. ISUMLVL uses the same scale of the current ADCs outputs, so writing +5,326,737 (0x514791) to the ISUMLVL register puts the mismatch detection level at full scale; see the Current Channel ADC section for details. Writing 0x000000, the default value, or a negative value, signifies the MISMTCH event is always triggered. The right value for the application must be written into the ISUMLVL register after power-up or after a hardware/software reset to avoid continuously triggering MISMTCH events.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. As presented in Figure 63, ISUM, the 28-bit signed register, is accessed as a 32-bit register with the four most significant bits padded with 0s.

Figure 63. The ISUM[27:0] Register is Transmitted As a 32-Bit Word

Similar to the registers presented in Figure 44, the ISUMLVL register is accessed as a 32-bit register with four most significant bits padded with 0s and sign extended to 28 bits.

PHASE COMPENSATION

As described in the Current Channel ADC and Voltage Channel ADC sections, the data path for both current and voltages is the same. The phase error between current and voltage signals introduced by the ADE7880 is negligible. However, the ADE7880 must work with transducers that may have inherent phase errors. For example, a current transformer (CT) with a phase error of 0.1° to 3° is not uncommon. These phase errors can vary from part to part, and they must be corrected to perform accurate power calculations.

The errors associated with phase mismatch are particularly noticeable at low power factors. The ADE7880 provides a means of digitally calibrating these small phase errors. The ADE7880 allows a small time delay or time advance to be introduced into the signal processing chain to compensate for the small phase errors.

The phase calibration registers (APHCAL, BPHCAL, and CPHCAL) are 10-bit registers that can vary the time advance in the voltage channel signal path from −374.0 µs to +61.5 µs. Negative values written to the PHCAL registers represent a time advance whereas positive values represent a time delay. One LSB is equivalent to 0.976 µs of time delay or time advance (clock rate of 1.024 MHz). With a line frequency of 60 Hz, this gives a phase resolution of 0.0211° (360° × 60 Hz/1.024 MHz) at the fundamental. This corresponds to a total correction range of −8.079° to +1.329° at 60 Hz. At 50 Hz, the correction range is −6.732° to +1.107° and the resolution is 0.0176° (360° × 50 Hz/1.024 MHz).

Given a phase error of x degrees, measured using the phase voltage as the reference, the corresponding LSBs are computed dividing x by the phase resolution (0.0211°/LSB for 60 Hz and 0.0176°/LSB for 50 Hz). Results between −383 and +63 only are acceptable; numbers outside this range are not accepted. If the current leads the voltage, the result is negative and the absolute value is written into the PHCAL registers. If the current lags the voltage, the result is positive and 512 is added to the result before writing it into xPHCAL.

$$APHCAL, BPHCAL, \text{or } CPHCAL = \begin{cases} \left| \frac{x}{phase_resolution} \right|, x \le 0 \\ \frac{x}{phase_resolution} + 512, x > 0 \end{cases} \quad (9)$$

Figure 65 illustrates how the phase compensation is used to remove x = −1° phase lead in IA of the current channel from the external current transducer (equivalent of 55.5 µs for 50 Hz systems). To cancel the lead (1°) in the current channel of Phase A, a phase lead must be introduced into the corresponding voltage channel. Using Equation 8, APHCAL is 57 least significant bits, rounded up from 56.8. The phase lead is achieved by introducing a time delay of 55.73 µs into the Phase A current.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. As shown in Figure 64, APHCAL, BPHCAL, and CPHCAL 10-bit registers are accessed as 16-bit registers with the six MSBs padded with 0s.

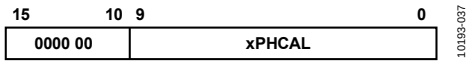

Figure 64. xPHCAL Registers Communicated As 16-Bit Registers

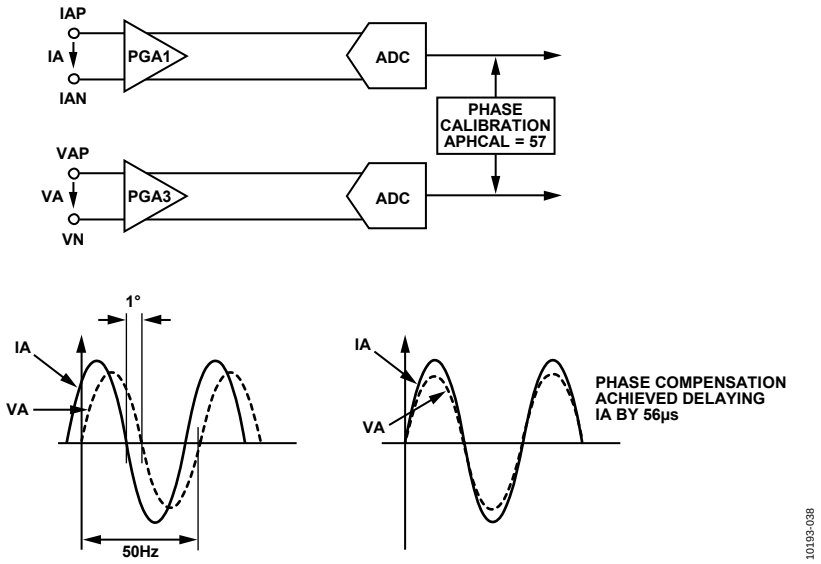

Figure 65. Phase Calibration on Voltage Channels

REFERENCE CIRCUIT

The nominal reference voltage at the $REF_{IN/OUT}$ pin is 1.2 V. This is the reference voltage used for the ADCs in the ADE7880. Use a typical external reference voltage of 1.2 V to overdrive the $REF_{IN/OUT}$ pin. Calculate the temperature coefficient of the internal voltage reference based on the endpoint method. To calculate the drift over temperature, measure and compare the values of the voltage reference at endpoints (−40°C and +85°C) to the reference value at 25°C to obtain the slope of the temperature coefficient curve. Figure 66 is a typical representation of the drift over temperature.

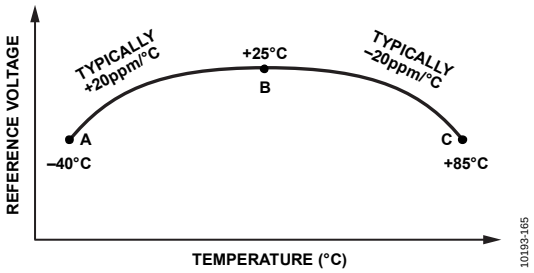

Figure 66. Internal Voltage Reference Temperature Drift

Figure 66 shows that independent consideration of two regions is necessary for accurate analysis of the drift over temperature, as follows:

- Considering the region between Point A and Point B, the reference value increases with increase in temperature; thus, the curve has a positive slope from A to B. This results in a positive temperature coefficient in this region.
- Considering the region between Point B and Point C, the slope of the curve is negative because the voltage reference decreases with an increase in temperature; thus, this region of the curve has a negative temperature coefficient.

The general relationship between the absolute value of the voltage reference at a particular endpoint temperature and the temperature coefficient for that region of the curve is explained by the following two equations:

$$V_{REF\ (-40°C)} = V_{REF\ (+25°C)} \times \left(1 + \frac{\alpha_c(-40°C - 25°C)}{10^6}\right)$$

$$V_{REF\ (85°C)} = V_{REF\ (25°C)} \times \left(1 + \frac{\alpha_h(85°C - 25°C)}{10^6}\right)$$

where αc and αh are cold and hot temperature coefficients, respectively, calculated by:

$$\alpha_c = \frac{\frac{V_{REF(-40°C)} - V_{REF(+25°C)}}{V_{REF(+25°C)}}}{(-40°C - 25°C)} \times 10^6 \text{ ppm/°C}$$

$$\alpha_h = \frac{\frac{V_{REF(85°C)} - V_{REF(25°C)}}{V_{REF(25°C)}}}{(85°C - 25°C)} \times 10^6 \text{ ppm/°C}$$

To find the typical, maximum, and minimum temperature coefficients as listed in the Specifications section, data based on the end-point method is collected on ICs spread out over different lots. Each IC has a temperature coefficient curve that differs slightly from any other, which necessitates the trimming of all devices based on a carefully chosen single voltage reference value. Though the absolute value of the reference voltage at 25°C differs from one device to another in mV range, the drift over temperature in a particular device always remains within the maximum limits, as stated in the Specifications section.

Because the reference is used for all ADCs, any x% drift in the reference results in a 2x% deviation of the meter accuracy. The reference drift resulting from temperature changes is usually very small and, typically, much smaller than the drift of other components on a meter. Alternatively, calibrate the meter at multiple temperatures.

The ADE7880 use the internal voltage reference when Bit 0 (EXTREFEN) in the CONFIG2 register is cleared to 0 (the default value); the external voltage reference is used when the bit is set to 1. Set the CONFIG2 register during the PSM0 mode; its value is maintained during the PSM1, PSM2, and PSM3 power modes.

DIGITAL SIGNAL PROCESSOR

The ADE7880 contains a fixed function digital signal processor (DSP) that computes all powers and rms values. It contains program memory ROM and data memory RAM.

The program used for the power and rms computations is stored in the program memory ROM and the processor executes it every 8 kHz. The end of the computations is signaled by setting Bit 17 (DREADY) to 1 in the STATUS0 register. An interrupt attached to this flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. If enabled, the $\overline{IRQ0}$ pin is set low and Status Bit DREADY is set to 1 at the end of the computations. The status bit is cleared and the $\overline{IRQ0}$ pin is set to high by writing to the STATUS0 register with Bit 17 (DREADY) set to 1.

The registers used by the DSP are located in the data memory RAM, at addresses between 0x4380 and 0x43BE. The width of this memory is 28 bits. A two-stage pipeline is used when write operations to the data memory RAM are executed. This means two things: when only one register needs to be initialized, write it two more times to ensure the value has been written into RAM. When two or more registers need to be initialized, write the last register in the queue two more times to ensure the value is written into RAM.

As explained in the Power-Up Procedure section, at power-up or after a hardware or software reset, the DSP is in idle mode. No instruction is executed. All the registers located in the data memory RAM are initialized at 0, their default values and they can be read/written without any restriction. The Run register, used to start and stop the DSP, is cleared to 0x0000. The Run register needs to be written with 0x0001 for the DSP to start code execution. It is recommended to first initialize all ADE7880 registers located in the data memory RAM with their desired values. Next, write the last register in the queue two additional times to flush the pipeline and then write the Run register with

0x0001. In this way, the DSP starts the computations from a desired configuration.

To protect the integrity of the data stored in the data memory RAM of the DSP (between Address 0x4380 and Address 0x43BE), a write protection mechanism is available. By default, the protection is disabled and registers placed between 0x4380 and 0x43BE can be written without restriction. When the protection is enabled, no writes to these registers are allowed. Registers can be always read, without restriction, independent of the write protection state. To enable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3. To disable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. It is recommended to enable the write protection before starting the DSP. If any data memory RAM based register needs to be changed, simply disable the protection, change the value and then enable back the protection. There is no need to stop the DSP in order to change these registers.

To disable the protection, write 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3.

Use the following procedure to initialize the ADE7880 registers at power-up:

1. Select the PGA gains in the phase currents, voltages, and neutral current channels: Bits [2:0] (PGA1), Bits [5:3] (PGA2) and Bits [8:6] (PGA3) in the Gain register.
2. If Rogowski coils are used, enable the digital integrators in the phase and neutral currents: Bit 0 (INTEN) set to 1 in CONFIG register. Initialize DICOEFF register to 0xFF8000 before setting the INTEN bit in the CONFIG register.
3. If f_n is between 55 Hz and 66 Hz, set Bit 14 (SELFREQ) in COMPMODE register.
4. Initialize all the other data memory RAM registers. Write the last register in the queue three times to ensure that its value is written into the RAM.
5. Initialize WTHR, VARTHR, VATHR, VLEVEL and VNOM registers based on Equation 26, Equation 37, Equation 44, Equation 22, and Equation 42, respectively.
6. Initialize CF1DEN, CF2DEN, and CF3DEN based on Equation 49.
7. Enable the data memory RAM protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
8. Read back all data memory RAM registers to ensure that they initialized with the desired values. In the unlikely case that one or more registers does not initialize correctly, disable the protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. Reinitialize the registers, and write the last register in the queue three times. Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
9. Start the DSP by setting Run = 1.
10. Read the energy registers xWATTHR, xVAHR, xFWATTHR, and xFVARHR to erase their content and start energy accumulation from a known state.
11. Enable the CF1, CF2 and CF3 frequency converter outputs by clearing bits 9, 10 and 11 (CF1DIS, CF2DIS, and CF3DIS) to 0 in CFMODE register.

There is no obvious reason to stop the DSP if the ADE7880 is maintained in PSM0 normal mode. All ADE7880 registers, including ones located in the data memory RAM, can be modified without stopping the DSP. However, to stop the DSP, write 0x0000 into the Run register. To restart the DSP, follow one of the following procedures:

- If the ADE7880 registers located in the data memory RAM have not been modified, write 0x0001 into the Run register to start the DSP.
- If the ADE7880 registers located in the data memory RAM have to be modified, first execute a software or a hardware reset, initialize all ADE7880 registers at desired values, enable the write protection and then write 0x0001 into the Run register to start the DSP.

As mentioned in the Power Management section, when the ADE7880 switch out of PSM0 power mode, it is recommended to stop the DSP by writing 0x0000 into the Run register (see Table 10 and Table 11 for the recommended actions when changing power modes).

ROOT MEAN SQUARE MEASUREMENT

Root mean square (rms) is a measurement of the magnitude of an ac signal. Its definition can be both practical and mathematical. Defined practically, the rms value assigned to an ac signal is the amount of dc required to produce an equivalent amount of power in the load. Mathematically, the rms value of a continuous signal f(t) is defined as

$$F\,rms = \sqrt{\frac{1}{t}\int_0^t f^2(t)dt} \quad (10)$$

For time sampling signals, rms calculation involves squaring the signal, taking the average, and obtaining the square root.

$$F\,rms = \sqrt{\frac{1}{N}\sum_{N=1}^{N} f^2[n]} \quad (11)$$

Equation 10 implies that for signals containing harmonics, the rms calculation contains the contribution of all harmonics, not only the fundamental. The ADE7880 uses two different methods to calculate rms values. The first one is very accurate and is active only in PSM0 mode. The second one is less accurate, uses the estimation of the mean absolute value (mav) measurement, and is active in PSM0 and PSM1 modes.

The ADE7880 also computes the rms values of various fundamental and harmonic components of phase currents, phase voltages and neutral current as part of the harmonic calculations block. Refer to the Harmonics Calculations section for details.

The first method is to low-pass filter the square of the input signal (LPF) and take the square root of the result (see Figure 68).

$$\text{If } f(t) = \sum_{k=1}^{\infty} F_k\sqrt{2}\sin\left(k\omega t + \gamma_k\right) \quad (12)$$

then,

$$f^2(t) = \sum_{k=1}^{\infty} F_k^2 - \sum_{k=1}^{\infty} F_k^2\cos(2k\omega t + 2\gamma_k) + \\ +2\sum_{\substack{k,m=1\\k\neq m}}^{\infty} 2\times F_k\times F_m\sin\left(k\omega t+\gamma_k\right)\times\sin\left(m\omega t+\gamma_m\right) \quad (13)$$

After the LPF and the execution of the square root, the rms value of f(t) is obtained by

$$F = \sqrt{\sum_{k=1}^{\infty} F_k^2} \quad (14)$$

The rms calculation based on this method is simultaneously processed on all seven analog input channels. Each result is available in the 24-bit registers: AIRMS, BIRMS, CIRMS, AVRMS, BVRMS, CVRMS, and NIRMS.

The second method computes the absolute value of the input signal and then filters it to extract its dc component. It computes the absolute mean value of the input. If the input signal in Equation 16 has a fundamental component only, its average value is

$$F_{DC} = \frac{1}{T}\left[\int_0^{\frac{T}{2}}\sqrt{2}\times F_1\times\sin(\omega t)dt - \int_{\frac{T}{2}}^{T}\sqrt{2}\times F_1\times\sin(\omega t)dt\right]$$

$$F_{DC} = \frac{2}{\pi}\times\sqrt{2}\times F_1$$

The calculation based on this method is simultaneously processed only on the three phase currents. Each result is available in the 20-bit registers AIMAV, BMAV, and CMAV. Note that the proportionality between mav and rms values is maintained for the fundamental components only. If harmonics are present in the current channel, the mean absolute value is no longer proportional to rms.

Current RMS Calculation

This section presents the first approach to compute the rms values of all phase and neutral currents. The ADE7880 also computes the rms of the sum of the instantaneous values of the phase currents if Bit 2 (INSEL) in the CONFIG3 register is set to 1. Note that the instantaneous value of the sum is stored into ISUM register presented in the Neutral Current Mismatch section. In 3-phase four wired systems that only require sensing the phase currents, this value provides a measure of the neutral current.

Figure 68 shows the detail of the signal processing chain for the rms calculation on one of the phases of the current channel. The current channel rms value is processed from the samples used in the current channel. The current rms values are signed 24-bit values and they are stored into the AIRMS, BIRMS, CIRMS, NIRMS registers. The update rate of the current rms measurement is 8 kHz. If Bit 2 (INSEL) of the CONFIG3 register is 0 (default), the NIRMS register contains the rms value of the neutral current. If the INSEL bit is 1, the NIRMS register contains the rms value of the sum of the instantaneous values of the phase currents.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,326,737. The equivalent rms value of a full-scale sinusoidal signal is 3,766,572 (0x39792C), independent of the line frequency. If the integrator is enabled, that is, when Bit 0 (INTEN) in the CONFIG register is set to 1, the equivalent rms value of a full-scale sinusoidal signal at 50 Hz is 3,759,718 (0x395E66) and at 60 Hz is 3,133,207 (0x2FCF17).

The accuracy of the current rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input when PGA = 1. Additionally, this measurement has a bandwidth of 3.3 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The IRQ1 interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section). Table 12 shows the settling time for the I rms measurement, which is the time it takes for the rms register to settle within 99.5% of the input to the current channel when starting from 0 to full scale. However, during the IC power-up and DSP reset cases, it typically takes about 1.3 seconds from the moment the RUN register is set to 0x01 for a FS/1000 signal to be 99.5% settled.

Table 12. Settling Time for I rms Measurement

Integrator Status	50 Hz Input Signals	60 Hz Input Signals
Integrator Off	580 ms	580 ms
Integrator On	700 ms	700 ms

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 67, the AIRMS, BIRMS, CIRMS, NIRMS 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

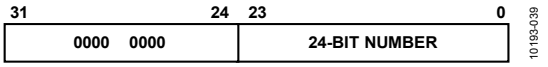

Figure 67. 24-Bit AIRMS, BIRMS, CIRMS and NIRMS Registers Transmitted as 32-Bit Words

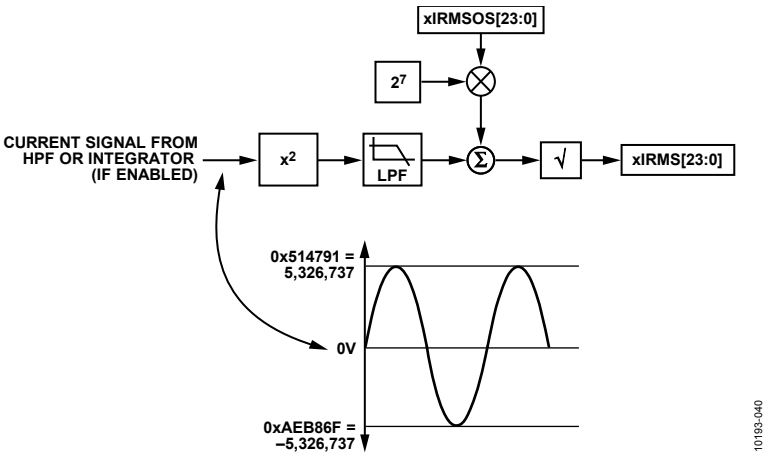

Figure 68. Current RMS Signal Processing

Current RMS Offset Compensation

The ADE7880 incorporates a current rms offset compensation register for each phase: AIRMSOS, BIRMSOS, CIRMSOS, and NIRMSOS. These are 24-bit signed registers that are used to remove offsets in the current rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $i^2(t)$. The current rms offset register is multiplied by 128 and added to the squared current rms before the square root is executed. Assuming that the maximum value from the current rms calculation is 3,766,572 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00045%

$$\left(\sqrt{3767^2 + 128} / 3767 - 1\right) \times 100$$

of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using currents equal to zero for this purpose.

$$I\,rms = \sqrt{I\,rms_0^2 + 128 \times IRMSOS} \quad (15)$$

where $I\,rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the register presented in Figure 44, the AIRMSOS, BIRMSOS, CIRMSOS, and NIRMSOS 24-bit signed registers are accessed as 32-bit registers with four MSBs padded with 0s and sign extended to 28 bits.

Current Mean Absolute Value Calculation

This section presents the second approach to estimate the rms values of all phase currents using the mean absolute value (mav) method. This approach is used in PSM1 mode, to allow energy accumulation based on current rms values when the missing neutral case demonstrates to be a tamper attack. This data path is active also in PSM0 mode to allow for its gain calibration. The gain is used in the external microprocessor during PSM1 mode. The mav value of the neutral current is not computed using this method. Figure 69 shows the details of the signal processing chain for the mav calculation on one of the phases of the current channel.

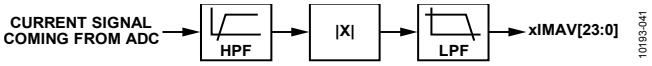

Figure 69. Current MAV Signal Processing for PSM1 Mode

The current channel mav value is processed from the samples used in the current channel waveform sampling mode. The samples are passed through a high-pass filter to eliminate the eventual dc offsets introduced by the ADCs and the absolute values are computed. The outputs of this block are then filtered to obtain the average. The current mav values are unsigned 20-bit values and they are stored in the AIMAV, BIMAV, and CIMAV registers. The update rate of this mav measurement is 8 kHz.

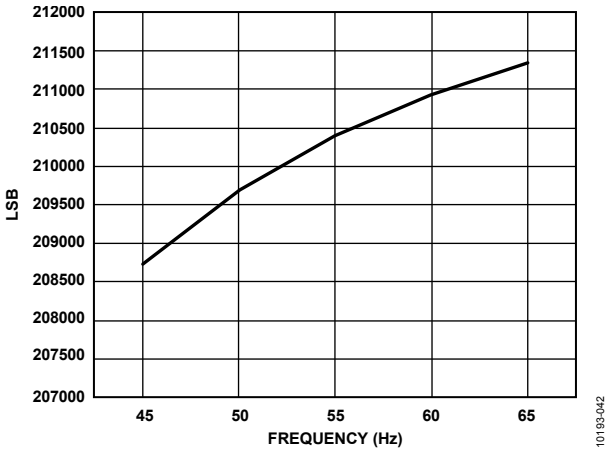

Figure 70. xIMAV Register Values at Full Scale, 45 Hz to 65 Hz Line Frequencies

The mav values of full-scale sinusoidal signals of 50 Hz and 60 Hz are 209,686 and 210,921, respectively. As seen in Figure 70, there is a 1.25% variation between the mav estimate at 45 Hz and the one at 65 Hz for full-scale sinusoidal inputs. The accuracy of the current mav is typically 0.5% error from the full-scale input down to 1/100 of the full-scale input. Additionally, this measurement has a bandwidth of 3.3 kHz. The settling time for the current mav measurement, that is the time it takes for the mav register to reflect the value at the input to the current channel within 0.5% error, is 500 ms. However, during the first measurement after entering this mode, it takes a longer time to settle to the correct value.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. As presented in Figure 71, the AIMAV, BIMAV, and CIMAV 20-bit unsigned registers are accessed as 32-bit registers with the 12 MSBs padded with 0s.

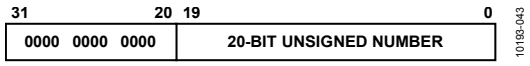

Figure 71. xIMAV Registers Transmitted as 32-Bit Registers

Current MAV Gain and Offset Compensation

The current rms values stored in the AIMAV, BIMAV, and CIMAV registers can be calibrated using gain and offset coefficients corresponding to each phase. Calculate the gains in PSM0 mode by supplying the ADE7880 with nominal currents. The offsets can be estimated by supplying the ADE7880 with low currents, usually equal to the minimum value at which the accuracy is required. Every time the external microcontroller reads the AIMAV, BIMAV, and CIMAV registers, it uses these coefficients stored in its memory to correct them.

Voltage Channel RMS Calculation

Figure 72 shows the detail of the signal processing chain for the rms calculation on one of the phases of the voltage channel. The voltage channel rms value is processed from the samples used in the voltage channel. The voltage rms values are signed 24-bit values and they are stored into the Registers AVRMS, BVRMS, and CVRMS. The update rate of the current rms measurement is 8 kHz.

With the specified full-scale analog input signal of 0.5 V, the ADC produces an output code that is approximately ±5,326,737. The equivalent rms value of a full-scale sinusoidal signal is 3,766,572 (0x39792C), independent of the line frequency.

The accuracy of the voltage rms is typically 0.1% error from the full-scale input down to 1/1000 of the full-scale input. Additionally, this measurement has a bandwidth of 3.3 kHz. It is recommended to read the rms registers synchronous to the voltage zero crossings to ensure stability. The IRQ1 interrupt can be used to indicate when a zero crossing has occurred (see the Interrupts section).

The V rms measurement settling time is 580 ms for both 50 Hz and 60 Hz input signals. The V rms measurement settling time is the time it takes for the rms register to reflect the value at the input to the voltage channel when starting from 0.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 59, the AVRMS, BVRMS, and CVRMS 24-bit signed registers are accessed as 32-bit registers with the eight MSBs padded with 0s.

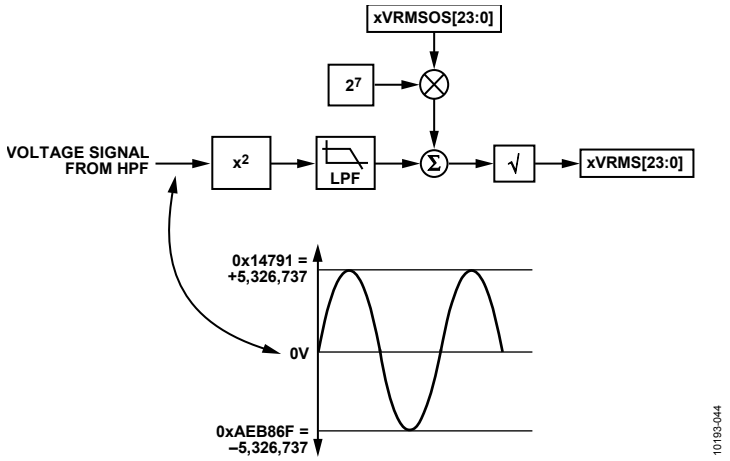

Figure 72. Voltage RMS Signal Processing

Voltage RMS Offset Compensation

The ADE7880 incorporates voltage rms offset compensation registers for each phase: AVRMSOS, BVRMSOS, and CVRMSOS. These are 24-bit signed registers used to remove offsets in the voltage rms calculations. An offset can exist in the rms calculation due to input noises that are integrated in the dc component of $V^2(t)$. The voltage rms offset register is multiplied by 128 and added to the squared voltage rms before the square root is executed. Assuming that the maximum value from the voltage rms calculation is 3,766,572 with full-scale ac inputs (50 Hz), one LSB of the current rms offset represents 0.00045%

$$\left(\sqrt{3767^2+128}/3767-1\right)\times 100$$

of the rms measurement at 60 dB down from full scale. Conduct offset calibration at low current; avoid using voltages equal to zero for this purpose.

$$V\ rms=\sqrt{V\ rms_0^2+128\times VRMSOS} \quad (16)$$

where $V\ rms_0$ is the rms measurement without offset correction.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 44, the AVRMSOS, BVRMSOS, and CVRMSOS 24-bit registers are accessed as 32-bit registers with the four most significant bits padded with 0s and sign extended to 28 bits.

Voltage RMS in 3-Phase, 3-Wire Delta Configurations

In 3-phase 3-wire delta configurations, Phase B is considered the ground of the system, and Phase A and Phase C voltages are measured relative to it. This configuration is chosen using CONSEL bits equal to 01 in ACCMODE register (see Table 15 for all configurations where the ADE7880 may be used). In this situation, all Phase B active, reactive, and apparent powers are 0.

In this configuration, the ADE7880 computes the rms value of the line voltage between Phase A and Phase C and stores the result into BVRMS register. BVGAIN and BVRMSOS registers may be used to calibrate BVRMS register computed in this configuration.

The apparent power computation, in 3-wire and 4-wire delta configurations, will be incorrect, because the line to line voltages are treated as phase voltages by the IC. To get the equivalent wye-configuration apparent power, a scaling factor needs to be applied. Refer to the Three Phase Configurations section of the AN-639 Application Note, *Analog Devices Energy (ADE) Products: Frequently Asked Questions (FAQ),* for details.

ACTIVE POWER CALCULATION

The ADE7880 computes the total active power on every phase. Total active power considers in its calculation all fundamental and harmonic components of the voltages and currents. In addition, the ADE7880 computes the fundamental active power, the power determined only by the fundamental components of the voltages and currents.

The ADE7880 also computes the harmonic active powers, the active powers determined by the harmonic components of the voltages and currents. See the Harmonics Calculations section for details.

Total Active Power Calculation

Electrical power is defined as the rate of energy flow from source to load, and it is given by the product of the voltage and current waveforms. The resulting waveform is called the instantaneous power signal, and it is equal to the rate of energy flow at every instant of time. The unit of power is the watt or joules/sec. If an ac system is supplied by a voltage, v(t), and consumes the current, i(t), and each of them contains harmonics, then

$$v(t)=\sum_{k=1}^{\infty}V_k\sqrt{2}\sin(k\omega t+\varphi_k) \quad (17)$$

$$i(t)=\sum_{k=1}^{\infty}I_k\sqrt{2}\sin(k\omega t+\gamma_k)$$

where:
V_k, I_k are rms voltage and current, respectively, of each harmonic.
φ_k, γ_k are the phase delays of each harmonic.

The instantaneous power in an ac system is

$$p(t)=v(t)\times i(t)=\sum_{k=1}^{\infty}V_kI_k\cos(\varphi_k-\gamma_k)-\sum_{k=1}^{\infty}V_kI_k\cos(2k\omega t+\varphi_k+\gamma_k)$$
$$+\sum_{\substack{k,m=1\\k\neq m}}^{\infty}V_kI_m\{\cos[(k-m)\omega t+\varphi_k-\gamma_m]-\cos[(k+m)\omega t+\varphi_k+\gamma_m]\} \quad (18)$$

The average power over an integral number of line cycles (n) is given by the equation in Equation 19.

$$P=\frac{1}{nT}\int_0^{nT}p(t)dt=\sum_{k=1}^{\infty}V_kI_k\cos(\varphi_k-\gamma_k) \quad (19)$$

where:
T is the line cycle period.
P is referred to as the total active or total real power.

Note that the total active power is equal to the dc component of the instantaneous power signal $p(t)$ in Equation 18, that is,

$$\sum_{k=1}^{\infty}V_kI_k\cos(\varphi_k-\gamma_k)$$

This is the equation used to calculate the total active power in the ADE7880 for each phase. The equation of fundamental active power is obtained from Equation 18 with k = 1, as follows:

$$FP=V_1I_1\cos(\varphi_1-\gamma_1) \quad (20)$$

Figure 76 shows how the ADE7880 computes the total active power on each phase. First, it multiplies the current and voltage signals in each phase. Next, it extracts the dc component of the instantaneous power signal in each phase (A, B, and C) using LPF2, the low-pass filter.

If the phase currents and voltages contain only the fundamental component, are in phase (that is, $\varphi_1 = \gamma_1 = 0$), and they correspond to full-scale ADC inputs, then multiplying them results in an instantaneous power signal that has a dc component, $V_1 \times I_1$, and a sinusoidal component, $V_1 \times I_1 \cos(2\omega t)$; Figure 73 shows the corresponding waveforms.

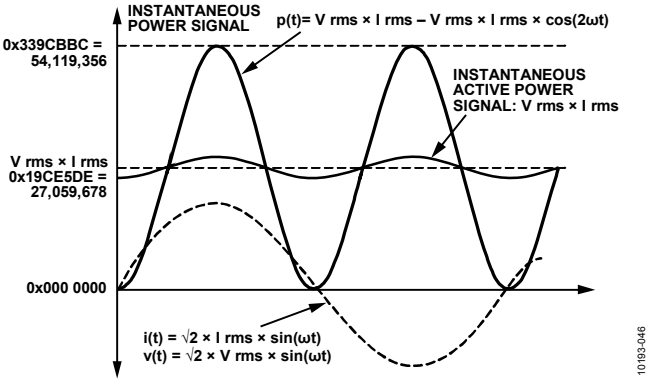

Figure 73. Active Power Calculation

Because LPF2 does not have an ideal brick wall frequency response, the active power signal has some ripple due to the instantaneous power signal. This ripple is sinusoidal and has a frequency equal to twice the line frequency. Because the ripple is sinusoidal in nature, it is removed when the active power signal is integrated over time to calculate the energy. Bit 1 (LPFSEL) of CONFIG3 register selects the LPF2 strength. If LPFSEL is 0 (default), the settling time is 650 ms and the ripple attenuation is 65 dB. If LPFSEL is 1, the settling time is 1300 ms and the ripple attenuation is 128 dB. Figure 74 shows the frequency response of LPF2 when LPFSEL is 0 and Figure 75 shows the frequency response of LPF2 when LPFSEL is 1.

The ADE7880 stores the instantaneous total phase active powers into the AWATT, BWATT, and CWATT registers. Their equation is

$$xWATT = \sum_{k=1}^{\infty} \frac{V_k}{V_{FS}} \times \frac{I_k}{I_{FS}} \times \cos(\varphi_k - \gamma_k) \times PMAX \times \frac{1}{2^4} \quad (21)$$

where:

V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.

$PMAX$ = 27,059,678 it is the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xWATT[23:0] waveform registers can be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

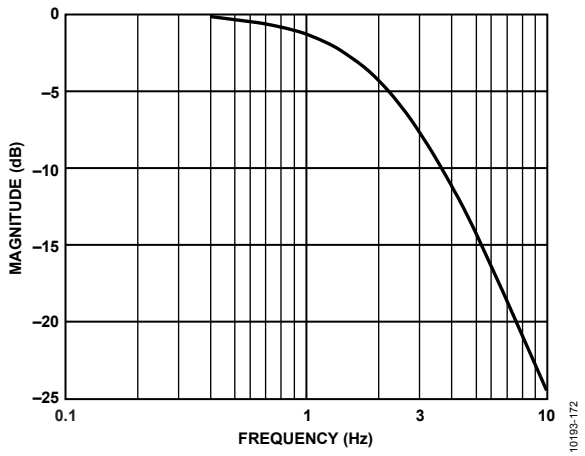

Figure 74. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase When the LPFSEL Bit of CONFIG3 is 0 (Default)

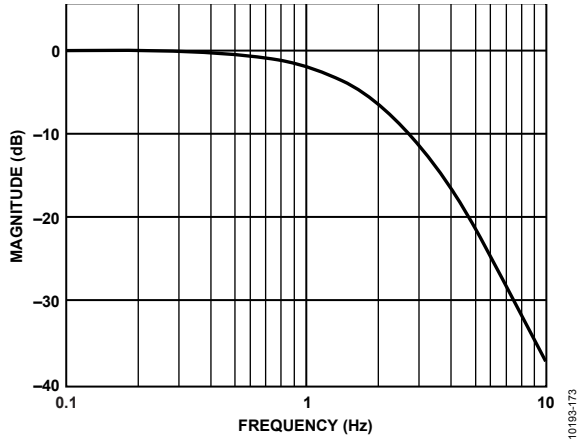

Figure 75. Frequency Response of the LPF Used to Filter Instantaneous Power in Each Phase when the LPFSEL Bit of CONFIG3 is 1

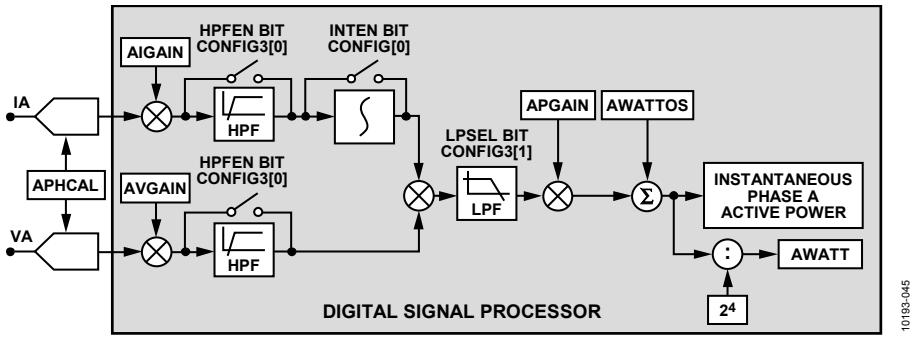

Figure 76. Total Active Power Data Path

Fundamental Active Power Calculation

The ADE7880 computes the fundamental active power using a proprietary algorithm that requires some initializations function of the frequency of the network and its nominal voltage measured in the voltage channel. Bit 14 (SELFREQ) in the COMPMODE register must be set according to the frequency of the network in which the ADE7880 is connected. If the network frequency is between 45 Hz and 55 Hz, clear this bit to 0 (the default value). If the network frequency is between 55 Hz and 66 Hz, set this bit to 1. In addition, initialize the VLEVEL 28-bit signed register based on the following equation:

$$VLEVEL = \frac{V_{FS}}{V_n} \times 4 \times 10^6 \quad (22)$$

where:
V_{FS} is the rms value of the phase voltages when the ADC inputs are at full scale.
V_n is the rms nominal value of the phase voltage.

The VLEVEL register is a 28-bit signed register and is zero padded to 32 bits.

Table 13 presents the settling time for the fundamental active power measurement.

Table 13. Settling Time for Fundamental Active Power

Input Signals	
63% PMAX	**100% PMAX**
375 ms	875 ms

Managing Change in Fundamental Line Frequency

The ADE7880 has a very accurate method for tracking changes in line frequency up to 10 Hz. Typical changes in line frequency are very slow. However, in some calibration or testing scenarios, the line frequency can change abruptly. It is recommended to keep changes in the line frequency within ±5 Hz at any one transition. To cover a wide frequency range from 45 Hz to 66 Hz, it is necessary to ensure that the SELFREQ bit of the COMPMODE register is changed according to the line frequency.

The following two scenarios are examples on how to manage the SELFREQ bit and how to change the line frequency.

Example 1: Consider the scenario where the user plans to calibrate the IC at 50 Hz and then at 60 Hz. In such a case, the following steps must be followed in sequential order.

1. Apply a 50 Hz line frequency.
2. Keep the SELFREQ bit of the COMPMODE register at 0.
3. Calibrate the IC.
4. Apply a 60 Hz line frequency.
5. Immediately, set the SELFREQ bit of the COMPMODE register to 1. It is essential to complete this step immediately after Step 4.
6. Wait for 10 seconds. This waiting period depends on how rapidly the frequency change from 50 Hz to 60 Hz takes place. For an instant change, the typical settling time for fundamental frequency based computations is 10 seconds. For a more gradual change, the waiting period is shorter.
7. Calibrate the IC.

Example 2: Consider the scenario where the user plans to evaluate the performance of the IC at 45 Hz and at 65 Hz. In such a case, the following steps must be followed in sequential order.

1. Apply a 45 Hz line frequency.
2. Keep the SELFREQ bit of the COMPMODE register at 0.
3. Evaluate the IC.
4. Apply a 50 Hz line frequency.
5. Wait for 10 seconds.
6. Apply a 65 Hz line frequency.
7. Immediately set the SELFREQ bit of the COMPMODE register to 1. It is essential to complete this step immediately after Step 6.
8. Wait for 10 seconds.
9. Evaluate the IC.

Active Power Gain Calibration

Note that the average active power result from the LPF2 output in each phase can be scaled by ±100% by writing to the watt gain 24-bit register of the phase (APGAIN, BPGAIN, CPGAIN). The xPGAIN registers are placed on data paths of all powers computed by the ADE7880: total active powers, fundamental active and reactive powers and apparent powers. This is possible because all power data paths have identical overall gains. Therefore, to compensate the gain errors in various powers data paths it is sufficient to analyze only one power data path, for example, the total active power, calculate the correspondent APGAIN, BPGAIN and CPGAIN registers, and all the power data paths are gain compensated.

The power gain registers are twos complement, signed registers and have a resolution of 2^{-23}/LSB. Equation 23 describes mathematically the function of the power gain registers.

$$Average\ Power\ Data = LPF2\ Output \times \left(1 + \frac{Power\ Gain\ Register}{2^{23}}\right) \quad (23)$$

The output is scaled by −50% by writing 0xC00000 to the watt gain registers, and it is increased by +50% by writing 0x400000 to them. These registers are used to calibrate the active, reactive and apparent power (or energy) calculation for each phase.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words, and the DSP works on 28 bits. Similar to registers presented in Figure 44, the APGAIN, BPGAIN, and CPGAIN 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Active Power Offset Calibration

The ADE7880 incorporates a watt offset 24-bit register on each phase and on each active power. The AWATTOS, BWATTOS, and CWATTOS registers compensate the offsets in the total active power calculations, and the AFWATTOS, BFWATTOS, and CFWATTOS registers compensate offsets in the fundamental active power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the active power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. One LSB in the active power offset register is equivalent to 1 LSB in the active power multiplier output. With full-scale current and voltage inputs, the LPF2 output is PMAX = 27,059,678. At −80 dB down from the full scale (active power scaled down 10^4 times), one LSB of the active power offset register represents 0.0369% of PMAX.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to registers presented in Figure 44, the AWATTOS, BWATTOS, CWATTOS, AFWATTOS, BFWATTOS, and CFWATTOS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

Sign of Active Power Calculation

The average active power is a signed calculation. If the phase difference between the current and voltage waveform is more than 90°, the average power becomes negative. Negative power indicates that energy is being injected back on the grid. The ADE7880 has sign detection circuitry for active power calculations. It can monitor the total active powers or the fundamental active powers. As described in the Active Energy Calculation section, the active energy accumulation is performed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the WTHR register threshold, a dedicated interrupt is triggered. The sign of each phase active power can be read in the PHSIGN register.

Bit 6 (REVAPSEL) in the ACCMODE register sets the type of active power being monitored. When REVAPSEL is 0, the default value, the total active power is monitored. When REVAPSEL is 1, the fundamental active power is monitored.

Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register are set when a sign change occurs in the power selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Bits[2:0] (CWSIGN, BWSIGN, and AWSIGN, respectively) in the PHSIGN register are set simultaneously with the REVAPC, REVAPB, and REVAPA bits. They indicate the sign of the power. When they are 0, the corresponding power is positive. When they are 1, the corresponding power is negative.

Bit REVAPx of STATUS0 and Bit xWSIGN in the PHSIGN register refer to the total active power of Phase x, the power type being selected by Bit 6 (REVAPSEL) in the ACCMODE register.

Interrupts attached to Bits[8:6] (REVAPC, REVAPB, and REVAPA, respectively) in the STATUS0 register can be enabled by setting Bits[8:6] in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is returned to high by writing to the STATUS0 register with the corresponding bit set to 1.

Active Energy Calculation

As previously stated, power is defined as the rate of energy flow. This relationship can be expressed mathematically as

$$Power = \frac{dEnergy}{dt} \quad (24)$$

Conversely, energy is given as the integral of power, as follows:

$$Energy = \int p(t)dt \quad (25)$$

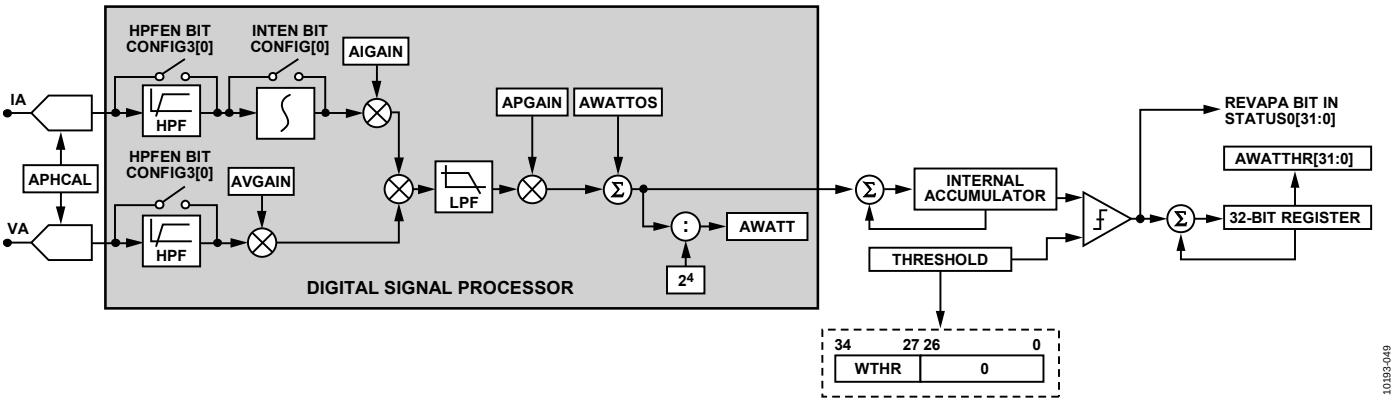

Figure 77. Total Active Energy Accumulation

The ADE7880 achieves the integration of the active power signal in two stages (see Figure 77). The process is identical for both total and fundamental active powers. The first stage accumulates the instantaneous phase total or fundamental active power at 1.024MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register.

The sign of the energy in this moment is considered the sign of the active power (see the Sign of Active Power Calculation section for details). The second stage consists of accumulating the pulses generated at the first stage into internal 32-bit accumulation registers. The content of these registers is transferred to watt-hour registers, xWATTHR and xFWATTHR, when these registers are accessed.

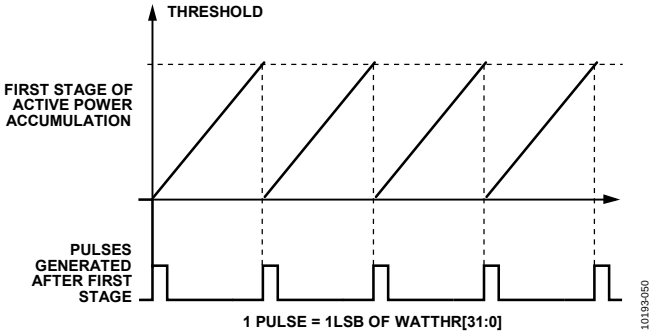

Figure 78. Active Power Accumulation Inside the DSP

Figure 78 explains this process. The threshold is formed by concatenating the WTHR 8-bit unsigned register to 27 bits equal to 0. It is introduced by the user and is common for total and fundamental active powers on all phases. Its value depends on how much energy is assigned to one LSB of watt-hour registers. Supposing a derivative of Wh [10^n Wh], n as an integer, is desired as one LSB of the xWATTHR register, WTHR is computed using the following equation:

$$WTHR = \frac{PMAX \times f_S \times 3600 \times 10^n}{U_{FS} \times I_{FS} \times 2^{27}} \quad (26)$$

where:
PMAX = 27,059,678 = 0x19CE5DE as the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
U_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

WTHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Avoid values lower than 3, that is, 2 or 1, and never use 0 as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation 27.

$$Energy = \int p(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} p(nT) \times T \right\} \quad (27)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7880, the total phase active powers are accumulated in the AWATTHR, BWATTHR, and CWATTHR 32-bit signed registers, and the fundamental phase active powers are accumulated in the AFWATTHR, BFWATTHR, and CFWATTHR 32-bit signed registers. The active energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the active power is positive. Conversely, if the active power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues decreasing in value.

The ADE7880 provides a status flag to signal when one of the xWATTHR and xFWATTHR registers is half full. Bit 0 (AEHF) in the STATUS0 register is set when Bit 30 of one of the xWATTHR registers changes, signifying one of these registers is half full. If the active power is positive, the watt-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the active power is negative, the watt-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF. Similarly, Bit 1 (FAEHF) in STATUS0 register, is set when Bit 30 of one of the xFWATTHR registers changes, signifying one of these registers is half full.

Setting Bits[1:0] in the MASK0 register enable the FAEHF and AEHF interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xWATTHR (for the AEHF interrupt) or xFWATTHR (for the FAEHF interrupt), become half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to logic high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all watt-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 976.5625 ns (1.024MHz frequency). With full-scale sinusoidal signals on the analog inputs and the watt gain registers set to 0x00000, the average word value from each LPF2 is PMAX = 27,059,678 = 0x19CE5DE. If the WTHR register threshold is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to watt-hour registers every

$$\frac{3 \times 2^{27}}{PMAX \times 1.024 \times 10^6} = 14.531 \mu sec$$

The maximum value that can be stored in the watt-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFF,FFFF \times 14.531\ \mu s = 8\ hr\ 40\ min\ 6\ sec \quad (28)$$

Active Energy Accumulation Modes

The active power is accumulated in each watt-hour accumulation 32-bit register (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) according to the configuration of Bit 5 and Bit 4 (CONSEL bits) in the ACCMODE register. The various configurations are described in Table 14.

Table 14. Inputs to Watt-Hour Accumulation Registers

CONSEL	AWATTHR	BWATTHR	CWATTHR
00	VA × IA	VB × IB	VC × IC
01	VA × IA	VB × IB VB = VA – VC[1]	VC × IC
10	VA × IA	VB × IB VB = –VA – VC	VC × IC
11	VA × IA	VB × IB VB = –VA	VC × IC

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7880 computes the rms value of the line voltage between Phase A and Phase C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase, 3-Wire Delta Configurations section). Consequently, the ADE7880 computes powers associated with Phase B that do not have physical meaning. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy-to-frequency converters by setting bits TERMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Depending on the polyphase meter service, choose the appropriate formula to calculate the active energy. The American ANSI C12.10 standard defines the different configurations of the meter. Table 15 describes which mode to choose in these various configurations.

Table 15. Meter Form Configuration

ANSI Meter Form	Configuration	CONSEL
5S/13S	3-wire delta	01
6S/14S	4-wire wye	10
8S/15S	4-wire delta	11
9S/16S	4-wire wye	00

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine how the active power is accumulated in the watt-hour registers and how the CF frequency output can be generated as a function of the total and fundamental active powers. See the Energy-to-Frequency Conversion section for details.

The apparent power computation, in 3-wire and 4-wire delta configurations, will be incorrect, because the line to line voltages are treated as phase voltages by the IC. To get the equivalent wye-configuration apparent power, a scaling factor needs to be applied. Refer to the Three Phase Configurations section of AN-639 Application Note, *Analog Devices Energy (ADE) Products: Frequently Asked Questions (FAQ)*, for details.

Line Cycle Active Energy Accumulation Mode

In line cycle energy accumulation mode, the energy accumulation is synchronized to the voltage channel zero crossings such that active energy is accumulated over an integral number of half line cycles. The advantage of summing the active energy over an integer number of line cycles is that the sinusoidal component in the active energy is reduced to 0. This eliminates any ripple in the energy calculation and allows the energy to be accumulated accurately over a shorter time. By using the line cycle energy accumulation mode, the energy calibration can be greatly simplified, and the time required to calibrate the meter can be significantly reduced. In line cycle energy accumulation mode, the ADE7880 transfers the active energy accumulated in the 32-bit internal accumulation registers into the xWATHHR or xFWATTHR registers after an integral number of line cycles, as shown in Figure 79. The number of half line cycles is specified in the LINECYC register.

The line cycle energy accumulation mode is activated by setting Bit 0 (LWATT) in the LCYCMODE register. The energy accumulation over an integer number of half line cycles is written to the watt-hour accumulation registers after LINECYC number of half line cycles is detected. When using the line cycle accumulation mode, the Bit 6 (RSTREAD) of the LCYCMODE register must be set to Logic 0 because the read with reset of watt-hour registers is not available in this mode.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero crossings count during calibration.

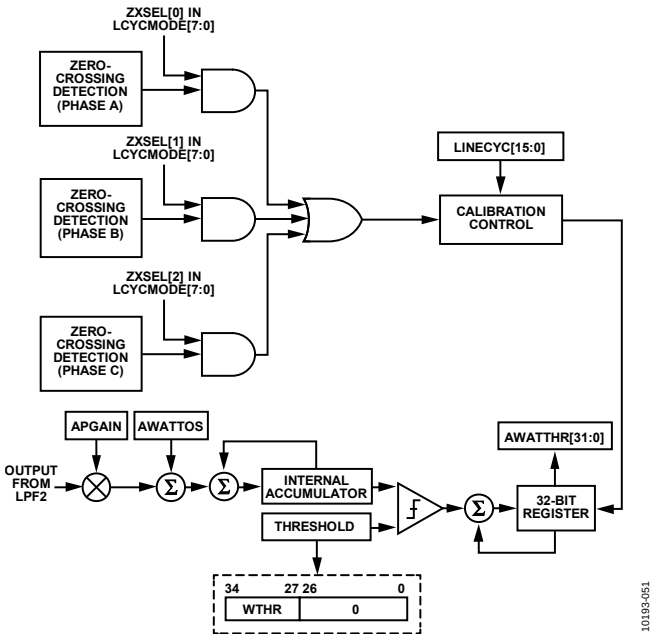

Figure 79. Line Cycle Active Energy Accumulation Mode

The number of zero crossings is specified by the LINECYC 16-bit unsigned register. The ADE7880 can accumulate active power for up to 65,535 combined zero crossings. Note that the internal zero-crossing counter is always active. By setting Bit 0 (LWATT) in the LCYCMODE register, the first energy accumulation result is, therefore, incorrect. Writing to the LINECYC register when

the LWATT bit is set resets the zero-crossing counter, thus ensuring that the first energy accumulation result is accurate.

At the end of an energy calibration cycle, Bit 5 (LENERGY) in the STATUS0 register is set. If the corresponding mask bit in the MASK0 interrupt mask register is enabled, the $\overline{\text{IRQ0}}$ pin also goes active low. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high again by writing to the STATUS0 register with the corresponding bit set to 1.

Because the active power is integrated on an integer number of half-line cycles in this mode, the sinusoidal components are reduced to 0, eliminating any ripple in the energy calculation. Therefore, total energy accumulated using the line cycle accumulation mode is

$$e = \int_{t}^{t+nT} p(t)dt = nT\sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k) \quad (29)$$

where nT is the accumulation time.

Note that line cycle active energy accumulation uses the same signal path as the active energy accumulation. The LSB size of these two methods is equivalent.

FUNDAMENTAL REACTIVE POWER CALCULATION

The ADE7880 computes the fundamental reactive power, the power determined only by the fundamental components of the voltages and currents.

The ADE7880 also computes the harmonic reactive powers, the reactive powers determined by the harmonic components of the voltages and currents. See Harmonics Calculations section for details. A load that contains a reactive element (inductor or capacitor) produces a phase difference between the applied ac voltage and the resulting current. The power associated with reactive elements is called reactive power, and its unit is VAR. Reactive power is defined as the product of the voltage and current waveforms when all harmonic components of one of these signals are phase shifted by 90°.

Equation 31 is an example of the instantaneous reactive power signal in an ac system when the phase of the current channel is shifted by +90°.

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin(k\omega t + \varphi_k) \quad (30)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin(k\omega t + \gamma_k) \quad (31)$$

$$i'(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin\left(k\omega t + \gamma_k + \frac{\pi}{2}\right)$$

where $i'(t)$ is the current waveform with all harmonic components phase shifted by 90°.

Next, the instantaneous reactive power, q(t), can be expressed as

$$q(t) = v(t) \times i'(t) \quad (32)$$

$$q(t) = \sum_{k=1}^{\infty} V_k I_k \times 2\sin(k\omega t + \varphi_k) \times \sin(k\omega t + \gamma_k + \frac{\pi}{2}) +$$

$$\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} V_k I_m \times 2\sin(k\omega t + \varphi_k) \times \sin(m\omega t + \gamma_m + \frac{\pi}{2})$$

Note that $q(t)$ can be rewritten as

$$q(t) = \sum_{k=1}^{\infty} V_k I_k \{\cos(\varphi_k - \gamma_k - \frac{\pi}{2}) - \cos(2k\omega t + \varphi_k + \gamma_k + \frac{\pi}{2})\} +$$

$$\sum_{\substack{k,m=1 \\ k\neq m}}^{\infty} V_k I_m \{\cos[(k-m)\omega t + \varphi_k - \gamma_k - \frac{\pi}{2}] -$$

$$\cos[(k+m)\omega t + \varphi_k + \gamma_k + \frac{\pi}{2}]\} \quad (33)$$

The average total reactive power over an integral number of line cycles (n) is shown in Equation 34.

$$Q = \frac{1}{nT}\int_{0}^{nT} q(t)dt = \sum_{k=1}^{\infty} V_k I_k \cos(\varphi_k - \gamma_k - \frac{\pi}{2}) \quad (34)$$

$$Q = \sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k - \gamma_k)$$

where:
T is the period of the line cycle.
Q is referred to as the total reactive power. Note that the total reactive power is equal to the dc component of the instantaneous reactive power signal q(t) in Equation 32, that is,

$$\sum_{k=1}^{\infty} V_k I_k \sin(\varphi_k - \gamma_k)$$

This is the relationship used to calculate the total reactive power for each phase. The instantaneous reactive power signal, q(t), is generated by multiplying each harmonic of the voltage signals by the 90° phase-shifted corresponding harmonic of the current in each phase.

The expression of fundamental reactive power is obtained from Equation 33 with k = 1, as follows:

$$FQ = V_1 I_1 \sin(\varphi_1 - \gamma_1)$$

The ADE7880 computes the fundamental reactive power using a proprietary algorithm that requires some initialization function of the frequency of the network and its nominal voltage measured in the voltage channel. These initializations are introduced in the Active Power Calculation section and are common for both fundamental active and reactive powers.

The ADE7880 stores the instantaneous fundamental phase reactive powers into the AFVAR, BFVAR, and CFVAR registers. Their equation is

$$xFVAR = \frac{V_1}{V_{FS}} \times \frac{I_1}{I_{FS}} \times \sin(\varphi_1 - \gamma_1) \times PMAX \times \frac{1}{2^4} \quad (35)$$

where:
V_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.

PMAX = 27,059,678, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xFVAR waveform registers are not mapped with an address in the register space and can be accessed only through HSDC port in the waveform sampling mode (see Waveform Sampling Mode section for details). Fundamental reactive power information is also available through the harmonic calculations of the ADE7880 (see Harmonics Calculations section for details).

Table 16 presents the settling time for the fundamental reactive power measurement, which is the time it takes the power to reflect the value at the input of the ADE7880.

Table 16. Settling Time for Fundamental Reactive Power

Input Signals	
63% PMAX	**100% PMAX**
375 ms	875 ms

Bit 14 (SELFREQ) in the COMPMODE register must be set according to the frequency of the network in which the ADE7880 is connected. If the network frequency is between 45 Hz and 55 Hz, clear this bit to 0 (the default value). If the network frequency is between 55 Hz and 66 Hz, set this bit to 1. In addition, initialize the VLEVEL, 28-bit signed register based on Equation 22.

Refer to the Managing Change in Fundamental Line Frequency section for details on how to manage changes in line frequency.

Fundamental Reactive Power Gain Calibration

The average fundamental reactive power in each phase can be scaled by ±100% by writing to one of the phase's VAR gain 24-bit register (APGAIN, BPGAIN, or CPGAIN). Note that these registers are the same gain registers used to compensate the other powers computed by the ADE7880. See the Active Power Gain Calibration section for details on these registers.

Fundamental Reactive Power Offset Calibration

The ADE7880 provides a fundamental reactive power offset register on each phase. The AFVAROS, BFVAROS, and CFVAROS registers compensate the offsets in the fundamental reactive power calculations. These are signed twos complement, 24-bit registers that are used to remove offsets in the fundamental reactive power calculations. An offset can exist in the power calculation due to crosstalk between channels on the PCB or in the chip itself. The resolution of the registers is the same as for the active power offset registers (see the Active Power Offset Calibration section).

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words and the DSP works on 28 bits. Similar to the registers presented in Figure 44, the AFVAROS, BFVAROS, and CFVAROS 24-bit signed registers are accessed as 32-bit registers with the four MSBs padded with 0s and sign extended to 28 bits.

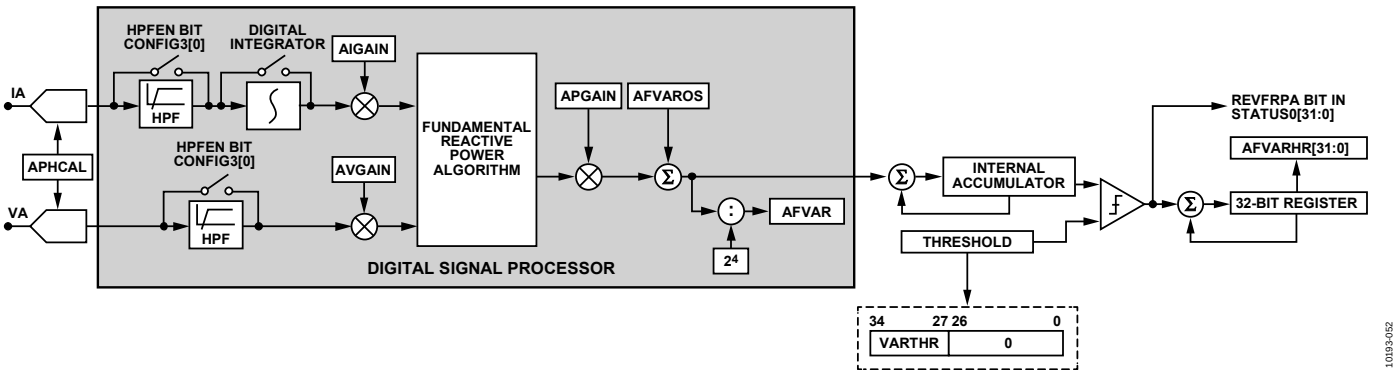

Figure 80. Fundamental Reactive Energy Accumulation

Sign of Fundamental Reactive Power Calculation

Note that the fundamental reactive power is a signed calculation. Table 17 summarizes the relationship between the phase difference between the voltage and the current and the sign of the resulting reactive power calculation.

The ADE7880 has sign detection circuitry for reactive power calculations that can monitor the fundamental reactive powers. As described in the Fundamental Reactive Energy Calculation section, the reactive energy accumulation is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated into the internal accumulator reaches the VARTHR register threshold, a dedicated interrupt is triggered. The sign of each phase reactive power can be read in the PHSIGN register.

Bits[12:10] (REVFRPC, REVFRPB, and REVFRPA, respectively) in the STATUS0 register are set when a sign change occurs in the fundamental reactive power.

Bits[6:4] (CFVARSIGN, BFVARSIGN, and AFVARSIGN, respectively) in the PHSIGN register are set simultaneously with the REVFRPC, REVFRPB, and REVFRPA bits. They indicate the sign of the fundamental reactive power. When they are 0, the reactive power is positive. When they are 1, the reactive power is negative.

Bit REVFRPx of the STATUS0 register and Bit xFVARSIGN in the PHSIGN register refer to the reactive power of Phase x.

Setting Bits[12:10] in the MASK0 register enables the REVFRPC, REVFRPB, and REVFRPA interrupts, respectively. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Table 17. Sign of Reactive Power Calculation

Φ[1]	Sign of Reactive Power
Between 0 to +180	Positive
Between −180 to 0	Negative

[1] Φ is defined as the phase angle of the voltage signal minus the current signal; that is, Φ is positive if the load is inductive and negative if the load is capacitive.

Fundamental Reactive Energy Calculation

Fundamental reactive energy is defined as the integral of fundamental reactive power.

$$Reactive\ Energy = \int q(t)dt \quad (36)$$

Similar to active power, the ADE7880 achieves the integration of the reactive power signal in two stages (see Figure 80).

- The first stage accumulates the instantaneous phase fundamental reactive power at 1.024 MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The sign of the energy in this moment is considered the sign of the reactive power (see the Sign of Fundamental Reactive Power Calculation section for details).
- The second stage consists in accumulating the pulses generated after the first stage into internal 32-bit accumulation registers. The content of these registers is transferred to the var-hour registers (xFVARHR) when these registers are accessed. AFWATTHR, BFWATTHR, and CFWATTHR represent phase fundamental reactive energies.

Figure 80 explains this process. The threshold is formed by concatenating the VARTHR 8-bit unsigned register to 27 bits equal to 0 and it is introduced by the user. Its value depends on how much energy is assigned to one LSB of var-hour registers. Supposing a derivative of a volt ampere reactive hour (varh) [10^n varh] where n is an integer, is desired as one LSB of the VARHR register, the VARTHR register can be computed using the following equation:

$$VARTHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{U_{FS} \times I_{FS} \times 2^{27}} \quad (37)$$

where:
$PMAX$ = 27,059,678 = 0x19CE5DE, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
U_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

VARTHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Avoid, values lower than 3, that is, 2 or 1, and never use 0 as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time, shown in Equation 38:

$$ReactiveEnergy = \int q(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} q(nT) \times T \right\} \quad (38)$$

where:
n is the discrete time sample number.
T is the sample period.

On the ADE7880, the fundamental phase reactive powers are accumulated in the AFVARHR, BFVARHR, and CFVARHR 32-bit signed registers. The reactive energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the reactive power is positive. Conversely, if the reactive power is negative, the energy register underflows to full-scale positive (0x7FFFFFFF) and continues to decrease in value.

The ADE7880 provides a status flag to signal when one of the xFVARHR registers is half full. Bit 3 (FREHF) in the STATUS0 register is set when Bit 30 of one of the xFVARHR registers changes, signifying one of these registers is half full. If the reactive power is positive, the var-hour register becomes half full when it increments from 0x3FFF FFFF to 0x4000 0000. If the reactive power is negative, the var-hour register becomes half full when it decrements from 0xC000 0000 to 0xBFFF FFFF.

Setting Bit 3 in the MASK0 register enables the FREHF interrupt. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the energy registers, xFVARHR, becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all var-hour accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period (T) for the accumulation register is 976.5625 ns (1.024 MHz frequency). With full-scale sinusoidal signals on the analog inputs and a 90° phase difference between the voltage and the current signal (the largest possible reactive power), the average word value representing the reactive power is PMAX = 27,059,678 = 0x19CE5DE. If the VARTHR threshold is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to var-hour registers every

$$\frac{3\times 2^{27}}{PMAX\times 1.024\times 10^{6}} = 14.531\,\mu\text{sec}$$

The maximum value that can be stored in the var-hour accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0\text{x}7\text{FFF,FFFF} \times 14.531\ \mu\text{s} = 8\ \text{hr}\ 40\ \text{min}\ 6\ \text{sec} \quad (39)$$

Fundamental Reactive Energy Accumulation Modes

The fundamental reactive power accumulated in each var-hour accumulation 32-bit register (AFVARHR, BFVARHR, and CFVARHR) depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register, in correlation with the watt-hour registers. The different configurations are described in Table 18. Note that IA′/IB′/IC′ are the phase-shifted current waveforms.

Table 18. Inputs to Var-Hour Accumulation Registers

CONSEL[1:0]	AFVARHR	BFVARHR	CFVARHR
00	VA × IA′	VB × IB′	VC × IC′
01	VA × IA′	VB × IB′ VB = VA – VC[1]	VC × IC′
10	VA × IA′	VB × IB′ VB = –VA – VC	VC x IC′
11	VA × IA′	VB × IB′ VB = –VA	VC × IC′

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7880 computes the rms value of the line voltage between phases A and C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase, 3-Wire Delta Configurations section). Consequently, the ADE7880 computes powers associated with Phase B that do not have physical meaning. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of Phase B to the energy to frequency converters by setting bits TERMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in COMPMODE register (see the Energy-to-Frequency Conversion section).

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine how the reactive power is accumulated in the var-hour registers and how the CF frequency output can be generated function of total and fundamental active and reactive powers. See the Energy-to-Frequency Conversion section for details.

The apparent power computation, in 3-wire and 4-wire delta configurations, will be incorrect, because the line to line voltages are treated as phase voltages by the IC. To get the equivalent wye-configuration apparent power, a scaling factor needs to be applied. Refer to the Three Phase Configurations section of AN-639 Application Note, *Analog Devices Energy (ADE) Products: Frequently Asked Questions (FAQ)*, for details.

Line Cycle Reactive Energy Accumulation Mode

As mentioned in the Line Cycle Active Energy Accumulation Mode section, in line cycle energy accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings so that reactive energy can be accumulated over an integral number of half line cycles.

In this mode, the ADE7880 transfers the reactive energy accumulated in the 32-bit internal accumulation registers into the xFVARHR registers after an integral number of line cycles, as shown in Figure 81. The number of half line cycles is specified in the LINECYC register.

The line cycle reactive energy accumulation mode is activated by setting Bit 1 (LVAR) in the LCYCMODE register. The fundamental reactive energy accumulated over an integer number of half line cycles or zero crossings is available in the var-hour accumulation registers after the number of zero crossings specified in the LINECYC register is detected. When using the line cycle accumulation mode, set Bit 6 (RSTREAD) of the LCYCMODE register to Logic 0 because a read with the reset of var-hour registers is not available in this mode.

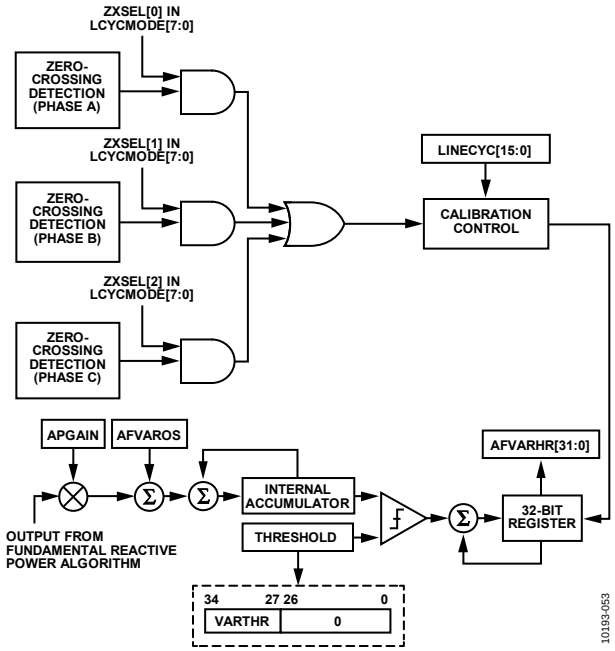

Figure 81. Line Cycle Fundamental Reactive Energy Accumulation Mode

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

APPARENT POWER CALCULATION

Apparent power is defined as the maximum active power that can be delivered to a load. One way to obtain the apparent power is by multiplying the voltage rms value by the current rms value (also called the arithmetic apparent power).

$$S = V\,rms \times I\,rms \tag{40}$$

where:
S is the apparent power.
$V\,rms$ and $I\,rms$ are the rms voltage and current, respectively.

The ADE7880 computes the arithmetic apparent power on each phase. Figure 82 illustrates the signal processing in each phase for the calculation of the apparent power in the ADE7880. Because V rms and I rms contain all harmonic information, the apparent power computed by the ADE7880 is total apparent power. The ADE7880 computes fundamental and harmonic apparent powers determined by the fundamental and harmonic components of the voltages and currents. See the Harmonics Calculations section for details.

The ADE7880 stores the instantaneous phase apparent powers into the AVA, BVA, and CVA registers. Their equation is

$$xVA = \frac{U}{U_{FS}} \times \frac{I}{I_{FS}} \times PMAX \times \frac{1}{2^4} \tag{41}$$

where:
U, I are the rms values of the phase voltage and current.
U_{FS}, I_{FS} are the rms values of the phase voltage and current when the ADC inputs are at full scale.
$PMAX$ = 27,059,678, the instantaneous power computed when the ADC inputs are at full scale and in phase.

The xVA[23:0] waveform registers may be accessed using various serial ports. Refer to the Waveform Sampling Mode section for more details.

The ADE7880 can compute the apparent power in an alternative way by multiplying the phase rms current by an rms voltage introduced externally. See the Apparent Power Calculation Using VNOM section for details.

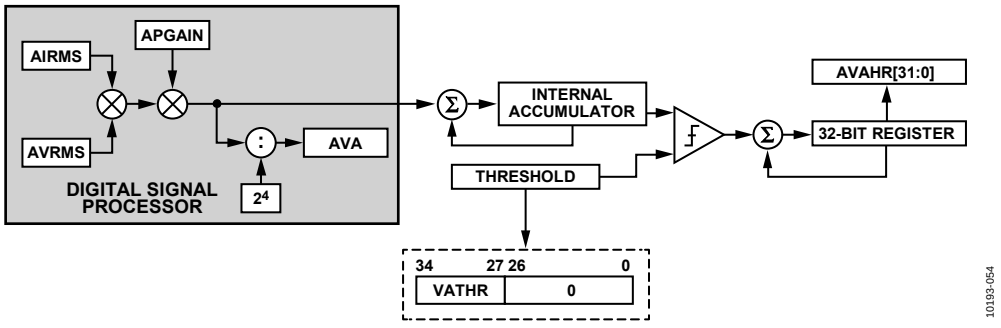

Figure 82. Apparent Power Data Flow and Apparent Energy Accumulation

Apparent Power Gain Calibration

The average apparent power result in each phase can be scaled by ±100% by writing to one of the phase's PGAIN 24-bit registers (APGAIN, BPGAIN, or CPGAIN). Note that these registers are the same gain registers used to compensate the other powers computed by the ADE7880. See the Active Power Gain Calibration section for details on these registers.

Apparent Power Offset Calibration

Each rms measurement includes an offset compensation register to calibrate and eliminate the dc component in the rms value (see the Root Mean Square Measurement section). The voltage and current rms values are multiplied together in the apparent power signal processing. As no additional offsets are created in the multiplication of the rms values, there is no specific offset compensation in the apparent power signal processing. The offset compensation of the apparent power measurement in each phase is accomplished by calibrating each individual rms measurement.

Apparent Power Calculation Using VNOM

The ADE7880 can compute the apparent power by multiplying the phase rms current by an rms voltage introduced externally in the VNOM 24-bit signed register.

When one of Bits[13:11] (VNOMCEN, VNOMBEN, or VNOMAEN) in the COMPMODE register is set to 1, the apparent power in the corresponding phase (Phase x for VNOMxEN) is computed in this way. When the VNOMxEN bits are cleared to 0, the default value, then the arithmetic apparent power is computed. When the VNOMxEN bit is set to 1, the applied voltage input in the corresponding phase is ignored and all corresponding rms voltage instances are replaced by the value in the VNOM register.

The VNOM register contains a number determined by V, the desired nominal phase rms voltage, and V_{FS}, the rms value of the phase voltage when the ADC inputs are at full scale:

$$VNOM = \frac{V}{V_{FS}} \times 3{,}766{,}572 \quad (42)$$

where V is the nominal phase rms voltage.

As stated in the Current Waveform Gain Registers, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. Similar to the register presented in Figure 59, the VNOM 24-bit signed register is accessed as a 32-bit register with the eight MSBs padded with 0s.

Apparent Energy Calculation

Apparent energy is defined as the integral of apparent power.

$$Apparent\ Energy = \int s(t)dt \quad (43)$$

Similar to active and reactive powers, the ADE7880 achieves the integration of the apparent power signal in two stages (see Figure 82). The first stage accumulates the instantaneous apparent power at 1.024 MHz, although they are computed by the DSP at 8 kHz rate. Every time a threshold is reached, a pulse is generated and the threshold is subtracted from the internal register. The second stage consists in accumulating the pulses generated after the first stage into internal 32-bit accumulation registers. The content of these registers is transferred to the VA-hour registers, xVAHR, when these registers are accessed.

Figure 82 illustrates this process. The threshold is formed by the VATHR 8-bit unsigned register concatenated to 27 bits equal to 0. It is introduced by the user and is common for all phase total active and fundamental powers. Its value depends on how much energy is assigned to one LSB of VA-hour registers. When a derivative of apparent energy (VAh) [10^n VAh], where n is an integer, is desired as one LSB of the xVAHR register, the xVATHR register can be computed using the following equation:

$$VATHR = \frac{PMAX \times f_s \times 3600 \times 10^n}{U_{FS} \times I_{FS} \times 2^{27}} \quad (44)$$

where:
$PMAX$ = 27,059,678 = 0x19CE5DE, the instantaneous power computed when the ADC inputs are at full scale.
f_S = 1.024 MHz, the frequency at which every instantaneous power computed by the DSP at 8 kHz is accumulated.
U_{FS}, I_{FS} are the rms values of phase voltages and currents when the ADC inputs are at full scale.

The VATHR register is an 8-bit unsigned number, so its maximum value is $2^8 - 1$. Its default value is 0x3. Avoid values lower than 3, that is, 2 or 1; never use 0 as the threshold must be a non-zero value.

This discrete time accumulation or summation is equivalent to integration in continuous time following the description in Equation 45.

$$ApparentEnergy = \int s(t)dt = \lim_{T \to 0} \left\{ \sum_{n=0}^{\infty} s(nT) \times T \right\} \quad (45)$$

where:
n is the discrete time sample number.
T is the sample period.

In the ADE7880, the phase apparent powers are accumulated in the AVAHR, BVAHR, and CVAHR 32-bit signed registers. The apparent energy register content can roll over to full-scale negative (0x80000000) and continue increasing in value when the apparent power is positive.

The ADE7880 provides a status flag to signal when one of the xVAHR registers is half full. Bit 4 (VAEHF) in the STATUS0 register is set when Bit 30 of one of the xVAHR registers changes, signifying one of these registers is half full. As the apparent power is always positive and the xVAHR registers are signed, the VA-hour registers become half full when they increment from 0x3FFFFFFF to 0x40000000. Interrupts attached to Bit VAEHF in the STATUS0 register can be enabled by setting Bit 4 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low and the status bit is set to 1 whenever one of the Energy Registers xVAHR becomes half full. The status bit is cleared and the $\overline{\text{IRQ0}}$ pin is set to high

by writing to the STATUS0 register with the corresponding bit set to 1.

Setting Bit 6 (RSTREAD) of the LCYCMODE register enables a read-with-reset for all xVAHR accumulation registers, that is, the registers are reset to 0 after a read operation.

Integration Time Under Steady Load

The discrete time sample period for the accumulation register is 976.5625 ns (1.024 MHz frequency). With full-scale pure sinusoidal signals on the analog inputs, the average word value representing the apparent power is PMAX. If the VATHR threshold register is set at 3, its minimum recommended value, the first stage accumulator generates a pulse that is added to the xVAHR registers every $\frac{3\times 2^{27}}{PMAX\times 1.024\times 10^{6}} = 14.531\mu\text{sec}$

The maximum value that can be stored in the xVAHR accumulation register before it overflows is $2^{31} - 1$ or 0x7FFFFFFF. The integration time is calculated as

$$Time = 0x7FFFFFFF \times 14.531\ \mu s = 8\ hr\ 40\ min\ 6\ sec \quad (46)$$

Apparent Energy Accumulation Modes

The apparent power accumulated in each accumulation register depends on the configuration of Bits[5:4] (CONSEL[1:0]) in the ACCMODE register. The various configurations are described in Table 19.

Table 19. Inputs to VA-Hour Accumulation Registers

CONSEL[1:0]	AVAHR	BVAHR	CVAHR
00	AVRMS × AIRMS	BVRMS × BIRMS	CVRMS × CIRMS
01	AVRMS × AIRMS	BVRMS × BIRMS VB = VA – VC[1]	CVRMS × CIRMS
10	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA – VC	CVRMS × CIRMS
11	AVRMS × AIRMS	BVRMS × BIRMS VB = –VA	CVRMS × CIRMS

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7880 computes the rms value of the line voltage between Phase A and Phase C and stores the result into the BVRMS register (see the Voltage RMS in 3-Phase, 3-Wire Delta Configurations section). Consequently, the ADE7880 computes powers associated with Phase B that do not have physical meaning. To avoid any errors in the frequency output pins (CF1, CF2, or CF3) related to the powers associated with Phase B, disable the contribution of phase B to the energy to frequency converters by setting bits TERMSEL1[1] or TERMSEL2[1] or TERMSEL3[1] to 0 in COMPMODE register (see the Energy-to-Frequency Conversion section).

The apparent power computation, in 3-wire and 4-wire delta configurations, will be incorrect, because the line to line voltages are treated as phase voltages by the IC. To get the equivalent wye-configuration apparent power, a scaling factor needs to be applied. Refer to the Three Phase Configurations section of AN-639 Application Note, *Analog Devices Energy (ADE) Products: Frequently Asked Questions (FAQ)*, for details.

Line Cycle Apparent Energy Accumulation Mode

As described in the Line Cycle Active Energy Accumulation Mode section, associated with the line cycle accumulation mode, the energy accumulation can be synchronized to the voltage channel zero crossings allowing apparent energy to be accumulated over an integral number of half line cycles. In this mode, the ADE7880 transfers the apparent energy accumulated in the 32-bit internal accumulation registers into the xVAHR registers after an integral number of line cycles, as shown in Figure 83. The number of half line cycles is specified in the LINECYC register.

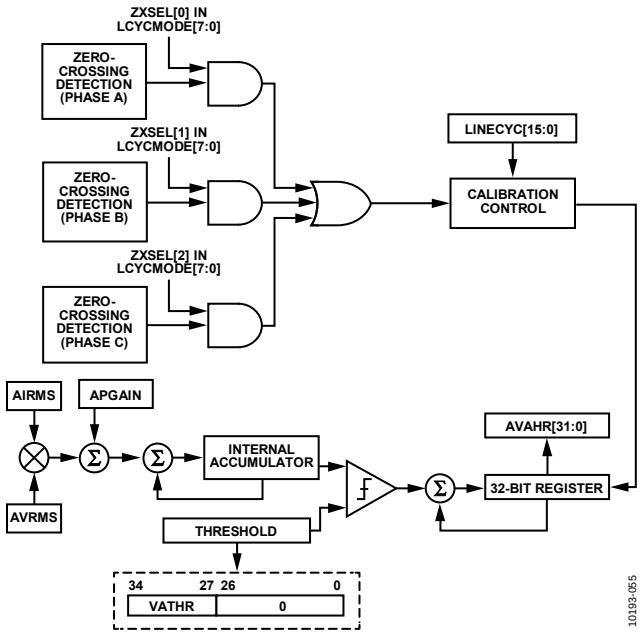

Figure 83. Line Cycle Apparent Energy Accumulation Mode

The line cycle apparent energy accumulation mode is activated by setting Bit 2 (LVA) in the LCYCMODE register. The apparent energy accumulated over an integer number of zero crossings is written to the xVAHR accumulation registers after the number of zero crossings specified in LINECYC register is detected. When using the line cycle accumulation mode, set Bit 6 (RSTREAD) of the LCYCMODE register to Logic 0 because a read with the reset of xVAHR registers is not available in this mode.

Phase A, Phase B, and Phase C zero crossings are, respectively, included when counting the number of half line cycles by setting Bits[5:3] (ZXSEL[x]) in the LCYCMODE register. Any combination of the zero crossings from all three phases can be used for counting the zero crossing. Select only one phase at a time for inclusion in the zero-crossings count during calibration.

For details on setting the LINECYC register and Bit 5 (LENERGY) in the MASK0 interrupt mask register associated with the line cycle accumulation mode, see the Line Cycle Active Energy Accumulation Mode section.

POWER FACTOR CALCULATION

The ADE7880 provides a direct power factor measurement simultaneously on all phases. Power factor in an ac circuit is defined as the ratio of the total active power flowing to the load to the apparent power. The absolute power factor measurement is defined in terms of leading or lagging referring to whether the current is leading or lagging the voltage waveform. When the current is leading the voltage, the load is capacitive and this is defined as a negative power factor. When the current is lagging the voltage, the load is inductive and this defined as a positive power factor. The relationship of the current to the voltage waveform is illustrated in Figure 84.

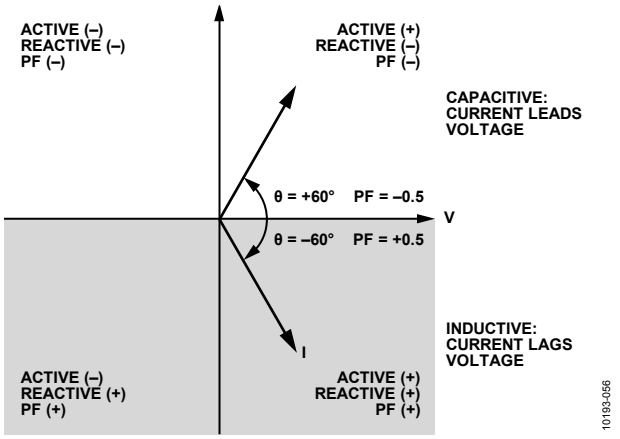

Figure 84. Capacitive and Inductive Loads

As shown in Figure 84, the reactive power measurement is negative when the load is capacitive, and positive when the load is inductive. The sign of the reactive power can therefore be used to reflect the sign of the power factor. Note that the ADE7880 computes the fundamental reactive power, so its sign is used as the sign of the absolute power factor. If the fundamental reactive power is in no load state, then the sign of the power factor is the sign of the total active power.

The mathematical definition of power factor is shown in Equation 47:

$$Power\ Factor = (Sign\ Fundamental\ Reactive\ Power) \times \frac{abs(Total\ Active\ Power)}{Apparent\ Power} \quad (47)$$

As previously mentioned, the ADE7880 provides a power factor measurement on all phases simultaneously. These readings are provided into three 16-bit signed registers, APF (Address 0xE902) for Phase A, BPF (Address 0xE903) for Phase B, and CPF (Address 0xE904) for Phase C. The registers are signed twos complement register with the MSB indicating the polarity of the power factor. Each LSB of the APF, BPF, and CPF registers equates to a weight of 2^{-15}, hence the maximum register value of 0x7FFF equating to a power factor value of 1. The minimum register value of 0x8000 corresponds to a power factor of −1. If because of offset and gain calibrations, the power factor is outside the −1 to +1 range, the result is set at −1 or +1 depending on the sign of the fundamental reactive power.

By default the instantaneous total phase active and apparent powers are used to calculate the power factor and the registers are updated at a rate of 8 kHz. The sign bit is taken from the instantaneous fundamental phase reactive energy measurement on each phase.

If a measurement with more averaging is required, the ADE7880 provides an option of using the line cycle accumulation measurement on the active and apparent energies to determine the power factor. This option provides a more stable power factor reading. This mode is enabled by setting the PFMODE bit (Bit 7) in the LCYCMODE register (Address 0xE702). When this mode is enabled the line cycle accumulation mode must be enabled on both the active and apparent energies. This is done by setting the LWATT and LVA bits in the LCYCMODE register (Address 0xE702). The update rate of the power factor measurement is now an integral number of half line cycles that can be programmed into the LINECYC register (Address 0xE60C). For full details on setting up the line cycle accumulation mode see the Line Cycle Active Energy Accumulation Mode and Line Cycle Apparent Energy Accumulation Mode sections.

Note that the power factor measurement is effected by the no load condition if it is enabled (see the No Load Condition section). If the apparent energy no load is true, then the power factor measurement is set to 1. If the no load condition based on total active and apparent energies is true, the power factor measurement is set at 0.

The ADE7880 also computes the power factor on the fundamental and harmonic components based on the fundamental and harmonic active, reactive and apparent powers. See the Harmonics Calculations section for details.

HARMONICS CALCULATIONS

The ADE7880 contains a harmonic engine that analyzes one phase at a time. Harmonic information is computed with a no attenuation pass band of 2.8 kHz (corresponding to a −3 dB bandwidth of 3.3 kHz) and it is specified for line frequencies between 45 Hz and 66 Hz. It is essential that the VLEVEL and SELFREQ registers be set properly to obtain trustable harmonic measurements. Also, the voltage signal must be above ±100 mV peak for the harmonic engine to function properly. See the Managing Change in Fundamental Line Frequency section for details on managing changes in line frequency. Neutral current can also be analyzed simultaneously with the sum of the phase currents. Figure 85 presents a synthesized diagram of the harmonic engine, its settings and its output registers.

Harmonics Calcuations Theory

Consider a nonsinusoidal ac system supplied by a voltage, v(t) that consumes the current i(t). Then

$$v(t) = \sum_{k=1}^{\infty} V_k \sqrt{2} \sin(k\omega t + \varphi_k) \quad (48)$$

$$i(t) = \sum_{k=1}^{\infty} I_k \sqrt{2} \sin(k\omega t + \gamma_k)$$

where:
V_k, I_k are rms voltage and current, respectively, of each harmonic.
Φ_k, γ_k are the phase delays of each harmonic.
ω is the angular velocity at the fundamental (line) frequency f.

The ADE7880 harmonics calculations are specified for line frequencies between 45 Hz and 66 Hz. The phase nominal voltage used as time base must have an amplitude greater than 20% of full scale.

The number of harmonics N that can be analyzed within the 2.8 kHz pass band is the whole number of 2800/f. The absolute maximum number of harmonics accepted by the ADE7880 is 63.

$$N = \left[\frac{2800}{f}\right], \text{N}\leq 63$$

When the ADE7880 analyzes a phase, the following metering quantities are computed:

- Fundamental phase current rms: I_1
- Fundamental phase voltage rms: V_1
- RMS of up to three harmonics of phase current:
  I_x, I_y, I_z, x, y, z = 2, 3,…, N
- RMS of up to three harmonics of phase voltage:
  V_x, V_y, V_z, x, y, z = 2, 3,…, N
- Fundamental phase active power
  $P_1 = V_1 I_1 \cos(\varphi_1 - \gamma_1)$
- Fundamental phase reactive power
  $Q_1 = V_1 I_1 \sin(\varphi_1 - \gamma_1)$
- Fundamental phase apparent power
  $S_1 = V_1 I_1$
- Power factor of the fundamental

  $$pf_1 = \frac{P_1}{S_1}$$

  Active power of up to three harmonics:
  $P_x = V_x I_x \cos(\varphi_x - \gamma_x)$, x = 2, 3,…, N
  $P_y = V_y I_y \cos(\varphi_y - \gamma_y)$, y = 2, 3,…, N
  $P_z = V_z I_z \cos(\varphi_z - \gamma_z)$, z = 2, 3,…, N
- Reactive power of up to three harmonics:
  $Q_x = V_x I_x \sin(\varphi_x - \gamma_x)$, x = 2, 3,…, N
  $Q_y = V_y I_y \sin(\varphi_y - \gamma_y)$, y = 2, 3,…, N
  $Q_z = V_z I_z \sin(\varphi_z - \gamma_z)$, z = 2, 3,…, N
- Apparent power of up to three harmonics:
  $S_x = V_x I_x$, x = 2, 3, …, N
  $S_y = V_y I_y$, y = 2 , 3, …, N
  $S_z = V_z I_z$, z = 2, 3, …, N
- Power factor of up to three harmonics:

  $$pf_x = \frac{P_x}{S_x}, \text{x} = 2, 3,\ldots, \text{N}$$

  $$pf_y = \frac{P_y}{S_y}, \text{y} = 2, 3,\ldots, \text{N}$$

  $$pf_z = \frac{P_z}{S_z}, \text{z} = 2, 3,\ldots, \text{N}$$
- Total harmonic distortion of the phase current

  $$(THD)_I = \frac{\sqrt{I^2 - I_1^2}}{I_1}$$
- Total harmonic distortion of the phase voltage

  $$(THD)_V = \frac{\sqrt{V^2 - V_1^2}}{V_1}$$
- Harmonic distortion of up to three harmonics on the phase current

  $$HD_{I_x} = \frac{I_x}{I_1}, \text{x} = 2, 3,\ldots, \text{N}$$

  $$HD_{I_y} = \frac{I_y}{I_1}, \text{y} = 2, 3,\ldots, \text{N}$$

  $$HD_{I_z} = \frac{I_z}{I_1}, \text{z} = 2, 3,\ldots, \text{N}$$
- Harmonic distortion of up to three harmonics on the phase voltage:

  $$HD_{V_x} = \frac{V_x}{V_1}, \text{x} = 2, 3,\ldots, \text{N}$$

  $$HD_{V_y} = \frac{V_y}{V_1}, \text{y} = 2, 3,\ldots, \text{N}$$

  $$HD_{V_z} = \frac{V_z}{V_1}, \text{z} = 2, 3,\ldots, \text{N}$$

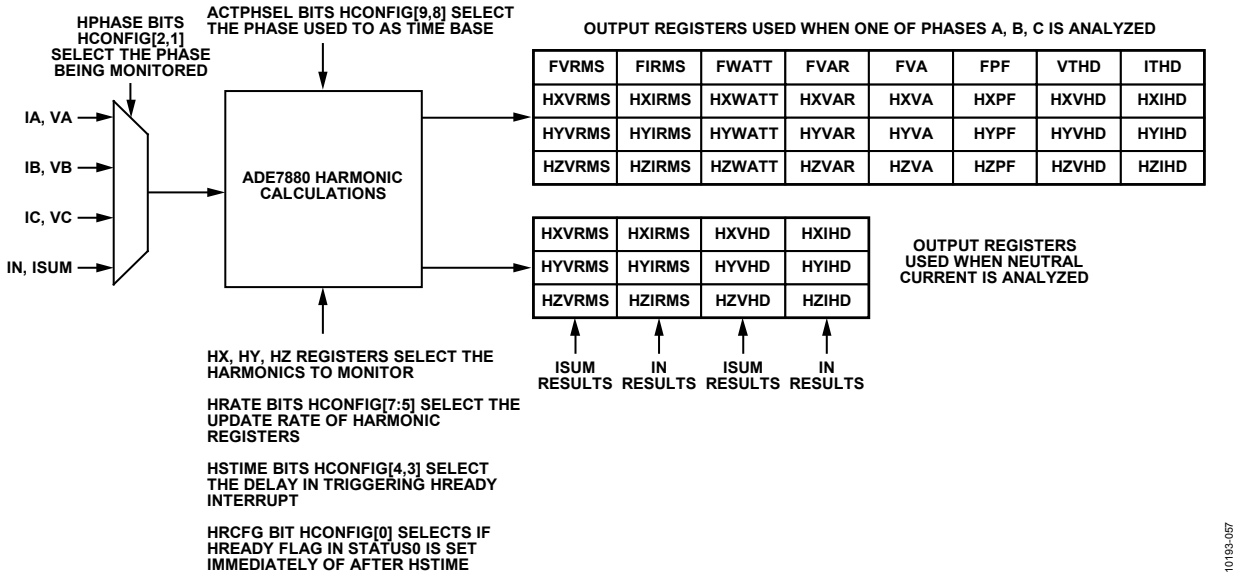

Figure 85. ADE7880 Harmonic Engine Block Diagram

When the neutral current and the sum of the three phase currents represented by ISUM register are analyzed, the following metering quantities are computed for both currents:

- RMS of fundamental and of up to 2 harmonics or rms of up to three harmonics: I_x, I_y, I_z, x, y, z = 1,2, 3,…, N.
- Harmonic distortions of the analyzed harmonics.

Configuring the Harmonic Calculations

The ADE7880 requires a time base provided by a phase voltage. Bit 9 and Bit 8 (ACTPHSEL) of HCONFIG[15:0]register select this phase voltage. If ACTPHSEL = 00, the phase A is used. If ACTPHSEL = 01, the Phase B is used and if ACTPHSEL = 10, the Phase C is used. If the phase voltage used as time base is down, select another phase, and the harmonic engine continues to work properly.

The phase under analysis is selected by Bit 2 and Bit 1 (HPHASE) of HCONFIG[15:0]register. If HPHASE = 00, the Phase A is monitored. If HPHASE = 01, the Phase B is monitored and if HPHASE = 10, the Phase C is monitored. If HPHASE = 11, the neutral current together with the sum of the phase currents represented by ISUM register are monitored.

Harmonic Calculations When a Phase is Monitored

When a phase is monitored, fundamental information together with information about up to three harmonics is computed. The indexes of the three additional harmonics simultaneously monitored by the ADE7880 are provided by the 8-bit registers HX, HY, and HZ. Simply write the index of the harmonic into the register for that harmonic to be monitored. If the second harmonic is monitored, write 2. If harmonic 51 is desired, write 51. The fundamental components are always monitored, independent of the values written into HX, HY, or HZ. Therefore, if one of these registers is made equal to 1, the ADE7880 monitors the fundamental components multiple times. The maximum index allowed in HX, HY, and HZ registers is 63. The no attenuation pass band is 2.8 kHz, corresponding to a −3 dB bandwidth of 3.3 kHz, thus all harmonics of frequency lower than 2800 Hz are supported without attenuation.

The rms of the phase voltage and phase current fundamental components are stored into FVRMS and FIRMS 24-bit signed registers. The associated data path is presented in Figure 86. Similar to the rms current and voltage rms data paths presented in the Root Mean Square Measurement section, the data path contains 24-bit signed offset compensation registers xIRMSOS, xVRMSOS, x = A, B, C for each phase quantity. The rms of the phase current and phase voltage three harmonic components are stored into HXVRMS, HXIRMS, HYVRMS, HYIRMS, HZVRMS, and HZIRMS 24-bit signed registers. The associated data path is presented in Figure 87 and contains the following 24-bit signed offset compensation registers: HXIRMSOS, HYIRMSOS, HZIRMSOS, HXVRMSOS, HYVRMSOS, and HZVRMSOS.

It is recommended to leave the offset compensation registers at 0, the default value.

Table 20. Harmonic Engine Outputs When Phase A, Phase B, or Phase C is Analyzed and the Registers Where the Values are Stored

Quantity	Definition	ADE7880 Register
RMS of the Fundamental Component	V1, I1	FVRMS, FIRMS
RMS of a Harmonic Component	V_x, I_x, x = 2, 3,…,N	HXVRMS, HXIRMS
	V_y, I_y, y = 2, 3,…,N	HYVRMS, HYIRMS
	V_z, I_z, z = 2, 3,…,N	HZVRMS, HZIRMS
Active Power of the Fundamental Component	$P_1 = V_1I_1\cos(\varphi_1 - \gamma_1)$	FWATT
Active Power of a Harmonic Component	$P_x = V_xI_x\cos(\varphi_x - \gamma_x)$, x = 2, 3,…,N	HXWATT
	$P_y = V_yI_y\cos(\varphi_y - \gamma_y)$, y = 2, 3,…,N	HYWATT
	$P_z = V_zI_z\cos(\varphi_z - \gamma_z)$, z = 2, 3,…,N	HZWATT
Reactive Power of the Fundamental Component	$Q_1 = V_1I_1\sin(\varphi_1 - \gamma_1)$	FVAR
Reactive Power of a Harmonic Component	$Q_x = V_xI_x\sin(\varphi_1 - \gamma_1)$, x = 2, 3,…,N	HXVAR
	$Q_y = V_yI_y\sin(\varphi_y - \gamma_y)$, y = 2, 3,…,N	HYVAR
	$Q_z = V_zI_z\sin(\varphi_z - \gamma_z)$, z = 2, 3,…,N	HZVAR
Apparent Power of the Fundamental Component	$S_1 = V_1I_1$	FVA
Apparent Power of a Harmonic Component	$S_x = V_xI_x$, x = 2, 3, …,N	HXVA
	$S_y = V_yI_y$, y = 2, 3, …,N	HYVA
	$S_z = V_zI_z$, z = 2, 3, …,N	HZVA
Power Factor of the Fundamental Component	$pf_1 = \frac{P_1}{S_1}$	FPF
Power Factor of a Harmonic Component	$pf_x = \frac{P_x}{S_x}$, x = 2, 3,…,N	HXPF
	$pf_y = \frac{P_y}{S_y}$, y = 2, 3,…,N	HYPF
	$pf_z = \frac{P_z}{S_z}$, z = 2, 3,…,N	HZPF
Total Harmonic Distortion	$(THD)_V = \frac{\sqrt{V^2 - V_1^2}}{V_1}$	VTHD
	$(THD)_I = \frac{\sqrt{I^2 - I_1^2}}{I_1}$	ITHD
Harmonic Distortion of a Harmonic Component	$HD_{V_x} = \frac{V_x}{V_1}$, $HD_{I_x} = \frac{I_x}{I_1}$, x = 2, 3,…,N	HXVHD, HXIHD
	$HD_{V_y} = \frac{V_y}{V_1}$, $HD_{I_y} = \frac{I_y}{I_1}$, y = 2, 3,…,N	HYVHD, HYIHD
	$HD_{V_z} = \frac{V_z}{V_1}$, $HD_{I_z} = \frac{I_z}{I_1}$, z = 2, 3,…,N	HZVHD, HZIHD

Table 21. Harmonic Engine Outputs when Neutral Current and ISUM are Analyzed and the Registers Where the Values are Stored

Quantity	Definition	ADE7880 Register
RMS of a Harmonic Component (Including the Fundamental) of the Neutral Current	I_x, x = 1, 2, 3,…,N	HXIRMS
	I_y, y = 1, 2, 3,…,N	HYIRMS
	I_z, z = 1, 2, 3,…,N	HZIRMS
RMS of a Harmonic Component (Including the Fundamental) of ISUM	ISUMx, x = 1, 2, 3,…,N	HXVRMS
	ISUMy, y = 1, 2, 3,…,N	HYVRMS
	ISUMz, z = 1, 2, 3,…,N	HZVRMS
Harmonic Distortion of a Harmonic Component (Including the Fundamental) of the Neutral Current (Note that the HX Register Must be Set to 1 for These Calculations to be Executed)	$HD_{I_x} = \frac{I_x}{I_1}$, x = 1, 2, 3,…,N	HXIHD
	$HD_{I_y} = \frac{I_y}{I_1}$, y = 1, 2, 3,…,N	HYIHD
	$HD_{I_z} = \frac{I_z}{I_1}$, z = 1, 2, 3,…,N	HZIHD
Harmonic Distortion of a Harmonic Component (Including the Fundamental) of ISUM. (Note that the HX Register Must be Set to 1 for These Calculations to be Executed)	$HD_{ISUM_x} = \frac{ISUM_x}{ISUM_1}$, x = 1, 2, 3,…,N	HXVHD
	$HD_{ISUM_y} = \frac{ISUM_y}{ISUM_1}$, y = 1, 2, 3,…,N	HYVHD
	$HD_{ISUM_z} = \frac{ISUM_z}{ISUM_1}$, z = 1, 2, 3,…,N	HZVHD

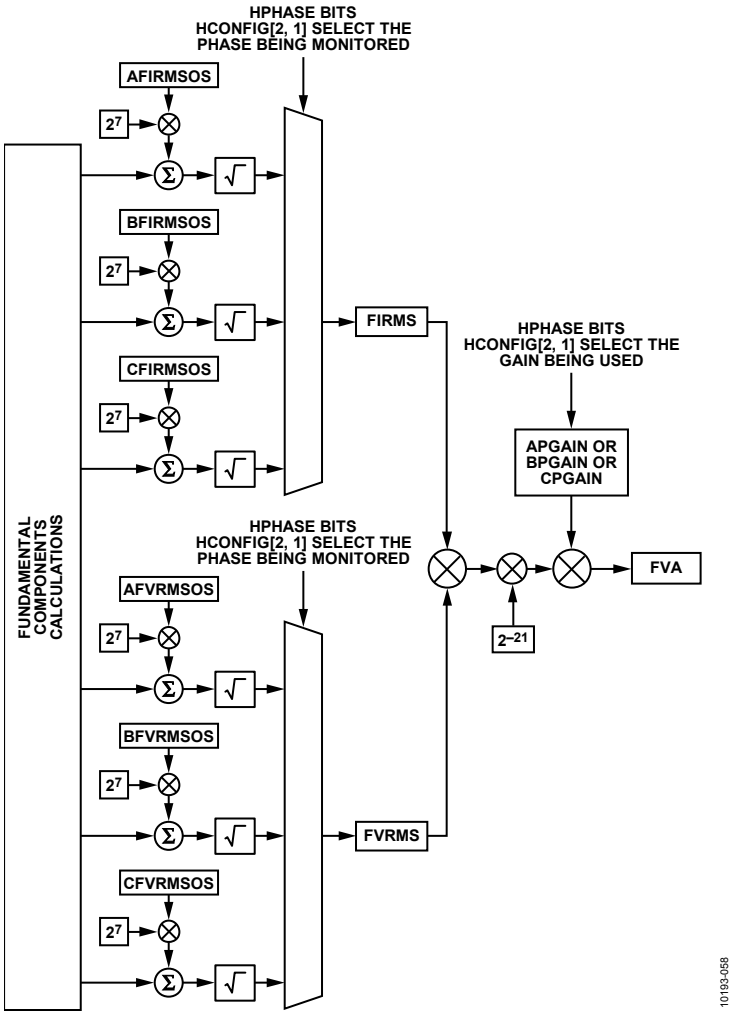

Figure 86. Fundamental RMS Signal Processing

The active, reactive, and apparent powers of the fundamental component are stored into the FWATT, FVAR, and FVA 24-bit signed registers. Figure 88 presents the associated data path. The active, reactive and apparent powers of the 3 harmonic components are stored into the HXWATT, HXVAR, HXVA, HYWATT, HYVAR, HYVA, HZWATT, HZVAR, and HZVA 24-bit signed registers. The HPGAIN register is a 24-bit signed register used to scale the output of the harmonic active, reactive and apparent power components, as shown in Figure 89. The 24-bit HPGAIN register is accessed as a 32-bit register with the four most significant bits (MSBs) padded with 0s and sign extended to 28 bits (See Figure 44 for details). HXWATTOS, HYWATTOS, HZWATTOS, HXVAROS, HYVAROS and HZVAROS are 24-bit offset compensation registers located in the active and reactive harmonic power data paths. Figure 89 presents the associated data path.

The power factor of the fundamental component is stored into FPF 24-bit signed register. The power factors of the three harmonic components are stored into the HXPF, HYPF, and HZPF 24-bit signed registers.

The total harmonic distortion ratios computed using the rms of the fundamental components and the rms of the phase current and the phase voltage (see Root Mean Square Chapter for details about these measurements) are stored into the VTHD and ITHD 24-bit registers in 3.21 signed format. This means the ratios are limited to +3.9999 and all greater results are clamped to it.

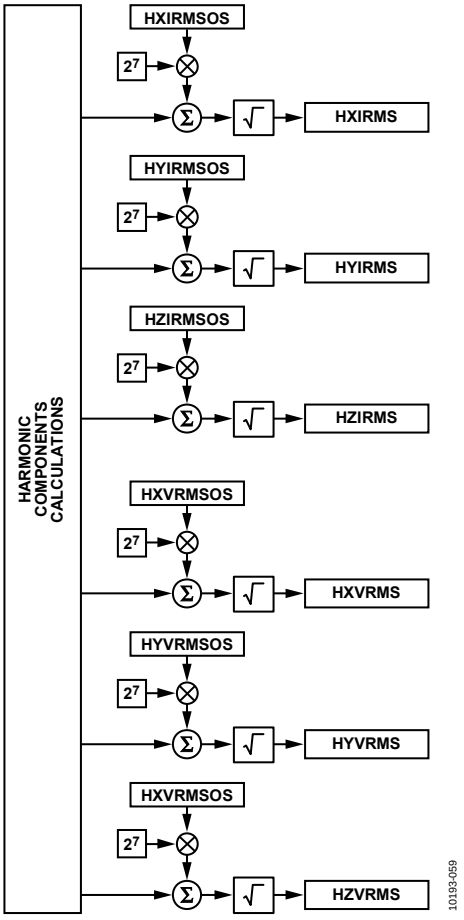

Figure 87. Harmonic RMS Signal Processing

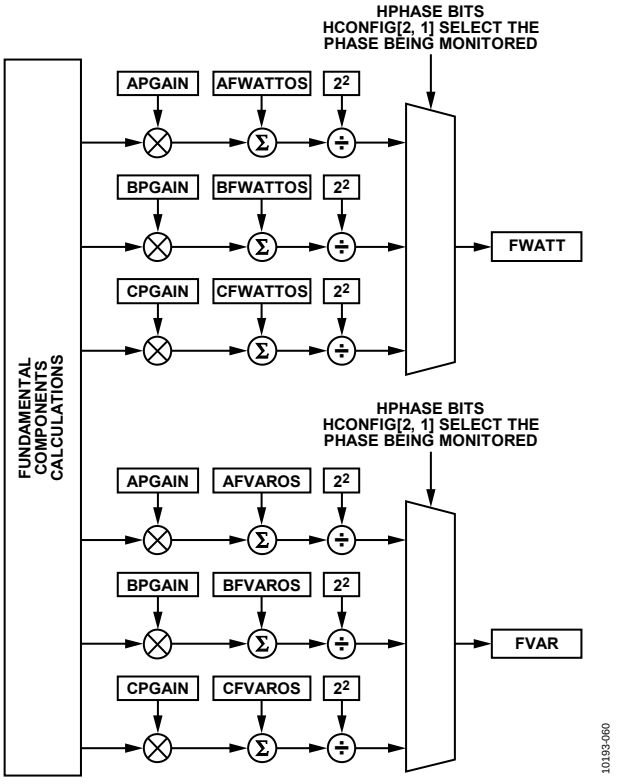

Figure 88. Fundamental Active and Reactive Powers Signal Processing

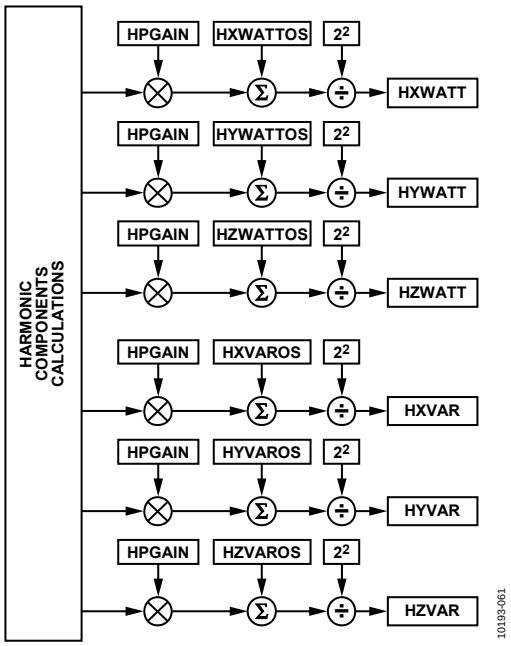

Figure 89. Harmonic Active and Reactive Powers Signal Processing

The harmonic distortions of the three harmonic components are stored into the HXVHD, HXIHD, HYVHD, HYIHD, HZVHD, and HZIHD 24-bit registers in 3.21 signed format. This means the ratios are limited to +3.9999 and all greater results are clamped to it.

As a reference, Table 20 presents the ADE7880 harmonic engine outputs when one phase is analyzed and the registers in which the outputs are stored.

Harmonic Calculations When the Neutral is Monitored

When the neutral current and the sum of phase currents are monitored, only the harmonic rms related registers are updated.

The registers HX, HY and HZ identify the index of the harmonic, including the fundamental. When a phase is analyzed, the fundamental rms values are calculated continuously and the results are stored in dedicated registers FIRMS and FVRMS. When the neutral is analyzed, the fundamental information is calculated by setting one of the harmonic index registers HX, HY or HZ to 1 and the results are stored in harmonic registers. The maximum index allowed in HX, HY and HZ registers is 63. The no attenuation pass band is 2.8 kHz, corresponding to a −3 dB bandwidth of 3.3 kHz, thus all harmonics of frequency lower than 2800 Hz are supported without attenuation.

HXIRMS, HYIRMS and HZIRMS registers contain the harmonic rms components of the neutral current and HXVRMS, HYVRMS and HZVRMS registers contain the harmonic rms components of ISUM. Note that in this case, the rms of the fundamental component is not computed into FIRMS or FVRMS registers, but it is computed if one of the index registers HX, HY and HZ is initialized with 1.

If the HX register is initialized to 1, the ADE7880 computes the harmonic distortions of the other harmonics identified into HY and HZ registers and stores them in 3.21 signed format into the HYVHD, HYIHD, HZVHD, and HZIHD 24-bit registers. The distortions of the neutral current are saved into HYIHD and HZIHD registers and the distortions of the ISUM are stored into the HYVHD and HZVHD registers. As HX is set to 1, the HXIHD and HXVHD registers contain 0x1FFFFF, a number representing 1 in 3.21 signed format.

As a reference, Table 21 presents the ADE7880 harmonic engine outputs when the neutral current and ISUM are analyzed and the registers in which the outputs are stored.

Configuring Harmonic Calculations Update Rate

The ADE7880 harmonic engine functions at 8 kHz rate. From the moment the HCONFIG register is initialized and the harmonic indexes are set in the HX, HY and HZ index registers, the ADE7880 calculations take typically 750 ms to settle within the specification parameters.

The update rate of the harmonic engine output registers is managed by Bits[7:5] (HRATE) in HCONFIG register and is independent of the engine's calculations rate of 8 kHz. The default value of 000 means the registers are updated every 125 µs (8 kHz rate). Other update periods are: 250 µs (HRATE = 001), 1 ms (010), 16 ms (011), 128 ms (100), 512 ms (101), 1.024 sec (110). If HRATE bits are 111, then the harmonic calculations are disabled.

The ADE7880 provides two ways to manage the harmonic computations. The first approach, enabled when Bit 0 (HRCFG) of HCONFIG register is cleared to its default value of 0, sets Bit 19 (HREADY) in STATUS0 register to 1 after a certain period of time and then every time the harmonic calculations are updated at HRATE frequency. This allows an external microcontroller to access the harmonic calculations only after they have settled. The time period is determined by the state of Bits[4:3] (HSTIME) in the HCONFIG register. The default value of 01 sets the time

to 750 ms, the settling time of the harmonic calculations. Other possible values are 500 ms (HSTIME = 00), 1 sec (10) and 1250 ms (11).

The second approach, enabled when Bit 0 (HRCFG) of HCONFIG register is set to 1, sets Bit 19 (HREADY) in STATUS0 register to 1 every time the harmonic calculations are updated at the update frequency determined by HRATE bits without waiting for the harmonic calculations to settle. This allows an external microcontroller to access the harmonic calculations immediately after they have been started. If the corresponding mask bit in the MASK0 interrupt mask register is enabled, the $\overline{\text{IRQ}}$ pin also goes active low. The status bit is cleared and the pin $\overline{\text{IRQ}}$ is set to high again by writing to the STATUS0 register with the corresponding bit set to 1.

Additionally, the ADE7880 provides a periodical output signal called HREADY at the CF2/HREADY pin synchronous to the moment the harmonic calculations are updated in the harmonic registers. This functionality is chosen if Bit 2 (CF2DIS) is set to 1 in the CONFIG register. If CF2DIS is set to 0 (default value), the CF2 energy to frequency converter output is provided at CF2/HREADY pin. The default state of this signal is high. Every time the harmonic registers are updated based on HRATE bits in HCONFIG register, the signal HREADY goes low for approximately 10 µs and then goes back high. If Bit 0 (HRCFG) in the HCONFIG register is set to 1, the HREADY bit in the STATUS0 register is set to 1 every HRATE period right after the harmonic calculations start, and the HREADY signal toggles high, low, and back synchronously. If the HRCFG bit is set to 0, the HREADY bit in the STATUS0 register is set to 1 after the HSTIME period, and the HREADY signal toggles high, low and back synchronously. The HREADY signal allows fast access to the harmonic registers without having to use HREADY interrupt in MASK0 register.

In order to facilitate the fast reading of the registers in which the harmonic calculations are stored, a special burst registers reading has been implemented in the serial interfaces. See the I²C Read Operation of Harmonic Calculations Registers and the SPI Read Operation sections for details.

Recommended Approach to Managing Harmonic Calculations

The recommended approach to managing the ADE7880 harmonic calculations is the following:

- Set up Bit 2 (CF2DIS) in the CONFIG register. Set the CF2DIS bit to 1 to use the CF2/HREADY pin to signal when the harmonic calculations have settled and are updated. The high to low transition of HREADY signal indicates when to read the harmonic registers. Use the burst reading mode to read the harmonic registers as it is the most efficient way to read them.
- Choose the harmonics to be monitored by setting HX, HY and HZ appropriately.
- Select all the HCONFIG register bits.
- Initialize the gain registers used in the harmonic calculations. Leave the offset registers to 0.
- Read the registers in which the harmonic information is stored using the burst or regular reading mode at high to low transitions of CF2/HREADY pin.

WAVEFORM SAMPLING MODE

The waveform samples of the current and voltage waveform, the active, reactive, and apparent power outputs are stored every 125 µs (8 kHz rate) into 24-bit signed registers that can be accessed through various serial ports of the ADE7880. Table 22 provides a list of registers and their descriptions.

Table 22. Waveform Registers List

Register	Description
IAWV	Phase A current
VAWV	Phase A voltage
IBWV	Phase B current
VBWV	Phase B voltage
ICWV	Phase C current
VCWV	Phase C voltage
INWV	Neutral current
AVA	Phase A apparent power
BVA	Phase B apparent power
CVA	Phase C apparent power
AWATT	Phase A active power
BWATT	Phase B active power
CWATT	Phase C active power

Bit 17 (DREADY) in the STATUS0 register can be used to signal when the registers listed in Table 22 can be read using I²C or SPI serial ports. An interrupt attached to the flag can be enabled by setting Bit 17 (DREADY) in the MASK0 register. (see the Digital Signal Processor section for more details on Bit DREADY).

The ADE7880 contains a high speed data capture (HSDC) port that is specially designed to provide fast access to the waveform sample registers. Read the HSDC Interface section for more details.

As stated in the Current Waveform Gain Registers section, the serial ports of the ADE7880 work on 32-, 16-, or 8-bit words. All registers listed in Table 22 are transmitted signed extended from 24 bits to 32 bits (see Figure 45).

ENERGY-TO-FREQUENCY CONVERSION

The ADE7880 provides three frequency output pins: CF1, CF2, and CF3. The CF2 pin is multiplexed with the HREADY pin of the harmonic calculations block. When HREADY is enabled, the CF2 functionality is disabled at the pin. The CF3 pin is multiplexed with the HSCLK pin of the HSDC interface. When HSDC is enabled, the CF3 functionality is disabled at the pin. The CF1 pin and the CF2 pin are always available. After initial calibration at manufacturing, the manufacturer or end customer verifies the energy meter calibration. One convenient way to verify the meter calibration is to provide an output frequency proportional to

the active, reactive, or apparent powers under steady load conditions. This output frequency can provide a simple, single-wire, optically isolated interface to external calibration equipment. Figure 90 illustrates the energy-to-frequency conversion in the ADE7880.

The DSP computes the instantaneous values of all phase powers: total active, fundamental active, fundamental reactive, and apparent. The process in which the energy is sign accumulated in various xWATTHR, xFVARHR, and xVAHR registers has already been described in the energy calculation sections: Active Energy Calculation, Fundamental Reactive Energy Calculation, and Apparent Energy Calculation. In the energy-to-frequency conversion process, the instantaneous powers generate signals at the frequency output pins (CF1, CF2, and CF3). One energy-to-frequency converter is used for every CFx pin. Every converter sums certain phase powers and generates a signal proportional to the sum. Two sets of bits decide what powers are converted.

First, Bits[2:0] (TERMSEL1[2:0]), Bits[5:3] (TERMSEL2[2:0]), and Bits[8:6] (TERMSEL3[2:0]) of the COMPMODE register decide which phases, or which combination of phases, are added.

The TERMSEL1 bits refer to the CF1 pin, the TERMSEL2 bits refer to the CF2 pin, and the TERMSEL3 bits refer to the CF3 pin. The TERMSELx[0] bits manage Phase A. When set to 1, Phase A power is included in the sum of powers at the CFx converter. When cleared to 0, Phase A power is not included. The TERMSELx[1] bits manage Phase B, and the TERMSELx[2] bits manage Phase C. Setting all TERMSELx bits to 1 means all 3-phase powers are added at the CFx converter. Clearing all TERMSELx bits to 0 means no phase power is added and no CF pulse is generated.

Second, Bits[2:0] (CF1SEL[2:0]), Bits[5:3] (CF2SEL[2:0]), and Bits[8:6] (CF3SEL[2:0]) in the CFMODE register decide what type of power is used at the inputs of the CF1, CF2, and CF3 converters, respectively. Table 23 shows the values that CFxSEL can have: total active, apparent, fundamental active, or fundamental reactive powers.

Table 23. CFxSEL Bits Description

CFxSEL	Description	Registers Latched When CFxLATCH = 1
000	CFx signal proportional to the sum of total phase active powers	AWATTHR, BWATTHR, CWATTHR
001	Reserved	
010	CFx signal proportional to the sum of phase apparent powers	AVAHR, BVAHR, CVAHR
011	CFx signal proportional to the sum of fundamental phase active powers	AFWATTHR, BFWATTHR, CFWATTHR
100	CFx signal proportional to the sum of fundamental phase reactive powers	AFVARHR, BFVARHR, CFVARHR
101 to 111	Reserved	

By default, the TERMSELx bits are all 1 and the CF1SEL bits are 000, the CF2SEL bits are 100, and the CF3SEL bits are 010. This means that by default, the CF1 digital-to-frequency converter produces signals proportional to the sum of all 3-phase total active powers, CF2 produces signals proportional to fundamental reactive powers, and CF3 produces signals proportional to apparent powers.

Similar to the energy accumulation process, the energy-to-frequency conversion is accomplished in two stages. The first stage is the same stage illustrated in the energy accumulation sections of active, reactive and apparent powers (see Active Energy Calculation, Fundamental Reactive Energy Calculation, Apparent Energy Calculation sections). The second stage consists of the frequency divider by the CFxDEN 16-bit unsigned registers. The values of CFxDEN depend on the meter constant (MC), measured in impulses/kWh and how much energy is assigned to one LSB of various energy registers: xWATTHR, xFVARHR, and so forth. Suppose a derivative of Wh [10^n Wh] where n is a positive or negative integer, is desired as one LSB of xWATTHR register. Then, CFxDEN is as follows:

$$CFxDEN = \frac{10^3}{MC[\text{imp/kwh}] \times 10^n} \quad (49)$$

The derivative of wh must be chosen in such a way to obtain a CFxDEN register content greater than 1. If CFxDEN = 1, then the CFx pin stays active low for only 1 µs. Thus, CFxDEN register must not be set to 1. The frequency converter cannot accommodate fractional results; the result of the division must be rounded to the nearest integer. If CFxDEN is set equal to 0, then the ADE7880 considers it to be equal to 1.

The CFx pulse output stays low for 80 ms if the pulse period is larger than 160 ms (6.25 Hz). If the pulse period is smaller than 160 ms and CFxDEN is an even number, the duty cycle of the pulse output is exactly 50%. If the pulse period is smaller than 160 ms and CFxDEN is an odd number, the duty cycle of the pulse output is

$$(1+1/CFxDEN) \times 50\%$$

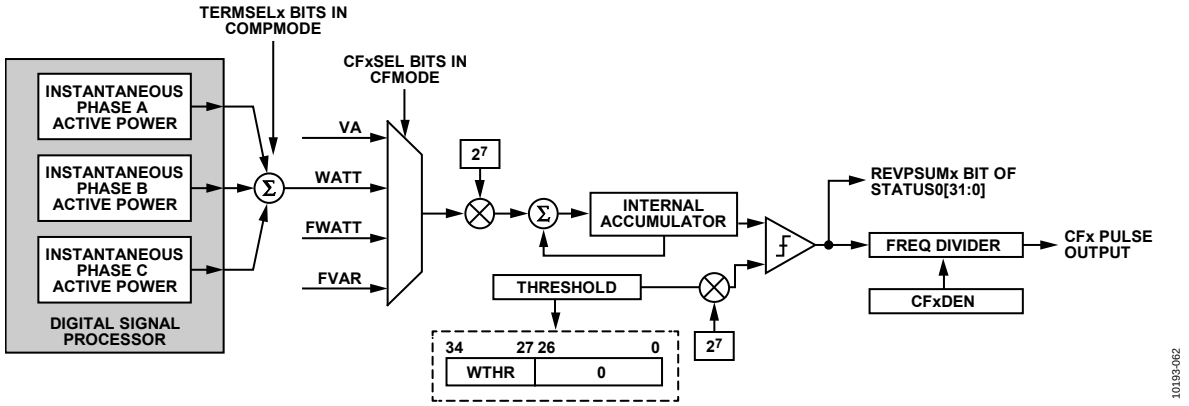

Figure 90. Energy-to-Frequency Conversion

The CFx pulse output is active low and preferably connected to an LED, as shown in Figure 91.

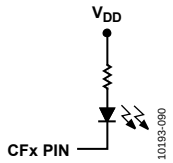

Figure 91. CFx Pin Recommended Connection

Bits[11:9] (CF3DIS, CF2DIS, and CF1DIS) of the CFMODE register decide if the frequency converter output is generated at the CF3, CF2, or CF1 pin. When Bit CFxDIS is set to 1 (the default value), the CFx pin is disabled and the pin stays high. When Bit CFxDIS is cleared to 0, the corresponding CFx pin output generates an active low signal.

Bits[16:14] (CF3, CF2, CF1) in the Interrupt Mask register MASK0 manage the CF3, CF2, and CF1 related interrupts. When the CFx bits are set, whenever a high-to-low transition at the corresponding frequency converter output occurs, an interrupt $\overline{\text{IRQ0}}$ is triggered and a status bit in the STATUS0 register is set to 1. The interrupt is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Synchronizing Energy Registers with CFx Outputs

The ADE7880 contains a feature that allows synchronizing the content of phase energy accumulation registers with the generation of a CFx pulse. When a high-to-low transition at one frequency converter output occurs, the content of all internal phase energy registers that relate to the power being output at CFx pin is latched into hour registers and then resets to 0. See Table 23 for the list of registers that are latched based on the CFxSEL[2:0] bits in the CFMODE register. All 3-phase registers are latched independent of the TERMSELx bits of the COMPMODE register. The process is shown in Figure 92 for CF1SEL[2:0] = 010 (apparent powers contribute at the CF1 pin) and CFCYC = 2.

The CFCYC 8-bit unsigned register contains the number of high to low transitions at the frequency converter output between two consecutive latches. Avoid writing a new value into the CFCYC register during a high-to-low transition at any CFx pin.

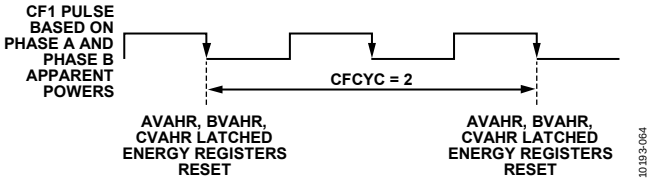

Figure 92. Synchronizing AVAHR and BVAHR with CF1

Bits[14:12] (CF3LATCH, CF2LATCH, and CF1LATCH) of the CFMODE register enable this process when set to 1. When cleared to 0, the default state, no latch occurs. The process is available even if the CFx output is not enabled by the CFxDIS bits in the CFMODE register.

Energy Registers and CF Outputs for Various Accumulation Modes

Bits[1:0] (WATTACC[1:0]) in the ACCMODE register determine the accumulation modes of the total and fundamental active powers when signals proportional to the active powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 000 or 011). They also determine the accumulation modes of the watt-hour energy registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR and CFWATTHR). When WATTACC[1:0] = 00 (the default value), the active powers are sign accumulated in the watt-hour registers and before entering the energy-to-frequency converter. Figure 93 shows how signed active power accumulation works. In this mode, the CFx pulses synchronize perfectly with the active energy accumulated in xWATTHR registers because the powers are sign accumulated in both data paths.

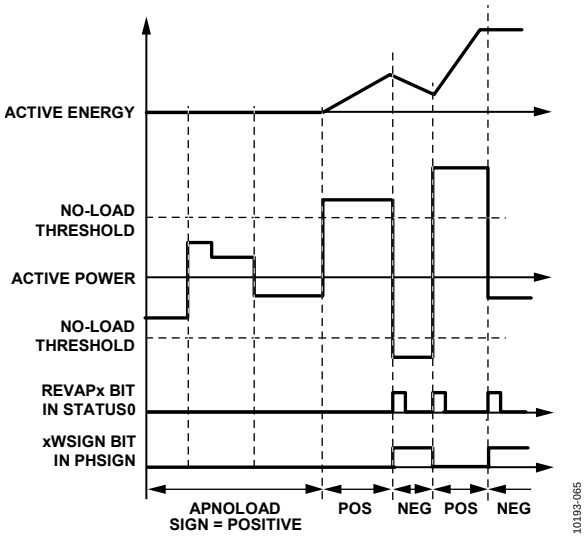

Figure 93. Active Power Signed Accumulation Mode

When WATTACC[1:0] = 01, the active powers are accumulated in positive only mode. When the powers are negative, the watt-hour energy registers are not accumulated. CFx pulses are generated based on signed accumulation mode. In this mode, the CFx pulses do not synchronize perfectly with the active energy accumulated in xWATTHR registers because the powers are accumulated differently in each data path. Figure 94 shows how positive only active power accumulation works.

WATTACC[1:0] = 10 setting is reserved and the ADE7880 behaves identically to the case when WATTACC[1:0] = 00.

When WATTACC[1:0] = 11, the active powers are accumulated in absolute mode. When the powers are negative, they change sign and accumulate together with the positive power in the watt-hour registers and before entering the energy-to-frequency converter. In this mode, the CFx pulses synchronize perfectly with the active energy accumulated in xWATTHR registers because the powers are accumulated in the same way in both data paths. Figure 95 shows how absolute active power accumulation works.

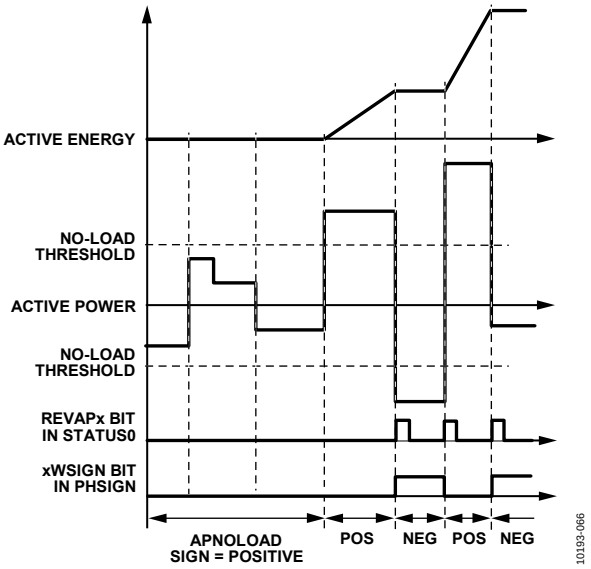

Figure 94. Active Power Positive Only Accumulation Mode

Bits[3:2] (VARACC[1:0]) in the ACCMODE register determine the accumulation modes of the fundamental reactive powers when signals proportional to the fundamental reactive powers are chosen at the CFx pins (the CFxSEL[2:0] bits in the CFMODE register equal 100). When VARACC[1:0] = 00, the default value, the fundamental reactive powers are sign accumulated in the var-hour energy registers and before entering the energy-to-frequency converter. Figure 96 shows how signed fundamental reactive power accumulation works. In this mode, the CFx pulses synchronize perfectly with the fundamental reactive energy accumulated in the xFVARHR registers because the powers are sign accumulated in both data paths.

VARACC[1:0] = 01 setting is reserved and ADE7880 behaves identically to the case when VARACC[1:0] = 00.

When VARACC[1:0] = 10, the fundamental reactive powers are accumulated depending on the sign of the corresponding active power in the var-hour energy registers and before entering the energy-to-frequency converter. If the fundamental active power is positive or considered 0 when lower than the no load threshold, the fundamental reactive power is accumulated as is. If the fundamental active power is negative, the sign of the fundamental reactive power is changed for accumulation. Figure 97 shows how the sign adjusted fundamental reactive power accumulation mode works. In this mode, the CFx pulses synchronize perfectly with the fundamental reactive energy accumulated in xFVARHR registers because the powers are accumulated in the same way in both data paths.

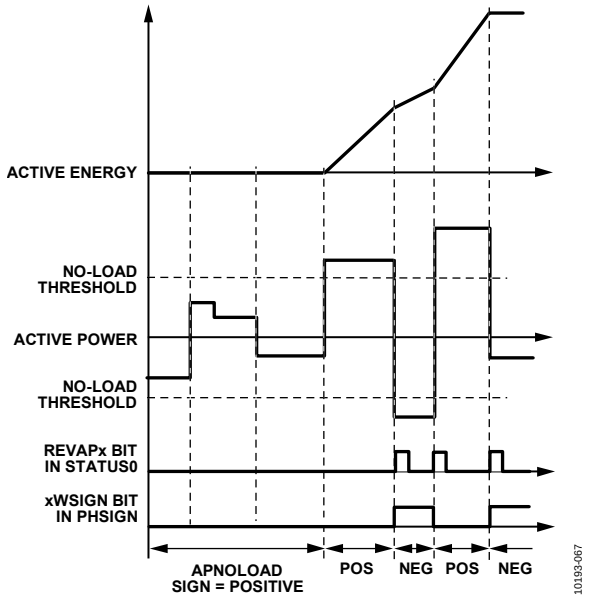

Figure 95. Active Power Absolute Accumulation Mode

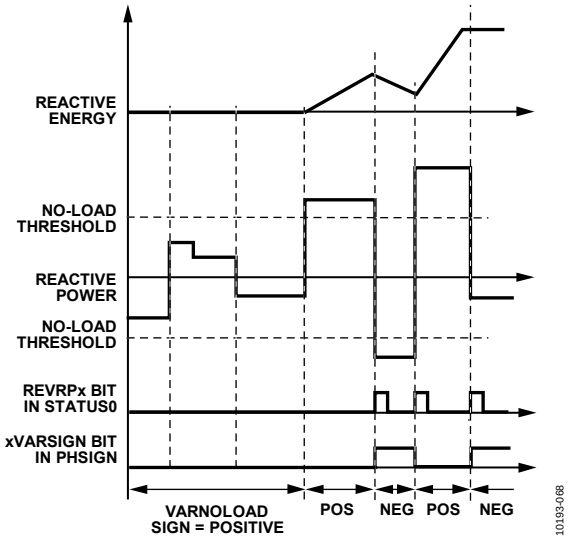

Figure 96. Fundamental Reactive Power Signed Accumulation Mode

When VARACC[1:0] = 11, the fundamental reactive powers are accumulated in absolute mode. When the powers are negative, they change sign and accumulate together with the positive power in the var-hour registers. CFx pulses are generated based on signed accumulation mode. In this mode, the CFx pulses do not synchronize perfectly with the fundamental reactive energy accumulated in x VARHR registers because the powers are accumulated differently in each data path. Figure 98 shows how absolute fundamental reactive power accumulation works.

Sign of Sum of Phase Powers in the CFx Data Path

The ADE7880 has sign detection circuitry for the sum of phase powers that are used in the CFx data path. As seen in the beginning of the Energy-to-Frequency Conversion section, the energy accumulation in the CFx data path is executed in two stages. Every time a sign change is detected in the energy accumulation at the end of the first stage, that is, after the energy accumulated

into the accumulator reaches one of the WTHR, VARTHR, or VATHR thresholds, a dedicated interrupt can be triggered synchronously with the corresponding CFx pulse. The sign of each sum can be read in the PHSIGN register.

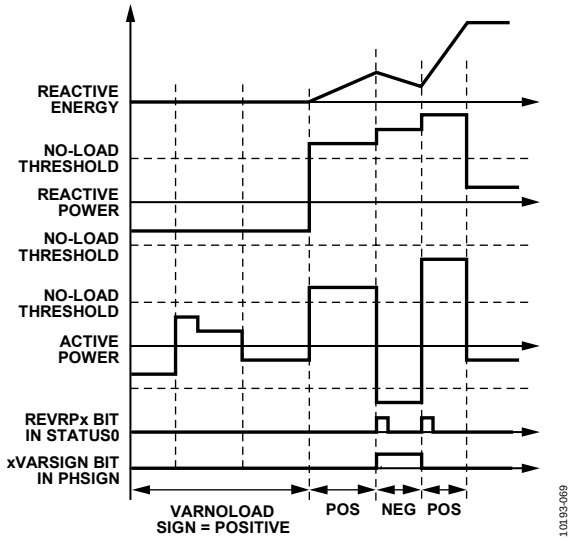

Figure 97. Fundamental Reactive Power Accumulation in Sign Adjusted Mode

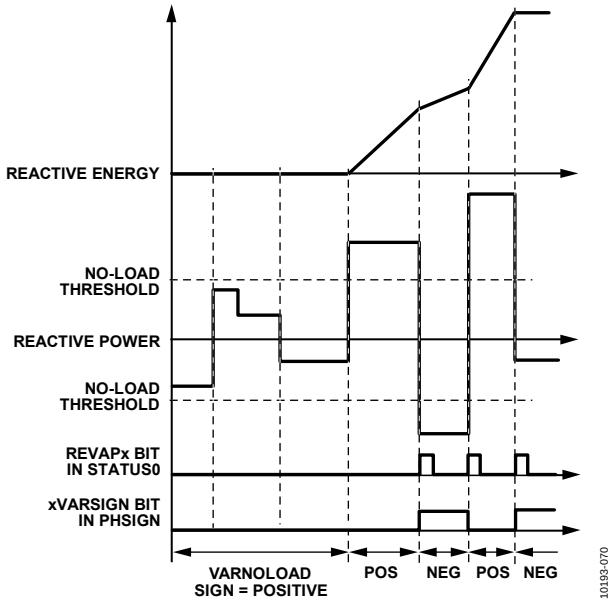

Figure 98. Fundamental Reactive Power Accumulation in Absolute Mode

Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) of the STATUS0 register are set to 1 when a sign change of the sum of powers in CF3, CF2, or CF1 data paths occurs. To correlate these events with the pulses generated at the CFx pins, after a sign change occurs, Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 are set in the same moment in which a high-to-low transition at the CF3, CF2, and CF1 pin, respectively, occurs.

Bit 8, Bit 7, and Bit 3 (SUM3SIGN, SUM2SIGN, and SUM1SIGN, respectively) of the PHSIGN register are set in the same moment with Bit REVPSUM3, Bit REVPSUM2, and Bit REVPSUM1 and indicate the sign of the sum of phase powers. When cleared to 0, the sum is positive. When set to 1, the sum is negative.

Interrupts attached to Bit 18, Bit 13, and Bit 9 (REVPSUM3, REVPSUM2, and REVPSUM1, respectively) in the STATUS0 register are enabled by setting Bit 18, Bit 13, and Bit 9 in the MASK0 register. If enabled, the $\overline{\text{IRQ0}}$ pin is set low, and the status bit is set to 1 whenever a change of sign occurs. To find the phase that triggered the interrupt, the PHSIGN register is read immediately after reading the STATUS0 register. Next, the status bit is cleared, and the $\overline{\text{IRQ0}}$ pin is set high again by writing to the STATUS0 register with the corresponding bit set to 1.

NO LOAD CONDITION

The no load condition is defined in metering equipment standards as occurring when the voltage is applied to the meter and no current flows in the current circuit. To eliminate any creep effects in the meter, the ADE7880 contains three separate no load detection circuits: one related to the total active power, one related to the fundamental active and reactive powers, and one related to the apparent powers.

No Load Detection Based On Total Active Power and Apparent Power

This no load condition uses the total active energy and the apparent energy to trigger this no load condition. The apparent energy is proportional to the rms values of the corresponding phase current and voltage. If neither total active energy nor apparent energy are accumulated for a time indicated in the respective APNOLOAD and VANOLOAD unsigned 16-bit registers, the no load condition is triggered, the total active energy of that phase is not accumulated and no CFx pulses are generated based on the total active energy.

The equations used to compute the APNOLOAD and VANOLOAD unsigned 16-bit values are

$$APNOLOAD = 2^{16} - \frac{Y \times WTHR \times 2^{17}}{PMAX}$$

$$VANOLOAD = 2^{16} - \frac{Y \times VATHR \times 2^{17}}{PMAX} \quad (50)$$

where:
Y is the required no load current threshold computed relative to full scale. For example, if the no load threshold current is set 10,000 times lower than full scale value, then Y = 10,000.

WTHR and VATHR represent values stored in the WTHR and VATHR registers and are used as the thresholds in the first stage energy accumulators for active and apparent energy, respectively (see Active Energy Calculation section). PMAX = 27,059,678 = 0x19CE5DE, the instantaneous active power computed when the ADC inputs are at full scale. Do not write 0xFFFF to the APNOLOAD and VANOLOAD registers.

The VANOLOAD register usually contains the same value as the APNOLOAD register. When APNOLOAD and VANOLOAD are set to 0x0, the no load detection circuit is disabled. If only VANOLOAD is set to 0, then the no load condition is triggered

based only on the total active power being lower than APNOLOAD. In the same way, if only APNOLOAD is set to 0x0, the no load condition is triggered based only on the apparent power being lower than VANOLOAD.

Bit 0 (NLOAD) in the STATUS1 register is set when a no load condition in one of the three phases is triggered. Bits[2:0] (NLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit NLOAD in the STATUS1 register. NLPHASE[0] indicates the state of Phase A, NLPHASE[1] indicates the state of Phase B, and NLPHASE[2] indicates the state of Phase C. When Bit NLPHASE[x] is cleared to 0, it means the phase is out of a no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to Bit 0 (NLOAD) in the STATUS1 register can be enabled by setting Bit 0 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set to low, and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Fundamental Active and Reactive Powers

This no load condition is triggered when no less significant bits are accumulated into the fundamental active and reactive energy registers on one phase (xFWATTHR and xFVARHR, x = A, B, or C) for a time indicated in the respective APNOLOAD and VARNOLOAD unsigned 16-bit registers. In this case, the fundamental active and reactive energies of that phase are not accumulated and no CFx pulses are generated based on these energies. APNOLOAD is the same no load threshold set for the total active powers. The VARNOLOAD register usually contains the same value as the APNOLOAD register. If only APNOLOAD is set to 0x0, then the fundamental active power is accumulated without restriction. In the same way, if only VARNOLOAD is set to 0x0, the fundamental reactive power is accumulated without restriction. As with the APNOLOAD and VANOLOAD registers, do not write 0xFFFF to the VARNOLOAD register.

Bit 1 (FNLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[5:3] (FNLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and are set simultaneously with Bit FNLOAD in the STATUS1 register. FNLPHASE[0] indicates the state of Phase A, FNLPHASE[1] indicates the state of Phase B, and FNLPHASE[2] indicates the state of Phase C. When Bit FNLPHASE[x] is cleared to 0, it means the phase is out of the no load condition. When set to 1, it means the phase is in a no load condition.

An interrupt attached to the Bit 1 (FNLOAD) in the STATUS1 register can be enabled by setting Bit 1 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Then the status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set back high by writing to the STATUS1 register with the corresponding bit set to 1.

No Load Detection Based on Apparent Power

This no load condition is triggered when no less significant bits are accumulated into the apparent energy register on one phase (xVAHR, x = A, B, or C) for a time indicated by the VANOLOAD unsigned 16-bit register. In this case, the apparent energy of that phase is not accumulated and no CFx pulses are generated based on this energy.

The equation used to compute the VANOLOAD unsigned 16-bit value is

$$VANOLOAD = 2^{16} - \frac{Y \times VATHR \times 2^{17}}{PMAX} \quad (51)$$

where:

Y is the required no load current threshold computed relative to full scale. For example, if the no load threshold current is set 10,000 times lower than full scale value, then Y=10,000.

VATHR is the VATHR register used as the threshold of the first stage energy accumulator (see Apparent Energy Calculation section) PMAX = 27,059,678 = 0x19CE5DE, the instantaneous apparent power computed when the ADC inputs are at full scale. When the VANOLOAD register is set to 0x0, the no load detection circuit is disabled.

Bit 2 (VANLOAD) in the STATUS1 register is set when this no load condition in one of the three phases is triggered. Bits[8:6] (VANLPHASE[2:0]) in the PHNOLOAD register indicate the state of all phases relative to a no load condition and they are set simultaneously with Bit VANLOAD in the STATUS1 register:

- Bit VANLPHASE[0] indicates the state of Phase A.
- Bit VANLPHASE[1] indicates the state of Phase B.
- Bit VANLPHASE[2] indicates the state of Phase C.

When Bit VANLPHASE[x] is cleared to 0, it means the phase is out of no load condition. When set to 1, it means the phase is in no load condition.

An interrupt attached to Bit 2 (VANLOAD) in the STATUS1 register is enabled by setting Bit 2 in the MASK1 register. If enabled, the $\overline{\text{IRQ1}}$ pin is set low and the status bit is set to 1 whenever one of three phases enters or exits this no load condition. To find the phase that triggered the interrupt, the PHNOLOAD register is read immediately after reading the STATUS1 register. Next, the status bit is cleared, and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the corresponding bit set to 1.

CHECKSUM REGISTER

The ADE7880 has a checksum 32-bit register, CHECKSUM, that ensures the configuration registers maintain their desired value during Normal Power Mode PSM0.

The registers covered by this register are MASK0, MASK1, COMPMODE, gain, CFMODE, CF1DEN, CF2DEN, CF3DEN, CONFIG, MMODE, ACCMODE, LCYCMODE, HSDC_CFG, all registers located in the DSP data memory RAM between Address 0x4380 and Address 0x43BE, and another eight 8-bit reserved internal registers that always have default values. The ADE7880 computes the cyclic redundancy check (CRC) based on the IEEE802.3 standard. The registers are introduced one-by-one into a linear feedback shift register (LFSR) based generator starting with the least significant bit (as shown in Figure 99). The 32-bit result is written in the CHECKSUM register. After power-up or a hardware/software reset, the CRC is computed on the default values of the registers giving a result equal to 0xAFFA63B9.

Figure 100 shows how the LFSR works: the MASK0, MASK1, COMPMODE, Gain, CFMODE, CF1DEN, CF2DEN, CF3DEN, CONFIG, MMODE, ACCMODE, LCYCMODE, and HSDC_CFG registers, the registers located between Address 0x4380, and Address 0x43BE and the eight 8-bit reserved internal registers form the bits [a_{2271}, a_{2270},…, a_0] used by LFSR. Bit a_0 is the least significant bit of the first register to enter LFSR; Bit a_{2271} is the most significant bit of the last register to enter LFSR. The formulas that govern LFSR are as follows:

- $b_i(0) = 1$, i = 0, 1, 2, …, 31, the initial state of the bits that form the CRC. Bit b_0 is the least significant bit, and Bit b_{31} is the most significant.
- g_i, i = 0, 1, 2, …, 31 are the coefficients of the generating polynomial defined by the IEEE802.3 standard as follows:

$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (52)$$

$$g_0 = g_1 = g_2 = g_4 = g_5 = g_7 = 1$$
$$g_8 = g_{10} = g_{11} = g_{12} = g_{16} = g_{22} = g_{23} = g_{26} = 1 \quad (53)$$

All of the other g_i coefficients are equal to 0.

$$FB(j) = a_{j-1} \text{ XOR } b_{31}(j-1) \quad (54)$$

$$b_0(j) = FB(j) \text{ AND } g_0 \quad (55)$$

$$b_i(j) = FB(j) \text{ AND } g_i \text{ XOR } b_{i-1}(j-1),\ i = 1, 2, 3, ..., 31 \quad (56)$$

Equation 54, Equation 55, and Equation 56 must be repeated for j = 1, 2, …, 2272. The value written into the CHECKSUM register contains the Bit $b_i(2272)$, i = 0, 1, …, 31.

Every time a configuration register of the ADE7880 is written or changes value inadvertently, the Bit 25 (CRC) in STATUS1 register is set to 1 to signal CHECKSUM value has changed. If Bit 25 (CRC) in MASK1 register is set to 1, then the $\overline{\text{IRQ1}}$ interrupt pin is driven low and the status flag CRC in STATUS1 is set to 1. The status bit is cleared and the $\overline{\text{IRQ1}}$ pin is set to high by writing to the STATUS1 register with the status bit set to 1.

When Bit CRC in STATUS1 is set to 1 without any register being written, it can be assumed that one of the registers has changed value and therefore, the ADE7880 has changed configuration. The recommended response is to initiate a hardware/software reset that sets the values of all registers to the default, including the reserved ones, and then reinitialize the configuration registers.

Bit 3 of the internal configuration register at Address 0xE7E4 determines if the checksum feature is enabled or disabled. If the bit is set, which is the default state, the checksum functionality works as expected. Though the register is write protected, it is important to ensure that the bit remains set while working with this feature. If for any reason the bit gets reset to 0, the checksum functionality no longer works. Resetting the chip sets the bit to 1 again.

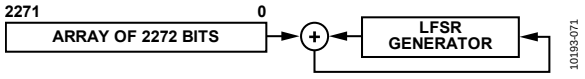

Figure 99. CHECKSUM Register Calculation

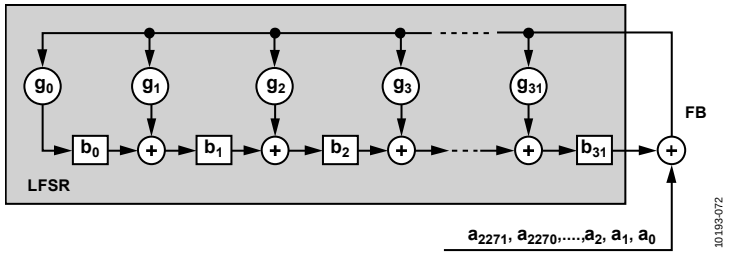

Figure 100. LFSR Generator Used in CHECKSUM Register Calculation

INTERRUPTS

The ADE7880 has two interrupt pins, $\overline{\text{IRQ0}}$ and $\overline{\text{IRQ1}}$. Each of the pins is managed by a 32-bit interrupt mask register, MASK0 and MASK1, respectively. To enable an interrupt, a bit in the MASKx register must be set to 1. To disable it, the bit must be cleared to 0. Two 32-bit status registers, STATUS0 and STATUS1, are associated with the interrupts. When an interrupt event occurs in the ADE7880, the corresponding flag in the interrupt status register is set to a logic 1 (see Table 36 and Table 37). If the mask bit for this interrupt in the interrupt mask register is logic 1, then the $\overline{\text{IRQx}}$ logic output goes active low. The flag bits in the interrupt status register are set irrespective of the state of the mask bits. To determine the source of the interrupt, the MCU must perform a read of the corresponding STATUSx register and identify which bit is set to 1. To erase the flag in the status register, write back to the STATUSx register with the flag set to 1. After an interrupt pin goes low, the status register is read and the source of the interrupt is identified. Then, the status register is written back without any change to clear the status flag to 0. The $\overline{\text{IRQx}}$ pin remains low until the status flag is cancelled.

By default, all interrupts are disabled. However, the RSTDONE interrupt is an exception. This interrupt can never be masked (disabled) and, therefore, Bit 15 (RSTDONE) in the MASK1 register does not have any functionality. The $\overline{\text{IRQ1}}$ pin always goes low, and Bit 15 (RSTDONE) in the STATUS1 register is set to 1 whenever a power-up or a hardware/software reset process ends. To cancel the status flag, the STATUS1 register has to be written with Bit 15 (RSTDONE) set to 1.

Certain interrupts are used in conjunction with other status registers. The following bits in the MASK1 register work in conjunction with the status bits in the PHNOLOAD register:

- Bit 0 (NLOAD)
- Bit 1 (FNLOAD)
- Bit 2 (VANLOAD)

The following bits in the MASK1 register work with the status bits in the PHSTATUS register:

- Bit 16, (SAG)
- Bit 17 (OI)
- Bit 18 (OV)

The following bits in the MASK1 register work with the status bits in the IPEAK and VPEAK registers, respectively:

- Bit 23 (PKI)
- Bit 24 (PKV)

The following bits in the MASK0 register work with the status bits in the PHSIGN register:

- Bits[6:8] (REVAPx)
- Bits[10:12] (REVRPx)
- Bit 9, Bit 13, and Bit 18 (REVPSUMx)

When the STATUSx register is read and one of these bits is set to 1, the status register associated with the bit is immediately read to identify the phase that triggered the interrupt and only at that time can the STATUSx register be written back with the bit set to 1.

Using the Interrupts with an MCU

Figure 101 shows a timing diagram that illustrates a suggested implementation of the ADE7880 interrupt management using an MCU. At Time t_1, the $\overline{\text{IRQx}}$ pin goes active low indicating that one or more interrupt events have occurred in the ADE7880, at which point, take the following steps:

1. Tie the $\overline{\text{IRQx}}$ pin to a negative-edge-triggered external interrupt on the MCU.
2. On detection of the negative edge, configure the MCU to start executing its interrupt service routine (ISR).
3. On entering the ISR, disable all interrupts using the global interrupt mask bit. At this point, the MCU external interrupt flag can be cleared to capture interrupt events that occur during the current ISR.
4. When the MCU interrupt flag is cleared, a read from STATUSx, the interrupt status register, is carried out. The interrupt status register content is used to determine the source of the interrupt(s) and, therefore, the appropriate action to be taken.
5. The same STATUSx content is written back into the ADE7880 to clear the status flag(s) and reset the $\overline{\text{IRQx}}$ line to logic high (t_2).

If a subsequent interrupt event occurs during the ISR (t_3), that event is recorded by the MCU external interrupt flag being set again.

On returning from the ISR, the global interrupt mask bit is cleared (same instruction cycle) and the external interrupt flag uses the MCU to jump to its ISR once again. This ensures that the MCU does not miss any external interrupts.

Figure 102 shows a recommended timing diagram when the status bits in the STATUSx registers work in conjunction with bits in other registers. When the $\overline{\text{IRQx}}$ pin goes active low, the STATUSx register is read, and if one of these bits is 1, a second status register is read immediately to identify the phase that triggered the interrupt. The name, PHx, in Figure 102 denotes one of the PHSTATUS, IPEAK, VPEAK, or PHSIGN registers. Then, STATUSx is written back to clear the status flag(s).

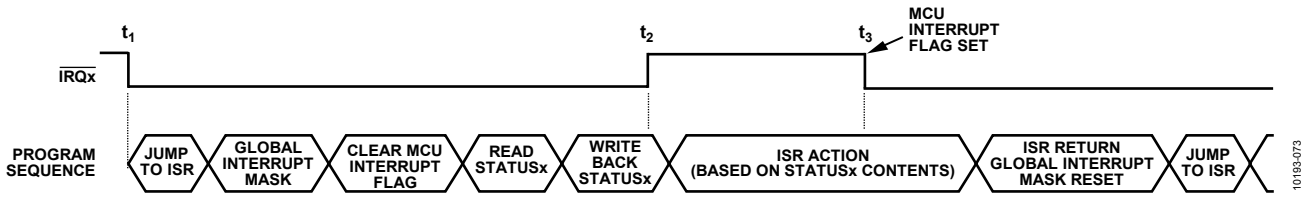

Figure 101. Interrupt Management

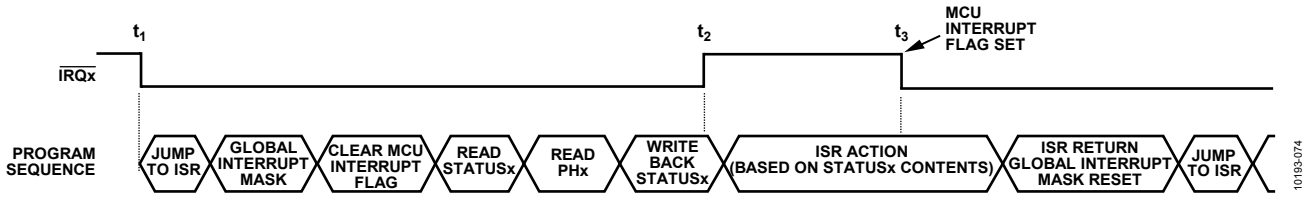

Figure 102. Interrupt Management when PHSTATUS, IPEAK, VPEAK, or PHSIGN Registers are Involved

SERIAL INTERFACES

The ADE7880 has three serial port interfaces: one fully licensed I²C interface, one serial peripheral interface (SPI), and one high speed data capture port (HSDC). As the SPI pins are multiplexed with some of the pins of the I²C and HSDC ports, the ADE7880 accepts two configurations: one using the SPI port only and one using the I²C port in conjunction with the HSDC port.

Serial Interface Choice

After reset, the HSDC port is always disabled. Choose between the I²C and SPI ports by manipulating the $\overline{SS}$/HSA pin after power-up or after a hardware reset. If the $\overline{SS}$/HSA pin is kept high, then the ADE7880 uses the I²C port until a new hardware reset is executed. If the $\overline{SS}$/HSA pin is toggled high to low three times after power-up or after a hardware reset, the ADE7880 uses the SPI port until a new hardware reset is executed. This manipulation of the $\overline{SS}$/HSA pin can be accomplished in two ways. First, use the $\overline{SS}$/HSA pin of the master device (that is, the microcontroller) as a regular I/O pin and toggle it three times. Second, execute three SPI write operations to a location in the address space that is not allocated to a specific ADE7880 register (for example 0xEBFF, where eight bit writes can be executed). These writes allow the $\overline{SS}$/HSA pin to toggle three times. See the SPI Write Operation section for details on the write protocol involved.

After the serial port choice is completed, it needs to be locked. Consequently, the active port remains in use until a hardware reset is executed in PSM0 normal mode or until a power-down. If I²C is the active serial port, Bit 1 (I2C_LOCK) of the CONFIG2 register must be set to 1 to lock it in. From this moment, the ADE7880 ignores spurious toggling of the $\overline{SS}$ pin and an eventual switch into using the SPI port is no longer possible. If the SPI is the active serial port, any write to the CONFIG2 register locks the port. From this moment, a switch into using the I²C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7880 changes PSMx power modes.

The functionality of the ADE7880 is accessible via several on-chip registers. The contents of these registers can be updated or read using either the I²C or SPI interfaces. The HSDC port provides the state of up to 16 registers representing instantaneous values of phase voltages and neutral currents, and active, reactive, and apparent powers.

Communication Verification

The ADE7880 includes a set of three registers that allow any communication via I²C or SPI to be verified. The LAST_OP (Address 0xEA01), LAST_ADD (Address 0xE9FE) and LAST_RWDATA registers record the nature, address and data of the last successful communication respectively. The LAST_RWDATA register has three separate addresses depending on the length of the successful communication.

Table 24. LAST_RWDATA Register Locations

Communication Type	Address
8-Bit Read/Write	0xE7FD
16-Bit Read/Write	0xE9FF
32-Bit Read/Write	0xE5FF

After each successful communication with the ADE7880, the address of the last accessed register is stored in the 16-bit LAST_ADD register (Address 0xE9FE). This is a read only register that stores the value until the next successful read or write is complete. The LAST_OP register (Address 0xEA01) stores the nature of the operation. That is, it indicates whether a read or a write was performed. If the last operation is a write, the LAST_OP register stores the value 0xCA. If the last operation is a read, the LAST_OP register stores the value 0x35. The LAST_RWDATA register stores the data that was written or read from the register. Any unsuccessful read or write operation is not reflected in these registers.

When LAST_OP, LAST_ADD and LAST_RWDATA registers are read, their values are not stored into themselves.

I²C-Compatible Interface

The ADE7880 supports a fully licensed I²C interface. The I²C interface is implemented as a full hardware slave. SDA is the data I/O pin, and SCL is the serial clock. These two pins are shared with the MOSI and SCLK pins of the on-chip SPI interface. The maximum serial clock frequency supported by this interface is 400 kHz.

The two pins used for data transfer, SDA and SCL, are configured in a wire-AND'ed format that allows arbitration in a multimaster system. Note that the ADE7880 requires a minimum of 100 ns hold time for I²C communication. Refer to the $t_{HD;DAT}$ specification in Table 2.

The transfer sequence of an I²C system consists of a master device initiating a transfer by generating a start condition while the bus is idle. The master transmits the address of the slave device and the direction of the data transfer in the initial address transfer. If the slave acknowledges, the data transfer is initiated. This continues until the master issues a stop condition, and the bus becomes idle.

I²C Write Operation

The write operation using the I²C interface of the ADE7880 initiate when the master generates a start condition and consists in one byte representing the address of the ADE7880 followed by the 16-bit address of the target register and by the value of the register.

The most significant seven bits of the address byte constitute the address of the ADE7880 and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a write operation, it has to be cleared to 0; therefore, the first byte of the write operation is 0x70. After every byte is received, the ADE7880 generates an acknowledge. As registers can have 8, 16, or 32 bits, after the last bit of the register is transmitted and the ADE7880 acknowledges the transfer, the master generates a stop condition. The addresses and the register content are sent with the most significant bit first. See Figure 103 for details of the I²C write operation.

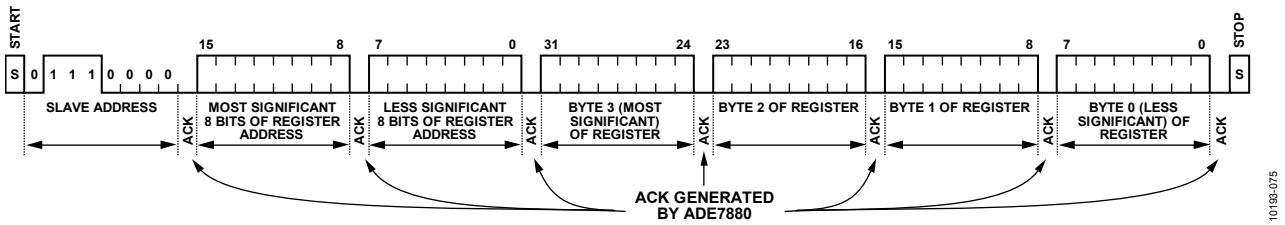

Figure 103. I²C Write Operation of a 32-Bit Register

I²C Read Operation

The read operation using the I²C interface of the ADE7880 is accomplished in two stages. The first stage sets the pointer to the address of the register. The second stage reads the content of the register.

As seen in Figure 104, the first stage initiates when the master generates a start condition and consists in one byte representing the address of the ADE7880 followed by the 16-bit address of the target register. The ADE7880 acknowledges every byte received. The address byte is similar to the address byte of a write operation and is equal to 0x70 (see the I²C Write Operation section for details). After the last byte of the register address is sent and acknowledged by the ADE7880, the second stage begins with the master generating a new start condition followed by an address byte. The most significant seven bits of this address byte constitute the address of the ADE7880, and they are equal to 0111000b. Bit 0 of the address byte is a read/write bit. Because this is a read operation, it must be set to 1; thus, the first byte of the read operation is 0x71. After this byte is received, the ADE7880 generates an acknowledge. Then, the ADE7880 sends the value of the register, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. Because registers can have 8, 16, or 32 bits, after the last bit of the register is received, the master does not acknowledge the transfer but generates a stop condition.

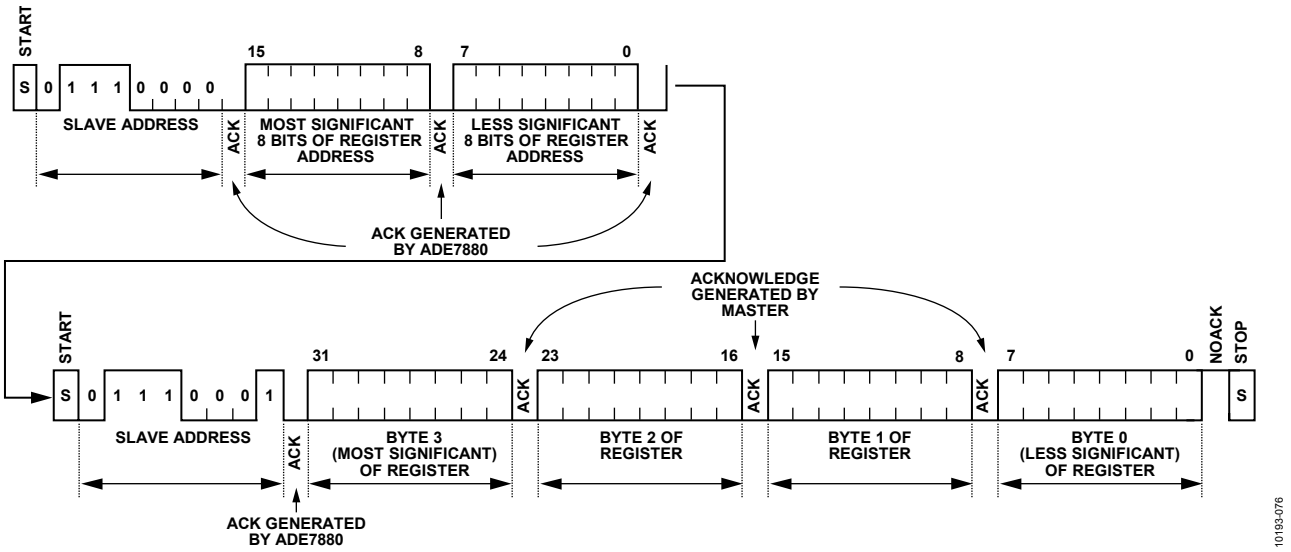

Figure 104. I²C Read Operation of a 32-Bit Register

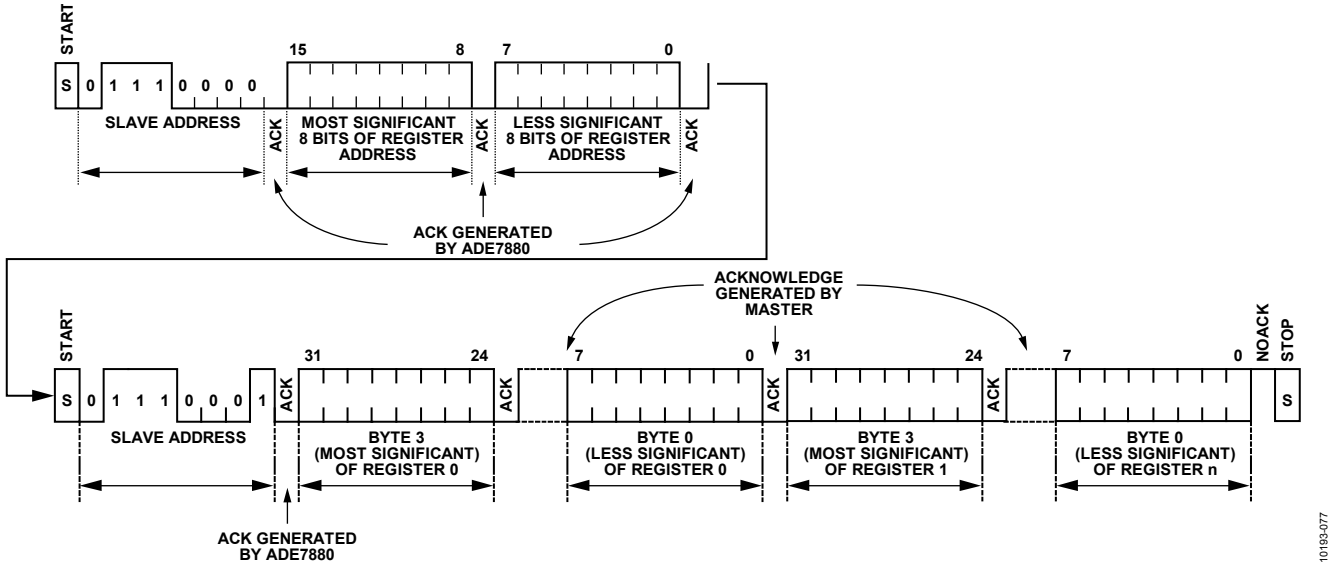

Figure 105. I²C Read Operation of n 32-Bit Harmonic Calculations Registers

I²C Read Operation of Harmonic Calculations Registers

The registers containing the harmonic calculation results are located starting at Address 0xE880 and are all 32-bit width. They can be read in two ways: one register at a time (see the I²C Read Operation section for details) or multiple consecutive registers at a time in a burst mode. This burst mode is accomplished in two stages. As seen in Figure 105, the first stage sets the pointer to the address of the register and is identical to the first stage executed when only one register is read. The second stage reads the content of the registers. The second stage begins with the master generating a new start condition followed by an address byte equal to the address byte used when one single register is read, 0x71. After this byte is received, the ADE7880 generates an acknowledge. Then, the ADE7880 sends the value of the first register located at the pointer, and after every eight bits are received, the master generates an acknowledge. All the bytes are sent with the most significant bit first. After the bytes of the first register are sent, if the master acknowledges the last byte, the ADE7880 increments the pointer by one location to position it at the next register and begins to send it out byte by byte, most significant bit first. If the master acknowledges the last byte, the ADE7880 increments the pointer again and begins to send data from the next register. The process continues until the master ceases to generate an acknowledge at the last byte of the register and then generates a stop condition. It is recommended to not allow locations greater than 0xE89F, the last location of the harmonic calculations registers.

SPI-Compatible Interface

The SPI of the ADE7880 is always a slave of the communication and consists of four pins (with dual functions): SCLK/SCL, MOSI/SDA, MISO/HSD, and $\overline{SS}$/HSA. The functions used in the SPI-compatible interface are SCLK, MOSI, MISO, and $\overline{SS}$. The serial clock for a data transfer is applied at the SCLK logic input. All data transfer operations synchronize to the serial clock. Data shifts into the ADE7880 at the MOSI logic input on the falling edge of SCLK and the ADE7880 samples it on the rising edge of SCLK. Data shifts out of the ADE7880 at the MISO logic output on a falling edge of SCLK and can be sampled by the master device on the raising edge of SCLK. The most significant bit of the word is shifted in and out first. The maximum serial clock frequency supported by this interface is 2.5 MHz. MISO stays in high impedance when no data is transmitted from the ADE7880. See Figure 106 for details of the connection between the ADE7880 SPI and a master device containing an SPI interface.

The $\overline{SS}$ logic input is the chip select input. This input is used when multiple devices share the serial bus. Drive the $\overline{SS}$ input low for the entire data transfer operation. Bringing $\overline{SS}$ high during a data transfer operation aborts the transfer and places the serial bus in a high impedance state. A new transfer can then be initiated by returning the $\overline{SS}$ logic input to low. However, because aborting a data transfer before completion leaves the accessed register in a state that cannot be guaranteed, every time a register is written, verify its value by reading it back. The protocol is similar to the protocol used in I²C interface.

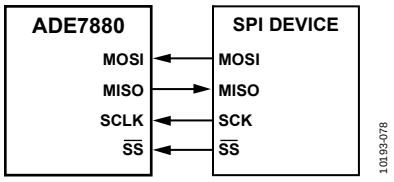

Figure 106. Connecting ADE7880 SPI with an SPI Device

SPI Read Operation

The read operation using the SPI interface of the ADE7880 initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7880, on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, it is recommended they be different from 0111000b, the seven bits used in the I²C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be 1 for a read operation. Next, the master sends the 16-bit address of the register that is read. After the ADE7880 receives the last bit of address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit, it sets the $\overline{SS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 107 for details of the SPI read operation.

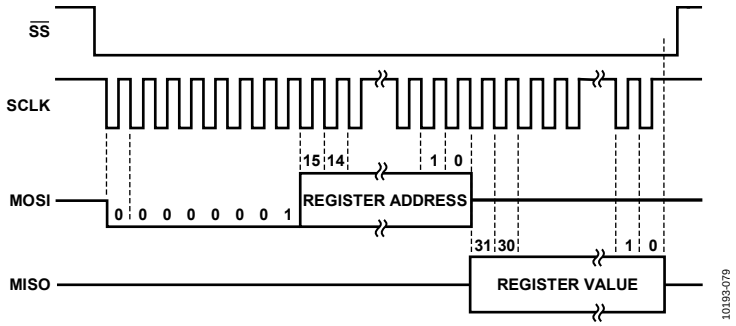

Figure 107. SPI Read Operation of a 32-Bit Register

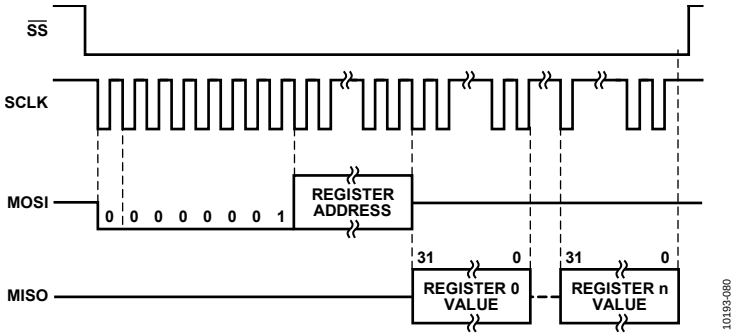

Figure 108. SPI Read Operation of n 32-Bit Harmonic Calculations Registers

SPI Read Operation of Harmonic Calculations Registers

The registers containing the harmonic calculation results are located starting at Address 0xE880 and are all 32-bit width. They can be read in two ways: one register at a time (see the SPI Read Operation section for details) or multiple consecutive registers at a time in a burst mode. The burst mode initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte, representing the address of the ADE7880, on the MOSI line. The address is the same address byte used for reading only one register. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. Next, the master sends the 16-bit address of the first harmonic calculations register that is read. After the ADE7880 receives the last bit of the address of the register on a low-to-high transition of SCLK, it begins to transmit its contents on the MISO line when the next SCLK high-to-low transition occurs; thus, the master can sample the data on a low-to-high SCLK transition. After the master receives the last bit of the first register, the ADE7880 sends the harmonic calculations register placed at the next location and so forth until the master sets the $\overline{SS}$ and SCLK lines high and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 108 for details of the SPI read operation of harmonic calculations registers.

SPI Write Operation

The write operation using the SPI interface of the ADE7880 initiates when the master sets the $\overline{SS}$/HSA pin low and begins sending one byte representing the address of the ADE7880 on the MOSI line. The master sets data on the MOSI line starting with the first high-to-low transition of SCLK. The SPI of the ADE7880 samples data on the low-to-high transitions of SCLK. The most significant seven bits of the address byte can have any value, but as a good programming practice, it is recommended they be different from 0111000b, the seven bits used in the I^2C protocol. Bit 0 (read/$\overline{write}$) of the address byte must be 0 for a write operation. Next, the master sends the 16-bit address of the register that is written and the 32-, 16-, or 8-bit value of that register without losing any SCLK cycle. After the last bit is transmitted, the master sets the $\overline{SS}$ and SCLK lines high at the end of the SCLK cycle and the communication ends. The data lines, MOSI and MISO, go into a high impedance state. See Figure 109 for details of the SPI write operation.

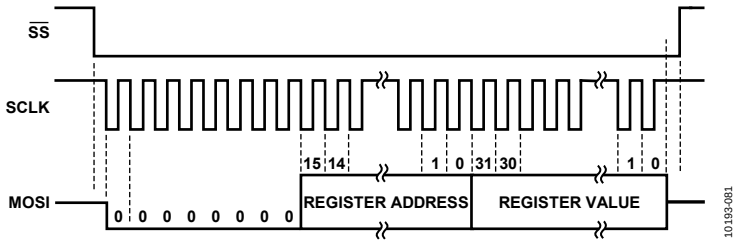

Figure 109. SPI Write Operation of a 32-Bit Register

HSDC Interface

The high speed data capture (HSDC) interface is disabled after default. It can be used only if the ADE7880 is configured with an I²C interface. The SPI interface of ADE7880 cannot be used at the same time with HSDC.

Bit 6 (HSDCEN) in the CONFIG register activates HSDC when set to 1. If Bit HSDCEN is cleared to 0, the default value, the HSDC interface is disabled. Setting Bit HSDCEN to 1 when SPI is in use does not have any effect. HSDC is an interface for sending to an external device (usually a microprocessor or a DSP) up to sixteen 32-bit words. The words represent the instantaneous values of the phase currents and voltages, neutral current, and active, reactive, and apparent powers. The registers being transmitted include IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. All are 24-bit registers that are sign extended to 32-bits (see Figure 45 for details).

HSDC can be interfaced with SPI or similar interfaces. HSDC is always a master of the communication and consists of three pins: HSA, HSD, and HSCLK. HSA represents the select signal. It stays active low or high when a word is transmitted and it is usually connected to the select pin of the slave. HSD sends data to the slave and it is usually connected to the data input pin of the slave. HSCLK is the serial clock line that is generated by the ADE7880 and it is usually connected to the serial clock input of the slave. Figure 110 shows the connections between the ADE7880 HSDC and slave devices containing an SPI interface.

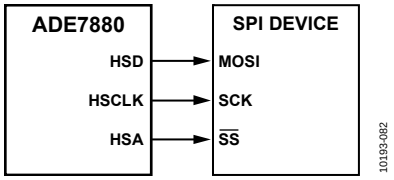

Figure 110. Connecting the ADE7880 HSDC with an SPI

The HSDC communication is managed by the HSDC_CFG register (see Table 52). It is recommended to set the HSDC_CFG register to the desired value before enabling the port using Bit 6 (HSDCEN) in the CONFIG register. In this way, the state of various pins belonging to the HSDC port do not take levels inconsistent with the desired HSDC behavior. After a hardware reset or after power-up, the MISO/HSD and $\overline{SS}$/HSA pins are set high.

Bit 0 (HCLK) in the HSDC_CFG register determines the serial clock frequency of the HSDC communication. When HCLK is 0 (the default value), the clock frequency is 8 MHz. When HCLK is 1, the clock frequency is 4 MHz. A bit of data is transmitted for every HSCLK high-to-low transition. The slave device that receives data from HSDC samples the HSD line on the low-to-high transition of HSCLK.

The words can be transmitted as 32-bit packages or as 8-bit packages. When Bit 1 (HSIZE) in the HSDC_CFG register is 0 (the default value), the words are transmitted as 32-bit packages. When Bit HSIZE is 1, the registers are transmitted as 8-bit packages. The HSDC interface transmits the words MSB first.

Bit 2 (HGAP) introduces a gap of seven HSCLK cycles between packages when Bit 2 (HGAP) is set to 1. When Bit HGAP is cleared to 0 (the default value), no gap is introduced between packages and the communication time is shortest. In this case, HSIZE does not have any influence on the communication and a data bit is placed on the HSD line with every HSCLK high-to-low transition.

Bits[4:3] (HXFER[1:0]) decide how many words are transmitted. When HXFER[1:0] is 00, the default value, then all 16 words are transmitted. When HXFER[1:0] is 01, only the words representing the instantaneous values of phase and neutral currents and phase voltages are transmitted in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and one 32-bit word that is always equal to INWV. When HXFER[1:0] is 10, only the instantaneous values of phase powers are transmitted in the following order: AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. The value, 11, for HXFER[1:0] is reserved and writing it is equivalent to writing 00, the default value.

Bit 5 (HSAPOL) determines the polarity of HSA function of the $\overline{SS}$/HSA pin during communication. When HSAPOL is 0 (the default value), HSA is active low during the communication. This means that HSA stays high when no communication is in progress. When a communication is executed, HSA is low when the 32-bit or 8-bit packages are transferred, and it is high during the gaps. When HSAPOL is 1, the HSA function of the $\overline{SS}$/HSA pin is active high during the communication. This means that HSA stays low when no communication is in progress. When a communication is executed, HSA is high when the 32-bit or 8-bit packages are transferred, and it is low during the gaps.

Bits[7:6] of the HSDC_CFG register are reserved. Any value written into these bits does not have any consequence on HSDC behavior.

Figure 111 shows the HSDC transfer protocol for HGAP = 0, HXFER[1:0] = 00 and HSAPOL = 0. Note that the HSDC interface sets a data bit on the HSD line every HSCLK high-to-low transition and the value of Bit HSIZE is irrelevant.

Figure 112 shows the HSDC transfer protocol for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 32-bit word.

Figure 113 shows the HSDC transfer protocol for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0. Note that the HSDC interface introduces a seven-HSCLK cycles gap between every 8-bit word.

See Table 52 for the HSDC_CFG register and descriptions for the HCLK, HSIZE, HGAP, HXFER[1:0], and HSAPOL bits. Table 25 lists the time it takes to execute an HSDC data transfer for all HSDC_CFG register settings. For some settings, the transfer time is less than 125 µs (8 kHz), the waveform sample registers update rate. This means the HSDC port transmits data every sampling cycle. For settings in which the transfer time is greater than 125 µs, the HSDC port transmits data only in the first of two consecutive 8 kHz sampling cycles. This means it transmits registers at an effective rate of 4 kHz.

Table 25. Communication Times for Various HSDC Settings

HXFER[1:0]	HGAP	HSIZE[1]	HCLK	Communication Time (µs)
00	0	N/A	0	64
00	0	N/A	1	128
00	1	0	0	77.125
00	1	0	1	154.25
00	1	1	0	119.25
00	1	1	1	238.25
01	0	N/A	0	28
01	0	N/A	1	56
01	1	0	0	33.25
01	1	0	1	66.5
01	1	1	0	51.625
01	1	1	1	103.25
10	0	N/A	0	36
10	0	N/A	1	72
10	1	0	0	43
10	1	0	1	86
10	1	1	0	66.625
10	1	1	1	133.25

[1] N/A means not applicable.

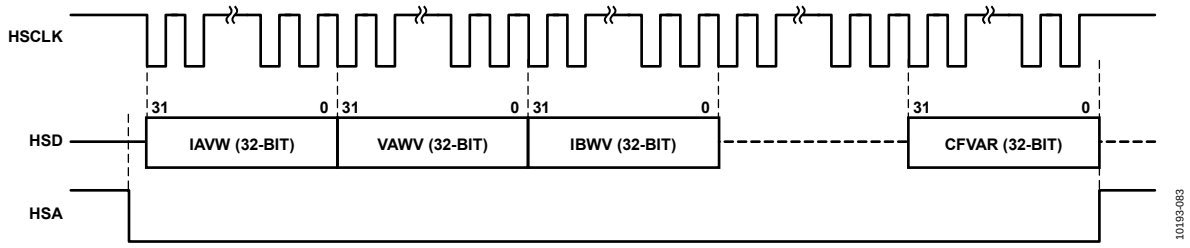

Figure 111. HSDC Communication for HGAP = 0, HXFER[1:0] = 00, and HSAPOL = 0; HSIZE Is Irrelevant

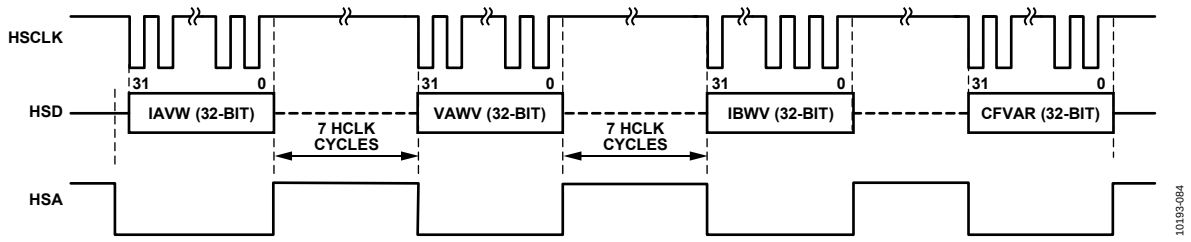

Figure 112. HSDC Communication for HSIZE = 0, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

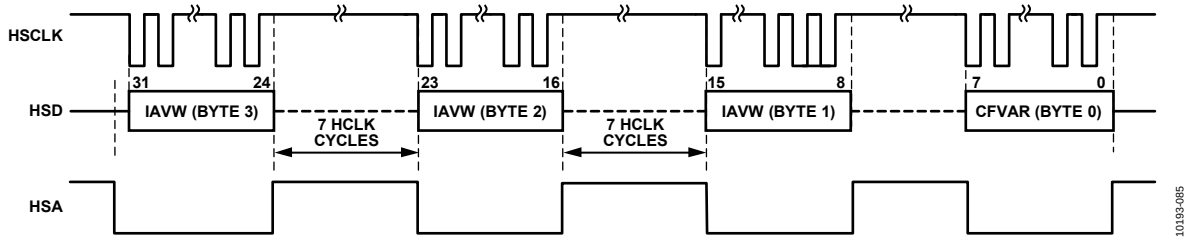

Figure 113. HSDC Communication for HSIZE = 1, HGAP = 1, HXFER[1:0] = 00, and HSAPOL = 0

ADE7880 QUICK SETUP AS ENERGY METER

An energy meter is usually characterized by the nominal current I_n, nominal voltage V_n, nominal frequency f_n, and the meter constant MC.

To quickly set up the ADE7880, execute the following steps:

1. Select the PGA gains in the phase currents, voltages and neutral current channels: Bits[2:0] (PGA1), Bits[5:3] (PGA2) and Bits[8:6] (PGA3) in the Gain register.
2. If Rogowski coils are used, enable the digital integrators in the phase and neutral currents: Bit 0 (INTEN)set to 1 in the CONFIG register. Initialize the DICOEFF register to 0xFF8000 before setting the INTEN bit in the CONFIG register.
3. If f_n is between 55 Hz and 66 Hz, set Bit 14 (SELFREQ) in the COMPMODE register.
4. Initialize all the other data memory RAM registers. Write the last register in the queue three times to ensure that its value is written into the RAM.
5. Initialize the WTHR, VARTHR, VATHR, VLEVEL and VNOM registers based on Equation 26, Equation 37, Equation 44, Equation 22, and Equation 42, respectively.
6. Initialize CF1DEN, CF2DEN, and CF3DEN based on Equation 49.
7. Enable the data memory RAM protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
8. Read back all data memory RAM registers to ensure that they initialized with the desired values. If one or more registers did not initialize correctly, disable the protection by writing 0xAD to an internal 8-bit register at Address 0xE7FE, followed by a write of 0x00 to an internal 8-bit register located at Address 0xE7E3. Reinitialize the registers, and write the last register in the queue three times. Enable the write protection by writing 0xAD to an internal 8-bit register located at Address 0xE7FE, followed by a write of 0x80 to an internal 8-bit register located at Address 0xE7E3.
9. Start the DSP by setting Run = 1.
10. Read the energy registers xWATTHR, xVAHR, xFWATTHR, and xFVARHR to erase their content and start energy accumulation from a known state.
11. Enable the CF1, CF2, and CF3 frequency converter outputs by clearing bits 9, 10, and 11 (CF1DIS, CF2DIS, and CF3DIS) to 0 in the CFMODE register.

For a quick setup of the ADE7880 harmonic calculations, see the Recommended Approach to Managing Harmonic Calculations section.

LAYOUT GUIDELINES

Figure 114 presents a basic schematic of the ADE7880 together with its surrounding circuitry: decoupling capacitors at pins VDD, AVDD, DVDD, and $REF_{IN/OUT}$, the 16.384 MHz crystal, and its load capacitors. The rest of the pins are dependent on the particular application and are not shown here.

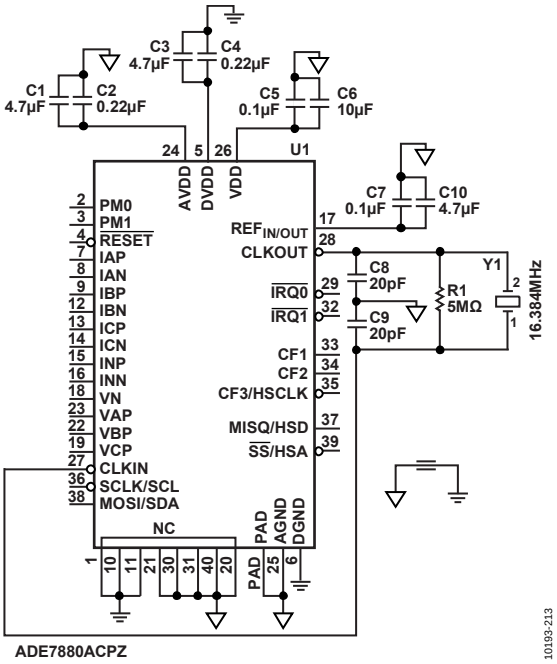

Figure 114. ADE7880 Crystal and Capacitors Selection

Figure 115 and Figure 116 present a proposed layout of a printed circuit board (PCB) with two layers that have the components placed only on the top of the board. Following these layout guidelines helps in creating a low noise design with higher immunity to EMC influences.

The VDD, AVDD, DVDD, and $REF_{IN/OUT}$ pins have two decoupling capacitors each, one of µF order and a ceramic one of 220 nF or 100 nF. These ceramic capacitors need to be placed the closest to the ADE7880 as they decouple high frequency noises, while the µF ones must be placed in close proximity.

The crystal load capacitors need to be placed closest to the ADE7880, while the crystal can be placed in close proximity.

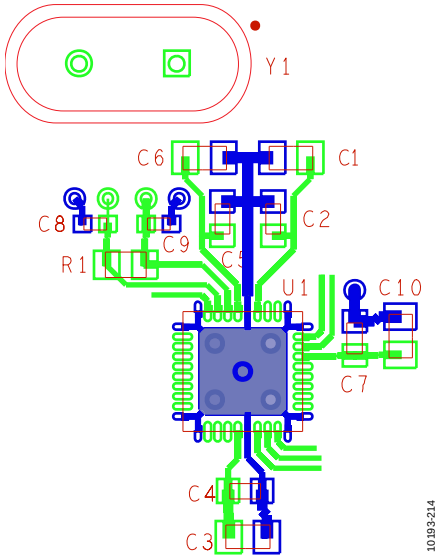

Figure 115. ADE7880 Top Layer Printed Circuit Board

The exposed pad of the ADE7880 is soldered to an equivalent pad on the PCB. The AGND and DGND traces of the ADE7880 are then routed directly into the PCB pad.

The bottom layer is composed mainly of a ground plane surrounding as much as possible the crystal traces.

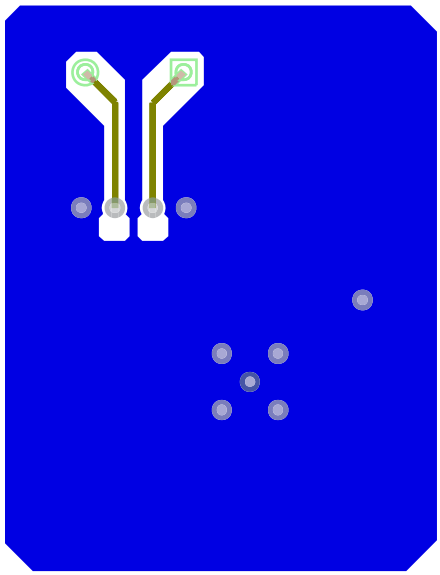

Figure 116. ADE7880 Bottom Layer Printed Circuit Board

CRYSTAL CIRCUIT

A digital clock signal of 16.384 MHz can be provided to the CLKIN pin of the ADE7880. Alternatively, attach a crystal of the specified frequency, as shown in Figure 117. CL_1 and CL_2 denote the capacitances of the ceramic capacitors attached to the crystal pins, whereas CP_1 and CP_2 denote the parasitic capacitances on those pins.

The recommended typical value of total capacitance at each clock pin, CLKIN and CLKOUT, is 24 pF, which means that

$$Total\ Capacitance = CP_1 + CL_1 = CP_2 + CL_2 = 24\ pF$$

Crystal manufacturer data sheets specify the load capacitance value. A total capacitance of 24 pF per clock pin is recommended; therefore, select a crystal with a 12 pF load capacitance. In addition, when selecting the ceramic capacitors, CL_1 and CL_2, the parasitic capacitances, CP_1 and CP_2, on the crystal pins of the IC must be taken into account. Thus, the values of CL_1 and CL_2 must be based on the following expression:

$$CL_1 = CL_2 = 2 \times Crystal\ Load\ Capacitance - CP_1$$

where $CP_1 = CP_2$.

For example, if a 12 pF crystal is chosen and the parasitic capacitances on the clock pins are $CP_1 = CP_2 = 2$ pF, the ceramic capacitors that must be used in the crystal circuit are $CL_1 = CL_2 = 22$ pF.

The EVAL-ADE7880EBZ evaluation board uses the crystal VM6-1D11C12-TR-16.384MHZ (maximum drive level 1 mW; maximum ESR 20 Ω; load capacitance 12 pF). Select the same crystal or a crystal with similar specifications. Lower values of ESR and load capacitance and higher values of drive level capability of the crystal are preferable.

It is also recommended that a 5 MΩ resistor be attached in parallel to the crystal, as shown in Figure 117.

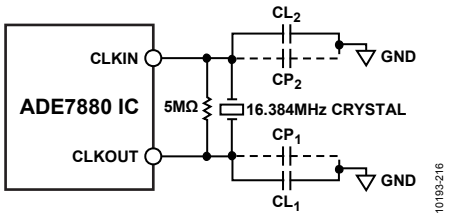

Figure 117. Crystal Circuit

ADE7880 EVALUATION BOARD

An evaluation board built upon the ADE7880 configuration is available. Visit www.analog.com/ADE7880 for details.

DIE VERSION

The register named version identifies the version of the die. It is an 8-bit, read-only register located at Address 0xE707.

SILICON ANOMALY

This anomaly list describes the known issues with the ADE7880 silicon identified by the Version register (Address 0xE707) being equal to 1.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADE7880 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
Version = 1	ADE7880ACPZ	Released	Rev. B	4 (er001, er002, er003, er004)

FUNCTIONALITY ISSUES

Table 26. LAST_ADDR and LAST_RWDATA_x Registers Show Wrong Value in Burst SPI Mode [er001, Version = 1 Silicon]

Background	When any ADE7880 register is read using SPI or I2C communication, the address is stored in the LAST_ADDR register and the data is stored in the respective LAST_RWDATA_x register.
Issue	When the waveform registers located between Address 0xE880 and Address 0xE89F are read using burst SPI mode, the LAST_ADDR register contains the address of the register incremented by 1 and the LAST_RWDATA_x register contains the data corresponding to the faulty address in the LAST_ADDR register. The issue is not present if the I^2C communication is used.
Workaround	After accessing the waveform registers in burst SPI mode, perform another read/write operation elsewhere before using the communication verification registers.
Related Issues	None.

Table 27. To Obtain Best Accuracy Performance, Internal Setting Must Be Changed [er002, Version = 1 Silicon]

Background	Internal default settings provide best accuracy performance for ADE7880.
Issue	It was found that if a different setting is used, the accuracy performance can be improved.
Workaround	To enable a new setting for this internal register, execute three consecutive write operations: The first write operation is to an 8-bit location: 0xAD is written to Address 0xE7FE. The second write operation is to a 16-bit location: 0x3BD is written to Address 0xE90C. The third write operation is to an 8-bit location: 0x00 is written to Address 0xE7FE. The write operations must be executed consecutively without any other read/write operation in between. As a verification that the value was captured correctly, a simple 16-bit read of Address 0xE90C shows the 0x3BD value.
Related Issues	None.

Table 28. High-Pass Filter Cannot be Disabled in Phase C Voltage Data Path [er003, Version = 1 Silicon]

Background	When Bit 0 (HPFEN) of the CONFIG3 register is 0, all high-pass filters (HPF) in the phase and neutral currents and phase voltages data paths are disabled (see the ADE7880 data sheet for more information about the current channel HPF and the voltage channel HPF).
Issue	The HPF in the Phase C voltage data path remains enabled independent of the state of Bit HPFEN.
Workaround	There is no workaround.
Related Issues	None.

Table 29. No Load Condition Does Not Function as Defined [er004, Version = 1 Silicon]

Background	Total active power no load uses the total active energy and the apparent energy to trigger the no load condition. If neither total active energy nor apparent energy are accumulated for a time indicated in the respective APNOLOAD and VANOLOAD unsigned, 16-bit registers, the no load condition is triggered, the total active energy of that phase is not accumulated and no CF pulses are generated based on the total active energy. Fundamental active and reactive powers no load uses the fundamental active and reactive energies to trigger the no load condition. If neither the fundamental active energy nor the fundamental reactive energy are accumulated for a time indicated in the respective APNOLOAD and VARNOLOAD unsigned 16-bit registers, the no load condition is triggered, the fundamental active and reactive energies of that phase are not accumulated, and no CF pulses are generated based on the fundamental active and reactive energies.
Issue	When the total active energy on Phase x (x = A, B, or C) is lower than APNOLOAD and the apparent energy is above VANOLOAD, the no load condition is not triggered. It was observed that although CF pulses continue to be generated, the Bit 0 (NLOAD) and Bits[2:0] (NLPHASE) in STATUS1 and PHNOLOAD registers continue to be cleared to 0 indicating an out of no load condition, the xWATTHR register stops accumulating energy. It was observed that the fundamental active energy no load functions independently of the fundamental reactive energy no load. If, for example, the fundamental active energy is below APNOLOAD and the fundamental reactive energy is above VARNOLOAD, both energies continue to accumulate because the phase is out of no load condition. Instead, the CF pulses, based on the phase fundamental active energy, are not generated and the FWATTHR registers are blocked, while the CF pulses, based on the fundamental reactive energy, are generated. Thus, the FVARHR registers continue to accumulate and the Bit 1 (FNLOAD) in the STATUS1 register and Bits[5:3] (FNLPHASE) in the PHNOLOAD register are cleared to 0. $\overline{\text{IRQ}}$
Workaround	The workaround suggested here uses the VANOLOAD register only to determine the no-load condition. 1. Clear VARNOLOAD and APNOLOAD to 0. 2. Set VANOLOAD at desired value. 3. When the apparent energy on any one of the phases becomes less than VANOLOAD, or when it has just become larger than VANOLOAD, Bit 2 (VANLOAD) in the STATUS1 register is set to 1. The corresponding interrupt can be observed via the $\overline{\text{IRQ}}$ pin if the Bit 2 in MASK1 register is set to 1. The $\overline{\text{IRQ}}$ pin goes low whenever any of the phases enters or leaves the no-load condition. 4. To find the phase that triggered the interrupt, read the PHNOLOAD register immediately. One of the bits VANLPHASE [2:0] changes state, indicating that the particular phase has either entered or left no-load condition. 5. If the particular phase has entered no-load condition, remove the contribution of the energies of that phase to the CFx output by clearing the appropriate TERMSEL_x bits of the COMPMODE register. If that particular phase has left no-load condition, include the contribution of the energies of that phase to the CFx output by setting the appropriate TERMSEL_x bits of the COMPMODE register. 6. Write 1 to the VANLOAD bit of the STATUS1 register, to clear the status bit and to bring the $\overline{\text{IRQ}}$ pin high. 7. If the phase comes out of no-load condition, read with reset all the energy registers to flush out the unnecessary values in the signal path before taking further energy measurements. This can be done by reading the energy registers while the RSTREAD bit (Bit 6) is set to 1 in the LCYCMODE register. 8. Whenever the $\overline{\text{IRQ}}$ pin goes low again, perform the actions starting from Step 3 to service the interrupt.
Related Issues	None.

SECTION 1. ADE7880 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	The LAST_ADDR and LAST_RWDATA_x registers show the wrong values in burst SPI mode.	Identified
er002	To obtain the best accuracy performance, the internal setting must be changed.	Identified
er003	The high-pass filter cannot be disabled in the Phase C voltage data path.	Identified
er004	The no load condition does not function as defined.	Identified

REGISTERS LIST

Table 30. Registers Located in DSP Data Memory RAM

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x4380	AIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A current gain adjust.
0x4381	AVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A voltage gain adjust.
0x4382	BIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B current gain adjust.
0x4383	BVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B voltage gain adjust.
0x4384	CIGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C current gain adjust.
0x4385	CVGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C voltage gain adjust.
0x4386	NIGAIN	R/W	24	32 ZPSE	S	0x000000	Neutral current gain adjust.
0x4387	Reserved	R/W	24	32 ZPSE	S	0x000000	Do not write this location for proper operation.
0x4388	DICOEFF	R/W	24	32 ZPSE	S	0x0000000	Register used in the digital integrator algorithm. If the integrator is turned on, it must be set at 0xFF8000. In practice, it is transmitted as 0xFFF8000.
0x4389	APGAIN	R/W	24	32 ZPSE	S	0x000000	Phase A power gain adjust.
0x438A	AWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A total active power offset adjust.
0x438B	BPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase B power gain adjust.
0x438C	BWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B total active power offset adjust.
0x438D	CPGAIN	R/W	24	32 ZPSE	S	0x000000	Phase C power gain adjust.
0x438E	CWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C total active power offset adjust.
0x438F	AIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A current rms offset.
0x4390	AVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A voltage rms offset.
0x4391	BIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B current rms offset.
0x4392	BVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B voltage rms offset.
0x4393	CIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C current rms offset.
0x4394	CVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C voltage rms offset.
0x4395	NIRMSOS	R/W	24	32 ZPSE	S	0x000000	Neutral current rms offset.
0x4396-0x4397	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x4398	HPGAIN	R/W	24	32 ZPSE	S	0x000000	Harmonic powers gain adjust.
0x4399	ISUMLVL	R/W	24	32 ZPSE	S	0x000000	Threshold used in comparison between the sum of phase currents and the neutral current.
0x439A-0x439E	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x439F	VLEVEL	R/W	28	32 ZP	S	0x0000000	Register used in the algorithm that computes the fundamental active and reactive powers. Set this register according to Equation 22 for proper functioning of fundamental powers and harmonic computations.
0x43A0-0x43A1	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x43A2	AFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental active power offset adjust.
0x43A3	BFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental active power offset adjust.
0x43A4	CFWATTOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental active power offset adjust.
0x43A5	AFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental reactive power offset adjust.
0x43A6	BFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental reactive power offset adjust.
0x43A7	CFVAROS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental reactive power offset adjust.
0x43A8	AFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental current rms offset.
0x43A9	BFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental current rms offset.
0x43AA	CFIRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental current rms offset.
0x43AB	AFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase A fundamental voltage rms offset.
0x43AC	BFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase B fundamental voltage rms offset.
0x43AD	CFVRMSOS	R/W	24	32 ZPSE	S	0x000000	Phase C fundamental voltage rms offset.
0x43AE	HXWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic X (see Harmonics Calculations section for details).

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value	Description
0x43AF	HYWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Y (see Harmonics Calculations section for details).
0x43B0	HZWATTOS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Z (see Harmonics Calculations section for details).
0x43B1	HXVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic X (see Harmonics Calculations section for details).
0x43B2	HYVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Y (see Harmonics Calculations section for details).
0x43B3	HZVAROS	R/W	24	32 ZPSE	S	0x000000	Active power offset adjust on harmonic Z (see Harmonics Calculations section for details).
0x43B4	HXIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic X (see Harmonics Calculations section for details).
0x43B5	HYIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic Y (see Harmonics Calculations section for details).
0x43B6	HZIRMSOS	R/W	24	32 ZPSE	S	0x000000	Current rms offset on harmonic Z (see Harmonics Calculations section for details).
0x43B7	HXVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic X (see Harmonics Calculations section for details).
0x43B8	HYVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic Y (see Harmonics Calculations section for details).
0x43B9	HZVRMSOS	R/W	24	32 ZPSE	S	0x000000	Voltage rms offset on harmonic Z (see Harmonics Calculations section for details).
0x43BA to 0x43BF	Reserved	N/A	N/A	N/A	N/A	0x000000	Do not write these memory locations for proper operation.
0x43C0	AIRMS	R	24	32 ZP	S	N/A	Phase A current rms value.
0x43C1	AVRMS	R	24	32 ZP	S	N/A	Phase A voltage rms value.
0x43C2	BIRMS	R	24	32 ZP	S	N/A	Phase B current rms value.
0x43C3	BVRMS	R	24	32 ZP	S	N/A	Phase B voltage rms value.
0x43C4	CIRMS	R	24	32 ZP	S	N/A	Phase C current rms value.
0x43C5	CVRMS	R	24	32 ZP	S	N/A	Phase C voltage rms value.
0x43C6	NIRMS	R	24	32 ZP	S	N/A	Neutral current rms value.
0x43C7	ISUM	R	28	32 ZP	S	N/A	Sum of IAWV, IBWV and ICWV registers.
0x43C8 to 0x43FF	Reserved	N/A	N/A	N/A	N/A	N/A	Do not write these memory locations for proper operation.

[1] R is read, and W is write.
[2] 32 ZPSE = 24-bit signed register that is transmitted as a 32-bit word with four MSBs padded with 0s and sign extended to 28 bits. Whereas 32 ZP = 28- bit or 24-bit signed or unsigned register that is transmitted as a 32-bit word with four or eight MSBs, respectively, padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 31. Internal DSP Memory RAM Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication	Type[2]	Default Value	Description
0xE203	Reserved	R/W	16	16	U	0x0000	Do not write this memory location for proper operation.
0xE228	Run	R/W	16	16	U	0x0000	Run register starts and stops the DSP. See the Digital Signal Processor section for more details.

[1] R is read, and W is write.
[2] U is unsigned register, and S is signed register in twos complement format.

Table 32. Billable Registers

Address	Register Name	R/W[1, 2]	Bit Length[2]	Bit Length During Communication[2]	Type[2, 3]	Default Value	Description
0xE400	AWATTHR	R	32	32	S	0x00000000	Phase A total active energy accumulation.
0xE401	BWATTHR	R	32	32	S	0x00000000	Phase B total active energy accumulation.
0xE402	CWATTHR	R	32	32	S	0x00000000	Phase C total active energy accumulation.
0xE403	AFWATTHR	R	32	32	S	0x00000000	Phase A fundamental active energy accumulation.
0xE404	BFWATTHR	R	32	32	S	0x00000000	Phase B fundamental active energy accumulation.
0xE405	CFWATTHR	R	32	32	S	0x00000000	Phase C fundamental active energy accumulation.
0xE406 to 0xE408	Reserved	R	32	32	S	0x00000000	
0xE409	AFVARHR	R	32	32	S	0x00000000	Phase A fundamental reactive energy accumulation.
0xE40A	BFVARHR	R	32	32	S	0x00000000	Phase B fundamental reactive energy accumulation.
0xE40B	CFVARHR	R	32	32	S	0x00000000	Phase C fundamental reactive energy accumulation.
0xE40C	AVAHR	R	32	32	S	0x00000000	Phase A apparent energy accumulation.
0xE40D	BVAHR	R	32	32	S	0x00000000	Phase B apparent energy accumulation.
0xE40E	CVAHR	R	32	32	S	0x00000000	Phase C apparent energy accumulation.

[1] R is read, and W is write.
[2] N/A is not applicable.
[3] U is unsigned register, and S is signed register in twos complement format.

Table 33. Configuration and Power Quality Registers

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE500	IPEAK	R	32	32	U	N/A	Current peak register. See Figure 60 and Table 34 for details about its composition.
0xE501	VPEAK	R	32	32	U	N/A	Voltage peak register. See Figure 60 and Table 35 for details about its composition.
0xE502	STATUS0	R/W	32	32	U	N/A	Interrupt Status Register 0. See Table 36.
0xE503	STATUS1	R/W	32	32	U	N/A	Interrupt Status Register 1. See Table 37.
0xE504	AIMAV	R	20	32 ZP	U	N/A	Phase A current mean absolute value computed during PSM0 and PSM1 modes.
0xE505	BIMAV	R	20	32 ZP	U	N/A	Phase B current mean absolute value computed during PSM0 and PSM1 modes.
0xE506	CIMAV	R	20	32 ZP	U	N/A	Phase C current mean absolute value computed during PSM0 and PSM1 modes.
0xE507	OILVL	R/W	24	32 ZP	U	0xFFFFFF	Overcurrent threshold.
0xE508	OVLVL	R/W	24	32 ZP	U	0xFFFFFF	Overvoltage threshold.
0xE509	SAGLVL	R/W	24	32 ZP	U	0x000000	Voltage SAG level threshold.
0xE50A	MASK0	R/W	32	32	U	0x00000000	Interrupt Enable Register 0. See Table 38.
0xE50B	MASK1	R/W	32	32	U	0x00000000	Interrupt Enable Register 1. See Table 39.
0xE50C	IAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A current.
0xE50D	IBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B current.
0xE50E	ICWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C current.
0xE50F	INWV	R	24	32 SE	S	N/A	Instantaneous value of neutral current.
0xE510	VAWV	R	24	32 SE	S	N/A	Instantaneous value of Phase A voltage.
0xE511	VBWV	R	24	32 SE	S	N/A	Instantaneous value of Phase B voltage.
0xE512	VCWV	R	24	32 SE	S	N/A	Instantaneous value of Phase C voltage.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE513	AWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase A total active power.
0xE514	BWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase B total active power.
0xE515	CWATT	R	24	32 SE	S	N/A	Instantaneous value of Phase C total active power.
0xE516 to 0xE518	Reserved	R	24	32 SE	S	0x000000	
0xE519	AVA	R	24	32 SE	S	N/A	Instantaneous value of Phase A apparent power.
0xE51A	BVA	R	24	32 SE	S	N/A	Instantaneous value of Phase B apparent power.
0xE51B	CVA	R	24	32 SE	S	N/A	Instantaneous value of Phase C apparent power.
0xE51F	CHECKSUM	R	32	32	U	0xAFFA63B9	Checksum verification. See the Checksum Register section for details.
0xE520	VNOM	R/W	24	32 ZP	S	0x000000	Nominal phase voltage rms used in the alternative computation of the apparent power. When the VNOMxEN bit is set, the applied voltage input in the corresponding phase is ignored and all corresponding rms voltage instances are replaced by the value in the VNOM register.
0xE521 to 0xE5FE	Reserved						Do not write these addresses for proper operation.
0xE5FF	LAST_RWDATA32	R	32	32	U	N/A	Contains the data from the last successful 32-bit register communication.
0xE600	PHSTATUS	R	16	16	U	N/A	Phase peak register. See Table 40.
0xE601	ANGLE0	R	16	16	U	N/A	Time Delay 0. See the Time Interval Between Phases section for details.
0xE602	ANGLE1	R	16	16	U	N/A	Time Delay 1. See the Time Interval Between Phases section for details.
0xE603	ANGLE2	R	16	16	U	N/A	Time Delay 2. See the Time Interval Between Phases section for details.
0xE604 to 0xE607	Reserved						Do not write these addresses for proper operation.
0xE608	PHNOLOAD	R	16	16	U	N/A	Phase no load register. See Table 41.
0xE609 to 0xE60B	Reserved						Do not write these addresses for proper operation.
0xE60C	LINECYC	R/W	16	16	U	0xFFFF	Line cycle accumulation mode count.
0xE60D	ZXTOUT	R/W	16	16	U	0xFFFF	Zero-crossing timeout count.
0xE60E	COMPMODE	R/W	16	16	U	0x01FF	Computation-mode register. See Table 42.
0xE60F	Gain	R/W	16	16	U	0x0000	PGA gains at ADC inputs. See Table 43.
0xE610	CFMODE	R/W	16	16	U	0x0EA0	CFx configuration register. See Table 44.
0xE611	CF1DEN	R/W	16	16	U	0x0000	CF1 denominator.
0xE612	CF2DEN	R/W	16	16	U	0x0000	CF2 denominator.
0xE613	CF3DEN	R/W	16	16	U	0x0000	CF3 denominator.
0xE614	APHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase A. See Table 45.
0xE615	BPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration of Phase B. See Table 45.
0xE616	CPHCAL	R/W	10	16 ZP	S	0x0000	Phase calibration Phase of C. See Table 45.
0xE617	PHSIGN	R	16	16	U	N/A	Power sign register. See Table 46.
0xE618	CONFIG	R/W	16	16	U	0x0002	ADE7880 configuration register. See Table 47.
0xE700	MMODE	R/W	8	8	U	0x1C	Measurement mode register. See Table 48.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE701	ACCMODE	R/W	8	8	U	0x80	Accumulation mode register. See Table 49.
0xE702	LCYCMODE	R/W	8	8	U	0x78	Line accumulation mode behavior. See Table 51.
0xE703	PEAKCYC	R/W	8	8	U	0x00	Peak detection half line cycles.
0xE704	SAGCYC	R/W	8	8	U	0x00	SAG detection half line cycles.
0xE705	CFCYC	R/W	8	8	U	0x01	Number of CF pulses between two consecutive energy latches. See the Synchronizing Energy Registers with CFx Outputs section.
0xE706	HSDC_CFG	R/W	8	8	U	0x00	HSDC configuration register. See Table 52.
0xE707	Version	R	8	8	U		Version of die.
0xE7E4	Reserved	R	8	8	U	0x08	This register must remain at this value for checksum functionality to work. If this register shows a different value while being read, reset the chip before working with the checksum feature.
0xE7FD	LAST_RWDATA8	R	8	8	U	N/A	Contains the data from the last successful 8-bit register communication.
0xE880	FVRMS	R	24	32	S	N/A	The rms value of the fundamental component of the phase voltage.
0xE881	FIRMS	R	24	32	S	N/A	The rms value of the fundamental component of the phase current
0xE882	FWATT	R	24	32	S	N/A	The active power of the fundamental component.
0xE883	FVAR	R	24	32	S	N/A	The reactive power of the fundamental component.
0xE884	FVA	R	24	32	S	N/A	The apparent power of the fundamental component.
0xE885	FPF	R	24	32	S	N/A	The power factor of the fundamental component.
0xE886	VTHD	R	24	32	S	N/A	Total harmonic distortion of the phase voltage.
0xE887	ITHD	R	24	32	S	N/A	Total harmonic distortion of the phase current.
0xE888	HXVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic X.
0xE889	HXIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic X.
0xE88A	HXWATT	R	24	32	S	N/A	The active power of the harmonic X.
0xE88B	HXVAR	R	24	32	S	N/A	The reactive power of the harmonic X.
0xE88C	HXVA	R	24	32	S	N/A	The apparent power of the harmonic X.
0xE88D	HXPF	R	24	32	S	N/A	The power factor of the harmonic X.
0xE88E	HXVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic X relative to the fundamental.
0xE88F	HXIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic X relative to the fundamental.
0xE890	HYVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic Y.
0xE891	HYIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic Y.
0xE892	HYWATT	R	24	32	S	N/A	The active power of the harmonic Y.
0xE893	HYVAR	R	24	32	S	N/A	The reactive power of the harmonic Y.
0xE894	HYVA	R	24	32	S	N/A	The apparent power of the harmonic Y.
0xE895	HYPF	R	24	32	S	N/A	The power factor of the harmonic Y.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xE896	HYVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic Y relative to the fundamental.
0xE897	HYIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic Y relative to the fundamental.
0xE898	HZVRMS	R	24	32	S	N/A	The rms value of the phase voltage harmonic Z.
0xE899	HZIRMS	R	24	32	S	N/A	The rms value of the phase current harmonic Z.
0xE89A	HZWATT	R	24	32	S	N/A	The active power of the harmonic Z.
0xE89B	HZVAR	R	24	32	S	N/A	The reactive power of the harmonic Z.
0xE89C	HZVA	R	24	32	S	N/A	The apparent power of the harmonic Z.
0xE89D	HZPF	R	24	32	S	N/A	The power factor of the harmonic Z.
0xE89E	HZVHD	R	24	32	S	N/A	Harmonic distortion of the phase voltage harmonic Z relative to the fundamental.
0xE89F	HZIHD	R	24	32	S	N/A	Harmonic distortion of the phase current harmonic Z relative to the fundamental.
0xE8A0 to 0xE8FF	Reserved		24	32			Reserved. These registers are always 0.
0xE900	HCONFIG	R/W	16	16	U	0x08	Harmonic Calculations Configuration register. See Table 54.
0xE902	APF	R	16	16	S	N/A	Phase A power factor.
0xE903	BPF	R	16	16	S	N/A	Phase B power factor.
0xE904	CPF	R	16	16	S	N/A	Phase C power factor.
0xE905	APERIOD	R	16	16	U	N/A	Line period on Phase A voltage.
0xE906	BPERIOD	R	16	16	U	N/A	Line period on Phase B voltage.
0xE907	CPERIOD	R	16	16	U	N/A	Line period on Phase C voltage.
0xE908	APNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental active power data paths. Do not write 0xFFFF to this register.
0xE909	VARNOLOAD	R/W	16	16	U	0x0000	No load threshold in the total/ fundamental reactive power data path. Do not write 0xFFFF to this register.
0xE90A	VANOLOAD	R/W	16	16	U	0x0000	No load threshold in the apparent power data path. Do not write 0xFFFF to this register.
0xE9FE	LAST_ADD	R	16	16	U	N/A	The address of the register successfully accessed during the last read/write operation.
0xE9FF	LAST_RWDATA16	R	16	16	U	N/A	Contains the data from the last successful 16-bit register communication.
0xEA00	CONFIG3	R/W	8	8	U	0x01	Configuration register. See Table 53.
0xEA01	LAST_OP	R	8	8	U	N/A	Indicates the type, read or write, of the last successful read/write operation.
0xEA02	WTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental active power data path.
0xEA03	VARTHR	R/W	8	8	U	0x03	Threshold used in phase total/ fundamental reactive power data path.
0xEA04	VATHR	R/W	8	8	U	0x03	Threshold used in phase apparent power data path.
0xEA05 to 0xEA07	Reserved		8	8			Reserved. These registers are always 0.
0xEA08	HX	R/W	8	8	U	3	Selects an index of the harmonic monitored by the harmonic computations.
0xEA09	HY	R/W	8	8	U	5	Selects an index of the harmonic monitored by the harmonic computations.

Address	Register Name	R/W[1]	Bit Length	Bit Length During Communication[2]	Type[3]	Default Value[4]	Description
0xEA0A	HZ	R/W	8	8	U	7	Selects an index of the harmonic monitored by the harmonic computations.
0xEA0B to 0xEBFE	Reserved		8	8			Reserved. These registers are always 0.
0xEBFF	Reserved		8	8			This address can be used in manipulating the $\overline{SS}$/HSA pin when SPI is chosen as the active port. See the Serial Interfaces section for details.
0xEC00	LPOILVL	R/W	8	8	U	0x07	Overcurrent threshold used during PSM2 mode. See Table 55 in which the register is detailed.
0xEC01	CONFIG2	R/W	8	8	U	0x00	Configuration register used during PSM1 mode. See Table 56.

[1] R is read, and W is write.
[2] 32 ZP = 24- or 20-bit signed or unsigned register that is transmitted as a 32-bit word with 8 or 12 MSBs, respectively, padded with 0s. 32 SE = 24-bit signed register that is transmitted as a 32-bit word sign extended to 32 bits. 16 ZP = 10-bit unsigned register that is transmitted as a 16-bit word with six MSBs padded with 0s.
[3] U is unsigned register, and S is signed register in twos complement format.
[4] N/A is not applicable.

Table 34. IPEAK Register (Address 0xE500)

Bit	Mnemonic	Default Value	Description
23:0	IPEAKVAL[23:0]	0	These bits contain the peak value determined in the current channel.
24	IPPHASE[0]	0	When this bit is set to 1, Phase A current generated IPEAKVAL[23:0] value.
25	IPPHASE[1]	0	When this bit is set to 1, Phase B current generated IPEAKVAL[23:0] value.
26	IPPHASE[2]	0	When this bit is set to 1, Phase C current generated IPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 35. VPEAK Register (Address 0xE501)

Bit	Mnemonic	Default Value	Description
23:0	VPEAKVAL[23:0]	0	These bits contain the peak value determined in the voltage channel.
24	VPPHASE[0]	0	When this bit is set to 1, Phase A voltage generated VPEAKVAL[23:0] value.
25	VPPHASE[1]	0	When this bit is set to 1, Phase B voltage generated VPEAKVAL[23:0] value.
26	VPPHASE[2]	0	When this bit is set to 1, Phase C voltage generated VPEAKVAL[23:0] value.
31:27		00000	These bits are always 0.

Table 36. STATUS0 Register (Address 0xE502)

Bit	Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) has changed.
1	FAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental active energy registers, FWATTHR, BFWATTHR, or CFWATTHR, has changed.
2	Reserved	0	This bit is always 0.
3	FREHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the fundamental reactive energy registers, AFVARHR, BFVARHR, or CFVARHR, has changed.
4	VAEHF	0	When this bit is set to 1, it indicates that Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) has changed.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it indicates the end of an integration over an integer number of half line cycles set in the LINECYC register.

Bit	Mnemonic	Default Value	Description
6	REVAPA	0	When this bit is set to 1, it indicates that the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 0 (AWSIGN) of the PHSIGN register (see Table 46).
7	REVAPB	0	When this bit is set to 1, it indicates that the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 1 (BWSIGN) of the PHSIGN register (see Table 46).
8	REVAPC	0	When this bit is set to 1, it indicates that the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) has changed sign. The sign itself is indicated in Bit 2 (CWSIGN) of the PHSIGN register (see Table 46).
9	REVPSUM1	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF1 data path has changed sign. The sign itself is indicated in Bit 3 (SUM1SIGN) of the PHSIGN register (see Table 46).
10	REVFRPA	0	When this bit is set to 1, it indicates that the Phase A fundamental reactive power has changed sign. The sign itself is indicated in Bit 4 (AFVARSIGN) of the PHSIGN register (see Table 46).
11	REVFRPB	0	When this bit is set to 1, it indicates that the Phase B fundamental reactive power has changed sign. The sign itself is indicated in Bit 5 (BFVARSIGN) of the PHSIGN register (see Table 46).
12	REVFRPC	0	When this bit is set to 1, it indicates that the Phase C fundamental reactive power has changed sign. The sign itself is indicated in Bit 6 (CFVARSIGN) of the PHSIGN register (see Table 46).
13	REVPSUM2	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF2 data path has changed sign. The sign itself is indicated in Bit 7 (SUM2SIGN) of the PHSIGN register (see Table 46).
14	CF1		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF1 pin; that is, an active low pulse has been generated. The bit is set even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 44).
15	CF2		When this bit is set to 1, it indicates a high-to-low transition has occurred at the CF2 pin; that is, an active low pulse has been generated. The bit is set even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 44).
16	CF3		When this bit is set to 1, it indicates a high-to-low transition has occurred at CF3 pin; that is, an active low pulse has been generated. The bit is set even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 44).
17	DREADY	0	When this bit is set to 1, it indicates that all periodical (at 8 kHz rate) DSP computations have finished.
18	REVPSUM3	0	When this bit is set to 1, it indicates that the sum of all phase powers in the CF3 data path has changed sign. The sign itself is indicated in Bit 8 (SUM3SIGN) of the PHSIGN register (see Table 46).
19	HREADY	0	When this bit is set to 1, it indicates the harmonic block output registers are updated. If Bit 0 (HRCFG) in the HCONFIG register is cleared to 0, this flag is set to 1 every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in the HCONFIG register starting HSTIME (Bits [4:3] in the HCONFIG register) after the harmonic block setup. If Bit HRCFG is set to 1, the HREADY flag is set to 1 every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in the HCONFIG register, starting immediately after the harmonic block setup.
31:18	Reserved	0 0000 0000 0000	Reserved. These bits are always 0.

Table 37. STATUS1 Register (Address 0xE503)

Bit	Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition determined by the total active power and apparent power. The phase is indicated in Bits[2:0] (NLPHASE[x]) in the PHNOLOAD register (see Table 41.)
1	FNLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on fundamental active and reactive powers. The phase is indicated in Bits[5:3] (FNLPHASE[x]) in the PHNOLOAD register (see Table 41).
2	VANLOAD	0	When this bit is set to 1, it indicates that at least one phase entered no load condition based on apparent power. The phase is indicated in Bits[8:6] (VANLPHASE[x]) in the PHNOLOAD register (see Table 41).
3	ZXTOVA	0	When this bit is set to 1, it indicates a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it indicates a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it indicates a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it indicates a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it indicates a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it indicates a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it indicates a zero crossing has been detected on Phase C current.
15	RSTDONE	1	In case of a software reset command, Bit 7 (SWRST) is set to 1 in the CONFIG register, or a transition from PSM1, PSM2, or PSM3 to PSM0, or a hardware reset, this bit is set to 1 at the end of the transition process and after all registers change value to default. The $\overline{\text{IRQ1}}$ pin goes low to signal this moment because this interrupt cannot be disabled.
16	SAG	0	When this bit is set to 1, it indicates one of phase voltages entered or exited a sag state. The phase is indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it indicates an overcurrent event has occurred on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it indicates an overvoltage event has occurred on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).
19	SEQERR	0	When this bit is set to 1, it indicates a negative-to-positive zero crossing on Phase A voltage was not followed by a negative-to-positive zero crossing on Phase B voltage but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it indicates $\left\|\|ISUM\| - \|INWV\right\| > ISUMLVL$, where *ISUMLVL* is indicated in the ISUMLVL register.
21	Reserved	1	Reserved. This bit is always set to 1.
22	Reserved	0	Reserved. This bit is always set to 0.
23	PKI	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the current channel has ended. The IPEAK register contains the peak value and the phase where the peak has been detected (see Table 34).

Bit	Mnemonic	Default Value	Description
24	PKV	0	When this bit is set to 1, it indicates that the period used to detect the peak value in the voltage channel has ended. VPEAK register contains the peak value and the phase where the peak has been detected (see Table 35).
25	CRC	0	When this bit is set to 1, it indicates the ADE7880 has computed a different checksum relative to the one computed when the Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits are always 0.

Table 38. MASK0 Register (Address 0xE50A)

Bit	Mnemonic	Default Value	Description
0	AEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the total active energy registers (AWATTHR, BWATTHR, or CWATTHR) changes.
1	FAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental active energy registers (AFWATTHR, BFWATTHR, or CFWATTHR) changes.
2	Reserved	0	This bit does not manage any functionality.
3	FREHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the fundamental reactive energy registers (AFVARHR, BFVARHR, or CFVARHR) changes.
4	VAEHF	0	When this bit is set to 1, it enables an interrupt when Bit 30 of any one of the apparent energy registers (AVAHR, BVAHR, or CVAHR) changes.
5	LENERGY	0	When this bit is set to 1, in line energy accumulation mode, it enables an interrupt at the end of an integration over an integer number of half line cycles set in the LINECYC register.
6	REVAPA	0	When this bit is set to 1, it enables an interrupt when the Phase A active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
7	REVAPB	0	When this bit is set to 1, it enables an interrupt when the Phase B active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
8	REVAPC	0	When this bit is set to 1, it enables an interrupt when the Phase C active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total or fundamental) changes sign.
9	REVPSUM1	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF1 data path changes sign.
10	REVFRPA	0	When this bit is set to 1, it enables an interrupt when the Phase A fundamental reactive power changes sign.
11	REVFRPB	0	When this bit is set to 1, it enables an interrupt when the Phase B fundamental reactive power changes sign.
12	REVFRPC	0	When this bit is set to 1, it enables an interrupt when the Phase C fundamental reactive power changes sign.
13	REVPSUM2	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF2 data path changes sign.
14	CF1		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at the CF1 pin, that is an active low pulse is generated. The interrupt can be enabled even if the CF1 output is disabled by setting Bit 9 (CF1DIS) to 1 in the CFMODE register. The type of power used at the CF1 pin is determined by Bits[2:0] (CF1SEL[2:0]) in the CFMODE register (see Table 44).
15	CF2		When this bit is set to 1, it enables an interrupt when a high-to-low transition occurs at CF2 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF2 output is disabled by setting Bit 10 (CF2DIS) to 1 in the CFMODE register. The type of power used at the CF2 pin is determined by Bits[5:3] (CF2SEL[2:0]) in the CFMODE register (see Table 44).
16	CF3		When this bit is set to 1, it enables an interrupt when a high to low transition occurs at CF3 pin, that is an active low pulse is generated. The interrupt may be enabled even if the CF3 output is disabled by setting Bit 11 (CF3DIS) to 1 in the CFMODE register. The type of power used at the CF3 pin is determined by Bits[8:6] (CF3SEL[2:0]) in the CFMODE register (see Table 44).
17	DREADY	0	When this bit is set to 1, it enables an interrupt when all periodical (at 8 kHz rate) DSP computations finish.

Bit	Mnemonic	Default Value	Description
18	REVPSUM3	0	When this bit is set to 1, it enables an interrupt when the sum of all phase powers in the CF3 data path changes sign.
19	HREADY	0	When this bit is set to 1, it enables an interrupt when the harmonic block output registers have been updated. If Bit 0 (HRCFG) in HCONFIG register is cleared to 0, the interrupt is triggered every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in HCONFIG register starting HSTIME (Bits [4:3] in HCONFIG register) after the harmonic block setup. If Bit HRCFG is set to 1, the interrupt is triggered every time the harmonic block output registers are updated at a rate identified by Bits [7:5] (HRATE) in HCONFIG register starting immediately after the harmonic block setup.
31:19	Reserved	00 0000 0000 0000	Reserved. These bits do not manage any functionality.

Table 39. MASK1 Register (Address 0xE50B)

Bit	Mnemonic	Default Value	Description
0	NLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition determined by the total active power and VNOM based apparent power.
1	FNLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on fundamental active and reactive powers.
2	VANLOAD	0	When this bit is set to 1, it enables an interrupt when at least one phase enters no load condition based on apparent power.
3	ZXTOVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A voltage is missing.
4	ZXTOVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B voltage is missing.
5	ZXTOVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C voltage is missing.
6	ZXTOIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase A current is missing.
7	ZXTOIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase B current is missing.
8	ZXTOIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing on Phase C current is missing.
9	ZXVA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A voltage.
10	ZXVB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B voltage.
11	ZXVC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C voltage.
12	ZXIA	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase A current.
13	ZXIB	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase B current.
14	ZXIC	0	When this bit is set to 1, it enables an interrupt when a zero crossing is detected on Phase C current.
15	RSTDONE	0	Because the RSTDONE interrupt cannot be disabled, this bit does not have any functionality attached. It can be set to 1 or cleared to 0 without having any effect.
16	SAG	0	When this bit is set to 1, it enables an interrupt when one of the phase voltages entered or exited a sag state. The phase is indicated by Bits[14:12] (VSPHASE[x]) in the PHSTATUS register (see Table 40).
17	OI	0	When this bit is set to 1, it enables an interrupt when an overcurrent event occurs on one of the phases indicated by Bits[5:3] (OIPHASE[x]) in the PHSTATUS register (see Table 40).
18	OV	0	When this bit is set to 1, it enables an interrupt when an overvoltage event occurs on one of the phases indicated by Bits[11:9] (OVPHASE[x]) in the PHSTATUS register (see Table 40).

Bit	Mnemonic	Default Value	Description
19	SEQERR	0	When this bit is set to 1, it enables an interrupt when a negative-to-positive zero crossing on Phase A voltage is not followed by a negative-to-positive zero crossing on Phase B voltage, but by a negative-to-positive zero crossing on Phase C voltage.
20	MISMTCH	0	When this bit is set to 1, it enables an interrupt when $\left\|\|ISUM\| - \|INWV\right\| > ISUMLVL$ is greater than the value indicated in ISUMLVL register.
22:21	Reserved	00	Reserved. These bits do not manage any functionality.
23	PKI	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the current channel has ended.
24	PKV	0	When this bit is set to 1, it enables an interrupt when the period used to detect the peak value in the voltage channel has ended.
25	CRC	0	When this bit is set to 1, it enables an interrupt when the latest checksum value is different from the checksum value computed when Run register was set to 1.
31:26	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 40. PHSTATUS Register (Address 0xE600)

Bit	Mnemonic	Default Value	Description
2:0	Reserved	000	Reserved. These bits are always 0.
3	OIPHASE[0]	0	When this bit is set to 1, Phase A current generates Bit 17 (OI) in the STATUS1 register.
4	OIPHASE[1]	0	When this bit is set to 1, Phase B current generates Bit 17 (OI) in the STATUS1 register.
5	OIPHASE[2]	0	When this bit is set to 1, Phase C current generates Bit 17 (OI) in the STATUS1 register.
8:6	Reserved	000	Reserved. These bits are always 0.
9	OVPHASE[0]	0	When this bit is set to 1, Phase A voltage generates Bit 18 (OV) in the STATUS1 register.
10	OVPHASE[1]	0	When this bit is set to 1, Phase B voltage generates Bit 18 (OV) in the STATUS1 register.
11	OVPHASE[2]	0	When this bit is set to 1, Phase C voltage generates Bit 18 (OV) in the STATUS1 register.
12	VSPHASE[0]	0	0: Phase A voltage is above SAGLVL level for SAGCYC half line cycles. 1: Phase A voltage is below SAGLVL level for SAGCYC half line cycles. When this bit is switches from 0 to 1 or from 1 to 0, the Phase A voltage generates Bit 16 (SAG) in the STATUS1 register.
13	VSPHASE[1]	0	0: Phase B voltage is above SAGLVL level for SAGCYC half line cycles. 1: Phase B voltage is below SAGLVL level for SAGCYC half line cycles. When this bit is switches from 0 to 1 or from 1 to 0, the Phase B voltage generates Bit 16 (SAG) in the STATUS1 register.
14	VSPHASE[2]	0	0: Phase C voltage is above SAGLVL level for SAGCYC half line cycles 1: Phase C voltage is below SAGLVL level for SAGCYC half line cycles When this bit is switches from 0 to 1 or from 1 to 0, the Phase C voltage generates Bit 16 (SAG) in the STATUS1 register.
15	Reserved	0	Reserved. This bit is always 0.

Table 41. PHNOLOAD Register (Address 0xE608)

Bit	Mnemonic	Default Value	Description
0	NLPHASE[0]	0	0: Phase A is out of no load condition determined by the Phase A total active power and apparent power. 1: Phase A is in no load condition determined by phase A total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
1	NLPHASE[1]	0	0: Phase B is out of no load condition determined by the Phase B total active power and apparent power. 1: Phase B is in no load condition determined by the Phase B total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
2	NLPHASE[2]	0	0: Phase C is out of no load condition determined by the Phase C total active power and apparent power. 1: Phase C is in no load condition determined by the Phase C total active power and apparent power. Bit set together with Bit 0 (NLOAD) in the STATUS1 register.
3	FNLPHASE[0]	0	0: Phase A is out of no load condition based on fundamental active/reactive powers. 1: Phase A is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.

Bit	Mnemonic	Default Value	Description
4	FNLPHASE[1]	0	0: Phase B is out of no load condition based on fundamental active/reactive powers. 1: Phase B is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
5	FNLPHASE[2]	0	0: Phase C is out of no load condition based on fundamental active/reactive powers. 1: Phase C is in no load condition based on fundamental active/reactive powers. This bit is set together with Bit 1 (FNLOAD) in STATUS1.
6	VANLPHASE[0]	0	0: Phase A is out of no load condition based on apparent power. 1: Phase A is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
7	VANLPHASE[1]	0	0: Phase B is out of no load condition based on apparent power. 1: Phase B is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
8	VANLPHASE[2]	0	0: Phase C is out of no load condition based on apparent power. 1: Phase C is in no load condition based on apparent power. Bit set together with Bit 2 (VANLOAD) in the STATUS1 register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 42. COMPMODE Register (Address 0xE60E)

Bit	Mnemonic	Default Value	Description
0	TERMSEL1[0]	1	Setting all TERMSEL1[2:0] to 1 signifies the sum of all three phases is included in the CF1 output. Phase A is included in the CF1 outputs calculations.
1	TERMSEL1[1]	1	Phase B is included in the CF1 outputs calculations.
2	TERMSEL1[2]	1	Phase C is included in the CF1 outputs calculations.
3	TERMSEL2[0]	1	Setting all TERMSEL2[2:0] to 1 signifies the sum of all three phases is included in the CF2 output. Phase A is included in the CF2 outputs calculations.
4	TERMSEL2[1]	1	Phase B is included in the CF2 outputs calculations.
5	TERMSEL2[2]	1	Phase C is included in the CF2 outputs calculations.
6	TERMSEL3[0]	1	Setting all TERMSEL3[2:0] to 1 signifies the sum of all three phases is included in the CF3 output. Phase A is included in the CF3 outputs calculations.
7	TERMSEL3[1]	1	Phase B is included in the CF3 outputs calculations.
8	TERMSEL3[2]	1	Phase C is included in the CF3 outputs calculations.
10:9	ANGLESEL[1:0]	00	00: the angles between phase voltages and phase currents are measured. 01: the angles between phase voltages are measured. 10: the angles between phase currents are measured. 11: no angles are measured.
11	VNOMAEN	0	When this bit is 0, the apparent power on Phase A is computed regularly. When this bit is 1, the apparent power on Phase A is computed using the VNOM register instead of regular measured rms phase voltage. The applied Phase A voltage input is ignored, and all Phase A rms voltage instances are replaced by the value in the VNOM register.
12	VNOMBEN	0	When this bit is 0, the apparent power on Phase B is computed regularly. When this bit is 1, the apparent power on Phase B is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase B voltage input is ignored, and all Phase B rms voltage instances are replaced by the value in the VNOM register.
13	VNOMCEN	0	When this bit is 0, the apparent power on Phase C is computed regularly. When this bit is 1, the apparent power on Phase C is computed using VNOM register instead of regular measured rms phase voltage. The applied Phase C voltage input is ignored, and all Phase C rms voltage instances are replaced by the value in the VNOM register.
14	SELFREQ	0	When the ADE7880 is connected to networks with fundamental frequencies between 45 Hz and 55 Hz, clear this bit to 0 (default value). When the ADE7880 is connected to networks with fundamental frequencies between 55 Hz and 66 Hz, set this bit to 1.
15	Reserved	0	This bit is 0 by default and it does not manage any functionality.

Table 43. Gain Register (Address 0xE60F)

Bit	Mnemonic	Default Value	Description
2:0	PGA1[2:0]	000	Phase currents gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA1[2:0] = 000.
5:3	PGA2[2:0]	000	Neutral current gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA2[2:0] = 000.
8:6	PGA3[2:0]	000	Phase voltages gain selection. 000: gain = 1. 001: gain = 2. 010: gain = 4. 011: gain = 8. 100: gain = 16. 101, 110, 111: reserved. When set, the ADE7880 behaves like PGA3[2:0] = 000.
15:9	Reserved	000 0000	Reserved. These bits do not manage any functionality.

Table 44. CFMODE Register (Address 0xE610)

Bit	Mnemonic	Default Value	Description
2:0	CF1SEL[2:0]	000	000: the CF1 frequency is proportional to the sum of total active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 010: the CF1 frequency is proportional to the sum of apparent powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 011: the CF1 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 100: the CF1 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[2:0] (TERMSEL1[x]) in the COMPMODE register. 001, 101, 110, 111: reserved.
5:3	CF2SEL[2:0]	100	000: the CF2 frequency is proportional to the sum of total active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 010: the CF2 frequency is proportional to the sum of apparent powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 011: the CF2 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 100: the CF2 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[5:3] (TERMSEL2[x]) in the COMPMODE register. 001, 101,110,111: reserved.

Bit	Mnemonic	Default Value	Description
8:6	CF3SEL[2:0]	010	000: the CF3 frequency is proportional to the sum of total active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 010: the CF3 frequency is proportional to the sum of apparent powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 011: CF3 frequency is proportional to the sum of fundamental active powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 100: CF3 frequency is proportional to the sum of fundamental reactive powers on each phase identified by Bits[8:6] (TERMSEL3[x]) in the COMPMODE register. 001, 101,110,111: reserved.
9	CF1DIS	1	When this bit is set to 1, the CF1 output is disabled. The respective digital to frequency converter remains enabled even if CF1DIS = 1. When this bit is set to 0, the CF1 output is enabled.
10	CF2DIS	1	When this bit is set to 1, the CF2 output is disabled. The respective digital to frequency converter remains enabled even if CF2DIS = 1. When this bit is set to 0, the CF2 output is enabled.
11	CF3DIS	1	When this bit is set to 1, the CF3 output is disabled. The respective digital to frequency converter remains enabled even if CF3DIS = 1. When this bit is set to 0, the CF3 output is enabled.
12	CF1LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF1 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
13	CF2LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF2 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
14	CF3LATCH	0	When this bit is set to 1, the content of the corresponding energy registers is latched when a CF3 pulse is generated. See the Synchronizing Energy Registers with CFx Outputs section.
15	Reserved	0	Reserved. This bit does not manage any functionality.

Table 45. APHCAL, BPHCAL, CPHCAL Registers (Address 0xE614, Address 0xE615, Address 0xE616)

Bit	Mnemonic	Default Value	Description
9:0	PHCALVAL	0000000000	If the current leads the voltage, these bits can vary between 0 and 383. If the current lags the voltage, these bits can vary between 512 and 575. If the PHCALVAL bits are set with numbers between 384 and 511, the compensation behaves like PHCALVAL set between 256 and 383. If the PHCALVAL bits are set with numbers between 576 and 1023, the compensation behaves like PHCALVAL bits set between 384 and 511.
15:10	Reserved	000000	Reserved. These bits do not manage any functionality.

Table 46. PHSIGN Register (Address 0xE617)

Bit	Mnemonic	Default Value	Description
0	AWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase A is negative.
1	BWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is positive. 1: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase B is negative.
2	CWSIGN	0	0: if the active power identified by Bit 6 (REVAPSEL) in the ACCMODE register (total of fundamental) on Phase C is positive. 1: if the active power identified by Bit 6 (REVAPSEL) bit in the ACCMODE register (total of fundamental) on Phase C is negative.

Bit	Mnemonic	Default Value	Description
3	SUM1SIGN	0	0: if the sum of all phase powers in the CF1 data path is positive. 1: if the sum of all phase powers in the CF1 data path is negative. Phase powers in the CF1 data path are identified by Bits[2:0] (TERMSEL1[x]) of the COMPMODE register and by Bits[2:0] (CF1SEL[x]) of the CFMODE register.
4	AFVARSIGN	0	0: if the fundamental reactive power on Phase A is positive. 1: if the fundamental reactive power on Phase A is negative.
5	BFVARSIGN	0	0: if the fundamental reactive power on Phase B is positive. 1: if the fundamental reactive power on Phase B is negative.
6	CFVARSIGN	0	0: if the fundamental reactive power on Phase C is positive. 1: if the fundamental reactive power on Phase C is negative.
7	SUM2SIGN	0	0: if the sum of all phase powers in the CF2 data path is positive. 1: if the sum of all phase powers in the CF2 data path is negative. Phase powers in the CF2 data path are identified by Bits[5:3] (TERMSEL2[x]) of the COMPMODE register and by Bits[5:3] (CF2SEL[x]) of the CFMODE register.
8	SUM3SIGN	0	0: if the sum of all phase powers in the CF3 data path is positive. 1: if the sum of all phase powers in the CF3 data path is negative. Phase powers in the CF3 data path are identified by Bits[8:6] (TERMSEL3[x]) of the COMPMODE register and by Bits[8:6] (CF3SEL[x]) of the CFMODE register.
15:9	Reserved	000 0000	Reserved. These bits are always 0.

Table 47. CONFIG Register (Address 0xE618)

Bit	Mnemonic	Default Value	Description
0	INTEN	0	This bit manages the integrators in the phase current channels. If INTEN = 0, then the integrators in the phase current channels are always disabled. If INTEN = 1, then the integrators in the phase currents channels are enabled. The neutral current channel integrator is managed by Bit 3 (ININTEN) of CONFIG3 register.
1	Reserved	1	Reserved. Maintain this bit at 1 for proper operation.
2	CF2DIS	0	When this bit is cleared to 0, the CF2 functionality is chosen at CF2/HREADY pin. When this bit is set to 1, the HREADY functionality is chosen at CF2/HREADY pin.
3	SWAP	0	When this bit is set to 1, the voltage channel outputs are swapped with the current channel outputs. Thus, the current channel information is present in the voltage channel registers and vice versa.
4	MOD1SHORT	0	When this bit is set to 1, the voltage channel ADCs behave as if the voltage inputs were put to ground.
5	MOD2SHORT	0	When this bit is set to 1, the current channel ADCs behave as if the voltage inputs were put to ground.
6	HSDCEN	0	When this bit is set to 1, the HSDC serial port is enabled and HSCLK functionality is chosen at CF3/HSCLK pin. When this bit is cleared to 0, HSDC is disabled and CF3 functionality is chosen at CF3/HSCLK pin.
7	SWRST	0	When this bit is set to 1, a software reset is initiated.
9:8	VTOIA[1:0]	00	These bits decide what phase voltage is considered together with Phase A current in the power path. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIA[1:0] = 00.
11:10	VTOIB[1:0]	00	These bits decide what phase voltage is considered together with Phase B current in the power path. 00 = Phase B voltage. 01 = Phase C voltage. 10 = Phase A voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIB[1:0] = 00.

Bit	Mnemonic	Default Value	Description
13:12	VTOIC[1:0]	00	These bits decide what phase voltage is considered together with Phase C current in the power path. 00 = Phase C voltage. 01 = Phase A voltage. 10 = Phase B voltage. 11 = reserved. When set, the ADE7880 behaves like VTOIC[1:0] = 00.
15:14	Reserved		Reserved.

Table 48. MMODE Register (Address 0xE700)

Bit	Mnemonic	Default Value	Description
1:0	Reserved		Reserved.
2	PEAKSEL[0]	1	PEAKSEL[2:0] bits can all be set to 1 simultaneously to allow peak detection on all three phases simultaneously. If more than one PEAKSEL[2:0] bits are set to 1, then the peak measurement period indicated in the PEAKCYC register decreases accordingly because zero crossings are detected on more than one phase. When this bit is set to 1, Phase A is selected for the voltage and current peak registers.
3	PEAKSEL[1]	1	When this bit is set to 1, Phase B is selected for the voltage and current peak registers.
4	PEAKSEL[2]	1	When this bit is set to 1, Phase C is selected for the voltage and current peak registers.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 49. ACCMODE Register (Address 0xE701)

Bit	Mnemonic	Default Value	Description
1:0	WATTACC[1:0]	00	00: signed accumulation mode of the total and fundamental active powers. The total and fundamental active energy registers and the CFx pulses are generated in the same way. 01: positive only accumulation mode of the total and fundamental active powers. In this mode, although the total and fundamental active energy registers are accumulated in positive only mode, the CFx pulses are generated in signed accumulation mode. 10: reserved. When set, the device behaves like WATTACC[1:0] = 00. 11: absolute accumulation mode of the total and fundamental active powers. The total and fundamental energy registers and the CFx pulses are generated in the same way.
3:2	VARACC[1:0]	00	00: signed accumulation of the fundamental reactive powers. The fundamental reactive energy registers and the CFx pulses are generated in the same way. 01: reserved. When set, the device behaves like VARACC[1:0] = 00. 10: the fundamental reactive power is accumulated, depending on the sign of the fundamental active power: if the active power is positive, the reactive power is accumulated as is, whereas if the active power is negative, the reactive power is accumulated with reversed sign. In this mode, although the total and fundamental reactive energy registers are accumulated in absolute mode, the CFx pulses are generated in signed accumulation mode. 11: absolute accumulation mode of the fundamental reactive powers. In this mode, although the total and fundamental reactive energy registers are accumulated in absolute mode, the CFx pulses are generated in signed accumulation mode.
5:4	CONSEL[1:0]	00	These bits select the inputs to the energy accumulation registers. IA′, IB′, and IC′ are IA, IB, and IC shifted respectively by −90°. See Table 50. 00: 3-phase four wires with three voltage sensors. 01: 3-phase three wires delta connection. In this mode, BVRMS register contains the rms value of VA-VC. 10: 3-phase four wires with two voltage sensors. 11: 3-phase four wires delta connection.

Bit	Mnemonic	Default Value	Description
6	REVAPSEL	0	0: The total active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC). 1: The fundamental active power on each phase is used to trigger a bit in the STATUS0 register as follows: on Phase A triggers Bit 6 (REVAPA), on Phase B triggers Bit 7 (REVAPB), and on Phase C triggers Bit 8 (REVAPC).
7	Reserved	1	Reserved. This bit does not manage any functionality.

Table 50. CONSEL[1:0] Bits in Energy Registers[1]

Energy Registers	CONSEL[1:0] = 00	CONSEL[1:0] = 01	CONSEL[1:0] = 10	CONSEL[1:0] = 11
AWATTHR, AFWATTHR	VA × IA	VA × IA	VA × IA	VA × IA
BWATTHR, BFWATTHR	VB × IB	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB ×IB[1]	VB × IB	VB × IB
CWATTHR, CFWATTHR	VC × IC	VC × IC	VC × IC	VC × IC
AVARHR, AFVARHR	VA × IA′	VA × IA′	VA × IA′	VA × IA′
BVARHR, BFVARHR	VB × IB′	VB = VA – VC	VB = –VA – VC	VB = –VA
		VB × IB′[1]	VB × IB′	VB × IB′
CVARHR, CFVARHR	VC ×IC′	VC × IC′	VC × IC′	VC × IC′
AVAHR	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms	VA rms × IA rms
BVAHR	VB rms × IB rms	VB rms × IB rms	VB rms × IB rms	VB rms × IB rms
		VB = VA – VC[1]	VB = –VA – VC	VB = –VA
CVAHR	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms	VC rms × IC rms

[1] In a 3-phase three wire case (CONSEL[1:0] = 01), the ADE7880 computes the rms value of the line voltage between Phase A and and Phase C and stores the result into BVRMS register (see the Voltage RMS in 3-Phase, 3-Wire Delta Configurations section). Consequently, the ADE7880 computes powers associated with Phase B that do not have physical meaning. To avoid any errors in the frequency output pins CF1, CF2 or CF3 related to the powers associated with Phase B, disable the contribution of Phase B to the energy to frequency converters by setting bits TERMSEL1[1], or TERMSEL2[1], or TERMSEL3[1] to 0 in the COMPMODE register (see the Energy-to-Frequency Conversion section).

Table 51. LCYCMODE Register (Address 0xE702)

Bit	Mnemonic	Default Value	Description
0	LWATT	0	0: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed in regular accumulation mode. 1: the watt-hour accumulation registers (AWATTHR, BWATTHR, CWATTHR, AFWATTHR, BFWATTHR, and CFWATTHR) are placed into line cycle accumulation mode.
1	LVAR	0	0: the var-hour accumulation registers (AFVARHR, BFVARHR, and CFVARHR) are placed in regular accumulation mode. 1: the var-hour accumulation registers (AFVARHR, BFVARHR, and CFVARHR) are placed into line-cycle accumulation mode.
2	LVA	0	0: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed in regular accumulation mode. 1: the VA-hour accumulation registers (AVAHR, BVAHR, and CVAHR) are placed into line-cycle accumulation mode.
3	ZXSEL[0]	1	0: Phase A is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase A is selected for zero-crossings counts in the line cycle accumulation mode. If more than one phase is selected for zero-crossing detection, the accumulation time is shortened accordingly.
4	ZXSEL[1]	1	0: Phase B is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase B is selected for zero-crossings counts in the line cycle accumulation mode.
5	ZXSEL[2]	1	0: Phase C is not selected for zero-crossings counts in the line cycle accumulation mode. 1: Phase C is selected for zero-crossings counts in the line cycle accumulation mode.
6	RSTREAD	1	0: read-with-reset of all energy registers is disabled. Clear this bit to 0 when Bits[2:0] (LWATT, LVAR, and LVA) are set to 1. 1: enables read-with-reset of all xWATTHR, xVARHR, xVAHR, xFWATTHR, and xFVARHR registers. This means a read of those registers resets them to 0.

Bit	Mnemonic	Default Value	Description
7	PFMODE	0	0: power factor calculation uses instantaneous values of various phase powers used in its expression. 1: power factor calculation uses phase energies values calculated using line cycle accumulation mode. Bits LWATT and LVA in LCYCMODE register must be enabled for the power factors to be computed correctly. The update rate of the power factor measurement in this case is the integral number of half line cycles that are programmed into the LINECYC register.

Table 52. HSDC_CFG Register (Address 0xE706)

Bit	Mnemonic	Default Value	Description
0	HCLK	0	0: HSCLK is 8 MHz. 1: HSCLK is 4 MHz.
1	HSIZE	0	0: HSDC transmits the 32-bit registers in 32-bit packages, most significant bit first. 1: HSDC transmits the 32-bit registers in 8-bit packages, most significant bit first.
2	HGAP	0	0: no gap is introduced between packages. 1: a gap of seven HCLK cycles is introduced between packages.
4:3	HXFER[1:0]	00	00 = HSDC transmits sixteen 32-bit words in the following order: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, INWV, AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. 01 = HSDC transmits seven instantaneous values of currents and voltages: IAWV, VAWV, IBWV, VBWV, ICWV, VCWV, and INWV. 10 = HSDC transmits nine instantaneous values of phase powers: AVA, BVA, CVA, AWATT, BWATT, CWATT, AFVAR, BFVAR, and CFVAR. 11 = reserved. If set, the ADE7880 behaves as if HXFER[1:0] = 00.
5	HSAPOL	0	0: $\overline{SS}$/has output pin is active low. 1: $\overline{SS}$/HSA output pin is active high.
7:6	Reserved	00	Reserved. These bits do not manage any functionality.

Table 53. CONFIG3 Register (Address 0xEA00)

Bit	Mnemonic	Default Value	Description
0	HPFEN	1	When HPFEN = 1, then all high-pass filters in voltage and current channels are enabled. When HPFEN = 0, then all high-pass filters are disabled.
1	LPFSEL	0	When LPFSEL = 0, the LPF in the total active power data path introduces a settling time of 650 ms. When LPFSEL = 1, the LPF in the total active power data path introduces a settling time of 1300 ms.
2	INSEL	0	When INSEL = 0, the register NIRMS contains the rms value of the neutral current. When INSEL = 1, the register NIRMS contains the rms value of ISUM, the instantaneous value of the sum of all 3 phase currents, IA, IB, and IC.
3	ININTEN	0	This bit manages the integrator in the neutral current channel. If ININTEN = 0, then the integrator in the neutral current channel is disabled. If ININTDIS = 1, then the integrator in the neutral channel is enabled. The integrators in the phase currents channels are managed by Bit 0 (INTEN) of CONFIG register.
4	Reserved	0	Reserved. Maintain this bit at 0 for proper operation.
7:5	Reserved	000	Reserved. These bits do not manage any functionality.

Table 54. HCONFIG Register (Address 0xE900)

Bit	Mnemonic	Default Value	Description
0	HRCFG	0	When this bit is cleared to 0, the Bit 19 (HREADY) interrupt in MASK0 register is triggered after a certain delay period. The delay period is set by bits HSTIME. The update frequency after the settling time is determined by bits HRATE. When this bit is set to 1, the Bit 19 (HREADY) interrupt in MASK0 register is triggered starting immediately after the harmonic calculations block has been setup. The update frequency is determined by Bits HRATE.
2:1	HPHASE	00	These bits decide what phase or neutral is analyzed by the harmonic calculations block. 00 = Phase A voltage and current. 01 = Phase B voltage and current. 10 = Phase C voltage and current. 11 = neutral current.
4:3	HSTIME	01	These bits decide the delay period after which, if HRCFG bit is set to 0, Bit 19 (HREADY) in the STATUS0 register is set to 1. 00 = 500 ms. 01 = 750 ms. 10 = 1000 ms. 11 = 1250 ms.
7:5	HRATE	000	These bits manage the update rate of the harmonic registers. 000 = 125 µs (8 kHz rate). 001 = 250 µs (4 kHz rate). 010 = 1 ms (1 kHz rate). 011 = 16 ms (62.5 Hz rate). 100 = 128 ms (7.8125 Hz rate). 101 = 512 ms (1.953125 Hz rate). 110 = 1.024 sec (0.9765625 Hz rate). 111 = harmonic calculations disabled.
9:8	ACTPHSEL	00	These bits select the phase voltage used as time base for harmonic calculations. 00 = Phase A voltage. 01 = Phase B voltage. 10 = Phase C voltage. 11 = reserved. If selected, phase C voltage is used.
15:10	Reserved	0	Reserved. These bits do not manage any functionality.

Table 55. LPOILVL Register (Address 0xEC00)

Bit	Mnemonic	Default Value	Description
2:0	LPOIL[2:0]	111	Threshold is put at a value corresponding to full scale multiplied by LPOIL/8.
7:3	LPLINE[4:0]	00000	The measurement period is (LPLINE + 1)/50 seconds.

Table 56. CONFIG2 Register (Address 0xEC01)

Bit	Mnemonic	Default Value	Description
0	EXTREFEN	0	When this bit is 0, it signifies that the internal voltage reference is used in the ADCs. When this bit is 1, an external reference is connected to the Pin 17 $REF_{IN/OUT}$.
1	I2C_LOCK	0	When this bit is 0, the $\overline{SS}$/HSA pin can be toggled three times to activate the SPI port. If I^2C is the active serial port, this bit must be set to 1 to lock it in. From this moment on, toggling of the $\overline{SS}$/HSA pin and an eventual switch into using the SPI port is no longer possible. If SPI is the active serial port, any write to CONFIG2 register locks the port. From this moment on, a switch into using I^2C port is no longer possible. Once locked, the serial port choice is maintained when the ADE7880 changes PSMx power modes.
7:2	Reserved	0	Reserved. These bits do not manage any functionality.

OUTLINE DIMENSIONS

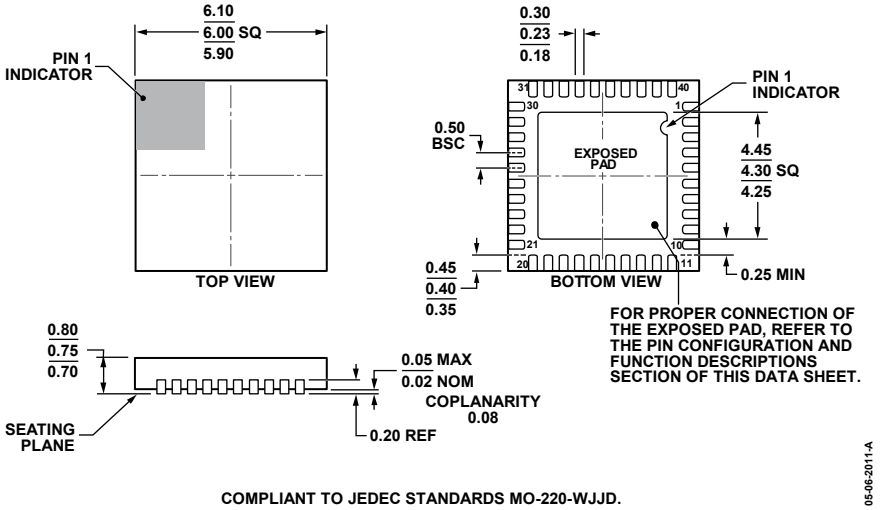

Figure 118. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm Body, Very Very Thin Quad
(CP-40-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADE7880ACPZ	−40°C to +85°C	40-Lead LFCSP_WQ	CP-40-10
ADE7880ACPZ-RL	−40°C to +85°C	40-Lead LFCSP_WQ, 13" Tape and Reel	CP-40-10
EVAL-ADE7880EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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