



**THE DATASHEET OF  
ADG201HSJN**



### FEATURES

**50ns max Switching Time Over Full Temperature Range**

**Low R<sub>ON</sub> (30Ω typ)**

**Single Supply Specifications for +10.8V to +16.5V Operation**

**Extended Plastic Temperature Range (-40°C to +85°C)**

**Break-Before-Make Switching**

**Low Leakage (100pA typ)**

**44V Supply max Rating**

**Available in 16-Lead DIP/SOIC and 20-Lead LCCC/PLCC Packages**

**ADG201HS (K, B, T) Replaces HI-201HS**

**ADG201HS (J, A, S) Replaces DG271**

### GENERAL DESCRIPTION

The ADG201HS is a monolithic CMOS device comprising four independently selectable SPST switches. It is designed on an enhanced LC<sup>2</sup>MOS process which gives very fast switching speeds and low R<sub>ON</sub>.

The switches also feature break-before-make switching action for use in multiplexer applications and low charge injection for minimum transients on the output when switching the digital inputs.

### ORDERING GUIDE

| Model <sup>1</sup>      | Temperature Range | Package Option <sup>2</sup> |
|-------------------------|-------------------|-----------------------------|
| ADG201HSJN              | -40°C to +85°C    | N-16                        |
| ADG201HSKN              | -40°C to +85°C    | N-16                        |
| ADG201HSKR              | -40°C to +85°C    | R-16                        |
| ADG201HSAQ              | -40°C to +85°C    | Q-16                        |
| ADG201HSBQ              | -40°C to +85°C    | Q-16                        |
| ADG201HSJP              | -40°C to +85°C    | P-20A                       |
| ADG201HSKP              | -40°C to +85°C    | P-20A                       |
| ADG201HSSQ              | -55°C to +125°C   | Q-16                        |
| ADG201HSTQ <sup>3</sup> | -55°C to +125°C   | Q-16                        |
| ADG201HSTE <sup>3</sup> | -55°C to +125°C   | E-20A                       |

#### NOTES

<sup>1</sup>To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers. See the Analog Devices Military Products Databook (1994) for military data sheet.

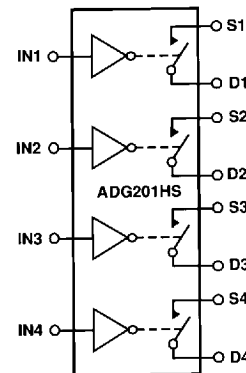
<sup>2</sup>E = Leadless Ceramic Chip Carrier; N = Narrow Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = 0.15" Small Outline IC (SOIC).

<sup>3</sup>Standard Military Drawing (SMD) approved by DESC. SMD numbers are

5962-86716012X (ADG201HSTE/883B)

5962-8671601EX (ADG201HSTQ/883B)

### FUNCTIONAL BLOCK DIAGRAM



### PRODUCT HIGHLIGHTS

#### 1. 50ns max t<sub>ON</sub> and t<sub>OFF</sub>:

The ADG201HS top grades (K, B, T) have guaranteed 50ns max turn-on and turn-off times over the full operating temperature range. The lower grades (J,A,S) have guaranteed 75ns switching times over the full operating temperature range.

#### 2. Single Supply Specifications:

The ADG201HS is fully specified for applications which require a single positive power supply in the +10.8V to +16.5V range.

#### 3. Low Leakage:

Leakage currents in the range of 100pA make these switches suitable for high precision circuits. The added feature of break-before-make allows for multiple outputs to be tied together for multiplexer applications while keeping leakage errors to a minimum.

| IN | Switch Condition |
|----|------------------|
| 0  | ON               |
| 1  | OFF              |

Truth Table

### REV. B

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# ADG201HS — SPECIFICATIONS

**DUAL SUPPLY** ( $V_{DD} = +13.5V$  to  $+16.5V$ ,  $= -13.5V$  to  $-16.5V$ ,  $GND = 0V$ ,  
 $V_{IN} = 3V$  [Logic High Level] or  $0.8V$  [Logic Low Level] unless otherwise noted)

| Parameter                                    | Version    | +25°C    | $T_{min} - T_{max}^1$ | Units        | Comments   |
|--|------------|----------|-----------------------|--------------|--|
| <b>ANALOG SWITCH</b>                         |            |          |                       |              |  |
| Analog Signal Range                          | All        | $V_{SS}$ | $V_{SS}$              | V min        |  |
|  | All        | $V_{DD}$ | $V_{DD}$              | V max        |  |
| $R_{ON}$                                     | All        | 30       | —                     | $\Omega$ typ | $-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$ ; Test Circuit 1                        |
|  | All        | 50       | 75                    | $\Omega$ max |  |
| $R_{ON}$ Drift                               | All        | 0.5      | —                     | %/°C typ     | $-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$   |
| $R_{ON}$ Match                               | All        | 3        | —                     | % typ        | $-10V \leq V_S \leq +10V$ , $I_{DS} = 1mA$   |
| $I_S$ (OFF), Off Input Leakage <sup>2</sup>  | All        | 0.1      | —                     | nA typ       | $V_D = \pm 14V$ ; $V_S = \mp 14V$ ; Test Circuit 2                                 |
|  | J, K, A, B | 1        | 20                    | nA max       |  |
|  | S, T       | 1        | 60                    | nA max       |  |
| $I_D$ (OFF), Off Output Leakage <sup>2</sup> | All        | 0.1      | —                     | nA typ       | $V_D = \pm 14V$ ; $V_S = \mp 14V$ ; Test Circuit 2                                 |
|  | J, K, A, B | 1        | 20                    | nA max       |  |
|  | S, T       | 1        | 60                    | nA max       |  |
| $I_D$ (ON), On Channel Leakage <sup>2</sup>  | All        | 0.1      | —                     | nA typ       | $V_D = V_S = \pm 14V$ ; Test Circuit 3   |
|  | J, K, A, B | 1        | 20                    | nA max       |  |
|  | S, T       | 1        | 60                    | nA max       |  |
| <b>DIGITAL CONTROL</b>                       |            |          |                       |              |  |
| $V_{INH}$ , Input High Voltage               | All        | 2.4      | 2.4                   | V min        |  |
| $V_{INL}$ , Input Low Voltage                | All        | 0.8      | 0.8                   | V max        |  |
| $I_{INL}$ or $I_{INH}$                       | All        | 1        | 1                     | $\mu A$ max  |  |
| $C_{IN}$                                     | All        | 8        | 8                     | pF max       |  |
| <b>DYNAMIC CHARACTERISTICS</b>               |            |          |                       |              |  |
| $t_{ON}$                                     | K, B, T    | 50       | 50                    | ns max       | Test Circuit 4   |
|  | J, A, S    | 75       | 75                    | ns max       |  |
| $t_{OFF1}$                                   | K, B, T    | 50       | 50                    | ns max       | Test Circuit 4   |
|  | J, A, S    | 75       | 75                    | ns max       |  |
| $t_{OFF2}$                                   | All        | 150      | —                     | ns typ       | Test Circuit 4   |
| $t_{OPEN}$                                   | All        | 5        | 5                     | ns typ       | $t_{ON} - t_{OFF1}$ ; Test Circuit 4   |
| Output Settling Time to 0.1%                 | All        | 180      | —                     | ns typ       | $V_{IN} = 3V$ to $0V$ ; Test Circuit 4   |
| OFF Isolation                                | All        | 72       | —                     | dB typ       | $V_S = 3V$ rms, $f = 100kHz$ , $R_L = 1k\Omega$ ;<br>$C_L = 10pF$ ; Test Circuit 5 |
| Channel-to-Channel Crosstalk                 | All        | 86       | —                     | dB typ       | $V_S = 3V$ rms, $f = 100kHz$ , $R_L = 1k\Omega$ ;<br>$C_L = 10pF$ ; Test Circuit 6 |
| $Q_{INJ}$ , Charge Injection                 | All        | 10       | —                     | pC typ       | $R_S = 0\Omega$ , $V_S = 0V$ ; Test Circuit 7                                      |
| $C_S$ (OFF)                                  | All        | 10       | —                     | pF typ       |  |
| $C_D$ (OFF)                                  | All        | 10       | —                     | pF typ       |  |
| $C_D$ , $C_S$ (ON)                           | All        | 30       | —                     | pF typ       |  |
| $C_{DS}$ (OFF)                               | All        | 0.5      | —                     | pF typ       |  |
| <b>POWER SUPPLY</b>                          |            |          |                       |              |  |
| $I_{DD}$                                     | All        | 10       | 10                    | mA max       |  |
| $I_{SS}$                                     | All        | 6        | 6                     | mA max       |  |
| Power Dissipation                            | All        | 240      | 240                   | mW max       | $V_{DD} = +15V$ , $V_{SS} = -15V$  |

## NOTES

<sup>1</sup>Temperature ranges are as follows: ADG201HSJ, K;  $-40^\circ C$  to  $+85^\circ C$   
 ADG201HSA, B;  $-40^\circ C$  to  $+85^\circ C$   
 ADG201HSS, T;  $-55^\circ C$  to  $+125^\circ C$

<sup>2</sup>Leakage specifications apply with a  $V_D$  ( $V_S$ ) of  $\pm 14V$  or with a  $V_D$  ( $V_S$ ) of  $0.5V$  within the supply voltages ( $V_{DD}$ ,  $V_{SS}$ ), whichever is the minimum.  
 Specifications subject to change without notice.

**SINGLE SUPPLY** ( $V_{DD} = +10.8V$  to  $+16.5V$ ,  $V_{SS} = GND = 0V$ ,  $V_{IN} = 3V$  [Logic High Level] or  $0.8V$  [Logic Low Level] unless otherwise noted)

| Parameter                                    | Version    | +25°C    | $T_{min} - T_{max}$ | Units        | Comments   |
|--|------------|----------|---------------------|--------------|--|
| <b>ANALOG SWITCH</b>                         |            |          |                     |              |  |
| Analog Signal Range                          | All        | $V_{SS}$ | $V_{SS}$            | V min        |  |
|  | All        | $V_{DD}$ | $V_{DD}$            | V max        |  |
| $R_{ON}$                                     | All        | 65       | –                   | $\Omega$ typ | $0V \leq V_S \leq +10V$ , $I_{DS} = 1mA$ ; Test Circuit 1                          |
|  | All        | 90       | 120                 | $\Omega$ max |  |
| $R_{ON}$ Drift                               | All        | 0.5      | –                   | %/°C typ     | $0V \leq V_S \leq +10V$ , $I_{DS} = 1mA$   |
| $R_{ON}$ Match                               | All        | 3        | –                   | % typ        | $0V \leq V_S \leq +10V$ , $I_{DS} = 1mA$   |
| $I_S$ (OFF), Off Input Leakage <sup>1</sup>  | All        | 0.1      | –                   | nA typ       | $V_D = +10V/+0.5V$ ; $V_S = +0.5V/+10V$ ; Test Circuit 2                           |
|  | J, K, A, B | 1        | 20                  | nA max       |  |
|  | S, T       | 1        | 60                  | nA max       |  |
| $I_D$ (OFF), Off Output Leakage <sup>1</sup> | All        | 0.1      | –                   | nA typ       | $V_D = +10V/+0.5V$ ; $V_S = +0.5V/+10V$ ; Test Circuit 2                           |
|  | J, K, A, B | 1        | 20                  | nA max       |  |
|  | S, T       | 1        | 60                  | nA max       |  |
| $I_D$ (ON), On Channel Leakage <sup>1</sup>  | All        | 0.1      | –                   | nA typ       | $V_D = V_S = +10V/+0.5V$ ; Test Circuit 3  |
|  | J, K, A, B | 1        | 20                  | nA max       |  |
|  | S, T       | 1        | 60                  | nA max       |  |
| <b>DIGITAL CONTROL</b>                       |            |          |                     |              |  |
| $V_{INH}$ , Input High Voltage               | All        | 2.4      | 2.4                 | V min        |  |
| $V_{INL}$ , Input Low Voltage                | All        | 0.8      | 0.8                 | V max        |  |
| $I_{INL}$ or $I_{INH}$                       | All        | 1        | 1                   | $\mu A$ max  |  |
| $C_{IN}$                                     | All        | 8        | 8                   | pF max       |  |
| <b>DYNAMIC CHARACTERISTICS</b>               |            |          |                     |              |  |
| $t_{ON}$                                     | K, B, T    | 50       | 70                  | ns max       | Test Circuit 4   |
|  | J, A, S    | 75       | 90                  | ns max       |  |
| $t_{OFF1}$                                   | K, B, T    | 50       | 70                  | ns max       | Test Circuit 4   |
|  | J, A, S    | 75       | 90                  | ns max       |  |
| $t_{OFF2}$                                   | All        | 150      | –                   | ns typ       | Test Circuit 4   |
| $t_{OPEN}$                                   | All        | 5        | 5                   | ns typ       | $t_{ON} - t_{OFF1}$ ; Test Circuit 4   |
| Output Settling Time to 0.1%                 | All        | 180      | –                   | ns typ       | $V_{IN} = 3V$ to $0V$ ; Test Circuit 4   |
| OFF Isolation                                | All        | 72       | –                   | dB typ       | $V_S = 3V$ rms, $f = 100kHz$ , $R_L = 1k\Omega$ ;<br>$C_L = 10pF$ ; Test Circuit 5 |
| Channel-to-Channel Crosstalk                 | All        | 86       | –                   | dB typ       | $V_S = 3V$ rms, $f = 100kHz$ , $R_L = 1k\Omega$ ;<br>$C_L = 10pF$ ; Test Circuit 6 |
| $Q_{INJ}$ , Charge Injection                 | All        | 10       | –                   | pC typ       | $R_S = 0\Omega$ , $V_S = 0V$ ; Test Circuit 7                                      |
| $C_S$ (OFF)                                  | All        | 10       | –                   | pF typ       |  |
| $C_D$ (OFF)                                  | All        | 10       | –                   | pF typ       |  |
| $C_D$ , $C_S$ (ON)                           | All        | 30       | –                   | pF typ       |  |
| $C_{DS}$ (OFF)                               | All        | 0.5      | –                   | pF typ       |  |
| <b>POWER SUPPLY</b>                          |            |          |                     |              |  |
| $I_{DD}$                                     | All        | 10       | 10                  | mA max       |  |
| Power Dissipation                            | All        | 150      | 150                 | mW max       | $V_{DD} = +15V$  |

## NOTE

<sup>1</sup>The leakage specifications degrade marginally (typically 1nA at 25°C) with  $V_D(V_S) = V_{SS}$ .

Specifications subject to change without notice.

# ADG201HS

## ABSOLUTE MAXIMUM RATINGS\*

(T<sub>A</sub> = 25°C unless otherwise noted)

|  |  |
|--|--|
| V <sub>DD</sub> to V <sub>SS</sub> . . . . .       | 44V  |
| V <sub>DD</sub> to GND . . . . .                   | -0.3V, 25V   |
| V <sub>SS</sub> to GND <sup>1</sup> . . . . .      | +0.3V, -25V  |
| Analog Inputs <sup>2</sup>                         |  |
| Voltage at S, D . . . . .                          | V <sub>SS</sub> - 2V to V <sub>DD</sub> + 2V or 20mA, Whichever Occurs First |
| Continuous Current, S or D . . . . .               | 20mA   |
| Pulsed Current S or D . . . . .                    | 20mA   |
| I <sub>ms</sub> Duration, 10% Duty Cycle . . . . . | 70mA   |
| Digital Inputs <sup>2</sup>                        |  |
| Voltage at IN . . . . .                            | V <sub>SS</sub> - 4V to V <sub>DD</sub> + 4V or 20mA, Whichever Occurs First |

## Power Dissipation (Any Package)

|                                  |        |
|----------------------------------|--------|
| Up to +75°C . . . . .            | 470mW  |
| Derates above +75°C by . . . . . | 6mW/°C |

## Operating Temperature

|  |                 |
|--|-----------------|
| Commerical (J, K Version) . . . . .          | -40°C to +85°C  |
| Industrial (A, B Version) . . . . .          | -40°C to +85°C  |
| Extended (S, T Version) . . . . .            | -55°C to +125°C |
| Storage Temperature Range . . . . .          | -65°C to +150°C |
| Lead Temperature (Soldering 10sec) . . . . . | +300°C          |

## NOTES

<sup>1</sup>If V<sub>SS</sub> is open circuited with V<sub>DD</sub> and GND applied, the V<sub>SS</sub> pin will be pulled positive, exceeding the Absolute Maximum Ratings. If this possibility exists, a Schottky diode from V<sub>SS</sub> to GND (cathode end to GND) ensures that the Absolute Maximum Ratings will be observed.

<sup>2</sup>Overtoltage at IN, S or D, will be clamped by diodes. Current should be limited to the maximum rating above.

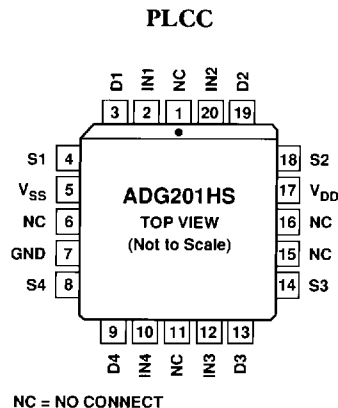
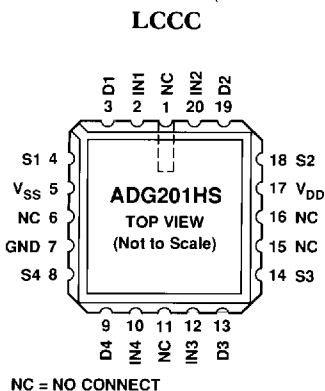
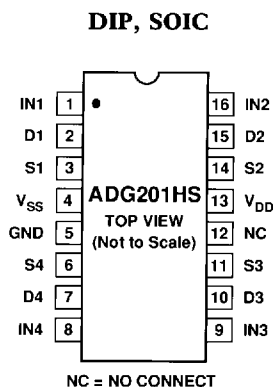
\*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## CAUTION:

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

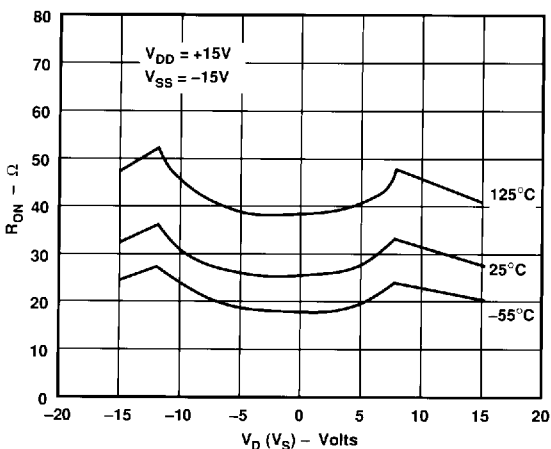


## PIN CONFIGURATIONS

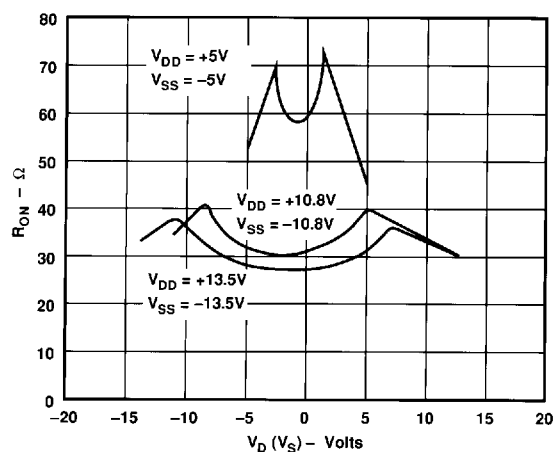


# Typical Performance Characteristics—ADG201HS

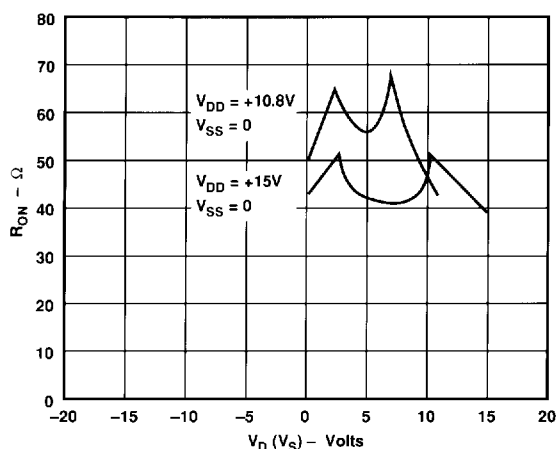
The switches are guaranteed functional with reduced single or dual supplies down to 4.5V.



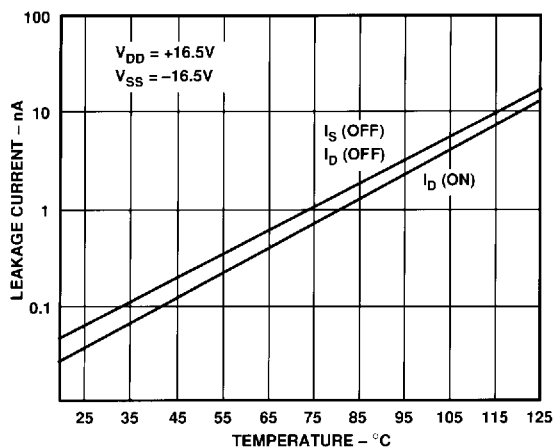
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply Voltage



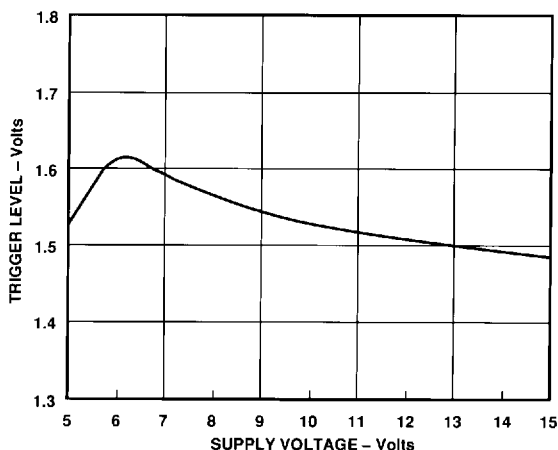
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply Voltage,  $T_A = +25^\circ\text{C}$



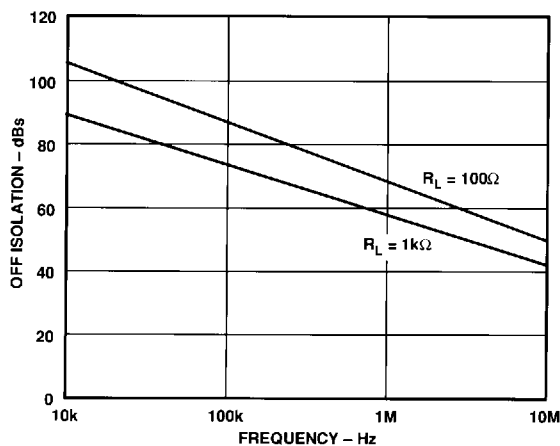
$R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Supply Voltage,  $T_A = +25^\circ\text{C}$



Leakage Current as a Function of Temperature Dual Supply Voltage. (Note: Leakage Currents Reduce as the Supply Voltages Reduce)

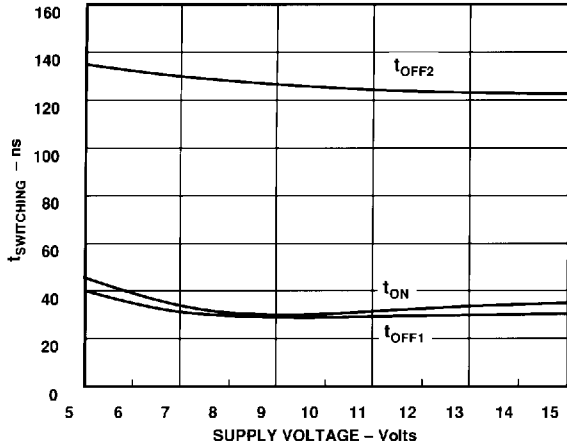


Trigger Levels vs. Power Supply Voltage, Dual or Single Supply,  $T_A = +25^\circ\text{C}$

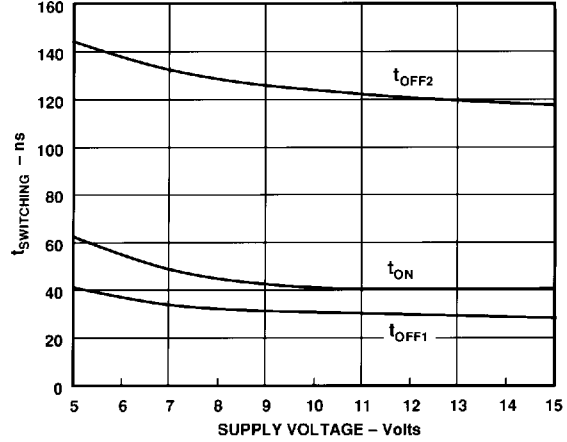


Off Isolation vs. Signal Frequency; Dual or Single 15V Supplies,  $T_A = +25^\circ\text{C}$

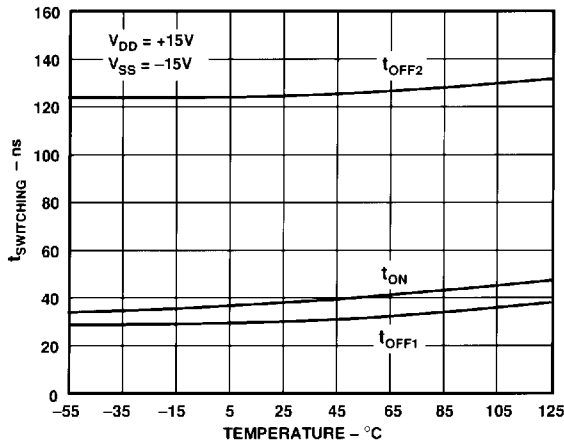
# ADG201HS—Typical Performance Characteristics (Continued)



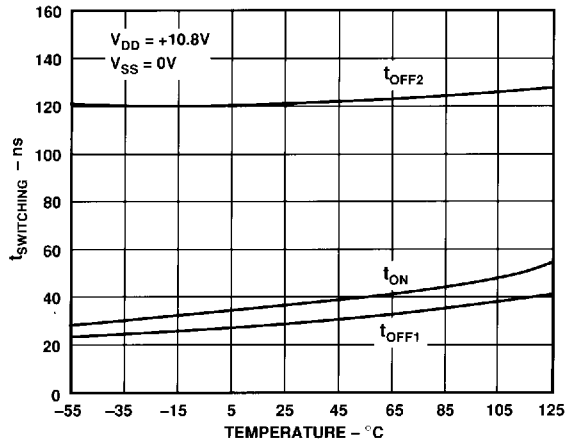
Switching Time vs. Supply Voltage (Dual Supply):  
 $T_A = +25^\circ\text{C}$ . (Note: See Test Circuit 4.)  
 For  $V_{DD} < 10\text{V}$ ,  $V_S = V_{DD}$



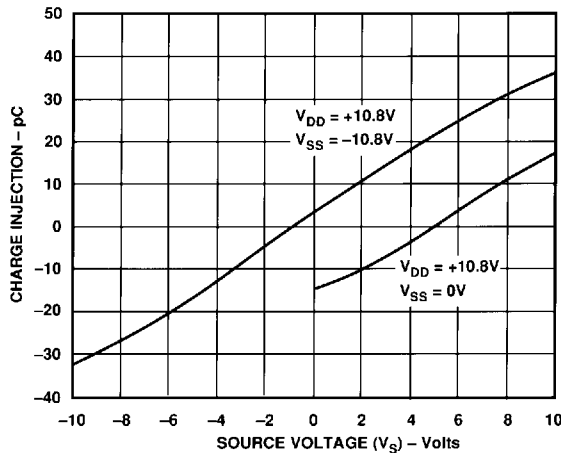
Switching Time vs. Supply Voltage (Single Supply):  
 $T_A = +25^\circ\text{C}$ . (Note: See Test Circuit 4.)  
 For  $V_{DD} < 10\text{V}$ ,  $V_S = V_{DD}$



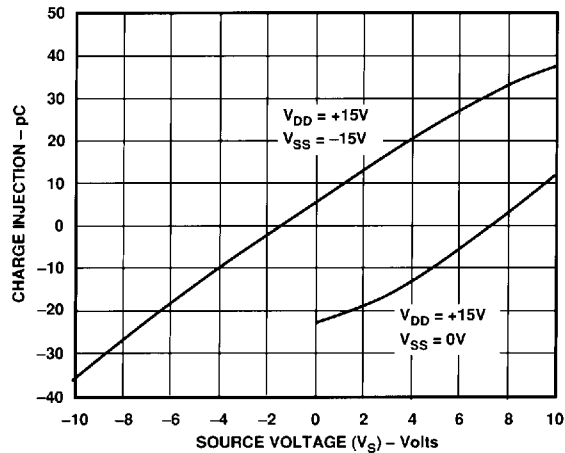
Switching Time vs. Temperature: Dual Supply Voltage



Switching Time vs. Temperature: Single Supply Voltage



Charge Injection vs. Source Voltage ( $V_S$ ) for Dual and Single 10.8V Supplies:  $T_A = +25^\circ\text{C}$

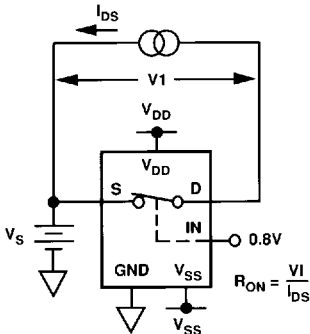


Charge Injection vs. Source Voltage ( $V_S$ ) for Dual and Single 15V Supplies:  $T_A = +25^\circ\text{C}$

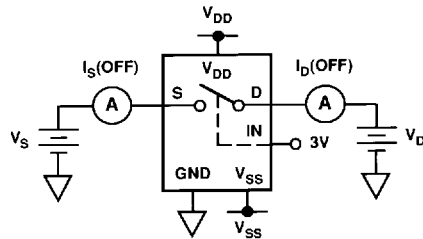
# Test Circuits—ADG201HS

Note: All digital input signal rise and fall times measured from 10% to 90% of 3V.  $t_R = t_F = 5\text{ns}$ . Decoupling capacitors ( $0.01\mu\text{F}$  min) from  $V_{DD}$  and  $V_{SS}$  to GND are recommended to achieve specified performance.

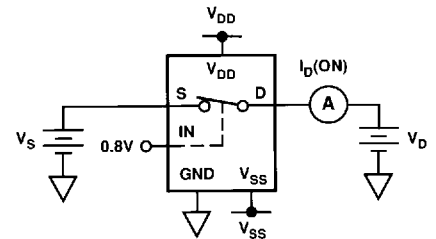
**TEST CIRCUIT 1**  
 **$R_{ON}$**



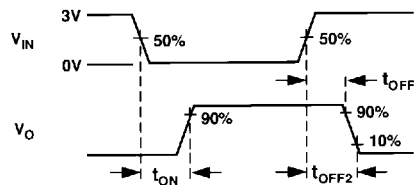
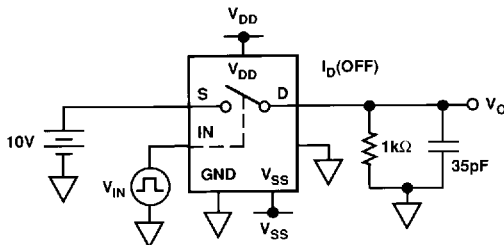
**TEST CIRCUIT 2**  
 **$I_S(\text{OFF}), I_D(\text{OFF})$**



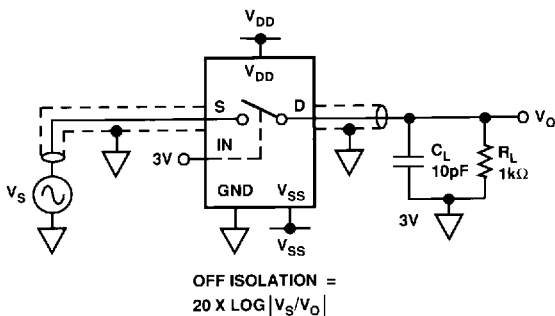
**TEST CIRCUIT 3**  
 **$I_D(\text{ON})$**



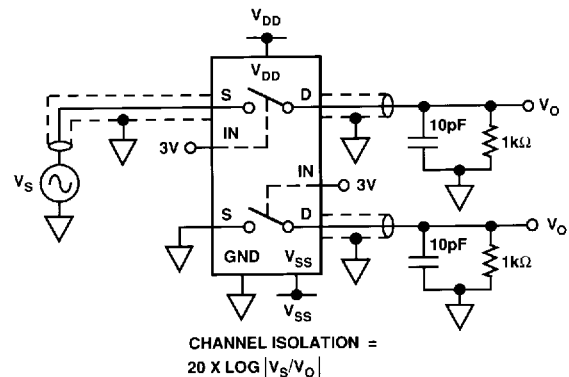
**TEST CIRCUIT 4**  
 **$t_{ON}, t_{OFF}, t_{OPEN}, \text{SETTLING TIME}$**



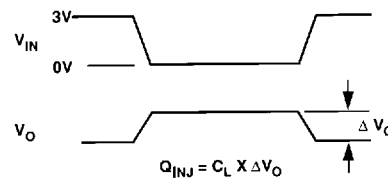
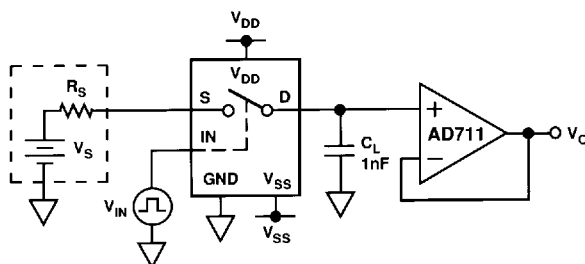
**TEST CIRCUIT 5**  
**OFF ISOLATION**



**TEST CIRCUIT 6**  
**CHANNEL-TO-CHANNEL CROSSTALK**



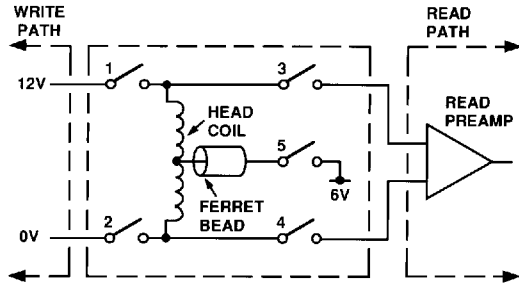
**TEST CIRCUIT 7**  
**CHARGE INJECTION**



# ADG201HS

## SINGLE SUPPLY DISK DRIVE APPLICATION

The excellent performance of the ADG201HS with single supply operation makes it suitable in applications such as disk drives where only positive power supply voltages are normally available. The accompanying circuit shows a typical application for the ADG201HS in the read/write head switching section of a disk drive. The circuit allows data (0s and 1s) to be written to and read from a disk. The principal advantage offered by the ADG201HS is that it retains very fast switching speed with single supply operation (see Single Supply Specifications). This allows disk drives to run at higher data rates.



SWITCHES 1 TO 5 ALL ADG201HS

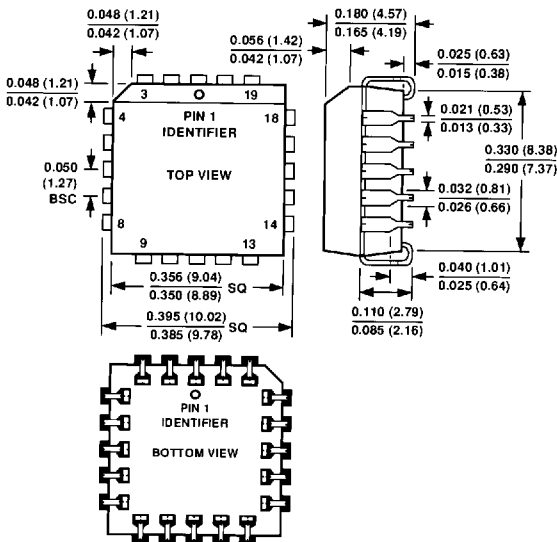
| SWITCH NUMBER | WRITE |     | READ |
|---------------|-------|-----|------|
|               | "0"   | "1" |      |
| 1             | OFF   | ON  | OFF  |
| 2             | ON    | OFF | OFF  |
| 3             | OFF   | OFF | ON   |
| 4             | OFF   | OFF | ON   |
| 5             | ON    | ON  | OFF  |

ADG201HS in the Read/Write Head Switching Circuit of a Disk Drive

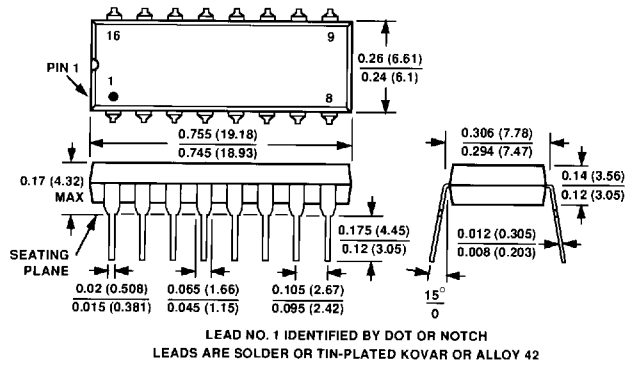
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

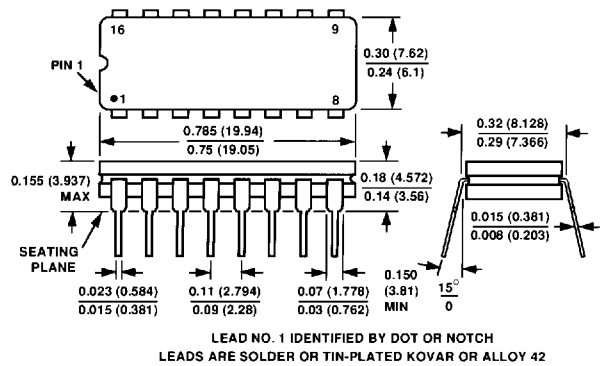
### 20-Terminal Plastic Leaded Chip Carrier (P-20A)



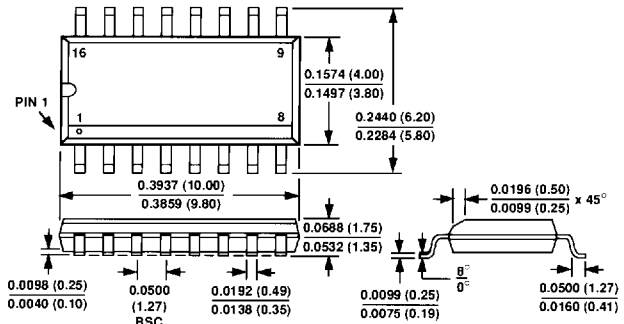
### 16-Pin Plastic DIP (N-16)



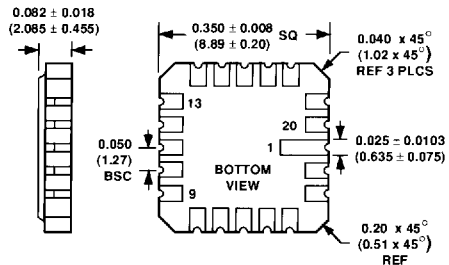
### 16-Pin Cerdip (Q-16)



### 16-Lead Narrow Body SOIC (R-16A)



### 20-Terminal Leadless Ceramic Chip Carrier (E-20A)



C1178-10-4 RR

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