THE DATASHEET OF

ADM1075-1ACPZ

–48 V Hot Swap Controller and Digital Power Monitor with PMBus Interface

Data Sheet **ADM1075**

FEATURES

- **Constant power foldback for FET SOA protection**
- **Precision (<1.0%) current and voltage measurement**
- **Controls inrush and faults for negative supply voltages**
- **Suitable for wide input range due to internal shunt regulator**
- **25 mV/50 mV full-scale sense voltage**
- **Fine tune current limit to allow use of standard sense resistor**
- **Soft start inrush current limit profiling**
- **1% accurate UVH and OV pins, 1.5% accurate UVL pin**
- **PMBus/I²C interface for control, telemetry, and fault recording**
- **28-lead LFCSP and TSSOP**
- **–40°C to 105°C junction temperature (T_J) operating range**

APPLICATIONS

- **Telecommunication and data communication equipment**
- **Central office switching**
- **–48 V distributed power systems**
- **Negative power supply control**
- **High availability servers**

PRODUCT HIGHLIGHTS

1. Constant Power Foldback.
   Maximum FET power set by a PLIM resistor divider. This eases complexity when designing to maintain FET SOA.
2. Adjustable Current Limit.
   The current limit is adjustable via the ISET pin allowing for the use of a standard value sense resistor.
3. 12-Bit ADC.
   Accurate voltage, current, and power measurements. Also enables calculation of energy consumption over time.
4. PMBus/I²C Interface.
   PMBus fast mode compliant interface used to read back status and data registers and set warning and fault limits.
5. Fault Recording.
   Latched status registers provide useful debugging information to help trace faults in high reliability systems.
6. Built-In Soft Start.
   Soft start capacitor controls inrush current profile with di/dt control.

FUNCTIONAL BLOCK DIAGRAM

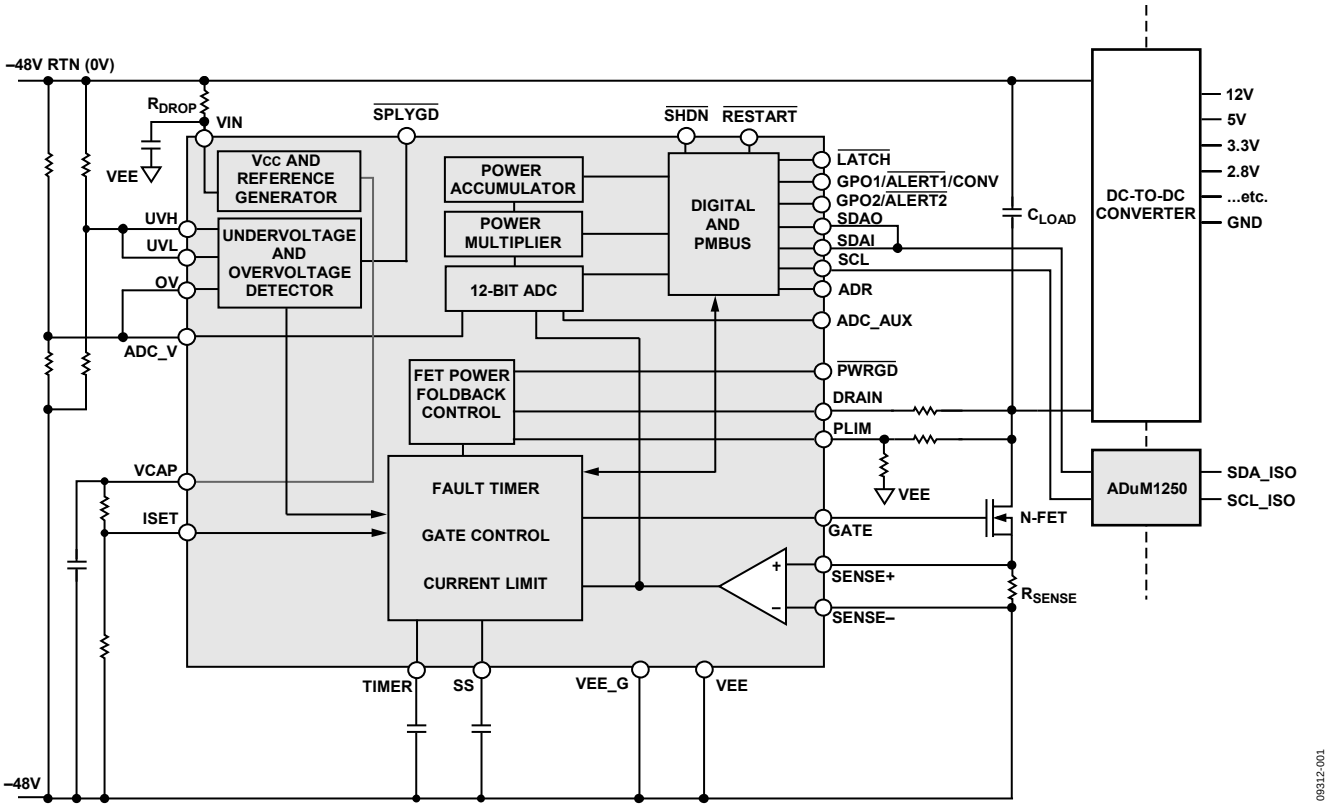

Figure 1.

Rev. D **Document Feedback**

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REVISION HISTORY

1/2018—Rev. C to Rev. D

Changed CP-28-6 to CP-28-10 ..... Throughout
Changes to Operation Command Register Section and Table 9 39
Changes to Device Configuration Register Section and Table 36 49
Updated Outline Dimensions 51
Changes to Ordering Guide 52

4/2014—Rev. B to Rev. C

Added Setting a Linear Output Voltage Ramp at Power-Up Section and Figure 51; Renumbered Sequentially 24

4/2013—Rev. A to Rev. B

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Added I Partial Transactions on I^2C Bus Section 28
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3/2012—Rev. 0 to Rev. A

Added 28-Lead LFCSP ..... Universal
Changes to Features Section and Product Highlights Section 1
Changes to ADC Conversion Time comments in Table 1 8
Changes to Table 4 10
Added Figure 4; Renumbered Sequentially; and changes to Table 5 11
Changes to Current Limit Reference Section 21
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10/2011—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM1075 is a full feature, negative voltage, hot swap controller with constant power foldback and high accuracy digital current and voltage measurement that allows boards to be safely inserted and removed from a live −48 V backplane. The part provides precise and robust current limiting and protection against both transient and nontransient short circuits and overvoltage and undervoltage conditions. The ADM1075 typically operates from a negative voltage of −35 V to −80 V and, due to shunt regulation, has excellent voltage transient immunity. The operating range of the part is flexible due to the shunt regulator, and the part can be powered directly by a 10 V rail to save shunt power dissipation (see the Powering the ADM1075 section for more details).

A full-scale current limit of 25 mV or 50 mV can be selected by choosing the appropriate model. The maximum current limit is set by the combination of the sense resistor, R_{SENSE}, and the input voltage on the ISET pin, using external resistors. This allows fine tuning of the trip voltage so that standard sense resistors can be used. Inrush current is limited to this programmable value by controlling the gate drive of an external N-channel FET. A built-in soft start function allows control of the inrush current profile by an external capacitor on the soft start (SS) pin.

An external capacitor on the TIMER pin determines the maximum allowed on-time for when the system is in current limit. This is based on the safe operating area (SOA) limits of the MOSFET. A constant power foldback scheme is used to control the power dissipation in the MOSFET during power-up and fault conditions. The ADM1075 regulates the current dynamically to ensure that the power in the MOSFET is within SOA limits as V_{DS} changes. After the timer has expired, the device shuts down the MOSFET. The level of this power, along with the TIMER regulation time, can be set to ensure that the MOSFET remains within the SOA limits.

The ADM1075 employs a limited consecutive retry scheme when the $\overline{\text{LATCH}}$ pin is tied to the $\overline{\text{SHDN}}$ pin. In this mode, if the load current reaches the limit, the FET gate is pulled low after the timer expires and retries after a cooling period for seven attempts only. If the fault remains, the device latches off, and the MOSFET is disabled until a manual restart is initiated. Alternatively, the ADM1075 can be set to retry only once by isolating the $\overline{\text{LATCH}}$ pin from the $\overline{\text{SHDN}}$ pin. The part can also be configured to retry an infinite number of times with a 10 second interval between restarts by connecting the GPO2 pin to the $\overline{\text{RESTART}}$ pin.

The ADM1075 has separate UVx and OV pins for undervoltage and overvoltage detection. The FET is turned off if a nontransient voltage less than the undervoltage threshold (typically −35 V) is detected on the UVx pins or if greater than the overvoltage threshold (typically −80 V) is detected on the OV pin. The operating voltage range of the ADM1075 is programmable via resistor networks on the UVx and OV pins. The hysteresis levels on the overvoltage detectors can also be altered by selecting the appropriate resistors. There are two separate UVx pins to allow accurate programming of hysteresis.

In the case of a short circuit, the ADM1075 has a fast response circuit to detect and respond adequately to this event. If the sense voltage exceeds 1.5 times the normal current limit, a high current (750 mA minimum) gate pull-down switch is activated to shut down the MOSFET as quickly as possible. There is a default internal glitch filter of 900 ns. If a longer filter time or different severe overcurrent limit is required, these parameters can be adjusted via the PMBus™ interface.

The ADM1075 also includes a 12-bit ADC to provide digital measurement of the voltage and load current. The current is measured at the output of the internal current sense amplifier and the voltage from the ADC_V input. This data can be read across the PMBus interface.

The PMBus interface allows a controller to read current, voltage, and power measurements from the ADC. Measurements can be initiated by a PMBus command or can be set up to run continuously. The user can read the latest conversion data whenever it is required. A power accumulator is also provided to report total power consumed in a user specified period (total energy). Up to four unique I^2C addresses can be created, depending on the configuration of the ADR pin.

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ outputs can be used as a flag to warn a microcontroller or FPGA of one or more fault/warning conditions becoming active. The fault type and level is programmed across the PMBus, and the user can select which faults/warnings activate the alert.

Other functions include

- $\overline{\text{PWRGD}}$ output, which can be used to enable a power module (the DRAIN and GATE pins are monitored to determine when the load capacitance is fully charged)
- $\overline{\text{SHDN}}$ input to manually disable the GATE drive
- $\overline{\text{RESTART}}$ input to remotely initiate a 10 second shutdown

SPECIFICATIONS

VEE = −48 V, V_{SENSE} = (V_{SENSE+} − V_{SENSE-}) = 0 mV, shunt regulation current = 10 mA, T_J = −40°C to +105°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SYSTEM SUPPLY					
Voltage Transient Immunity		−200		V	
Typical Operating Voltage	−80		−35	V	Determined by external component, R_{SHUNT}
SHUNT REGULATOR					
Operating Supply Voltage Range, VIN	11.5	12.3	13	V	Shunt regulation voltage, I_{IN} = 5.5 mA to 30 mA, maximum I_{IN} dependent on T_A, θ_{JA} (see the Powering the ADM1075 section)
Quiescent Supply Current			5.5	mA	VIN = 13 V
Undervoltage Lockout, V_{UVLO_RISING}			9.2	V	
Undervoltage Lockout Hysteresis			600	mV	
Power Directly Without Shunt	9.2		11.5	V	
UV PINS—UNDERVOLTAGE DETECTION					
Undervoltage Rising Threshold, V_{UVH}	0.99	1.0	1.01	V	
Undervoltage Falling Threshold, V_{UVL}	0.887	0.9	0.913	V	
Total Undervoltage Hysteresis		100		mV	When UVL and UVH are tied together
Undervoltage Fault Filter	3.5		7.5	µs	
UV Propagation Delay		5	8	µs	UV low to GATE pull-down active
UVL/UVH Input Current		1	50	nA	
OV PIN—OVERVOLTAGE DETECTION					
Overvoltage Rising Threshold, V_{OVR}	0.99	1.0	1.01	V	
Overvoltage Hysteresis Current	4.3	5	5.7	µA	
Overvoltage Fault Filter	1.75		3.75	µs	
OV Propagation Delay		2	4	µs	OV high to GATE pull-down active
OV Input Current		1	50	nA	
GATE PIN					
Gate Voltage High	11	12	13	V	I_{GATE} = −1.0 µA
Gate Voltage Low		10	100	mV	I_{GATE} = 100 µA
Pull-Up Current	−50		−30	µA	V_{GATE} = 0 V to 8 V; V_{SS} = 2 V
Pull-Down Current (Regulation)	100			µA	V_{GATE} ≥ 2 V
Pull-Down Current (UV/OV/OC)	5	10		mA	V_{GATE} ≥ 2 V
Pull-Down Current (Severe OC)	750	1500	2000	mA	V_{GATE} ≥ 6 V
Pull-Down On-Time (Severe OC)	8		16	µs	
Gate Hold-Off Resistance		20		Ω	0 V ≤ VIN ≤ 9.2 V
SENSE+, SENSE−					
SENSE+, SENSE− Input Current, I_{SENSEx}			100	µA	V_{SENSE} ≤ 65 mV for ADM1075-1, per individual pin; V_{SENSE} ≤ 130 mV for ADM1075-2, per individual pin
SENSE+, SENSE− Input Imbalance, $I_{\Delta SENSEx}$			1	µA	$I_{\Delta SENSEx}$ = I_{SENSE+} − I_{SENSE-}
VCAP					
Internally Regulated Voltage, V_{VCAP}	2.66	2.7	2.74	V	0 ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET					
ISET Reference Select Threshold, $V_{ISETRSTH}$	1.35	1.5	1.65	V	If V_{ISET} > $V_{ISETRSTH}$ an internal 1 V reference (V_{CLREF}) is used
ISET Internal Reference, V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier, AV_{CSAMP}		50/25		V/V	Accuracies included in total sense voltage accuracies
ISET Input Current, I_{ISET}			100	nA	V_{ISET} ≤ VCAP
ADM1075-1 ONLY (GAIN = 50)					
Hot Swap Sense Voltage					
Hot Swap Sense Voltage Current Limit, $V_{SENSECL}$	19.4	20	20.6	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	24.5	25	25.5	mV	V_{ISET} = 1.25 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	19.5	20	20.5	mV	V_{ISET} = 1.0 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	14.5	15	15.5	mV	V_{ISET} = 0.75 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Constant Power Active	9.4	10	11.0	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.2 V
	4.5	5	5.7	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.4 V
	1.4	2	2.6	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 1.2 V
Circuit Breaker Offset, V_{CBOS}	0.6	0.75	0.95	mV	Circuit breaker voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
Severe Overcurrent					Activates high current gate pull-down
Voltage Threshold, $V_{SENSEOC}$	23	25	27	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	28	30	32	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; default at power-up
	38	40	42	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	43	45	47	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
Response Time					
Glitch Filter Duration	50		200	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	500		900	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; default at power-up
	6.2		10.7	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	44		57	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
Total Response Time	180		300	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	610		950	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; default at power-up
	7		13	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
	45		60	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 18 mV to 52 mV; optional select through PMBus
ADM1075-2 ONLY (GAIN = 25)					
Hot Swap Sense Voltage					
Hot Swap Sense Voltage Current Limit, $V_{SENSECL}$	39.2	40	40.8	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	49.2	50	50.8	mV	V_{ISET} = 1.25 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	39.2	40	40.8	mV	V_{ISET} = 1.0 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
	29.2	30	30.8	mV	V_{ISET} = 0.75 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0 V
Constant Power Active	19	20	21.9	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.2 V
	9.2	10	11.2	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 0.4 V
	3	4	5.0	mV	V_{ISET} > 1.65 V; V_{GATE} = 3 V; I_{GATE} = 0 µA; V_{SS} ≥ 2 V; V_{PLIM} = 1.2 V
Circuit Breaker Offset, V_{CBOS}	1.1	1.5	1.9	mV	Circuit breaker voltage, $V_{CB} = V_{SENSECL} - V_{CBOS}$
Severe Overcurrent					Activates high current gate pull-down
Voltage Threshold, $V_{SENSEOC1}$	46	50	54	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	56	60	64	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; default at power-up
	76	80	84	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
	86	90	94	mV	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; optional select through PMBus
Response Time					
Glitch Filter Duration	50		200	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	400		900	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; default at power-up
	6.2		10.7	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	44		57	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Total Response Time	180		300	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	610		950	ns	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; default at power-up
	7		13	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
	45		60	µs	V_{ISET} > 1.65 V; V_{SS} ≥ 2 V; V_{SENSE} step from 36 mV to 104 mV; optional select through PMBus
SOFT START					
SS Pull-Up Current, I_{SS}	−11.5	−10	−8.5	µA	V_{SS} = 0V
Default $V_{SENSECL}$ Limit	0.6	1.25	1.9	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping; V_{SS} = 0 V; ADM1075-1 only (gain = 50)
	1.2	2.5	3.8	mV	When V_{SENSE} reaches this level, I_{SS} is enabled, ramping; V_{SS} = 0 V; ADM1075-2 only (gain = 25)
SS Pull-Down Current		100		µA	V_{SS} = 1 V
TIMER					
Timer Pull-Up Current (POR), $I_{TIMERUPPOR}$	−4	−3	−2	µA	Initial power-on reset; V_{TIMER} = 0.5 V
Timer Pull-Up Current (OC Fault), $I_{TIMERUPFLT}$	−63	−60	−57	µA	Overcurrent fault; 0.05 V ≤ V_{TIMER} ≤ 1 V
Timer Pull-Down Current (Retry), $I_{TIMERDNRT}$	1.7	2	2.3	µA	After a fault when GATE is off; V_{TIMER} = 0.5 V
Timer Retry/OC Fault Current Ratio		3.33		%	Defines the limits of the autoretry duty cycle
Timer Pull-Down Current (Hold), $I_{TIMERDNHOLD}$		100		µA	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5 V
Timer High Threshold, V_{TIMERH}	0.98	1.0	1.02	V	
Timer Low Threshold, V_{TIMERL}	0.03	0.05	0.07	V	
PLIM					
PLIM Active Threshold	0.08	0.09	0.1	V	V_{ISET} > 1.65 V
Input Current, I_{PLIM}			100	nA	V_{PLIM} ≤ 1 V
Minimum Current Clamp, V_{ICLAMP}	75	100	125	mV	V_{PLIM} = 1.2 V; V_{SENSE_IMIN} = (V_{ICLAMP} ÷ gain) = minimum allowed current control
DRAIN					
DRAIN Voltage at Which $\overline{PWRGD}$ Asserts	1.9	2	2.1	V	I_{DRAIN} ≤ 50 µA
ADC_AUX/ADC_V					
Input Current			100	nA	0 V ≤ V_{ADC} ≤ 1.5 V
$\overline{SHDN}$ PIN					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Glitch Filter		1		µs	
Internal Pull-Up Current		8		µA	Pull-up to VIN
$\overline{RESTART}$ PIN					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Glitch Filter		1		µs	
Internal Pull-Up Current		8		µA	Pull-up to VIN
$\overline{SPLYGD}$ PIN					
Output Low Voltage, V_{OL_LATCH}			0.4	V	I_{SPLYGD} = 1 mA
			1.5	V	I_{SPLYGD} = 5 mA
Leakage Current			100	nA	V_{SPLYGD} ≤ 2 V; $\overline{SPLYGD}$ pin disabled
			1	µA	V_{SPLYGD} ≤ 14 V; $\overline{SPLYGD}$ pin disabled
$\overline{LATCH}$ PIN					
Output Low Voltage, V_{OL_LATCH}			0.4	V	I_{LATCH} = 1 mA
			1.5	V	I_{LATCH} = 5 mA
Leakage Current			100	nA	V_{LATCH} ≤ 2 V; $\overline{LATCH}$ pin disabled
			1	µA	V_{LATCH} ≤ 14 V; $\overline{LATCH}$ pin disabled
GPO1/$\overline{ALERT1}$/CONV PIN					
Output Low Voltage, V_{OL_GPO1}			0.4	V	I_{GPO} = 1 mA
			1.5	V	I_{GPO} = 5 mA

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
Leakage Current			100	nA	V_{GPO} ≤ 2 V; GPO disabled
			1	µA	V_{GPO} = 14 V; GPO disabled
Input High Voltage, V_{IH}	1.1			V	Configured as CONV pin
Input Low Voltage, V_{IL}			0.8	V	Configured as CONV pin
Glitch Filter		1		µs	Configured as CONV pin
GPO2/$\overline{\text{ALERT2}}$ PIN					
Output Low Voltage, V_{OL_GPO2}			0.4	V	I_{GPO} = 1 mA
			1.5	V	I_{GPO} = 5 mA
Leakage Current			100	nA	V_{GPO} ≤ 2 V; GPO disabled
			1	µA	V_{GPO} = 14 V; GPO disabled
$\overline{\text{PWRGD}}$ PIN					
Output Low Voltage, V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
			1.5	V	I_{PWRGD} = 5 mA
VIN That Guarantees Valid Output	1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current			100	nA	V_{PWRGD} ≤ 2 V; $\overline{\text{PWRGD}}$ active
			1	µA	V_{PWRGD} = 14 V; $\overline{\text{PWRGD}}$ active
CURRENT AND VOLTAGE MONITORING					
Current Sense Absolute Error (ADM1075-1)					25 mV input range; 128 sample averaging (unless otherwise noted)
		−0.01	±0.7	%	V_{SENSE} = 25 mV
		0.05	±0.85	%	V_{SENSE} = 20 mV
		0.07	±0.85	%	V_{SENSE} = 20 mV; 16 sample averaging
		0.04	±2.8	%	V_{SENSE} = 20 mV; 1 sample averaging
			±1.0	%	V_{SENSE} = 15 mV
			±1.4	%	V_{SENSE} = 10 mV
			±2.7	%	V_{SENSE} = 5 mV
			±5.9	%	V_{SENSE} = 2.5 mV
Current Sense Absolute Error (ADM1075-2)					50 mV input range; 128 sample averaging (unless otherwise noted)
		−0.03	±0.65	%	V_{SENSE} = 50 mV
		−0.03	±0.7	%	V_{SENSE} = 40 mV
		−0.03	±0.7	%	V_{SENSE} = 40 mV; 16 sample averaging
		−0.04	±1.35	%	V_{SENSE} = 40 mV; 1 sample averaging
			±0.75	%	V_{SENSE} = 30 mV
			±0.9	%	V_{SENSE} = 20 mV
			±1.7	%	V_{SENSE} = 10 mV
			±3.0	%	V_{SENSE} = 5 mV
ADC_V/ADC_AUX Absolute Accuracy	−0.8		+0.8	%	0.6 V ≤ V_{ADC} ≤ 1.5 V
ADC Conversion Time					1 sample of voltage and current; from command received to valid data in register
		191	219	µs	VAUX disabled
		263	301	µs	VAUX enabled
					16 samples of voltage and current averaged; from command received to valid data in register
		2.830	3.243	ms	VAUX disabled
		3.987	4.568	ms	VAUX enabled
					128 samples of voltage and current averaged; from command received to valid data in register
		22.54	25.83	ms	VAUX disabled (default on power-up)
		31.79	36.43	ms	VAUX enabled
Power Multiplication Time		14		µs	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ADR PIN					See Table 6
Address Set to 00	0		0.8	V	Connect to VEE
Input Current for Address 00	−40	−22		µA	V_{ADR} = 0 V to 0.8 V
Address Set to 01	135	150	165	kΩ	Resistor to VEE
Address Set to 10	−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11	2.1			V	Connect to VCAP
Input Current for Address 11		3	10	µA	V_{ADR} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
SERIAL BUS DIGITAL INPUTS (SDAI/SDAO, SCL)					
Input High Voltage, V_{IH}	1.1			V	
Input Low Voltage, V_{IL}			0.8	V	
Output Low Voltage, V_{OL}			0.4	V	I_{OL} = 4 mA, SDAO only
Input Leakage, $I_{LEAK-PIN}$	−10		+10	µA	
	−5		+5	µA	Device is not powered
Nominal Bus Voltage, V_{DD}	2.7		5.5	V	3 V to 5 V ±10%
Capacitive Load per Bus Segment, C_{BUS}			400	pF	
Capacitance for SDAI, SDAO, or SCL Pin, C_{PIN}		5		pF	
Input Glitch Filter, t_{SP}	0		50	ns	

SERIAL BUS TIMING

Table 2.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
f_{SCLK}	Clock frequency			400	kHz	
t_{BUF}	Bus free time	1.3			µs	
$t_{HD;STA}$	Start hold time	0.6			µs	
$t_{SU;STA}$	Start setup time	0.6			µs	
$t_{SU;STO}$	Stop setup time	0.6			µs	
$t_{HD;DAT}$	SDA[1] hold time	300		900	ns	
$t_{SU;DAT}$	SDA[1] setup time	100			ns	
t_{LOW}	SCL low time	1.3			µs	
t_{HIGH}	SCL high time	0.6			µs	
t_R[2]	SCL, SDA[1] rise time	20		300	ns	
t_F	SCL, SDA[1] fall time	20		300	ns	
t_{OF}	SCL, SDA[1] output fall time	20 + 0.1 × C_{BUS}		250	ns	

[1] SDAI and SDAO tied together.
[2] t_R = ($V_{IL(MAX)}$ − 0.15) to (V_{IH3V3} + 0.15) and t_F = 0.9 V_{DD} to ($V_{IL(MAX)}$ − 0.15); where V_{IH3V3} = 2.1 V, and V_{DD} = 3.3 V.

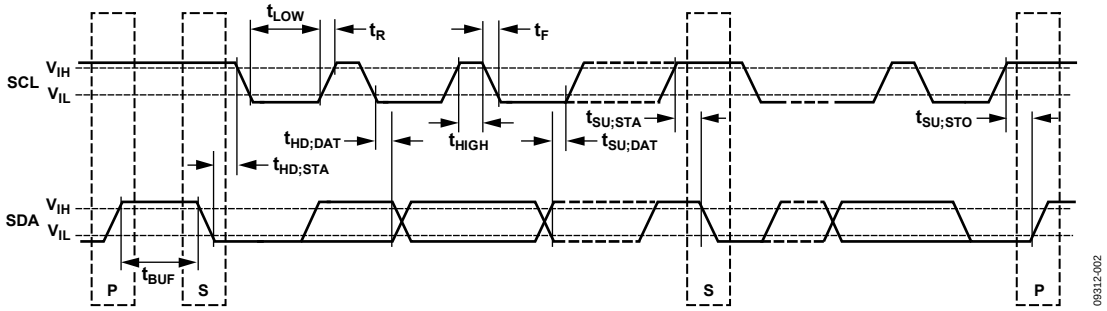


Figure 2. Serial Bus Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN Pin to VEE	−0.3 V to +14 V
UVL Pin to VEE	−0.3 V to +4 V
UVH Pin to VEE	−0.3 V to +4 V
OV Pin to VEE	−0.3 V to +4 V
ADC_V Pin to VEE	−0.3 V to +4 V
ADC_AUX Pin to VEE	−0.3 V to +4 V
SS Pin to VEE	−0.3 V to (VCAP + 0.3 V)
TIMER Pin to VEE	−0.3 V to (VCAP + 0.3 V)
VCAP Pin to VEE	−0.3 V to +4 V
ISET Pin to VEE	−0.3 V to +4 V
$\overline{\text{SPLYGD}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{LATCH}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{RESTART}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{SHDN}}$ Pin to VEE	−0.3 V to +18 V
$\overline{\text{PWRGD}}$ Pin to VEE	−0.3 V to +18 V
DRAIN Pin to VEE	−0.3 V to (VCAP + 0.3 V)
SCL Pin to VEE	−0.3 V to +6.5 V
SDAI Pin to VEE	−0.3 V to +6.5 V
SDAO Pin to VEE	−0.3 V to +6.5 V
ADR Pin to VEE	−0.3 V to (VCAP + 0.3 V)
GPO1/$\overline{\text{ALERT1}}$/CONV Pin to VEE	−0.3 V to +18 V
GPO2/$\overline{\text{ALERT2}}$ Pin to VEE	−0.3 V to +18 V
PLIM Pin to VEE	−0.3 V to +4 V
GATE Pin to VEE	−0.3 V to +18 V
SENSE+ Pin to VEE	−0.3 V to +4 V
SENSE− Pin to VEE	−0.3 V to +0.3 V
VEE to VEE_G	−0.3 V to +0.3 V
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Junction Temperature Range	−40°C to +105°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	150°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}	Unit
28-Lead TSSOP	68	20	°C/W
28-Lead LFCSP	35	4	°C/W

[1] Measured on JEDEC 4-layer board in still air.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTION

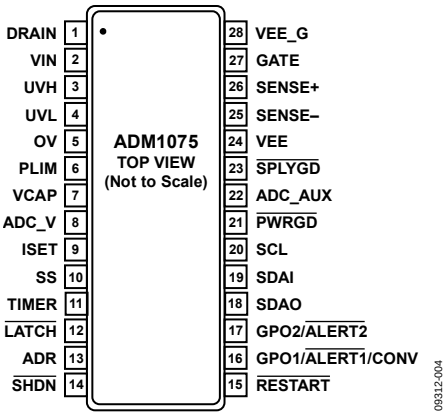


Figure 3. TSSOP Pin Configuration

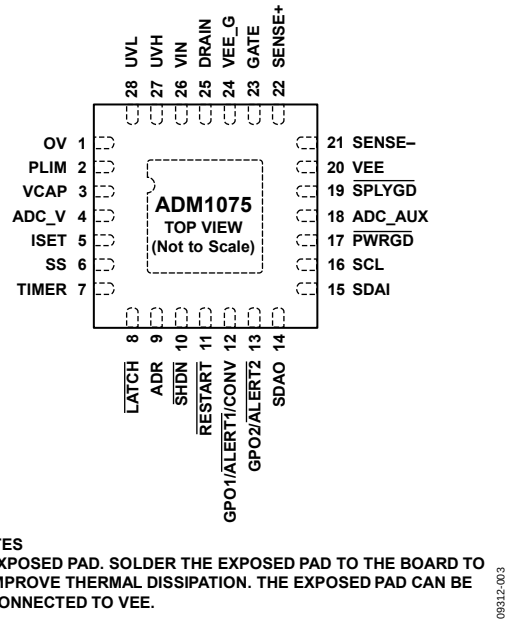


Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	25	DRAIN	Connect to the drain pin of the FET through a resistor. The current in this resistor is used to determine the V_{DS} of the MOSFET. This is used for $\overline{PWRGD}$.
2	26	VIN	Shunt Regulated Positive Supply to Chip. Connect to the positive supply rail via a shunt resistor. A 1 µF capacitor to VEE is recommended on the VIN pin.
3	27	UVH	Undervoltage Rising Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is under the UVH limit.
4	28	UVL	Undervoltage Falling Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is under the UVL limit.
5	1	OV	Overvoltage Input Pin. An external resistor divider is used from the supply to this pin to allow an internal comparator to detect if the supply is above the OV limit.
6	2	PLIM	The voltage on this pin is proportional to the V_{DS} voltage of the FET. As the PLIM voltage changes, the current limit automatically adjusts to maintain constant power across the FET.
7	3	VCAP	A capacitor with a value of 1 µF or greater should be placed on this pin to maintain good accuracy. This is an internal regulated supply. This pin can be used as a reference to program the ISET pin voltage.
8	4	ADC_V	This pin is used to read back the input voltage using the internal ADC. It can be connected to the OV string or a separate divider.
9	5	ISET	This pin allows the current limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. Alternatively, using a resistor divider from VCAP, the current limit can be adjusted to achieve a user defined sense voltage. An external reference can also be used.
10	6	SS	A capacitor is used on this pin to set the inrush current soft start ramp profile. The voltage on the soft start pin controls the current sense voltage limit, allowing control over the inrush current profile.
11	7	TIMER	Timer Pin. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin turns off when the voltage on the TIMER pin exceeds the upper threshold.
12	8	$\overline{LATCH}$	This pin signals the device latching off after an overcurrent fault. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
13	9	ADR	PMBus Address Pin. This pin can be tied low, tied to VCAP, left floating, or tied low through a resistor to set four different PMBus addresses.

Pin No.			
TSSOP	LFCSP	Mnemonic	Description
14	10	$\overline{\text{SHDN}}$	Drive this pin low to shut down the gate. Internal weak pull-up to VIN. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
15	11	$\overline{\text{RESTART}}$	Falling Edge Triggered 10 sec Automatic Restart. The gate remains off for 10 seconds, and then powers back up. Internal weak pull-up to VIN. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.
16	12	GPO1/$\overline{\text{ALERT1}}$ /CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions have been detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. This pin defaults to indicate FET health mode at power-up. There is no internal pull-up on this pin.
17	13	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions have been detected. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for further details. This pin defaults to indicate a seven-attempt fail at power-up. There is no internal pull-up on this pin.
18	14	SDAO	PMBus Serial Data Output. This is a split version of the SDA for easy use with optocouplers.
19	15	SDAI	PMBus Serial Data Input. This is a split version of the SDA for easy use with optocouplers.
20	16	SCL	PMBus Clock Pin. Open-drain input requires an external resistive pull-up.
21	17	$\overline{\text{PWRGD}}$	Power-Good Signal. This pin is used to indicate that the FET is no longer in the linear region and capacitors are fully charged. See the $\overline{\text{PWRGD}}$ section for details on assert and deassert.
22	18	ADC_AUX	This pin is used to read back a voltage using the internal ADC.
23	19	$\overline{\text{SPLYGD}}$	This pin asserts low when the supply is within the UV and OV limits set by the UVx and OV pins.
24	20	VEE	Chip Ground Pin. Must connect to –VIN rail (lowest potential).
25	21	SENSE–	Negative Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation controls the external FET gate to maintain the ($V_{SENSE+} - V_{SENSE-}$) sense voltage. This pin also connects to the VEE node, but should be routed separately.
26	22	SENSE+	Positive Current Sense Input Pin. A sense resistor between the SENSE+ pin and the SENSE– pin sets the analog current limit. The hot swap operation controls the external FET gate to maintain the ($V_{SENSE+} - V_{SENSE-}$) sense voltage. This pin also connects to the FET source node.
27	23	GATE	Gate Output Pin. This pin is the gate drive of an external N-channel FET. It is driven by the FET drive controller. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low while the supply is out of the voltage range.
28	24	VEE_G	Chip Ground Pin. Must connect to –VIN rail (lowest potential). The PCB layout should configure this pin as the gate pull-down return.
	EPAD	EPAD	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to VEE.

TYPICAL PERFORMANCE CHARACTERISTICS

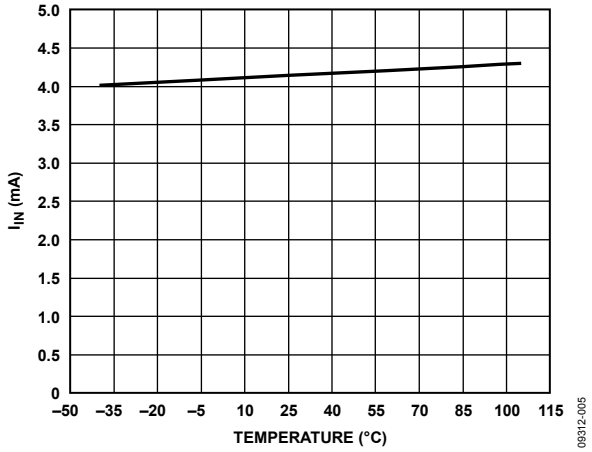


Figure 5. I_{IN} vs. Temperature

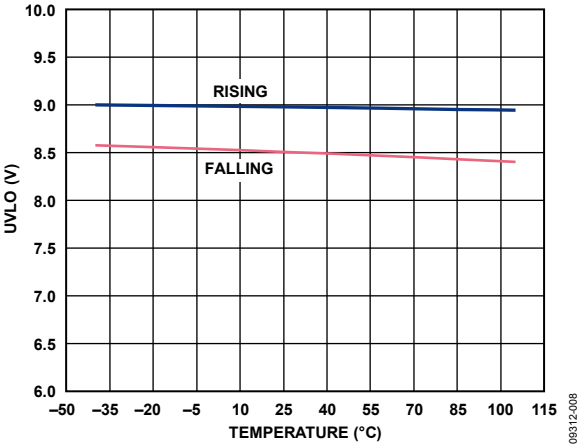


Figure 8. UVLO vs. Temperature

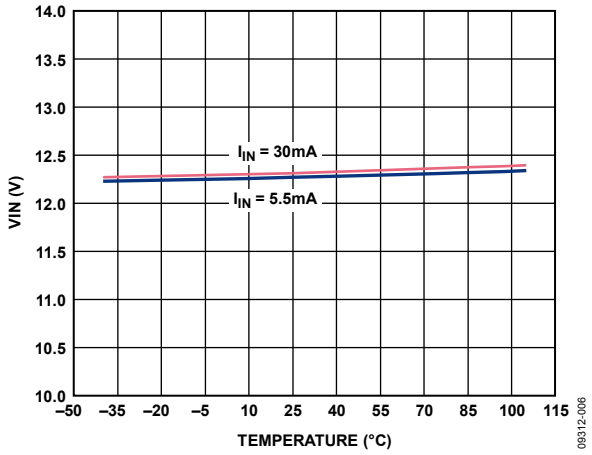


Figure 6. VIN vs. Temperature

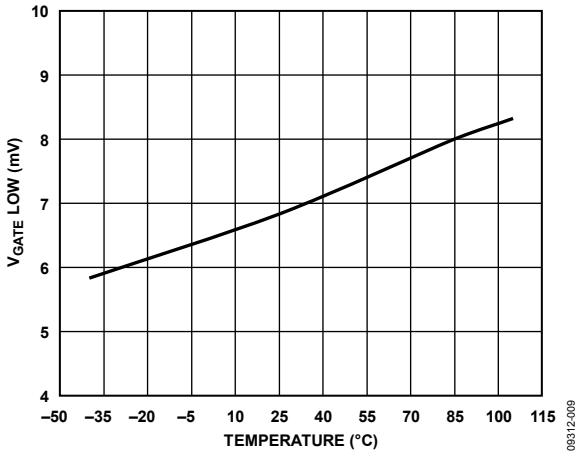


Figure 9. V_{GATE} Low vs. Temperature (I_{GATE} = 100 µA)

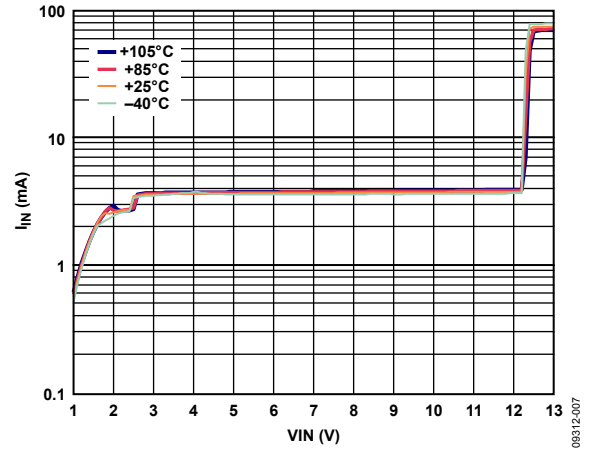


Figure 7. I_{IN} vs. VIN

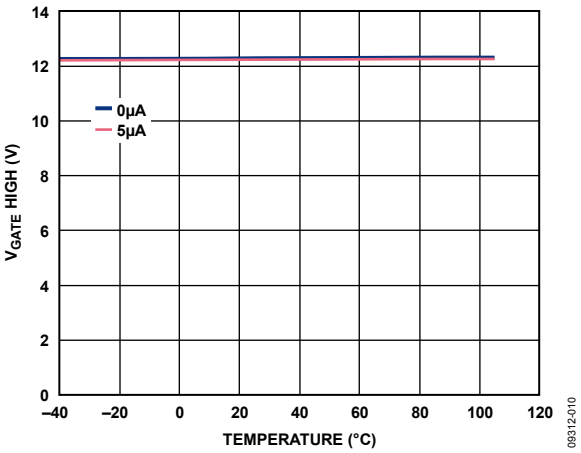


Figure 10. V_{GATE} High vs. Temperature

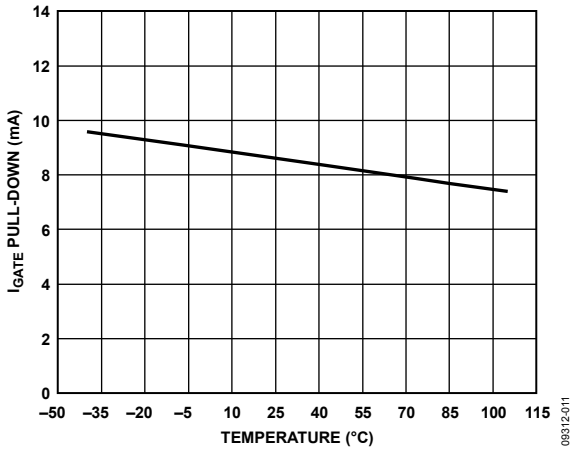


Figure 11. I_{GATE} Pull-Down vs. Temperature

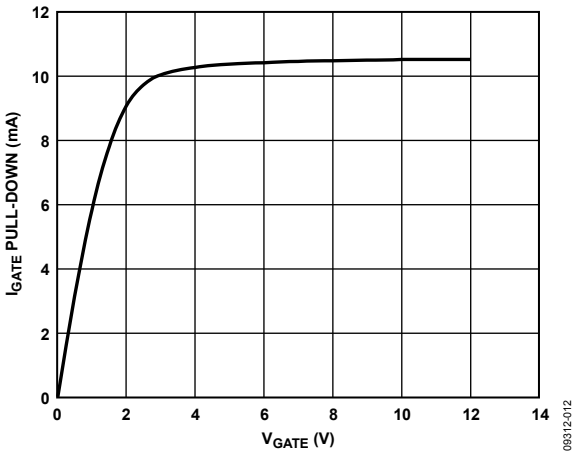


Figure 12. I_{GATE} Pull-Down vs. V_{GATE}

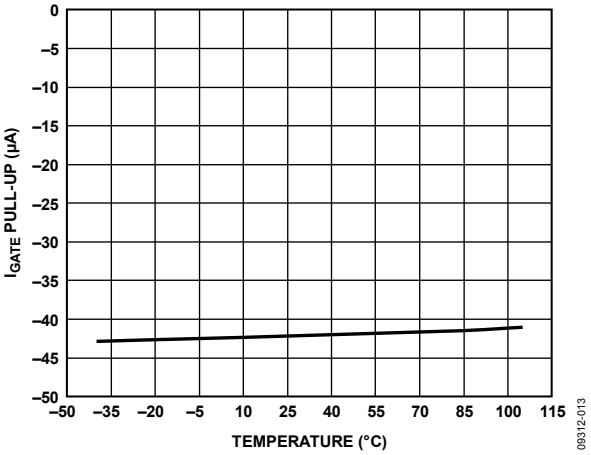


Figure 13. I_{GATE} Pull-Up vs. Temperature

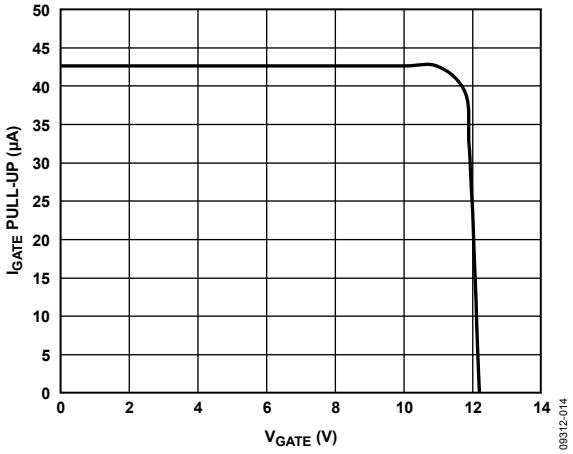


Figure 14. I_{GATE} Pull-Up vs. V_{GATE}

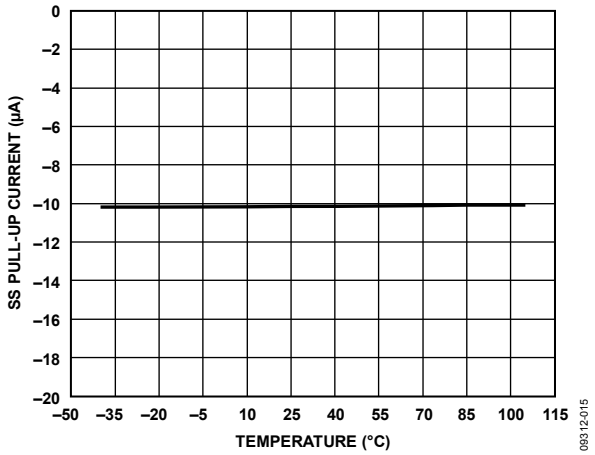


Figure 15. SS Pull-Up Current vs. Temperature

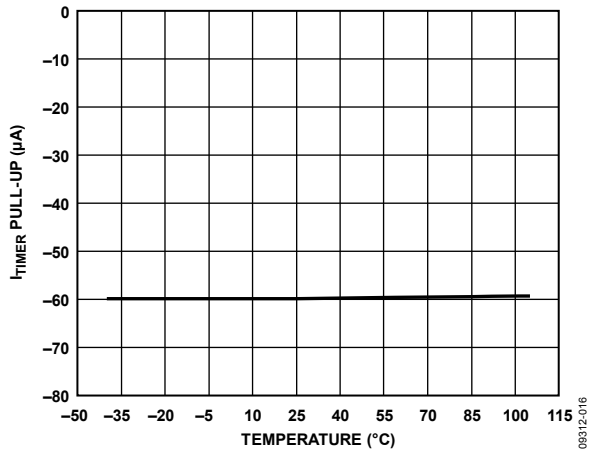


Figure 16. I_{TIMER} Pull-Up vs. Temperature

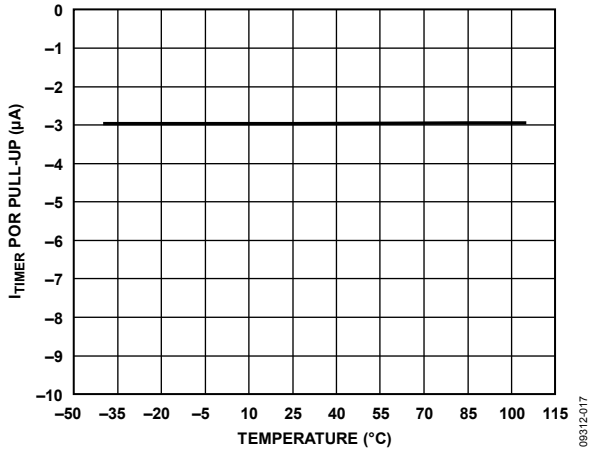


Figure 17. I_{TIMER} POR Pull-Up vs. Temperature

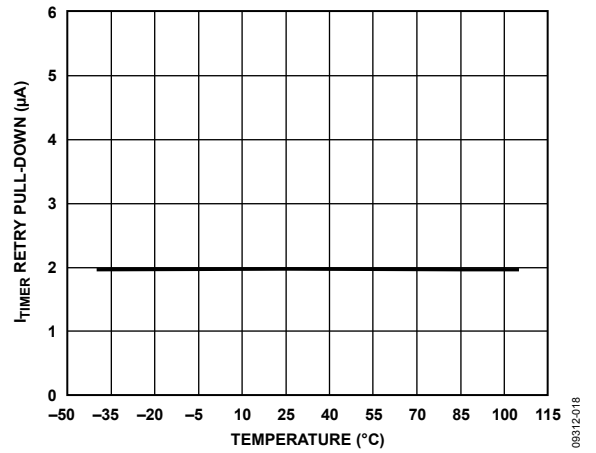


Figure 18. I_{TIMER} Retry Pull-Down vs. Temperature

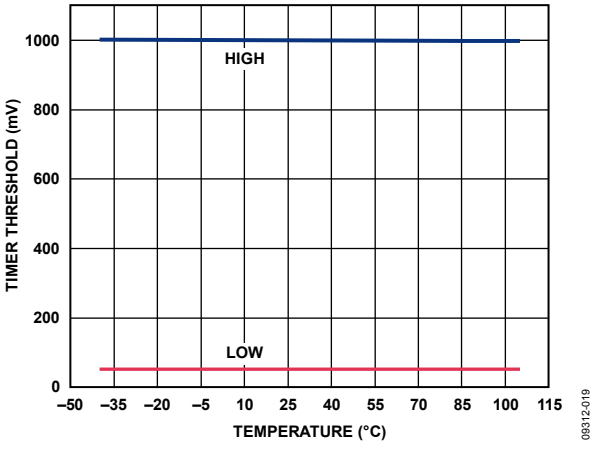


Figure 19. TIMER Threshold vs. Temperature

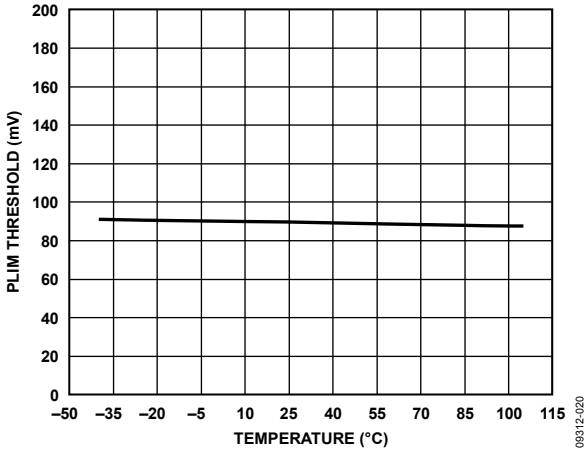


Figure 20. PLIM Threshold vs. Temperature

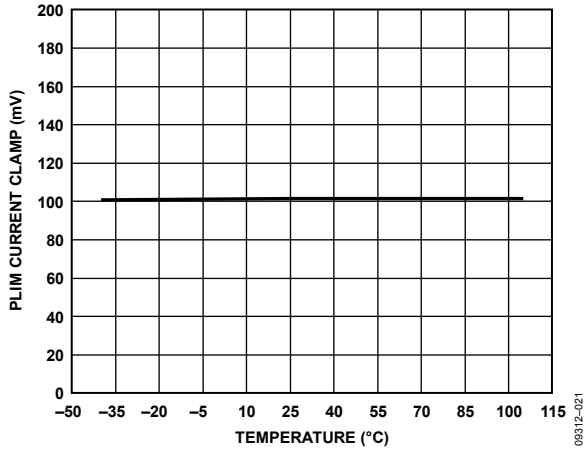


Figure 21. PLIM Current Clamp vs. Temperature

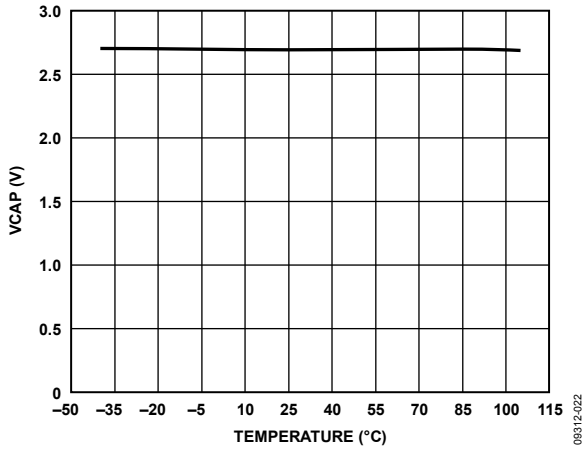


Figure 22. VCAP vs. Temperature (I_{VCAP} = 100 µA)

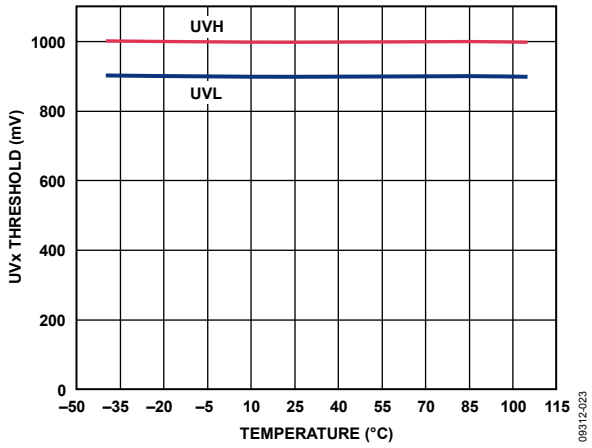


Figure 23. UVx Threshold vs. Temperature

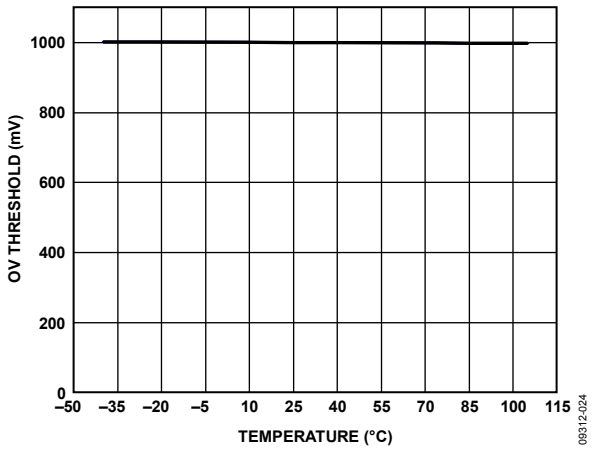


Figure 24. OV Threshold vs. Temperature

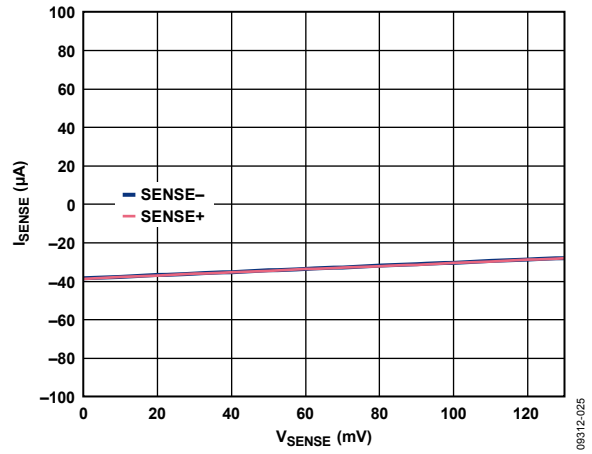


Figure 25. I_{SENSE} vs. V_{SENSE}

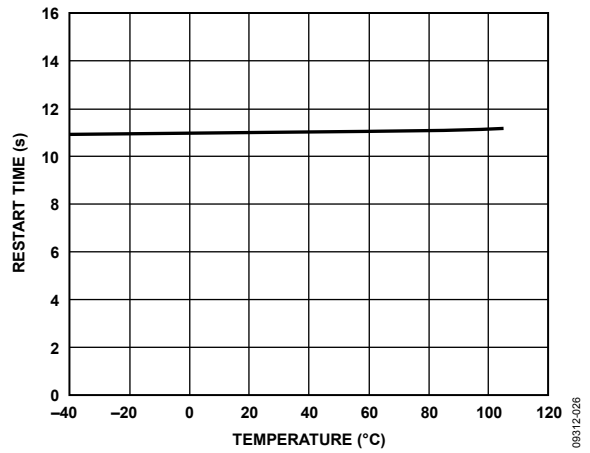


Figure 26. Restart Time vs. Temperature

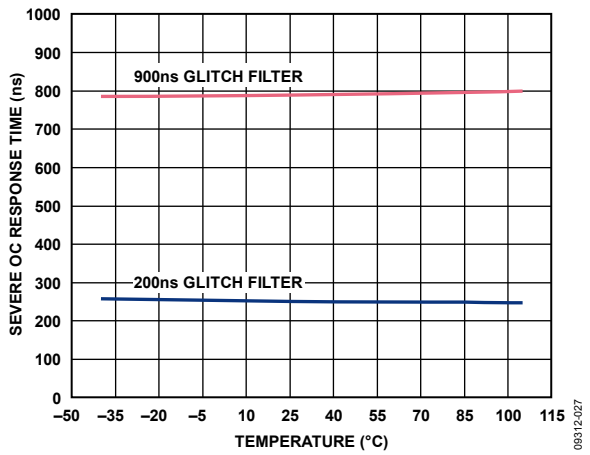


Figure 27. Severe OC Response vs. Temperature

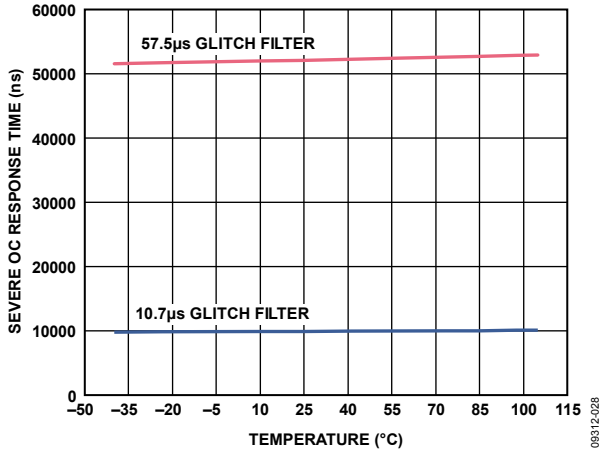


Figure 28. Severe OC Response vs. Temperature

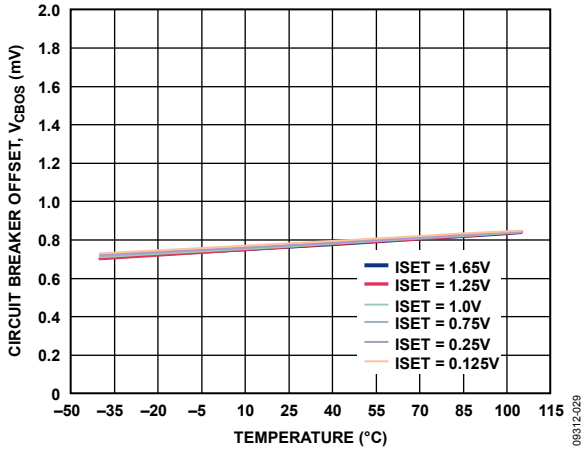


Figure 29. Circuit Breaker Offset vs. Temperature, ADM1075-1

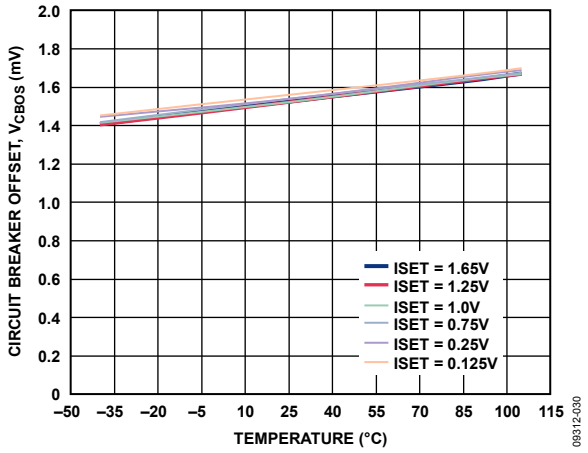


Figure 30. Circuit Breaker Offset vs. Temperature, ADM1075-2

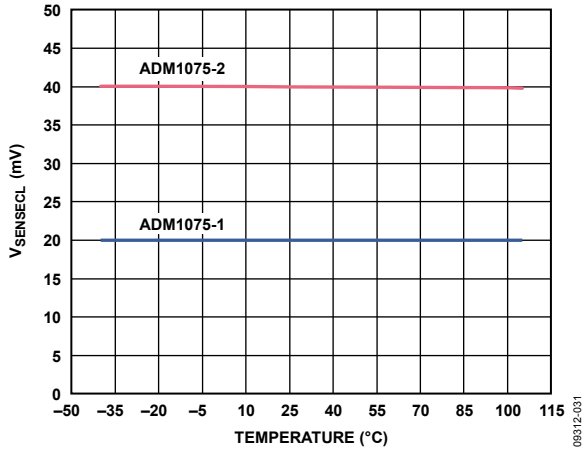


Figure 31. $V_{SENSECL}$ vs. Temperature, ISET = 1.65 V

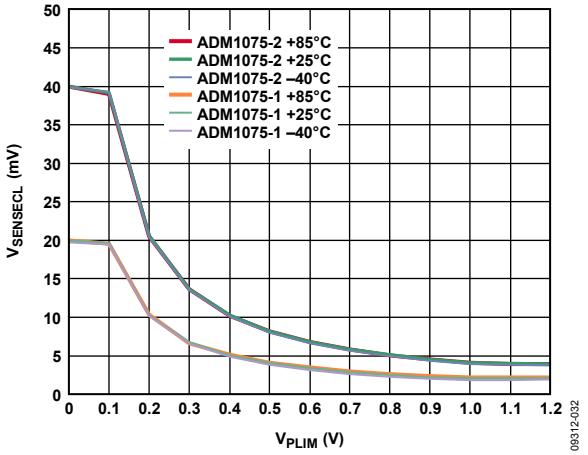


Figure 32. $V_{SENSECL}$ vs. PLIM

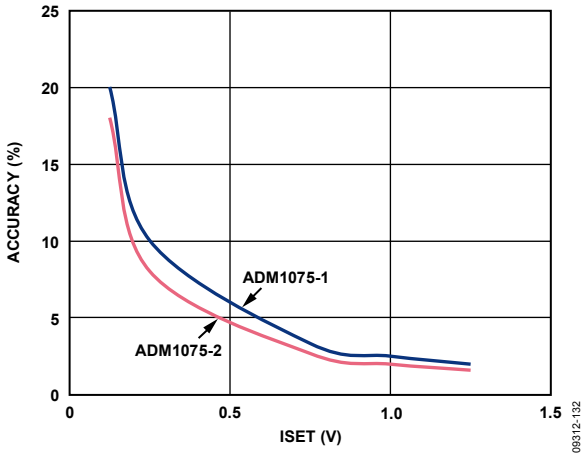


Figure 33. Worst-Case Hot Swap V_{SENSE} Accuracy vs. ISET

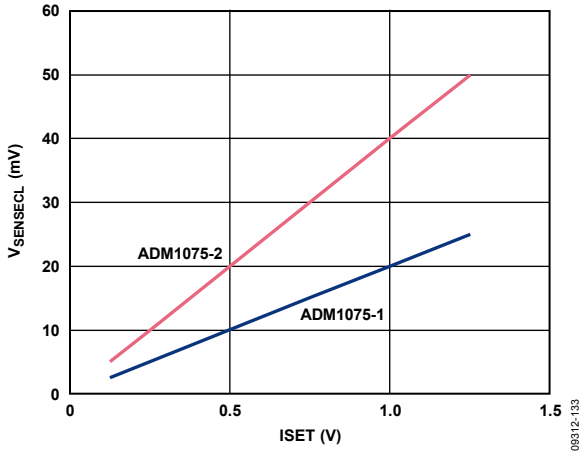


Figure 34. Typical Hot Swap $V_{SENSECL}$ vs. ISET

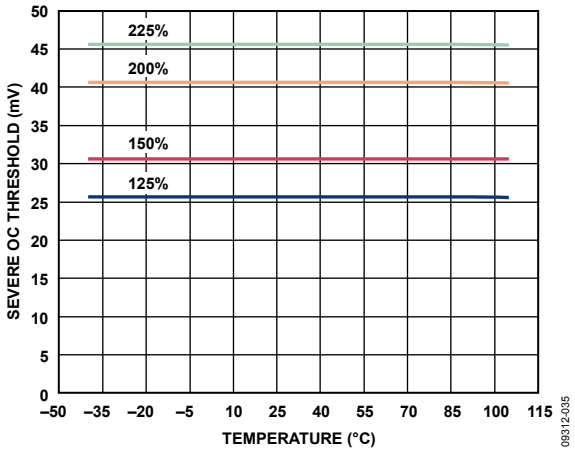


Figure 35. Severe OC Threshold vs. Temperature, ADM1075-1, ISET = 1.65 V

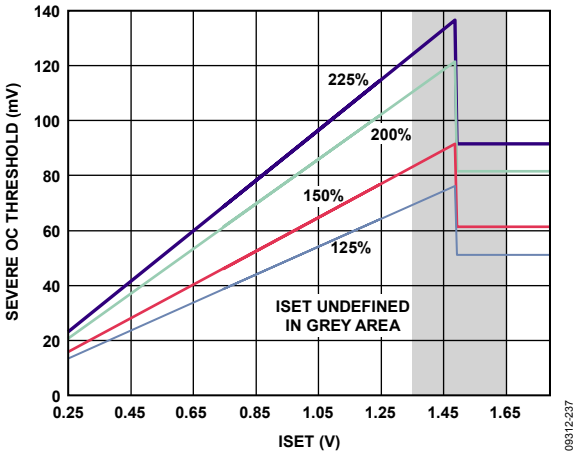


Figure 38. Severe OC Threshold vs. ISET, ADM1075-2

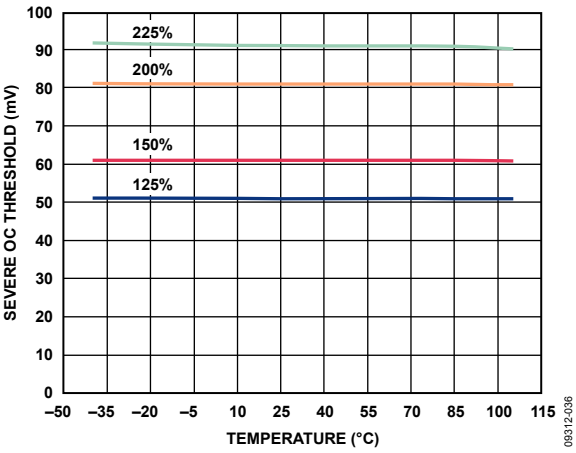


Figure 36. Severe OC Threshold vs. Temperature, ADM1075-2, ISET = 1.65 V

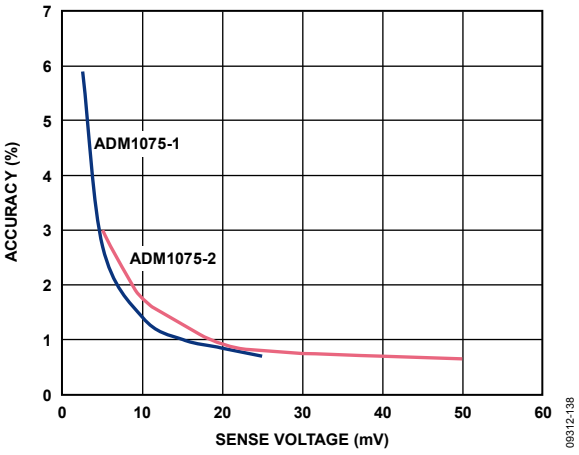


Figure 39. Worst-Case Current Sense Power Monitor Error vs. Current Sense Voltage (V_{SENSE})

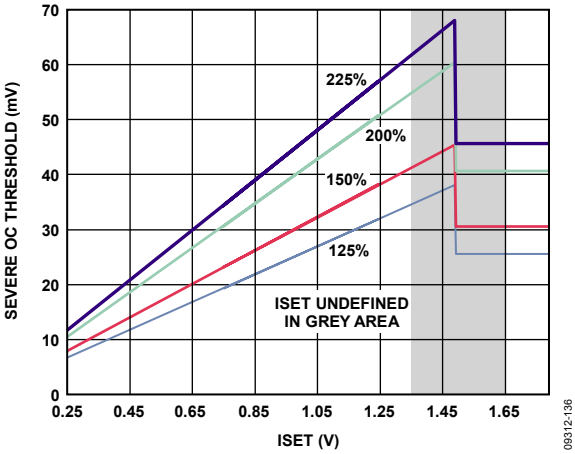


Figure 37. Severe OC Threshold vs. ISET, ADM1075-1

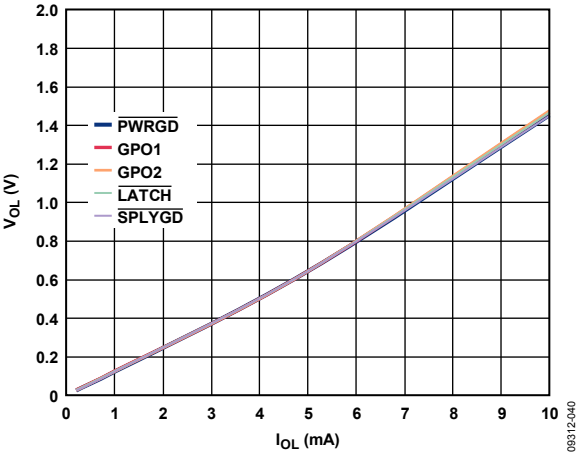


Figure 40. V_{OL} vs. I_{OL}

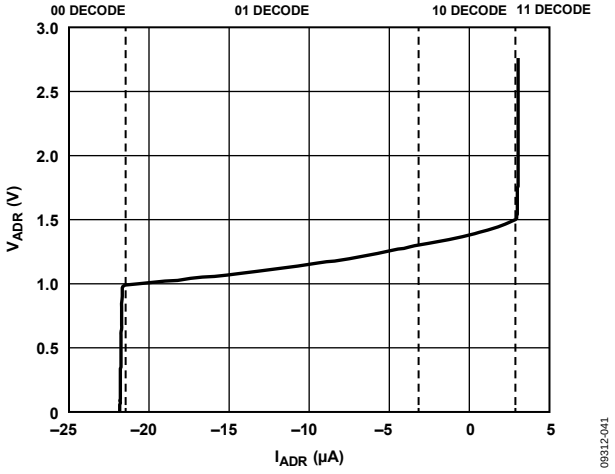


Figure 41. V_{ADR} vs. I_{ADR}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. Such transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1075 is intended to control the powering on and off of a board in a controlled manner, allowing the board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1075 can reside either on the backplane or on the removable board.

A minimal load current requirement is assumed when charging the load capacitance. If the load current is too large relative to the regulation current, it may not be possible to charge the load capacitance. The $\overline{\text{PWRGD}}$ pin can be used to disable the load until the load capacitance is fully charged.

POWERING THE ADM1075

The ADM1075 typically operates from a negative supply of −35 V to −80 V and can tolerate transient voltages of up to −200 V. The VIN pin is a positive supply pin with respect to chip ground. It is a current-driven supply and is shunt regulated to 12 V internally. It should be connected to the most positive supply terminal (usually −48 V RTN or 0 V) through a dropper resistor. The resistor should be chosen such that it always supplies enough current to overcome the maximum quiescent supply current of the chip while not exceeding the maximum allowable shunt current. After the system supply range has been established, an appropriate value for the dropper resistor can be calculated.

$$R_{SHUNT_MIN} = \frac{V_{IN_MAX} - V_{SHUNT_MIN}}{I_{SHUNT_MAX}}$$

$$R_{SHUNT_MAX} = \frac{V_{IN_MIN} - V_{SHUNT_MAX}}{I_{SHUNT_MIN}}$$

where:

V_{IN_MIN} and V_{IN_MAX} are the supply voltage extremes (that is, 35 V, 80 V).

V_{SHUNT_MIN} and V_{SHUNT_MAX} are the shunt regulator voltage data sheet specifications (see Table 1).

I_{SHUNT_MIN} is the maximum quiescent supply current (minimum shunt current).

I_{SHUNT_MAX} is the maximum shunt input current.

I_{SHUNT_MAX} can be calculated based on the maximum ambient temperature ($T_{A(MAX)}$) in the application, the maximum junction temperature ($T_{J(MAX)}$ = 105°C), and the θ_{JA} value of the package from Table 4. Worst-case internal power is at $VIN_{(MAX)}$ from Table 1.

$$I_{SHUNT_MAX} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA} \times VIN_{(MAX)}}$$

For example, the maximum shunt current with a TSSOP device at 80°C maximum ambient can be calculated as

$$I_{SHUNT_MAX} = \frac{105°C - 80°C}{68°C/W \times 13\ V} = 28\ mA$$

Tolerance of supplies and resistors should also be accounted for to ensure that the shunt current is always within the desired range.

Care must be taken to ensure that the power rating of the shunt resistor is sufficient. The power may be as high as 2 W at extreme supply conditions. Multiple shunt resistors can be used in series or in parallel to share power between resistors.

$$P_{R_SHUNT} = VI = (V_{IN_MAX} - V_{SHUNT_MIN}) \times I_{MAX}$$

where:

$$I_{MAX} = \frac{V_{IN_MAX} - V_{SHUNT_MIN}}{R_{SHUNT}}$$

The power dissipation in the shunt resistor can be saved if a suitable voltage rail is available to power the chip directly. This voltage rail must be well regulated to ensure that it is always greater than the UVLO threshold but less than the minimum shunt regulation voltage. The power directly without shunt specification in Table 1 shows the limits this voltage rail must meet. Note that this voltage is referenced to VEE.

The VIN pin provides the majority of the bias current for the device. The remainder of the current needed to control the gate drive and to best regulate the V_{GS} voltage is supplied by the SENSE± pins. The VEE and SENSE− pins are connected to the same voltage rail, although through separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 42).

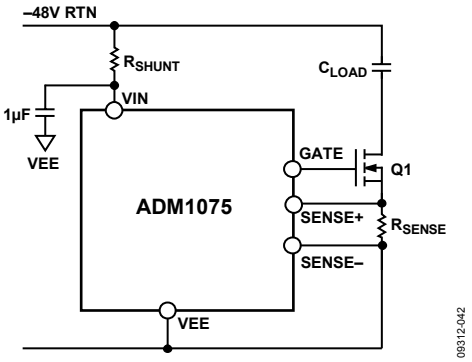


Figure 42. Powering the ADM1075

The available shunt current range should be wide enough to accommodate most telecommunication input voltage ranges. In an application where a wider input voltage range is possible, some external circuitry may be required to meet the shunt regulation current specifications. The applications diagram in Figure 43 shows an example of such a circuit, using a Zener diode and a bipolar junction transistor (BJT) device as an external pre-regulator on the −48 V supply. This ensures that the shunt regulation current is always within specification even at the extremes of supply voltage.

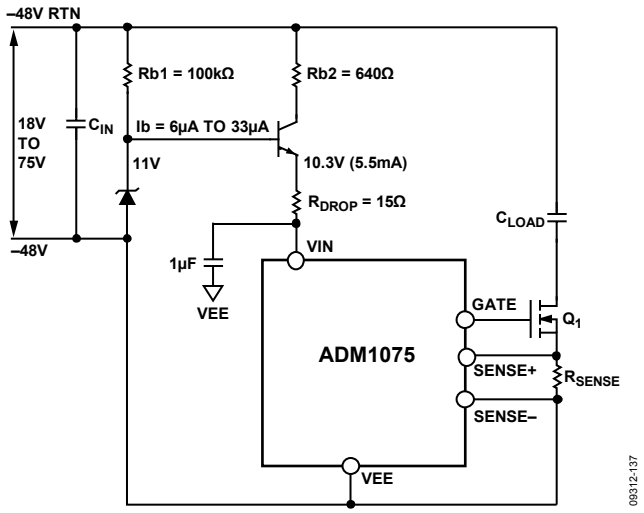


Figure 43. Wide Input Supply Range

CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE}. An internal current sense amplifier provides a gain of 25 or 50 (depending on the model) to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and detects when an overcurrent condition occurs.

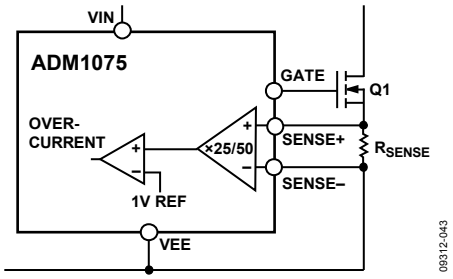


Figure 44. Hot-Swap Current Sense Amplifier

The SENSE± inputs can be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1075. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy. To achieve better accuracy, averaging resistors should be used to sum the sense nodes of each sense resistor, as shown in Figure 45. The typical value for the averaging resistors is 10 Ω. The value of the averaging resistors is chosen to be much greater than the trace resistance between the sense resistor terminals and the inputs to the ADM1075. This greatly reduces the effects of differences in the trace resistances.

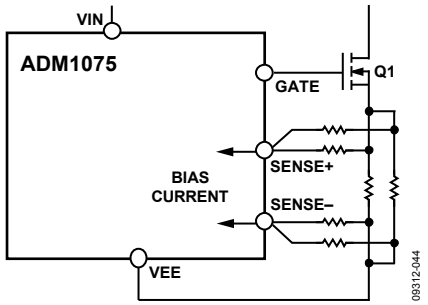


Figure 45. Connection of Multiple Sense Resistors to SENSE± Pins

CURRENT LIMIT REFERENCE

The current limit reference voltage determines the load current level to which the ADM1075 limits the current during an overcurrent event. This is the reference voltage to which the gained up current sense voltage is compared to determine if the limit is reached. This current limit voltage, shown in Figure 46, is then converted to a gate current to regulate the GATE pin.

$$I_{GATE} = V_{CURR_LIM} \times g_m$$

where g_m, the gate transconductance, = 660 µS.

An internal current limit reference selector block continuously compares the ISET, soft start, and foldback (derived from PLIM) voltages, determines which is the lowest at any given time, and uses it as the current limit reference. This ensures that the programmed current limit, ISET, is used in normal operation and the soft start and foldback features reduce the current limit when required.

The foldback and soft start voltages change during different stages of operation and are clamped to a lower level of 100 mV (typical) to prevent zero current flow due to the current limit being too low.

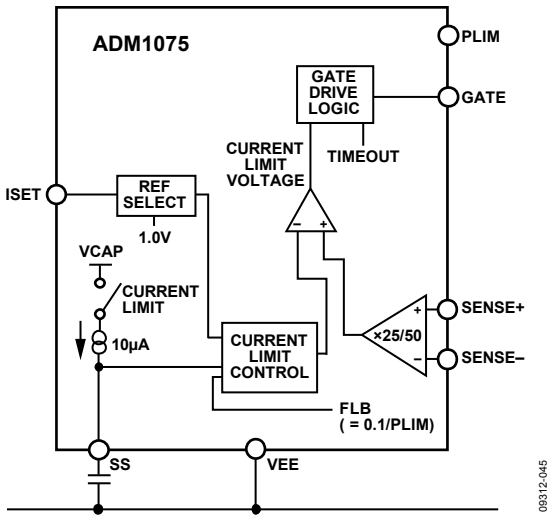


Figure 46. Current Limit Reference Selection

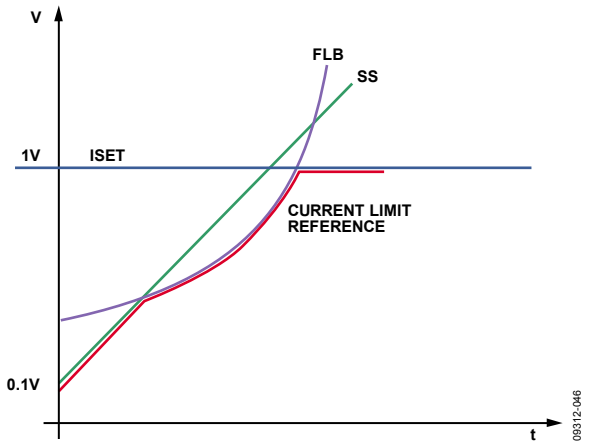


Figure 47. Interaction of Soft Start, Foldback, and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor value becomes smaller and resolution can be difficult to achieve when selecting the appropriate sense resistor value. The ADM1075 provides an adjustable sense voltage limit to deal with this issue. The device allows the user to program the required current sense voltage limit from 15 mV to 25 mV for the ADM1075-1 and from 30 mV to 50 mV for the ADM1075-2.

The default value of 20 mV/40 mV is achieved by connecting the ISET pin directly to the VCAP pin (VCAP > 1.65 V ISET reference select threshold). This configures the device to use an internal 1 V reference, which equates to 20 mV/40 mV at the sense inputs (see Figure 48(a)).

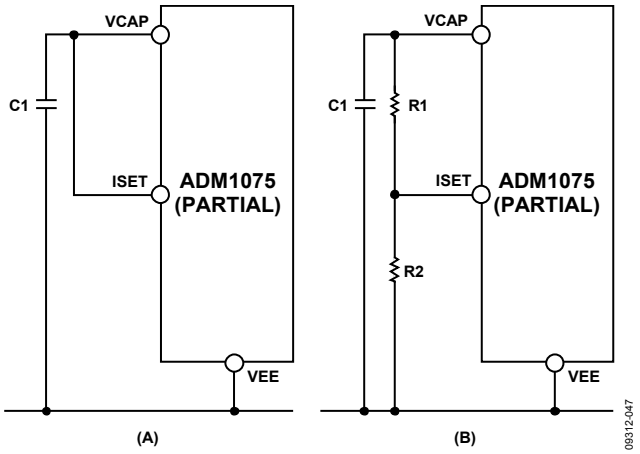


Figure 48. (a) Fixed 20 mV/40 mV Current Sense Limit
(b) Adjustable 15 mV to 50 mV Current Sense Limit

To set the sense voltage in the 15 mV to 50 mV range, a resistor divider is used to apply a reference voltage to the ISET pin (see Figure 48(b)). The VCAP pin has a 2.7 V internally generated voltage that can be used to set a voltage at the ISET pin.

Assuming V_{ISET} equals the voltage on the ISET pin, the resistor divider should be sized to set the ISET voltage as follows:

$V_{ISET} = (V_{SENSE} \times 50)$ for ADM1075-1 or

$V_{ISET} = (V_{SENSE} \times 25)$ for ADM1075-2

where V_{SENSE} is the sense voltage limit. The VCAP rail can also be used as the pull-up supply for setting the I²C address. The VCAP pin should not be used for any other purpose. To guarantee accuracy specifications, care must be taken to not load the VCAP pin by more than 100 µA.

SOFT START

A capacitor connected to the SS pin determines the inrush current profile. Before the FET is enabled, the output voltage of the current limit reference selector block is clamped at 100 mV. This, in turn, holds the current limit reference at approximately 2 mV for the ADM1075-1 or 4 mV for the ADM1075-2. When the FET is requested to turn on, the SS pin is held at ground until the voltage between the SENSE+ and SENSE− pins (V_{SENSE}) reaches the circuit breaker voltage, V_{CB}.

$$V_{CB} = V_{SENSECL} - V_{CBOS}$$

When the load current generates a sense voltage equal to V_{CB}, a 10 µA current source is enabled, which charges the SS capacitor and results in a linear ramping voltage on the SS pin. The current limit reference also ramps up accordingly, allowing the regulated load current to ramp up, while avoiding sudden transients during power-up. The SS capacitor value is given by

$$C_{SS} = \frac{I_{SS} \times t}{V_{ISET}}$$

where I_{SS} = 10 µA, and t is the SS ramp time.

For example, a 10 nF capacitor gives a soft start time of 1 ms.

Note that the SS voltage may intersect with the PLIM or foldback (FLB) voltage, and the current limit reference may change to follow PLIM (see Figure 47). This has minimal impact on startup because the output voltage rises at a similar rate to SS.

CONSTANT POWER FOLDBACK (PLIM)

Foldback is a method that actively reduces the current limit as the voltage drop across the FET increases. It keeps the power across the FET below the programmed value during power-up, overcurrent, or short-circuit events. This allows a smaller FET to be used, resulting in significant cost savings. The foldback method employed is a constant power foldback scheme, meaning power in the FET is held constant regardless of the V_{DS} of the FET. This simplifies the task of ensuring that the FET is always operating within the SOA region.

The ADM1075 detects the voltage drop across the FET by monitoring the voltage on the drain of the FET (via the PLIM pin). The device relies on the principle that the source of the FET is at the most negative expected supply voltage, and the magnitude of the drain voltage is relative to that of the V_{DS} of the FET. Using a resistor divider from the drain of the FET to

the PLIM pin, the relationship of V_{DS} to V_{PLIM} can be controlled. The foldback voltage, V_{FLB}, is the input to the current limit reference selector block and is defined as

$$V_{FLB} = 0.1/V_{PLIM}$$

The resistor divider should be designed to generate a V_{FLB} voltage equal to I_{SET} when the V_{DS} of the FET (and thus V_{PLIM}) rises above the desired power level. If I_{SET} = 1 V, V_{PLIM} needs to be 0.1 V at the point where constant power takes over (V_{FLB} = I_{SET}). For example, to generate a 200 W constant power limit at 10 A current limit, the maximum V_{DS} is required to be 20 V at the current limit. Therefore, the resistor divider must be 200:1 to generate a 0.1 V PLIM voltage at V_{DS} = 20 V. As V_{PLIM} continues to increase, the current limit reference follows V_{FLB} because it is now the lowest voltage input to the current limit reference selector block. This results in a reduction of the current limit, and, therefore, the regulated load current. To prevent complete current flow restriction, a clamp becomes active when the current limit reference reaches 100 mV. The current limit cannot drop below this level. This 200 W constant power example is illustrated in terms of FET SOA and real scope plots in Figure 49 and Figure 50.

When V_{FLB} has control of the current limit reference, the regulation current through the FET is

$$I_D = V_{FLB}/(Gain \times R_{SENSE})$$

where I_D is the external FET drain current, and *Gain* is the sense amplifier gain.

$$I_D = 0.1/(V_{PLIM} \times Gain \times R_{SENSE})$$

$$I_D = 0.1/(V_{DS} \times D \times Gain \times R_{SENSE})$$

where D is the resistor divider factor on PLIM.

Therefore, the FET power is calculated as

$$P_{FET} = I_D \times V_{DS} = 0.1/(D \times Gain \times R_{SENSE})$$

Because P_{FET} does not have any dependency on V_{DS}, it remains constant. Therefore, the FET power for a given system can be set by adjusting the divider (D) driving the PLIM pin.

The limits to the constant power system are when $V_{FLB} > I_{SET}$ (or 1 V if $V_{ISET} > V_{ISETRSTH}$) or when $V_{FLB} < 100$ mV (100 mV max clamp on V_{CLREF}). With an I_{SET} voltage of 1 V, this gives a 10:1 foldback current range.

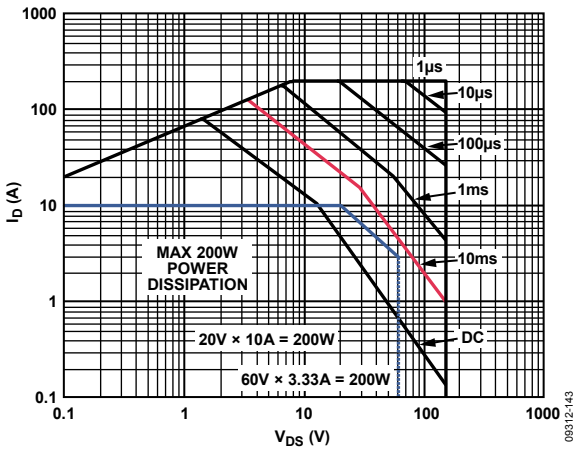


Figure 49. FET SOA

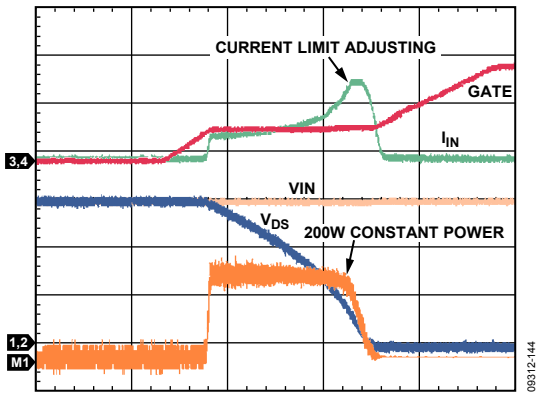


Figure 50. 200 W Constant Power Scope Plot, CH1 = VIN; CH2 = V_{DS}; CH3 = GATE; CH4 = System Current; M1 = FET Power

TIMER

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. There are two comparator thresholds: V_{TIMERH} (1.0 V) and V_{TIMERL} (0.05 V). The four timing current sources are a 3 µA pull-up, a 60 µA pull-up, a 2 µA pull-down, and a 100 µA pull-down.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time, the fault current limit time, and the hot swap retry duty cycle. The TIMER capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 60\ \mu A)/V_{TIMERH}$$

where t_{ON} is the time that the FET is allowed to spend in regulation. The choice of C_{TIMER} is based on matching this time with the SOA requirements of the FET. Foldback can be used here to simplify selection.

When V_{IN} is connected to the backplane supply, the internal supply of the ADM1075 must be charged up. A very short time later when the internal supply is fully up and above the undervoltage lockout voltage (UVLO), the device comes out of reset. During this first short reset period, the GATE and TIMER pins are both held low. The ADM1075 then goes through an initial

timing cycle. The TIMER pin is pulled up with 3 µA. When the TIMER reaches the V_{TIMERH} threshold (1.0 V), the first portion of the initial cycle is complete. The 100 µA current source then pulls down the TIMER pin until it reaches V_{TIMERL} (0.05 V). The initial cycle duration is related to C_{TIMER} by the following equation:

$$t_{INITIAL} = \frac{V_{TIMERH} \times C_{TIMER}}{3\,\mu A} + \frac{(V_{TIMERH} - V_{TIMERL}) \times C_{TIMER}}{100\,\mu A}$$

For example, a 470 nF capacitor results in a power-up delay of approximately 160 ms. Provided the UV and OV detectors are inactive when the initial timing cycle terminates, the device is ready to start a hot swap operation.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 60 µA timer pull-up current is activated, and the gate begins to regulate the current at the current limit. This initiates a ramp-up on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH} (1.0 V), the 60 µA pull-up is disabled, and the 2 µA pull-down is enabled.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which means that the timer actually starts a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 µA pull-up remains active and the FET remains in regulation. This allows the TIMER pin to reach V_{TIMERH} and initiate the GATE shutdown. The $\overline{\text{LATCH}}$ pin is pulled low immediately.

In latch-off mode, the TIMER pin is switched to the 2 µA pull-down when it reaches the V_{TIMERH} threshold. The $\overline{\text{LATCH}}$ pin remains low. While the TIMER pin is being pulled down, the hot swap controller is kept off and cannot be turned back on.

When the voltage on the TIMER pin goes below the V_{TIMERL} threshold, the hot swap controller can be reenabled by toggling the UVx pin or by using the PMBus OPERATION command to toggle the ON bit from on to off and then on again.

SETTING A LINEAR OUTPUT VOLTAGE RAMP AT POWER-UP

The ADM1075 standard method of operation is to control a constant power in the MOSFET during power-up into the load. This can result in non-linear output voltage ramps and often requires many retry attempts to charge larger load capacitances, due to MOSFET SOA limitations. However, there is a way to configure a single linear voltage ramp on the output which allows a constant inrush current to be maintained. For a typical power-up using constant power, as the output voltage increases in magnitude, the controlled current also increases to maintain a constant power in the pass MOSFET. This can be a challenge for maintaining MOSFET SOA, where higher drain currents limit energy transfer more than lower currents. However, if the output voltage is programmed to result in a linear ramp, the inrush into the load capacitance remains somewhat constant. This can have the advantage of setting very low inrush currents where required by combination of large output capacitance and FET SOA limitations.

The object of such a design is to allow a linear monotonic power-up event without the restrictions of the system fault timer. To achieve this, a power-up ramp is set so that the inrush is low enough not to reach the circuit breaker current limit, or constant power current limit. This allows power-up to continue without the timer running. When using this method, take separate care to ensure the power in the MOSFET during this event meets the SOA requirements. The components labeled R_{GD}, C_{GD} and C_G on the gate pin in Figure 51 show the required extra components.

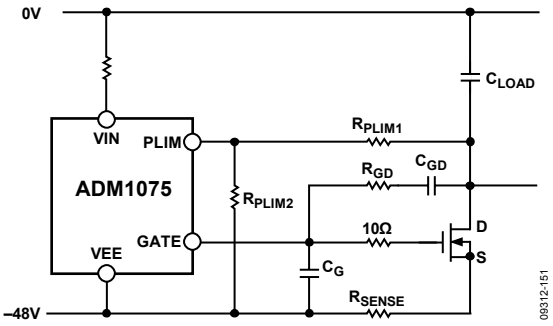


Figure 51. Required Extra Components

To ensure the inrush current does not approach or exceed the active current limit level, the output voltage ramp can be set by selecting the appropriate value for C_{GD} as follows:

$$C_{GD} = (I_{GATEUP}/I_{INRUSH}) \times C_{LOAD}$$

where I_{GATEUP} is the gate pull-up current specified.

Add margin and tolerance as necessary to ensure a robust design. Subtract any parasitic C_{GD} of the MOSFETS from the total to determine the additional external capacitance required.

The power-up ramp time can now be approximated by:

$$t_{RAMP} = (V_{IN} \times C_{LOAD})/I_{INRUSH}$$

Check the SOA of the MOSFET for conditions and the duration of this power-up ramp.

R_{GD} and C_G are used to limit the impact of sudden transients on the MOSFET Drain pin being coupled to the GATE pin through C_{GD}. R_G is chosen such that I_{GATEUP} has minimal voltage drop impact. Typical values would be 1 K. As a rule, C_G is recommended to be about 10× the value of C_{GD}, to a maximum of 470 nF. C_G must be minimized and must not exceed 470 nF to avoid slowing down gate shutdown in response to severe overcurrent events. This capacitance results in slowing down the gate ramp through V_{TH} and therefore the trans-conductance current ramp. This delay must also be considered when checking SOA during power-up into a fault. When using this method, always remove the SS cap, and TIMER can be minimized to provide a simple fault filtering solution.

HOT SWAP FAULT RETRY

The ADM1075 turns off the FET after an overcurrent fault. With the default pin configuration, the part latches off after an overcurrent fault and $\overline{\text{LATCH}}$ goes active low. This condition can then be reset by either a power cycling event or a low signal to either the $\overline{\text{SHDN}}$ input or $\overline{\text{RESTART}}$ input. It can also be reset by toggling the UVx pin, using the PMBus operation command or the PMBus power cycle command.

If the $\overline{\text{LATCH}}$ pin is connected to the $\overline{\text{SHDN}}$ pin, the part makes seven attempts to hot swap before latching off. In this mode, the part uses the TIMER pin to time a delay between each attempt. In this way, a large load capacitance can be charged using consecutive current limit periods.

The part can also be configured to autoretry an infinite number of times with a 10 second cooling period between each retry. Connecting $\overline{\text{LATCH}}$ to $\overline{\text{RESTART}}$ means that the part makes one hot swap attempt between each cooling period. Connecting $\overline{\text{LATCH}}$ to $\overline{\text{SHDN}}$ and GPO2/ALERT2 to $\overline{\text{RESTART}}$ means that the part makes seven hot swap attempts between each cooling period.

The duty cycle of the automatic retry cycle is set by the ratio of 2 µA/60 µA, which approximates to being on ~4% of the time. The value of the timer capacitor determines the on time of this cycle, which is calculated as follows:

$$t_{ON} = V_{TIMERH} \times (C_{TIMER}/60\ \mu A)$$

$$t_{OFF} = (V_{TIMERH} - V_{TIMERL}) \times (C_{TIMER}/2\ \mu A)$$

A 470 nF capacitor on the TIMER pin gives ~8 ms of on time (for example, to meet 10 ms SOA), and ~220 ms off time.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1075 features a very fast detection circuit that quickly responds to severe overcurrent events such as short circuits. Such an event may cause catastrophic damage if not controlled very quickly. A fast response circuit ensures that the ADM1075 detects an overcurrent event at approximately 150% of the normal current limit (ISET) and responds and controls the current within 1 µs in most cases. The severe overcurrent threshold and glitch filter times are digitally programmable through the PMBus. The threshold can be selected as 125%, 150%, 200%, or 225% of the normal current limit, and the glitch filter time can be set to 200 ns, 900 ns, 10.7 µs, or 57 µs. This sets a maximum response time of 300 ns, 950 ns, 13 µs, or 60 µs.

UV AND OV

The ADM1075 monitors the supply voltage for undervoltage (UV) and overvoltage (OV) conditions. The OV pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 1 V voltage reference. The user can program the value of the OV hysteresis by varying the top resistor of the resistor divider on the pin. This impedance in combination with the 5 µA OV hysteresis current (current turned on after OV trips) sets the OV hysteresis voltage.

$$OV_{RISING} = OV_{THRESHOLD} \times \frac{R_{TOP} + R_{BOTTOM}}{R_{BOTTOM}}$$

$$OV_{FALLING} \approx OV_{RISING} - (R_{TOP} \times 5\ \mu A)$$

The UV detector is split into two separate pins, UVH and UVL. The voltage on the UVH pin is compared internally to a 1 V reference, whereas the UVL pin is compared to a 0.9 V reference. Therefore, if the pins are tied together, the UV hysteresis is 100 mV. The hysteresis can be adjusted by placing a resistor between UVL and UVH.

Figure 52 illustrates the positive voltage monitoring input connection. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UVL pin falls below 0.9 V, and the gate is shut down using the 10 mA pull-down device. The fault is cleared after UVH pin rises above 1.0 V.

Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the gate is shut down using the 10 mA pull-down device.

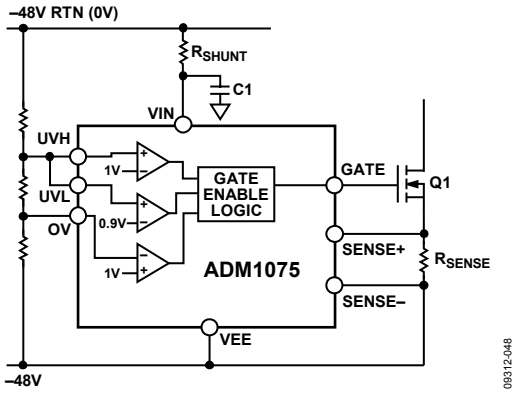


Figure 52. Undervoltage and Overvoltage Supply Monitoring

The maximum rating on the UVH pin is 4 V and the UVH threshold is 1 V. This limits the maximum input voltage to minimum input voltage ratio to 4:1. For example, if the UVH threshold is set at 20 V, the maximum input voltage is 80 V so as not to exceed the maximum ratings of the pin. If a wider input range is required, some protection circuitry is required on the UV pins to limit them to less than 4 V.

$\overline{\text{PWRGD}}$

The $\overline{\text{PWRGD}}$ output indicates the status of the output voltage. As shown in Figure 53, the $\overline{\text{PWRGD}}$ output is derived from the DRAIN pin voltage. It is an open-drain output that pulls low when the voltage on DRAIN is less than 2 V and the GATE pin voltage is near its 12 V rail (power good). When a fault occurs or hot swap is turned off, the open-drain pull-down is disabled, allowing $\overline{\text{PWRGD}}$ to go high (power bad). $\overline{\text{PWRGD}}$ is guaranteed to be in a valid state for $V_{IN} \geq 1$ V.

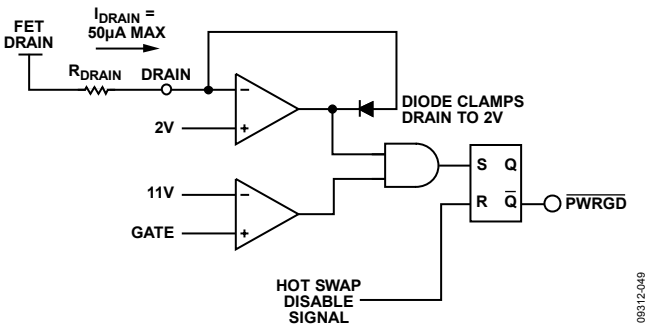


Figure 53. Generation of PWRGD Signal

DRAIN

Because the source of the FET is always at or near the most negative system supply, the drain voltage is a close approximation to the V_{DS} of the FET. When the voltage at the DRAIN pin is less than 2 V, it is assumed the FET is turned on. The DRAIN pin is used by the power-good circuitry to determine when PWRGD can be asserted. A resistor is required on the DRAIN pin to limit current on the pin to 50 µA. A 2 MΩ resistor is suitable to limit the current in most cases.

SPLYGD

The SPLYGD output indicates when the input supply is within the programmed voltage window. This is an open-drain output. An external pull-up resistor is required on this pin.

LATCH

The LATCH output signals that the device has latched off after an overcurrent fault. This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.

SHDN

The SHDN pin is a level-triggered input that allows the user to command a shutdown of the hot swap function. When this input is set low, the GATE output is switched to VEE to turn the FET off. This pin has an internal pull-up of approximately 8 µA, allowing it to be driven by an open-drain pull-down output or a push-pull output. The input threshold is ~1 V.

This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.

Take care if using the SHDN pin as an on/off pin. Pulling the SHDN low always turns off the gate. However, taking SHDN high again turns on hot swap only if there have been less than seven faults/shutdown events within a 10 second period. The retry scheme is configured to set GPO2/ALERT2 low after seven faults. The SHDN pin cannot clear the GPO2/ALERT2 fault. The retry counter is cleared after 10 seconds of power good. Therefore, this is not an issue if there is never going to be more than seven SHDN events within a 10 second period.

The UVH or UVL pin may work better as a system on/off pin if required. Toggling the UVx pin clears any faults (including GPO2/ALERT2 low after seven retry attempts). A switch shorting UVH or UVL to VEE works as an on/off switch.

RESTART

The RESTART pin is a falling edge triggered input that allows the user to command a 10 second automatic restart. When this input is set low, the gate turns off for 10 seconds, and then powers back up. The pin is falling edge triggered; therefore, holding RESTART low for more than 10 seconds generates only one restart. This pin has an internal pull-up of approximately 8 µA, allowing it to be driven by an open-drain pull-down output or a push-pull output. The input threshold is ~1 V.

This pin is also used to configure the desired retry scheme. See the Hot Swap Fault Retry section for additional details.

FET HEALTH

The ADM1075 features a method of detecting a shorted pass FET. The FET health status can be used to generate an alert on the GPO1/ALERT1/CONV and GPO2/ALERT2 pins. By default, at power-up, an alert is generated on GPO1/ALERT1/CONV if the FET health status indicates a bad FET is present. FET health is considered bad if all of the following conditions are true:

- The ADM1075 is holding the FET off, for example, during the initial power-on cycle time.
- V_{SENSE} > 2 mV for the ADM1075-1 and 4 mV for the ADM1075-2.
- V_{GATE} < ~1 V.

POWER MONITOR

The ADM1075 features an integrated ADC that accurately measures the current sense voltage and the ADC_V voltage. It can also optionally monitor the ADC_AUX voltage. The measured input voltage (ADC_V) and the current being delivered to the load are multiplied to give a power value that can be read back. Each power value is also added to an accumulator that can be read back to allow an external device to calculate the energy consumption of the load.

The PEAK_IOUT, PEAK_VIN, and PEAK_VAUX commands can be used to read the highest peak current or voltage since the value was last cleared.

An averaging function is provided for voltage and current that allows a number of samples to be averaged by the ADM1075. This function reduces the need for postprocessing of sampled data by the host processor. The number of samples that can be averaged is 2^N, where N is in the range of 0 to 7.

The power monitor current sense amplifier is bipolar and can measure both positive and negative currents. It has two input ranges and can be selected using the PMBus interface. The input ranges are ±25 mV and ±50 mV.

The two basic modes of operation for the power monitor are single shot and continuous. In single-shot mode, the power monitor samples the input voltage and current a number of times, depending on the averaging value selected by the user.

The ADM1075 returns a single value corresponding to the average voltage and current measured. When configured for continuous mode, the power monitor continuously samples voltage and current, making the most recent sample available to be read. The ADC runs in continuous mode by default at power-up.

The single-shot mode can be triggered in a number of ways. The simplest is by selecting the single-shot mode using the PMON_CONFIG command and writing to the CONVERT bit using the PMON_CONTROL command. The CONVERT bit can also be written as part of a PMBus group command. Using a group command allows multiple devices to be written to as part of the same I²C bus transaction, with all devices executing the command when the stop condition appears on the bus. In this way, several devices can be triggered to sample at the same time.

When the GPO1/$\overline{\text{ALERT1}}$/CONV pin is set to the convert (CONV) mode, an external hardware signal can be used to trigger the single-shot sampling of one or more parts at the same time.

Each time a current sense and input voltage measurement is taken, a power calculation is performed, multiplying the two measurements together. This can be read from the device using the READ_PIN command, returning the input power.

At the same time, the calculated power value is added to a power accumulator register that may increment a rollover counter if the value exceeds the maximum accumulator value, and that also increments a power sample counter.

The power accumulator and power sample counter are read back using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time. The bus host reading the data assigns a timestamp to show when the data is read. By calculating the time difference between consecutive uses of READ_EIN and determining the delta in power consumed, it is possible for the host to determine the total energy consumed over that period.

ISOLATION

Isolation is usually required in −48 V systems because there can be a large voltage difference between different ground planes in the system. The ADM1075 is referenced to −48 V, whereas the MCU is usually referenced to 0 V. In almost all cases, the I²C signals must be isolated. Any other ADM1075 digital input and output signals that go to or come from the MCU must also be isolated.

Analog Devices, Inc., provide a range of digital isolators using *i*Coupler® technology. *i*Coupler technology is based on chip scale transformers rather than the LEDs and photodiodes used in optocouplers. The ADuM1250 is a dual I²C isolator and can be used in conjunction with the ADM1075 for I²C isolation.

In cases where more digital signals need to be isolated, the ADuM3200 is a dual-channel digital isolator whereas the ADuM5404 is a quad-channel isolator with *iso*Power®, an integrated, isolated dc-to-dc converter.

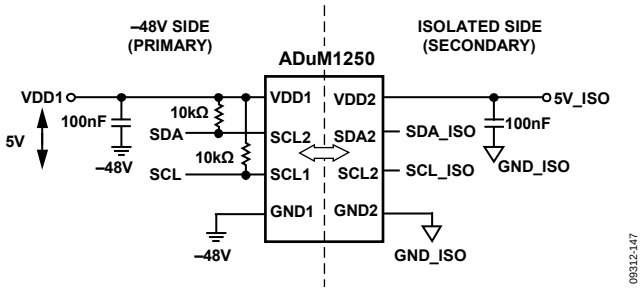


Figure 54. ADuM1250 I²C Isolation

The ADuM1250 and ADuM3200 must be powered from both the primary and secondary sides. The ADuM5404 only needs to be powered from the secondary side and can provide power across the isolation barrier via the integrated dc-to-dc converter. Therefore, the ADuM5404 can be used to power the primary side of the ADuM1250 if both are used on the board. Some extra care is required if using the ADuM5404 to power the ADuM3200. If the power at the secondary side is enabled by the ADM1075, the *iso*Power solution may not work. Because *iso*Power is unpowered in this case, the ADuM3200 outputs are in an undefined state. If the $\overline{\text{SHDN}}$ input comes from the ADuM3200, it may be held low, and the ADM1075 never turns on the FET or enables power at the secondary side.

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special precautions must be taken during printed circuit board (PCB) layout to meet emissions standards. See the AN-0971 Application Note for board layout recommendations.

Powering the *i*Couplers from the secondary side is usually straightforward because there is often a suitable voltage rail available. However, there is not always a suitable voltage rail available on the primary side (−48 V side). If the ADuM5404 is not used on the system, the ADuM1250 can be powered on the primary side in a number of different ways.

If a voltage rail is available on the primary side (3.3 V or 5 V referenced to VEE), that can be used to power the chip directly. Otherwise, the ADM1075 shunt voltage and/or the −48 V supply can be regulated down to power the part. A simple emitter follower circuit achieves this, as shown in Figure 55.

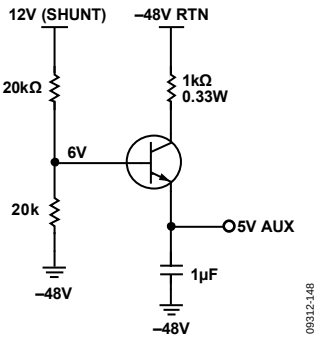


Figure 55. Powering iCoupler from −48 V Supply

PMBus INTERFACE

The I²C bus is a common, simple serial bus used by many devices to communicate. It defines the electrical specifications, the bus timing, the physical layer, and some basic protocol rules.

SMBus is based on I²C and aims to provide a more robust and fault-tolerant bus. Functions such as bus timeout and packet error checking are added to help achieve this robustness, along with more specific definitions of the bus messages used to read and write data to devices on the bus.

PMBus is layered on top of SMBus and, in turn, on I²C. Using the SMBus defined bus messages, PMBus defines a set of standard commands that can be used to control a device that is part of a power chain.

The ADM1075 command set is based upon the *PMBus™ Power System Management Protocol Specification*, Part I and Part II, Revision 1.2. This version of the standard is intended to provide a common set of commands for communicating with dc-to-dc type devices. However, many of the standard PMBus commands can be mapped directly to the functions of a hot swap controller.

Part I and Part II of the PMBus standard describe the basic commands and how they can be used in a typical PMBus setup. The following sections describe how the PMBus standard and the ADM1075 specific commands are used.

DEVICE ADDRESSING

The ADM1075 is available in two models: the ADM1075-1 and ADM1075-2. The PMBus address is seven bits in size. The upper five bits (MSBs) of the address word are fixed and are different for each model, as follows:

- ADM1075-1: Base address is 00100xx (0x10)
- ADM1075-2: Base address is 00110xx (0x18)

The ADM1075-1 and ADM1075-2 have a single ADR pin that is used to select one of four possible addresses for a given model. The ADR pin connection selects the lowest two bits (LSBs) of the 7-bit address word (see Table 6).

Table 6. PMBus Addresses and ADR Pin Connection

Value of Address LSBs	ADR Pin Connection
00	Connect to VEE
01	150 kΩ resistor to VEE
10	No connection (floating)
11	Connect to VCAP

SMBus PROTOCOL USAGE

All I²C transactions on the ADM1075 are performed using SMBus defined bus protocols. The following SMBus protocols are implemented by the ADM1075:

- Send byte
- Receive byte
- Write byte
- Read byte
- Write word
- Read word
- Block read

PACKET ERROR CHECKING

The ADM1075 PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the ADM1075 during a read transaction or sent by the bus host to the ADM1075 during a write transaction. The ADM1075 supports the use of PEC with all the SMBus protocols that it implements.

The use of the PEC byte is optional. The bus host can decide whether to use the PEC byte with the ADM1075 on a message-by-message basis. There is no need to enable or disable PEC in the ADM1075.

The PEC byte is used by the bus host or the ADM1075 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the ADM1075 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag.

Within a group command, the host can choose to send or not send a PEC byte as part of the message to the ADM1075.

PARTIAL TRANSACTIONS ON I²C BUS

In the event of a specific sequence of events occurring on the I²C bus, it is possible for the I²C interface on the device to go into a state where it fails to ACK the next I²C transaction directed to it. There are two ways that this behavior can be triggered:

- A partial I²C transaction consisting of a start condition, followed by a single SCL clock pulse and stop condition.
- If the I²C bus master does not follow the 300 ns SDA data hold time when signaling the ACK/NACK bit at the end of a transaction. The device sees this as a single SCL clock partial transaction.

In the event that the device NACKs a transaction, then the I²C interface on the device can be reset by sending a series of up to 16 SCL clock pulses, or performing a dummy transaction to another I²C address on the bus.

SMBus MESSAGE FORMATS

Figure 56 to Figure 64 show all the SMBus protocols supported by the ADM1075, along with the PEC variant. In these figures, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the ADM1075 is driving the bus.

Figure 56 to Figure 64 use the following abbreviations:
S = start condition
Sr = repeated start condition
P = stop condition
R = read bit
$\overline{W}$ = write bit
A = acknowledge bit (0)
$\overline{A}$ = acknowledge bit (1)

A represents the ACK (acknowledge) bit. The ACK bit is typically active low (Logic 0) if the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.

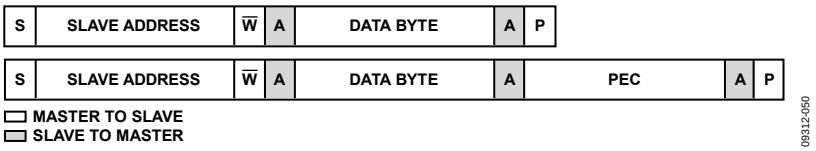


Figure 56. Send Byte and Send Byte with PEC

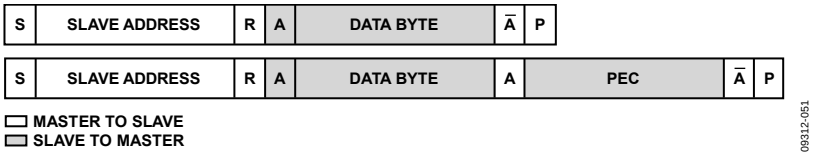


Figure 57. Receive Byte and Receive Byte with PEC

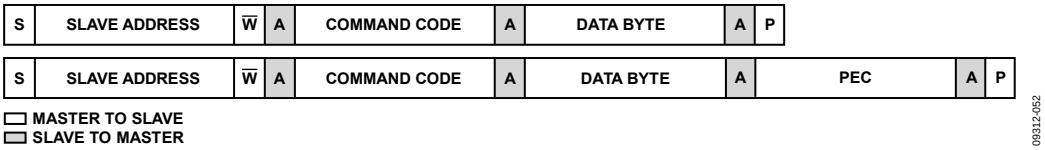


Figure 58. Write Byte and Write Byte with PEC

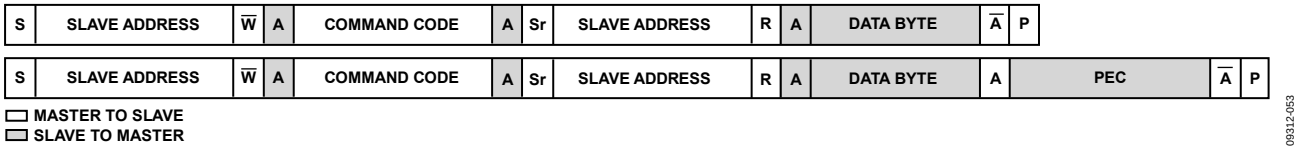


Figure 59. Read Byte and Read Byte with PEC

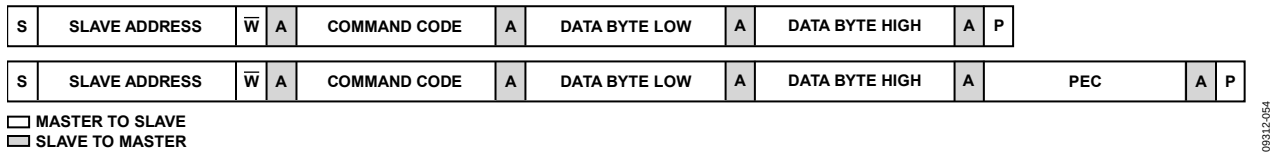


Figure 60. Write Word and Write Word with PEC

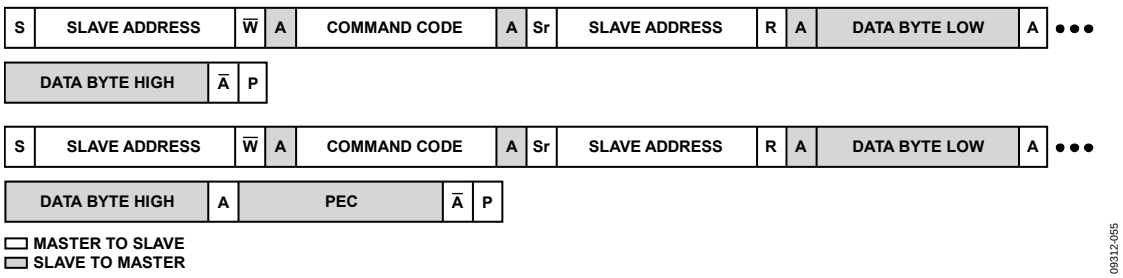


Figure 61. Read Word and Read Word with PEC

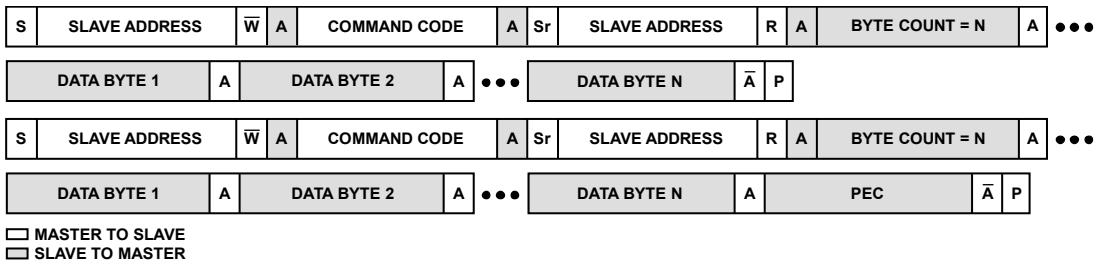


Figure 62. Block Read and Block Read with PEC

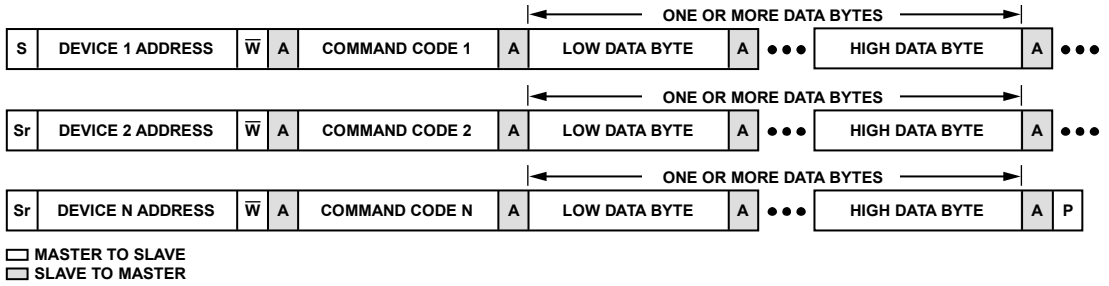


Figure 63. Group Command

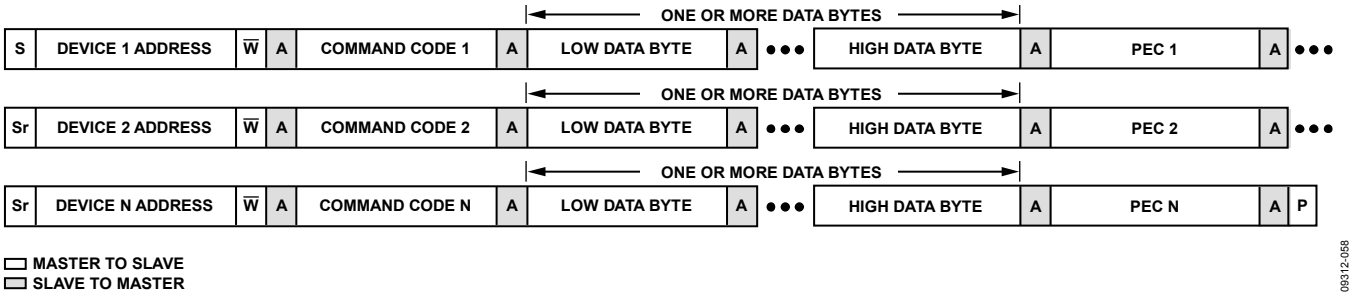


Figure 64. Group Command with PEC

GROUP COMMANDS

The PMBus standard defines what are known as group commands. Group commands are single bus transactions that send commands or data to more than one device at the same time. Each device is addressed separately, using its own address; there is no special group command address. A group command transaction can contain only write commands that send data to a device. It is not possible to use a group command to read data from devices.

From an I²C protocol point of view, a normal write command consists of the following:

- I²C start condition
- Slave address bits and a write bit (followed by ACK from the slave device)
- One or more data bytes (each of which is followed by ACK from the slave device)
- I²C stop condition to end the transaction

A group command differs from a nongroup command in that, after the data is written to one slave device, a repeated start condition is put on the bus followed by the address of the next slave device and data. This continues until all the devices have been written to, at which point the stop condition is put on the bus by the master device.

The format of a group command and a group command with PEC is shown in Figure 64.

Each device that is written to as part of the group command does not immediately execute the command written. The device must wait until the stop condition appears on the bus. At that point, all devices execute their commands at the same time.

Using a group command, it is possible, for example, to turn multiple PMBus devices on or off at the same time. In the case of the ADM1075, it is also possible to issue a power monitor command that initiates a conversion, causing multiple ADM1075 devices to sample together at the same time. This is analogous to connecting the GPO1/$\overline{\text{ALERT1}}$/CONV pins together and configuring the pin in the convert (CONV) mode to drive the power monitor sampling.

HOT SWAP CONTROL COMMANDS

OPERATION Command

The GATE pin that drives the FET is controlled by a dedicated hot swap state machine. The UVH, UVL, and OV input pins, along with the TIMER and SS pins and the current sense, all feed into the state machine and control when and how strongly the gate is turned off.

It is also possible to control the hot swap GATE output using commands over the PMBus interface. The OPERATION command can be used to request the hot swap output to turn on. However, if the UV pin indicates that the input supply is less than required, the hot swap output is not turned on, even if the OPERATION command indicates that the output should be enabled.

If the OPERATION command is used to disable the hot swap output, the GATE pin is held low, even if all hot swap state machine control inputs indicate that it can be enabled.

The default state of the OPERATION command ON bit is 1; therefore, the hot swap output is always enabled when the ADM1075 comes out of UVLO. If the ON bit is never changed, the UV input is the hot swap master on/off control signal.

By default, at power-up, the OPERATION command is disabled and must be enabled using the DEVICE_CONFIG command. This prevents inadvertent shutdowns of the hot swap controller by software.

If the ON bit is set to 0 while the UV signal is high, the hot swap output is turned off. If the UV signal is low or if the OV signal is high, the hot swap output is already off and the status of the ON bit has no effect.

If the ON bit is set to 1, the hot swap output is requested to turn on. If the UV signal is low or if the OV signal is high, setting the ON bit to 1 has no effect, and the hot swap output remains off.

It is possible to determine at any time whether the hot swap output is enabled using the STATUS_BYTE or the STATUS_WORD command (see the Status Commands section).

The OPERATION command can also be used to clear any latched faults in the status registers. To clear latched faults, set the ON bit to 0, and then reset it to 1.

DEVICE_CONFIG Command

The DEVICE_CONFIG command is used to configure certain settings within the ADM1075, for example, to modify the duration of the severe overcurrent glitch filter and to set the trip threshold. This command is also used to configure the polarity of the second IOUT current warnings.

At power-up, the OPERATION command is disabled, and the ADM1075 responds with a NACK if the OPERATION command is received. To allow use of the OPERATION command, the OPERATION_CMD_EN bit must be set using the DEVICE_CONFIG command.

POWER_CYCLE Command

The POWER_CYCLE command can be used to request that the ADM1075 be turned off for ~10 seconds and then back on. This command can be useful if the processor that controls the ADM1075 is also powered off when the part is turned off. This command allows the processor to request that the ADM1075 turn off and back on again as part of a single command.

ADM1075 INFORMATION COMMANDS

CAPABILITY Command

The CAPABILITY command can be used by host processors to determine the I²C bus features supported by the ADM1075. The features reported are the maximum bus speed and whether the device supports the packet error checking (PEC) byte and the SMBAlert reporting function.

PMBUS_REVISION Command

The PMBUS_REVISION command reports the version of Part I and Part II of the PMBus standard.

MFR_ID, MFR_MODEL, and MFR_REVISION Commands

The MFR_ID, MFR_MODEL, and MFR_REVISION commands return ASCII strings that can be used to facilitate detection and identification of the ADM1075 on the bus.

These commands are read using the SMBus block read message type. This message type requires that the ADM1075 return a byte count corresponding to the length of the string data that is to be read back.

STATUS COMMANDS

The ADM1075 provides a number of status bits that are used to report faults and warnings from the hot swap controller and the power monitor. These status bits are located in six different registers that are arranged in a hierarchy. The STATUS_BYTE and STATUS_WORD commands provide eight bits and 16 bits of high level information, respectively. The STATUS_BYTE and STATUS_WORD commands contain the most important status bits, as well as pointer bits that indicate whether any of the four other status registers need to be read for more detailed status information.

In the ADM1075, a particular distinction is made between faults and warnings. A fault is always generated by the hot swap controller and is defined by hardware component values. Three events can generate a fault.

- Overcurrent condition that causes the hot swap timer to time out
- Overvoltage condition on the OV pin
- Undervoltage condition on the UVx pin

When a fault occurs, the hot swap controller always takes some action, usually to turn off the GATE pin, which is driving the FET. A fault can also generate an SMBAlert on one or both of the GPOx/$\overline{\text{ALERTx}}$ pins.

All warnings in the ADM1075 are generated by the power monitor sampling voltage and current and then comparing these measurements to the threshold values set by the various limit commands. A warning has no effect on the hot swap controller, but it may generate an SMBAlert on one or both of the GPOx/ALERTx output pins.

When a fault or warning status bit is set, it always means that the status condition—fault or warning—is active or was active at some point in the past. When a fault or warning bit is set, it is latched until it is explicitly cleared using either the OPERATION or the CLEAR_FAULTS command. Some other status bits are live, that is, they always reflect a status condition and are never latched.

STATUS_BYTE and STATUS_WORD Commands

The STATUS_BYTE and STATUS_WORD commands can be used to obtain a snapshot of the overall part status. These commands indicate whether it is necessary to read more detailed information using the other status commands.

The low byte of the word returned by the STATUS_WORD command is the same byte returned by the STATUS_BYTE command. The high byte of the word returned by the STATUS_WORD command provides a number of bits that can be used to determine which of the other status commands must be issued to obtain all active status bits.

STATUS_INPUT Command

The STATUS_INPUT command returns a number of bits relating to voltage faults and warnings and power warnings on the input supply.

STATUS_IOUT Command

The STATUS_IOUT command returns a number of bits relating to current faults and warnings on the output supply.

STATUS_VAUX Command

The STATUS_VAUX command returns a number of bits relating to current faults and warnings on the output supply.

STATUS_MFR_SPECIFIC Command

The STATUS_MFR_SPECIFIC command is a standard PMBus command, but the contents of the byte returned is specific to the ADM1075.

CLEAR_FAULTS Command

The CLEAR_FAULTS command is used to clear fault and warnings bits when they are set. Fault and warnings bits are latched when they are set. In this way, a host can read the bits any time after the fault or warning condition occurs and determine which problem actually occurred.

If the CLEAR_FAULTS command is issued and the fault or warning condition is no longer active, the status bit is cleared. If the condition is still active—for example, if an input voltage is below the undervoltage threshold of the UV pin—the CLEAR_FAULTS command attempts to clear the status bit, but that status bit is immediately set again.

GPO AND ALERT PIN SETUP COMMANDS

Two multipurpose pins are provided on the ADM1075: GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$.

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins have two output modes of operation. These pins can be configured independently over the PMBus as general-purpose digital outputs. They can both be configured to generate an SMBAlert when one or more fault/warning status bits become active in the PMBus status registers. For an example of how to configure these pins to generate an SMBAlert and how to respond and clear the condition, see the Example Use of SMBus Alert Response Address section.

The GPO1/$\overline{\text{ALERT1}}$/CONV pin can also be configured as an input (CONV) to drive the power monitor in single-shot run mode and to control when a power monitor ADC sampling cycle begins. This function can be used to synchronize sampling across multiple ADM1075 devices, if required.

ALERT1_CONFIG and ALERT2_CONFIG Commands

Using combinations of bit masks, the ALERT1_CONFIG and ALERT2_CONFIG commands can be used to select the status bits that, when set, generate an SMBAlert signal to a processor. They can also be used to set a GPO mode on the pin, so that it is under software control. If this mode is set, the SMBAlert masking bits are ignored.

On the ADM1075, one of the inputs can also be configured as a hardware-based convert control signal. If this mode is set, the GPO and SMBAlert masking bits are ignored.

POWER MONITOR COMMANDS

The ADM1075 provides a high accuracy, 12-bit current and voltage power monitor. The power monitor can be configured in a number of different modes of operation and can run in either continuous mode or single-shot mode with a number of different sample averaging options.

The power monitor can measure the following:

- Input voltage (VIN)
- Output current (IOUT)
- Auxiliary voltage (VAUX)

The following quantities are then calculated:

- Input power (PIN)
- Input energy (EIN)

PMON_CONFIG Command

The power monitor can run in a number of different modes with different input voltage range settings. The PMON_CONFIG command is used to set up the power monitor.

The settings that can be configured are as follows:

- Single-shot or continuous sampling
- Enable VAUX sampling
- Current input range
- Current and voltage sample averaging

Modifying the power monitor settings while the power monitor is sampling is not recommended because it may cause spurious data or warnings to be generated.

PMON_CONTROL Command

Power monitor sampling can be initiated via software or via hardware, as follows:

- PMON_CONTROL command. This command can be used with single-shot or continuous mode.
- GPO1/ALERT1/CONV pin. If this pin is configured for convert mode, an external hardware signal can be used to take this pin high, triggering the single-shot sampling of one or more parts together.

READ_VIN, READ_VAUX, and READ_IOUT Commands

The ADM1075 power monitor measures the voltage developed across the sense resistor to provide a current measurement. The input voltage from the ADC_V pin is always measured, and the user can choose whether or not to measure the output voltage present on the ADC_AUX pin as well.

READ_PIN, READ_PIN_EXT, READ_EIN, and READ_EIN_EXT Commands

The VIN input voltage (12-bit) and IOUT current (12-bit) measurement values are multiplied by the ADM1075 to give the input power value. This is done using fixed point arithmetic and produces a 24-bit value. It is assumed that the numbers are of the 12.0 format, meaning there is no fractional part. It should be noted that only positive IOUT values are used to avoid returning a negative power.

This 24-bit value can be read from the ADM1075 using the READ_PIN_EXT command, where the most significant bit (MSB) is always a zero because PIN_EXT is a twos complement binary value that is always positive.

The 16 most significant bits of the 24-bit value are used as the value for input power (PIN). The MSB of the 16-bit PIN word is always zero because PIN is a twos complement binary value that is always positive.

Each time a power calculation is performed, the 24-bit power value is added to a 24-bit energy accumulator register. This is a twos complement representation as well; therefore, the MSB is always zero. Each time this energy accumulator register rolls over from 0x7FFFFF to 0x000000, a 16-bit rollover counter is incremented. The rollover counter is straight binary, with a maximum value of 0xFFFF before it rolls over.

There is also a 24-bit straight binary power sample counter that is incremented by one each time a power value is calculated and added to the energy accumulator.

These registers can be read back using one of two commands, depending on the level of accuracy required for the energy accumulator and the desire to limit the frequency of reads from the ADM1075.

A bus host can read these values, and, using some difference calculations, determine the amount of energy consumed since the last read and the number of samples in that time. The bus host, using an external real-time clock, can then determine the power used in the last time period.

To avoid the loss of data, the bus host must read at a rate that ensures the rollover counter does not wrap around more than once and, if it does wrap around, that the next rollover value is less than the previous one.

The READ_EIN command returns the top 16 bits of the energy accumulator, the lower eight bits of the rollover counter, and the full 24 bits of the sample counter.

The READ_EIN_EXT command returns the full 24 bits of the energy accumulator, the full 16 bits of the rollover counter, and the full 24 bits of the sample counter. The use of the longer rollover counter means that the time interval between reads of the part to ensure that no data is lost can be increased from seconds to minutes.

PEAK_IOUT, PEAK_VIN, PEAK_VAUX, and PEAK_PIN Commands

In addition to the standard PMBus commands for reading voltage and current, the ADM1075 provides commands that can report the maximum peak voltage, current, or power value since the peak value was last cleared.

The peak values are updated only after the power monitor has sampled and averaged the current and voltage measurements. Individual peak values are cleared by writing a 0 value with the corresponding commands.

WARNING LIMIT SETUP COMMANDS

The ADM1075 power monitor can monitor a number of different warning conditions simultaneously and report any current or voltage values that exceed the user-defined thresholds using the status commands.

All comparisons performed by the power monitor require the measured voltage or current value to be strictly greater or less than the threshold value.

At power-up, all threshold limits are set to either minimum scale (for undervoltage or undercurrent conditions) or to maximum scale (for overvoltage, overcurrent or overpower conditions). This effectively disables the generation of any status warnings by default; warning bits are not set in the status registers until the user explicitly sets the threshold values.

VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT Commands

The VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT commands are used to set the OV and UV thresholds on the input voltage, as measured at the ADC_V pin.

VAUX_OV_WARN_LIMIT and VAUX_UV_WARN_LIMIT Commands

The VAUX_OV_WARN_LIMIT and VAUX_UV_WARN_LIMIT commands are used to set the OV and UV thresholds on the output voltage, as measured at the ADC_VAUX pin on the ADM1075.

PIN_OP_WARN_LIMIT Command

The PIN_OP_WARN_LIMIT command is used to set the overpower (OP) threshold for the power measurement register.

IOUT_OC_WARN_LIMIT Command

The IOUT_OC_WARN_LIMIT command is used to set the overcurrent (OC) threshold for the current flowing through the sense resistor.

IOUT_WARN2_LIMIT Command

The IOUT_WARN2_LIMIT command provides a second current warning threshold that can be programmed. The polarity of this warning can be set to overcurrent or undercurrent using the DEVICE_CONFIG command.

PMBus DIRECT FORMAT CONVERSION

The ADM1075 uses the PMBus direct format internally to represent real-world quantities such as voltage, current, and power values. A direct format number takes the form of a 2-byte, twos complement binary integer value.

It is possible to convert between direct format value and real-world quantities using the following equations. Equation 1 converts from real-world quantities to PMBus direct values, and Equation 2 converts PMBus direct format values to real-world values.

$$Y = (mX + b) \times 10^{R} \quad (1)$$

$$X = 1/m \times (Y \times 10^{-R} - b) \quad (2)$$

where:
Y is the value in PMBus direct format.
X is the real-world value.
m is the slope coefficient, a 2-byte, twos complement integer.
b is the offset, a 2-byte, twos complement integer.
R is a scaling exponent, a 1-byte, twos complement integer.

The same equations are used for voltage, current, and power conversions, the only difference being the values of the m, b, and R coefficients used.

Table 7 lists all the coefficients required for the ADM1075. The coefficients shown are dependent on the value of the external sense resistor used in a given application. This means that an additional calculation must be performed to take the sense resistor value into account to obtain the coefficients for a specific sense resistor value. The resistor divider scaling factor on VIN/VAUX also needs to be taken into account when performing a voltage or power calculation (see Example 4).

The sense resistor value used in the calculations to obtain the coefficients is expressed in milliohms. The m coefficients are defined as 2-byte twos complement numbers in the PMBus standard; therefore, the maximum positive value that can be represented is 32,767. If the m value is greater than that, and is to be stored in PMBus standard form, the m coefficients should be divided by 10, and the R coefficient increased by a value of 1. For example, if performing a power calculation on the ADM1075-1 with a 10 mΩ sense resistor, the m coefficient is 8549, and the R coefficient is 0.

Example 1

IOUT_OC_WARN_LIMIT requires a current limit value expressed in direct format.

If the required current limit is 10 A, and the sense resistor is 2 mΩ, the first step is to determine the voltage coefficient. For an ADM1075-1, this is simply m = 806 × 2, giving 1612.

Using Equation 1, and expressing X, in units of amps,

$$Y = ((1612 \times 10) + 20{,}475) \times 10^{-1}$$

$$Y = 3659.5 = 3660 \text{ (rounded up to integer form)}$$

Writing a value of 3660 with the IOUT_OC_WARN_LIMIT command sets an overcurrent warning at 10 A.

Example 2

The READ_IOUT command returns a direct format value of 3341, representing the current flowing through a sense resistor of 1 mΩ.

To convert this value to the current flowing, use Equation 2, with $m = 806 \times 1$ (for the ADM1075-1):

$$X = 1/806 \times (3341 \times 10^{1} - 20{,}475)$$

$$X = 16.05 \text{ A}$$

This means that when READ_IOUT returns a value of 3341, 16.05 A is flowing in the sense resistor.

Note the following:

- The same calculations that are used to convert power values also apply to the energy accumulator value returned by the READ_EIN command because the energy accumulator is a summation of multiple power values.
- The READ_PIN_EXT and READ_EIN_EXT commands return 24-bit extended precision versions of the 16-bit values returned by READ_PIN and READ_EIN. The direct format values must be divided by 256 prior to being converted with the coefficients shown in Table 7.

Table 7. PMBus Conversion to Real-World Coefficients

Coefficient	Voltage (V)	Current (A)		Power (W)—Resistor Scaled	
		ADM1075-1	ADM1075-2	ADM1075-1	ADM1075-2
m	27,169	806 × R_{SENSE}	404 × R_{SENSE}	8549 × R_{SENSE}	4279 × R_{SENSE}
b	0	20,475	20,475	0	0
R	−1	−1	−1	−1	−1

Example 3

The READ_VIN command returns a direct format value of 1726. The ADC_V pin is shorted to the OV pin, which is connected to the input supply via an 820 kΩ/11 kΩ resistor divider.

To convert this value to the input voltage, use Equation 2

$$X = 1/27{,}169 \times (1726 \times 10^{1} - 0)$$

$$X = 0.635 \text{ V}$$

This corresponds to 0.635 V at the ADC_V pin. To obtain the input voltage, this must be amplified by the resistor divider ratio,

$$X = 0.635 \text{ V} \times (820 \text{ k}\Omega + 11 \text{ k}\Omega)/11 \text{ k}\Omega = 47.99 \text{ V}$$

Example 4

The PIN_OP_WARN_LIMIT command requires a power limit value expressed in direct format.

If the required power limit is 350 W and the sense resistor is 1 mΩ, the first step is to determine the m coefficient. Assuming an ADM1075-1 device, $m = 8549 \times 1 = 8549$. The resistor divider on VIN scales down the power limit referenced to the ADC input. Assuming a 49 kΩ and 1 kΩ resistor divider on VIN, this gives a scaling factor of 0.02.

Using Equation 1,

$$Y = (8549 \times (350 \times 0.02)) \times 10^{-1}$$

$$Y = 5984.3 = 5984 \text{ (rounded to the nearest integer)}$$

Writing a value of 5984 with the PIN_OP_WARN_LIMIT command sets an overpower warning at 350 W.

VOLTAGE AND CURRENT CONVERSION USING LSB VALUES

The direct format voltage and current values returned by the READ_VIN, READ_VAUX, and READ_IOUT commands, and the corresponding peak versions are the actual data output directly from the ADM1075 ADC. Because the voltages and currents are a 12-bit ADC output code, they can also be converted to real-world values with knowledge of the size of the LSB on the ADC.

The m, b, and R coefficients defined for the PMBus conversion are required to be whole integers by the standard and have therefore been rounded off slightly. Using this alternative method, with the exact LSB values, can provide slightly more accurate numerical conversions.

To convert an ADC code to current in amperes, the following formulas can be used:

$$V_{SENSE} = LSB_{xmV} \times (I_{ADC} - 2048)$$

$$I_{OUT} = V_{SENSE}/(R_{SENSE} \times 0.001)$$

where:
$V_{SENSE} = (V_{SENSE+}) - (V_{SENSE-})$.
$LSB_{25mV} = 12.4$ µV.
$LSB_{50mV} = 24.77$ µV.
I_{ADC} is the 12-bit ADC code.
I_{OUT} is the measured current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.

To convert an ADC code to a voltage, the following formula can be used:

$$V_M = LSB_{INPUTV} \times (V_{ADC} + 0.5)$$

where:
V_M is the measured value in volts.
V_{ADC} is the 12-bit ADC code.
$LSB_{INPUTV} = 368$ µV.

To convert a current in amperes to a 12-bit value, the following formulas can be used (round the result to the nearest integer):

$$V_{SENSE} = I_A \times R_{SENSE} \times 0.001$$

$$I_{CODE} = 2048 + (V_{SENSE}/LSB_{xmV})$$

where:
$V_{SENSE} = (V_{SENSE+}) - (V_{SENSE-})$.
I_A is the current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.
I_{CODE} is the 12-bit ADC code.
$LSB_{25mV} = 12.4$ µV.
$LSB_{50mV} = 24.77$ µV.

To convert a voltage to a 12-bit value, the following formula can be used (round the result to the nearest integer):

$$V_{CODE} = (V_A/LSB_{INPUTV}) - 0.5$$

where:
V_{CODE} is the 12-bit ADC code.
V_A is the voltage value in volts.
$LSB_{INPUTV} = 368$ µV.

ADM1075 ALERT PIN BEHAVIOR

The ADM1075 provides a very flexible alert system, whereby one or more fault/warning conditions can be indicated to an external device.

FAULTS AND WARNINGS

A PMBus fault on the ADM1075 is always generated due to an analog event and causes a change in state in the hot swap output, turning it off. The three defined fault sources are as follows:

- Undervoltage (UV) event detected on the UVH and UVL pins
- Overvoltage (OV) event detected on the OV pin
- Overcurrent (OC) event that causes a hot swap timeout

Faults are continuously monitored, and, as long as power is applied to the device, they cannot be disabled. When a fault occurs, a corresponding status bit is set in one or more STATUS_xxx registers.

A value of 1 in a status register bit field always indicates a fault or warning condition. Fault and warning bits in the status registers are latched when set to 1. To clear a latched bit to 0—provided that the fault condition is no longer active—use the CLEAR_FAULTS command or use the OPERATION command to turn the hot swap output off and then on again.

The latched status registers provide fault recording functionality. In the event of a fault, the HS_SHUTDOWN_CAUSE bits in the manufacturing specific status register (0x80) can be used to identify the fault source (UV, OV, or OC). Other status registers can also be checked for more fault and warning information.

A warning is less severe than a fault and never causes a change in the state of the hot swap controller. The eight sources of a warning are defined as follows:

- CML: a communications error occurred on the I^2C bus
- HS timer was active (HSTA): the current regulation was active but does not necessarily shut the system down
- IOUT OC warning from the ADC
- IOUT Warning 2 from the ADC
- VIN UV warning from the ADC
- VIN OV warning from the ADC
- VAUX UV warning from the ADC
- VAUX OV warning from the ADC
- PIN OP warning from the ADC

GENERATING AN ALERT

A host device can periodically poll the ADM1075 using the status commands to determine whether a fault/warning is active. However, this polling is very inefficient in terms of software and processor resources. The ADM1075 has two GPOx/$\overline{\text{ALERTx}}$ output pins that can be used to generate interrupts to a host processor, GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$.

By default, at power-up, the open-drain GPOx/$\overline{\text{ALERTx}}$ outputs are high impedance; therefore, the pins can be pulled high through resistors. No faults or warnings are enabled on the GPO2/$\overline{\text{ALERT2}}$ pin at power-up; the user must explicitly enable the faults or warnings to be monitored. The FET health bad warning is active by default on the GPO1/$\overline{\text{ALERT1}}$/CONV pin at power-up.

Any one or more of the faults and warnings listed in the Faults and Warnings section can be enabled and cause an alert, making the corresponding GPOx/$\overline{\text{ALERTx}}$ pin active. By default, the active state of a GPOx/$\overline{\text{ALERTx}}$ pin is low.

For example, to use GPO1/$\overline{\text{ALERT1}}$/CONV to monitor the IOUT OC warning from the ADC, the followings steps must be performed:

1. Set a threshold level with the IOUT_OC_WARN_LIMIT command.
2. Set the IOUT_OC_WARN_EN1 bit in the ALERT1_CONFIG register
3. Start the power monitor sampling on IOUT.

If an IOUT sample is taken that is above the configured IOUT OC value, the GPO1/$\overline{\text{ALERT1}}$/CONV pin is taken low, signaling an interrupt to a processor.

HANDLING/CLEARING AN ALERT

When faults/warnings are configured on the GPOx/$\overline{\text{ALERTx}}$ pins, the pins become active to signal an interrupt to the processor. (These pins are active low, unless inversion is enabled.) The GPOx/$\overline{\text{ALERTx}}$ signal performs the function of an SMBAlert.

Note that the GPOx/$\overline{\text{ALERTx}}$ pins can become active independently of each other, but they are always made inactive together.

A processor can respond to the interrupt in one of two basic ways:

- If there is only one device on the bus, the processor can simply read the status bytes and issue a CLEAR_FAULTS command to clear all the status bits, which causes the deassertion of the GPOx/$\overline{\text{ALERTx}}$ line. If there is a persistent fault—for example, an undervoltage on the input—the status bits remain set after the CLEAR_FAULTS command is executed because the fault has not been removed. However, the GPOx/$\overline{\text{ALERTx}}$ line is not pulled low unless a new fault/warning becomes active. If the cause of the SMBAlert is a power monitor generated warning and the power monitor is running continuously, the next sample generates a new SMBAlert after the CLEAR_FAULTS command is issued.
- If there are many devices on the bus, the processor can issue an SMBus alert response address command to find out which device asserted the SMBAlert line. The processor can read the status bytes from that device and issue a CLEAR_FAULTS command.

SMBus ALERT RESPONSE ADDRESS

The SMBus alert response address (ARA) is a special address that can be used by the bus host to locate any devices that need to talk to it. A host typically uses a hardware interrupt pin to monitor the SMBus alert pins of a number of devices. When the host interrupt occurs, the host issues a message on the bus using the SMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have an SMBAlert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active SMBAlert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its SMBusAlert signal. If the host sees that the SMBus alert signal is still low, it continues to read addresses until all devices that need to talk to it have successfully transmitted their addresses.

EXAMPLE USE OF SMBus ALERT RESPONSE ADDRESS

The full sequence of steps that occurs when an SMBAlert is generated and cleared is as follows:

1. A fault or warning is enabled using the ALERT1_CONFIG command, and the corresponding status bit for the fault or warning goes from 0 to 1, indicating that the fault/warning has just become active.
2. The GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin becomes active (low) to signal that an SMBAlert is active.
3. The host processor issues an SMBus alert response address to determine which device has an active alert.
4. If there are no other active alerts from devices with lower I^2C addresses, this device makes the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin inactive (high) during the NACK bit period after it sends its address to the host processor.
5. If the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin stays low, the host processor must continue to issue SMBus alert response address commands to devices to find out the addresses of all devices whose status it must check.
6. The ADM1075 continues to operate with the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin inactive and the contents of the status bytes unchanged until the host reads the status bytes and clears them, or until a new fault occurs. That is, if a status bit for a fault/warning that is enabled on the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin and that was not already active (equal to 1) goes from 0 to 1, a new alert is generated, causing the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin to become active again.

DIGITAL COMPARATOR MODE

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins can be configured to indicate if a user defined threshold for voltage, current, or power is being exceeded. In this mode, the output pin is live and is not latched when a warning threshold is exceeded. In effect, the pin acts as a digital comparator where the threshold is set using the warning limit threshold commands.

The ALERTx_CONFIG command is used, as for the SMBAlert configuration, to select the specific warning threshold to be monitored. The GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin then indicates if the measured value is above or below the threshold.

PMBus COMMAND REFERENCE

Register addresses are in hexadecimal format.

Table 8. PMBus Command Summary

Command Code	Command Name	SMBus Transaction Type	Number of Data Bytes	Reset
0x01	OPERATION	Read/write byte	1	0x00
0x03	CLEAR_FAULTS	Send byte	0	Not applicable
0x19	CAPABILITY	Read byte	1	0xB0
0x4A	IOUT_OC_WARN_LIMIT	Read/write word	2	0x0FFF
0x57	VIN_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0x58	VIN_UV_WARN_LIMIT	Read/write word	2	0x0000
0x6B	PIN_OP_WARN_LIMIT	Read/write word	2	0x7FFF
0x78	STATUS_BYTE	Read byte	1	0x00
0x79	STATUS_WORD	Read word	2	0x0000
0x7B	STATUS_IOUT	Read byte	1	0x00
0x7C	STATUS_INPUT	Read byte	1	0x00
0x80	STATUS_MFR_SPECIFIC	Read byte	1	0x00
0x86	READ_EIN	Block read	1 (byte count) + 6 (data)	0x06000000000000
0x88	READ_VIN	Read word	2	0x0000
0x8C	READ_IOUT	Read word	2	0x0000
0x97	READ_PIN	Read word	2	0x0000
0x98	PMBUS_REVISION	Read byte	1	0x22
0x99	MFR_ID	Block read	1 (byte count) + 3 (data)	0x03 + ASCII "ADI"
0x9A	MFR_MODEL	Block read	1 (byte count) + 9 (data)	0x09 + ASCII "ADM1075-1" or "ADM1075-2"
0x9B	MFR_REVISION	Block read	1 (byte count) + 1 (data)	0x01 + ASCII "1"
0xD0	PEAK_IOUT	Read/write word	2	0x0000
0xD1	PEAK_VIN	Read/write word	2	0x0000
0xD2	PEAK_VAUX	Read/write word	2	0x0000
0xD3	PMON_CONTROL	Read/write byte	1	0x01
0xD4	PMON_CONFIG	Read/write byte	1	0x8F for ADM1075-1; 0x97 for ADM1075-2
0xD5	ALERT1_CONFIG	Read/write word	2	0x8000
0xD6	ALERT2_CONFIG	Read/write word	2	0x0004
0xD7	IOUT_WARN2_LIMIT	Read/write word	2	0x0000
0xD8	DEVICE_CONFIG	Read/write byte	1	0x00
0xD9	POWER_CYCLE	Send byte	0	Not applicable
0xDA	PEAK_PIN	Read/write word	2	0x0000
0xDB	READ_PIN_EXT	Block read	1 (byte count) + 3 (data)	0x03000000
0xDC	READ_EIN_EXT	Block read	1 (byte count) + 8 (data)	0x080000000000000000
0xDD	READ_VAUX	Read word	2	0x0000
0xDE	VAUX_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0xDF	VAUX_UV_WARN_LIMIT	Read/write word	2	0x0000
0xF6	STATUS_VAUX	Read byte	1	0x00

REGISTER DETAILS

OPERATION COMMAND REGISTER

Address: 0x01, Reset: 0x80, Name: OPERATION

Table 9. Bit Descriptions for OPERATION

Bits	Bit Name	Settings	Description	Reset	Access
7	ON		Hot swap enable.	0x01	RW
		0	Hot swap output disabled.		
		1	Hot swap output enabled.		
[6:0]	RESERVED		Always reads as 0000000.	0x0	R

CLEAR FAULTS REGISTER

Address: 0x03, Send Byte, No Data, Name: CLEAR_FAULTS

PMBUS CAPABILITY REGISTER

Address: 0x19, Reset: 0xB0, Name: CAPABILITY

Table 10. Bit Descriptions for CAPABILITY

Bits	Bit Name	Settings	Description	Reset	Access
7	PEC_SUPPORT		Always reads as 1. Packet error checking (PEC) is supported.	0x1	R
[6:5]	MAX_BUS_SPEED		Always reads as 01. Maximum supported bus speed is 400 kHz.	0x01	R
4	SMBALERT_SUPPORT		Always reads as 1. Device supports SMBAlert and alert response address (ARA).	0x1	R
[3:0]	RESERVED		Always reads as 0000.	0x0000	R

IOUT OC WARN LIMIT REGISTER

Address: 0x4A, Reset: 0x0FFF, Name: IOUT_OC_WARN_LIMIT

Table 11. Bit Descriptions for IOUT_OC_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	IOUT_OC_WARN_LIMIT		Overcurrent threshold for the IOUT measurement through the sense resistor, expressed in ADC codes.	0xFFF	RW

VIN OV WARN LIMIT REGISTER

Address: 0x57, Reset: 0x0FFF, Name: VIN_OV_WARN_LIMIT

Table 12. Bit Descriptions for VIN_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	VIN_OV_WARN_LIMIT		Overvoltage threshold for the ADC_V pin measurement, expressed in ADC codes.	0xFFF	RW

VIN UV WARN LIMIT REGISTER

Address: 0x58, Reset: 0x0000, Name: VIN_UV_WARN_LIMIT

Table 13. Bit Descriptions for VIN_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	VIN_UV_WARN_LIMIT		Undervoltage threshold for the ADC_V pin measurement, expressed in ADC codes.	0x0	RW

PIN OP WARN LIMIT REGISTER

Address: 0x6B, Reset: 0x7FFF, Name: PIN_OP_WARN_LIMIT

Table 14. Bit Descriptions for PIN_OP_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Always reads as 0.	0x0	R
[14:0]	PIN_OP_WARN_LIMIT		Overpower threshold for the PMBus power measurement, expressed in ADC codes.	0x7FFF	RW

STATUS BYTE REGISTER

Address: 0x78, Reset: 0x00, Name: STATUS_BYTE

Table 15. Bit Descriptions for STATUS_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	R
6	HOTSWAP_OFF		Live register.	0x0	R
		0	The hot swap gate drive output is enabled.		
		1	The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the ADM1075 to latch off, an undervoltage condition on the UVx pin, or the use of the OPERATION command to turn the output off.		
5	RESERVED		Always reads as 0.	0x0	R
4	IOUT_OC_FAULT		Latched register.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down.		
3	VIN_UV_FAULT		Latched register.	0x0	R
		0	No undervoltage input fault detected on the UVH/UVL pins.		
		1	An undervoltage input fault was detected on the UVH/UVL pins.		
2	RESERVED		Always reads as 0.	0x0	R
1	CML_FAULT		Latched register.	0x0	R
		0	No communications error detected on the I^2C/PMBus interface.		
		1	An error was detected on the I^2C/PMBus interface. Errors detected are unsupported command, invalid PEC byte, and incorrectly structured message.		
0	NONE_OF_THE_ABOVE		Live register.	0x0	R
		0	No other active status bit to be reported by any other status command.		
		1	Active status bits are waiting to be read by one or more status commands.		

STATUS WORD REGISTER

Address: 0x79, Reset: 0x0000, Name: STATUS_WORD

Table 16. Bit Descriptions for STATUS_WORD

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Always reads as 0.	0x0	R
14	IOUT_STATUS		Live register.	0x0	R
		0	There are no active status bits to be read by STATUS_IOUT.		
		1	There are one or more active status bits to be read by STATUS_IOUT.		

Bits	Bit Name	Settings	Description	Reset	Access
13	INPUT_STATUS		Live register.	0x0	R
		0	There are no active status bits to be read by STATUS_INPUT.		
		1	There are one or more active status bits to be read by STATUS_INPUT.		
12	MFR_STATUS		Live register.	0x0	R
		0	There are no active status bits to be read by STATUS_MFR_SPECIFIC.		
		1	There are one or more active status bits to be read by STATUS_MFR_SPECIFIC.		
11	PGB_STATUS		Live register.	0x0	R
		0	The voltage on the DRAIN pin is above the required threshold, indicating that output power is considered good. This bit is the logical inversion of the $\overline{\text{PWRGD}}$ pin on the part.		
		1	The voltage on the DRAIN pin is below the required threshold, indicating that output power is considered bad.		
[10:8]	RESERVED		Always reads as 000.	0x0	R
[7:0]	STATUS_BYTE		This byte is the same as the byte returned by the STATUS_BYTE command.	0x0	R

IOUT STATUS REGISTER

Address: 0x7B, Reset: 0x00, Name: STATUS_IOUT

Table 17. Bit Descriptions for STATUS_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
7	IOUT_OC_FAULT		Latched register.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down.		
6	RESERVED		Always reads as 0.	0x0	R
5	IOUT_OC_WARN		Latched register.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
[4:0]	RESERVED		Always reads as 00000.	0x0	R

INPUT STATUS REGISTER

Address: 0x7C, Reset: 0x00, Name: STATUS_INPUT

Table 18. Bit Descriptions for STATUS_INPUT

Bits	Bit Name	Settings	Description	Reset	Access
7	VIN_OV_FAULT		Latched register.	0x0	R
		0	No overvoltage detected on the OV pin.		
		1	An overvoltage was detected on the OV pin.		
6	VIN_OV_WARN		Latched register.	0x0	R
		0	No overvoltage condition on the input supply detected by the power monitor.		
		1	An overvoltage condition on the input supply was detected by the power monitor.		
5	VIN_UV_WARN		Latched register.	0x0	R
		0	No undervoltage condition on the input supply detected by the power monitor.		
		1	An undervoltage condition on the input supply was detected by the power monitor.		

Bits	Bit Name	Settings	Description	Reset	Access
4	VIN_UV_FAULT		Latched register.	0x0	R
		0	No undervoltage detected on the UVx pin.		
		1	An undervoltage was detected on the UVx pin.		
[3:1]	RESERVED		Always reads as 000.	0x0	R
0	PIN_OP_WARN		Latched register.	0x0	R
		0	No overpower condition on the input supply detected by the power monitor.		
		1	An overpower condition on the input supply was detected by the power monitor.		

MANUFACTURING SPECIFIC STATUS REGISTER

Address: 0x80, Reset: 0x00, Name: STATUS_MFR_SPECIFIC

Table 19. Bit Descriptions for STATUS_MFR_SPECIFIC

Bits	Bit Name	Settings	Description	Reset	Access
7	FET_HEALTH_BAD		Latched register.	0x0	R
		0	FET behavior appears to be as expected.		
		1	FET behavior suggests that the FET may be shorted.		
6	UV_CMP_OUT		Live register.	0x0	R
		0	Input voltage to UVx pin is above threshold.		
		1	Input voltage to UVx pin is below threshold.		
5	OV_CMP_OUT		Live register.	0x0	R
		0	Input voltage to OV pin is below threshold.		
		1	Input voltage to OV pin is above threshold.		
4	VAUX_STATUS		Latched register.	0x0	R
		0	There are no active status bits to be read by STATUS_VAUX.		
		1	There are one or more active status bits to be read by STATUS_VAUX.		
3	HS_INLIM_FAULT		Latched register.	0x0	R
		0	The ADM1075 has not actively limited the current into the load.		
		1	The ADM1075 has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the time limit set by the capacitor on the TIMER pin elapses.		
[2:1]	HS_SHUTDOWN_CAUSE		Latched register.	0x0	R
		00	The ADM1075 is either enabled and working correctly, or has been shut down using the OPERATION command.		
		01	An IOUT_OC_FAULT condition occurred that caused the ADM1075 to shut down.		
		10	A VIN_UV_FAULT condition occurred that caused the ADM1075 to shut down.		
		11	A VIN_OV_FAULT condition occurred that caused the ADM1075 to shut down.		
0	IOUT_WARN2		Latched register.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_WARN2_LIMIT command.		
		1	An undercurrent or overcurrent condition on the output supply was detected by the power monitor using the IOUT_WARN2_LIMIT command. The polarity of the threshold condition is set by the IOUT_WARN2_OC_SELECT bit using the DEVICE_CONFIG command.		

READ EIN REGISTER

Address: 0x86, Reset: 0x06, 0x0000, 0x00, 0x000000, Name: READ_EIN

Table 20. Bit Descriptions for READ_EIN

Byte	Bit Name	Settings	Description	Reset	Access
[0]	BYTE_COUNT		Always reads as 0x06, the number of data bytes that the block read command should expect to read.	0x6	R
[2:1]	ENERGY_COUNT		Energy accumulator value in direct format. Byte 2 is the high byte, and Byte 1 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command. Use the READ_EIN_EXT to access the nontruncated version.	0x0	R
[3]	ROLLOVER_COUNT		Number of times that the energy count has rolled over, from 0x7FFF to 0x0000. This is a straight 8-bit binary value.	0x0	R
[6:4]	SAMPLE_COUNT		This is the total number of PIN samples acquired and accumulated in the energy count accumulator. Byte 6 is the high byte, Byte 5 is the middle byte, and Byte 4 is the low byte.	0x0	R

READ VIN REGISTER

Address: 0x88, Reset: 0x0000, Name: READ_VIN

Table 21. Bit Descriptions for READ_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	READ_VIN		Input voltage from the ADC_V pin measurement, expressed in ADC codes.	0x0	R

READ IOUT REGISTER

Address: 0x8C, Reset: 0x0000, Name: READ_IOUT

Table 22. Bit Descriptions for READ_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	READ_IOUT		Output current measurement through the sense resistor.	0x0	R

READ PIN REGISTER

Address: 0x97, Reset: 0x0000, Name: READ_PIN

Table 23. Bit Descriptions for READ_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	READ_PIN		Input power from the VIN × IOUT calculation.	0x0	R

PMBus REVISION REGISTER

Address: 0x98, Reset: 0x22, Name: PMBUS_REVISION

Table 24. Bit Descriptions for PMBUS_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PMBUS_P1_REVISION		Always reads as 0010, PMBus Specification Part I, Revision 1.2.	0x2	R
[3:0]	PMBUS_P2_REVISION		Always reads as 0010, PMBus Specification Part II, Revision 1.2.	0x2	R
		0000	Rev1.0.		
		0001	Rev1.1.		
		0010	Rev1.2.		

MANUFACTURING ID REGISTER

Address: 0x99, Reset: 0x03 + ASCII "ADI", Name: MFR_ID

Table 25. Bit Descriptions for MFR_ID

Byte	Bit Name	Settings	Description	Reset	Access
0	BYTE_COUNT		Always reads as 0x03, the number of data bytes that the block read command should expect to read.	0x3	R
1	CHARACTER1		Always reads as 0x41 = "A".	0x41	R
2	CHARACTER2		Always reads as 0x44 = "D".	0x44	R
3	CHARACTER3		Always reads as 0x49 = "I".	0x49	R

MANUFACTURING MODEL REGISTER

Address: 0x9A, Reset: 0x09 + ASCII "ADM1075-x", Name: MFR_MODEL

Table 26. Bit Descriptions for MFR_MODEL

Byte	Bit Name	Settings	Description	Reset	Access
0	BYTE_COUNT		Always reads as 0x03, the number of data bytes that the block read command should expect to read.	0x9	R
1	CHARACTER1		Always reads as 0x41 = "A".	0x41	R
2	CHARACTER2		Always reads as 0x44 = "D".	0x44	R
3	CHARACTER3		Always reads as 0x4D = "M".	0x4D	R
4	CHARACTER4		Always reads as 0x31 = "1".	0x31	R
5	CHARACTER5		Always reads as 0x30 = "0".	0x30	R
6	CHARACTER6		Always reads as 0x37 = "7".	0x37	R
7	CHARACTER7		Always reads as 0x35 = "5".	0x35	R
8	CHARACTER8		Always reads as 0x2D = "-".	0x2D	R
9	CHARACTER9		Always reads as 0x31 = "1" for ADM1075-1. Always reads as 0x32 = "2" for ADM1075-2.	0x31 or 0x32	R

MANUFACTURING REVISION REGISTER

Address: 0x9B, Reset: 0x01 + ASCII "1", Name: MFR_REVISION

Table 27. Bit Descriptions for MFR_REVISION

Byte	Bit Name	Settings	Description	Reset	Access
0	BYTE_COUNT		Always reads as 0x01, the number of data bytes that the block read command should expect to read.	0x1	R
1	CHARACTER1		Always reads as 0x31, Revision 1 of ADM1075.	0x31	R

PEAK IOUT REGISTER

Address: 0xD0, Reset: 0x0000, Name: PEAK_IOUT (writing 0x0000 clears the peak value)

Table 28. Bit Descriptions for PEAK_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	PEAK_IOUT		Returns the peak IOUT current since the register was last cleared.	0x0	R

PEAK VIN REGISTER

Address: 0xD1, Reset: 0x0000, Name: PEAK_VIN (writing 0x0000 clears the peak value)

Table 29. Bit Descriptions for PEAK_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	PEAK_VIN		Returns the peak VIN voltage since the register was last cleared.	0x0	R

PEAK VAUX REGISTER

Address: 0xD2, Reset: 0x0000, Name: PEAK_VAUX (writing 0x0000 clears the peak value)

Table 30. Bit Descriptions for PEAK_VAUX

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	PEAK_VAUX		Returns the peak VAUX voltage since the register was last cleared.	0x0	R

POWER MONITOR CONTROL REGISTER

Address: 0xD3, Reset: 0x01, Name: PMON_CONTROL

Table 31. Bit Descriptions for PMON_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Always reads as 0000000.	0x0	R
0	CONVERT			0x1	RW
		0	Power monitor is not running.		
		1	Default. Starts the sampling of current and voltage with the power monitor. In single-shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling.		

POWER MONITOR CONFIGURATION REGISTER

Address: 0xD4, Reset: 0x8F, Name: PMON_CONFIG

Table 32. Bit Descriptions for PMON_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
7	PMON_MODE			0x1	RW
		0	This setting selects single-shot sampling mode.		
		1	Default. This setting selects continuous sampling mode.		
6	VAUX_ENABLE			0x0	RW
		0	Default. The power monitor samples the input voltage on ADC_V and IOUT.		
		1	The power monitor also samples the voltage on the ADC_AUX pin.		
5	RESERVED		Always reads as 0.	0x0	RW
[4:3]	IRANGE			0x1 or 0x2	RW
		00	Reserved.		
		01	Sets current sense range to 25 mV. Default for ADM1075-1.		
		10	Sets current sense range to 50 mV. Default for ADM1075-2.		
		11	Reserved.		
[2:0]	AVERAGING			0x7	RW
		000	Disables sample averaging for current and voltage.		
		001	Sets sample averaging for current and voltage to two samples.		
		010	Sets sample averaging for current and voltage to four samples.		
		011	Sets sample averaging for current and voltage to eight samples.		
		100	Sets sample averaging for current and voltage to 16 samples.		
		101	Sets sample averaging for current and voltage to 32 samples.		
		110	Sets sample averaging for current and voltage to 64 samples.		
		111	Default. Sets sample averaging for current and voltage to 128 samples.		

ALERT1 CONFIGURATION REGISTER

Address: 0xD5, Reset: 0x8000, Name: ALERT1_CONFIG

Table 33. Bit Descriptions for ALERT1_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_BAD_EN1			0x1	RW
		0	Disables generation of SMBAlert when the FET_HEALTH_BAD bit is set.		
		1	Default. Generates SMBAlert when the FET_HEALTH_BAD bit is set. This bit is active from power-up so that a FET problem can be detected and flagged immediately without the need for software to set this bit.		
14	IOUT_OC_FAULT_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_OC_FAULT bit is set.		
		1	Generates SMBAlert when the IOUT_OC_FAULT bit is set.		
13	VIN_OV_FAULT_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_OV_FAULT bit is set.		
		1	Generates SMBAlert when the VIN_OV_FAULT bit is set.		
12	VIN_UV_FAULT_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_UV_FAULT bit is set.		
		1	Generates SMBAlert when the VIN_UV_FAULT bit is set.		
11	CML_ERROR_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the CML_FAULT bit is set.		
		1	Generates SMBAlert when the CML_ FAULT bit is set.		
10	IOUT_OC_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_OC_WARN bit is set.		
		1	Generates SMBAlert when the IOUT_OC_WARN bit is set.		
9	IOUT_WARN2_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_WARN2 bit is set.		
		1	Generates SMBAlert when the IOUT_WARN2 bit is set.		
8	VIN_OV_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_OV_WARN bit is set.		
		1	Generates SMBAlert when the VIN_OV_WARN bit is set.		
7	VIN_UV_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_UV_WARN bit is set.		
		1	Generates SMBAlert when the VIN_UV_WARN bit is set.		
6	VAUX_OV_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VAUX_OV_WARN bit is set.		
		1	Generates SMBAlert when the VAUX_OV_WARN bit is set.		
5	VAUX_UV_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the VAUX_UV_WARN bit is set.		
		1	Generates SMBAlert when the VAUX_UV_WARN bit is set.		
4	HS_INLIM_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the HS_INLIM_FAULT bit is set.		
		1	Generates SMBAlert when the HS_INLIM_FAULT bit is set.		

Bits	Bit Name	Settings	Description	Reset	Access
3	PIN_OP_WARN_EN1			0x0	RW
		0	Default. Disables generation of SMBAlert when the PIN_OP_WARN bit is set.		
		1	Generates SMBAlert when the PIN_OP_WARN bit is set.		
[2:1]	GPO1_MODE			0x0	RW
		00	Default. GPO1 is configured to generate SMBAlerts.		
		01	GPO1 can be used a general-purpose digital output pin. The GPO1_INVERT bit is used to change the output state.		
		10	GPO1 is configured as a convert (CONV) input pin.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.		
0	GPO1_INVERT			0x0	RW
		0	Default. In GPO mode, the GPO1 pin is active low.		
		1	In GPO mode, the GPO1 pin is active high.		

ALERT2 CONFIGURATION REGISTER

Address: 0xD6, Reset: 0x0004, Name: ALERT2_CONFIG

Table 34. Bit Descriptions for ALERT2_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_BAD_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the FET_HEALTH_BAD bit is set.		
		1	Generates SMBAlert when the FET_HEALTH_BAD bit is set. This bit is active from power-up so that a FET problem can be detected and flagged immediately without the need for software to set this bit.		
14	IOUT_OC_FAULT_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_OC_FAULT bit is set.		
		1	Generates SMBAlert when the IOUT_OC_FAULT bit is set.		
13	VIN_OV_FAULT_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_OV_FAULT bit is set.		
		1	Generates SMBAlert when the VIN_OV_FAULT bit is set.		
12	VIN_UV_FAULT_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_UV_FAULT bit is set.		
		1	Generates SMBAlert when the VIN_UV_FAULT bit is set.		
11	CML_ERROR_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the CML_FAULT bit is set.		
		1	Generates SMBAlert when the CML_FAULT bit is set.		
10	IOUT_OC_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_OC_WARN bit is set.		
		1	Generates SMBAlert when the IOUT_OC_WARN bit is set.		
9	IOUT_WARN2_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the IOUT_WARN2 bit is set.		
		1	Generates SMBAlert when the IOUT_WARN2 bit is set.		
8	VIN_OV_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_OV_WARN bit is set.		
		1	Generates SMBAlert when the VIN_OV_WARN bit is set.		

Bits	Bit Name	Settings	Description	Reset	Access
7	VIN_UV_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VIN_UV_WARN bit is set.		
		1	Generates SMBAlert when the VIN_UV_WARN bit is set.		
6	VAUX_OV_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VAUX_OV_WARN bit is set.		
		1	Generates SMBAlert when the VAUX_OV_WARN bit is set.		
5	VAUX_UV_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the VAUX_UV_WARN bit is set.		
		1	Generates SMBAlert when the VAUX_UV_WARN bit is set.		
4	HS_INLIM_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the HS_INLIM_FAULT bit is set.		
		1	Generates SMBAlert when the HS_INLIM_FAULT bit is set.		
3	PIN_OP_WARN_EN2			0x0	RW
		0	Default. Disables generation of SMBAlert when the PIN_OP_WARN bit is set.		
		1	Generates SMBAlert when the PIN_OP_WARN bit is set.		
[2:1]	GPO2_MODE			0x2	RW
		00	GPO2 is configured to generate SMBAlerts.		
		01	GPO2 can be used a general-purpose digital output pin. The GPO2_INVERT bit is used to change the output state.		
		10	Default. GPO2 is configured as a retry fail output.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.		
0	GPO2_INVERT			0x0	RW
		0	Default. In GPO mode, the GPO2 pin is active low.		
		1	In GPO mode, the GPO2 pin is active high.		

IOUT WARN2 LIMIT REGISTER

Address: 0xD7, Reset: 0x0000, Name: IOUT_WARN2_LIMIT

Table 35. Bit Descriptions for IOUT_WARN2_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	IOUT_WARN2_LIMIT		Threshold for the IOUT measurement through the sense resistor, expressed in ADC codes. This value can be either an undercurrent or overcurrent, depending on the state of the IOUT_WARN2_OC_SELECT bit set using the DEVICE_CONFIG command.	0x0	RW

DEVICE CONFIGURATION REGISTER

Address: 0xD8, Reset: 0x05, Name: DEVICE_CONFIG

Table 36. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Always reads as 00.	0x00	R
5	OPERATION_CMD_ENABLE		Enable operation command.	0x0	RW
		0	The OPERATION command is disabled, and the ADM1075 issues a NACK if the command is received. This setting provides some protection against a card accidentally turning itself off		
		1	The OPERATION command is enabled, and the ADM1075 responds to it.		

Bits	Bit Name	Settings	Description	Reset	Access
4	IOUT_WARN2_OC_SELECT		Sets IOUT Warning 2 limit to OC or UC.	0x0	RW
		0	Configures IOUT_WARN2_LIMIT as an undercurrent threshold.		
		1	Configured IOUT_WARN2_LIMIT as an overcurrent threshold.		
[3:2]	OC_TRIP_SELECT		Sets severe OC trip threshold.	0x1	RW
		00	125%.		
		01	150%. Default.		
		10	200%.		
		11	225%.		
[1:0]	OC_FILT_SELECT		Sets severe OC filter time.	0x1	RW
		00	200 ns.		
		01	900 ns. Default.		
		10	10.7 µs.		
		11	57 µs.		

POWER CYCLE REGISTER

Address: 0xD9, Send Byte, No Data, Name: POWER_CYCLE

PEAK PIN REGISTER

Address: 0xDA, Reset: 0x0000, Name: PEAK_PIN (writing 0x0000 clears the peak value)

Table 37. Bit Descriptions for PEAK_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PEAK_PIN		Returns the peak input power since the register was last cleared.	0x0	R

READ PIN_EXT REGISTER

Address: 0xDB, Reset: 0x03, 0x000000, Name: READ_PIN_EXT

Table 38. Bit Descriptions for READ_PIN_EXT

Byte	Bit Name	Settings	Description	Reset	Access
[0]	BYTE_COUNT		Always reads as 0x03, the number of data bytes that the block read command should expect to read.	0x3	R
[3:1]	READ_PIN_EXT		This is the result of the VIN × IOUT calculation that has not been truncated. Byte 3 is the high byte, Byte 2 is the middle byte, and Byte 1 is the low byte.	0x0	R

READ EIN_EXT REGISTER

Address: 0xDC, Reset: 0x08, 0x000000, 0x0000, 0x000000, Name: READ_EIN_EXT

Table 39. Bit Descriptions for READ_EIN_EXT

Byte	Bit Name	Settings	Description	Reset	Access
[0]	BYTE_COUNT		Always reads as 0x08, the number of data bytes that the block read command should expect to read.	0x8	R
[3:1]	ENERGY_EXT		This is the 24-bit energy accumulator in direct format. Byte 3 is the high byte, Byte 2 is the middle byte, and Byte 1 is the low byte.	0x0	R
[5:4]	ROLLOVER_EXT		Number of times that the energy count has rolled over, from 0x7FFF to 0x0000. This is a straight 16-bit binary value. Byte 5 is the high byte, Byte 4 is the low byte.	0x0	R
[8:6]	SAMPLE_COUNT		This is the total number of PIN samples acquired and accumulated in the energy count accumulator. Byte 8 is the high byte, Byte 7 is the middle byte, and Byte 6 is the low byte.	0x0	R

READ VAUX REGISTER

Address: 0xDD, Reset: 0x0000, Name: READ_VAUX

Table 40. Bit Descriptions for READ_VAUX

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	READ_VAUX		Output voltage from the ADC_AUX pin measurement, expressed in ADC codes.	0x0	R

VAUX OV WARN LIMIT REGISTER

Address: 0xDE, Reset: 0x0FFF, Name: VAUX_OV_WARN_LIMIT

Table 41. Bit Descriptions for VAUX_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	VAUX_OV_WARN_LIMIT		Overvoltage threshold for the ADC_AUX pin measurement, expressed in ADC codes.	0xFFF	RW

VAUX UV WARN LIMIT REGISTER

Address: 0xDF, Reset: 0x0000, Name: VAUX_UV_WARN_LIMIT

Table 42. Bit Descriptions for VAUX_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	R
[11:0]	VAUX_UV_WARN_LIMIT		Undervoltage threshold for the ADC_AUX pin measurement, expressed in ADC codes.	0x0	RW

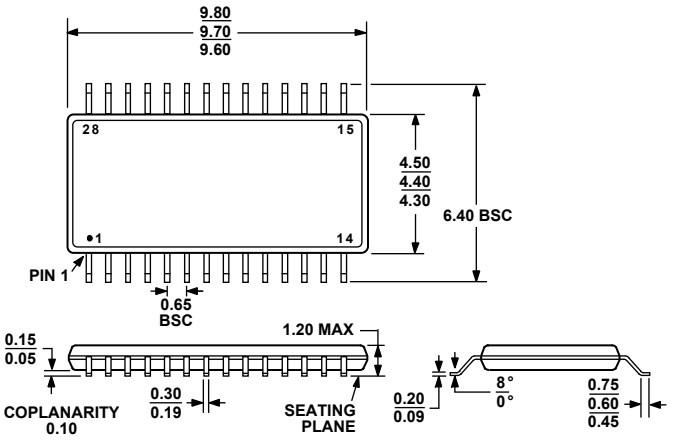
VAUX STATUS REGISTER

Address: 0xF6, Reset: 0x00, Name: STATUS_VAUX

Table 43. Bit Descriptions for STATUS_VAUX

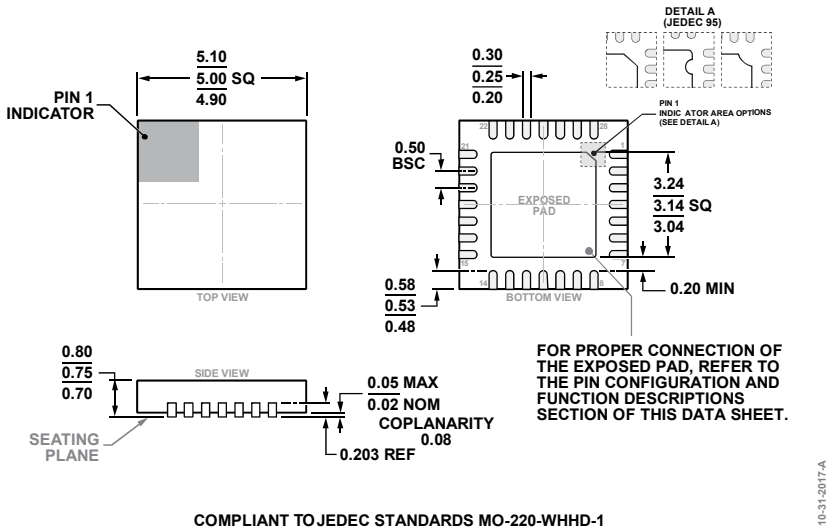
Bits	Bit Name	Settings	Description	Reset	Access
7	VAUX_OV_WARN		Latched register.	0x0	R
		0	No overvoltage condition was detected on the ADC_AUX pin by the power monitor using the VAUX_OV_WARN_LIMIT command.		
		1	An overvoltage condition was detected on the ADC_AUX pin by the power monitor using the VAUX_OV_WARN_LIMIT command.		
6	VAUX_UV_WARN		Latched register.	0x0	R
		0	No undervoltage condition was detected on the ADC_AUX pin by the power monitor using the VAUX_UV_WARN_LIMIT command.		
		1	An undervoltage condition was detected on the ADC_AUX pin by the power monitor using the VAUX_UV_WARN_LIMIT command.		
[5:0]	RESERVED		Always reads as 000000.	0x0	R

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AE

Figure 65. 28-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-28)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-1

Figure 66. 28-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-28-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADM1075-1ACPZ	−40°C to +85°C	28-Lead LFCSP (25 mV full-scale V_{SENSE})	CP-28-10
ADM1075-1ACPZ-RL7	−40°C to +85°C	28-Lead LFCSP (25 mV full-scale V_{SENSE})	CP-28-10
ADM1075-1ARUZ	−40°C to +85°C	28-Lead TSSOP (25 mV full-scale V_{SENSE})	RU-28
ADM1075-1ARUZ-RL7	−40°C to +85°C	28-Lead TSSOP (25 mV full-scale V_{SENSE})	RU-28
ADM1075-2ACPZ	−40°C to +85°C	28-Lead LFCSP_WQ (50 mV full-scale V_{SENSE})	CP-28-10
ADM1075-2ACPZ-RL7	−40°C to +85°C	28-Lead LFCSP_WQ (50 mV full-scale V_{SENSE})	CP-28-10
ADM1075-2ARUZ	−40°C to +85°C	28-Lead TSSOP (50 mV full-scale V_{SENSE})	RU-28
ADM1075-2ARUZ-RL7	−40°C to +85°C	28-Lead TSSOP (50 mV full-scale V_{SENSE})	RU-28
EVAL-ADM1075EBZ		Evaluation Board	
EVAL-ADM1075MEBZ		Evaluation Board	
USB-SDP-CABLEZ		Controller Board	

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature is −40°C to +105°C.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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