THE DATASHEET OF

ADM1278-2ACPZ-RL

Hot Swap Controller and Digital Power and Energy Monitor with PMBus Interface

Data Sheet **ADM1278**

FEATURES

- ±0.3% accurate, 12-bit ADC for I_{OUT}, V_{IN}, V_{OUT}, and temperature
- 320 ns response time to short circuit
- Shutdown on detection of FET health fault
- Constant power foldback for tighter FET SOA protection
- Remote temperature sensing with programmable warning and shutdown thresholds
- Resistor-programmable 5 mV to 25 mV V_{SENSE} current limit
- Programmable start-up current limit
- 1% accurate UV, OV, and PWRGD thresholds
- Split hot swap and power monitor inputs to allow additional external ADC filtering
- Reports power and energy consumption over time
- Peak detect registers for current, voltage, and power
- PROCHOT power throttling capability
- PMBus fast mode compliant interface
- 5 mm × 5 mm, 32-lead LFCSP

APPLICATIONS

- Servers
- Power monitoring and control/power budgeting
- Telecommunication and data communication equipment

TYPICAL APPLICATION CIRCUIT

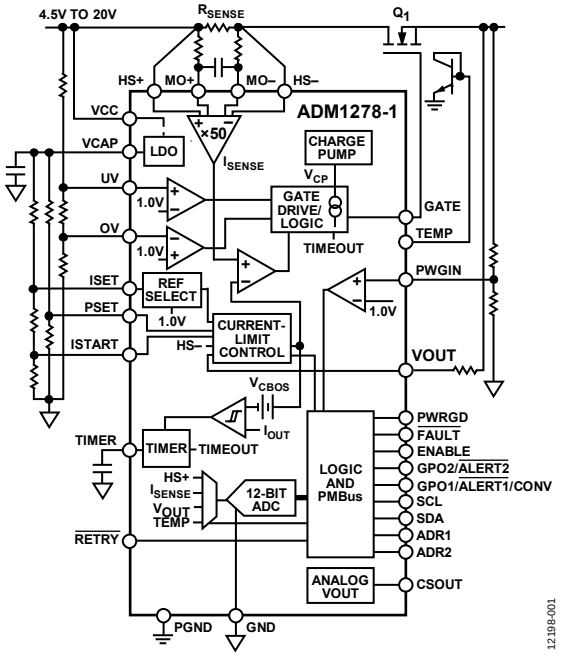

Figure 1.

GENERAL DESCRIPTION

The ADM1278 is a hot swap controller that allows a circuit board to be removed from or inserted into a live backplane. It also features current, voltage, power, and temperature readback via an integrated 12-bit analog-to-digital converter (ADC), accessed using a PMBus™ interface. The load current is measured using an internal current sense amplifier that measures the voltage across a sense resistor in the power path via the HS+ and HS− pins. A default current limit of 20 mV is set, but this limit can be adjusted, if required.

The ADM1278 limits the current through the sense resistor by controlling the gate voltage of an external N-channel FET in the power path, via the GATE pin. The sense voltage, and therefore the load current, is maintained below the preset maximum. The ADM1278 protects the external FET by limiting the time that the FET remains on while the current is at its maximum value. This current-limit time is set by the choice of capacitor connected to the TIMER pin. In addition, a constant power foldback scheme is used to control the power dissipation in the MOSFET during power-up and fault conditions. The level of this power, along with the TIMER regulation time, can be set to ensure that the MOSFET remains within safe operating area (SOA) limits.

In case of a short-circuit event, a fast internal overcurrent detector responds within 320 ns and signals the gate to shut down. A 1500 mA pull-down device ensures a fast FET response.

The ADM1278 features overvoltage (OV) and undervoltage (UV) protection, programmed using external resistor dividers on the UV and OV pins. A PWRGD signal can be used to detect when the output supply is valid, using the PWGIN pin to accurately monitor the output.

The ADM1278 is available in a 32-lead LFCSP with a $\overline{\text{RETRY}}$ pin that can be configured for automatic retry or latch-off when an overcurrent fault occurs.

Table 1. Model Options

Model	ADC Accuracy	SPI Interface	Enable Pin[1]
ADM1278-1AA	±0.3%	No	Active high
ADM1278-1A	±0.7%	No	Active high
ADM1278-1B	±1.0%	No	Active high
ADM1278-2A	±0.7%	Yes	Active high
ADM1278-3A	±0.7%	No	Active low

[1] Active high relates to the ENABLE pin, and active low relates to the $\overline{\text{ENABLE}}$ pin.

Rev. B Document Feedback
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TABLE OF CONTENTS

Features ... 1
Applications ... 1
Typical Application Circuit ... 1
General Description ... 1
Revision History ... 3
Specifications ... 4
Power Monitoring Accuracy Specifications ... 8
Serial Bus Timing Characteristics ... 8
SPI Timing Characteristics (ADM1278-2) ... 9
Absolute Maximum Ratings ... 10
Thermal Characteristics ... 10
ESD Caution ... 10
Pin Configurations and Function Descriptions ... 11
Typical Performance Characteristics ... 17
Theory of Operation ... 24
Powering the ADM1278 ... 24
Hot Swap Current Sense Inputs ... 24
Power Monitor Current Sense Inputs ... 25
Current-Limit Reference ... 25
Setting the Current Limit (ISET) ... 26
Setting a Linear Output Voltage Ramp at Power-Up ... 26
Start-Up Current Limit ... 27
Constant Power Foldback ... 28
Timer ... 28
Hot Swap Retry ... 29
FET Gate Drive Clamps ... 29
Fast Response to Severe Overcurrent ... 29
Undervoltage and Overvoltage ... 29
Power Good ... 29
$\overline{\text{FAULT}}$ Pin ... 29
ENABLE/$\overline{\text{ENABLE}}$ Input ... 30
Current Sense Output (CSOUT) ... 30
Remote Temperature Sensing ... 30
SPI Interface ... 31
V_{OUT} Measurement ... 32
FET Health ... 32
Power Throttling ... 32
Power Monitor ... 32
PMBus Interface ... 34
Device Addressing ... 34
SMBus Protocol Usage ... 34
Packet Error Checking ... 34
Partial Transactions on I^2C Bus ... 35
SMBus Message Formats ... 35
Group Commands ... 37
Hot Swap Control Commands ... 37
ADM1278 Information Commands ... 37
Status Commands ... 38
GPO and Alert Pin Setup Commands ... 38
Power Monitor Commands ... 39
Warning Limit Setup Commands ... 40
PMBus Direct Format Conversion ... 40
Voltage and Current Conversion Using LSB Values ... 41
Alert Pin Behavior ... 42
Faults and Warnings ... 42
Generating an Alert ... 42
Handling/Clearing an Alert ... 42
SMBus Alert Response Address ... 43
Example Use of SMBus ARA ... 43
Digital Comparator Mode ... 43
Typical Application Circuits ... 43
PMBus Command Reference ... 45
Register Details ... 46
Operation Register ... 46
Clear Faults Register ... 46
PMBus Capability Register ... 46
V_{OUT} OV Warning Limit Register ... 46
V_{OUT} UV Warning Limit Register ... 47
I_{OUT} OC Warning Limit Register ... 47
OT Fault Limit Register ... 47
OT Warning Limit Register ... 47
V_{IN} OV Warning Limit Register ... 47
V_{IN} UV Warning Limit Register ... 48
P_{IN} OP Warning Limit Register ... 48
Status Byte Register ... 48
Status Word Register ... 49
V_{OUT} Status Register ... 50
I_{OUT} Status Register ... 50
Input Status Register ... 50
Temperature Status Register ... 51

Manufacturer Specific Status Register....51
Read E_{IN} Register....52
Read V_{IN} Register....52
Read V_{OUT} Register....53
Read I_{OUT} Register....53
Read Temperature 1 Register....53
Read P_{IN} Register....53
PMBus Revision Register....53
Manufacturer ID Register....54
Manufacturer Model Register....54
Manufacturer Revision Register....54
Manufacturer Date Register....54
Peak I_{OUT} Register....54
Peak V_{IN} Register....55
Peak V_{OUT} Register....55
Power Monitor Control Register....55
Power Monitor Configuration Register....55
Alert 1 Configuration Register....56
Alert 2 Configuration Register....57
Peak Temperature Register....57
Device Configuration Register....57
Power Cycle Register....58
Peak P_{IN} Register....59
Read P_{IN} (Extended) Register....59
Read E_{IN} (Extended) Register....59
Hysteresis Low Level Register....59
Hysteresis High Level Register....59
Hysteresis Status Register....60
Start-Up I_{OUT} Limit Register....60
Outline Dimensions....61
Ordering Guide....61

REVISION HISTORY

10/2018—Rev. A to Rev. B

Changes to Figure 4 and Figure 5....11
Changes to Figure 6....14
Updated Outline Dimensions....61
Changes to Ordering Guide....61

12/2014—Rev. 0 to Rev. A

Changes to Features Section, General Description Section, and Applications Section....1
Added Table 1, Renumbered Sequentially....1
Changes to POWER_CYCLE Command Section....37
Change to Power Cycle Register Section....58

6/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 4.5 V to 20 V, $V_{CC} \geq V_{HS+}$ and V_{MO+}, V_{HS+} = 2 V to 20 V, $V_{SENSE_HS} = (V_{HS+} - V_{HS-}) = 0$ V, T_A = −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER SUPPLY						
Operating Voltage Range	V_{CC}	4.5		20	V	
Undervoltage Lockout	UVLO	2.4		2.7	V	V_{CC} rising
Undervoltage Hysteresis			90	120	mV	
Quiescent Current	I_{CC}			5.5	mA	GATE on and power monitor running
UV PIN						
Input Current	I_{UV}			50	nA	UV ≤ 3.6 V
UV Threshold	UV_{TH}					
A Grade and AA Grade		0.99	1.0	1.01	V	UV falling
B Grade Only		0.97	1.0	1.03	V	UV falling
UV Threshold Hysteresis	UV_{HYST}	45	60	75	mV	
UV Glitch Filter	UV_{GF}	2		7	µs	50 mV overdrive
UV Propagation Delay	UV_{PD}		5	8	µs	UV low to GATE pull-down active
OV PIN						
Input Current	I_{OV}			50	nA	OV ≤ 3.6 V
OV Threshold	OV_{TH}					
A Grade and AA Grade		0.99	1.0	1.01	V	OV rising
B Grade Only		0.97	1.0	1.03	V	OV rising
OV Threshold Hysteresis	OV_{HYST}	45	60	75	mV	
OV Glitch Filter	OV_{GF}	1.5		3.5	µs	50 mV overdrive
OV Propagation Delay	OV_{PD}		3.0	4.0	µs	OV high to GATE pull-down active
HS+ AND HS− PINS						
Input Current	I_{SENSEx}			150	µA	Per individual pin; V_{HS+}, V_{HS-} = 20 V
Input Imbalance	$I_{\Delta SENSE}$			5	µA	$I_{\Delta SENSE} = (I_+ - I_-)$
MO+ AND MO− PINS						
Input Current	$I_{MO\pm}$			25	nA	Per individual pin; V_{MO+}, V_{MO-} = 20 V
VCAP PIN						
Internally Regulated Voltage	V_{VCAP}					
A Grade and AA Grade		2.68	2.7	2.72	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
B Grade Only		2.66	2.7	2.74	V	0 µA ≤ I_{VCAP} ≤ 100 µA; C_{VCAP} = 1 µF
ISET PIN						
Reference Select Threshold	$V_{ISETRSTH}$	1.35	1.5	1.65	V	If $V_{ISET} > V_{ISETRSTH}$, an internal 1 V reference (V_{CLREF}) is used
Internal Reference	V_{CLREF}		1		V	Accuracies included in total sense voltage accuracies
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Recommended Maximum Operating Range	V_{ISET}	0.25		1.25	V	5 mV to 25 mV V_{SENSE} current limit
Input Current	I_{ISET}			100	nA	$V_{ISET} \leq V_{VCAP}$
GATE PIN						Maximum voltage on the gate is always clamped to ≤31 V
GATE Drive Voltage	ΔV_{GATE}					$\Delta V_{GATE} = V_{GATE} - V_{OUT}$
		10	12	14	V	20 V ≥ V_{CC} ≥ 8 V; I_{GATE} ≤ 5 µA
		8		10	V	$V_{HS+} = V_{CC}$ = 5 V; I_{GATE} ≤ 5 µA
		7		9	V	$V_{HS+} = V_{CC}$ = 4.5 V; I_{GATE} ≤ 1 µA
GATE Pull-Up Current	I_{GATEUP}	−20		−30	µA	V_{GATE} = 0 V
GATE Pull-Down Current	I_{GATEDN}					
Regulation	I_{GATEDN_REG}	45	60	75	µA	V_{GATE} ≥ 2 V; V_{ISET} = 1.0 V; $(V_{HS+} - V_{HS-})$ = 30 mV
Slow	I_{GATEDN_SLOW}	5	10	15	mA	V_{GATE} ≥ 2 V
Fast	I_{GATEDN_FAST}	750	1500	2250	mA	V_{GATE} ≥ 12 V; V_{CC} ≥ 12 V
GATE Holdoff Resistance			20		Ω	V_{CC} = 0 V, V_{GATE} = 2 V

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
HOT SWAP SENSE VOLTAGE						
Hot Swap Sense Voltage Current Limit	$V_{SENSECL}$					
A Grade and AA Grade		19.75	20	20.25	mV	V_{ISET} > 1.65 V; V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA
B Grade Only		19.6	20	20.4	mV	V_{ISET} > 1.65 V; V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA
Constant Power Inactive						V_{GATE} = (V_{HS+} + 3 V); I_{GATE} = 0 µA; V_{DS} = (HS−) − V_{OUT}
A Grade and AA Grade		24.75	25	25.25	mV	V_{ISET} = 1.25 V; V_{DS} < 2 V
		19.75	20	20.25	mV	V_{ISET} = 1.0 V; V_{DS} < 2 V
		14.75	15	15.25	mV	V_{ISET} = 0.75 V; V_{DS} < 2 V
B Grade Only		24.6	25	25.4	mV	V_{ISET} = 1.25 V; V_{DS} < 2 V
		19.6	20	20.4	mV	V_{ISET} = 1.0 V; V_{DS} < 2 V
		14.6	15	15.4	mV	V_{ISET} = 0.75 V; V_{DS} < 2V
Constant Power Active						FET power limit = (V_{PSET} × 8)/(50 × R_{SENSE}); constant power active when V_{DS} > (V_{PSET} × 8)/I_{SET}
A Grade and AA Grade		9.25	10	10.75	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 4 V
		4.65	5	5.35	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 8 V
		1.7	2	2.3	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 20 V
B Grade Only		9	10	11	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 4 V
		4.6	5	5.4	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 8 V
		1.4	2	2.6	mV	V_{ISET} > 1.65 V; V_{PSET} = 0.25 V; V_{DS} = 20 V
Start-Up Current Limit	$V_{ISTARTCL}$					
A Grade and AA Grade		4.7	5	5.3	mV	STRT_UP_IOUT_LIM = 3; V_{ISET} > 1.65 V
		3.7	4	4.3	mV	V_{ISTART} = 0.2 V
B Grade Only		4.5	5	5.5	mV	STRT_UP_IOUT_LIM = 3; V_{ISET} > 1.65 V
		3.5	4	4.5	mV	V_{ISTART} = 0.2 V
Start-Up Current-Limit Clamp	$V_{ISTARTCL_CLAMP}$					
A Grade and AA Grade		1.6	2	2.4	mV	V_{ISTART} = 0 V or STRT_UP_IOUT_LIM = 0
B Grade Only		1.4	2	2.6	mV	V_{ISTART} = 0 V or STRT_UP_IOUT_LIM = 0
Circuit Breaker Offset	V_{CBOS}	0.6	0.88	1.12	mV	Circuit breaker trip voltage, V_{CB} = $V_{SENSECL}$ − V_{CBOS}
SEVERE OVERCURRENT						
Voltage Threshold	$V_{SENSEOC}$					
A Grade and AA Grade		23	25	27	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (125%)
		28	30	32	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (150%)
		38	40	42	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (200%)
		43	45	47	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; default at power-up (225%)
B Grade Only		20	25	30	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (125%)
		25	30	35	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (150%)
		35	40	45	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; optional select PMBus (200%)
		40	45	50	mV	V_{ISET} > 1.65 V; V_{PSET} > 1.1 V; default at power-up (225%)
Short Glitch Filter Duration		100		220	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC_MAX}$)
Long Glitch Filter Duration (Default)		530		900	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC_MAX}$)
Response Time						
Short Glitch Filter		200		320	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC_MAX}$)
Long Glitch Filter		630		1000	ns	V_{SENSE_HS} step = 18 mV to (2 mV above $V_{SENSEOC_MAX}$)
ISTART PIN						
Active Range		0.1		1.25	V	Tie ISTART to VCAP to disable start-up current limit
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{ISTART}			100	nA	V_{ISTART} ≤ V_{VCAP}
TIMER PIN						
TIMER Pull-Up Current						
Power-On Reset (POR)	$I_{TIMERUPPOR}$	−2	−3	−4	µA	Initial power-on reset; V_{TIMER} = 0.5 V
Overcurrent (OC) Fault	$I_{TIMERUPFLT}$	−57	−60	−63	µA	Overcurrent fault; 0.2 V ≤ V_{TIMER} ≤ 1 V

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
TIMER Pull-Down Current						
Retry	$I_{TIMERDNRT}$	1.7	2	2.3	µA	After fault when GATE is off; V_{TIMER} = 0.5 V
Hold	$I_{TIMERDNHOLD}$		100		µA	Holds TIMER at 0 V when inactive; V_{TIMER} = 0.5 V
TIMER High Threshold	V_{TIMERH}	0.98	1.0	1.02	V	
TIMER Low Threshold	V_{TIMERL}	0.18	0.2	0.22	V	
TIMER Glitch Filter	$TIMER_{GF}$		10		µs	
Minimum POR Duration			27		ms	Minimum initial insertion delay regardless of C_{TIMER} value
PSET PIN						FET power limit = $(V_{PSET} \times 8)/(50 \times R_{SENSE})$
Reference Select Threshold	$V_{PSETRSTH}$	1.35	1.5	1.65	V	If $V_{PSET} > V_{PSETRSTH}$, constant power is disabled
Gain of Current Sense Amplifier	AV_{CSAMP}		50		V/V	Accuracies included in total sense voltage accuracies
Input Current	I_{PSET}			100	nA	$V_{PSET} \le V_{VCAP}$
VOUT PIN						
Input Current				40	µA	V_{OUT} = 20 V
$\overline{\text{FAULT}}$ PIN						
Output Low Voltage	V_{OL_LATCH}			0.4	V	I_{FAULT} = 1 mA
				1.5	V	I_{FAULT} = 5 mA
Leakage Current				100	nA	$V_{FAULT} \le 2$ V; $\overline{\text{FAULT}}$ output high-Z
				1	µA	V_{FAULT} = 20 V; $\overline{\text{FAULT}}$ output high-Z
ENABLE PIN						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Glitch Filter			1		µs	
$\overline{\text{RETRY}}$ PIN						
Input High Voltage	V_{IH}	1.1			V	Latch off when high; internal pull-up sets this as default
Input Low Voltage	V_{IL}			0.8	V	10 second automatic retry when pin pulled low
Glitch Filter			1		µs	
Internal Pull-Up Current			8		µA	
CSOUT PIN						
CSOUT Gain			350		V/V	CSOUT = $V_{SENSE_HS} \times 350$; VCC > CSOUT + 2 V
Total Output Error		−1.6		+1.6	%	V_{SENSE_HS} = 20 mV; $I_{CSOUT} \le 1$ mA; C_{CSOUT} = 1 nF
		−3.0		+3.0	%	V_{SENSE_HS} = 10 mV; $I_{CSOUT} \le 1$ mA; C_{CSOUT} = 1 nF
Output Swing to GND			40		mV	
Current Limiting			5		mA	CSOUT short-circuit current
GPO1/$\overline{\text{ALERT1}}$/CONV PIN						
Output Low Voltage	V_{OL_GPO1}			0.4	V	I_{GPO1} = 1 mA
				1.5	V	I_{GPO1} = 5 mA
Leakage Current				100	nA	$V_{GPO1} \le 2$ V; GPO1 output high-Z
				1	µA	V_{GPO1} = 20 V; GPO1 output high-Z
Input High Voltage	V_{IH}	1.1			V	Configured as CONV
Input Low Voltage	V_{IL}			0.8	V	Configured as CONV
Glitch Filter			1		µs	Configured as CONV
GPO2/$\overline{\text{ALERT2}}$ PIN						
Output Low Voltage	V_{OL_GPO2}			0.4	V	I_{GPO2} = 1 mA
				1.5	V	I_{GPO2} = 5 mA
Leakage Current				100	nA	$V_{GPO2} \le 2$ V; GPO2 output high-Z
				1	µA	V_{GPO2} = 20 V; GPO2 output high-Z
PWRGD PIN						
Output Low Voltage	V_{OL_PWRGD}			0.4	V	I_{PWRGD} = 1 mA
				1.5	V	I_{PWRGD} = 5 mA
VCC That Guarantees Valid Output		1			V	I_{SINK} = 100 µA; V_{OL_PWRGD} = 0.4 V
Leakage Current				100	nA	$V_{PWRGD} \le 2$ V; PWRGD output high-Z
				1	µA	V_{PWRGD} = 20 V; PWRGD output high-Z

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
PWGIN PIN						
Input Current	I_{PWGIN}			50	nA	PWGIN ≤ 3.6 V
PWGIN Threshold	$PWGIN_{TH}$					
A Grade and AA Grade		0.99	1.0	1.01	V	PWGIN falling
B Grade Only		0.97	1.0	1.03	V	PWGIN falling
PWGIN Threshold Hysteresis	$PWGIN_{HYST}$	50	60	70	mV	
Glitch Filter			1		µs	Asserting and deasserting of PWRGD pin
CURRENT AND VOLTAGE MONITORING						See Table 3 for power monitor accuracy specifications
ADC Conversion Time						Includes time for power multiplication
			144	165	µs	One sample of I_{OUT}; from command received to valid data in register
			64	73	µs	One sample of V_{IN}; from command received to valid data in register
			64	73	µs	One sample of V_{OUT}; from command received to valid data in register
ADRx PINS						
Address Set to 00		0		0.8	V	Connect to GND
Input Current for Address Set to 00		−40	−22		µA	V_{ADRx} = 0 V to 0.8 V
Address Set to 01		135	150	165	kΩ	Resistor to GND
Address Set to 10		−1		+1	µA	No connect state; maximum leakage current allowed
Address Set to 11		2			V	Connect to VCAP
Input Current for Address Set to 11			3	10	µA	V_{ADRx} = 2.0 V to VCAP; must not exceed the maximum allowable current draw from VCAP
TEMP PIN						External transistor is 2N3904
Operating Range		−55		+150	°C	Limited by external diode
Accuracy			±1	±10	°C	$T_A = T_{DIODE}$ = −40°C to +85°C
Resolution			0.25		°C	LSB size
Output Current Source[2]						
Low Level			5		µA	
Medium Level			30		µA	
High Level			105		µA	
Maximum Series Resistance for External Diode[2]	R_S			100	Ω	For <±0.5°C additional error, C_P = 0 F
Maximum Parallel Capacitance for External Diode[2]	C_P			1	nF	R_S = 0 Ω
SPI DIGITAL INPUTS ($\overline{SPI_SS}$, MCLK, MDAT)						Compatible with SPI Mode 0; MDAT is the output data pin; output is high impedance when not transmitting
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Leakage Current				1	µA	
Data Rate				1	MHz	
SERIAL BUS DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}	1.1			V	
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 4 mA
Input Leakage	$I_{LEAK-PIN}$	−10		+10	µA	
		−5		+5	µA	Device is not powered

Parameter[1]	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Nominal Bus Voltage	V_{DD}	2.7		5.5	V	3 V to 5 V ± 10%
Capacitance for SDA, SCL Pins	C_{PIN}		5		pF	
Input Glitch Filter	t_{SP}	0		50	ns	

[1] Dual function pin names are referenced by the relevant function only (see the Pin Configurations and Function Descriptions section for full pin mnemonics and descriptions).
[2] Sampled during initial release to ensure compliance, but not subject to production testing.

POWER MONITORING ACCURACY SPECIFICATIONS

Table 3.

	AA Grade			A Grade			B Grade				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
CURRENT AND VOLTAGE MONITORING											
Current Sense Absolute Error											V_{CC} = 4.5 V to 15 V; V_{MO+} = 2 V to 15 V, 128-sample averaging (unless otherwise noted)
			±0.25			±0.7			±1.0	%	V_{SENSE_MO} = 25 mV
		±0.04	±0.3		±0.04	±0.7			±1.0	%	V_{SENSE_MO} = 20 mV
			±0.5			±1.0			±1.5	%	V_{SENSE_MO} = 20 mV; 16-sample averaging
			±1.5			±2.8			±4.0	%	V_{SENSE_MO} = 20 mV; one-sample averaging
			±0.3			±0.8			±1.1	%	V_{SENSE_MO} = 15 mV
			±0.4			±1.1			±1.5	%	V_{SENSE_MO} = 10 mV
			±0.75			±2.0			±3.0	%	V_{SENSE_MO} = 5 mV
			±1.6			±4.3			±6.2	%	V_{SENSE_MO} = 2.5 mV
HS+/VOUT Absolute Error			±0.35			±1.0			±1.5	%	V_{HS+}, V_{OUT} = 10 V to 20 V
			±0.5			±1.0			±1.5	%	V_{HS+}, V_{OUT} = 5 V
Power Absolute Error			±0.65			±1.7			±2.5	%	V_{SENSE_MO} = 20 mV, V_{HS+} = 12 V

SERIAL BUS TIMING CHARACTERISTICS

Table 4.

Parameter	Description	Min	Typ	Max	Unit
f_{SCLK}	Clock frequency			400	kHz
t_{BUF}	Bus free time	1.3			µs
$t_{HD;STA}$	Start hold time	0.6			µs
$t_{SU;STA}$	Start setup time	0.6			µs
$t_{SU;STO}$	Stop setup time	0.6			µs
$t_{HD;DAT}$	SDA hold time	300		900	ns
$t_{SU;DAT}$	SDA setup time	100			ns
t_{LOW}	SCL low time	1.3			µs
t_{HIGH}	SCL high time	0.6			µs
t_R[1]	SCL, SDA rise time	20		300	ns
t_F[1]	SCL, SDA fall time	20		300	ns

[1] $t_R = (V_{IL(MAX)} - 0.15)$ to $(V_{IH3V3} + 0.15)$ and $t_F = 0.9\ V_{DD}$ to $(V_{IL(MAX)} - 0.15)$; where V_{IH3V3} = 2.1 V, and V_{DD} = 3.3 V. V_{IH3V3} is the input high voltage when V_{DD} = 3.3 V.

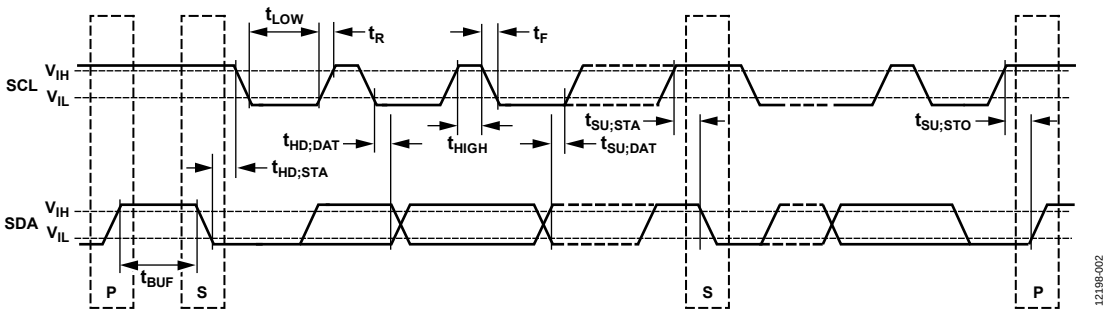


Figure 2. Serial Bus Timing Diagram

SPI TIMING CHARACTERISTICS (ADM1278-2)

Table 5.

Parameter	Description	Min	Typ	Max	Unit	Test Conditions/Comments
t_S[1]	$\overline{\text{SPI_SS}}$ falling edge to MCLK rising edge setup time	50			ns	
t_{HIGH}[1]	MCLK high time	180			ns	
t_{LOW}[1]	MCLK low time	180			ns	
t_{CLK}[1]	MCLK cycle time	1			µs	
t_H[1]	Hold time between $\overline{\text{SPI_SS}}$ and MCLK	1			µs	
t_V	Hold time between new data valid and MCLK falling edge	110		260	ns	Track capacitance = 120 pF; I_{OL} = 4 mA
t_{ON}	$\overline{\text{SPI_SS}}$ falling edge to MDAT active time	130		240	ns	Track capacitance = 120 pF; I_{OL} = 4 mA
t_{OFF}	Bus relinquish time after $\overline{\text{SPI_SS}}$ rising edge	130		280	ns	Track capacitance = 120 pF; I_{OL} = 4 mA

[1] Guaranteed by design, but not production tested.

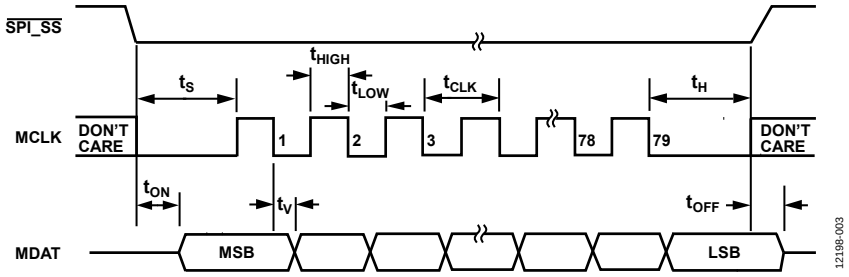


Figure 3. SPI Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
VCC Pin	−0.3 V to +25 V
UV Pin	−0.3 V to +4 V
OV Pin	−0.3 V to +4 V
ISTART Pin	−0.3 V to +4 V
TIMER Pin	−0.3 V to VCAP + 0.3 V
TEMP Pin	−0.3 V to VCAP + 0.3 V
VCAP Pin	−0.3 V to +4 V
ISET Pin	−0.3 V to +4 V
PSET Pin	−0.3 V to +4 V
$\overline{\text{FAULT}}$ Pin	−0.3 V to +25 V
$\overline{\text{RETRY}}$ Pin	−0.3 V to +4 V
PWGIN Pin	−0.3 V to +4 V
SCL Pin	−0.3 V to +6.5 V
SDA Pin	−0.3 V to +6.5 V
$\overline{\text{SPI_SS}}$ Pin	−0.3 V to +4 V
MCLK Pin	−0.3 V to +4 V
MDAT Pin	−0.3 V to +4 V
ADR1 Pin	−0.3 V to +6.5 V
ADR2 Pin	−0.3 V to +6.5 V
ENABLE Pin	−0.3 V to +25 V
GPO1/$\overline{\text{ALERT1}}$/CONV Pin	−0.3 V to +25 V
GPO2/$\overline{\text{ALERT2}}$ Pin	−0.3 V to +25 V
PWRGD Pin	−0.3 V to +25 V
VOUT Pin	−0.3 V to +25 V
GATE Pin (Internal Supply Only)[1]	−0.3 V to +36 V
HS+ Pin	−0.3 V to +25 V
HS− Pin	−0.3 V to +25 V
MO+ Pin	−0.3 V to +25 V
MO− Pin	−0.3 V to +25 V
PGND	±0.3 V
V_{SENSE_HS} ($V_{HS+} - V_{HS-}$)	±0.3 V
V_{SENSE_MO} ($V_{MO+} - V_{MO-}$)	±0.3 V
CSOUT Short-Circuit Duration	Indefinite
Continuous Current into Any Pin	±10 mA
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature, Soldering (10 sec)	300°C
Junction Temperature	105°C

[1] The GATE pin has internal clamping circuits to prevent the GATE pin voltage from exceeding the maximum ratings of a MOSFET with gain to source voltage, V_{GSMAX} = 20 V, and internal process limits. Applying a voltage source to this pin externally may cause irreversible damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

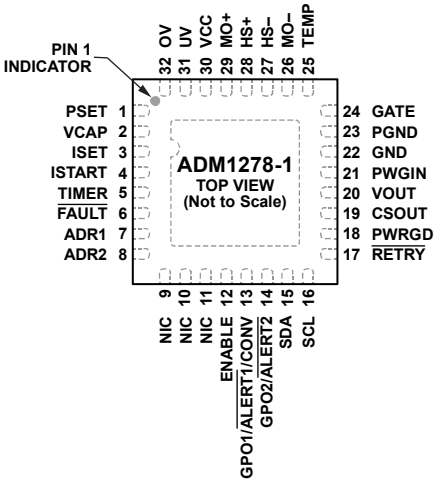
Table 7. Thermal Resistance

Package Type	θ_{JA}	Unit
CP-32-13	32.5	°C/W

ESD CAUTION

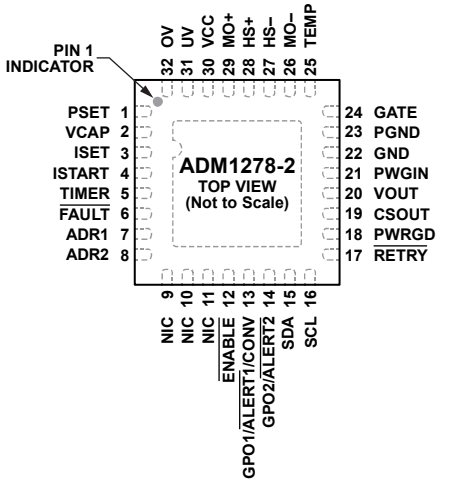
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. SOLDER THE EXPOSED PAD TO THE BOARD TO IMPROVE THERMAL DISSIPATION. THE EXPOSED PAD CAN BE CONNECTED TO GROUND.

Figure 4. ADM1278-1 Pin Configuration



NOTES
1. NIC = NOT INTERNALLY CONNECTED.
2. SOLDER THE EXPOSED PAD TO THE BOARD TO IMPROVE THERMAL DISSIPATION. THE EXPOSED PAD CAN BE CONNECTED TO GROUND.

Figure 5. ADM1278-3 Pin Configuration

Table 8. ADM1278-1 and ADM1278-3 Pin Function Descriptions

	Mnemonic		
Pin No.	**ADM1278-1**	**ADM1278-3**	**Description**
1	PSET	PSET	Power Limit. This pin allows the constant power limit to be programmed. The current limit is dynamically adjusted to ensure that the maximum power dissipation in the FET never exceeds this limit during any operating condition. The power limit can be adjusted to a user defined value using a resistor divider from VCAP. An external reference can also be used. The FET power is limited to $(V_{PSET} \times 8)/(50 \times R_{SENSE})$.
2	VCAP	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain accuracy. This pin can be used as a reference to program the ISET pin voltage.
3	ISET	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
4	ISTART	ISTART	Start-Up Current Limit. This pin allows a separate start-up current limit to be set for dv/dt power-up mode. When powering up in dv/dt mode, the current charging the capacitor is constant and is typically much smaller than the normal load current. The ISTART pin sets the start-up current limit in a similar manner as ISET is used to set the normal current limit. The start-up current limit is only active while PWRGD is low. The start-up current limit can also be set over PMBus with the STRT_UP_IOUT_LIM register. Start-up current limit = $V_{ISET} \times$ (STRT_UP_IOUT_LIM/16). The lowest of all the active current limits always takes priority.
5	TIMER	TIMER	Timer. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
6	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches after a fault has occurred. The faults that can trigger this pin include an overcurrent fault resulting in the TIMER pin voltage exceeding the upper threshold, an overtemperature fault, and an FET health fault. This is an open-drain output pin.
7, 8	ADR1, ADR2	ADR1, ADR2	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9, 10, 11	NIC	NIC	Not Internally Connected.

Pin No.	Mnemonic		Description
	ADM1278-1	ADM1278-3	
12	ENABLE	$\overline{\text{ENABLE}}$	Enable. On the ADM1278-1, the ENABLE pin is an active high digital input pin. This input must be high to allow the ADM1278-1 hot swap controller to begin a power-up sequence. If the ENABLE pin is held low, the ADM1278-1 is prevented from initiating a hot swap attempt. On the ADM1278-3, the $\overline{\text{ENABLE}}$ pin is an active low digital input pin. This input must be low to allow the ADM1278-3 hot swap controller to begin a power-up sequence. If the $\overline{\text{ENABLE}}$ pin is held high, the ADM1278-3 is prevented from initiating a hot swap attempt.
13	GPO1/$\overline{\text{ALERT1}}$/CONV	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$).This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. The GPO1/$\overline{\text{ALERT1}}$/CONV pin defaults to an alert output at power-up. This is an open-drain output pin.
14	GPO2/$\overline{\text{ALERT2}}$	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. The GPO2/$\overline{\text{ALERT2}}$ pin defaults to an alert output at power-up. This is an open-drain output pin.
15	SDA	SDA	Serial Data Input/Output. Open-drain input/output. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
16	SCL	SCL	Serial Clock. Open-drain input. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a pull-up resistor to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
17	$\overline{\text{RETRY}}$	$\overline{\text{RETRY}}$	Retry. The $\overline{\text{RETRY}}$ pin has an internal pull-up resistor; therefore, it can be left floating to enable the default latch off mode after an overcurrent fault. This pin can be pulled low to enable a 10 second autoretry following an overcurrent fault.
18	PWRGD	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults have been detected, and the ADM1278-1 hot swap is enabled with the gate fully enhanced. This is an open-drain output pin.
19	CSOUT	CSOUT	Current Sense Output. The V_{SENSE_HS} voltage is amplified to give an output voltage corresponding to the load current.
20	VOUT	VOUT	Output Voltage. VOUT is an input pin and is used to read back the output voltage using the internal ADC. Insert a 1 kΩ resistor in series between the source of a FET and the VOUT pin. This pin is also used along with HS− to calculate the drain to source voltage (V_{DS}) of the FET for constant power foldback operation.
21	PWGIN	PWGIN	Power-Good Input. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted high until the output voltage is above the threshold set by this pin.
22	GND	GND	Ground. This pin is the ground connection for all of the sensitive analog nodes. Take care to isolate this ground connection from the main high current path and any large transients. A good technique for this is to create a ground island around the ADM1278-1 device and the supporting small signal components. Connect this ground island to the main ground plane at a single point as close to the ADM1278-1 GND pin as possible. See the ADM1278 evaluation board (EVAL-ADM1278EBZ) as an example.
23	PGND	PGND	Power Ground. This pin is the ground return path for the strong gate pull-down current. It is also the ground return for the external transistor used for temperature measurements.
24	GATE	GATE	Gate Output. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below the undervoltage lockout threshold (UVLO).
25	TEMP	TEMP	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to the TEMP pin to report temperature. The voltage at the TEMP pin is measured by the internal ADC.

Pin No.	Mnemonic		Description
	ADM1278-1	ADM1278-3	
26	MO−	MO−	Negative Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
27	HS−	HS−	Negative Current Sense Input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-1 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$).
28	HS+	HS+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-1 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$). This pin is also used to measure the supply input voltage using the ADC.
29	MO+	MO+	Positive Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
30	VCC	VCC	Positive Supply Input. A UVLO circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, it is recommended that this pin be greater than or equal to HS+ and MO+ to ensure that specifications are adhered to. No sequencing is required.
31	UV	UV	Undervoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is below the UV limit.
32	OV	OV	Overvoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
	EPAD	EPAD	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to ground.

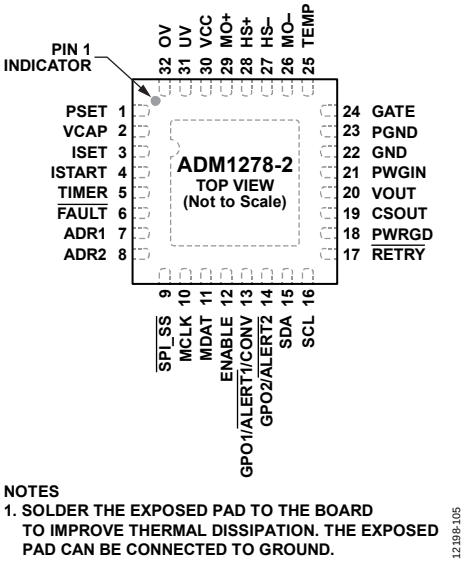


Figure 6. ADM1278-2 Pin Configuration

Table 9. ADM1278-2 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PSET	Power Limit. This pin allows the constant power limit to be programmed. The current limit is dynamically adjusted to ensure that the maximum power dissipation in the FET never exceeds this limit during any operating condition. The power limit can be adjusted to a user defined value using a resistor divider from VCAP. An external reference can also be used. The FET power is limited to $(V_{PSET} \times 8)/(50 \times R_{SENSE})$.
2	VCAP	Internal Regulated Supply. Place a capacitor with a value of 1 µF or greater on this pin to maintain accuracy. This pin can be used as a reference to program the ISET pin voltage.
3	ISET	Current Limit. This pin allows the current-limit threshold to be programmed. The default limit is set when this pin is connected directly to VCAP. To achieve a user defined sense voltage, the current limit can be adjusted using a resistor divider from VCAP. An external reference can also be used.
4	ISTART	Start-Up Current Limit. This pin allows a separate start-up current limit to be set for dv/dt power-up mode. When powering up in dv/dt mode, the current charging the capacitor is constant and is typically much smaller than the normal load current. The ISTART pin sets the start-up current limit in a similar manner as ISET is used to set the normal current limit. The start-up current limit is only active while PWRGD is low. The start-up current limit can also be set over PMBus with the STRT_UP_IOUT_LIM register. Start-up current limit = $V_{ISET} \times$ (STRT_UP_IOUT_LIM/16). The lowest of all the active current limits always takes priority.
5	TIMER	Timer. An external capacitor, C_{TIMER}, sets an initial timing cycle delay and a fault delay. The GATE pin is pulled low when the voltage on the TIMER pin exceeds the upper threshold.
6	$\overline{\text{FAULT}}$	Fault. This pin asserts low and latches after a fault has occurred. The faults that can trigger this pin include an overcurrent fault resulting in the TIMER pin voltage exceeding the upper threshold, an overtemperature fault, and an FET health fault. This is an open-drain output pin.
7, 8	ADR1, ADR2	PMBus Address. These pins can be tied to GND, tied to VCAP, left floating, or tied low through a resistor for a total of 16 unique PMBus device addresses (see the Device Addressing section).
9	$\overline{\text{SPI_SS}}$	Slave Select. When pulled low, this pin begins to transfer data on the MDAT line.
10	MCLK	Master Clock. The MCLK signal outputs data on the MDAT line. This pin is clocked by an external device.
11	MDAT	Master Data Output. Open-drain output. Requires an external pull-up resistor. The MDAT pin is an output only pin and can be used to stream data from the ADC. There is a fixed format for the current, voltage, and temperature data, and no header information is required. This pin is high impedance when not transmitting data.
12	ENABLE	Enable. This pin is an active high digital input pin. This input must be high to allow the ADM1278-2 hot swap controller to begin a power-up sequence. If this pin is held low, the ADM1278-2 is prevented from initiating a hot swap attempt.

Pin No.	Mnemonic	Description
13	GPO1/$\overline{\text{ALERT1}}$/CONV	General-Purpose Digital Output (GPO1). Alert ($\overline{\text{ALERT1}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. Conversion (CONV). This pin can be used as an input signal to control when a power monitor ADC sampling cycle begins. The GPO1/$\overline{\text{ALERT1}}$/CONV pin defaults to an alert output at power-up. This is an open-drain output pin.
14	GPO2/$\overline{\text{ALERT2}}$	General-Purpose Digital Output (GPO2). Alert ($\overline{\text{ALERT2}}$). This pin can be configured to generate an alert signal when one or more fault or warning conditions are detected. The GPO2/$\overline{\text{ALERT2}}$ pin defaults to an alert output at power-up. This is an open-drain output pin.
15	SDA	Serial Data Input/Output. Open-drain input/output. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
16	SCL	Serial Clock. Open-drain input. Requires an external pull-up resistor. If the I^2C pins, SDA and SCL, are not used, tie them to GND or via a resistor pull-up to VCAP or another supply. This avoids any glitches on the I^2C pins being interpreted as I^2C transactions.
17	$\overline{\text{RETRY}}$	Retry. The $\overline{\text{RETRY}}$ pin has an internal pull-up resistor; therefore, it can be left floating to enable the default latch off mode after an overcurrent fault. This pin can be pulled low to enable a 10 second autoretry following an overcurrent fault.
18	PWRGD	Power-Good Signal. This pin indicates that the supply is within tolerance (PWGIN input), no faults have been detected, and the ADM1278-2 hot swap is enabled with the gate fully enhanced. This is an open drain output pin.
19	CSOUT	Current Sense Output. The V_{SENSE_HS} voltage is amplified to give an output voltage corresponding to the load current.
20	VOUT	Output Voltage. VOUT is an input pin and is used to read back the output voltage using the internal ADC. Insert a 1 kΩ resistor in series between the source of a FET and the VOUT pin. This pin is also used along with HS− to calculate the drain to source voltage (V_{DS}) of the FET for constant power foldback operation.
21	PWGIN	Power-Good Input. This pin sets the power-good input threshold. The user can set an accurate power-good threshold with a resistor divider from the source of the FET (VOUT). The PWRGD output signal is not asserted high until the output voltage is above the threshold set by this pin.
22	GND	Ground. This pin is the ground connection for all of the sensitive analog nodes. Take care to isolate this ground connection from the main high current path and any large transients. A good technique for this is to create a ground island around the ADM1278-2 device and the supporting small signal components. Connect this ground island to the main ground plane at a single point as close to the ADM1278-2 GND pin as possible. See the ADM1278 evaluation board (EVAL-ADM1278EBZ) as an example.
23	PGND	Power Ground. This is the ground return path for the strong gate pull-down current. It is also the ground return for the external transistor used for temperature measurements.
24	GATE	Gate Output. This pin is the high-side gate drive of an external N-channel FET. This pin is driven by the FET drive controller, which uses a charge pump to provide a pull-up current to charge the FET gate pin. The FET drive controller regulates to a maximum load current by regulating the GATE pin. GATE is held low when the supply is below the UVLO threshold.
25	TEMP	Temperature Input. An external NPN device can be placed close to the MOSFETs and connected back to the TEMP pin to report temperature. The voltage at the TEMP pin is measured by the internal ADC.
26	MO−	Negative Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.
27	HS−	Negative Current Sense Input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-2 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$).
28	HS+	Positive Current Sense Input. This pin connects to the main supply input. A sense resistor between the HS+ pin and the HS− pin sets the analog current limit. The hot swap operation of the ADM1278-2 controls the external FET gate to maintain the sense voltage ($V_{HS+} - V_{HS-}$). This pin is also used to measure the supply input voltage using the ADC.
29	MO+	Positive Power Monitor Input. A sense resistor between the MO+ pin and the MO− pin sets the sense voltage that is used by the ADC internally to measure load current. Extra filtering can be added between the MO+ and MO− pins if required.

Pin No.	Mnemonic	Description
30	VCC	Positive Supply Input. A UVLO circuit resets the device when a low supply voltage is detected. GATE is held low when the supply is below UVLO. During normal operation, it is recommended that this pin be greater than or equal to HS+ and MO+ to ensure that specifications are adhered to. No sequencing is required.
31	UV	Undervoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is below the UV limit.
32	OV	Overvoltage Input. An external resistor divider is configured from the input supply to this pin to allow an internal comparator to detect whether the supply is above the OV limit.
	EPAD	Exposed Pad. Solder the exposed pad to the board to improve thermal dissipation. The exposed pad can be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

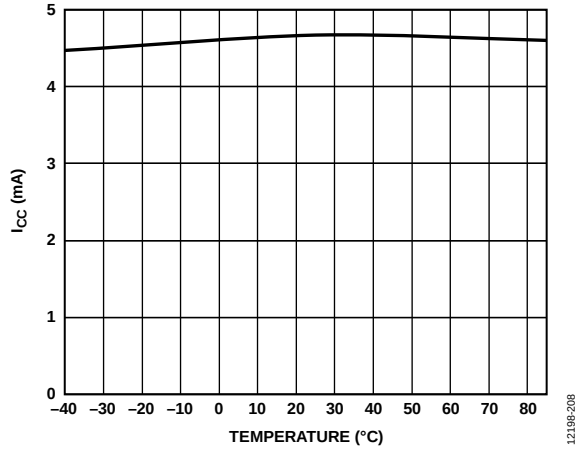


Figure 7. Supply Current (I_{CC}) vs. Temperature

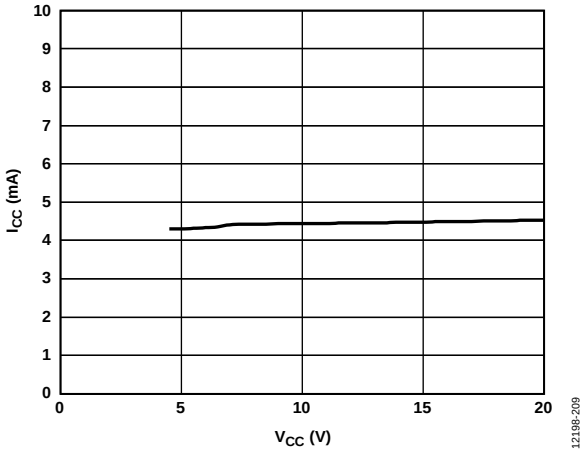


Figure 8. Supply Current (I_{CC}) vs. V_{CC}

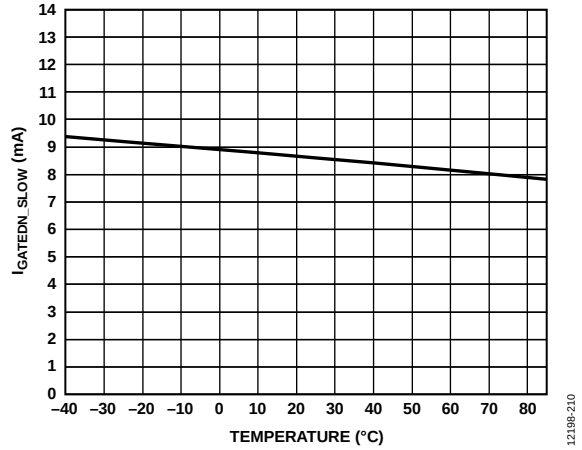


Figure 9. GATE Pull-Down Current (I_{GATEDN_SLOW}) vs. Temperature

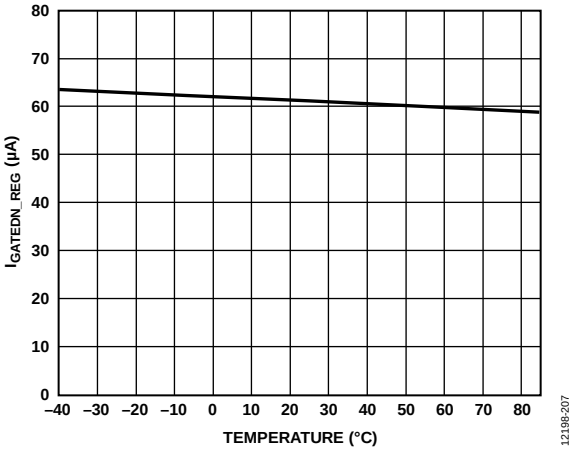


Figure 10. GATE Pull-Down Current (I_{GATEDN_REG}) vs. Temperature

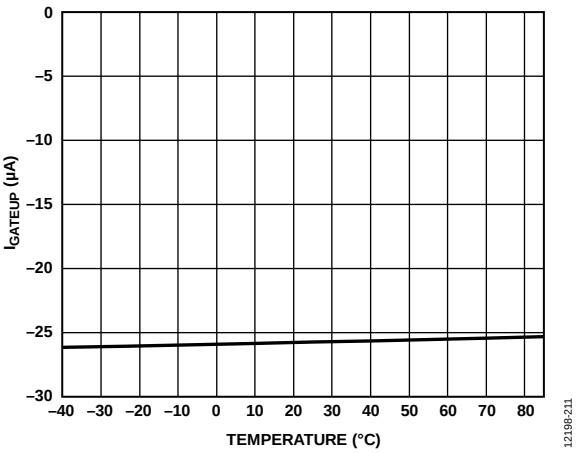


Figure 11. GATE Pull-Up Current (I_{GATEUP}) vs. Temperature

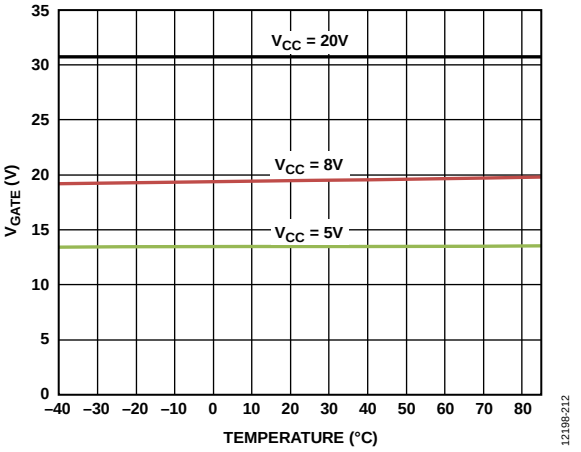


Figure 12. V_{GATE} (5 µA Load) vs. Temperature

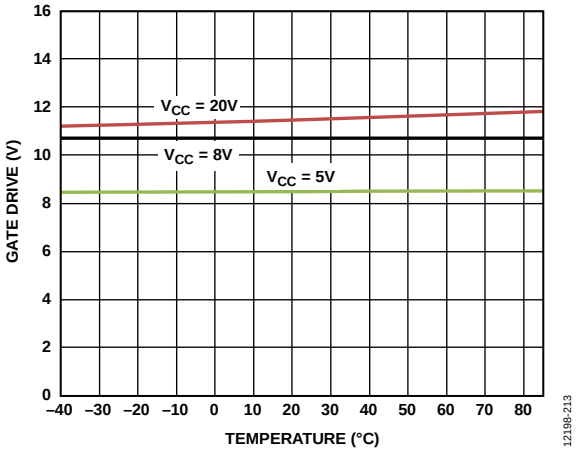


Figure 13. GATE Drive (5 µA Load) vs. Temperature

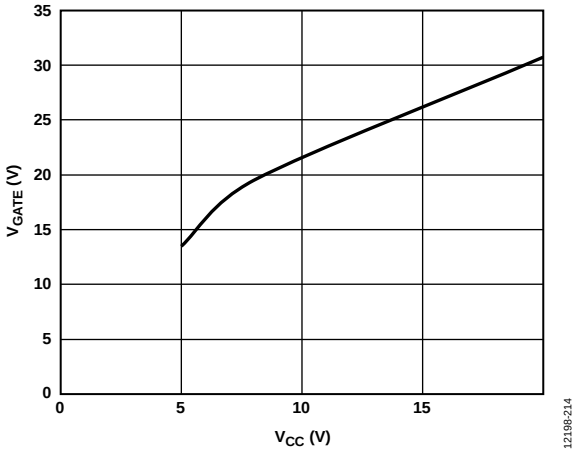


Figure 14. V_{GATE} (5 µA Load) vs. V_{CC}

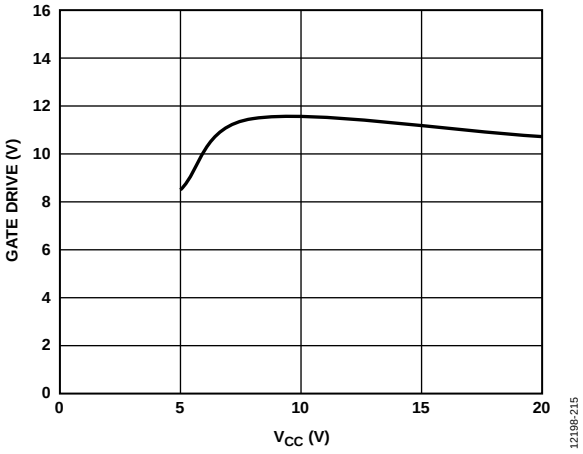


Figure 15. GATE Drive vs. V_{CC}

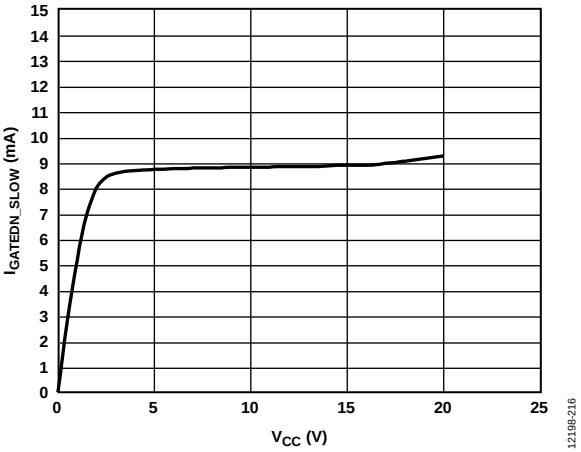


Figure 16. I_{GATEDN_SLOW} vs. V_{CC}

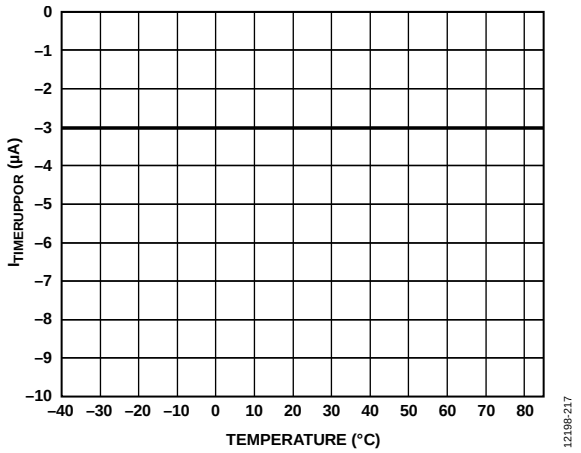


Figure 17. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. Temperature

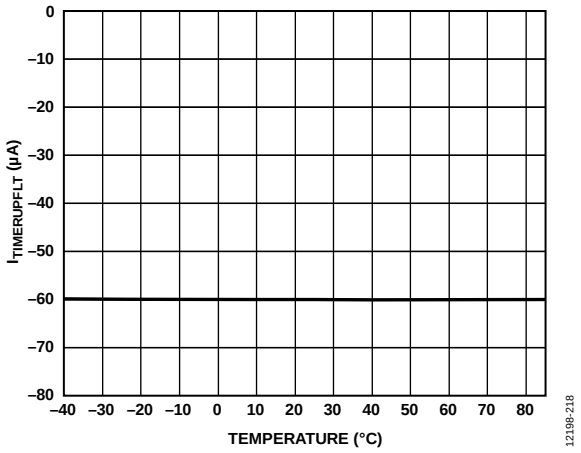


Figure 18. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. Temperature

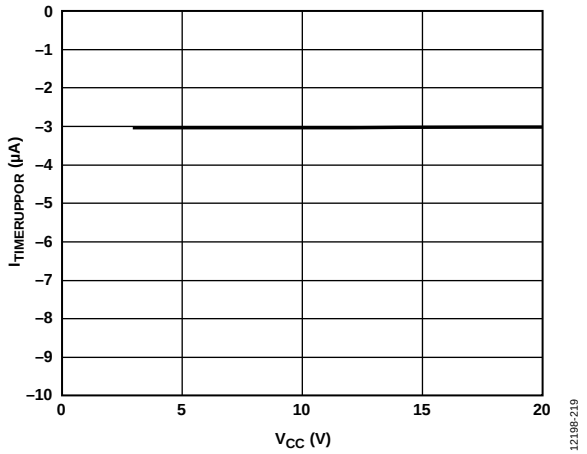


Figure 19. TIMER Pull-Up Current POR ($I_{TIMERUPPOR}$) vs. V_{CC}

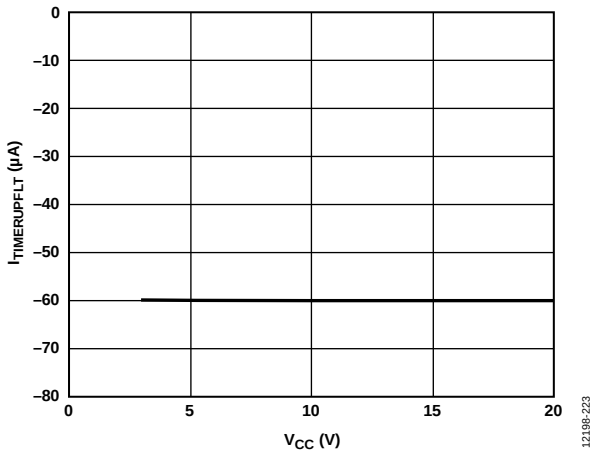


Figure 20. TIMER Pull-Up Current OC Fault ($I_{TIMERUPFLT}$) vs. V_{CC}

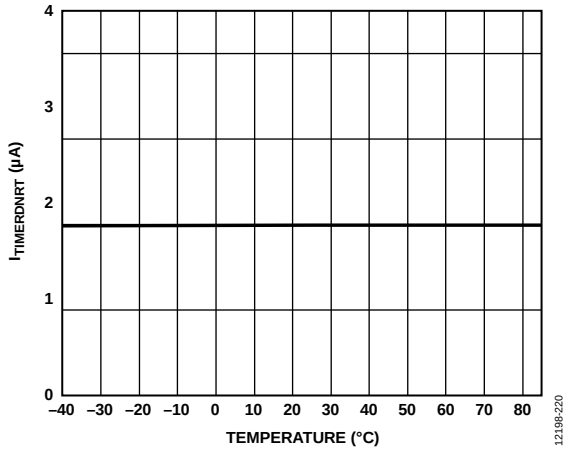


Figure 21. TIMER Pull-Down Current Retry ($I_{TIMERDNRT}$) vs. Temperature

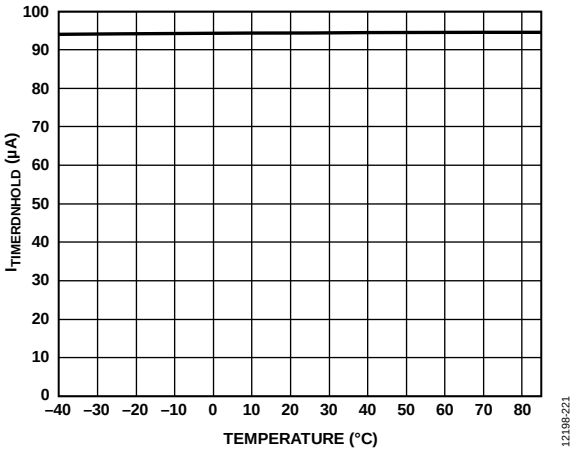


Figure 22. TIMER Pull-Down Current Hold ($I_{TIMERDNHOLD}$) vs. Temperature

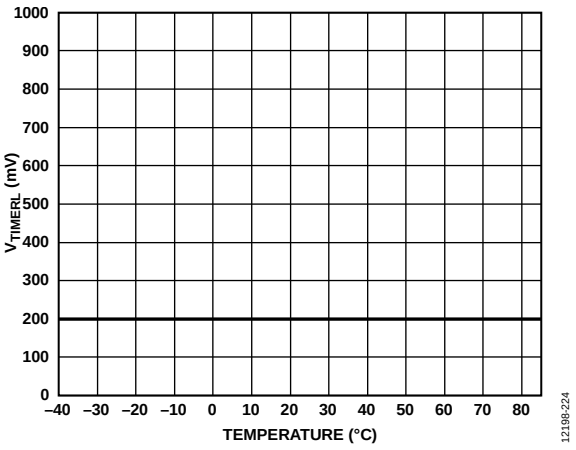


Figure 23. TIMER Low Threshold (V_{TIMERL}) vs. Temperature

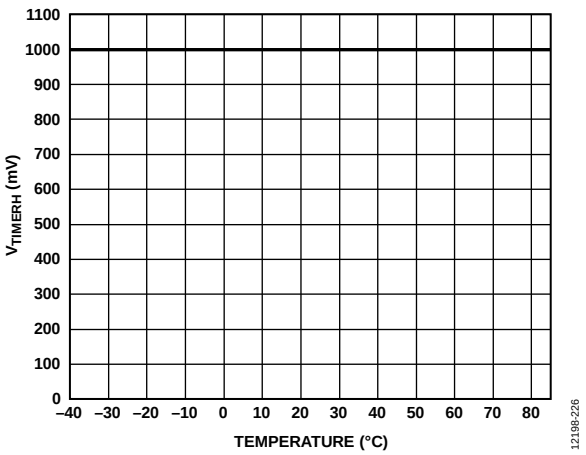


Figure 24. TIMER High Threshold (V_{TIMERH}) vs. Temperature

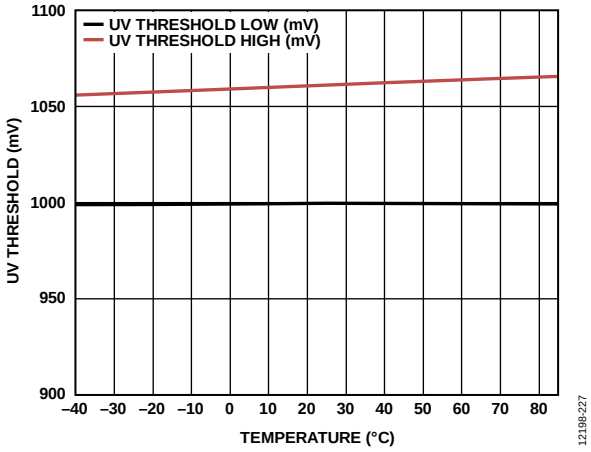


Figure 25. UV Threshold vs. Temperature

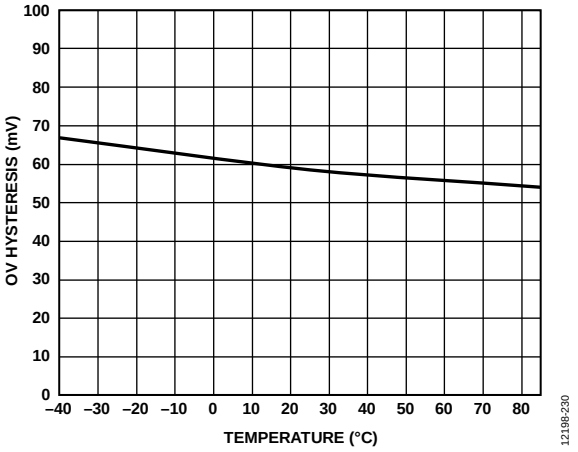


Figure 28. OV Hysteresis vs. Temperature

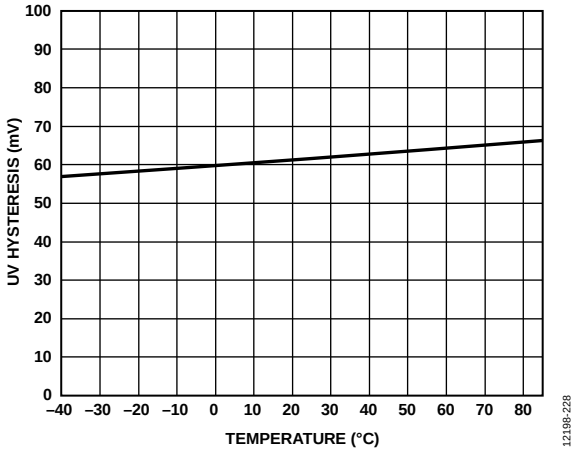


Figure 26. UV Hysteresis vs. Temperature

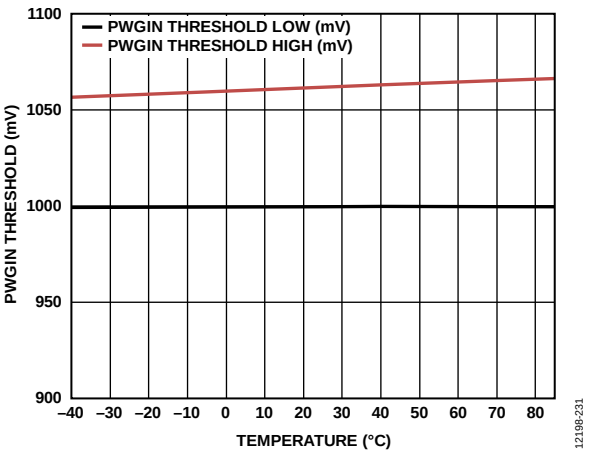


Figure 29. PWGIN Threshold vs. Temperature

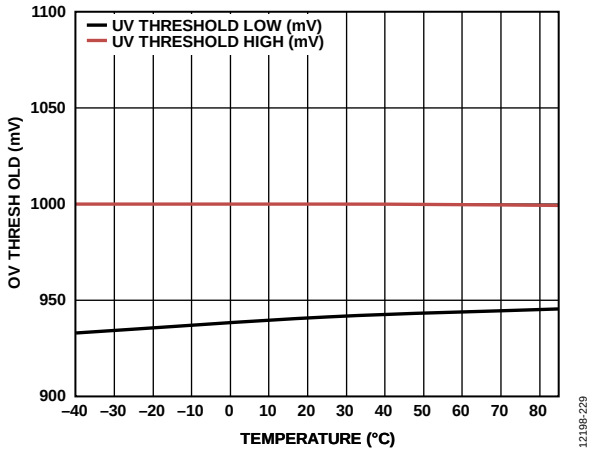


Figure 27. OV Threshold vs. Temperature

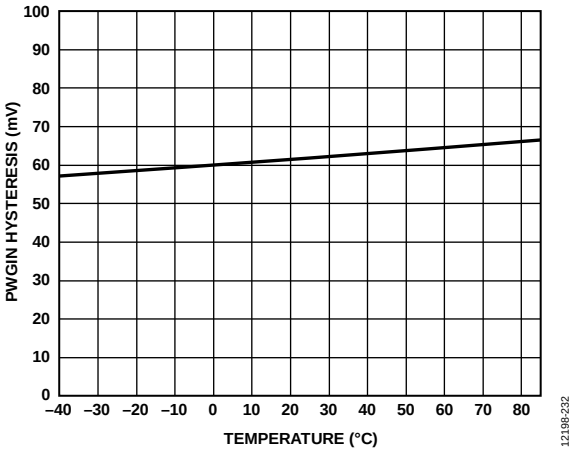


Figure 30. PGIN Hysteresis vs. Temperature

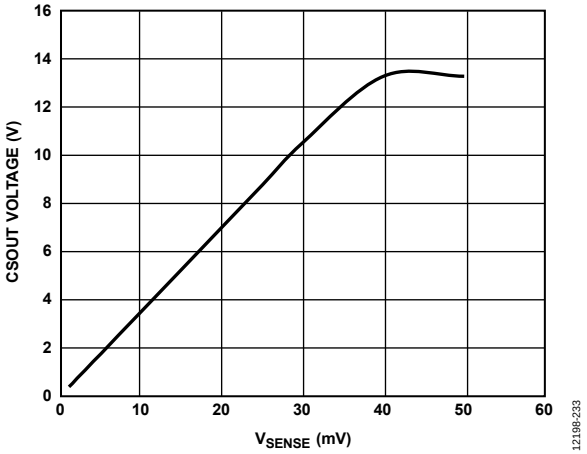


Figure 31. CSOUT Voltage vs. V_{SENSE}

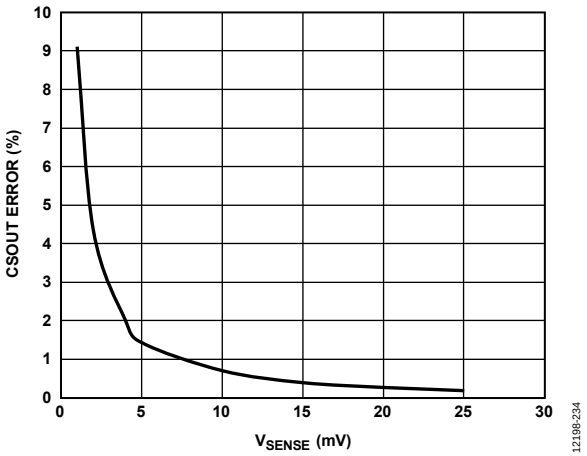


Figure 32. CSOUT Error vs. V_{SENSE}

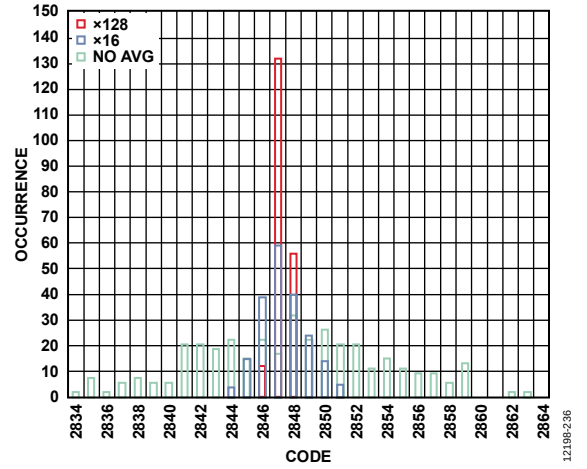


Figure 33. ADC Code Histogram (V_{SENSE} = 10 mV, 200 Measurements)

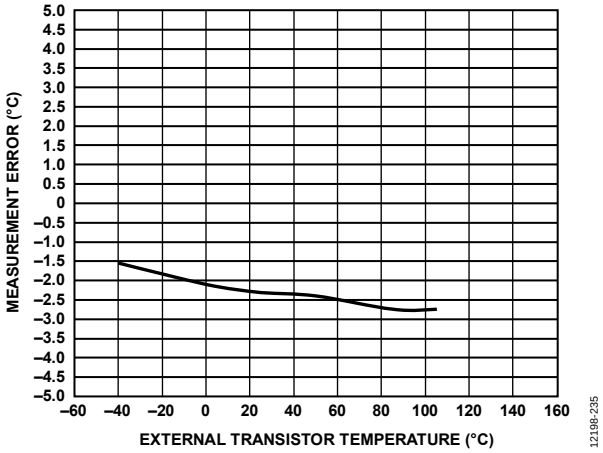


Figure 34. Measurement Error vs. External Transistor Temperature

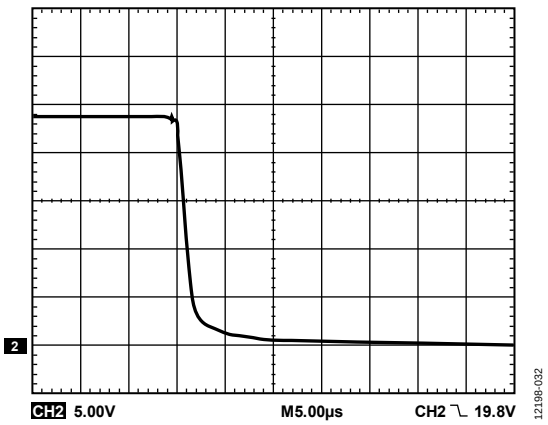


Figure 35. VGATE Response to Severe Overcurrent Event (GATE Fast Pull-Down)

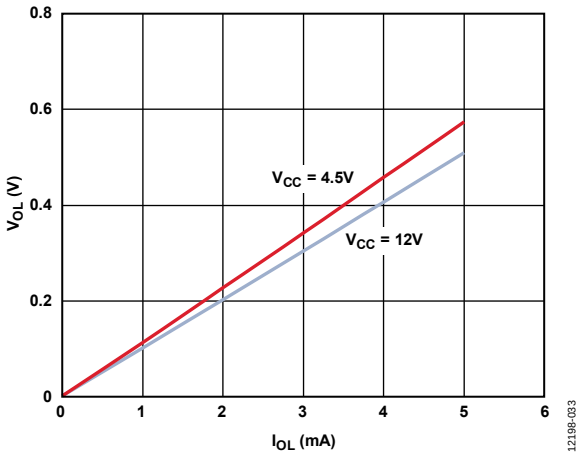


Figure 36. PWGD Pin, V_{OL} vs. I_{OL}

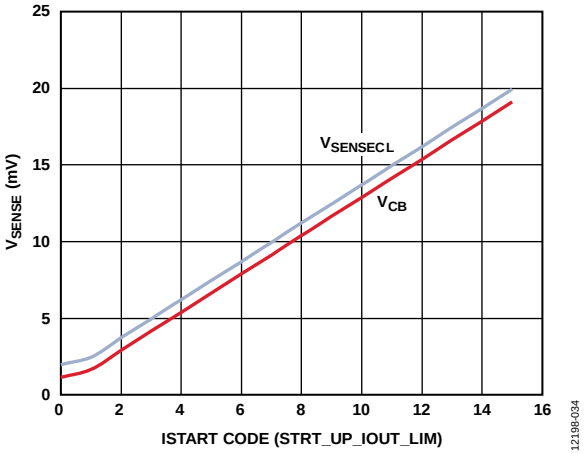


Figure 37. V_{SENSE} vs. ISTART Code (STRT_UP_IOUT_LIM)

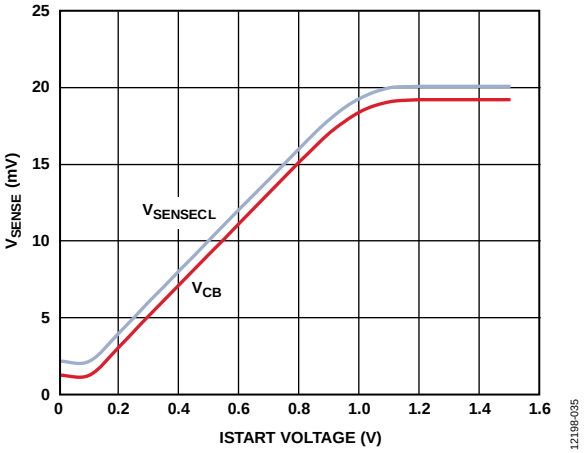


Figure 38. V_{SENSE} vs. ISTART Voltage

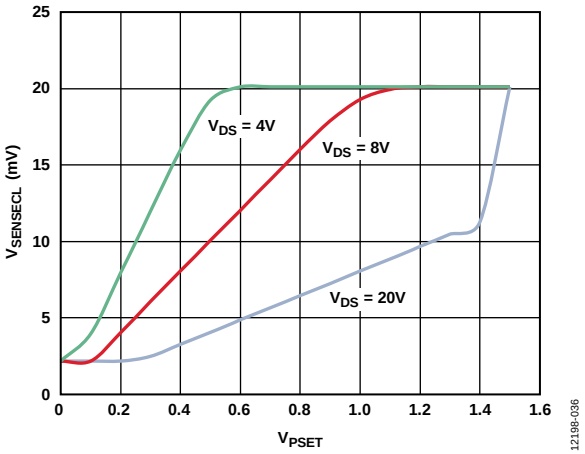


Figure 39. $V_{SENSECL}$ vs. V_{PSET}

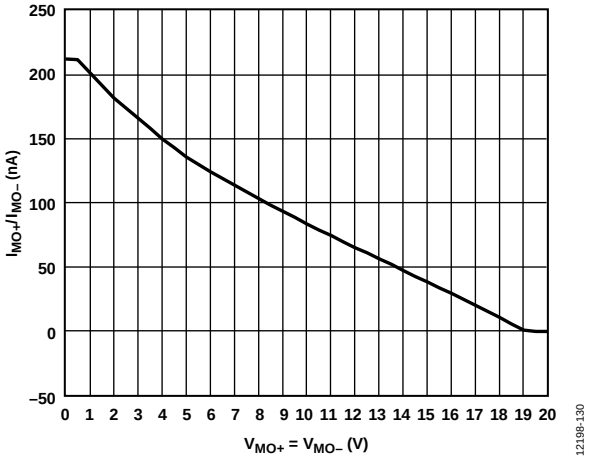


Figure 40. I_{MO+}/I_{MO-} vs. V_{MO+}/V_{MO-} with V_{CC} = 20 V

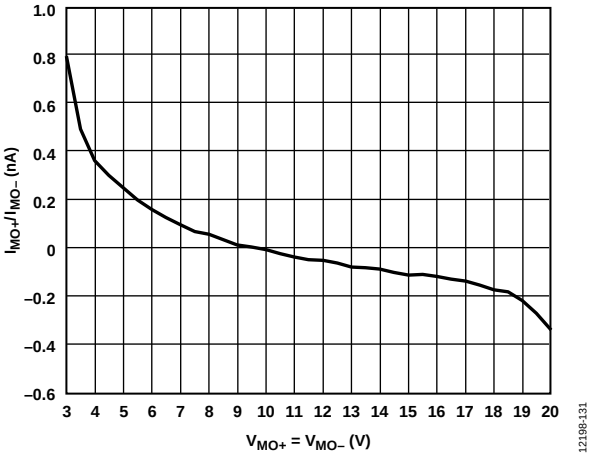


Figure 41. I_{MO+}/I_{MO-} vs. V_{MO+}/V_{MO-} with $V_{CC} = V_{MO+} = V_{MO-}$

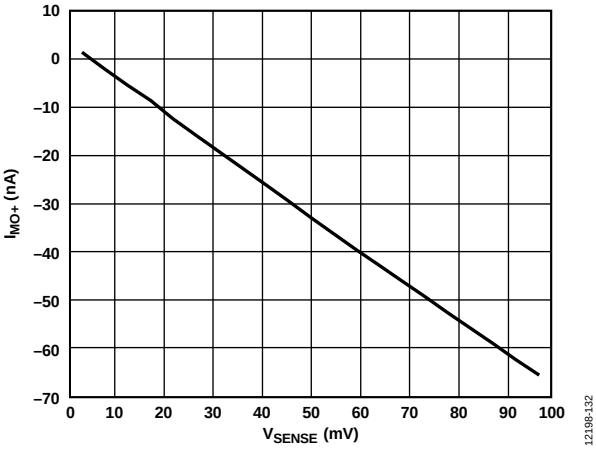


Figure 42. I_{MO+} vs. V_{SENSE} with $V_{CC} = V_{MO+}$ = 20 V

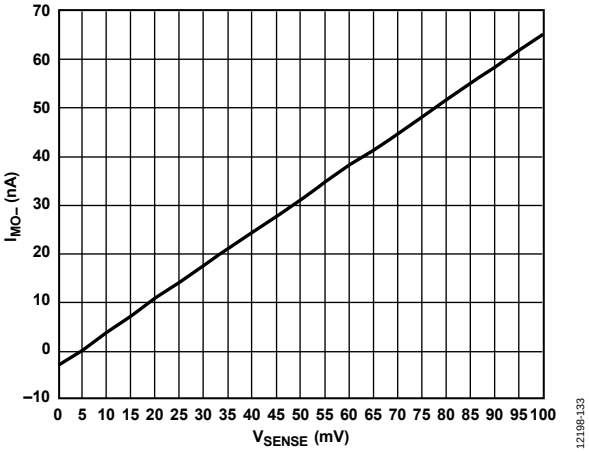


Figure 43. I_{MO-} vs. V_{SENSE} with $V_{CC} = V_{MO+} = 20$ V

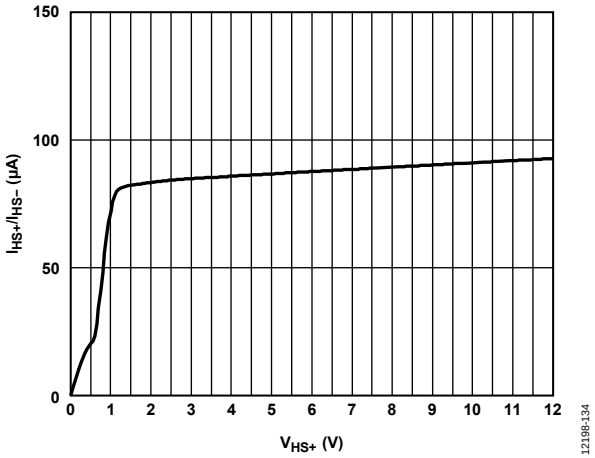


Figure 44. I_{HS+}/I_{HS-} vs. V_{HS+}

THEORY OF OPERATION

When circuit boards are inserted into a live backplane, discharged supply bypass capacitors draw large transient currents from the backplane power bus as they charge. These transient currents can cause permanent damage to connector pins, as well as dips on the backplane supply that can reset other boards in the system.

The ADM1278 is designed to control the powering on and off of a system in a controlled manner, allowing a board to be removed from, or inserted into, a live backplane by protecting it from excess currents. The ADM1278 can reside on the backplane or on the removable board.

POWERING THE ADM1278

A supply voltage from 4.5 V to 20 V is required to power the ADM1278 via the VCC pin. The VCC pin provides the majority of the bias current for the device; the remainder of the current needed to control the gate drive and to best regulate the V_{GS} voltage is supplied by the HS+ pin.

To ensure correct operation of the ADM1278, the voltage on the VCC pin must be greater than or equal to the voltage on the HS+ and MO+ pins. No sequencing of the VCC and HS+ rails is necessary. The HS+ pin can be as low as 2 V for normal operation, provided that a voltage of at least 4.5 V is connected to the VCC pin. In most applications, both the VCC and HS+ pins are connected to the same voltage rail, but they are connected via separate traces to prevent accuracy loss in the sense voltage measurement (see Figure 45).

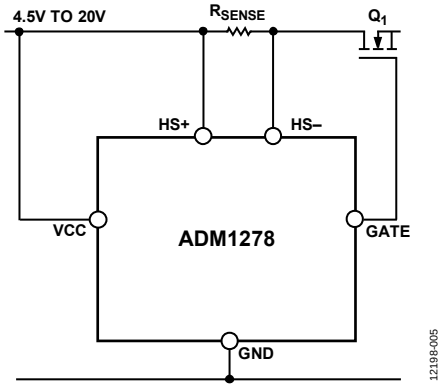


Figure 45. Powering the ADM1278

To protect the ADM1278 from unnecessary resets due to transient supply glitches, an external resistor and capacitor can be added, as shown in Figure 46. Choose the values of these components such that a time constant is provided that can filter any expected glitches. However, use a resistor that is small enough to keep voltage drops caused by quiescent current to a minimum. Unless a resistor is used to limit the inrush current, do not place a supply decoupling capacitor on the rail before the FET.

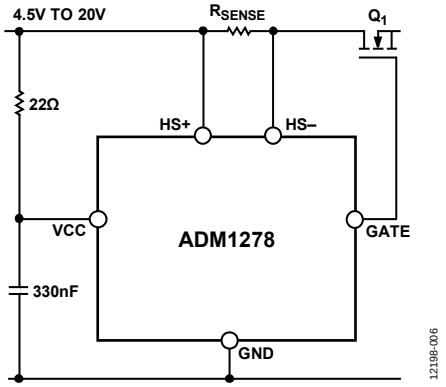


Figure 46. Transient Glitch Protection Using an RC Network

HOT SWAP CURRENT SENSE INPUTS

The load current is monitored by measuring the voltage drop across an external sense resistor, R_{SENSE} (see Figure 47). An internal current sense amplifier provides a gain of 50 to the voltage drop detected across R_{SENSE}. The result is compared to an internal reference and used by the hot swap control logic to detect when an overcurrent condition occurs.

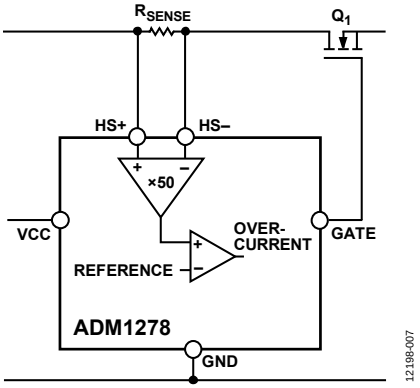


Figure 47. Hot Swap Current Sense Amplifier

The HS± inputs can be connected to multiple parallel sense resistors, which can affect the voltage drop detected by the ADM1278. The current flowing through the sense resistors creates an offset, resulting in reduced accuracy.

To achieve better accuracy, averaging resistors can be used to sum the current from the nodes of each sense resistor, as shown in Figure 48. A typical value for the averaging resistors is 10 Ω. The input current to each sense pin is matched to within 5 µA. This ensures that the same offset is observed by both sense inputs.

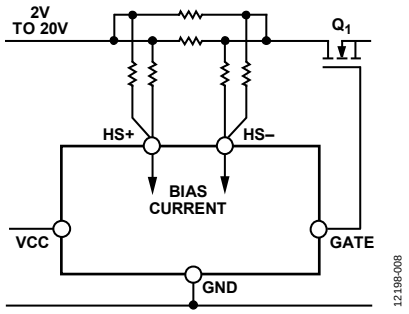


Figure 48. Connection of Multiple Sense Resistors to the HS± Pins

POWER MONITOR CURRENT SENSE INPUTS

The internal ADC uses separate current sense input pins for measuring the load current from those used by the hot swap circuitry. This allows additional filtering on the power monitor pins without affecting the response time of the hot swap to an overcurrent event.

The same external sense resistor, R_{SENSE}, is used for hot swap control and ADC measurements. If additional external filtering is not required, the HS± and MO± pins can be tied together, close to the device under test, as shown in Figure 49.

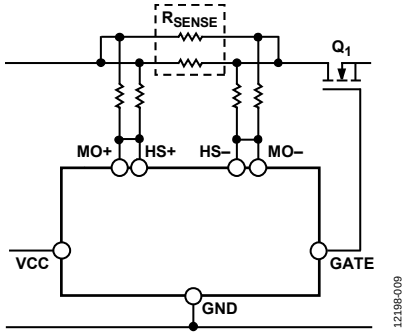


Figure 49. Power Monitor, No External Filtering

If additional antialiasing filtering is required, filtering components can be added, as shown in Figure 50, without affecting the hot swap performance.

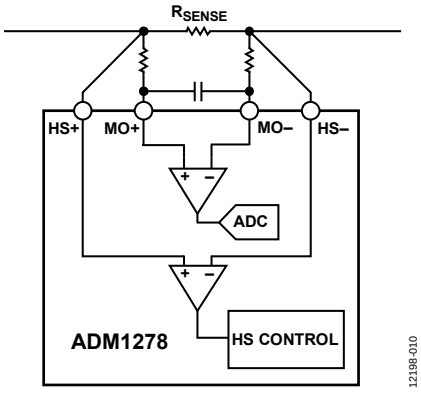


Figure 50. Power Monitor Current Sense Filtering

CURRENT-LIMIT REFERENCE

The current-limit reference voltage determines the load current level to which the ADM1278 limits the current during an overcurrent event. This reference voltage is compared to the amplified current sense voltage to determine whether the limit is reached.

An internal current-limit reference selector block continuously compares the ISET and PSET voltages to determine which voltage reference is the lowest at any given time; the lowest voltage is used as the current-limit reference. The ISTART pin is also monitored while PWRGD is inactive. This ensures that the programmed current limit, ISET, is used in normal operation, and that the start-up current limit and foldback features reduce the current limit when required during startup and/or fault conditions.

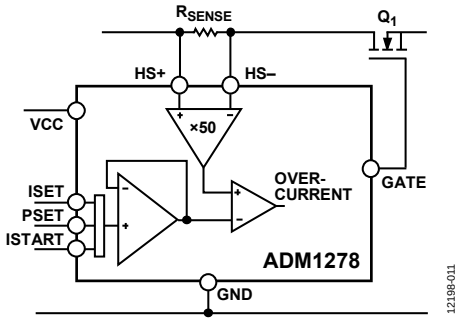


Figure 51. Current-Limit Reference Selection

The foldback and start-up current-limit voltage inputs to the internal comparator are clamped to minimum levels of 100 mV (that is, $V_{SENSECL}$ = 2 mV) to prevent zero current flow caused by the current limit being too low. Figure 52 provides an example of how the ISTART, PSET, and ISET voltages interact during startup as the ADM1278 is enhancing the FET and charging the output load capacitance.

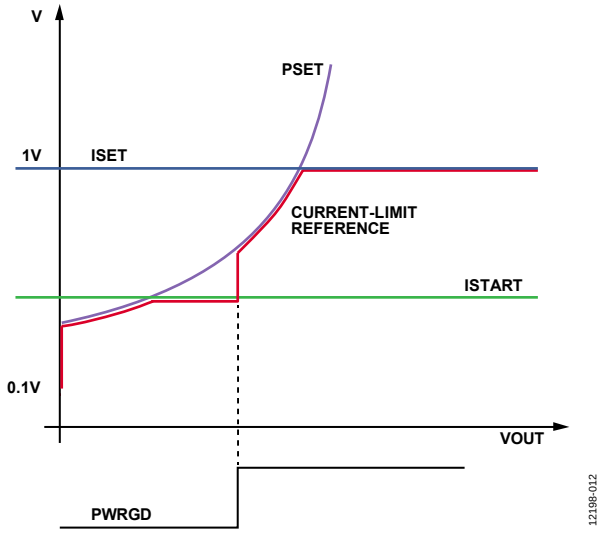


Figure 52. Interaction of ISTART, PSET, and ISET Current Limits

SETTING THE CURRENT LIMIT (ISET)

The maximum current limit is partially determined by selecting a sense resistor to match the current sense voltage limit on the controller for the desired load current. However, as currents become larger, the sense resistor requirements become smaller, and resolution can be difficult to achieve when selecting the appropriate sense resistor. The ADM1278 provides an adjustable current sense voltage limit to manage this issue. The device allows the user to program the required current sense voltage limit from 5 mV to 25 mV.

The default value of 20 mV is achieved by connecting the ISET pin directly to the VCAP pin. This connection configures the device to use an internal 1 V reference, which equates to 20 mV at the sense inputs (see Figure 53).

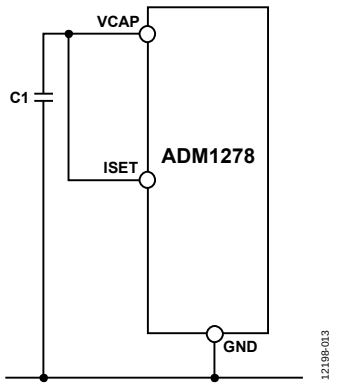


Figure 53. Fixed 20 mV Current Sense Limit

To program the sense voltage from 5 mV to 25 mV, a resistor divider is used to set a reference voltage on the ISET pin (see Figure 54).

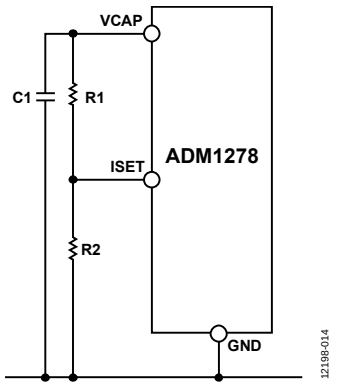


Figure 54. Adjustable 5 mV to 25 mV Current Sense Limit

The VCAP pin has a 2.7 V internal generated voltage that can be used to set a voltage at the ISET pin. Assuming that V_{ISET} equals the voltage on the ISET pin, size the resistor divider to set the ISET voltage as follows:

$$V_{ISET} = V_{SENSECL} \times 50$$

where $V_{SENSECL}$ is the current sense voltage limit.

The VCAP rail can also be used as the pull-up supply for the resistor divider on the PSET and ISTART pins and for setting the I^2C address. Do not use the VCAP pin for any other purpose. To guarantee accuracy specifications, do not load the VCAP pin by more than 100 µA.

SETTING A LINEAR OUTPUT VOLTAGE RAMP AT POWER-UP

The ADM1278 standard method of power-up in a server application is to configure a single linear voltage ramp on the output, which allows a constant inrush current into the load capacitance. This method has the advantage of setting very low inrush currents where required by a combination of large output capacitance and FET SOA limitations.

The object of such a design is to allow a linear monotonic power-up event without the restrictions of the system fault timer. To achieve this, a power-up ramp is set such that the inrush is low enough not to reach the active circuit breaker current limit. This allows the power-up to continue without the timer running. When using this method, ensure that the power in the MOSFET during this event meets the SOA requirements. An extra component, C_{GATE}, is required on the GATE pin as shown in Figure 55.

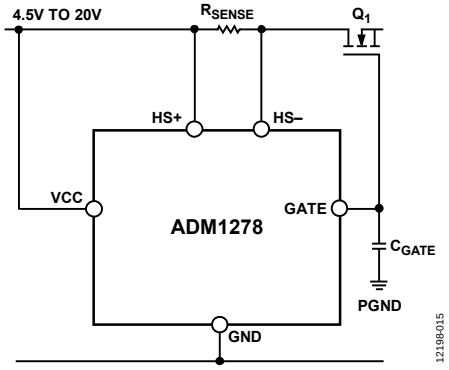


Figure 55. DV/DT Power-Up Configuration

To ensure that the inrush current does not approach or exceed the active current-limit level, the output voltage ramp can be set by selecting the appropriate value for C_{GD} as follows:

$$C_{GATE} = (I_{GATEUP}/I_{INRUSH}) \times C_{LOAD}$$

where I_{GATEUP} is the gate pull-up current specified.

Add margin and tolerance as necessary to ensure a robust design. Subtract any parasitic C_{GD} of the MOSFETs from the total to determine the additional external capacitance required.

Next, the power-up ramp time can be approximated by

$$t_{RAMP} = (V_{IN} \times C_{LOAD})/I_{INRUSH} = (V_{IN} \times C_{GATE})/I_{GATEUP}$$

Check the SOA of the MOSFET for conditions and the duration of this power-up ramp. TIMER regulation period can be minimized to provide a simple fault filtering solution.

The diagram in Figure 56 shows a typical hot swap power-up with a gate capacitor configured for a linear output voltage ramp.

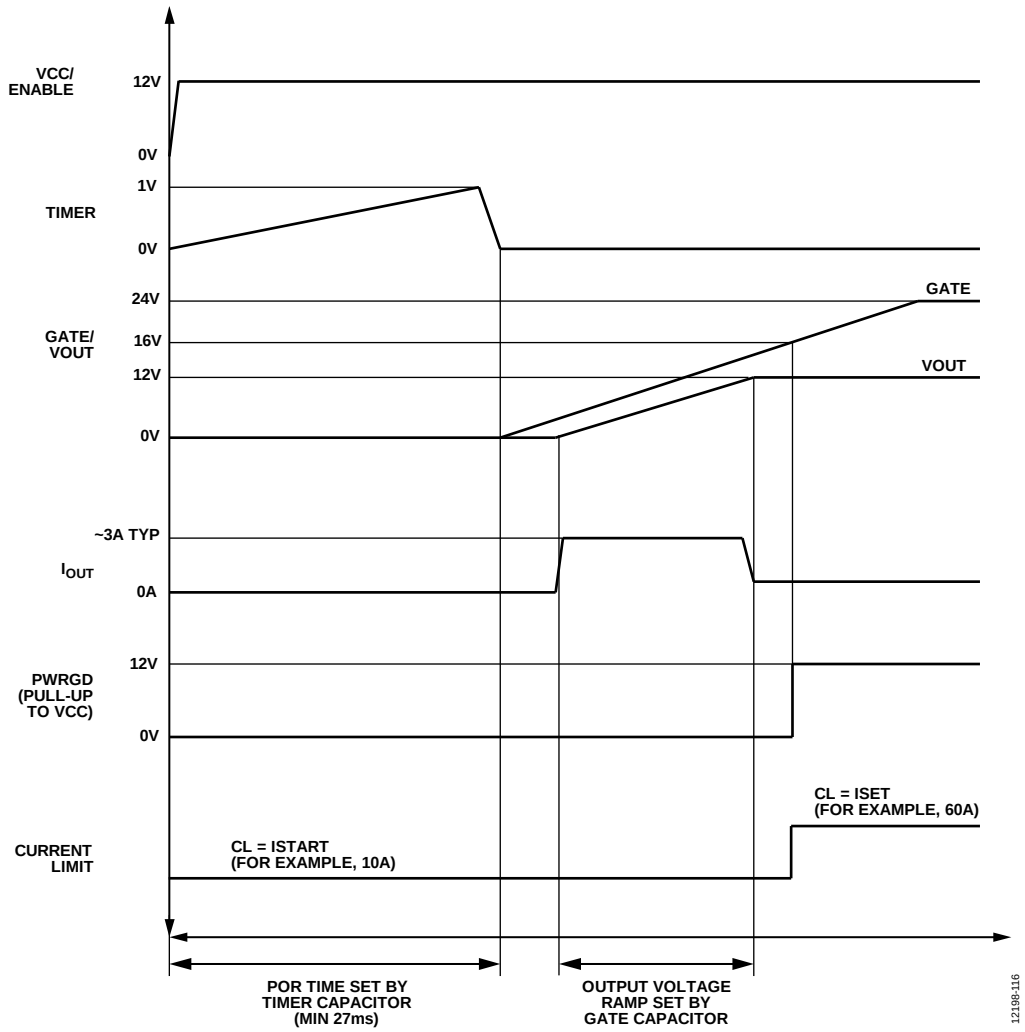


Figure 56. Linear Voltage Ramp Power-Up

START-UP CURRENT LIMIT

When powering up in dv/dt mode, the inrush current is typically configured to be in the order of <5 A. The other active current limits (PSET and ISET) may be much higher than this. The start-up current limit is intended as an extra level of protection during this initial power-up stage. It helps catch a resistive type fault that causes the inrush to be higher than expected.

The start-up current limit is only active during power-up. It is enabled while PWRGD is deasserted and is disabled when PWRGD is asserted.

The start-up current limit can be programmed via the ISTART pin or via the PMBus register, STRT_UP_IOUT_LIM (Register 0xF6). If both are configured, the lowest current limit is selected as the active current limit. The clamp level in both cases is a 2 mV V_{SENSE} current limit.

When configuring with the ISTART pin, the current limit is

$$Startup_CL = \frac{V_{ISTART}}{50 \times R_{SENSE}}$$

More importantly, the circuit breaker level can be calculated using the following equation:

$$Startup_CB = \frac{\left(\frac{V_{ISTART}}{50} - 0.88\ \text{mV}\right)}{R_{SENSE}}$$

To prevent the start-up current limit from being triggered during a normal dv/dt power-up, set the circuit breaker level above the maximum expected inrush current.

The ISTART pin can be tied to VCAP to disable the start-up current limit. The start-up current limit PMBus register is set to the maximum by default; therefore, it is effectively disabled by default.

If configuring the start-up current limit with the PMBus register, the start-up current limit is set as a fraction of the ISET current limit. There are four register bits so that the start-up current limit can be set from 1/16th to 16/16th of the normal current limit. The effective ISTART voltage can be calculated as

$$V_{ISTART} = V_{ISET} \times \left(\frac{(STRT_UP_IOUT_LIM) + 1}{16}\right)$$

The start-up circuit breaker and current limits can then be calculated from this effective ISTART voltage.

CONSTANT POWER FOLDBACK

Foldback is a method that actively reduces the current limit as the voltage drop across the FET increases. It keeps the power across the FET below the programmed value during power-up, overcurrent, or short-circuit events. This allows a smaller FET to be used, resulting in board size savings and cost savings. The foldback method used is a constant power foldback scheme, meaning power in the FET is held constant, regardless of the V_{DS} of the FET. This simplifies the task of ensuring that the FET is always operating within the SOA limits.

The ADM1278 detects the V_{DS} voltage drop across the FET by sensing the HS+ and VOUT pins. The foldback current limit dynamically changes as the V_{DS} voltage changes to maintain a constant power level in the MOSFET. For example, as V_{OUT} drops, the current-limit reference follows V_{PSET} after it becomes the lowest voltage input to the current-limit reference selector block. This results in a reduction of the current limit and, therefore, the regulated load current. To prevent complete current flow restriction, a clamp becomes active when the current-limit reference reaches 100 mV. The current limit cannot drop below this level.

The maximum FET power level is configured with a resistor divider on the PSET pin

$$FET\ Power\ Limit = \frac{(V_{PSET} \times 8)}{(50 \times R_{SENSE})}$$

Therefore, after determining the desired FET power limit and R_{SENSE} values, the required PSET voltage can be calculated. Set this voltage with a resistor divider from the VCAP pin.

TIMER

The TIMER pin handles several timing functions with an external capacitor, C_{TIMER}. The two comparator thresholds are V_{TIMERL} (0.2 V) and V_{TIMERH} (1 V). There are four timing current sources: a 3 µA pull-up, a 60 µA pull-up, a 2 µA pull-down, and a 100 µA pull-down.

These current and voltage levels, together with the value of C_{TIMER} chosen by the user, determine the initial timing cycle time and the fault regulation time. The TIMER pin capacitor value is determined using the following equation:

$$C_{TIMER} = (t_{ON} \times 60\ \mu A)/V_{TIMERH}$$

where t_{ON} is the time that the FET is allowed to spend in regulation at the set current limit.

The choice of FET is based on matching this time with the SOA requirements of the FET. Foldback can be used to simplify the selection.

When VCC is connected to the backplane supply, the internal supply of the ADM1278 must be charged up. In a very short time, the internal supply is fully charged up and, because the UVLO voltage is exceeded at VCC, the device emerges from reset. During this first short reset period, the GATE and TIMER pins are both held low.

The ADM1278 then goes through an initial timing cycle. The TIMER pin is pulled high with 3 µA. When the TIMER pin reaches the V_{TIMERH} threshold (1.0 V), the first portion of the initial timing cycle is complete. The initial timing cycle is a minimum of approximately 27 ms to allow FET health checks to be completed. If the initial TIMER cycle is set shorter than 27 ms by the TIMER capacitor, the TIMER pin continues to be pulled up to the VCAP voltage level until the 27 ms has expired. The 100 µA current source then pulls down the TIMER pin until it reaches V_{TIMERL} (0.2 V). The initial timing cycle duration is related to C_{TIMER} by the following equation:

$$t_{INITIAL} = \frac{V_{TIMERH} \times C_{TIMER}}{3\ \mu A} + \frac{(V_{TIMERH} - V_{TIMERL}) \times C_{TIMER}}{100\ \mu A}$$

where $t_{INITIAL} \geq 27$ ms, regardless of C_{TIMER} value.

For example, a 100 nF capacitor results in an initial insertion delay of approximately 34 ms. If the UV and OV inputs indicate that the supply is within the defined window of operation when the initial timing cycle terminates, the device is ready to start a hot swap operation.

When the voltage across the sense resistor reaches the circuit breaker trip voltage, V_{CB}, the 60 µA TIMER pull-up current is activated, and the gate begins to regulate the current at the current limit. This initiates a ramp-up on the TIMER pin. If the sense voltage falls below this circuit breaker trip voltage before the TIMER pin reaches V_{TIMERH}, the 60 µA pull-up is disabled and the 2 µA pull-down is enabled.

The circuit breaker trip voltage is not the same as the hot swap sense voltage current limit. There is a small circuit breaker offset, V_{CBOS}, which means that the TIMER pin actually starts ramping a short time before the current reaches the defined current limit.

However, if the overcurrent condition is continuous and the sense voltage remains above the circuit breaker trip voltage, the 60 µA pull-up current remains active and the FET remains in regulation.

This allows the TIMER pin to reach V_{TIMERH} and to initiate the GATE shutdown. On the ADM1278, the $\overline{\text{FAULT}}$ pin is pulled low immediately and PWRGD is deasserted.

In latch-off mode, the TIMER pin is switched to the 2 µA pull-down current when it reaches the V_{TIMERH} threshold. While the TIMER pin is being pulled down, the hot swap controller remains off and cannot be turned back on.

When the voltage on the TIMER pin goes below the V_{TIMERL} threshold, the hot swap controller can be reenabled by toggling the UV pin or by using the PMBus OPERATION command to toggle the on bit from on to off and then on again.

HOT SWAP RETRY

The $\overline{\text{RETRY}}$ pin is used to configure latch-off or autoretry mode. The $\overline{\text{RETRY}}$ pin has an internal pull-up current; therefore, it can be left floating to enable latch-off mode after an overcurrent fault. The $\overline{\text{RETRY}}$ pin can be pulled low to enable a 10 second autoretry following an overcurrent fault.

FET GATE DRIVE CLAMPS

The charge pump used on the GATE pin is capable of driving the pin to V_{CC} + (2 × V_{CC}), but it is clamped to less than 14 V above the HS± pins and less than 31 V. These clamps ensure that the maximum V_{GS} rating of the FET is not exceeded.

FAST RESPONSE TO SEVERE OVERCURRENT

The ADM1278 features a separate high bandwidth current sense amplifier that detects a severe overcurrent that is indicative of a short-circuit condition. A fast response time allows the ADM1278 to handle events of this type that may otherwise cause catastrophic damage if not detected and acted on very quickly. The fast response circuit ensures that the ADM1278 can detect an overcurrent event at approximately 125% to 225% of the normal current limit (ISET) and can respond to and control the current within 1 µs, in most cases.

There are four severe overcurrent threshold options and two severe overcurrent glitch filter options selectable via the PMBus registers.

UNDERVOLTAGE AND OVERVOLTAGE

The ADM1278 monitors the supply voltage for undervoltage (UV) and overvoltage (OV) conditions. The UV and OV pins are connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 1 V voltage reference.

Figure 57 illustrates the voltage monitoring input connections. An external resistor network divides the supply voltage for monitoring. An undervoltage event is detected when the voltage connected to the UV pin falls below 1 V, and the gate is shut down using the 10 mA pull-down device. Similarly, when an overvoltage event occurs and the voltage on the OV pin exceeds 1 V, the gate is shut down using the 10 mA pull-down device. There is a fixed 60 mV hysteresis on the UV and OV pin thresholds.

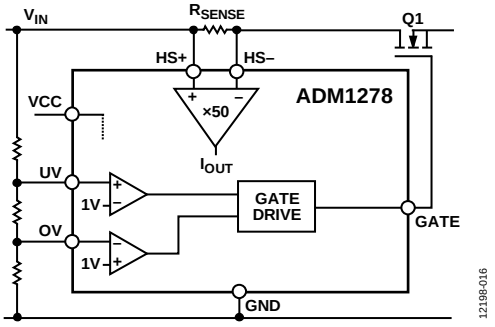


Figure 57. Undervoltage and Overvoltage Supply Monitoring

POWER GOOD

The power-good (PWRGD) output can be used to indicate whether the output voltage is above a user defined threshold and can, therefore, be considered good. A resistor divider on the PWGIN pin sets an accurate power-good threshold on the output voltage.

The PWRGD pin is an open-drain output that pulls low when the voltage at the PWGIN pin is lower than 1.0 V (power bad). When the voltage at the PWGIN pin is above this threshold plus a fixed hysteresis of 60 mV, output power is considered to be good.

However, PWRGD asserts only when the following conditions are met:

- PWGIN is above the rising threshold voltage.
- Hot swap is enabled, that is, the ENABLE pin is high ($\overline{\text{ENABLE}}$ pin is low), and UV and OV are within range.
- There is no active fault condition, that is, the $\overline{\text{FAULT}}$ pin has been cleared following any fault condition.
- The MOSFET is fully enhanced (gate voltage > VMOSFET_DRAIN + 4 V).

After all of these conditions are met, the open-drain pull-down current is disabled, allowing PWRGD to be pulled high. PWRGD is guaranteed to be in a valid state for VCC ≥ 1 V.

If the gate voltage drops below V_{MOSFET_DRAIN} + 4 V (that is, no longer meets MOSFET fully enhanced condition), PWRGD still remains asserted for 100 ms. If the condition persists for longer than 100 ms, PWRGD is deasserted and an FET health fault is signaled.

If any of the other conditions for PWRGD are no longer met, PWRGD is deasserted immediately.

$\overline{\text{FAULT}}$ PIN

The $\overline{\text{FAULT}}$ pin asserts when one of the following faults causes the hot swap to shut down:

- FET health fault
- Overcurrent fault
- Overtemperature fault

The $\overline{\text{FAULT}}$ pin is latched, and it can only be cleared by a rising edge on the ENABLE pin (falling edge on the $\overline{\text{ENABLE}}$ pin), a PMBus OPERATION on command from the off state, or a POWER_CYCLE command, assuming no faults are still active. The fault registers are not cleared by the ENABLE/$\overline{\text{ENABLE}}$ pin or the POWER_CYCLE command; they can only be cleared by a PMBus OPERATION off to on command or a CLEAR_FAULTS command.

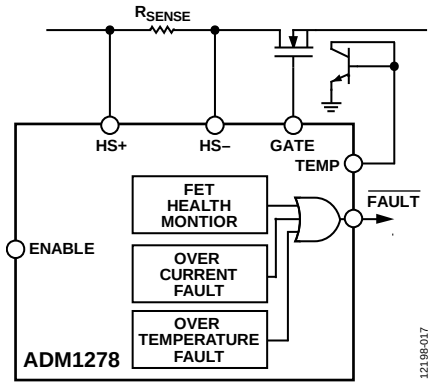


Figure 58. $\overline{FAULT}$ Pin Operation

ENABLE/$\overline{ENABLE}$ INPUT

The ADM1278 provides a dedicated ENABLE/$\overline{ENABLE}$ digital input pin. The ADM1278-1 and ADM1278-2 have an active high ENABLE pin whereas the ADM1278-3 has an active low $\overline{ENABLE}$ pin. The ENABLE/$\overline{ENABLE}$ pin allows the ADM1278 to remain off by using a hardware signal, even when the voltage on the UV pin is greater than 1.0 V and the voltage on the OV pin is less than 1.0 V. Although the UV pin can be used to provide a digital enable signal, using the ENABLE/$\overline{ENABLE}$ pin for this purpose means that the ability to monitor for undervoltage conditions is not lost.

In addition to the conditions for the UV and OV pins, the ADM1278 ENABLE/$\overline{ENABLE}$ input pin must be asserted for the device to begin a power-up sequence.

CURRENT SENSE OUTPUT (CSOUT)

The ADM1278 provides a CSOUT pin voltage output that is proportional to the V_{SENSE_HS} voltage.

$$CSOUT = V_{SENSE_HS} \times 350$$

The CSOUT voltage is an analog representation of the main system current flowing through R_{SENSE}. A resistor divider can be added to CSOUT to clamp the voltage output to any downstream devices, provided the maximum load conditions described in Table 2 are not exceeded.

The response time of the CSOUT pin to a change in V_{SENSE} voltage is very fast; therefore, it can be used when fast response time is required, for example, power throttling. The CSOUT response time to a 10 mV step in V_{SENSE} voltage is typically 10 µs.

REMOTE TEMPERATURE SENSING

The ADM1278 provides the capability to measure temperature at a remote location with a single discrete NPN or PNP transistor. The temperature measurements can be read back over the PMBus interface. Warning and fault thresholds can also be set on the temperature measurement. Exceeding a fault threshold causes the controller to turn off the pass MOSFET, deassert the PWRGD pin, and assert the $\overline{FAULT}$ pin.

The external transistor is typically placed close to the main pass MOSFETs to provide an additional level of protection. The controller can then monitor and respond to an elevated MOSFET operating temperature. It is not possible to measure temperature at more than one location on the board.

Place the transistor close to the MOSFET for best accuracy. If the transistor is placed on the opposite side of the PCB, use multiple vias to ensure the optimum transfer of heat from the MOSFET to the transistor.

Temperature Measurement Method

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode by measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. However, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from device to device.

The technique used in the ADM1278 is to measure the change in V_{BE} when the device is operated at three different currents. The use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

The temperature sensor takes control of the ADC for 64 µs (typical) every 6 ms. It takes 12 ms to obtain a new temperature measurement from the ADC.

Remote Sensing Diode

The ADM1278 is designed to work with discrete transistors. The transistor can be either a PNP or NPN connected as a diode (base shorted to the collector). If an NPN transistor is used, the collector and base are connected to the TEMP pin and the emitter to PGND. If a PNP transistor is used, the collector and base are connected to PGND and the emitter to TEMP.

The best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage greater than 0.25 V at 6 µA, at the highest operating temperature.
- Base-emitter voltage less than 0.95 V at 100 µA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as the 2N3904, 2N3906, or equivalent in SOT-23 packages are suitable devices to use.

Noise Filtering

For temperature sensors operating in noisy environments, the industry standard practice has been to place a capacitor across the temperature pins to mitigate the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF. Although this capacitor reduces the noise, it does not eliminate it, making it difficult to use the sensor in a very noisy environment.

The ADM1278 has a major advantage over other devices for eliminating the effects of noise on the external sensor. The

series resistance cancellation feature allows a filter to be constructed between the external temperature sensor and the device. The effect of any filter resistance seen in series with the remote sensor is automatically cancelled from the temperature result.

The construction of a filter allows the ADM1278 and the remote temperature sensor to operate in noisy environments. Figure 59 shows a low-pass R-C-R filter with the following values: R = 100 Ω and C = 1 nF. This filtering reduces both common-mode noise and differential noise.

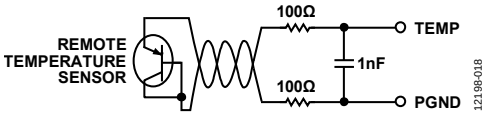


Figure 59. Filter Between Remote Sensor and ADM1278

SPI INTERFACE

The serial peripheral interface (SPI) allows the user to output a stream of raw data from the ADC as soon as new data is available, removing the bandwidth limitations of the PMBus interface for data readback. The PMBus remains as an active data bus and all configuration and register access must still be completed over the PMBus interface. However, the SPI interface can be used at the same time to serially output the ADC monitoring data. It is a 3-pin serial interface capable of operating at speeds of up to 1 MHz.

The SPI pins are only available on the ADM1278-2 model. If the ADM1278-2 model is used but the SPI pins are not required, tie the SPI input pins ($\overline{\text{SPI_SS}}$, MCLK) to VCAP and the SPI output pin (MDAT) can be left floating or tied to GND.

$\overline{\text{SPI_SS}}$ is the slave select pin, and when it is held low, the MCLK pin can be used to clock data out on the MDAT serial output pin. The $\overline{\text{SPI_SS}}$ pin is also used to frame the output data. The SPI pins are compatible with SPI Mode 0 (CPOL = CPHA = 0), but it is also possible to launch and capture data on the same clock edge for extra timing margin if required.

The interface has the following characteristics:

- MDAT is driven by the ADM1278 (master input, slave output). $\overline{\text{SPI_SS}}$ and MCLK are driven by the user, for example, a baseboard management controller (BMC).
- No header or ID information required. The 80-bit data format is fixed regardless of ADC sampling selection (see Figure 60).
- The falling edge of $\overline{\text{SPI_SS}}$ activates the serial interface, at which point MCLK can be used to clock out data on MDAT. The time between $\overline{\text{SPI_SS}}$falling edges must be greater than or equal to the maximum ADC sampling time to avoid duplicate data.
- Select single shot mode to allow the falling edge of $\overline{\text{SPI_SS}}$ to trigger ADC sampling (ADC convert start signal).
- Maximum clock speed (MCLK) is approximately 1 MHz.
- The output stream can be stopped at any point in the output frame via a rising edge on the $\overline{\text{SPI_SS}}$ pin.
- The MSB of each sample is output first.
- The output data line is high impedance when not transmitting.

For example, if configuring the SPI interface to read back ADC current samples (16 bits), 15 MCLK falling edges are required to clock out all of the bits after the initial falling edge on $\overline{\text{SPI_SS}}$. These bits can be clocked out at 1 MHz; therefore, with an ADC sample time of approximately 165 µs, the latency between sample and data is 181 µs. See Figure 3 for SPI timing information.

Note that the MDAT output samples are offset by one sample from the ADC.

Figure 60. Output Data Format

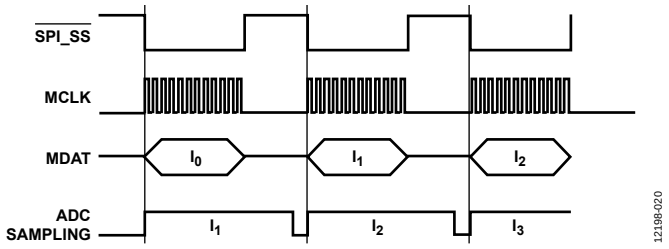


Figure 61. Streaming Current Data Only

V_{OUT} MEASUREMENT

The VOUT pin measures the output voltage after the FET. This voltage is used by the device to determine the V_{DS} of the MOSFET for foldback operation. Add a 1 kΩ resistor in series between the source of the FET and the VOUT pin. This resistor provides some separation between the ADM1278 and the FET source during a fault condition; thus, ADM1278 operation is not affected.

The VOUT pin on the ADM1278 can also be used to provide an alternate voltage for the power monitor to measure. The user can choose to measure the input voltage at the HS+ pin and/or the output voltage at the VOUT pin.

FET HEALTH

The ADM1278 provides a comprehensive method of detecting a faulty pass MOSFET. When a faulty FET is detected, the following occurs:

- PWRGD is deasserted.
- FAULT is asserted and latched low.
- FET health PMBus status bits are asserted and latched.

This detection feature ensures that any downstream dc-to-dc converters are disabled, limiting the power dissipation in any faulty or overheating FETs until the user clears the fault, which can be critical to avoid any catastrophic events due to faulty FETs.

A gate to source or gate to drain short is a common type of FET failure. This type of failure is detected by the ADM1278 at any time during operation.

A less common failure is a drain to source short. This normally occurs due to a board manufacturing defect such as a solder short. This type of failure is detected during the initial power-on reset cycle after power-up or after a 10 second autoretry attempt.

There is also an option to disable FET health detection via the PMBus.

POWER THROTTLING

The ADM1278 provides a number of methods for initiating power throttling of a processor. The simplest method is to configure one of the alert pins for HS_INLIM_ENx (Alert 1 and Alert 2 configuration registers, Bit 4). A latched alert is then generated within a few microseconds after the circuit breaker threshold is exceeded (that is, when the TIMER pin starts ramping). This signal throttles the processor in an attempt to reduce the system current level below the circuit breaker threshold before the TIMER regulation period expires.

The CSOUT pin can be used for the purposes of power throttling as well. The response time of the CSOUT pin to a V_{SENSE} step of 10 mV is approximately 10 µs. The CSOUT pin can then be fed into a comparator (via a resistor divider) to set a programmable analog threshold for the system current. The output of the comparator can be used to throttle the processor after the configured threshold has been exceeded. The advantage of using the CSOUT pin is that the threshold for power throttling can be configured independently of the active hot swap current limit. However, the accuracy of the CSOUT pin has to be taken into account when setting the power throttling threshold.

The latest Intel® processors have a fast processor hot (fast PROCHOT) input/output pin that can be used for power throttling. Asserting this pin initiates a deep throttle of the processor. This is usually used as a last attempt at throttling to avoid a card shutting down when all else has failed. The HS_INLIM_FAULT alert signal or the CSOUT pin can be used to drive this fast PROCHOT pin to achieve power throttling.

POWER MONITOR

The ADM1278 features an integrated ADC that accurately measures the current sense voltage, the input voltage, and optionally, the output voltage and temperature at an external transistor. The measured input voltage and current being delivered to the load are multiplied together to give a power value that can be read back. Each power value is also added to an energy accumulator that can be read back to allow an external device to calculate the energy consumption of the load.

The ADM1278 reports the measured current, input voltage, output voltage, and temperature. The PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE commands can be used to read the highest readings since the value was last cleared.

An averaging function is provided for voltage, current, and power that allows a number of samples to be averaged together by the ADM1278. This function reduces the need for postprocessing of sampled data by the host processor. The number of samples that can be averaged is 2^N, where N is in the range of 0 to 7.

The power monitor current sense amplifier is bipolar and measures both positive and negative currents. The power monitor amplifier has an input range of ±25 mV.

The two basic modes of operation for the power monitor are single shot and continuous. In single shot mode, the ADC samples the input voltage and current a number of times, depending on the averaging value selected by the user. The ADM1278 returns a single value corresponding to the average voltage and current measured. When configured for continuous mode, the power monitor continuously samples the voltage and current, making the most recent sample available to be read.

The single shot mode can be triggered in a number of ways. The simplest method is by selecting the single shot mode using the PMON_CONFIG command and writing to the convert bit using the PMON_CONTROL command. The convert bit can also be written as part of a PMBus group command. Using a group command allows multiple devices to be written to as part of the same I^2C bus transaction, with all devices executing the command when the stop condition appears on the bus. In this way, several devices can be triggered to sample at the same time.

Each time current sense and input voltage measurements are taken, a power calculation is performed, multiplying the two measurements together. This can be read from the device using the READ_PIN command, returning the input power.

At the same time, the calculated power value is added to a power accumulator register that may increment a rollover counter if the value exceeds the maximum accumulator value. The power accumulator register also increments a power sample counter.

The power accumulator and power sample counter are read using the same READ_EIN command to ensure that the accumulated value and sample count are from the same point in time. The bus host reading the data assigns a time stamp when the data is read. By calculating the time difference between consecutive uses of READ_EIN and determining the delta in power consumed, it is possible for the host to determine the total energy consumed over that period.

PMBUS INTERFACE

The I²C bus is a common, simple serial bus used by many devices to communicate. It defines the electrical specifications, the bus timing, the physical layer, and some basic protocol rules.

SMBus is based on I²C and aims to provide a more robust and fault tolerant bus. Functions such as bus timeout and packet error checking are added to help achieve this robustness, together with more specific definitions of the bus messages used to read and write data to devices on the bus.

PMBus is layered on top of SMBus and, in turn, on I²C. Using the SMBus defined bus messages, PMBus defines a set of standard commands that can be used to control a device that is part of a power chain.

The ADM1278 command set is based on the *PMBus™ Power System Management Protocol Specification*, Part I and Part II, Revision 1.2. This version of the standard is intended to provide a common set of commands for communicating with dc-to-dc type devices. However, many of the standard PMBus commands can be mapped directly to the functions of a hot swap controller.

Part I and Part II of the PMBus standard describe the basic commands and their use in a typical PMBus setup. The following sections describe how the PMBus standard and the ADM1278 specific commands are used.

DEVICE ADDRESSING

The ADM1278 is available in three A grade models: the ADM1278-1, ADM1278-2, and ADM1278-3. There is also an AA grade version of the ADM1278-1 with improved power monitoring accuracy and a B grade version with lower power monitoring accuracy.

The PMBus device address is seven bits in size. There are no default addresses for any of the models; any device can be programmed to any of 16 possible addresses. Two quad level ADRx pins map to the 16 possible device addresses.

Table 10. ADRx Pin Connections

ADRx State	ADRx Pin Connection
Low	Connect to GND
Resistor	150 kΩ resistor to GND
High-Z	No connection (floating)
High	Connect to VCAP

Table 11. PMBus Address Decode (7-Bit Address)

ADR2 State	ADR1 State	Device Address (Hex)
Low	Low	0x10
Low	Resistor	0x11
Low	High-Z	0x12
Low	High	0x13
Resistor	Low	0x40
Resistor	Resistor	0x41
Resistor	High-Z	0x42
Resistor	High	0x43
High-Z	Low	0x44
High-Z	Resistor	0x45
High-Z	High-Z	0x46
High-Z	High	0x47
High	Low	0x50
High	Resistor	0x51
High	High-Z	0x52
High	High	0x53

SMBUS PROTOCOL USAGE

All I²C transactions on the ADM1278 are performed using SMBus defined bus protocols. The following SMBus protocols are implemented by the ADM1278:

- Send byte
- Receive byte
- Write byte
- Read byte
- Write word
- Read word
- Block read

PACKET ERROR CHECKING

The ADM1278 PMBus interface supports the use of the packet error checking (PEC) byte that is defined in the SMBus standard. The PEC byte is transmitted by the ADM1278 during a read transaction or sent by the bus host to the ADM1278 during a write transaction. The ADM1278 supports the use of PEC with all the SMBus protocols that it implements.

The use of the PEC byte is optional. The bus host can decide whether to use the PEC byte with the ADM1278 on a message by message basis. There is no need to enable or disable PEC in the ADM1278.

The PEC byte is used by the bus host or the ADM1278 to detect errors during a bus transaction, depending on whether the transaction is a read or a write. If the host determines that the PEC byte read during a read transaction is incorrect, it can decide to repeat the read if necessary. If the ADM1278 determines that the PEC byte sent during a write transaction is incorrect, it ignores the command (does not execute it) and sets a status flag.

Within a group command, the host can choose whether to send a PEC byte as part of the message to the ADM1278.

PARTIAL TRANSACTIONS ON I²C BUS

If there is a partial transaction on the I²C bus (for example, spurious data interpreted as a start command), the ADM1278 I²C bus is not locked up, thinking it is in the middle of an I²C transaction. A new start command is recognized even in the middle of another transaction.

SMBUS MESSAGE FORMATS

Figure 62 to Figure 70 show all the SMBus protocols supported by the ADM1278, along with the PEC variant. In these figures, unshaded cells indicate that the bus host is actively driving the bus; shaded cells indicate that the ADM1278 is driving the bus.

Figure 62 to Figure 70 use the following abbreviations:

- S is the start condition.
- Sr is the repeated start condition.
- P is the stop condition.
- R is the read bit.
- $\overline{W}$ is the write bit.
- A is the acknowledge bit (0).
- $\overline{A}$ is the acknowledge bit (1).

A, the acknowledge bit, is typically active low (Logic 0) when the transmitted byte is successfully received by a device. However, when the receiving device is the bus master, the acknowledge bit for the last byte read is a Logic 1, indicated by $\overline{A}$.

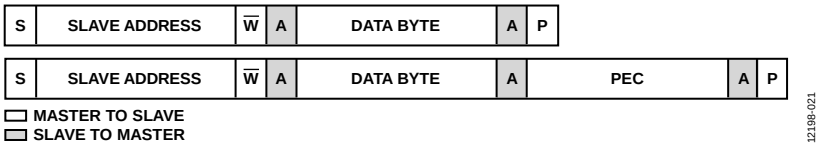


Figure 62. Send Byte and Send Byte with PEC

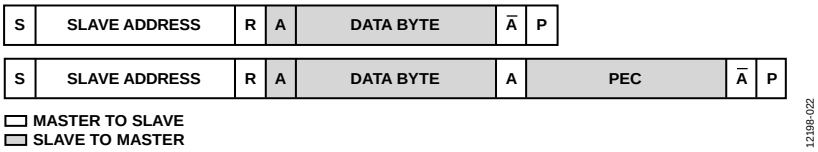


Figure 63. Receive Byte and Receive Byte with PEC

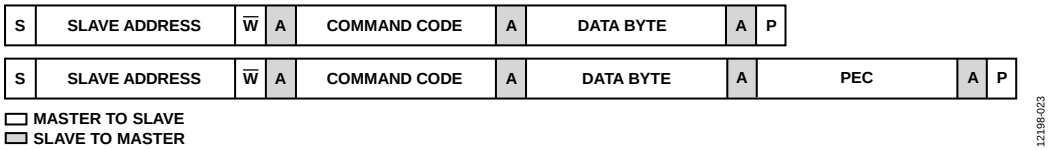


Figure 64. Write Byte and Write Byte with PEC

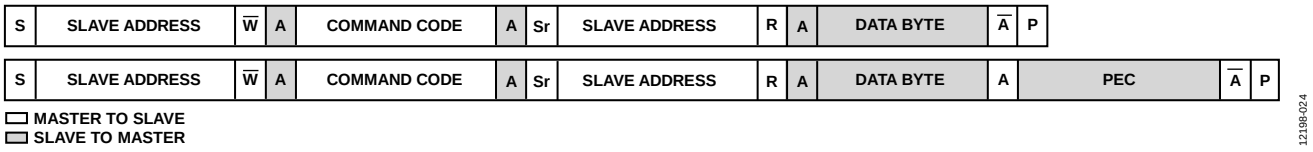


Figure 65. Read Byte and Read Byte with PEC

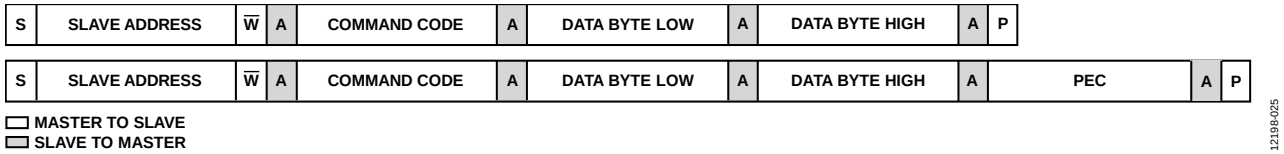


Figure 66. Write Word and Write Word with PEC

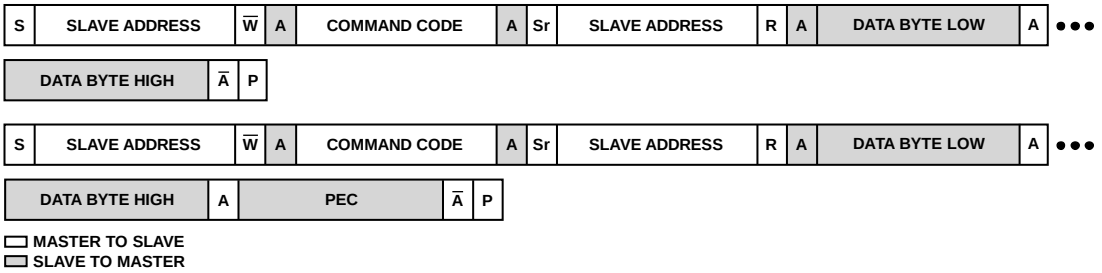


Figure 67. Read Word and Read Word with PEC

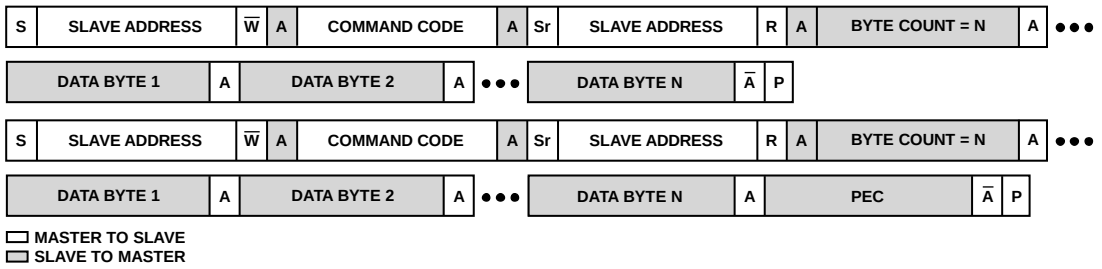


Figure 68. Block Read and Block Read with PEC

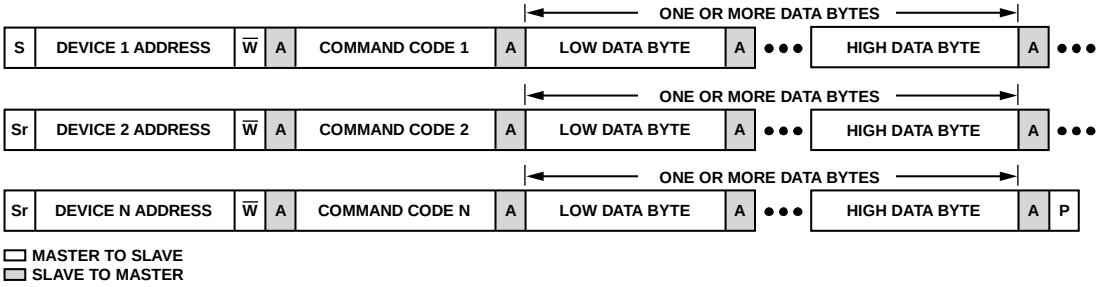


Figure 69. Group Command

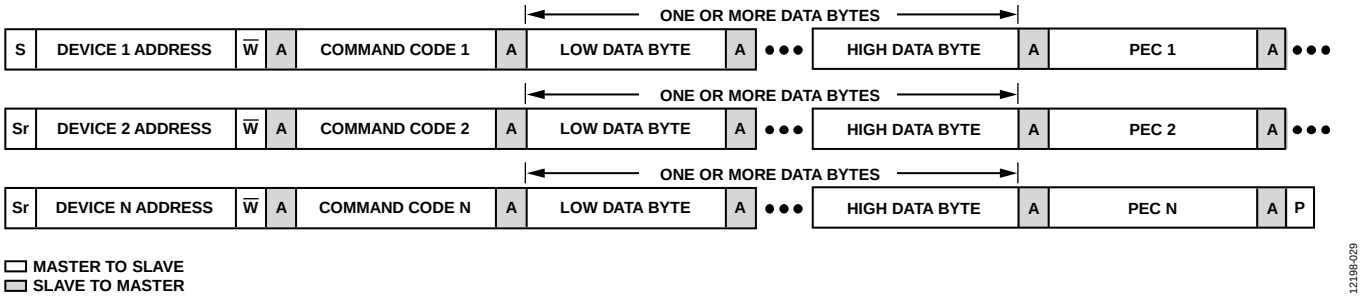


Figure 70. Group Command with PEC

GROUP COMMANDS

The PMBus standard defines what are known as group commands. Group commands are single bus transactions that send commands or data to more than one device at the same time. Each device is addressed separately, using its own address; there is no special group command address. A group command transaction can contain only write commands that send data to a device. It is not possible to use a group command to read data from devices.

From an I²C protocol point of view, a normal write command consists of the following:

- I²C start condition.
- Slave address bits and a write bit (followed by an acknowledge from the slave device).
- One or more data bytes (each of which is followed by an acknowledge from the slave device).
- I²C stop condition to end the transaction.

A group command differs from a nongroup command in that after the data is written to one slave device, a repeated start condition is placed on the bus followed by the address of the next slave device and data. This continues until all of the devices have been written to, at which point the stop condition is placed on the bus by the master device.

The format of a group command and a group command with PEC is shown in Figure 69 and Figure 70, respectively.

Each device that is written to as part of the group command does not immediately execute the command written. The device must wait until the stop condition appears on the bus. At that point, all devices execute their commands at the same time.

Using a group command, it is possible, for example, to turn multiple PMBus devices on or off simultaneously. In the case of the ADM1278, it is also possible to issue a power monitor command that initiates a conversion, causing multiple ADM1278 devices to sample together at the same time.

HOT SWAP CONTROL COMMANDS

OPERATION Command

The GATE pin that drives the FET is controlled by a dedicated hot swap state machine. The UV and OV input pins, the TIMER, PWGIN, and ENABLE pins, and the current sense all feed into the state machine, and they control when and how strongly the gate is turned off.

It is also possible to control the hot swap GATE output using commands over the PMBus interface. The OPERATION command can be used to request the hot swap output to turn on. However, if the UV pin indicates that the input supply is less than required, the hot swap output is not turned on, even if the OPERATION command requests that the output be enabled.

If the OPERATION command is used to disable the hot swap output, the GATE pin is held low, even if all hot swap state machine control inputs indicate that it can be enabled.

The default state of Bit 7 (also named the ON bit) of the OPERATION command is 1; therefore, the hot swap output is always enabled when the ADM1278 emerges from UVLO. If the on bit is never changed, the UV input or the ENABLE/$\overline{\text{ENABLE}}$ input is the hot swap master on/off control signal.

If the on bit is set to 0 while the UV signal is high, the hot swap output is turned off. If the UV signal is low or if the OV signal is high, the hot swap output is already off and the status of the on bit has no effect.

If the on bit is set to 1, the hot swap output is requested to turn on. If the UV signal is low or if the OV signal is high, setting the on bit to 1 has no effect, and the hot swap output remains off.

It is possible to determine at any time whether the hot swap output is enabled using the STATUS_BYTE or the STATUS_WORD command (see the Status Commands section).

The OPERATION command can also clear any latched faults in the status registers. To clear latched faults, set the on bit to 0 and then reset it to 1. This also clears the latched $\overline{\text{FAULT}}$ pin.

DEVICE_CONFIG Command

The DEVICE_CONFIG command configures certain settings within the ADM1278, for example, enabling or disabling FET health detection, general-purpose output pin configuration, and modifying the duration of the severe overcurrent settings.

POWER_CYCLE Command

The POWER_CYCLE command can be used to request that the ADM1278 be turned off for approximately five seconds and then turned back on. This command is useful if the processor that controls the ADM1278 is also powered off when the ADM1278 is turned off. This command allows the processor to request that the ADM1278 turn off and on again as part of a single command.

ADM1278 INFORMATION COMMANDS

CAPABILITY Command

The CAPABILITY command can be used by host processors to determine the I²C bus features that are supported by the ADM1278. The features that can be reported include the maximum bus speed, whether the device supports the packet error checking (PEC) byte, and the SMBAlert reporting function.

PMBUS_REVISION Command

The PMBUS_REVISION command reports the version of Part I and Part II of the PMBus standard.

MFR_ID, MFR_MODEL, and MFR_REVISION Commands

The MFR_ID, MFR_MODEL, and MFR_REVISION commands return ASCII strings that can be used to facilitate detection and identification of the ADM1278 on the bus.

These commands are read using the SMBus block read message type. This message type requires that the ADM1278 return a byte count corresponding to the length of the string data that is to be read back.

STATUS COMMANDS

The ADM1278 provides a number of status bits to report faults and warnings from the hot swap controller and the power monitor. These status bits are located in six different registers that are arranged in a hierarchy. The STATUS_BYTE and STATUS_WORD commands provide 8 bits and 16 bits of high level information, respectively. The STATUS_BYTE and STATUS_WORD commands contain the most important status bits, as well as pointer bits that indicate whether any of the five other status registers need to be read for more detailed status information.

In the ADM1278, a particular distinction is made between faults and warnings. A fault is always generated by the hot swap controller and is typically defined by hardware component values. Events that can generate a fault are

- Overcurrent condition that causes the hot swap timer to time out
- Overvoltage condition on the OV pin
- Undervoltage condition on the UV pin
- Overtemperature condition
- FET health issue detected

When a fault occurs, the hot swap controller always takes some action, usually to turn off the GATE pin, which is driving the FET. The $\overline{\text{FAULT}}$ pin is asserted, and the PWRGD pin is deasserted. A fault can also generate an SMBAlert on the GPO2/$\overline{\text{ALERT2}}$ pin.

All warnings in the ADM1278 are generated by the power monitor, which samples the voltage, current, and temperature and then compares these measurements to the threshold values set by the various limit commands. A warning has no effect on the hot swap controller, but it may generate an SMBAlert on one or both of the GPOx/$\overline{\text{ALERTx}}$ output pins.

When a status bit is set, it always means that the status condition—fault or warning—is active or was active at some point in the past. When a fault or warning bit is set, it is latched until it is explicitly cleared using either the OPERATION or the CLEAR_FAULTS command. Some other status bits are live, that is, they always reflect a status condition and are never latched.

STATUS_BYTE and STATUS_WORD Commands

The STATUS_BYTE and STATUS_WORD commands obtain a snapshot of the overall device status. These commands indicate whether it is necessary to read more detailed information using the other status commands.

The low byte of the word returned by the STATUS_WORD command is the same byte returned by the STATUS_BYTE command. The high byte of the word returned by the STATUS_WORD command provides a number of bits that determine which of the other status commands needs to be issued to obtain all active status bits. The status bits for FET health and power good are also found in the high byte of STATUS_WORD.

STATUS_INPUT Command

The STATUS_INPUT command returns a number of bits relating to voltage faults and warnings on the input supply as well as the overpower warning.

STATUS_VOUT Command

The STATUS_VOUT command returns a number of bits relating to voltage warnings on the output supply.

STATUS_IOUT Command

The STATUS_IOUT command returns a number of bits relating to current faults and warnings on the output supply.

STATUS_TEMPERATURE Command

The STATUS_TEMPERATURE command returns a number of bits relating to temperature faults and warnings at the external transistor.

STATUS_MFR_SPECIFIC Command

The STATUS_MFR_SPECIFIC command is a standard PMBus command, but the contents of the byte returned are specific to the ADM1278.

CLEAR_FAULTS Command

The CLEAR_FAULTS command clears fault and warnings bits when they are set. Fault and warnings bits are latched when they are set. In this way, a host can read the bits any time after the fault or warning condition occurs and determine which problem actually occurred.

If the CLEAR_FAULTS command is issued and the fault or warning condition is no longer active, the status bit is cleared. If the condition is still active—for example, if an input voltage is below the undervoltage threshold of the UV pin—the CLEAR_FAULTS command attempts to clear the status bit, but that status bit is immediately set again.

GPO AND ALERT PIN SETUP COMMANDS

Two multipurpose pins are provided on the ADM1278: GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$.

These pins can be configured over the PMBus in one of three output modes, as follows:

- General-purpose digital output
- Output for generating an SMBAlert when one or more fault/warning status bits become active in the PMBus status registers
- Digital comparator

In digital comparator mode, the current, voltage, power and temperature warning thresholds are compared to the values read or calculated by the ADM1278. The comparison result sets the output high or low according to whether the value is greater or less than the warning threshold that has been set.

For an example of how to configure these pins to generate an SMBAlert and how to respond and clear the condition, see the Example Use of SMBus ARA section.

ALERT1_CONFIG and ALERT2_CONFIG Commands

Using combinations of bit masks, the ALERT1_CONFIG and ALERT2_CONFIG commands select the status bits that, when set, generate an SMBAlert signal to a processor, or control the digital comparator mode. Pin 13 and Pin 14 (GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$) must be configured in SMBAlert or digital comparator mode in the DEVICE_CONFIG register.

When Pin 13 or Pin 14 is configured in GPO mode, the pin is under software control. If this mode is set, the SMBAlert masking bits are ignored.

POWER MONITOR COMMANDS

The ADM1278 provides a high accuracy, 12-bit current, voltage, and temperature power monitor. The power monitor can be configured in a number of different modes of operation and can run in either continuous mode or single shot mode with different sample averaging options.

The power monitor can measure the following quantities:

- Input voltage (V_{IN})
- Output voltage (V_{OUT})
- Output current (I_{OUT})
- External temperature

The following quantities are then calculated:

- Input power (P_{IN})
- Input energy (E_{IN})

PMON_CONFIG Command

The power monitor can run in a variety of modes. The PMON_CONFIG command sets up the power monitor.

The settings that can be configured are as follows:

- Single shot or continuous sampling
- V_{IN}/V_{OUT}/temperature sampling enable/disable
- Current and voltage sample averaging
- Power sample averaging
- Simultaneous sampling enable/disable
- Temperature sensor filter enable/disable

Modifying the power monitor settings while the power monitor is sampling is not recommended. To ensure correct operation of the device and to avoid any potential spurious data or the generation of status alerts, stop the power monitor before any of these settings are changed.

PMON_CONTROL Command

Power monitor sampling can be initiated via hardware or via software using the PMON_CONTROL command. This command can be used with single shot or continuous mode.

READ_VIN, READ_VOUT, and READ_IOUT Commands

The ADM1278 power monitor always measures the voltage developed across the sense resistor to provide a current measurement. The input voltage measurement from the HS+ pin is also enabled by default. The output voltage present on the VOUT pin is available if enabled with the PMON_CONFIG command.

READ_TEMPERATURE_1 Command

Temperature measurement at an external transistor can also be enabled with the PMON_CONFIG command. If enabled, the temperature sensor takes over the ADC for 64 µs (typical) every 6 ms and returns a measurement every 12 ms.

READ_PIN, READ_PIN_EXT, READ_EIN, and READ_EIN_EXT Commands

The 12-bit input voltage (V_{IN}) and 12-bit current (I_{OUT}) measurement values are multiplied by the ADM1278 to give the input power value. This is accomplished by using fixed point arithmetic, and produces a 24-bit value. It is assumed that the numbers are in the 12.0 format, meaning that there is no fractional part. Note that only positive I_{OUT} values are used to avoid returning a negative power.

This 24-bit value can be read from the ADM1278 using the READ_PIN_EXT command, where the most significant bit (MSB) is always a zero because PIN_EXT is a twos complement binary value that is always positive.

The 16 most significant bits of the 24-bit value are used as the value for P_{IN}. The MSB of the 16-bit P_{IN} word is always zero, because P_{IN} is a twos complement binary value that is always positive.

Each time a power calculation is completed, the 24-bit power value is added to a 24-bit energy accumulator register. This is a twos complement representation as well; therefore, the MSB is always zero. Each time this energy accumulator register rolls over from 0x7FFFFF to 0x000000, a 16-bit rollover counter is incremented. The rollover counter is straight binary, with a maximum value of 0xFFFF before it rolls over.

A 24-bit straight binary power sample counter is also incremented by 1 each time a power value is calculated and added to the energy accumulator.

These registers can be read back using one of two commands, depending on the level of accuracy required for the energy accumulator and the desire to limit the frequency of reads from the ADM1278.

A bus host can read these values, and by calculating the delta in the energy accumulated, the delta in the number of samples, and the time delta since the last read, the host can calculate the average power since the last read, as well as the energy consumed since then.

The time delta is calculated by the bus host based on when it sends its commands to read from the device, and is not provided by the ADM1278.

To avoid loss of data, the bus host must read at a rate that ensures the rollover counter does not wrap around more than once, and if the counter does wrap around, that the next value read for P_{IN} is less than the previous one.

The READ_EIN command returns the top 16 bits of the energy accumulator, the lower 8 bits of the rollover counter, and the full 24 bits of the sample counter.

The READ_EIN_EXT command returns the full 24 bits of the energy accumulator, the full 16 bits of the rollover counter, and the full 24 bits of the sample counter. The use of the longer rollover counter means that the time interval between reads of the device can be increased from seconds to minutes without losing any data.

PEAK_IOUT, PEAK_VIN, PEAK_VOUT, PEAK_PIN, and PEAK_TEMPERATURE Commands

In addition to the standard PMBus commands for reading voltage and current, the ADM1278 provides commands that can report the maximum peak voltage, current, power, or temperature value since the peak value was last cleared.

The peak values are updated only after the power monitor has sampled and averaged the current and voltage measurements. Individual peak values are cleared by writing a 0 value with the corresponding command.

WARNING LIMIT SETUP COMMANDS

The ADM1278 power monitor can monitor a number of different warning conditions simultaneously and report any current, voltage, power, or temperature values that exceed the user defined thresholds using the status commands.

All comparisons performed by the power monitor require the measured value to be strictly greater or less than the threshold value.

At power-up, all threshold limits are set to either minimum scale (for undervoltage or undercurrent conditions) or to maximum scale (for overvoltage, overcurrent, overpower, or overtemperature conditions). This effectively disables the generation of any status warnings by default; warning bits are not set in the status registers until the user explicitly sets the threshold values.

VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT Commands

The VIN_OV_WARN_LIMIT and VIN_UV_WARN_LIMIT commands set the OV and UV thresholds on the input voltage, as measured at the HS+ pin.

VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT Commands

The VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_ LIMIT commands set the OV and UV thresholds on the output voltage, as measured at the VOUT pin.

IOUT_OC_WARN_LIMIT Command

The IOUT_OC_WARN_LIMIT command sets the OC threshold for the current flowing through the sense resistor.

OT_WARN_LIMIT Command

The OT_WARN_LIMIT command sets the overtemperature threshold for the temperature measured at the external transistor.

PIN_OP_WARN_LIMIT Command

The PIN_OP_WARN_LIMIT command sets the overpower threshold for the power delivered to the load.

PMBUS DIRECT FORMAT CONVERSION

The ADM1278 uses the PMBus direct format to represent real-world quantities such as voltage, current, and power values. A direct format number takes the form of a 2-byte, twos complement, binary integer value.

It is possible to convert between direct format value and real-world quantities using the following equations. Equation 1 converts from real-world quantities to PMBus direct values, and Equation 2 converts PMBus direct format values to real-world values.

$$Y = (mX + b) \times 10^{R} \quad (1)$$

$$X = 1/m \times (Y \times 10^{-R} - b) \quad (2)$$

where:
Y is the value in PMBus direct format.
X is the real-world value.
m is the slope coefficient, a 2-byte, twos complement integer.
b is the offset, a 2-byte, twos complement integer.
R is a scaling exponent, a 1-byte, twos complement integer.

The same equations are used for voltage, current, power, and temperature conversions, the only difference being the values of the m, b, and R coefficients that are used. Table 12 lists all the coefficients required for the ADM1278. The current and power coefficients shown are dependent on the value of the external sense resistor used in a given application. This means that an additional calculation must be performed to take the sense resistor value into account to obtain the coefficients for a specific sense resistor value.

The sense resistor value used in the calculations to obtain the coefficients is expressed in milliohms. The m coefficients are defined as 2-byte, twos complement numbers in the PMBus standard; therefore, the maximum positive value that can be represented is 32,767. If the m value is greater than that, and is to be stored in PMBus standard form, then divide the m coefficients by 10, and increase the R coefficient by a value of 1. For example, if a 10 mΩ sense resistor is used, the m coefficient for power is 6123, and the R coefficient is −1.

Example 1: IOUT_OC_WARN_LIMIT requires a current-limit value expressed in direct format.

If the required current limit is 10 A and the sense resistor is 2 mΩ, the first step is to determine the voltage coefficient. This is simply m = 800 × 2, giving 1600.

Using Equation 1, and expressing X, in units of amperes,

$$Y = ((1600 \times 10) + 20{,}475) \times 10^{-1}$$

$$Y = 3647.5 = 3648 \text{ (rounded up to integer form)}$$

Writing a value of 3648 with the IOUT_OC_WARN_LIMIT command sets an overcurrent warning at 10 A.

Example 2: the READ_IOUT command returns a direct format value of 3339 representing the current flowing through a sense resistor of 1 mΩ.

To convert this value to the current flowing, use Equation 2, with m = 800 × 1.

$$X = 1/800 \times (3339 \times 10^{1} - 20{,}475)$$

$$X = 16.14 \text{ A}$$

This means that, when READ_IOUT returns a value of 3339, 16.14 A is flowing in the sense resistor.

Note that the same calculations that are used to convert power values also apply to the energy accumulator value returned by the READ_EIN command because the energy accumulator is a summation of multiple power values.

The READ_PIN_EXT and READ_EIN_EXT commands return 24-bit extended precision versions of the 16-bit values returned by READ_PIN and READ_EIN. The direct format values must be divided by 256 prior to being converted with the coefficients shown in Table 12.

Example 3: The PIN_OP_WARN_LIMIT command requires a power limit value expressed in direct format.

If the required power limit is 350 W and the sense resistor is 1 mΩ, the first step is to determine the m coefficient, that is, m = 6123 × 1, which is 6123.

Using Equation 1,

$$Y = ((6123 \times 350) \times 10^{-2}$$

$$Y = 21{,}430.5 = 21{,}431 \text{ (rounded up to integer form)}$$

Writing a value of 21,431 with the PIN_OP_WARN_LIMIT command sets an overpower warning at 350 W.

VOLTAGE AND CURRENT CONVERSION USING LSB VALUES

The direct format voltage and current values returned by the READ_VIN, READ_VOUT, and READ_IOUT commands and the corresponding peak versions are the data output directly by the ADM1278 ADC. Because the voltages and currents are 12-bit ADC output codes, they can also be converted to real-world values when there is knowledge of the size of the LSB on the ADC.

The m, b, and R coefficients defined for the PMBus conversion are required to be whole integers by the standard and have, therefore, been rounded slightly. Using this alternative method, with the exact LSB values, can provide somewhat more accurate numerical conversions.

To convert an ADC code to current in amperes, use the following formulas:

$$V_{SENSE_MO} = LSB_{CURRENT} \times (I_{ADC} - 2048)$$

$$I_{OUT} = V_{SENSE_MO}/(R_{SENSE} \times 0.001)$$

where:
$V_{SENSE_MO} = (V_{MO+}) - (V_{MO-})$.
$LSB_{CURRENT}$ = 12.51 µV.
I_{ADC} is the 12-bit ADC code.
I_{OUT} is the measured current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.

To convert an ADC code to a voltage, use the following formula:

$$V_M = LSB_{VOLTAGE} \times (V_{ADC} + 0.5)$$

where:
V_M is the measured value in volts.
$LSB_{VOLTAGE}$ = 5.104 mV.
V_{ADC} is the 12-bit ADC code.

To convert a current in amperes to a 12-bit value, use the following formula (round the result to the nearest integer):

$$V_{SENSE_MO} = I_A \times R_{SENSE} \times 0.001$$

$$I_{CODE} = 2048 + (V_{SENSE_MO}/LSB_{CURRENT})$$

where:
$V_{SENSE_MO} = (V_{MO+}) - (V_{MO-})$.
I_A is the current value in amperes.
R_{SENSE} is the value of the sense resistor in milliohms.
I_{CODE} is the 12-bit ADC code.
$LSB_{CURRENT}$ = 12.51 µV.

To convert a voltage to a 12-bit value, the following formula can be used (round the result to the nearest integer):

$$V_{CODE} = (V_A/LSB_{VOLTAGE}) - 0.5$$

where:
V_{CODE} is the 12-bit ADC code.
V_A is the voltage value in volts.
$LSB_{VOLTAGE}$ = 5.104 mV.

Table 12. PMBus Conversion to Real-World Coefficients

Coefficient	Voltage (V)	Current (A)	Power (W)	Temperature (°C)
m	+19,599	+800 × R_{SENSE}	+6123 × R_{SENSE}	+42
b	0	+20,475	0	+31,880
R	−2	−1	−2	−1

ALERT PIN BEHAVIOR

The ADM1278 provides a very flexible alert system, whereby one or more fault/warning conditions can be indicated to an external device.

FAULTS AND WARNINGS

A PMBus fault on the ADM1278 is typically generated due to an analog event (the exception being a temperature fault) and causes a change in state in the hot swap output, turning it off. The defined fault sources are as follows:

- Undervoltage (UV) event detected on the UV pin.
- Overvoltage (OV) event detected on the OV pin.
- Overcurrent (OC) event that causes a hot swap timeout.
- Overtemperature (OT) event detected at the external transistor.
- Fault detected with the pass MOSFET.

Faults are continuously monitored, and, as long as power is applied to the device, they cannot be disabled. When a fault occurs, a corresponding status bit is set in one or more STATUS_xxx registers.

A value of 1 in a status register bit field always indicates a fault or warning condition. Fault and warning bits in the status registers are latched when set to 1. To clear a latched bit to 0—provided that the fault condition is no longer active—use the CLEAR_FAULTS command or use the OPERATION command to turn the hot swap output off and then on again.

A warning is less severe than a fault and never causes a change in the state of the hot swap controller. The sources of a warning are defined as follows:

- CML: a communications error occurred on the I^2C bus.
- HS_INLIM_FAULT: the circuit breaker threshold was tripped and the TIMER pin started ramping, but did not necessarily shut the system down.
- I_{OUT} OC warning from the ADC.
- V_{IN} UV warning from the ADC.
- V_{IN} OV warning from the ADC.
- V_{OUT} UV warning from the ADC.
- V_{OUT} OV warning from the ADC.
- P_{IN} overpower (OP) warning from the $V_{IN} \times I_{OUT}$ calculation.
- OT warning from the ADC.
- Hysteretic output warning from the ADC.

GENERATING AN ALERT

A host device can periodically poll the ADM1278 using the status commands to determine whether a fault/warning is active. However, this polling is very inefficient in terms of software and processor resources. The ADM1278 has two output pins (GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$) that can be used to generate interrupts to a host processor.

By default at power-up, the open-drain GPO1/$\overline{\text{ALERT1}}$ /CONV and GPO2/$\overline{\text{ALERT2}}$ outputs are high impedance; therefore, the pins can be pulled high through a resistor. The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins are disabled by default on the ADM1278.

Any one or more of the faults and warnings listed in the Faults and Warnings section can be enabled and cause an alert, making the corresponding GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pin active. By default, the active state of the GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins are low.

For example, to use GPO2/$\overline{\text{ALERT2}}$ to monitor the V_{OUT} UV warning from the ADC, the followings steps must be performed:

1. Set a threshold level with the VOUT_UV_WARN_LIMIT command.
2. Set the VOUT_UV_WARN_EN2 bit in the ALERT2_CONFIG register.
3. Start the power monitor sampling on V_{OUT} (ensure the power monitor is configured to sample V_{OUT} in the PMON_CONFIG register).

If a V_{OUT} sample is taken that is below the configured V_{OUT} UV value, the GPO2/$\overline{\text{ALERT2}}$ pin is pulled low, signaling an interrupt to a processor.

HANDLING/CLEARING AN ALERT

When faults/warnings are configured on the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ pins, the pin becomes active to signal an interrupt to the processor. (The pin is active low, unless inversion is enabled.) The GPO1/$\overline{\text{ALERT1}}$ /CONV or GPO2/$\overline{\text{ALERT2}}$ signal performs the functions of an SMBAlert.

Note that the GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins can become active independently but they are always made inactive together.

A processor can respond to the interrupt in one of two ways, depending on whether there is a single or multiple devices on the bus.

Single Device on Bus

When there is only one device on the bus, the processor simply reads the status bytes and issues a CLEAR_FAULTS command to clear all the status bits, which causes the deassertion of the GPO1/$\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ line. If there is a persistent fault (for example, an undervoltage on the input), the status bits remain set after the CLEAR_ FAULTS command is executed because the fault has not been removed. However, the GPO1/ $\overline{\text{ALERT1}}$/CONV or GPO2/$\overline{\text{ALERT2}}$ line is not pulled low unless a new fault or warning becomes active. If the cause of the SMBAlert is a power monitor generated warning and the power monitor is running continuously, the next sample generates a new SMBAlert after the CLEAR_FAULTS command is issued.

Multiple Devices on Bus

When there are several devices on the bus, the processor issues an SMBus alert response address (ARA) command to find out which device asserted the SMBAlert line. The processor reads the status bytes from that device and issues a CLEAR_FAULTS command.

SMBUS ALERT RESPONSE ADDRESS

The SMBus ARA is a special address that can be used by the bus host to locate any devices that need to communicate with the bus host. A host typically uses a hardware interrupt pin to monitor the SMBus alert pins of multiple devices. When the host interrupt occurs, the host issues a message on the bus using the SMBus receive byte or receive byte with PEC protocol.

The special address used by the host is 0x0C. Any devices that have an SMB alert signal return their own 7-bit address as the seven MSBs of the data byte. The LSB value is not used and can be either 1 or 0. The host reads the device address from the received data byte and proceeds to handle the alert condition.

More than one device may have an active SMBAlert signal and attempt to communicate with the host. In this case, the device with the lowest address dominates the bus and succeeds in transmitting its address to the host. The device that succeeds disables its SMBus alert signal. If the host sees that the SMBus alert signal is still low, it continues to read addresses until all devices that need to communicate have successfully transmitted their addresses.

EXAMPLE USE OF SMBUS ARA

The full sequence of steps that occurs when an SMBAlert is generated and cleared is as follows:

1. A fault or warning is enabled using the ALERT2_CONFIG command, and the corresponding status bit for the fault or warning changes from 0 to 1, indicating that the fault or warning has just become active.
2. The GPO2/$\overline{\text{ALERT2}}$ pin becomes active (set low) to signal that an SMBAlert is active.
3. The host processor issues an SMBus ARA command to determine which device has an active alert.
4. If there are no other active alerts from devices with lower I2C addresses, this device makes the GPO2/$\overline{\text{ALERT2}}$ pin inactive (set high) during the no acknowledge bit period after it sends its address to the host processor.
5. If the GPO2/$\overline{\text{ALERT2}}$ pin stays low, the host processor must continue to issue SMBus ARA commands to devices to determine the addresses of all devices that require a status check.
6. The ADM1278 continues to operate with the GPO2/$\overline{\text{ALERT2}}$ pin inactive and the contents of the status bytes unchanged until the host reads the status bytes and clears them, or until a new fault occurs. That is, if a status bit for a fault/warning that is enabled on the GPO2/$\overline{\text{ALERT2}}$ pin and that was not already active (equal to 1) changes from 0 to 1, a new alert is generated, causing the GPO2/$\overline{\text{ALERT2}}$ pin to become active again.

DIGITAL COMPARATOR MODE

The GPO1/$\overline{\text{ALERT1}}$/CONV and GPO2/$\overline{\text{ALERT2}}$ pins can be configured to indicate if a user defined threshold for voltage, current, or power is being exceeded. In this mode, the output pin is live and is not latched when a warning threshold is exceeded. In effect, the pin acts as a digital comparator, where the threshold is set using the warning limit threshold commands.

The ALERTx_CONFIG command is used, as for the SMBAlert configuration, to select the specific warning threshold to be monitored. The GPO1/ALERT1/CONV or GPO2/ALERT2 pin then indicates if the measured value is above or below the threshold.

TYPICAL APPLICATION CIRCUITS

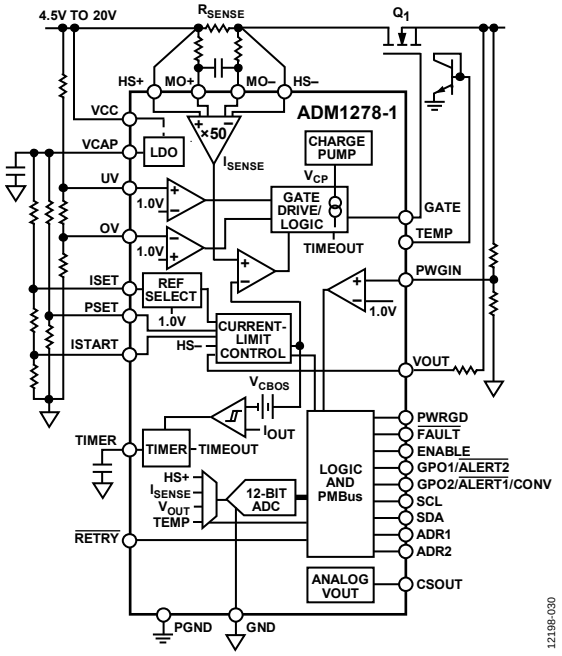


Figure 71. ADM1278-1 Typical Application Circuit

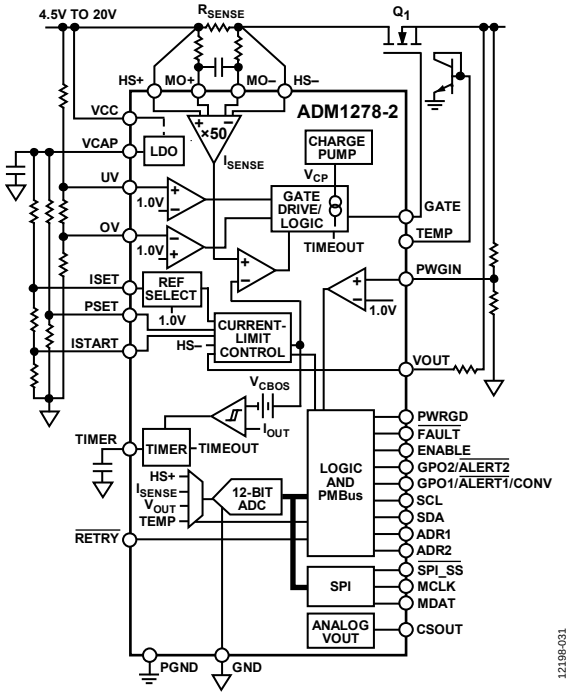


Figure 72. ADM1278-2 Typical Application Circuit

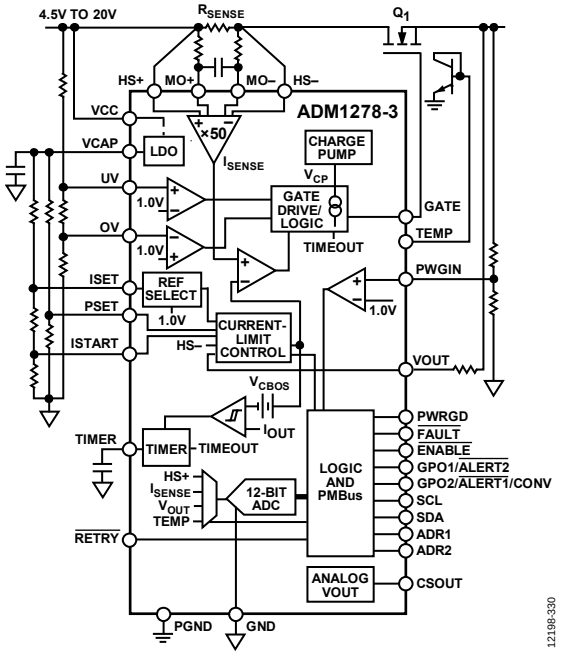


Figure 73. ADM1278-3 Typical Application Circuit

PMBUS COMMAND REFERENCE

Register addresses are in hexadecimal format.

Table 13. PMBus Command Summary

Address	Name	SMBus Transaction Type	Number of Data Bytes	Reset
0x01	OPERATION	Read/write byte	1	0x80
0x03	CLEAR_FAULTS	Send byte	0	Not applicable
0x19	CAPABILITY	Read byte	1	0xB0
0x42	VOUT_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0x43	VOUT_UV_WARN_LIMIT	Read/write word	2	0x0000
0x4A	IOUT_OC_WARN_LIMIT	Read/write word	2	0x0FFF
0x4F	OT_FAULT_LIMIT	Read/write word	2	0x0FFF
0x51	OT_WARN_LIMIT	Read/write word	2	0x0FFF
0x57	VIN_OV_WARN_LIMIT	Read/write word	2	0x0FFF
0x58	VIN_UV_WARN_LIMIT	Read/write word	2	0x0000
0x6B	PIN_OP_WARN_LIMIT	Read/write word	2	0x7FFF
0x78	STATUS_BYTE	Read byte	1	0x00
0x79	STATUS_WORD	Read word	2	0x0000
0x7A	STATUS_VOUT	Read byte	1	0x00
0x7B	STATUS_IOUT	Read byte	1	0x00
0x7C	STATUS_INPUT	Read byte	1	0x00
0x7D	STATUS_TEMPERATURE	Read byte	1	0x00
0x80	STATUS_MFR_SPECIFIC	Read byte	1	0x00
0x86	READ_EIN	Block read	6	0x000000000000
0x88	READ_VIN	Read word	2	0x0000
0x8B	READ_VOUT	Read word	2	0x0000
0x8C	READ_IOUT	Read word	2	0x0000
0x8D	READ_TEMPERATURE_1	Read word	2	0x0000
0x97	READ_PIN	Read word	2	0x0000
0x98	PMBUS_REVISION	Read byte	1	0x22
0x99	MFR_ID	Block read	3	ASCII = ADI
0x9A	MFR_MODEL	Block read	10	ASCII = ADM1278-xy
0x9B	MFR_REVISION	Block read	1	0x33
0x9D	MFR_DATE	Block read	6	ASCII = YYMMDD
0xD0	PEAK_IOUT	Read/write word	2	0x0000
0xD1	PEAK_VIN	Read/write word	2	0x0000
0xD2	PEAK_VOUT	Read/write word	2	0x0000
0xD3	PMON_CONTROL	Read/write byte	1	0x01
0xD4	PMON_CONFIG	Read/write word	2	0x0714
0xD5	ALERT1_CONFIG	Read/write word	2	0x0000
0xD6	ALERT2_CONFIG	Read/write word	2	0x0000
0xD7	PEAK_TEMPERATURE	Read/write word	2	0x0000
0xD8	DEVICE_CONFIG	Read/write word	2	0x000D
0xD9	POWER_CYCLE	Send byte	0	Not applicable
0xDA	PEAK_PIN	Read/write word	2	0x0000
0xDB	READ_PIN_EXT	Block read	3	0x000000
0xDC	READ_EIN_EXT	Block read	8	0x0000000000000000
0xF2	HYSTERESIS_LOW	Read/write word	2	0x0000
0xF3	HYSTERESIS_HIGH	Read/write word	2	0xFFFF
0xF4	STATUS_HYSTERESIS	Read byte	1	0x00
0xF6	STRT_UP_IOUT_LIM	Read/write word	2	0x000F

REGISTER DETAILS

OPERATION REGISTER

Address: 0x01, Reset: 0x80, Name: OPERATION

This command requests the hot swap turn on and turn off. When turning the hot swap on, it clears status bits for any faults or warnings that are not active.

Table 14. Bit Descriptions for OPERATION

Bits	Bit Name	Settings	Description	Reset	Access
7	ON		Hot swap enable.	0x1	RW
		0	Hot swap output disabled.		
		1	Hot swap output enabled.		
[6:0]	RESERVED		Always reads as 0000000.	0x00	RESERVED

CLEAR FAULTS REGISTER

Address: 0x03, Send Byte, No Data, Name: CLEAR_FAULTS

This command clears fault and warning bits in all the status registers. Any faults that are still active are not cleared and remain set. Any warnings and the OT_FAULT that are generated by the power monitor are cleared, but may be asserted again if they remain active following the next power monitor conversion cycle.

This command does not require any data.

PMBUS CAPABILITY REGISTER

Address: 0x19, Reset: 0xB0, Name: CAPABILITY

Allows the host system to determine the SMBus interface capabilities of the device.

Table 15. Bit Descriptions for CAPABILITY

Bits	Bit Name	Settings	Description	Reset	Access
7	PEC_SUPPORT		Packet error correction (PEC) support.	0x1	R
		1	Always reads as 1. PEC is supported.		
[6:5]	MAX_BUS_SPEED		Maximum bus interface speed.	0x1	R
		01	Always reads as 01. Maximum supported bus speed is 400 kHz.		
4	SMBALERT_SUPPORT		SMBAlert support.	0x1	R
		1	Always reads as 1. Device supports SMBAlert and ARA.		
[3:0]	RESERVED		Always reads as 0000.	0x0	RESERVED

V_{OUT} OV WARNING LIMIT REGISTER

Address: 0x42, Reset: 0x0FFF, Name: VOUT_OV_WARN_LIMIT

This register sets the overvoltage warning limit for the voltage measured on the VOUT pin.

Table 16. Bit Descriptions for VOUT_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_OV_WARN_LIMIT		Overvoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0xFFF	RW

V_{OUT} UV WARNING LIMIT REGISTER

Address: 0x43, Reset: 0x0000, Name: VOUT_UV_WARN_LIMIT

This register sets the undervoltage warning limit for the voltage measured on the VOUT pin.

Table 17. Bit Descriptions for VOUT_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VOUT_UV_WARN_LIMIT		Undervoltage warning threshold for the VOUT pin measurement, expressed in direct format.	0x000	RW

I_{OUT} OC WARNING LIMIT REGISTER

Address: 0x4A, Reset: 0x0FFF, Name: IOUT_OC_WARN_LIMIT

This register sets the overcurrent warning limit for the current measured between the MO+ and the MO− pins.

Table 18. Bit Descriptions for IOUT_OC_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	IOUT_OC_WARN_LIMIT		Overcurrent warning threshold for the I_{OUT} measurement, expressed in direct format.	0xFFF	RW

OT FAULT LIMIT REGISTER

Address: 0x4F, Reset: 0x0FFF, Name: OT_FAULT_LIMIT

This register sets the overtemperature fault limit for the temperature measured on the TEMP pin.

Table 19. Bit Descriptions for OT_FAULT_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_FAULT_LIMIT		Overtemperature fault threshold for the TEMP pin measurement, expressed in direct format.	0xFFF	RW

OT WARNING LIMIT REGISTER

Address: 0x51, Reset: 0x0FFF, Name: OT_WARN_LIMIT

This register sets the overtemperature warning limit for the temperature measured on the TEMP pin.

Table 20. Bit Descriptions for OT_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	OT_WARN_LIMIT		Overtemperature warning threshold for the TEMP pin measurement, expressed in direct format.	0xFFF	RW

V_{IN} OV WARNING LIMIT REGISTER

Address: 0x57, Reset: 0x0FFF, Name: VIN_OV_WARN_LIMIT

This register sets the overvoltage warning limit for the voltage measured on the HS+ pin.

Table 21. Bit Descriptions for VIN_OV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_OV_WARN_LIMIT		Overvoltage warning threshold for the HS+ pin measurement, expressed in direct format.	0xFFF	RW

V_{IN} UV WARNING LIMIT REGISTER

Address: 0x58, Reset: 0x0000, Name: VIN_UV_WARN_LIMIT

This register sets the undervoltage warning limit for the voltage measured on the HS+ pin.

Table 22. Bit Descriptions for VIN_UV_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	VIN_UV_WARN_LIMIT		Undervoltage warning threshold for the HS+ pin measurement, expressed in direct format.	0x000	RW

P_{IN} OP WARNING LIMIT REGISTER

Address: 0x6B, Reset: 0x7FFF, Name: PIN_OP_WARN_LIMIT

This register sets the overpower warning limit for the power calculated based on $V_{IN} \times I_{OUT}$.

Table 23. Bit Descriptions for PIN_OP_WARN_LIMIT

Bits	Bit Name	Settings	Description	Reset	Access
15	RESERVED		Always reads as 0.	0x0	RESERVED
[14:0]	PIN_OP_WARN_LIMIT		Overpower warning threshold for the $V_{IN} \times I_{OUT}$ power calculation, expressed in direct format.	0x7FFF	RW

STATUS BYTE REGISTER

Address: 0x78, Reset: 0x00, Name: STATUS_BYTE

Provides status information for critical faults and certain top-level status commands in the device. This is also the lower byte returned by STATUS_WORD. A bit set to 1 indicates that a fault or warning has occurred.

Table 24. Bit Descriptions for STATUS_BYTE

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	HOTSWAP_OFF		Hot swap gate is off. This bit is live.	0x0	R
		0	The hot swap gate drive output is enabled.		
		1	The hot swap gate drive output is disabled, and the GATE pin is pulled down. This can be due to, for example, an overcurrent fault that causes the device to latch off, an undervoltage condition on the UV pin, or the use of the OPERATION command to turn the output off.		
5	RESERVED		Always reads as 0.	0x0	RESERVED
4	IOUT_OC_FAULT		I_{OUT} overcurrent fault. This bit is latched.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down.		
3	VIN_UV_FAULT		V_{IN} fault. This bit is latched.	0x0	R
		0	No undervoltage input fault detected on the UV pin.		
		1	An undervoltage input fault was detected on the UV pin.		
2	TEMP_FAULT		Temperature fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by STATUS_TEMPERATURE.		
		1	There are one or more active status bits to be read by STATUS_TEMPERATURE.		
1	CML_FAULT		CML fault. This bit is latched.	0x0	R
		0	No communications error detected on the I^2C/PMBus interface.		
		1	An error was detected on the I^2C/PMBus interface. Errors detected include an unsupported command, invalid PEC byte, and incorrectly structured message.		

Bits	Bit Name	Settings	Description	Reset	Access
0	NONEABOVE_STATUS		None of the above. This bit is live.	0x0	R
		0	No other active status bit reported by any other status command.		
		1	Active status bits are waiting to be read by one or more status commands.		

STATUS WORD REGISTER

Address: 0x79, Reset: 0x0000, Name: STATUS_WORD

Provides status information for critical faults and all top-level status commands in the device. The lower byte is also returned by STATUS_BYTE.

Table 25. Bit Descriptions for STATUS_WORD

Bits	Bit Name	Settings	Description	Reset	Access
15	VOUT_STATUS		V_{OUT} warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by the STATUS_VOUT register.		
		1	There are one or more active status bits to be read by STATUS_VOUT.		
14	IOUT_STATUS		I_{OUT} fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by the STATUS_IOUT register.		
		1	There are one or more active status bits to be read by the STATUS_IOUT register.		
13	INPUT_STATUS		Input warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by the STATUS_INPUT register.		
		1	There are one or more active status bits to be read by STATUS_INPUT.		
12	MFR_STATUS		Manufacture specific fault or warning. This bit is live.	0x0	R
		0	There are no active status bits to be read by the STATUS_MFR_SPECIFIC register.		
		1	There are one or more active status bits to be read by STATUS_MFR_SPECIFIC register.		
11	PGB_STATUS		Power is not good. This bit is live.	0x0	R
		0	Output power is good. The voltage on the PWGIN pin is above the threshold.		
		1	Output power is bad. The voltage on the PWGIN pin is below the threshold.		
[10:9]	RESERVED			0x0	RESERVED
8	FET_HEALTH_FAULT		FET health fault. This bit is latched.	0x0	R
		0	No FET faults have been detected.		
		1	A fault condition has been detected on the FET.		
7	RESERVED		Always set to 0.	0x0	RESERVED
6	HOTSWAP_OFF		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
5	RESERVED		Always set to 0.	0x0	RESERVED
4	IOUT_OC_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
3	VIN_UV_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
2	TEMP_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
1	CML_FAULT		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R
0	NONEABOVE_STATUS		Duplicate of corresponding bit in the STATUS_BYTE register.	0x0	R

V_{OUT} STATUS REGISTER

Address: 0x7A, Reset: 0x00, Name: STATUS_VOUT

Provides status information for warnings related to V_{OUT}.

Table 26. Bit Descriptions for STATUS_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
7	RESERVED		Always reads as 0.	0x0	RESERVED
6	VOUT_OV_WARN		V_{OUT} Overvoltage Warning.	0x0	R
		0	No overvoltage condition on the output supply detected by the power monitor.		
		1	An overvoltage condition on the output supply was detected by the power monitor. This bit is latched.		
5	VOUT_UV_WARN		V_{OUT} UV warning.	0x0	R
		0	No undervoltage condition on the output supply detected by the power monitor.		
		1	An undervoltage condition on the output supply was detected by the power monitor. This bit is latched.		
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

I_{OUT} STATUS REGISTER

Address: 0x7B, Reset: 0x00, Name: STATUS_IOUT

Provides status information for faults and warnings related to I_{OUT}.

Table 27. Bit Descriptions for STATUS_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
7	IOUT_OC_FAULT		I_{OUT} overcurent fault.	0x0	R
		0	No overcurrent output fault detected.		
		1	The hot swap controller detected an overcurrent condition and the time limit set by the capacitor on the TIMER pin has elapsed, causing the hot swap gate drive to shut down. This bit is latched.		
6	RESERVED		Always reads as 0.	0x0	RESERVED
5	IOUT_OC_WARN		I_{OUT} overcurrent warning.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command. This bit is latched.		
[4:0]	RESERVED		Always reads as 00000.	0x00	RESERVED

INPUT STATUS REGISTER

Address: 0x7C, Reset: 0x00, Name: STATUS_INPUT

Provides status information for faults and warnings related to V_{IN} and P_{IN}.

Table 28. Bit Descriptions for STATUS_INPUT

Bits	Bit Name	Settings	Description	Reset	Access
7	VIN_OV_FAULT		V_{IN} overvoltage fault.	0x0	R
		0	No overvoltage detected on the OV pin.		
		1	An overvoltage was detected on the OV pin. This bit is latched.		
6	VIN_OV_WARN		V_{IN} overvoltage warning fault.	0x0	R
		0	No overvoltage condition on the input supply detected by the power monitor.		
		1	An overvoltage condition on the input supply was detected by the power monitor. This bit is latched.		

Bits	Bit Name	Settings	Description	Reset	Access
5	VIN_UV_WARN		V_{IN} undervoltage warning.	0x0	R
		0	No undervoltage condition on the input supply detected by the power monitor.		
		1	An undervoltage condition on the input supply was detected by the power monitor. This bit is latched.		
4	VIN_UV_FAULT		V_{IN} undervoltage fault.	0x0	R
		0	No undervoltage detected on the UV pin.		
		1	An undervoltage was detected on the UV pin. This bit is latched.		
[3:1]	RESERVED		Always reads as 000.	0x0	RESERVED
0	PIN_OP_WARN		P_{IN} overpower warning.	0x0	R
		0	No overpower condition on the input supply detected by the power monitor.		
		1	An overpower condition on the input supply was detected by the power monitor. This bit is latched.		

TEMPERATURE STATUS REGISTER

Address: 0x7D, Reset: 0x00, Name: STATUS_TEMPERATURE

Provides status information for faults and warnings related to temperature.

Table 29. Bit Descriptions for STATUS_TEMPERATURE

Bits	Bit Name	Settings	Description	Reset	Access
7	OT_FAULT		Overtemperature fault.	0x0	R
		0	No overtemperature fault detected by the ADC.		
		1	An overtemperature fault was detected by the ADC. This bit is latched.		
6	OT_WARNING		Overtemperature warning.	0x0	R
		0	No overtemperature warning detected by the ADC.		
		1	An overtemperature warning was detected by the ADC. This bit is latched.		
[5:0]	RESERVED		Always reads as 000000.	0x0	RESERVED

MANUFACTURER SPECIFIC STATUS REGISTER

Address: 0x80, Reset: 0x00, Name: STATUS_MFR_SPECIFIC

Provides status information for manufacturer specific faults and warnings.

Table 30. Bit Descriptions for STATUS_MFR_SPECIFIC

Bits	Bit Name	Settings	Description	Reset	Access
7	FET_HEALTH_FAULT		FET health fault.	0x0	R
		0	No FET health problems have been detected.		
		1	An FET health fault has been detected. This bit is latched.		
6	UV_CMP_OUT		UV input comparator fault output.	0x0	R
		0	Input voltage to UV pin is above threshold.		
		1	Input voltage to UV pin is below threshold. This bit is live.		
5	OV_CMP_OUT		OV input comparator fault output.	0x0	R
		0	Input voltage to OV pin is below threshold.		
		1	Input voltage to OV pin is above threshold. This bit is live.		
4	SEVERE_OC_FAULT		Severe overcurrent fault.	0x0	R
		0	A severe overcurrent has not been detected by the hot swap.		
		1	A severe overcurrent has been detected by the hot swap. This bit is latched.		

Bits	Bit Name	Settings	Description	Reset	Access
3	HS_INLIM_FAULT		Hot swap in limit fault.	0x0	R
		0	The hot swap has not actively limited the current into the load.		
		1	The hot swap has actively limited current into the load. This bit differs from the IOUT_OC_FAULT bit in that the HS_INLIM_FAULT bit is set immediately, whereas the IOUT_OC_FAULT bit is not set unless the time limit set by the capacitor on the TIMER pin elapses. This bit is latched.		
[2:0]	HS_SHUTDOWN_CAUSE		Cause of last hot swap shutdown. This bit is latched until the status registers are cleared.	0x0	R
		000	The hot swap is either enabled and working correctly, or has been shut down using the OPERATION command.		
		001	An OT_FAULT condition occurred that caused the hot swap to shut down.		
		010	An IOUT_OC_FAULT condition occurred that caused the hot swap to shut down.		
		011	An FET_HEALTH_FAULT condition occurred that caused the hot swap to shut down.		
		100	A VIN_UV_FAULT condition occurred that caused the hot swap to shut down.		
		110	A VIN_OV_FAULT condition occurred that caused the hot swap to shut down.		

READ E_{IN} REGISTER

Address: 0x86, Reset: 0x000000000000, Name: READ_EIN

Read the energy metering registers in a single operation to ensure time consistent data.

Table 31. Bit Descriptions for READ_EIN

Bits	Bit Name	Settings	Description	Reset	Access
[47:24]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 5 is the high byte, Byte 4 is the middle byte, and Byte 3 is the low byte.	0x000000	R
[23:16]	ROLLOVER_COUNT		Number of times that the energy count has rolled over from 0x7FFF to 0x0000. This is an unsigned 8-bit binary value.	0x00	R
[15:0]	ENERGY_COUNT		Energy accumulator value in PMBus direct format. Byte 1 is the high byte, and Byte 0 is the low byte. Internally, the energy accumulator is a 24-bit value, but only the most significant 16 bits are returned with this command. Use the READ_EIN_EXT register to access the nontruncated version.	0x0000	R

READ V_{IN} REGISTER

Address: 0x88, Reset: 0x0000, Name: READ_VIN

Reads the input voltage, V_{IN}, from the device.

Table 32. Bit Descriptions for READ_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VIN		Input voltage from the HS+ pin measurement after averaging, expressed in direct format.	0x000	R

READ V_{OUT} REGISTER

Address: 0x8B, Reset: 0x0000, Name: READ_VOUT

Reads the output voltage, V_{OUT}, from the device.

Table 33. Bit Descriptions for READ_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_VOUT		Input voltage from the VOUT pin measurement after averaging, expressed in direct format.	0x000	R

READ I_{OUT} REGISTER

Address: 0x8C, Reset: 0x0000, Name: READ_IOUT

Reads the output current, I_{OUT}, from the device.

Table 34. Bit Descriptions for READ_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_IOUT		Output current derived from MO+/MO− sense pin voltage measurement after averaging, expressed in direct format.	0x000	R

READ TEMPERATURE 1 REGISTER

Address: 0x8D, Reset: 0x0000, Name: READ_TEMPERATURE_1

Reads the temperature measured by the device.

Table 35. Bit Descriptions for READ_TEMPERATURE_1

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	READ_TEMPERATURE_1		Temperature from the TEMP pin measurement after averaging, expressed in direct format.	0x000	R

READ P_{IN} REGISTER

Address: 0x97, Reset: 0x0000, Name: READ_PIN

Reads the calculated input power, P_{IN}, from the device.

Table 36. Bit Descriptions for READ_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	READ_PIN		Input power calculation, using $V_{IN} \times I_{OUT}$, after averaging, expressed in PMBus direct format. P_{IN} values are calculated for each $V_{IN} \times I_{OUT}$ sample, all P_{IN} values are then averaged before the value is returned to the READ_PIN register.	0x0000	R

PMBUS REVISION REGISTER

Address: 0x98, Reset: 0x22, Name: PMBUS_REVISION

Allows the system to read the PMBus revision that the device supports.

Table 37. Bit Descriptions for PMBUS_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	PMBUS_P1_REVISION	0010	PMBus Part I Support. Revision 1.2.	0x2	R
[3:0]	PMBUS_P2_REVISION	0010	PMBus Part II Support. Revision 1.2.	0x2	R

MANUFACTURER ID REGISTER

Address: 0x99, Reset: ASCII = ADI, Name: MFR_ID

Returns a string identifying the Manufacturer of the device.

Table 38. Bit Descriptions for MFR_ID

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	MFR_ID		String identifying manufacturer as Analog Devices (ADI).	0x494441	R

MANUFACTURER MODEL REGISTER

Address: 0x9A, Reset: ASCII = ADM1278-xy, Name: MFR_MODEL

Returns a string identifying the specific model of the device.

Table 39. Bit Descriptions for MFR_MODEL

Bits	Bit Name	Settings	Description	Reset	Access
[79:0]	MFR_MODEL		String identifying model as ADM1278-xy, where xy identifies the particular model type. Note that the ADM1278-1AA model is identified as ADM1278-1A in the MFR_MODEL register.	0x41312D383732314D4441	R

MANUFACTURER REVISION REGISTER

Address: 0x9B, Reset: 0x33, Name: MFR_REVISION

Returns a string identifying the hardware revision of the device.

Table 40. Bit Descriptions for MFR_REVISION

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	MFR_REVISION		String identifying hardware revision as, for example, 3.	0x33	R

MANUFACTURER DATE REGISTER

Address: 0x9D, Reset: ASCII = YYMMDD, Name: MFR_DATE

Returns a string identifying the production test date of the device.

Table 41. Bit Descriptions for MFR_DATE

Bits	Bit Name	Settings	Description	Reset	Access
[47:0]	DATE		String identifying test date, in the form of YYMMDD.	0x313338303231	R

PEAK I_{OUT} REGISTER

Address: 0xD0, Reset: 0x0000, Name: PEAK_IOUT

Reports the peak output current, I_{OUT}. Writing 0x0000 with this command resets the peak value.

Table 42. Bit Descriptions for PEAK_IOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_IOUT		Peak output current measurement, I_{OUT}, expressed in direct format.	0x000	R

PEAK V_{IN} REGISTER

Address: 0xD1, Reset: 0x0000, Name: PEAK_VIN

Reports the peak input voltage, V_{IN}. Writing 0x0000 with this command resets the peak value.

Table 43. Bit Descriptions for PEAK_VIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VIN		Peak input voltage measurement, V_{IN}, expressed in direct format.	0x000	R

PEAK V_{OUT} REGISTER

Address: 0xD2, Reset: 0x0000, Name: PEAK_VOUT

Reports the peak output voltage, V_{OUT}. Writing 0x0000 with this command resets the peak value.

Table 44. Bit Descriptions for PEAK_VOUT

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_VOUT		Peak output voltage measurement, V_{OUT}, expressed in direct format.	0x000	R

POWER MONITOR CONTROL REGISTER

Address: 0xD3, Reset: 0x01, Name: PMON_CONTROL

This command starts and stops the power monitor.

Table 45. Bit Descriptions for PMON_CONTROL

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Always reads as 0000000.	0x00	RESERVED
0	CONVERT		Conversion enable.	0x1	RW
		0	Power monitor is not running.		
		1	Power monitor is sampling. Default. In single shot mode, this bit clears itself after one complete cycle. In continuous mode, this bit must be written to 0 to stop sampling. A rising edge on the conversion input (CONV function of Pin 13) or a falling edge on $\overline{\text{SPI_SS}}$ sets this bit to 1. During sampling, additional conversion edges on these pins are ignored.		

POWER MONITOR CONFIGURATION REGISTER

Address: 0xD4, Reset: 0x0714, Name: PMON_CONFIG

This command configures the power monitor. Different combinations of channels can be included in the rotational sampling, and averaging can be set for different measurements.

Table 46. Bit Descriptions for PMON_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	TSFILT		Temperature sensor filter enable.	0x0	RW
		0	Disabled.		
		1	Enabled. Data sheet specifications are with the temperature sensor filter disabled.		
14	SIMULTANEOUS		Simultaneous sampling.	0x0	RW
		0	Disabled.		
		1	Enabled. Power monitoring accuracy is reduced. Data sheet specifications are with simultaneous sampling disabled.		

Bits	Bit Name	Settings	Description	Reset	Access
[13:11]	PWR_AVG		P_{IN} averaging.	0x0	RW
		000	Disables sample averaging for power.		
		001	Sets sample averaging for power to two samples.		
		010	Sets sample averaging for power to four samples.		
		011	Sets sample averaging for power to eight samples.		
		100	Sets sample averaging for power to 16 samples.		
		101	Sets sample averaging for power to 32 samples.		
		110	Sets sample averaging for power to 64 samples.		
		111	Sets sample averaging for power to 128 samples.		
[10:8]	VI_AVG		$V_{IN}/V_{OUT}/I_{OUT}$ averaging.	0x7	RW
		000	Disables sample averaging for current and voltage.		
		001	Sets sample averaging for current and voltage to two samples.		
		010	Sets sample averaging for current and voltage to four samples.		
		011	Sets sample averaging for current and voltage to eight samples.		
		100	Sets sample averaging for current and voltage to 16 samples.		
		101	Sets sample averaging for current and voltage to 32 samples.		
		110	Sets sample averaging for current and voltage to 64 samples.		
		111	Sets sample averaging for current and voltage to 128 samples.		
[7:5]	RESERVED		Always reads as 000.	0x0	RESERVED
4	PMON_MODE		Conversion mode.	0x1	RW
		0	Single shot sampling.		
		1	Continuous sampling.		
3	TEMP1_EN		Enable temperature sampling.	0x0	RW
		0	Temperature sampling disabled.		
		1	Temperature sampling enabled.		
2	VIN_EN		Enable V_{IN} sampling.	0x1	RW
		0	V_{IN} sampling disabled.		
		1	V_{IN} sampling enabled.		
1	VOUT_EN		Enable V_{OUT} sampling.	0x0	RW
		0	V_{OUT} sampling disabled.		
		1	V_{OUT} sampling enabled.		
0	RESERVED		Always reads as 0.	0x0	RESERVED

ALERT 1 CONFIGURATION REGISTER

Address: 0xD5, Reset: 0x0000, Name: ALERT1_CONFIG

This commands allows different combinations of faults and warnings to be configured on the GPO1 output of the GPO1/$\overline{\text{ALERT1}}$/CONV pin. The pin can operate in different modes, configured using the DEVICE_CONFIG command.

Table 47. Bit Descriptions for ALERT1_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_FAULT_EN1		FET health fault enable.	0x0	RW
14	IOUT_OC_FAULT_EN1		I_{OUT} overcurrent fault enable.	0x0	RW
13	VIN_OV_FAULT_EN1		V_{IN} overvoltage fault enable.	0x0	RW
12	VIN_UV_FAULT_EN1		V_{IN} undervoltage fault enable.	0x0	RW
11	CML_ERROR_EN1		Communications error enable.	0x0	RW
10	IOUT_OC_WARN_EN1		I_{OUT} overcurrent warning enable.	0x0	RW
9	HYSTERETIC_EN1		Hysteretic output enable.	0x0	RW
8	VIN_OV_WARN_EN1		V_{IN} overvoltage warning enable.	0x0	RW
7	VIN_UV_WARN_EN1		V_{IN} undervoltage warning enable.	0x0	RW
6	VOUT_OV_WARN_EN1		V_{OUT} overvoltage warning enable.	0x0	RW
5	VOUT_UV_WARN_EN1		V_{OUT} undervoltage warning enable.	0x0	RW
4	HS_INLIM_EN1		Hot swap in-limit enable.	0x0	RW

Bits	Bit Name	Settings	Description	Reset	Access
3	PIN_OP_WARN_EN1		P_{IN} overpower warning enable.	0x0	RW
2	OT_FAULT_EN1		Overtemperature fault enable.	0x0	RW
1	OT_WARN_EN1		Overtemperature warning enable.	0x0	RW
0	RESERVED		Always reads as 0.	0x0	RESERVED

ALERT 2 CONFIGURATION REGISTER

Address: 0xD6, Reset: 0x0000, Name: ALERT2_CONFIG

This commands allows different combinations of faults and warnings to be configured on the GPO2 output of the GPO2/$\overline{\text{ALERT2}}$ pin. The pin can operate in different modes, configured using the DEVICE_CONFIG command.

Table 48. Bit Descriptions for ALERT2_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
15	FET_HEALTH_FAULT_EN2		FET health fault enable.	0x0	RW
14	IOUT_OC_FAULT_EN2		I_{OUT} overcurrent fault enable.	0x0	RW
13	VIN_OV_FAULT_EN2		V_{IN} overvoltage fault enable.	0x0	RW
12	VIN_UV_FAULT_EN2		V_{IN} undervoltage fault enable.	0x0	RW
11	CML_ERROR_EN2		Communications error enable.	0x0	RW
10	IOUT_OC_WARN_EN2		I_{OUT} overcurrent warning enable.	0x0	RW
9	HYSTERETIC_EN2		Hysteretic output enable.	0x0	RW
8	VIN_OV_WARN_EN2		V_{IN} overvoltage warning enable.	0x0	RW
7	VIN_UV_WARN_EN2		V_{IN} undervoltage warning enable.	0x0	RW
6	VOUT_OV_WARN_EN2		V_{OUT} overvoltage warning enable.	0x0	RW
5	VOUT_UV_WARN_EN2		V_{OUT} undervoltage warning enable.	0x0	RW
4	HS_INLIM_EN2		Hot swap in-limit enable.	0x0	RW
3	PIN_OP_WARN_EN2		P_{IN} overpower warning enable.	0x0	RW
2	OT_FAULT_EN2		Overtemperature fault enable.	0x0	RW
1	OT_WARN_EN2		Overtemperature warning enable.	0x0	RW
0	RESERVED		Always reads as 0.	0x0	RESERVED

PEAK TEMPERATURE REGISTER

Address: 0xD7, Reset: 0x0000, Name: PEAK_TEMPERATURE

Reports the peak measured temperature. Writing 0x0000 with this command resets the peak value.

Table 49. Bit Descriptions for PEAK_TEMPERATURE

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
[11:0]	PEAK_TEMPERATURE		Peak temperature measurement, expressed in direct format.	0x000	R

DEVICE CONFIGURATION REGISTER

Address: 0xD8, Reset: 0x000D, Name: DEVICE_CONFIG

This command configures the hot swap overcurrent threshold and filtering, and GPO1/GPO2 output modes. Note that dual function pin names are referenced by the relevant function only, for example, GPO2 for the general-purpose output function of the GPO2/$\overline{\text{ALERT2}}$ pin (see the Pin Configurations and Function Descriptions section for full pin mnemonics and descriptions).

Table 50. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Settings	Description	Reset	Access
[15:12]	RESERVED		Always reads as 0000.	0x0	RESERVED
11	FHDIS		FET health disable.	0x0	RW
		0	FET health checks enabled.		
		1	FET health checks disabled.		

Bits	Bit Name	Settings	Description	Reset	Access
10	PWR_HYST_EN		When enabled, the general-purpose output alert hysteresis functions refer to power rather than current. The HYSTERETIC_ENx bit also needs to be set in ALERT_CONFIG.	0x0	RW
		0	Current hysteresis mode.		
		1	Power hysteresis mode.		
[9:8]	GPO2_MODE		GPO2 configuration mode.	0x0	RW
		00	Default. GPO2 is configured to generate SMBAlerts.		
		01	GPO2 can be used as a general-purpose digital output pin. Use the GPO2_INVERT bit to change the output state.		
		10	Reserved.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.		
7	GPO2_INVERT		GPO2 invert mode.	0x0	RW
		0	In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.		
		1	In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.		
[6:5]	GPO1_MODE		GPO1 configuration mode.	0x0	RW
		00	Default. GPO1 is configured to generate SMBAlerts.		
		01	GPO1 can be used as a general-purpose digital output pin. Use the GPO1_INVERT bit to change the output state.		
		10	GPO1 is configured as a convert (CONV) input pin.		
		11	This is digital comparator mode. The output pin now reflects the live status of the warning or fault bit selected for the output. In effect, this is a nonlatched SMBAlert.		
4	GPO1_INVERT		GPO1 invert mode.	0x0	RW
		0	In SMBAlert mode, the output is not inverted, and active low. In GPO mode, the output is set low.		
		1	In SMBAlert mode, the output is inverted, and active high. In GPO mode, the output is set high.		
[3:2]	OC_TRIP_SELECT		Severe overcurrent threshold select.	0x11	RW
		00	125%.		
		01	150%.		
		10	200%.		
		11	Default, 225%.		
1	OC_RETRY_DIS		Severe OC retry mode.	0x0	RW
		0	Retry once immediately after severe overcurrent event.		
		1	Latch off after severe overcurrent event.		
0	OC_FILT_SELECT		Severe overcurrent filter select.	0x1	RW
		0	200 ns.		
		1	Default, 900 ns.		

POWER CYCLE REGISTER

Address: 0xD9, Send Byte, No Data, Name: POWER_CYCLE

This command is provided to allow a processor to request the hot swap to turn off and turn back on again approximately five seconds later. This is useful in the event that the hot swap output is powering the processor.

This command does not require any data.

PEAK P_{IN} REGISTER

Address: 0xDA, Reset: 0x0000, Name: PEAK_PIN

Reports the peak input power, P_{IN}. Writing 0x0000 with this command resets the peak value.

Table 51. Bit Descriptions for PEAK_PIN

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	PEAK_PIN		Peak input power calculation, P_{IN}, expressed in direct format.	0x0000	R

READ P_{IN} (EXTENDED) REGISTER

Address: 0xDB, Reset: 0x000000, Name: READ_PIN_EXT

Reads the extended precision version of the calculated input power, P_{IN}, from the device.

Table 52. Bit Descriptions for READ_PIN_EXT

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	READ_PIN_EXT		Extended precision version of peak input power calculation, P_{IN}, expressed in PMBus direct format.	0x000000	R

READ E_{IN} (EXTENDED) REGISTER

Address: 0xDC, Reset: 0x0000000000000000, Name: READ_EIN_EXT

Read the extended precision energy metering registers in a single operation to ensure time consistent data.

Table 53. Bit Descriptions for READ_EIN_EXT

Bits	Bit Name	Settings	Description	Reset	Access
[63:40]	SAMPLE_COUNT		This is the total number of P_{IN} samples acquired and accumulated in the energy count accumulator. This is an unsigned 24-bit binary value. Byte 7 is the high byte, Byte 6 is the middle byte, and Byte 5 is the low byte.	0x000000	R
[39:24]	ROLLOVER_EXT		Number of times that the energy count has rolled over from 0x7FFFFF to 0x000000. This is an unsigned 16-bit binary value. Byte 4 is the high byte, and Byte 3 is the low byte.	0x0000	R
[23:0]	ENERGY_EXT		Extended precision energy accumulator value in PMBus direct format. Byte 2 is the high byte, Byte 1 is the middle byte, and Byte 0 is the low byte.	0x000000	R

HYSTERESIS LOW LEVEL REGISTER

Address: 0xF2, Reset: 0x0000, Name: HYSTERESIS_LOW

This sets the lower threshold used to generate the hysteretic output signal, which can be made available on a general-purpose output pin.

Table 54. Bit Descriptions for HYSTERESIS_LOW

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	HYSTERESIS_LOW		Value setting the lower hysteresis threshold, expressed in direct format.	0x000	RW

HYSTERESIS HIGH LEVEL REGISTER

Address: 0xF3, Reset: 0xFFFF, Name: HYSTERESIS_HIGH

This sets the higher threshold used to generate the hysteretic output signal, which can be made available on a general-purpose output pin.

Table 55. Bit Descriptions for HYSTERESIS_HIGH

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	HYSTERESIS_HIGH		Value setting the higher hysteresis threshold, expressed in direct format.	0xFFFF	RW

HYSTERESIS STATUS REGISTER

Address: 0xF4, Reset: 0x00, Name: STATUS_HYSTERESIS

This status register reports whether the hysteretic comparison is above or below the user defined thresholds, and the IOUT_OC_WARNING status bit as well.

Table 56. Bit Descriptions for STATUS_HYSTERESIS

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Always reads as 0000.	0x0	RESERVED
3	IOUT_OC_WARN		I_{OUT} overcurrent warning.	0x0	R
		0	No overcurrent condition on the output supply detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
		1	An overcurrent condition was detected by the power monitor using the IOUT_OC_WARN_LIMIT command.		
2	HYST_STATE		Hysteretic comparison output.	0x0	R
		0	Comparison output low.		
		1	Comparison output high.		
1	HYST_GT_HIGH		Hysteretic upper threshold comparison.	0x0	R
		0	Compared value is below upper threshold.		
		1	Compared value is above upper threshold.		
0	HYST_LT_LOW		Hysteretic lower threshold comparison.	0x0	R
		0	Compared value is above lower threshold.		
		1	Compared value is below lower threshold.		

START-UP I_{OUT} LIMIT REGISTER

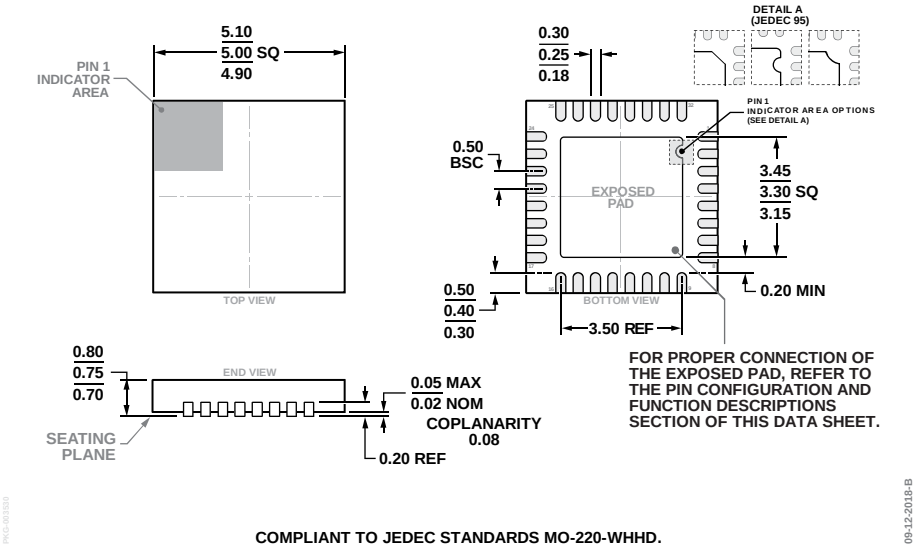
Address: 0xF6, Reset: 0x000F, Name: STRT_UP_IOUT_LIM

This sets the current limit initially used while the hot swap is turning on the FET.

Table 57. Bit Descriptions for STRT_UP_IOUT_LIM

Bits	Bit Name	Settings	Description	Reset	Access
[15:4]	RESERVED		Always reads as 0x00.	0x00	RESERVED
[3:0]	STRT_UP_IOUT_LIM		Current limit used during startup, expressed in direct format.	0xF	RW

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD.

Figure 74. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm Body and 0.75 mm Package Height
(CP-32-13)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADM1278-1AACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-1AACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-1ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-1ACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-1BCPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-1BCPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-2ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-2ACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-3ACPZ	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
ADM1278-3ACPZ-RL	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP]	CP-32-13
EVAL-ADM1278EBZ		Evaluation Kit	

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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