THE DATASHEET OF

ADM3101EARQZ

±15 kV ESD Protected, 3.3 V Single-Channel RS-232 Line Driver/Receiver

Data Sheet

ADM3101E

FEATURES

460 kbps data rate
1 Tx and 1 Rx
Meets EIA/TIA-232E specifications
0.1 µF charge pump capacitors
Contact discharge: ±8 kV
Air gap discharge: ±15 kV

APPLICATIONS

General-purpose RS-232 data links
Industrial/telecommunications diagnostics ports

FUNCTIONAL BLOCK DIAGRAM

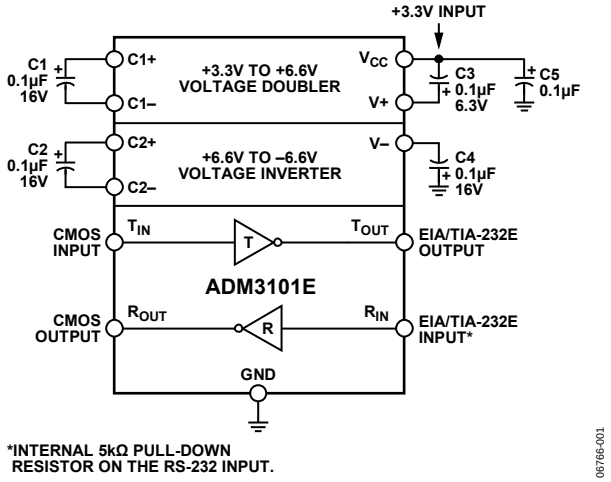

Figure 1.

GENERAL DESCRIPTION

The ADM3101E is a high speed, single-channel, RS-232/ITU-T V.28 transceiver interface device that operates from a single 3.3 V power supply. Low power consumption makes it ideal for battery-powered portable instruments.

The ADM3101E conforms to the EIA/TIA-232E and ITU-T V.28 specifications and operates at data rates of up to 460 kbps.

All RS-232 (T_{OUT} and R_{IN}) and CMOS (T_{IN} and R_{OUT}) inputs and outputs are protected against electrostatic discharges (up to ±15 kV ESD protection).

Because of the ±15 kV ESD protection of the ADM3101E input/output pins, this device is ideally suited for operation in electrically harsh environments or where RS-232 cables are frequently plugged and unplugged.

Four external 0.1 µF charge pump capacitors are used for the voltage doubler/inverter permitting operation from a single 3.3 V supply.

The ADM3101E is available in both a 12-lead LFCSP and 16-lead QSOP, specified over the −40°C to +85°C temperature range.

Rev. D Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
Technical Support **www.analog.com**

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5/07—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.3 V ± 0.3 V, C1 to C4 = 0.1 µF, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
DC CHARACTERISTICS					
Operating Voltage Range		3.0	3.3	5.5	V
Power Supply Current, V_{CC}	No load		1.5	2.6	mA
	R_L = 3 kΩ to GND		5	7	mA
LOGIC					
Input Logic Threshold Low, V_{INL}	T_{IN}			0.6	V
Input Logic Threshold High, V_{INH}	T_{IN}	1.4			V
Input Logic Threshold Low, V_{INL}	T_{IN}, V_{CC} = 5.0 V ± 0.5 V			0.8	V
Input Logic Threshold High, V_{INH}	T_{IN}, V_{CC} = 5.0 V ± 0.5 V	2.0			V
CMOS Output Voltage Low, V_{OL}	I_{OUT} = 1.6 mA			0.4	V
CMOS Output Voltage High, V_{OH}	I_{OUT} = −1 mA	V_{CC} − 0.6			V
Logic Pull-Up Current	T_{IN} = GND to V_{CC}		5	12	µA
RS-232 RECEIVER					
EIA/TIA-232E Input Voltage Range[1]		−30		+30	V
EIA/TIA-232E Input Threshold Low	V_{CC} = 3.0 V to 5.5 V	0.6	1.3		V
EIA/TIA-232E Input Threshold High			1.6	2.4	V
EIA/TIA-232E Input Hysteresis			0.4		V
EIA/TIA-232E Input Resistance		3	5	7	kΩ
TRANSMITTER					
Output Voltage Swing					
RS-232	V_{CC} = 3.3 V to 5.5 V; transmitter output loaded with 3 kΩ to ground	±5.0	±5.7		V
RS-562	V_{CC} = 3.0 V	±4.5			V
Transmitter Output Resistance	V_{CC} = 0 V, V_{OUT} = ±2 V[1]	300			Ω
RS-232 Output Short-Circuit Current			±15		mA
TIMING CHARACTERISTICS					
Maximum Data Rate	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ, C_L = 50 pF to 1000 pF	460			kbps
Receiver Propagation Delay					
t_{PHL}			0.4		µs
t_{PLH}			0.4		µs
Transmitter Propagation Delay	R_L = 3 kΩ, C_L = 1000 pF		600		ns
Transmitter Skew			80		ns
Receiver Skew			70		ns
Transition Region Slew Rate	+3 V to −3 V or −3 V to +3 V, V_{CC} = +3.3 V, R_L = 3 kΩ, C_L = 1000 pF, T_A = 25°C[1]	5.5	10	30	V/µs
ESD PROTECTION					
RS-232 and CMOS I/O Pins	Human body model air discharge		±15		kV
	Human body model contact discharge		±8		kV

[1] Guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

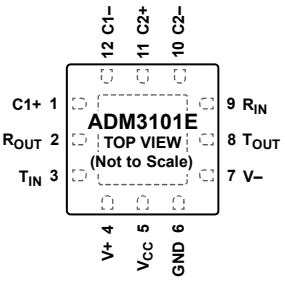
Parameter	Rating
V_{CC}	−0.3 V to +6 V
V+	(V_{CC} − 0.3 V) to +13 V
V−	+0.3 V to −13 V
Input Voltages	
T_{IN}	−0.3 V to (V_{CC} + 0.3 V)
R_{IN}	±30 V
Output Voltages	
T_{OUT}	±15 V
R_{OUT}	−0.3 V to (V_{CC} + 0.3 V)
Short-Circuit Duration	
T_{OUT}	Continuous
Package Information	
θ_{JA}, Thermal Impedance (LFCSP)	80°C/W
θ_{JA}, Thermal Impedance (QSOP)	149.97°C/W
Operating Temperature Range	
Industrial (A Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Pb-Free Temperature (Soldering, 10 sec)	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO GND. THIS CONNECTION IS NOT REQUIRED TO MEET ELECTRICAL PERFORMANCE.

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Figure 2. LFCSP Pin Configuration

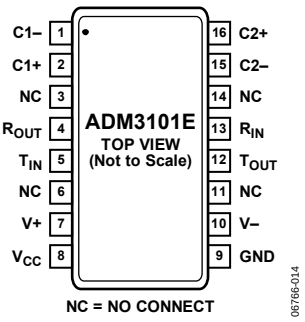

Figure 3. QSOP Pin Configuration

Table 3. Pin Function Descriptions

Pin No.[1]			
LFCSP	**QSOP**	**Mnemonic**	**Description**
1, 12	2, 1	C1+, C1−	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C1 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used.
2	4	R_{OUT}	Receiver Output. This pin outputs CMOS output logic levels.
3	5	T_{IN}	Transmitter (Driver) Input. This input accepts TTL/CMOS levels.
4	7	V+	Internally Generated Positive Supply (+6 V Nominal).
5	8	V_{CC}	Power Supply Input, 3.0 V to 5.5 V.
6	9	GND	Ground. Must be connected to 0 V.
7	10	V−	Internally Generated Negative Supply (−6 V Nominal).
8	12	T_{OUT}	Transmitter (Driver) Output. This pin outputs RS-232 signal levels (typically ±6 V).
9	13	R_{IN}	Receiver Input. This input accepts RS-232 signal levels. An internal 5 kΩ pull-down resistor to GND is connected on the input.
10, 11	15, 16	C2−, C2+	Positive and Negative Connections for Charge Pump Capacitor. External Capacitor C2 is connected between these pins; a 0.1 µF capacitor is recommended, but larger capacitors up to 10 µF can be used.
N/A	3, 6, 11, 14	NC	No Connect. These pins should always remain unconnected.
EPAD	N/A	EPAD	Exposed Pad. The exposed pad must be connected to GND. This connection is not required to meet electrical performance.

[1] N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

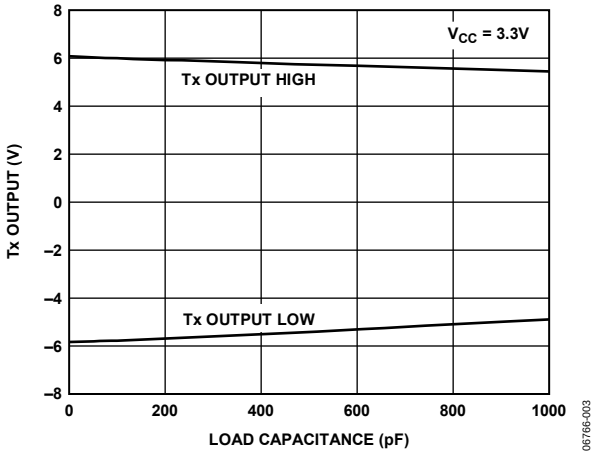

Figure 4. Transmitter Output Voltage High/Low vs. Load Capacitance @ 460 kbps

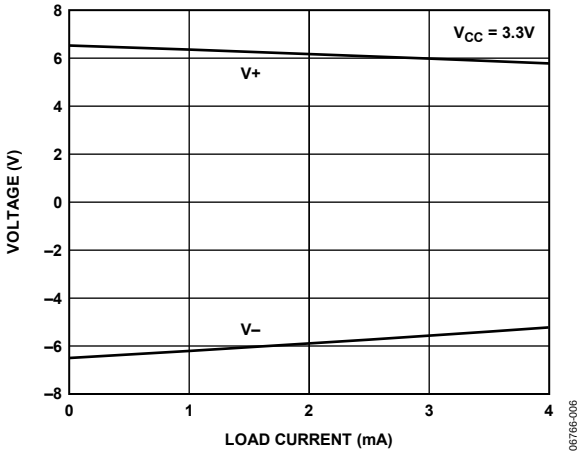

Figure 7. Charge Pump V+, V– vs. Load Current

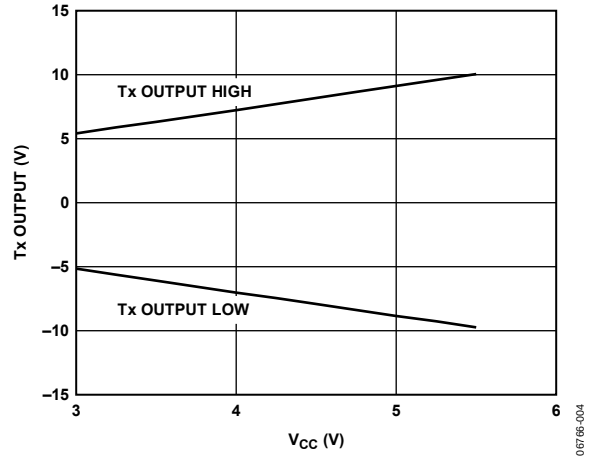

Figure 5. Transmitter Output Voltage High/Low vs. V_{CC}, R_L = 3 kΩ

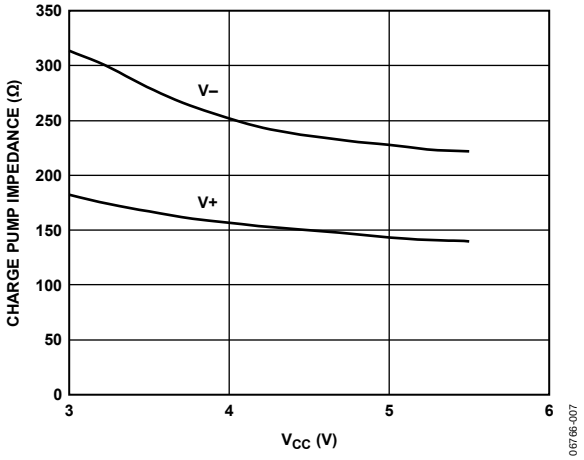

Figure 8. Charge Pump Impedance vs. V_{CC}

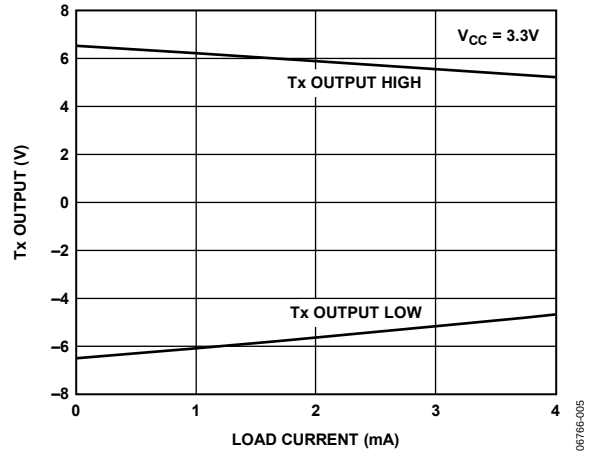

Figure 6. Transmitter Output Voltage High/Low vs. Load Current

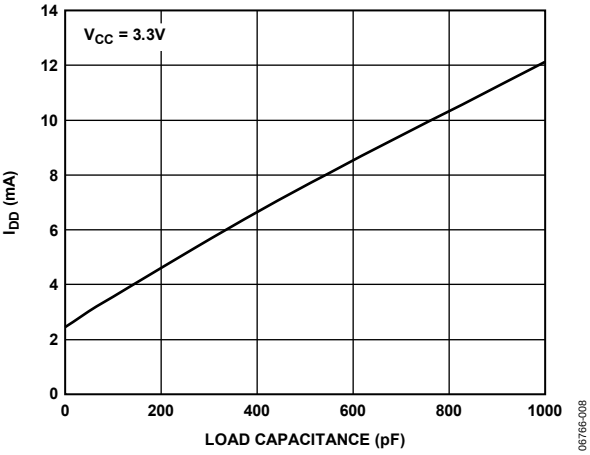

Figure 9. Power Supply Current vs. Load Capacitance

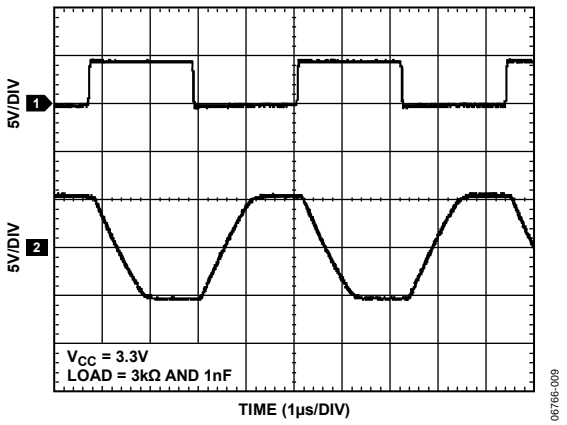

Figure 10. 460 kbps Data Transmission

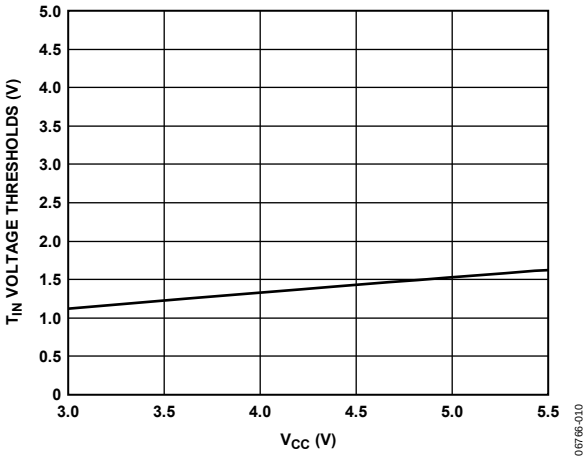

Figure 11. T_{IN} Voltage Threshold vs. V_{CC}

THEORY OF OPERATION

The ADM3101E is a single-channel RS-232 line driver/receiver. Step-up voltage converters, coupled with level shifting transmitters and receivers, allow RS-232 levels to be developed while operating from a single 3.3 V supply.

CMOS technology is used to keep the power dissipation to an absolute minimum, allowing maximum battery life in portable applications.

CIRCUIT DESCRIPTION

The internal circuitry consists of the following main sections:

- A charge pump voltage converter
- A 3.3 V logic to an EIA/TIA-232E transmitter
- An EIA/TIA-232E to a 3.3 V logic receiver

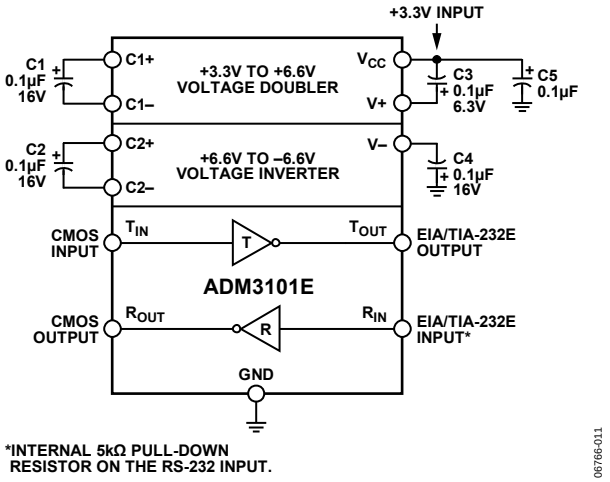

Figure 12. Typical Operating Circuit

Charge Pump Voltage Converter

The charge pump voltage converter consists of a 200 kHz oscillator and a switching matrix. The converter generates a ±6.6 V supply (when unloaded) from the 3.3 V input level. This is achieved in two stages by using a switched capacitor technique, as illustrated in Figure 13 and Figure 14. First, the 3.3 V input supply is doubled to +6.6 V by using C1 as the charge storage element. The +6.6 V level is then inverted to generate −6.6 V using C2 as the storage element. C3 is shown connected between V+ and V_{CC} but is equally effective if connected between V+ and GND.

The C3 and C4 capacitors are used to reduce the output ripple. The values are not critical and can be increased, if desired. Larger capacitors (up to 10 µF) can also be used in place of the C1, C2, C3, and C4 capacitors.

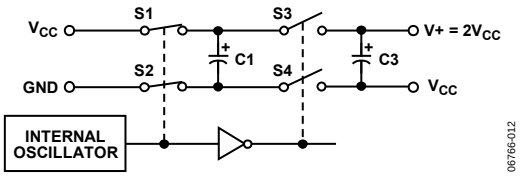

Figure 13. Charge Pump Voltage Doubler

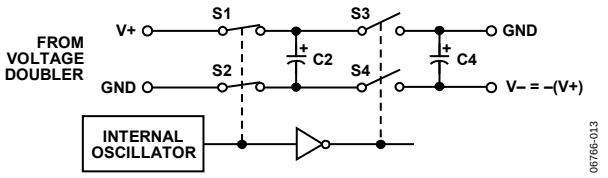

Figure 14. Charge Pump Voltage Inverter

3.3 V Logic to EIA/TIA-232E Transmitter

The transmitter driver converts the 3.3 V logic input levels into RS-232 output levels. When driving an RS-232 load with V_{CC} = 3.3 V, the output voltage swing is typically ±6 V. Internally, the T_{IN} pin has a weak pull-up that allows it to be driven by an open-drain output, but the maximum operating data rate is reduced when the T_{IN} pin is driven by an open-drain pin.

EIA/TIA-232E to 3.3 V Logic Receiver

The receiver is an inverting level shifter that accepts the RS-232 input level and translates it into a 3.3 V logic output level. The input has an internal 5 kΩ pull-down resistor to ground and is protected against overvoltages of up to ±30 V. An unconnected input is pulled to 0 V by the internal 5 kΩ pull-down resistor, which, therefore, results in a Logic 1 output level for an unconnected input or for an input connected to GND.

The receiver has a Schmitt trigger input with a hysteresis level of 0.4 V, which ensures error-free reception for both a noisy input and for an input with slow transition times.

CMOS Input Voltage Thresholds

The CMOS input and output pins (T_{IN} and R_{OUT}) of the ADM3101E are designed to interface with 1.8 V logic thresholds when V_{CC} = 3.3 V.

The CMOS input and output pins (T_{IN} and R_{OUT}) of the ADM3101E are also designed to interface with TTL/CMOS logic thresholds when V_{CC} = 5 V.

ESD Protection on RS-232 and CMOS I/O Pins

All RS-232 (T_{OUT} and R_{IN}) and CMOS (T_{IN} and R_{OUT}) inputs and outputs are protected against electrostatic discharges (up to ±15 kV).

HIGH BAUD RATE

The ADM3101E features high slew rates, permitting data transmission at rates well in excess of the EIA/RS-232 specifications. The RS-232 voltage levels are maintained at data rates of up to 460 kbps, even under worst-case loading conditions, when T_{IN} is driven by a push-pull output. The slew rate is internally controlled to less than 30 V/µs to minimize EMI interference.

OUTLINE DIMENSIONS

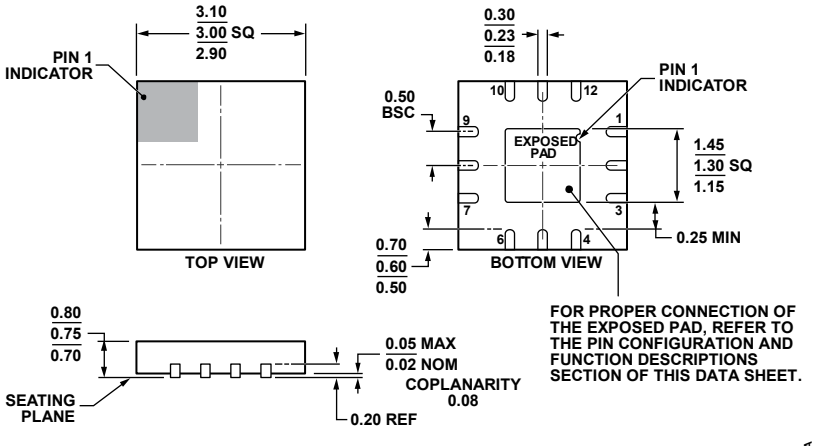

Figure 15. 12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
3 mm × 3 mm Body, Very Very Thin Quad
(CP-12-4)
Dimensions shown in millimeters

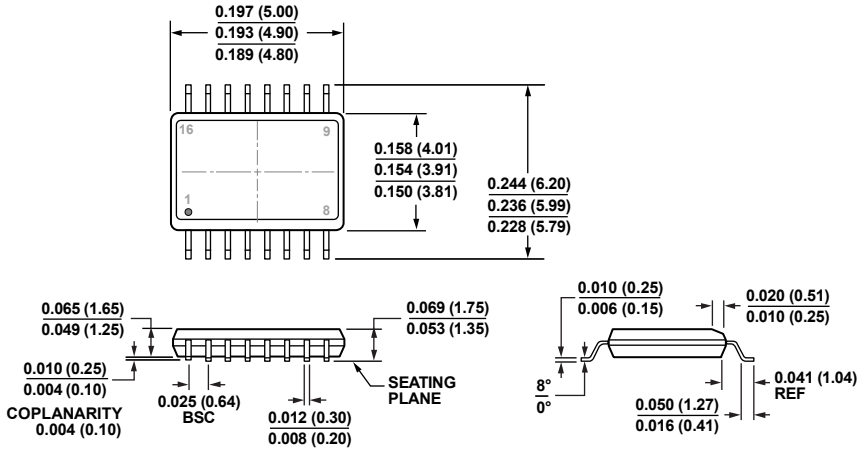

Figure 16. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
ADM3101EACPZ-REEL	−40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-12-4	MA6
ADM3101EACPZ-250R7	−40°C to +85°C	12-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-12-4	MA6
ADM3101EARQZ	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	
ADM3101EARQZ-REEL	−40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	

[1] Z = RoHS Compliant Part.

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