



**THE DATASHEET OF
ADM6315-26D2ART-RL**



FEATURES

- Specified over temperature
- Low power consumption (5 μ A typical)
- Precision voltage monitor of voltages from 2.5 V to 5 V at 100 mV increments
- Reset assertion down to $V_{CC} > 1$ V
- Reset timeout periods: 1 ms, 20 ms, 140 ms, or 1120 ms (minimum)
- Built-in manual reset
- Pin compatible with the ADM811
- Available in SOT-143 package

APPLICATIONS

- Microprocessor systems
- Controllers
- Intelligent instruments
- Automotive systems
- Safety systems
- Portable instruments

GENERAL DESCRIPTION

The **ADM6315** is a reliable voltage monitoring device that is suitable for use in most voltage monitoring applications.

The **ADM6315** is designed to monitor as little as a 1.8% degradation of a power supply voltage. The **ADM6315** can monitor all voltages (at 100 mV increments) from 2.5 V to 5 V.

Included in this circuit is a debounced manual reset input. $\overline{\text{RESET}}$ can be activated using an ordinary switch (pulling $\overline{\text{MR}}$ low), a low input from another digital device, or a degradation of the supply voltage.

FUNCTIONAL BLOCK DIAGRAM



Figure 1.



Figure 2. Typical Operating Circuit

The manual reset function is very useful, especially if the circuit in which the **ADM6315** is operating enters into a state that can be detected only by the user. Allowing the user to reset a system manually can reduce the damage or danger that could otherwise be caused by an out of control or locked up system.

The **ADM6315** is available in a cost efficient and space efficient SOT-143 package.

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REVISION HISTORY

11/2018—Rev. G to Rev. H

Change to Features Section	1
Deleted Automotive Products Section	8
Changes to Ordering Guide	8

9/2013—Rev. F to Rev. G

Changed Date in Revision F Revision History	2
Updated Outline Dimensions	8

12/2011—Rev. E to Rev. F

Added Automotive Part	Universal
Changes to Ordering Guide	8

9/2007—Rev. D to Rev. E

Changes to Absolute Maximum Ratings	4
Updated Outline Dimensions	8
Changes to Ordering Guide	8

4/2006—Rev. C to Rev. D

Updated Format	Universal
Updated Outline Dimensions	8
Changes to Ordering Guide	8

12/2003—Rev. B to Rev. C

Edit to Absolute Maximum Ratings	3
Edits to Ordering Guide	4
Deleted Table I and Table II	6
Deleted Table III and Table IV	7
Updated Outline Dimensions	8

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2/2003—Rev. A to Rev. B

Edits to Features	1
Edits to Specifications	2
Edits to Absolute Maximum Ratings	3
Edits to Ordering Guide	3
Edits to Table I and Table II	6
Edits to Table III and Table IV	7
Updated Outline Dimensions	8

10/2001—Rev. 0 to Rev. A

Edits to Table III	7
Edits to Table IV	7

1999—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = full operating range, $T_A = T_{MIN}$ to T_{MAX} , V_{CC} typical = 5 V, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
Operating Voltage	1		5.5	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
V_{CC} Supply Current		5	12	μA	$V_{CC} = 5.5\text{ V}$, no load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
			15	μA	$V_{CC} = 5.5\text{ V}$, no load, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
		4	10	μA	$V_{CC} = 3.6\text{ V}$, no load, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
			12	μA	$V_{CC} = 3.6\text{ V}$, no load, $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
RESET VOLTAGE THRESHOLD (V_{TH})					
	$V_{TH} - 1.8\%$	V_{TH}	$V_{TH} + 1.8\%$	V	$T_A = 25^\circ\text{C}$
	$V_{TH} - 2.5\%$		$V_{TH} + 2.5\%$	V	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	$V_{TH} - 3.5\%$		$V_{TH} + 3.5\%$	V	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
RESET THRESHOLD TEMPERATURE COEFFICIENT					
		60		ppm/ $^\circ\text{C}$	
V_{CC} TO RESET DELAY					
		35		μs	V_{CC} = falling at 1 mV/ μs
RESET ACTIVE TIMEOUT PERIOD					
ADM6315xxD1	1	1.4	2	ms	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	0.8		2.4	ms	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
ADM6315xxD2	20	28	40	ms	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	16		48	ms	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
ADM6315xxD3	140	200	280	ms	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	112		336	ms	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
ADM6315xxD4	1120	1570	2240	ms	$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$
	896		2688	ms	$T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$
MANUAL RESET					
Input Threshold	0.8			V	$V_{TH} > 4\text{ V}$ (V_{IL})
			2.4	V	$V_{TH} > 4\text{ V}$ (V_{IH})
	$0.3 \times V_{CC}$			V	$V_{TH} < 4\text{ V}$ (V_{IL})
			$0.7 \times V_{CC}$	V	$V_{TH} < 4\text{ V}$ (V_{IH})
Minimum Input Pulse	1			μs	
Glitch Rejection		100		ns	
To Reset Delay		500		ns	
Pull-Up Resistance	32	63	100	k Ω	
RESET OUTPUT					
Output Voltage			0.4	V	$V_{CC} > 4.25\text{ V}$, $I_{SINK} = 3.2\text{ mA}$
			0.3	V	$V_{CC} > 2.5\text{ V}$, $I_{SINK} = 1.2\text{ mA}$
			0.3	V	$V_{CC} > 1\text{ V}$, $I_{SINK} = 80\text{ }\mu\text{A}$
Output Leakage Current			1	μA	$V_{CC} > V_{TH}$, $\overline{\text{RESET}}$ deasserted

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Rating
Terminal Voltage (with Respect to Ground)	
V_{CC}	-0.3 V to +6 V
All Other Inputs	-0.3 V to +6 V
Input Current	
V_{CC}	20 mA
Output Current	
$\overline{\text{RESET}}$	20 mA
Operating Temperature Range	-40°C to $+125^\circ\text{C}$
Storage Temperature Range	-65°C to $+160^\circ\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C
ESD Rating	2.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
4-Lead SOT-143	330	$^\circ\text{C}/\text{W}$

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	GND	Ground Reference for All Signals, 0 V.
2	$\overline{\text{RESET}}$	Active Low Logic Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold or when $\overline{\text{MR}}$ is low. $\overline{\text{RESET}}$ then remains low for a minimum of 1 ms, 20 ms, 140 ms, or 1120 ms after V_{CC} rises above the reset threshold and MR is high.
3	$\overline{\text{MR}}$	Manual Reset. This active low debounced input ignores input pulses of 100 ns (typical) and is guaranteed to accept input pulses of greater than 1 μs . Leave floating when not used.
4	V_{CC}	Monitored Supply Voltage.

TYPICAL PERFORMANCE CHARACTERISTICS



Figure 4. Supply Current vs. Temperature



Figure 7. Maximum Transient Duration vs. \overline{RESET} Comparator Overdrive



Figure 5. Power-Down Reset Delay vs. Temperature



Figure 8. Normalized Reset Threshold vs. Temperature (V_{CC} Falling)



Figure 6. Normalized Reset Timeout Period vs. Temperature (V_{CC} Rising)



Figure 9. Supply Current vs. Supply Voltage

THEORY OF OPERATION

INTERFACING TO OUTPUT OF OTHER DEVICES

The ADM6315 series is designed to integrate with as many devices as possible. One feature of the ADM6315 is the $\overline{\text{RESET}}$ open-drain output, which can sink current from sources with a voltage greater than the V_{CC} of the ADM6315 input, making it suitable for use in more diverse applications.

BENEFITS OF AN ACCURATE $\overline{\text{RESET}}$ THRESHOLD

Because the ADM6315 series can operate effectively even when there are large degradations of the supply voltages (due to an accurate internal voltage reference circuit), the possibility of a malfunction during a power failure is greatly reduced.

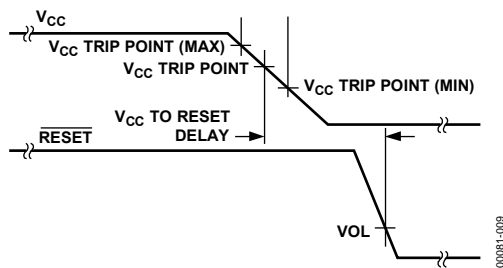


Figure 10. V_{CC} Power-Down/Brownout Timing Diagram

DETAILED DESCRIPTION

The ADM6315 is designed to protect the integrity of a system's operation by ensuring the proper operation of the system during power-up, power-down, and brownout conditions.

When the ADM6315 is powered up, the $\overline{\text{RESET}}$ output of the ADM6315 remains low for a period typically equal to the $\overline{\text{RESET}}$ active timeout period. This feature allows adequate time for the system to power up correctly and for the power supply to stabilize before any devices are brought out of reset and allowed to begin executing instructions. Initializing a system in this way provides a more reliable startup for microprocessor systems.

When a brownout condition occurs (assuming V_{CC} is falling at $1 \text{ mV}/\mu\text{s}$), the ADM6315 produces a reset in $35 \mu\text{s}$ typical. Producing a reset this fast means that the entire system can be reset together before any part of the system's voltage falls below its recommended operating voltage. This system reset can avoid dangerous and/or erroneous operation of a microprocessor-based system.

MANUAL RESET INPUT

The ADM6315 also provides an additional input, $\overline{\text{MR}}$. This input can be used either as a means for the system operator to reset the system manually via a switch or for a digital circuit to reset the system.

The $\overline{\text{MR}}$ input (typically) ignores negative-going pulses that are faster than 100 ns , and it is guaranteed to accept any negative-going input pulse of a duration greater than or equal to $1 \mu\text{s}$. If $\overline{\text{MR}}$ is connected to long cables or is used in a noisy environment, placing a $1 \mu\text{F}$ decoupling capacitor between the $\overline{\text{MR}}$ input and ground further improves the glitch immunity of the ADM6315.



Figure 11. V_{CC} Power-Up Timing Diagram

TRANSIENT IMMUNITY

As well as being an accurate reset circuit, the ADM6315 has good immunity from negative-going transients (see Figure 7). Because of this characteristic, the ADM6315 is suitable for use in noisy environments.

Figure 7 shows the $\overline{\text{RESET}}$ comparator overdrive (the maximum magnitude of negative-going pulses with respect to the typical reset threshold) vs. the pulse duration without a reset.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS TO-253-AA

Figure 12. 4-Lead Small Outline Transistor Package [SOT-143] (RA-4)

Dimensions shown in millimeters

03-13-2012-B

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Trip Point	Minimum Timeout (ms)	Marking Code
ADM6315-44D1ARTRL7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.39	1	MDT
ADM6315-31D1ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	3.08	1	M7X
ADM6315-29D1ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.93	1	M7T
ADM6315-26D1ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.63	1	MDB#
ADM6315-45D2ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.50	20	MA8
ADM6315-31D2ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	3.08	20	M7Y
ADM6315-29D2ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.93	20	M7U
ADM6315-26D2ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.63	20	MEB#
ADM6315-46D3ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.63	140	M84
ADM6315-44D3ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.39	140	MFT#
ADM6315-31D3ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	3.08	140	M4G
ADM6315-29D3ARTRL7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.93	140	MFC
ADM6315-26D3ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.63	140	MFB#
ADM6315-46D4ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.63	1120	M85
ADM6315-44D4ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	4.39	1120	M9H
ADM6315-31D4ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	3.08	1120	M7Z
ADM6315-29D4ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.93	1120	M7W
ADM6315-26D4ARTZR7	-40°C to +125°C	4-Lead SOT-143	RA-4	2.63	1120	MGB#

¹ Z = RoHS-Compliant Part, # denotes lead-free product may be top or bottom marked.

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