



**THE DATASHEET OF  
NVD4804NT4G**



# NTD4804N, NVD4804N

## MOSFET – Power, Single, N-Channel, DPAK/IPAK 30 V, 117 A



ON Semiconductor®

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### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- AEC Q101 Qualified – NVD4804N
- These Devices are Pb-Free and are RoHS Compliant

### Applications

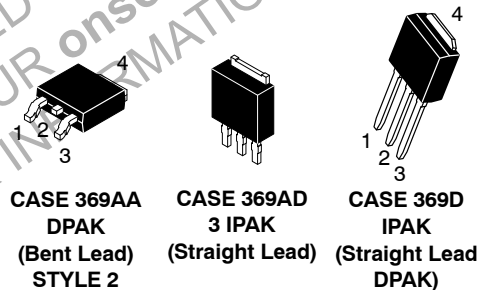
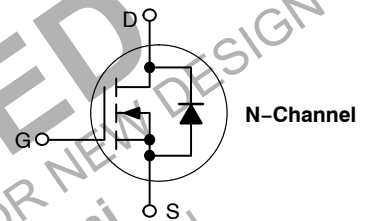
- CPU Power Delivery
- DC-DC Converters
- Low Side Switching

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	4.0 mΩ @ 10 V	117 A
	5.5 mΩ @ 4.5 V	

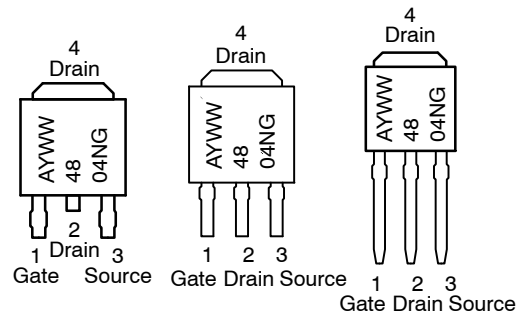
### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit		
Drain-to-Source Voltage	$V_{DSS}$	30	V		
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V		
Continuous Drain Current ( $R_{\theta JA}$ ) (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	19.6	A	
		$T_A = 85^\circ\text{C}$	15.2		
Power Dissipation ( $R_{\theta JA}$ ) (Note 1)	$P_D$	$T_A = 25^\circ\text{C}$	2.66	W	
		$T_A = 85^\circ\text{C}$	11		
Continuous Drain Current ( $R_{\theta JA}$ ) (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	14.5	A	
		$T_A = 85^\circ\text{C}$	11		
Power Dissipation ( $R_{\theta JA}$ ) (Note 2)	$P_D$	$T_A = 25^\circ\text{C}$	1.43	W	
		$T_A = 85^\circ\text{C}$	1.43		
Continuous Drain Current ( $R_{\theta JC}$ ) (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	124	A	
		$T_C = 85^\circ\text{C}$	96		
Power Dissipation ( $R_{\theta JC}$ ) (Note 1)	$P_D$	$T_C = 25^\circ\text{C}$	107	W	
Pulsed Drain Current	$t_p = 10\mu\text{s}$	$T_A = 25^\circ\text{C}$	$I_{DM}$	230	A
Current Limited by Package		$T_A = 25^\circ\text{C}$	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature	$T_J, T_{stg}$	-55 to 175		$^\circ\text{C}$	
Source Current (Body Diode)	$I_S$	78		A	
Drain to Source dV/dt	dV/dt	6.0		V/ns	
Single Pulse Drain-to-Source Avalanche Energy ( $V_{DD} = 24\text{ V}, V_{GS} = 10\text{ V}, L = 1.0\text{ mH}, I_{L(pk)} = 30\text{ A}, R_G = 25\ \Omega$ )	$E_{AS}$	450		mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



### MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location  
 Y = Year  
 WW = Work Week  
 4804N = Device Code  
 G = Pb-Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NTD4804N, NVD4804N

## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.4	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	56.4	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	105	

- Surface-mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
- Surface-mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			26		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.5		2.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			7.6		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ to }11.5\text{ V}$	$I_D = 30\text{ A}$	3.4	4.0	m $\Omega$
			$I_D = 15\text{ A}$	3.4		
		$V_{GS} = 4.5\text{ V}$	$I_D = 30\text{ A}$	4.7	5.5	
			$I_D = 15\text{ A}$	4.6		
Forward Transconductance	$g_{FS}$	$V_{DS} = 15\text{ V}, I_D = 15\text{ A}$		23		S

### CHARGES AND CAPACITANCES

Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 12\text{ V}$		4490		pF
Output Capacitance	$C_{oss}$			952		
Reverse Transfer Capacitance	$C_{rss}$			556		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		30	40	nC
Threshold Gate Charge	$Q_{G(TH)}$			5.5		
Gate-to-Source Charge	$Q_{GS}$			13		
Gate-to-Drain Charge	$Q_{GD}$			13		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 30\text{ A}$		73		nC

### SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		18		ns
Rise Time	$t_r$			20		
Turn-Off Delay Time	$t_{d(off)}$			24		
Fall Time	$t_f$			8		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 11.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		10		ns
Rise Time	$t_r$			19		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall Time	$t_f$			5		

- Pulse Test: Pulse Width  $\leq 300\ \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .
- Switching characteristics are independent of operating junction temperatures.

# NTD4804N, NVD4804N

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V <sub>SD</sub>	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 30 A	T <sub>J</sub> = 25°C		0.81	1.2	V
			T <sub>J</sub> = 125°C		0.72		
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs, I <sub>S</sub> = 30 A			34		ns
Charge Time	t <sub>a</sub>				19		
Discharge Time	t <sub>b</sub>				15		
Reverse Recovery Time	Q <sub>RR</sub>				30		

### PACKAGE PARASITIC VALUES

Source Inductance	L <sub>S</sub>	T <sub>A</sub> = 25°C		2.49		nH
Drain Inductance, DPAK	L <sub>D</sub>			0.0164		
Drain Inductance, IPAK	L <sub>D</sub>			1.88		
Gate Inductance	L <sub>G</sub>			3.46		
Gate Resistance	R <sub>G</sub>			0.6		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

DISCONTINUED

THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN

PLEASE CONTACT YOUR onsemi REPRESENTATIVE FOR INFORMATION

# NTD4804N, NVD4804N

## TYPICAL PERFORMANCE CURVES

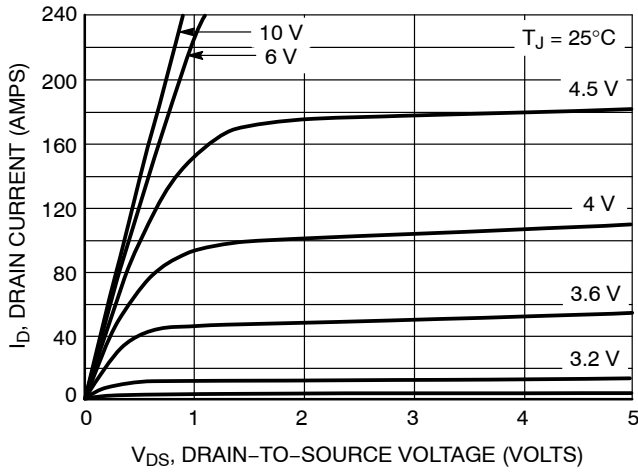


Figure 1. On-Region Characteristics

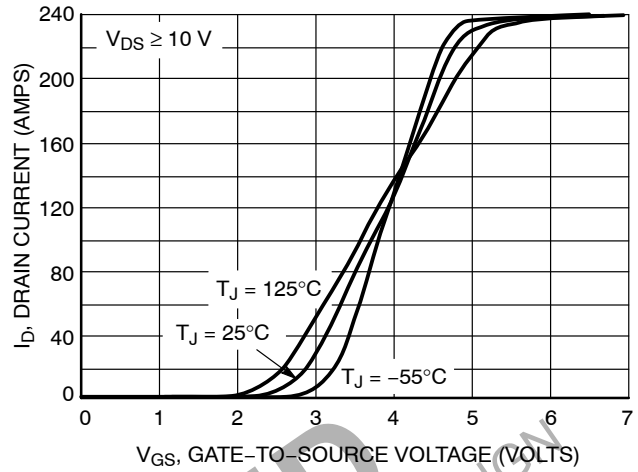


Figure 2. Transfer Characteristics

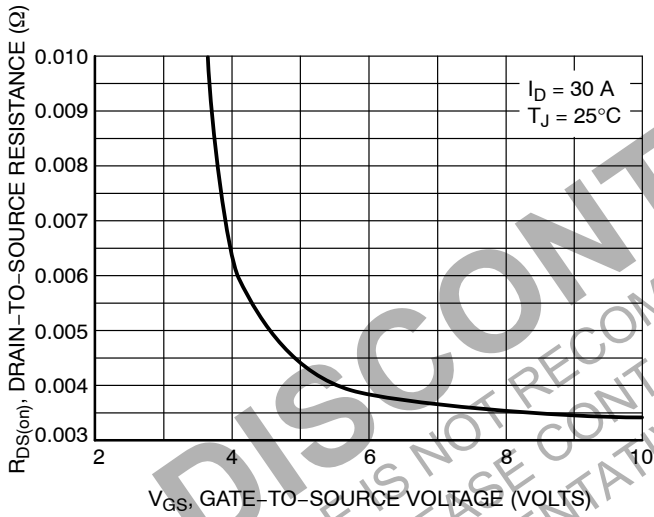


Figure 3. On-Resistance vs. Gate-to-Source Voltage

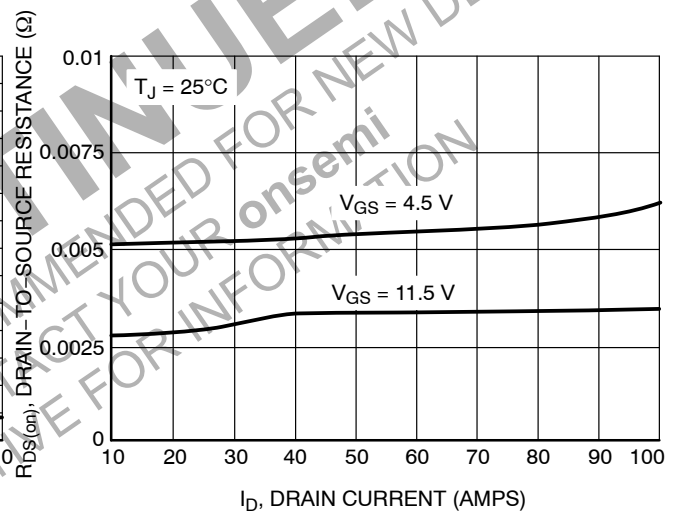


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

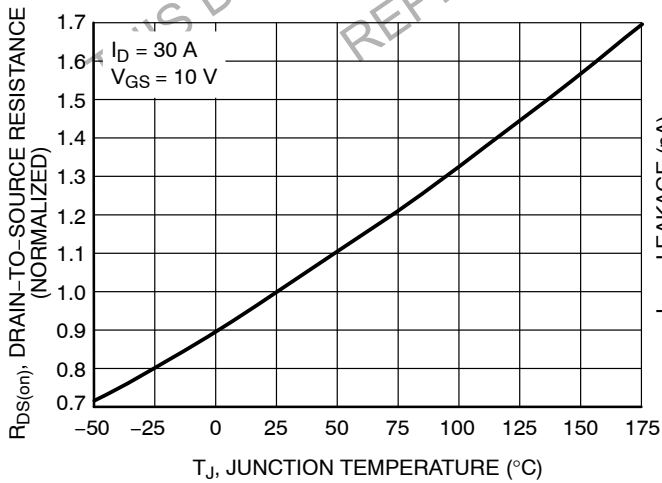


Figure 5. On-Resistance Variation with Temperature

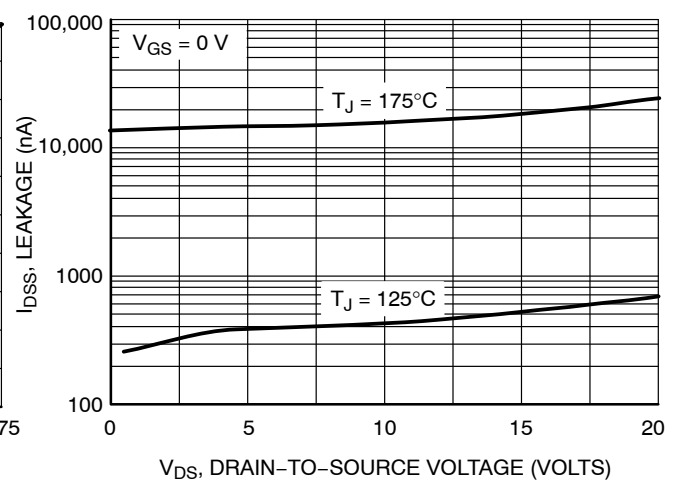


Figure 6. Drain-to-Source Leakage Current vs. Drain Voltage

# NTD4804N, NVD4804N

## TYPICAL PERFORMANCE CURVES

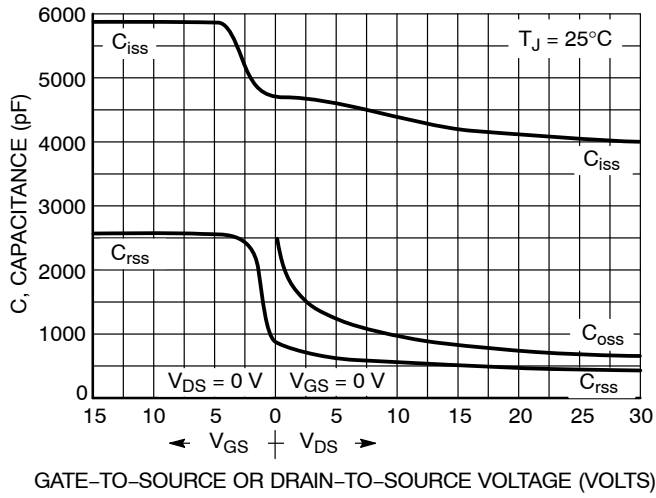


Figure 7. Capacitance Variation

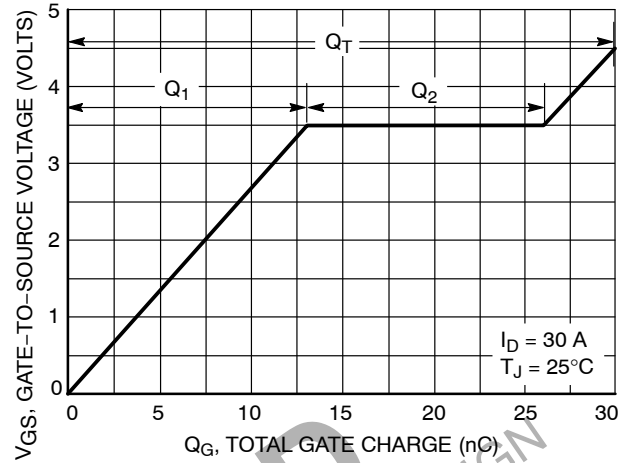


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

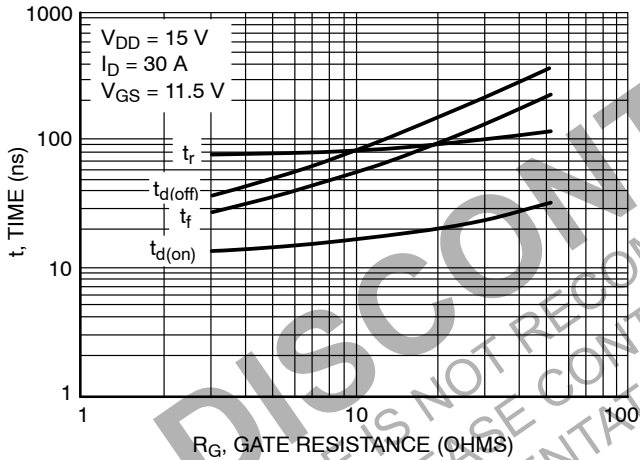


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

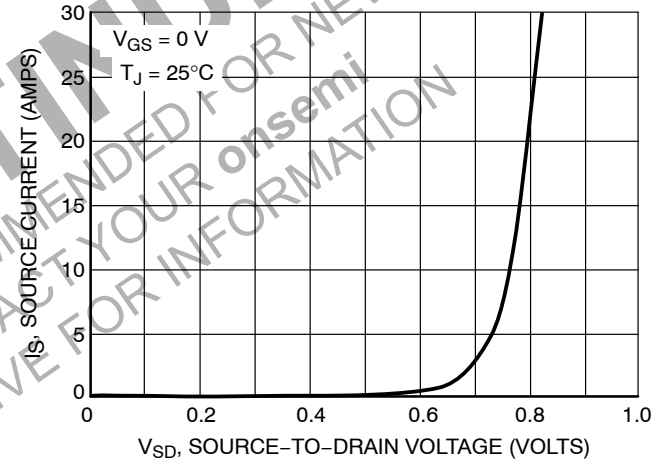


Figure 10. Diode Forward Voltage vs. Current

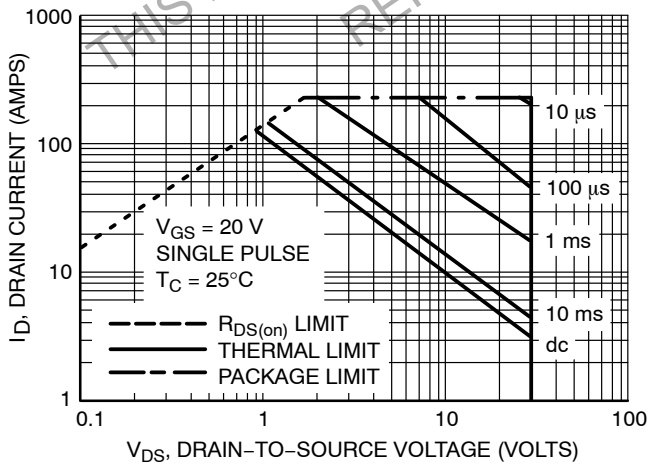


Figure 11. Maximum Rated Forward Biased Safe Operating Area

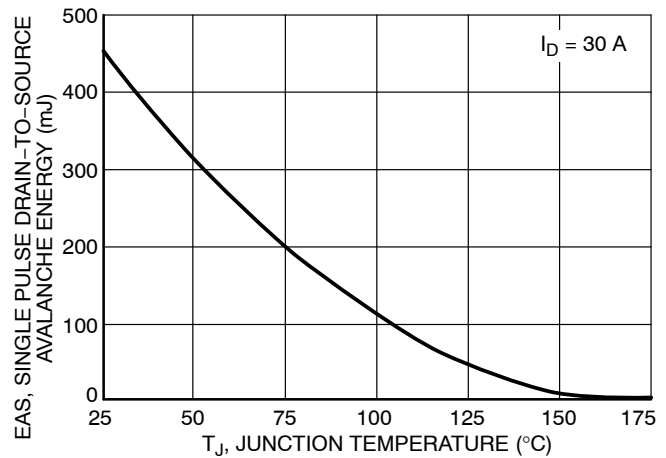


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTD4804N, NVD4804N

## TYPICAL PERFORMANCE CURVES

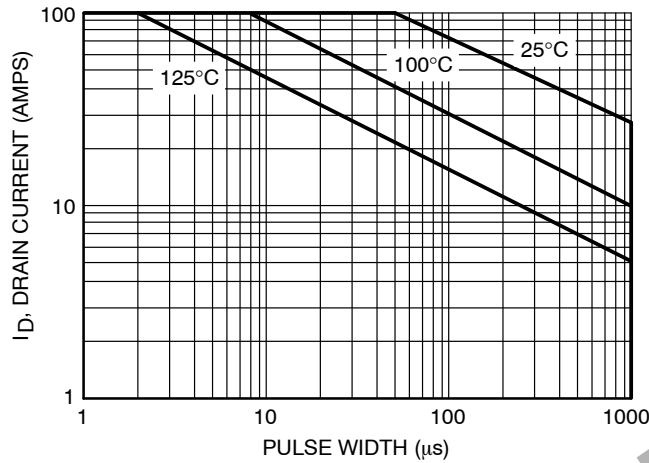


Figure 13. Avalanche Characteristics

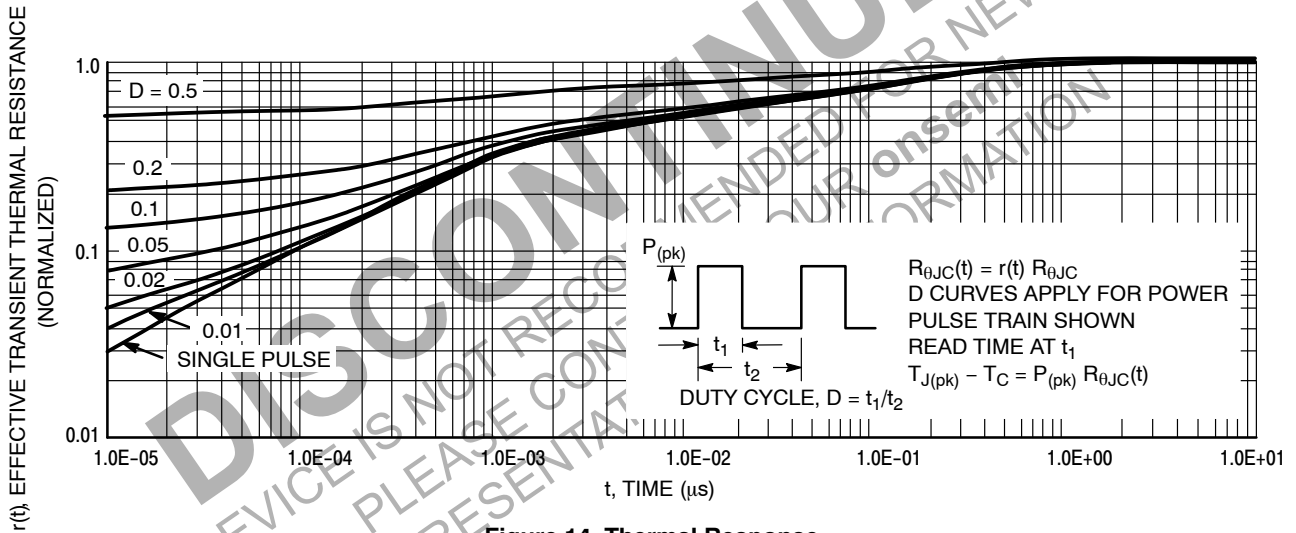


Figure 14. Thermal Response

### ORDERING INFORMATION

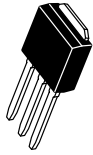
Order Number	Package	Shipping†
NTD4804NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NTD4804N-35G	IPAK Trimmed Lead (3.5 ± 0.15 mm) (Pb-Free)	75 Units / Rail
NVD4804NT4G	DPAK (Pb-Free)	2500 / Tape & Reel
NVD4804NT4G-VF01	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

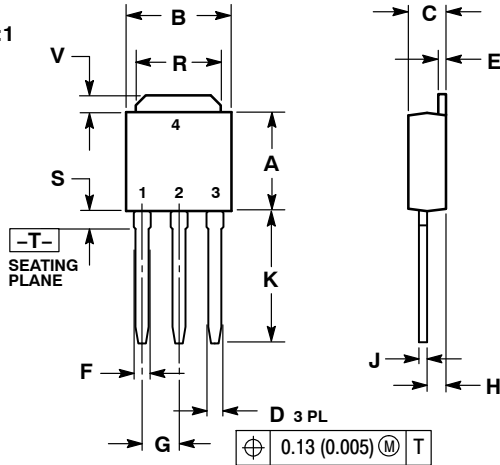
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### IPAK CASE 369D-01 ISSUE C

DATE 15 DEC 2010

SCALE 1:1

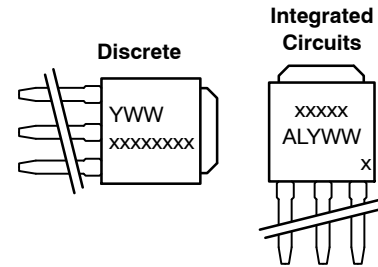


- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>      | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### MARKING DIAGRAMS



- xxxxxxx = Device Code  
A = Assembly Location  
IL = Wafer Lot  
Y = Year  
WW = Work Week

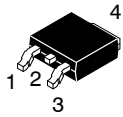
<b>DOCUMENT NUMBER:</b>	<b>98AON10528D</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>IPAK (DPAK INSERTION MOUNT)</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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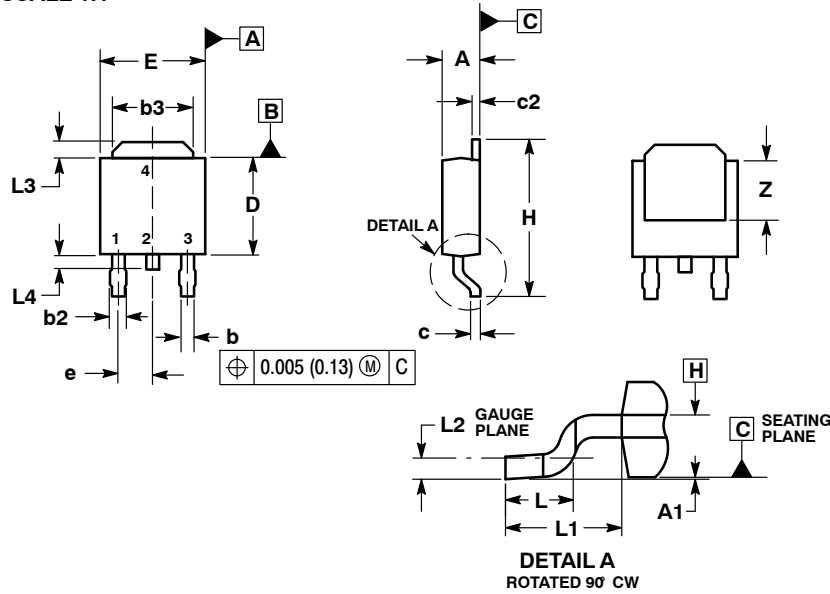
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### DPAK (SINGLE GAUGE)

#### CASE 369AA-01

#### ISSUE B

DATE 03 JUN 2010



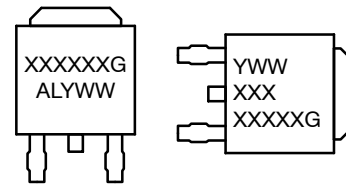
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

- |  |   |  |  |
|--|---|--|--|
| <p>STYLE 1:<br/>PIN 1. BASE<br/>2. COLLECTOR<br/>3. EMITTER<br/>4. COLLECTOR</p> | <p>STYLE 2:<br/>PIN 1. GATE<br/>2. DRAIN<br/>3. SOURCE<br/>4. DRAIN</p> | <p>STYLE 3:<br/>PIN 1. ANODE<br/>2. CATHODE<br/>3. ANODE<br/>4. CATHODE</p>  | <p>STYLE 4:<br/>PIN 1. CATHODE<br/>2. ANODE<br/>3. GATE<br/>4. ANODE</p> |
| <p>STYLE 5:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. CATHODE<br/>4. ANODE</p>         | <p>STYLE 6:<br/>PIN 1. MT1<br/>2. MT2<br/>3. GATE<br/>4. MT2</p>        | <p>STYLE 7:<br/>PIN 1. GATE<br/>2. ANODE<br/>3. EMITTER<br/>4. COLLECTOR</p> |  |

### GENERIC MARKING DIAGRAM\*

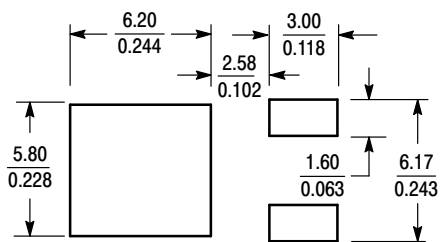


IC Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking.

### SOLDERING FOOTPRINT\*



SCALE 3:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

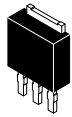
DOCUMENT NUMBER:	98AON13126D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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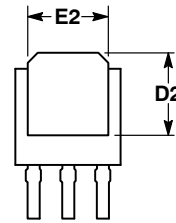
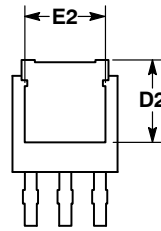
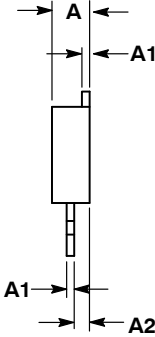
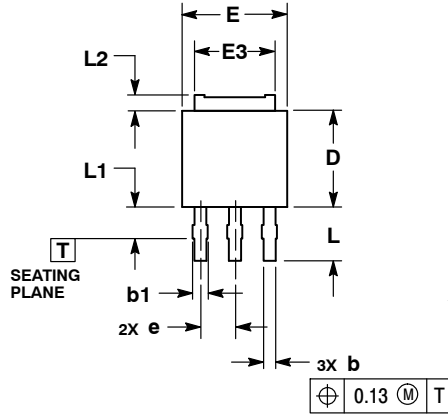
### 3.5 MM IPAK, STRAIGHT LEAD

#### CASE 369AD

#### ISSUE B

DATE 18 APR 2013

SCALE 1:1



OPTIONAL CONSTRUCTION

NOTES:

- 1.. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
- 2.. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

DIM	MILLIMETERS	
	MIN	MAX
A	2.19	2.38
A1	0.46	0.60
A2	0.87	1.10
b	0.69	0.89
b1	0.77	1.10
D	5.97	6.22
D2	4.80	---
E	6.35	6.73
E2	4.57	5.45
E3	4.45	5.46
e	2.28 BSC	
L	3.40	3.60
L1	---	2.10
L2	0.89	1.27

### GENERIC MARKING DIAGRAMS\*

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 2:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

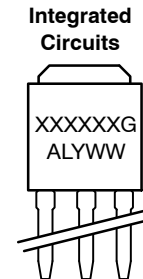
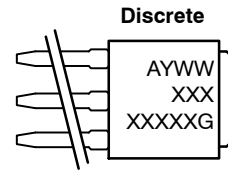
STYLE 3:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 4:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 5:  
PIN 1. GATE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 6:  
PIN 1. MT1  
2. MT2  
3. GATE  
4. MT2

STYLE 7:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR



XXXXXX = Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

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DESCRIPTION:	3.5 MM IPAK, STRAIGHT LEAD	PAGE 1 OF 1

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