# THE DATASHEET OF

# ADP170AUJZ-1.8-R7

# 300 mA, Low Quiescent Current, CMOS Linear Regulators

Data Sheet

# ADP170/ADP171

## FEATURES

- Maximum output current: 300 mA
- Input voltage range: 1.6 V to 3.6 V
- Low quiescent current
  - $I_{GND}$ = 23 µA with 0 mA load
  - $I_{GND}$ = 170 µA with 300 mA load
- Low shutdown current: <1 µA
- Low dropout voltage: 66 mV at 300 mA load
- Output voltage accuracy: ±1%
- Up to 31 fixed-output voltage options available from 0.8 V to 3.0 V
- Adjustable-output voltage range
  - 0.8 V to 3.0 V (ADP171)
- Accuracy over line, load, and temperature: ±3%
- Stable with small 1 µF ceramic output capacitor
- PSRR performance of 70 dB at 10 kHz and 73 dB at 1 kHz
- Low noise: 30 µV rms at $V_{OUT}$ = 0.8 V
- Current limit and thermal overload protection
- Logic-controlled enable
- Compact 5-lead TSOT package

## APPLICATIONS

- Mobile phones
- Digital camera and audio devices
- Portable and battery-powered equipment
- DSP/FPGA/microprocessor supplies
- Post dc-dc regulation

## TYPICAL APPLICATION CIRCUITS

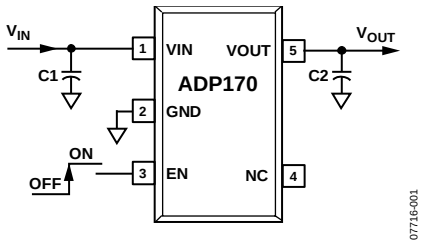


*Figure 1. ADP170 with Fixed Output Voltage, 1.8 V*

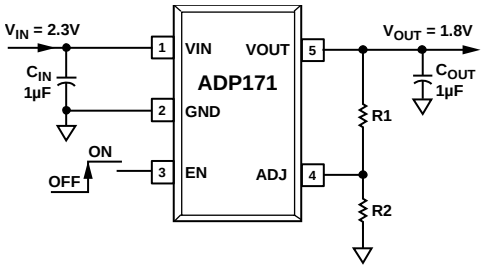


*Figure 2. ADP171 with Adjustable Output Voltage*

## GENERAL DESCRIPTION

The ADP170/ADP171 are low voltage input, low quiescent current, low-dropout (LDO) linear regulators that operate from 1.6 V to 3.6 V and provide up to 300 mA of output current. The low 66 mV dropout voltage at 300 mA load improves efficiency and allows operation over a wide input voltage range. The low 23 µA of quiescent current at a 0 mA load makes the ADP170/ADP171 ideal for battery-operated portable equipment.

The ADP170 is capable of 31 fixed-output voltage options, ranging from 0.8 V to 3.0 V. ADP171 is an adjustable version, which allows output voltages that range from 0.8 V to 3.0 V via an external divider. The ADP170/ADP171 are optimized for stable operation with small 1 µF ceramic output capacitors. Ideal for powering digital processors, the ADP170/ADP171 exhibit good transient performance and occupy minimal board space. Compared with commodity types of LDOs, the ADP170/ADP171 provide 20 dB to 40 dB better power supply rejection ratio (PSRR) at 100 kHz, making the ADP170/ADP171 an ideal power source for analog-to-digital converter (ADC) mixed-signal processor systems and allowing use of smaller size bypass capacitors. In addition, low output noise performance without the need for an additional bypass capacitor further reduces printed circuit board (PCB) component count.

Short-circuit protection and thermal overload protection circuits prevent damage in adverse conditions. The ADP170/ADP171 are available in tiny 5-lead TSOT for the smallest footprint solution to meet a variety of portable power applications.

Rev. C
Document Feedback


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# TABLE OF CONTENTS



## REVISION HISTORY

**1/14—Rev. B to Rev. C**

Changes to Ordering Guide ..... 17

**5/10—Rev. A to Rev. B**

Changes to Figure 1 and Figure 2 ..... 1
Updated Outline Dimensions ..... 17
Changes to Ordering Guide ..... 17

**6/09—Rev. 0 to Rev. A**

Changes to Features Section ..... 1
Updated Outline Dimensions ..... 17

**1/09—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{IN}$ = ($V_{OUT}$ + 0.4 V) or 1.6 V (whichever is greater), EN = $V_{IN}$, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 1 µF, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT VOLTAGE RANGE | $V_{IN}$ | $T_J$ = −40°C to +125°C | 1.6 | | 3.6 | V |
| OPERATING SUPPLY CURRENT[1] | $I_{GND}$ | $I_{OUT}$ = 0 µA | | 23 | | µA |
| | | $I_{OUT}$ = 0 µA, $T_J$ = −40°C to +125°C | | | 60 | µA |
| | | $I_{OUT}$ = 1 mA | | 50 | | µA |
| | | $I_{OUT}$ = 1 mA, $T_J$ = −40°C to +125°C | | | 100 | µA |
| | | $I_{OUT}$ = 150 mA | | 130 | | µA |
| | | $I_{OUT}$ = 150 mA, $T_J$ = −40°C to +125°C | | | 210 | µA |
| | | $I_{OUT}$ = 300 mA | | 170 | | µA |
| | | $I_{OUT}$ = 300 mA, $T_J$ = −40°C to +125°C | | | 260 | µA |
| SHUTDOWN CURRENT | $I_{GND-SD}$ | EN = GND | | 0.1 | | µA |
| | | EN = GND, $V_{IN}$ = 3.6 V, $T_J$ = −40°C to +85°C | | | 2 | µA |
| | | EN = GND, $V_{IN}$ = 3.6 V, $T_J$ = 85°C to 125°C | | | 25 | µA |
| FIXED-OUTPUT VOLTAGE ACCURACY | $V_{OUT}$ | $I_{OUT}$ = 10 mA | −1 | | +1 | % |
| | | 1 mA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 3.6 V | −2 | | +2 | % |
| | | 1 mA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 3.6 V, $T_J$ = −40°C to +125°C | −3 | | +3 | % |
| ADJUSTABLE-OUTPUT VOLTAGE ACCURACY (ADP171)[2] | $V_{ADJ}$ | $I_{OUT}$ = 10 mA | 0.495 | 0.5 | 0.505 | V |
| | | 1 mA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 3.6 V | 0.490 | | 0.510 | V |
| | | 1 mA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 3.6 V, $T_J$ = −40°C to +125°C | 0.485 | | 0.515 | V |
| ADJ INPUT BIAS CURRENT (ADP171) | $ADJ_{I-BIAS}$ | 1.6 V ≤ $V_{IN}$ ≤ 3.6 V, ADJ connected to VOUT | | 15 | | nA |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 3.6 V, $T_J$ = −40°C to +125°C | −0.25 | | +0.25 | %/V |
| LOAD REGULATION[3] | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT}$ = 1 mA to 300 mA | | 0.001 | | %/mA |
| | | $I_{OUT}$ = 1 mA to 300 mA, $T_J$ = −40°C to +125°C | | | 0.007 | %/mA |
| DROPOUT VOLTAGE[4] | $V_{DROPOUT}$ | $I_{OUT}$ = 10 mA, $V_{OUT}$ ≥ 1.8 V | | 2 | | mV |
| | | $I_{OUT}$ = 10 mA, $V_{OUT}$ ≥ 1.8 V, $T_J$ = −40°C to +125°C | | | 7 | mV |
| | | $I_{OUT}$ = 150 mA, $V_{OUT}$ ≥ 1.8 V | | 33 | | mV |
| | | $I_{OUT}$ = 150 mA, $V_{OUT}$ ≥ 1.8 V, $T_J$ = −40°C to +125°C | | | 70 | mV |
| | | $I_{OUT}$ = 300 mA, $V_{OUT}$ ≥ 1.8 V | | 66 | | mV |
| | | $I_{OUT}$ = 300 mA, $V_{OUT}$ ≥ 1.8 V, $T_J$ = −40°C to +125°C | | | 135 | mV |
| START-UP TIME[5] | $t_{START-UP}$ | $V_{OUT}$ = 1.8 V | | 120 | | µs |
| CURRENT-LIMIT THRESHOLD[6] | $I_{LIMIT}$ | | 400 | 450 | 800 | mA |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | $TS_{SD}$ | $T_J$ rising | | 150 | | °C |
| Thermal Shutdown Hysteresis | $TS_{SD-HYS}$ | | | 15 | | °C |
| EN INPUT | | | | | | |
| Logic High Voltage | $V_{IH}$ | 1.6 V ≤ $V_{IN}$ ≤ 3.6 V | 1.2 | | | V |
| Logic Low Voltage | $V_{IL}$ | 1.6 V ≤ $V_{IN}$ ≤ 3.6 V | | | 0.4 | V |
| Leakage Current Voltage | $V_{I-LEAKAGE}$ | EN = VIN or GND | | 0.1 | | µA |
| | | EN = VIN or GND, $T_J$ = −40°C to +125°C | | | 1 | µA |
| UNDERVOLTAGE LOCKOUT | UVLO | | | | | |
| Input Voltage Rising | $UVLO_{RISE}$ | $T_J$ = −40°C to +125°C | | | 1.5 | V |
| Input Voltage Falling | $UVLO_{FALL}$ | $T_J$ = −40°C to +125°C | 0.7 | | | V |
| Hysteresis | $UVLO_{HYS}$ | | | 80 | | mV |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT NOISE | $OUT_{NOISE}$ | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 3.0 V | | 72 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.8 V | | 50 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V | | 40 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.8 V | | 30 | | μV rms |
| POWER SUPPLY REJECTION RATIO | PSRR | 1 kHz, $V_{IN}$ = 3.6 V, $I_{OUT}$ = 10 mA, $V_{OUT}$ = 0.8 V | | 73 | | dB |
| | | 10 kHz, $V_{IN}$ = 3.6 V, $I_{OUT}$ = 10 mA, $V_{OUT}$ = 0.8 V | | 70 | | dB |
| | | 10 kHz, $V_{IN}$ = ($V_{OUT}$ + 1 V), $I_{OUT}$ = 10 mA to 300 mA | | 50 | | dB |
| | | 100 kHz, $V_{IN}$ = ($V_{OUT}$ + 1 V), $I_{OUT}$ = 10 mA to 300 mA | | 47 | | dB |

[1] The current from the external resistor divider network in the case of adjustable voltage output (as with the ADP171) should be subtracted from the ground current measured.
[2] Accuracy when VOUT is connected directly to ADJ. When the VOUT voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of resistors used.
[3] Based on an end-point calculation using 1 mA and 300 mA loads. See Figure 6 for typical load regulation performance for loads less than 1 mA.
[4] Applies only for output voltages above 1.6 V. Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage.
[5] Start-up time is defined as the time between the rising edge of EN and VOUT being at 90% of its nominal value.
[6] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

## INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MINIMUM INPUT AND OUTPUT CAPACITANCE[1] | $C_{MIN}$ | $T_J$ = −40°C to +125°C | 0.45 | | | μF |
| CAPACITOR ESR | $R_{ESR}$ | $T_J$ = −40°C to +125°C | 0.001 | | 1 | Ω |

[1] The minimum input and output capacitance should be greater than 0.45 μF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended; Y5V and Z5U capacitors are not recommended for use with any LDO.

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| VIN to GND | −0.3 V to +3.6 V |
| VOUT to GND | −0.3 V to VIN |
| EN to GND | −0.3 V to +3.6 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Operating Ambient Temperature Range | −40°C to +85°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses above those listed under absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL DATA

Absolute maximum ratings apply only individually, not in combination. The ADP170/ADP171 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that $T_J$ is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature ($T_J$) of the device is dependent on the ambient temperature ($T_A$), the power dissipation of the device ($P_D$), and the junction-to-ambient thermal resistance of the package ($\theta_{JA}$).

Maximum junction temperature ($T_J$) is calculated from the ambient temperature ($T_A$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance ($\theta_{JA}$) of the package is based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of $\theta_{JA}$ may vary, depending on PCB material, layout, and environmental conditions. The specified values of $\theta_{JA}$ are based on a 4-layer, 4 in. × 3 in. PCB. Refer to JESD 51-7 for detailed information regarding board construction.

$\Psi_{JB}$ is the junction-to-board thermal characterization parameter with units of °C/W. The $\Psi_{JB}$ of the package is based on modeling and calculation using a 4-layer board. The *Guidelines for Reporting and Using Electronic Package Thermal Information: JESD51-12* states that thermal characterization parameters are not the same as thermal resistances. $\Psi_{JB}$ measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, $\theta_{JB}$. Therefore, $\Psi_{JB}$ thermal paths include convection from the top of the package as well as radiation from the package—factors that make $\Psi_{JB}$ more useful in real-world applications. Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about $\Psi_{JB}$.

## THERMAL RESISTANCE

$\theta_{JA}$ and $\Psi_{JB}$ are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\Psi_{JB}$ | Unit |
|---|---|---|---|
| 5-Lead TSOT | 170 | 43 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

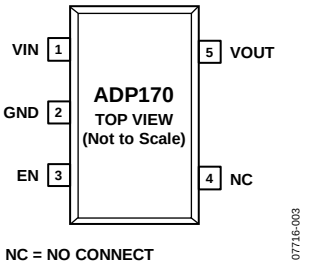



*Figure 3. ADP170 5-Lead TSOT*

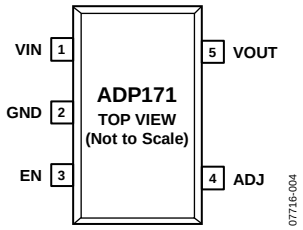



*Figure 4. ADP171 5-Lead TSOT*

**Table 5. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **ADP170** | **ADP171** | **Mnemonic** | **Description** |
| 1 | 1 | VIN | Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor. |
| 2 | 2 | GND | Ground. |
| 3 | 3 | EN | Enable Input. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. For automatic startup, connect EN to VIN. |
| 4 | | NC | No Connect. Not connected internally. |
| | 4 | ADJ | Adjust. A resistor divider from VOUT to ADJ sets the output voltage. |
| 5 | 5 | VOUT | Regulated Output Voltage. Bypass VOUT to GND with a 1 µF or greater capacitor. |

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.8 V, $I_{OUT}$ = 10 mA, $C_{IN}$ = $C_{OUT}$ = 1 µF, $T_A$ = 25°C, unless otherwise noted.

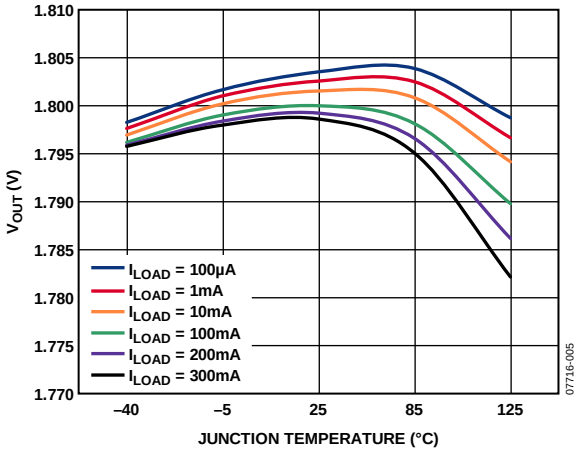



Figure 5. Output Voltage vs. Junction Temperature

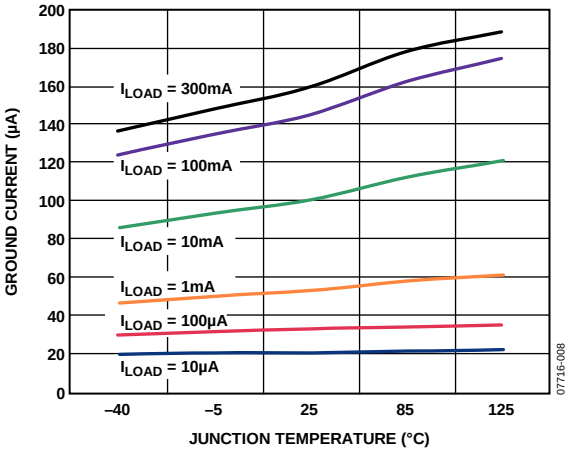



Figure 8. Ground Current vs. Junction Temperature

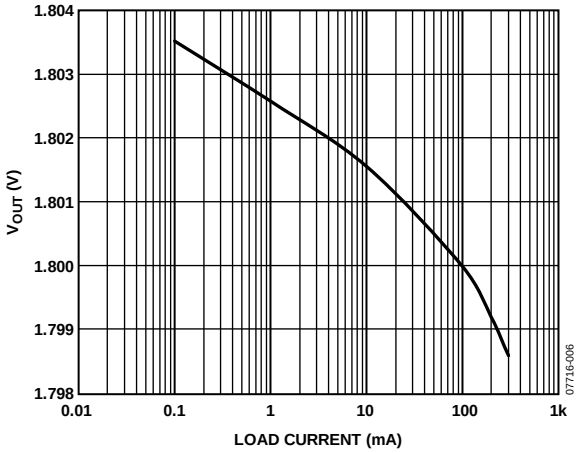



Figure 6. Output Voltage vs. Load Current

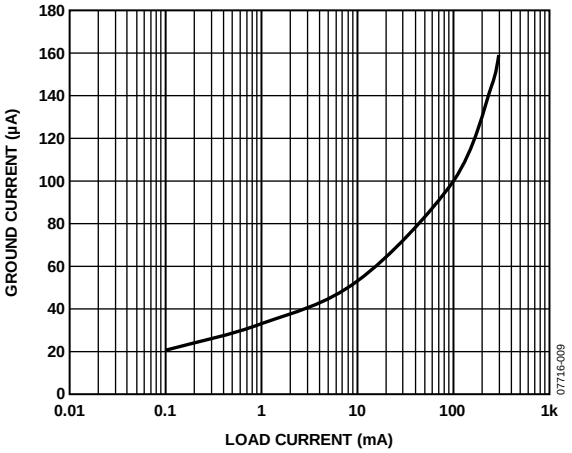



Figure 9. Ground Current vs. Load Current

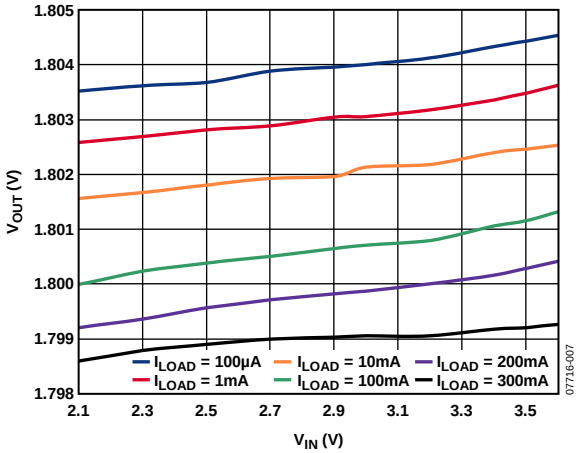



Figure 7. Output Voltage vs. Input Voltage

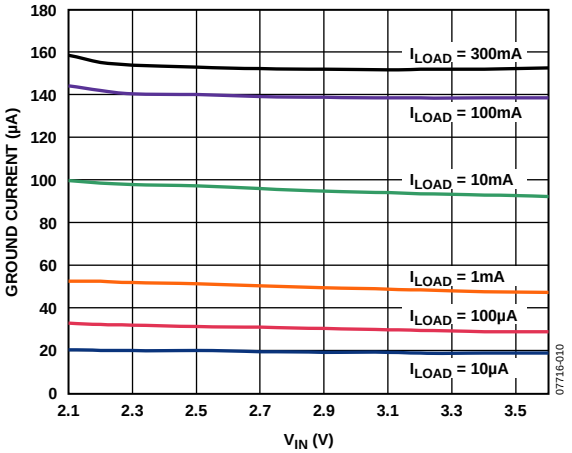



Figure 10. Ground Current vs. Input Voltage

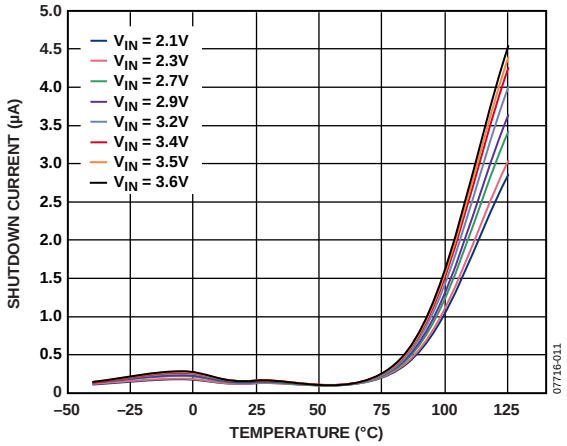



Figure 11. Shutdown Current vs. Temperature at Various Input Voltages

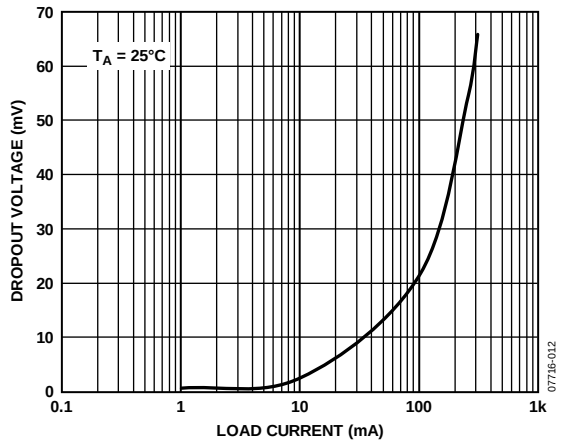



Figure 12. Dropout Voltage vs. Load Current

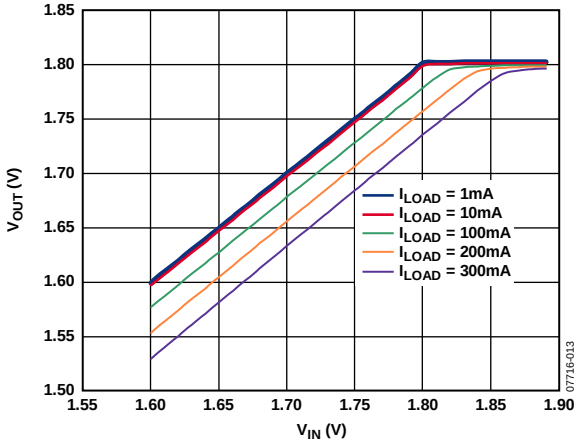



Figure 13. Output Voltage vs. Input Voltage (in Dropout)

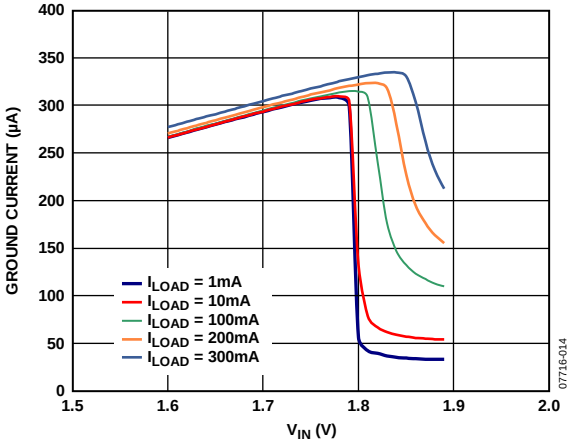



Figure 14. Ground Current vs. Input Voltage (In Dropout)

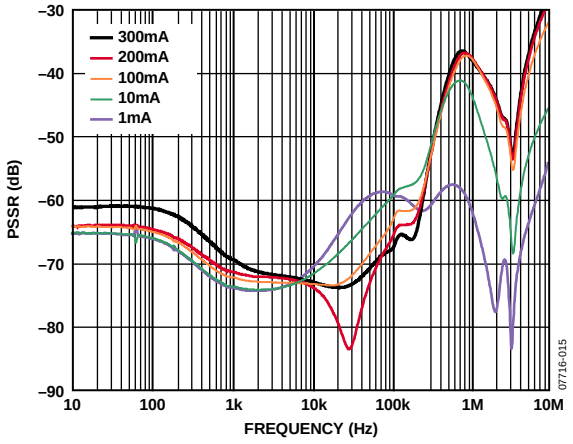



Figure 15. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 0.8 V

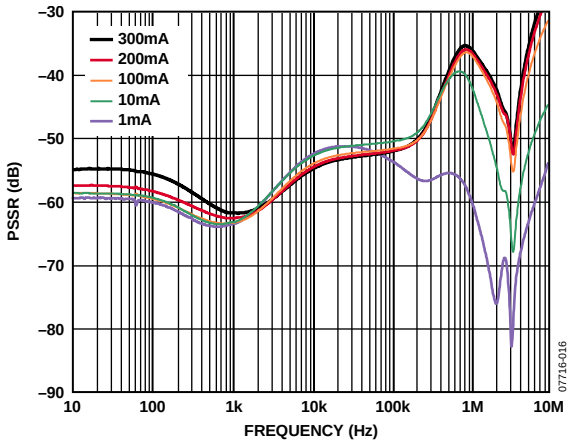



Figure 16. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 1.8 V

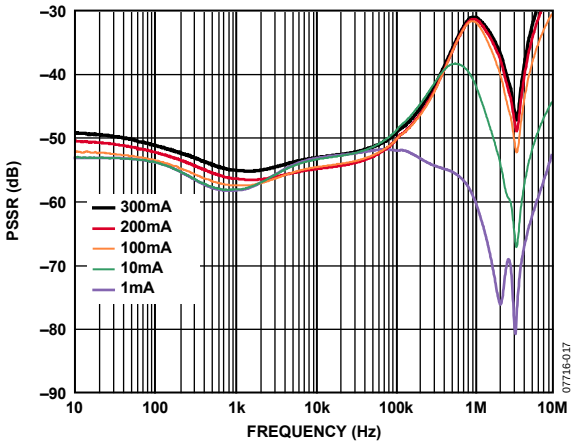



Figure 17. Power Supply Rejection Ratio vs. Frequency, $V_{OUT}$ = 3.0 V

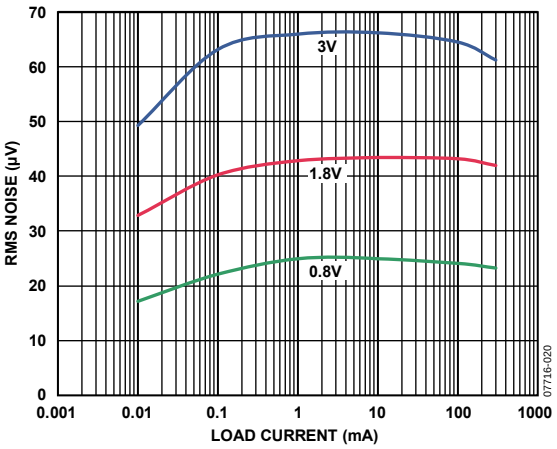



Figure 20. RMS Noise vs. Load Current and Output Voltage

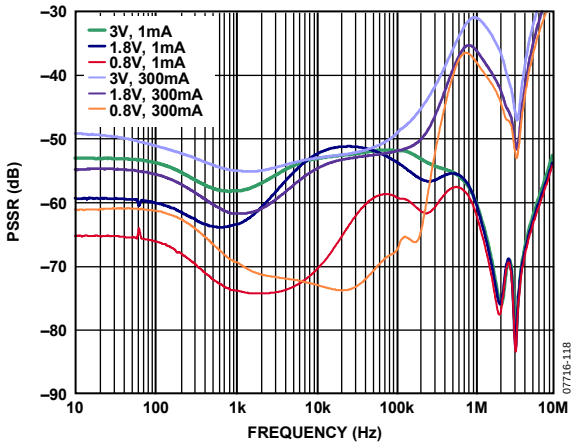



Figure 18. Power Supply Rejection Ratio vs. Frequency, Various Output Voltages and Load Currents

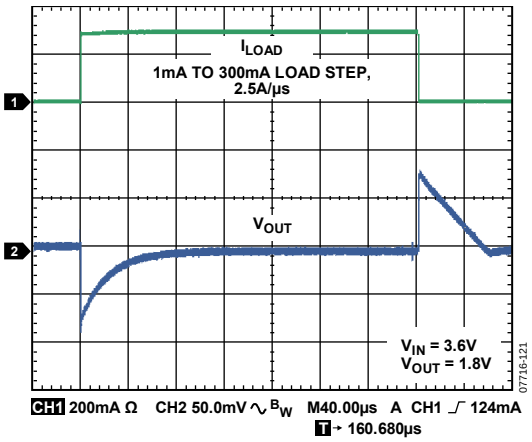



Figure 21. Load Transient Response, $C_{IN}$ and $C_{OUT}$ = 1 µF

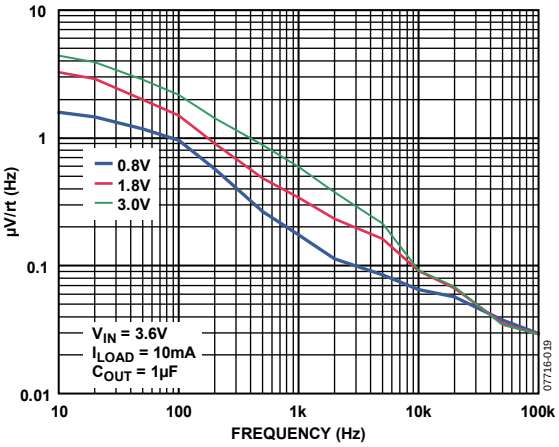



Figure 19. Output Noise Spectrum

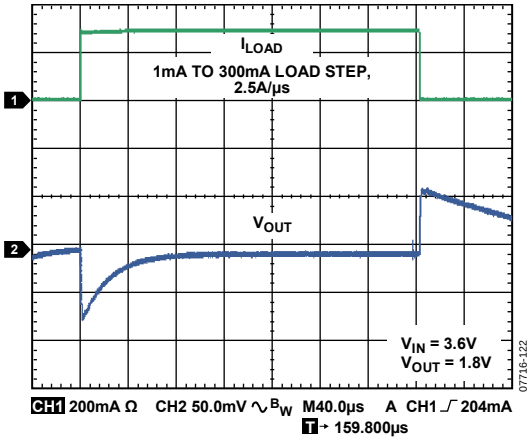



Figure 22. Load Transient Response, $C_{IN}$ and $C_{OUT}$ = 4.7 µF

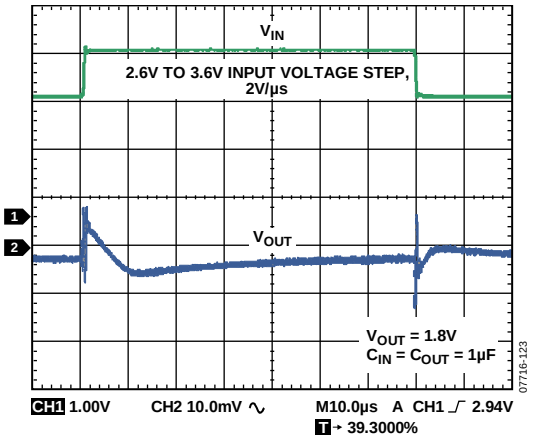



*Figure 23. Line Transient Response, Load Current = 1 mA*

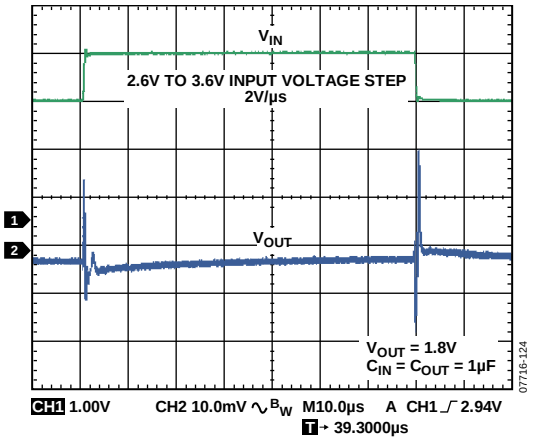
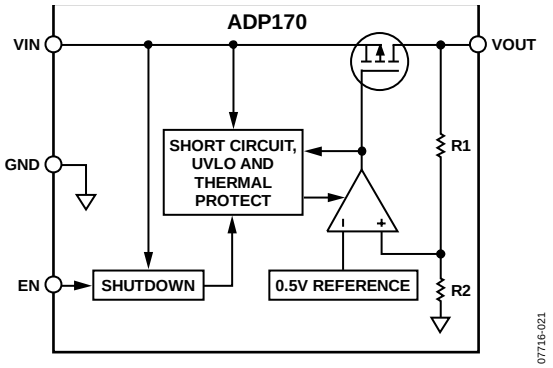



*Figure 24. Line Transient Response, Load Current = 300 mA*

# THEORY OF OPERATION

The ADP170/ADP171 are low quiescent current, low-dropout linear regulators that operate from 1.6 V to 3.6 V and can provide up to 300 mA of output current. Drawing a low 170 µA of quiescent current (typical) at full load makes the ADP170/ADP171 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP170/ADP171 provide excellent transient performance.




NOTES
1. R1 AND R2 ARE INTERNAL RESISTORS, AVAILABLE ON THE ADP170 ONLY.

*Figure 25. ADP170 Internal Block Diagram*

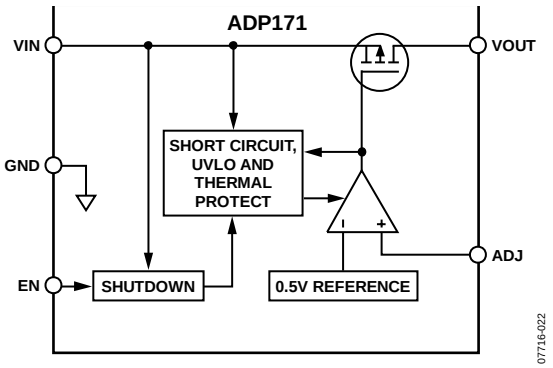



*Figure 26. ADP171 Internal Block Diagram*

Internally, the ADP170/ADP171 consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The adjustable ADP171 has an output voltage range of 0.8 V to 3.0 V. The output voltage is set by the ratio of two external resistors, as shown in Figure 2. The device servos the output to maintain the voltage at the ADJ pin at 0.5 V referenced to ground. The current in R1 is then equal to 0.5 V/R2 and the current in R1 is the current in R2 plus the ADJ pin bias current. The ADJ pin bias current, 15 nA at 25°C, flows through R1 into the ADJ pin.

The output voltage can be calculated using the equation:

$$V_{OUT} = 0.5\ \text{V}(1 + R1/R2) + (ADJ_{I\text{-}BIAS})(R1)$$

The value of R1 should be less than 200 kΩ to minimize errors in the output voltage caused by the ADJ pin bias current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 1.0 V. The output voltage error introduced by the ADJ pin bias current is 3 mV or 0.3%, assuming a typical ADJ pin bias current of 15 nA at 25°C.

Note that in shutdown, the output is turned off and the divider current is zero.

The ADP170/ADP171 use the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on; when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

# APPLICATIONS INFORMATION

## CAPACITOR SELECTION

### Output Capacitor

The ADP170/ADP171 are designed for operation with small, space-saving ceramic capacitors but will function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure stability of the ADP170/ADP171. The transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP170/ADP171 to large changes in load current. Figure 27 and Figure 28 show the transient responses for output capacitance values of 1 µF and 4.7 µF, respectively.

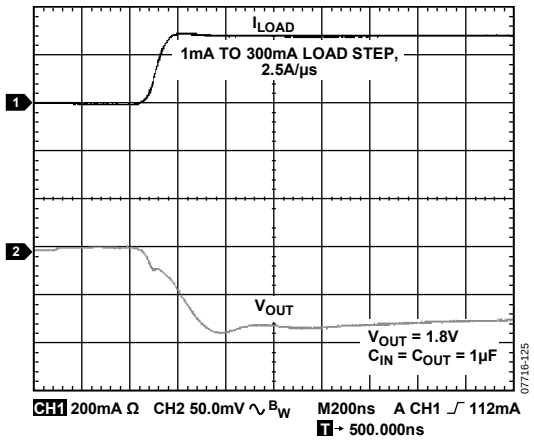



*Figure 27. Output Transient Response, $C_{OUT}$ = 1 µF*

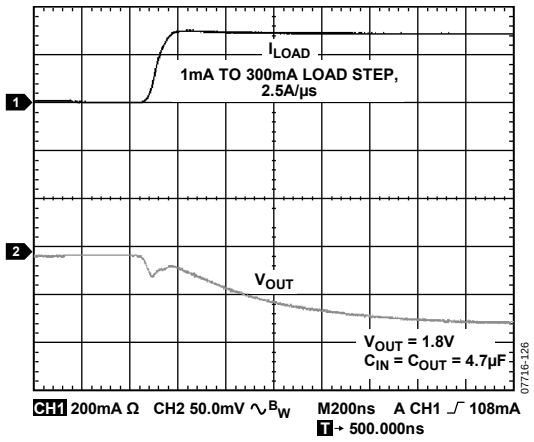



*Figure 28. Output Transient Response, $C_{OUT}$ = 4.7 µF*

### Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

### Input and Output Capacitor Properties

Any good quality ceramic capacitor can be used with the ADP170/ADP171, as long as it meets the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. A X5R or X7R dielectric with a voltage rating of 6.3 V or 10 V is recommended. The Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 29 depicts the capacitance vs. bias voltage characteristics of a 0402, 1 µF, 10 V X5R capacitor. The variance of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating will exhibit less capacitance variance over bias voltage. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

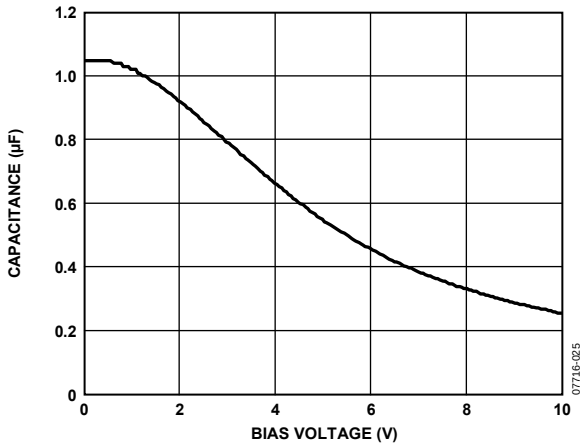



*Figure 29. Capacitance vs. Bias Voltage Characteristics*

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:

$C_{BIAS}$ is the effective capacitance at the operating voltage.
*TEMPCO* is the worst-case capacitor temperature coefficient.
*TOL* is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and $C_{BIAS}$ is 0.94 µF at 1.8 V, as shown in Figure 29.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP170/ADP171, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors are evaluated for each application.

## UNDERVOLTAGE LOCKOUT

The ADP170/ADP171 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 1.2 V. This ensures that the ADP170/ADP171 inputs and the output behave in a predictable manner during power-up.

## ENABLE FEATURE

The ADP170/ADP171 use the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 30, when a rising voltage on EN crosses the active threshold, VOUT turns on. When a falling voltage on EN crosses the inactive threshold, VOUT turns off.

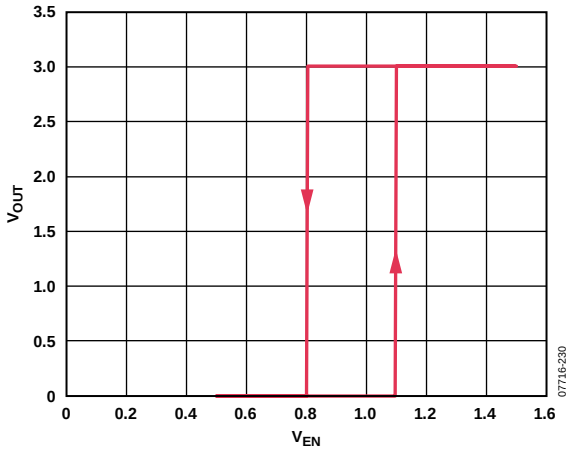



*Figure 30. ADP170/ADP171 Typical EN Pin Operation*

As shown in Figure 30, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 31 shows typical EN active/inactive thresholds when the input voltage varies from 1.6 V to 3.6 V.

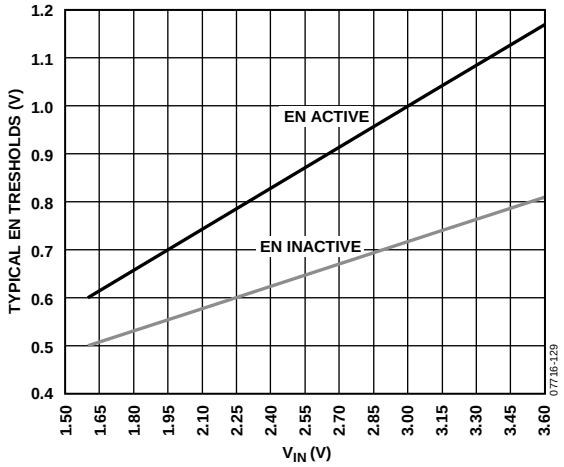



*Figure 31. Typical EN Pin Thresholds vs. Input Voltage*

The ADP170/ADP171 utilize an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 1.8 V option is approximately 120 µs from the time the EN active threshold is crossed to when the output reaches 90% of its final value. As shown in Figure 32, the start-up time is dependent on the output voltage setting.

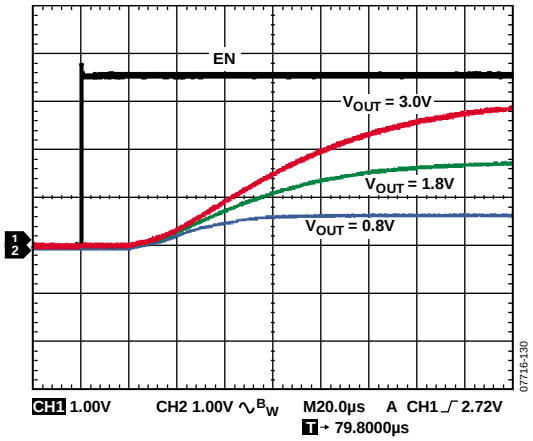



*Figure 32. Typical Start-Up Time*

## CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP170/ADP171 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP170/ADP171 are designed to limit the current when the output load reaches 450 mA (typical). When the output load exceeds 450 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation), when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to 0. When the junction temperature drops below 135°C, the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from VOUT to GND occurs. At first, the ADP170/ADP171 will limit the current so that only 450 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown will activate, turning off the output and reducing the output current to 0. As the junction temperature cools and drops below 135°C, the output turns on and conducts 450 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 450 mA and 0 mA, which continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions.

## THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP170/ADP171 must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air ($\theta_{JA}$). The $\theta_{JA}$ number is dependent on the package assembly compounds used and the amount of copper to which the GND pin of the package is soldered on the PCB. Table 6 shows typical $\theta_{JA}$ values of the 5-lead TSOT package for various PCB copper sizes.

**Table 6. Typical $\theta_{JA}$ Values**

| Copper Size (mm²) | $\theta_{JA}$ (°C/W) |
|---|---|
| 0[1] | 170 |
| 50 | 152 |
| 100 | 146 |
| 300 | 134 |
| 500 | 131 |

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP170/ADP171 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
$T_A$ is the ambient temperature.
$P_D$ is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:
$I_{LOAD}$ is the load current.
$I_{GND}$ is the ground current.
$V_{IN}$ and $V_{OUT}$ are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 33 to Figure 38 show junction temperature calculations for different ambient temperatures, load currents, $V_{IN}$ to $V_{OUT}$ differentials, and areas of PCB copper.

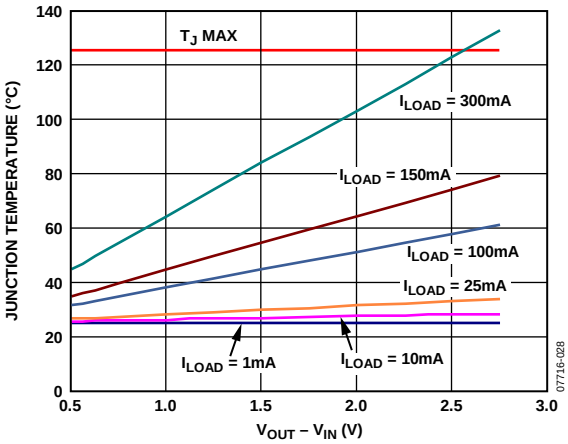



*Figure 33. 500 mm² of PCB Copper, $T_A$ = 25°C*

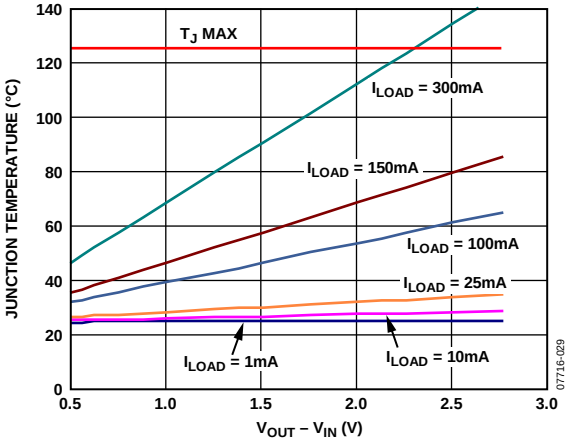



*Figure 34. 100 mm² of PCB Copper, $T_A$ = 25°C*

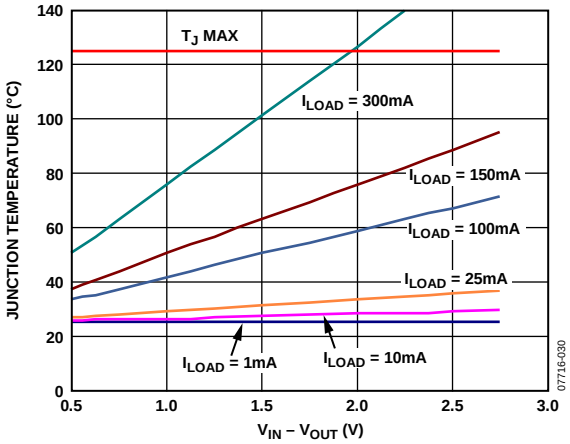



Figure 35. 0 mm² of PCB Copper, $T_A$ = 25°C

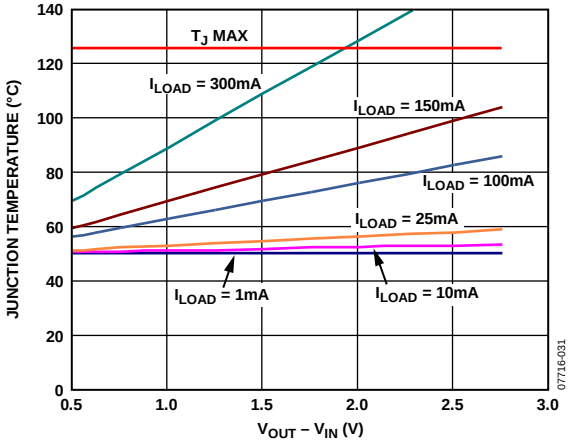



Figure 36. 500 mm² of PCB Copper, $T_A$ = 50°C

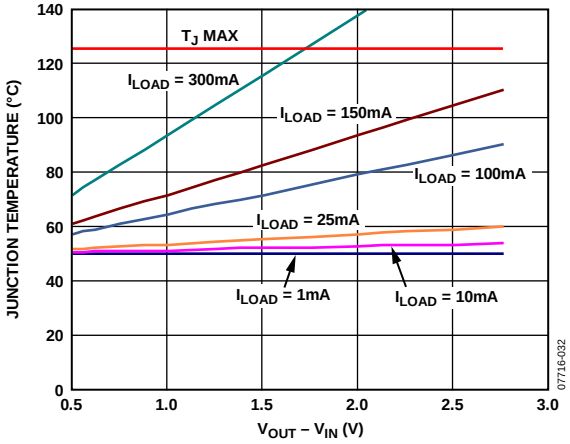



Figure 37. 100 mm² of PCB Copper, $T_A$ = 50°C

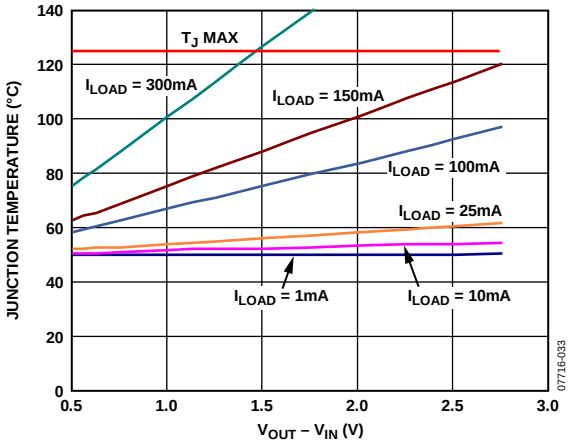



Figure 38. 0 mm² of PCB Copper, $T_A$ = 50°C

In cases where board temperature is known, use the thermal characterization parameter, $\Psi_{JB}$, to estimate the junction temperature rise (see Figure 39). Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (5)$$

The typical value of $\Psi_{JB}$ is 42.8°C/W for the 5-lead TSOT package.

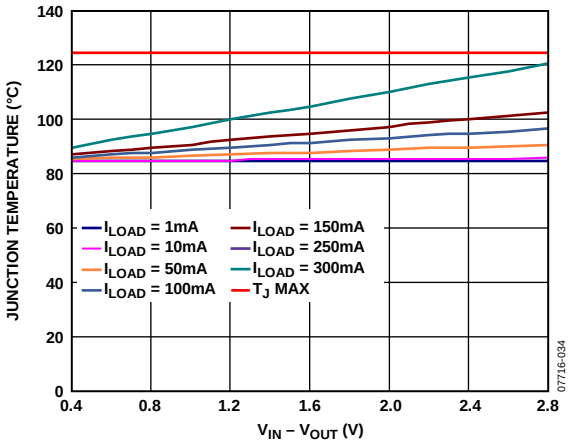



Figure 39. TSOT, $T_A$ = 85°C

## PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP170/ADP171. However, as can be seen from Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

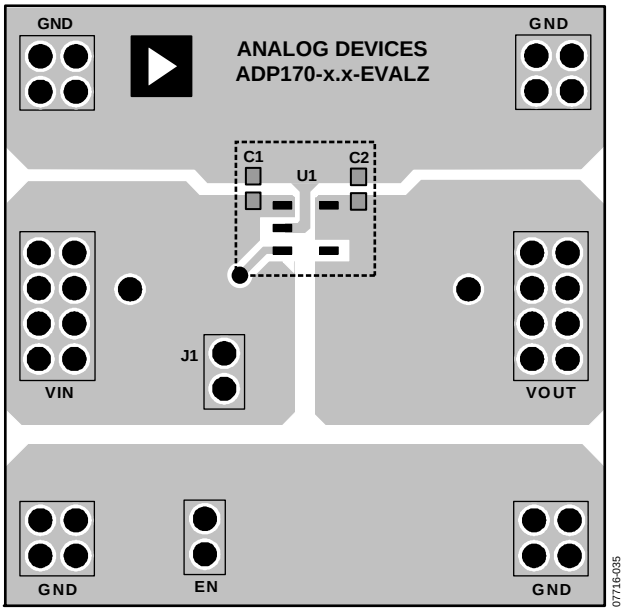



*Figure 40. Example ADP170 PCB Layout*

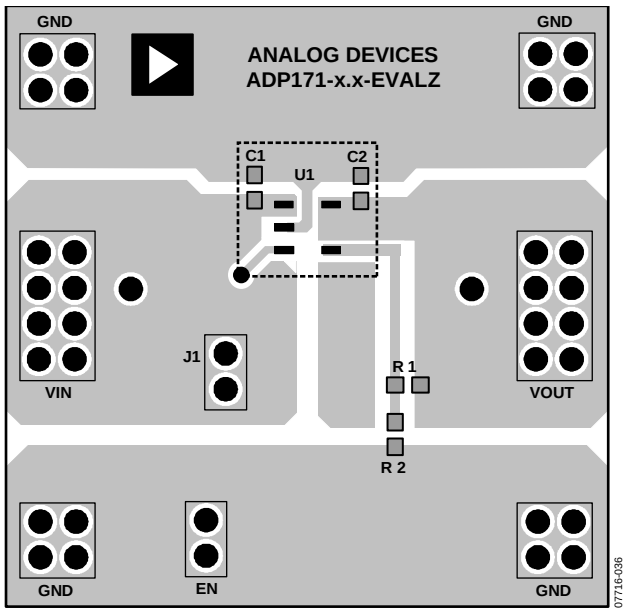



*Figure 41. Example ADP171 PCB Layout*

# OUTLINE DIMENSIONS

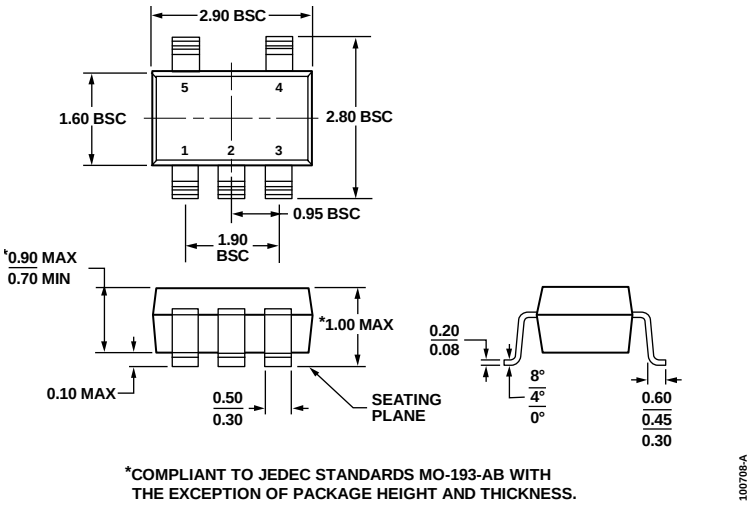



*Figure 42. 5-Lead Thin Small Outline Transistor Package [TSOT] (UJ-5)*
*Dimensions show in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Output Voltage (V)[2] | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| ADP170AUJZ-1.2-R7 | –40°C to +125°C | 1.2 | 5-Lead TSOT | UJ-5 | L8E |
| ADP170AUJZ-1.25-R7 | –40°C to +125°C | 1.25 | 5-Lead TSOT | UJ-5 | LQD |
| ADP170AUJZ-1.5-R7 | –40°C to +125°C | 1.5 | 5-Lead TSOT | UJ-5 | L8F |
| ADP170AUJZ-1.8-R7 | –40°C to +125°C | 1.8 | 5-Lead TSOT | UJ-5 | L8G |
| ADP170AUJZ-2.5-R7 | –40°C to +125°C | 2.5 | 5-Lead TSOT | UJ-5 | L8H |
| ADP170AUJZ-2.8-R7 | –40°C to +125°C | 2.8 | 5-Lead TSOT | UJ-5 | L8P |
| ADP171AUJZ-R7 | –40°C to +125°C | 0.8 to 3.0 (Adjustable) | 5-Lead TSOT | UJ-5 | L9A |
| ADP170-1.8-EVALZ | | | Evaluation Board | | |
| ADP171-EVALZ | | | Evaluation Board | | |

[1] Z = RoHS Compliant Part.
[2] For additional voltage options, contact your local Analog Devices, Inc., sales or distribution representative.

## NOTES

## NOTES

## NOTES

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