WINSOURCE ELECTRONICS

THE DATASHEET OF

ADP1710AUJZ-R7

150 mA, Low Dropout, CMOS Linear Regulator

ADP1710/ADP1711

FEATURES

Maximum output current: 150 mA
Input voltage range: 2.5 V to 5.5 V
Light load efficient
- **I_{GND} = 35 µA with zero load**
- **I_{GND} = 40 µA with 100 µA load**

Low shutdown current: <1 µA
Low dropout voltage: 150 mV @ 150 mA load
Initial accuracy: ±1%
Accuracy over line, load, and temperature: ±2%
Stable with small 1µF ceramic output capacitor
16 fixed output voltage options: 0.75 V to 3.3 V (ADP1710)
Adjustable output voltage option: 0.8 V to 5.0 V (ADP1710 Adjustable)
16 fixed output voltage options with reference bypass: 0.75 V to 3.3 V (ADP1711)
High PSRR: 69 dB @ 1 kHz
Low noise: 40 µV_{RMS}
Excellent load/line transient response
Current limit and thermal overload protection
Logic controlled enable
5-lead TSOT package

APPLICATIONS

Mobile phones
Digital camera and audio devices
Portable and battery-powered equipment
Post dc-dc regulation

TYPICAL APPLICATION CIRCUITS

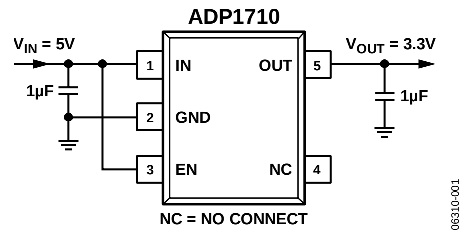

Figure 1. ADP1710 with Fixed Output Voltage, 3.3 V

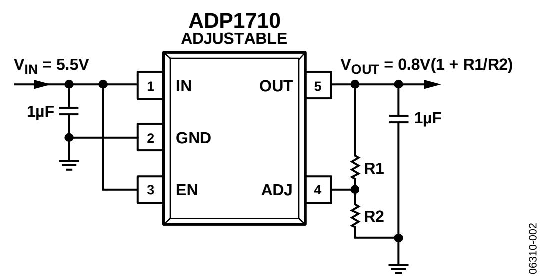

Figure 2. ADP1710 with Adjustable Output Voltage, 0.8 V to 5.0 V

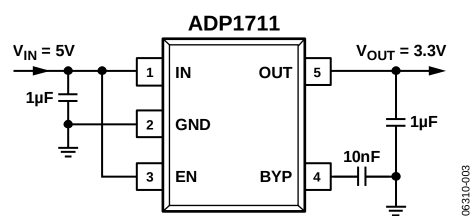

Figure 3. ADP1711 with Fixed Output Voltage and Bypass Capacitor, 3.3 V

GENERAL DESCRIPTION

The ADP1710/ADP1711 are low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 150 mA of output current. Utilizing a novel scaling architecture, ground current drawn is a very low 40 µA, when driving a 100 µA load, making the ADP1710/ADP1711 ideal for battery-operated portable equipment.

The ADP1710 and the ADP1711 are each available in sixteen fixed output voltage options. The ADP1710 is also available in an adjustable version, which allows output voltages that range from 0.8 V to 5 V via an external divider. The ADP1711 allows for a reference bypass capacitor to be connected, which reduces output voltage noise and improves power supply rejection.

The ADP1710/ADP1711 are optimized for stable operation with small 1 µF ceramic output capacitors, allowing for good transient performance while occupying minimal board space. An enable pin controls the output voltage on both devices. There is also an under-voltage lockout circuit on both devices, which disables the regulator if IN drops below a minimum threshold.

An internal soft start gives a typical start-up time of 80 µs. Short-circuit protection and thermal overload protection circuits prevent damage to the devices in adverse conditions. Both the ADP1710 and the ADP1711 are available in tiny 5-lead TSOT packages, for the smallest footprint solution to all your power needs.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.5 V (whichever is greater), I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		35		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			50	µA
		I_{OUT} = 100 µA		40		µA
		I_{OUT} = 100 µA, T_J = −40°C to +125°C			80	µA
		I_{OUT} = 100 mA		665		µA
		I_{OUT} = 100 mA, T_J = −40°C to +125°C			860	µA
		I_{OUT} = 150 mA		1		mA
		I_{OUT} = 150 mA, T_J = −40°C to +125°C			1.3	mA
SHUTDOWN CURRENT	$I_{GND\text{-}SD}$	EN = GND		0.1		µA
		EN = GND, T_J = −40°C to +125°C			1.0	µA
FIXED OUTPUT VOLTAGE ACCURACY (ADP1710 AND ADP1711)	V_{OUT}	I_{OUT} = 1 mA	−1		+1	%
		100 µA < I_{OUT} < 150 mA, T_J = −40°C to +125°C	−2		+2	%
ADJUSTABLE OUTPUT VOLTAGE ACCURACY (ADP1710 ADJUSTABLE)[1]	V_{OUT}	I_{OUT} = 1 mA	0.792	0.8	0.808	V
		100 µA < I_{OUT} < 150 mA, T_J = −40°C to +125°C	0.784		0.816	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.1		+0.1	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 10 mA to 150 mA		0.002		%/mA
		I_{OUT} = 10 mA to 150 mA, T_J = −40°C to +125°C			0.004	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	I_{OUT} = 100 mA, V_{OUT} ≥ 3.0 V		100		mV
		I_{OUT} = 100 mA, V_{OUT} ≥ 3.0 V, T_J = −40°C to +125°C			175	mV
		I_{OUT} = 150 mA, V_{OUT} ≥ 3.0 V		150		mV
		I_{OUT} = 150 mA, V_{OUT} ≥ 3.0 V, T_J = −40°C to +125°C			250	mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.0 V		120		mV
		I_{OUT} = 100 mA, 2.5 V ≤ V_{OUT} < 3.0 V, T_J = −40°C to +125°C			200	mV
		I_{OUT} = 150 mA, 2.5 V ≤ V_{OUT} < 3.0 V		180		mV
		I_{OUT} = 150 mA, 2.5 V ≤ V_{OUT} < 3.0 V, T_J = −40°C to +125°C			300	mV
START-UP TIME[4]	$T_{START\text{-}UP}$					
ADP1710				80		µs
ADP1711		With 10 nF bypass capacitor		100		µs
CURRENT LIMIT THRESHOLD[5]	I_{LIMIT}		180	270	360	mA
THERMAL SHUTDOWN THRESHOLD	TS_{SD}	T_J rising		150		°C
THERMAL SHUTDOWN HYSTERESIS	$TS_{SD\text{-}HYS}$			15		°C
UVLO ACTIVE THRESHOLD	$UVLO_{ACTIVE}$	V_{IN} falling	1.95			V
UVLO INACTIVE THRESHOLD	$UVLO_{INACTIVE}$	V_{IN} rising			2.45	V
UVLO HYSTERESIS	$UVLO_{HYS}$			250		mV
EN INPUT LOGIC HIGH	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.8			V
EN INPUT LOGIC LOW	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
EN INPUT LEAKAGE CURRENT	$V_{I\text{-}LEAKAGE}$	EN = IN or GND		0.1	1	µA
ADJ INPUT BIAS CURRENT (ADP1710 ADJUSTABLE)	$ADJ_{I\text{-}BIAS}$			30	100	nA
OUTPUT NOISE	OUT_{NOISE}					
ADP1710		10 Hz to 100 kHz, V_{OUT} = 3.3 V		330		µVrms
ADP1711		10 Hz to 100 kHz, V_{OUT} = 0.75 V, with 10 nF bypass capacitor		40		µVrms
POWER SUPPLY REJECTION RATIO	PSRR					
ADP1710		1 kHz, V_{OUT} = 3.3 V		58		dB
ADP1711		1 kHz, V_{OUT} = 0.75 V, with 10 nF bypass capacitor		69		dB

[1] Accuracy when OUT is connected directly to ADJ. When OUT voltage is set by external feedback resistors, absolute accuracy in adjust mode depends on the tolerances of resistors used.
[2] Based on an end-point calculation using 10 mA and 150 mA loads. See Figure 8 for typical load regulation performance for loads less than 10 mA.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[4] Start-up time is defined as the time between the rising edge of EN to OUT being at 90% of its nominal value.
[5] Current limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 1.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 1.0 V, or 0.9 V.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
IN to GND	–0.3 V to +6 V
OUT to GND	–0.3 V to IN
EN to GND	–0.3 V to +6 V
ADJ/BYP to GND	–0.3 V to +6 V
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

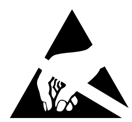
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
5-Lead TSOT	170	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

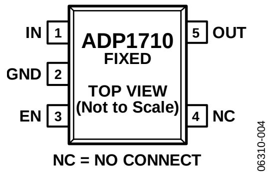


Figure 4. 5-Lead TSOT (UJ-Suffix)

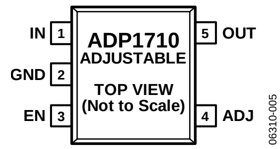


Figure 5. 5-Lead TSOT (UJ-Suffix)

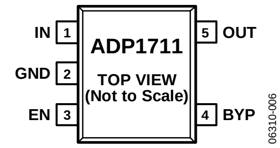


Figure 6. 5-Lead TSOT (UJ-Suffix)

Table 4. Pin Function Descriptions

ADP1710 Fixed Pin No.	ADP1710 Adjustable Pin No.	ADP1711 Pin No.	Mnemonic	Description
1	1	1	IN	Regulator Input Supply. Bypass IN to GND with a 1 µF or greater capacitor.
2	2	2	GND	Ground.
3	3	3	EN	Enable Input. Drive EN high to turn on the regulator; drive it low to turn off the regulator. For automatic startup, connect EN to IN.
4			NC	No Connect.
	4		ADJ	Adjust. A resistor divider from OUT to ADJ sets the output voltage.
		4	BYP	Connect a 1 nF or greater capacitor (10 nF is recommended) between BYP and GND to reduce the internal reference noise for low noise applications.
5	5	5	OUT	Regulated Output Voltage. Bypass OUT to GND with a 1 µF or greater capacitor.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, T_A = 25°C, unless otherwise noted.

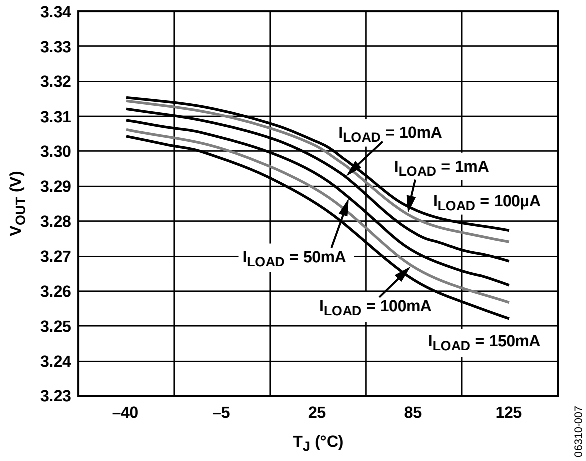


Figure 7. Output Voltage vs. Junction Temperature

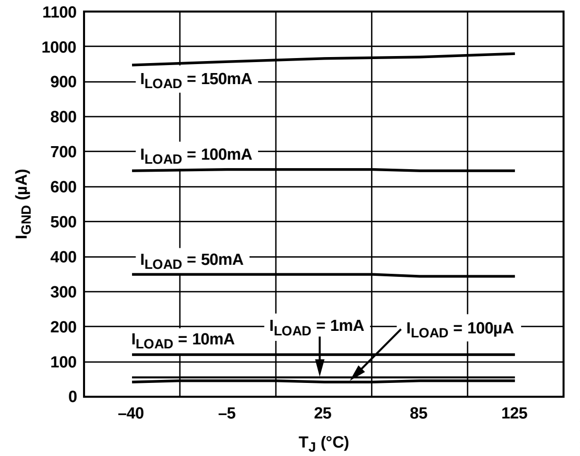


Figure 10. Ground Current vs. Junction Temperature

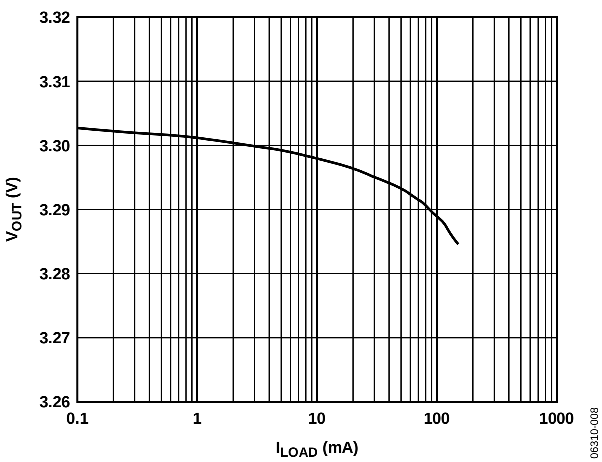


Figure 8. Output Voltage vs. Load Current

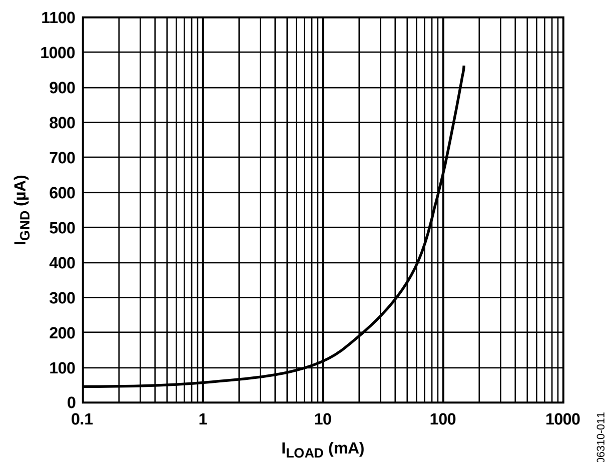


Figure 11. Ground Current vs. Load Current

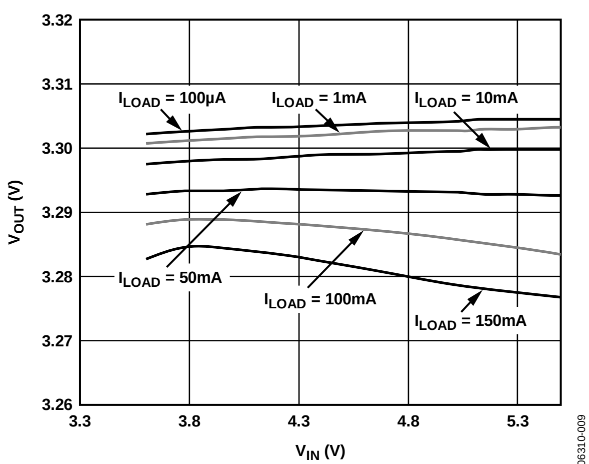


Figure 9. Output Voltage vs. Input Voltage

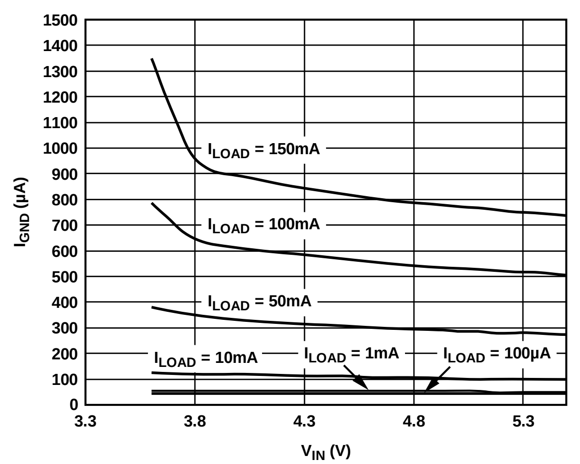


Figure 12. Ground Current vs. Input Voltage

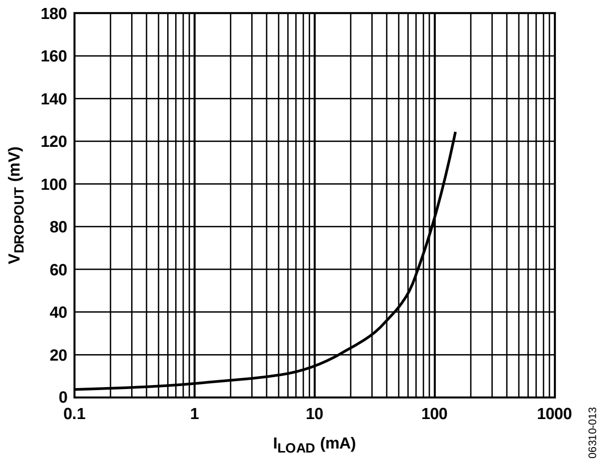


Figure 13. Dropout Voltage vs. Load Current

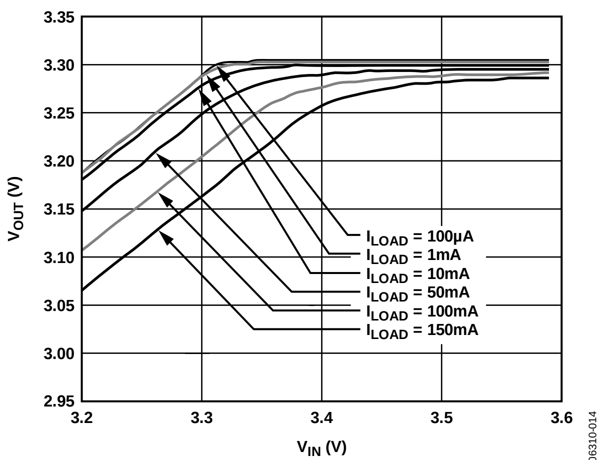


Figure 14. Output Voltage vs. Input Voltage (in Dropout)

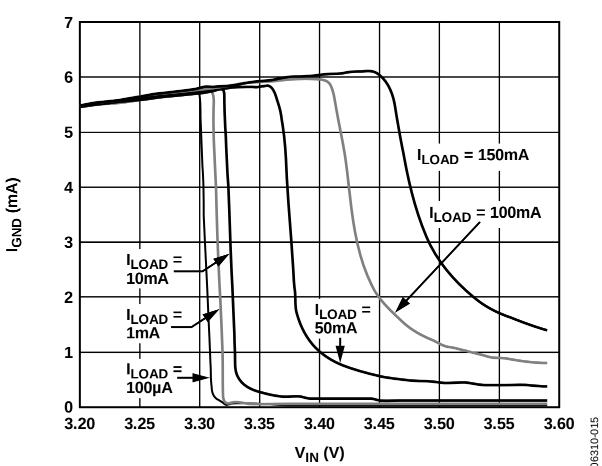


Figure 15. Ground Current vs. Input Voltage (In Dropout)

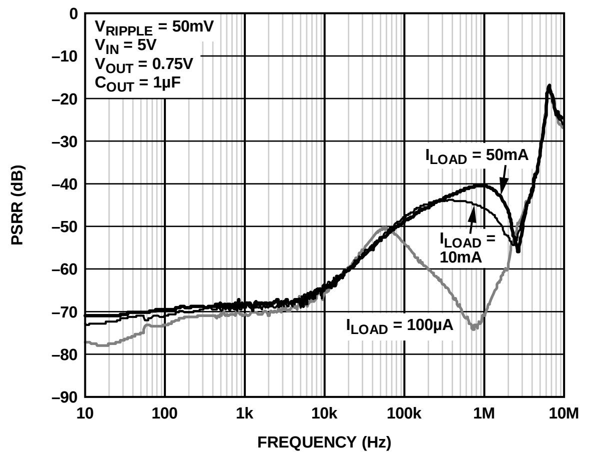


Figure 16. ADP1711 Power Supply Rejection Ratio vs. Frequency (10 nF Bypass Capacitor)

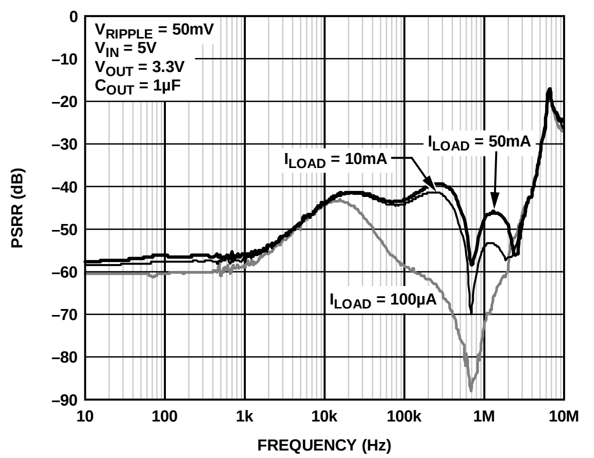


Figure 17. ADP1710 Power Supply Rejection Ratio vs. Frequency

THEORY OF OPERATION

The ADP1710/ADP1711 are low dropout, CMOS linear regulators that use an advanced, proprietary architecture to provide high power supply rejection ratio (PSRR) and excellent line and load transient response with just a small 1 μF ceramic output capacitor. Both devices operate from a 2.5 V to 5.5 V input rail and provide up to 150 mA of output current. Incorporating a novel scaling architecture, ground current is very low when driving light loads. Ground current in shutdown mode is typically 100 nA.

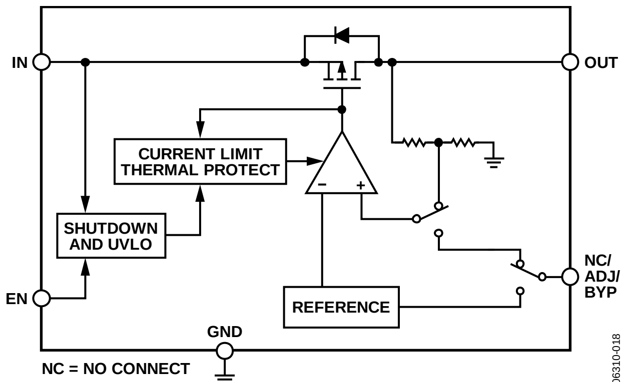


Figure 18. Internal Block Diagram

Internally, the ADP1710/ADP1711 each consist of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP1710 is available in two versions, one with fixed output voltage options and one with an adjustable output voltage. The fixed output voltage option is set internally to one of sixteen values between 0.75 V and 3.3 V, using an internal feedback network. The adjustable output voltage can be set to between 0.8 V and 5.0 V by an external voltage divider connected from OUT to ADJ. The ADP1711 is available with fixed output voltage options and features a bypass pin, which allows an external capacitor to be connected, which reduces internal reference noise. All devices are controlled by an enable pin (EN).

ADJUSTABLE OUTPUT VOLTAGE (ADP1710 ADJUSTABLE)

The ADP1710 adjustable version can have its output voltage set over a 0.8 V to 5.0 V range. The output voltage is set by connecting a resistive voltage divider from OUT to ADJ. The output voltage is calculated using the equation

$$V_{OUT} = 0.8\text{ V } (1 + R1/R2) \quad (1)$$

where:

R1 is the resistor from OUT to ADJ.
R2 is the resistor from ADJ to GND.

The maximum bias current into ADJ is 100 nA, so for less than 0.5% error due to the bias current, use values less than 60 kΩ for R2.

BYPASS CAPACITOR (ADP1711)

The ADP1711 allows for an external bypass capacitor to be connected to the internal reference, which reduces output voltage noise and improves power supply rejection. A low leakage capacitor of 1 nF or greater (10 nF is recommended) must be connected between the BYP and GND pins.

ENABLE FEATURE

The ADP1710/ADP1711 use the EN pin to enable and disable the OUT pin under normal operating conditions. As shown in Figure 19, when a rising voltage on EN crosses the active threshold, OUT turns on. When a falling voltage on EN crosses the inactive threshold, OUT turns off.

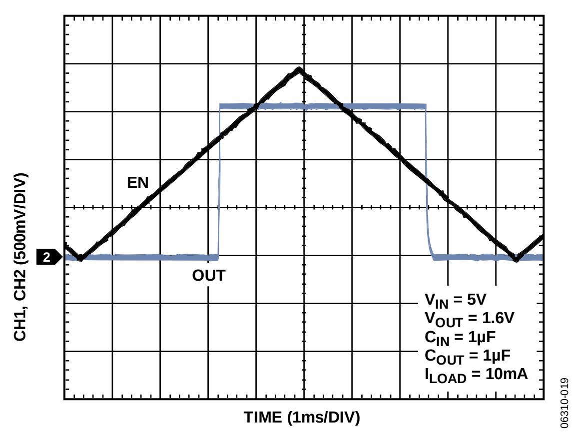


Figure 19. ADP1710 Adjustable Typical EN Pin Operation

As can be seen, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds are derived from the IN voltage. Therefore, these thresholds vary with changing input voltage. Figure 20 shows typical EN active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

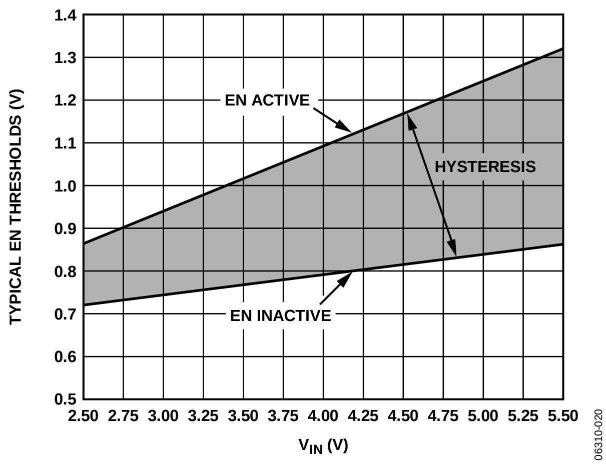


Figure 20. Typical EN Pin Thresholds vs. Input Voltage

UNDERVOLTAGE LOCKOUT (UVLO)

The ADP1710/ADP1711 have an undervoltage lockout circuit, which monitors the voltage on the IN pin. When the voltage on IN drops below 1.95 V (minimum), the circuit activates, disabling the OUT pin.

APPLICATION INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1710/ADP1711 are designed for operation with small, space-saving ceramic capacitors, but they will function with most commonly used capacitors as long as care is taken about the effective series resistance (ESR) value. The ESR of the output capacitor affects stability of the LDO control loop. A minimum of 1 μF capacitance with an ESR of 500 mΩ or less is recommended to ensure stability of the ADP1710/ADP1711. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1710/ADP1711 to large changes in load current. Figure 21 and Figure 22 show the transient responses for output capacitance values of 1 μF and 22 μF, respectively.

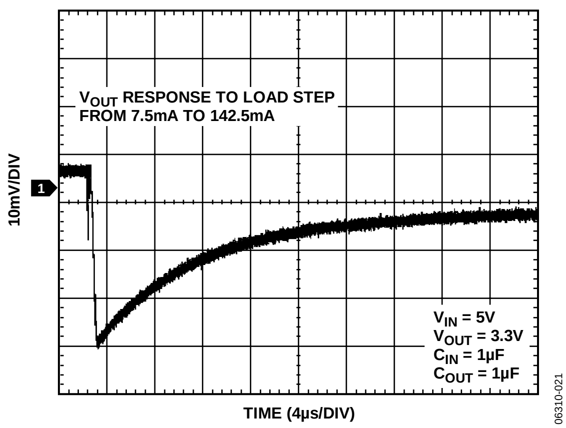


Figure 21. Output Transient Response, C_{OUT} = 1 μF

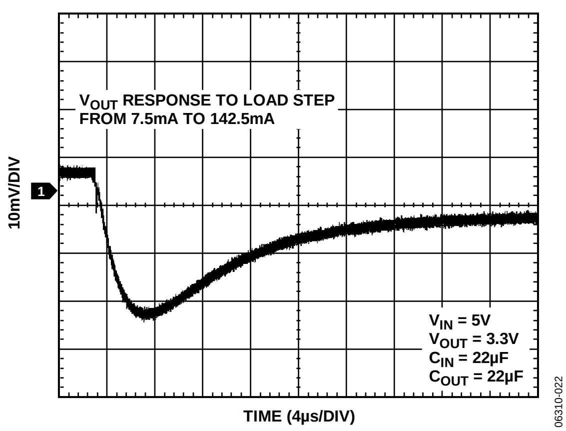


Figure 22. Output Transient Response, C_{OUT} = 22 μF

Input Bypass Capacitor

Connecting a 1 μF capacitor from IN to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 μF of output capacitance is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1710/ADP1711, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1710/ADP1711 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP1710/ADP1711 are designed to current limit when the output load reaches 270 mA (typical). When the output load exceeds 270 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again and output current is restored to its nominal value.

Consider the case where a hard short from OUT to ground occurs. At first the ADP1710/ADP1711 current limits, so that only 270 mA is conducted into the short. If self heating of the junction is great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 270 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 270 mA and 0 mA, which continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1710/ADP1711 must not exceed 125°C. To ensure the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds used and the amount of copper to which the GND pins of the package are soldered on the PCB. Table 5 shows typical θ_{JA} values of the 5-lead TSOT package for various PCB copper sizes.

Table 5.

Copper Size (mm²)	θ_{JA} (°C/W)
0[1]	170
50	152
100	146
300	134
500	131

[1] Device soldered to minimum size pin traces.

The junction temperature of the ADP1710/ADP1711 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:

T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (3)$$

where:

I_{LOAD} is the load current.
I_{GND} is the ground current.
V_{IN} and V_{OUT} are the input voltage and output voltage, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (4)$$

As shown in Equation 4, for a given ambient temperature, input to output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure the junction temperature does not rise above 125°C. The following figures show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

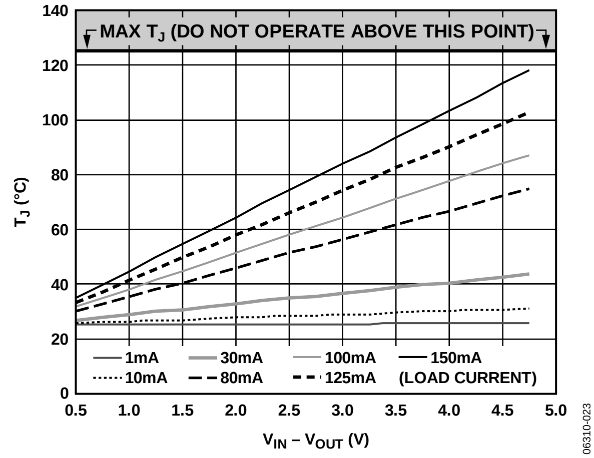


Figure 23. 500 mm² of PCB Copper, T_A = 25°C

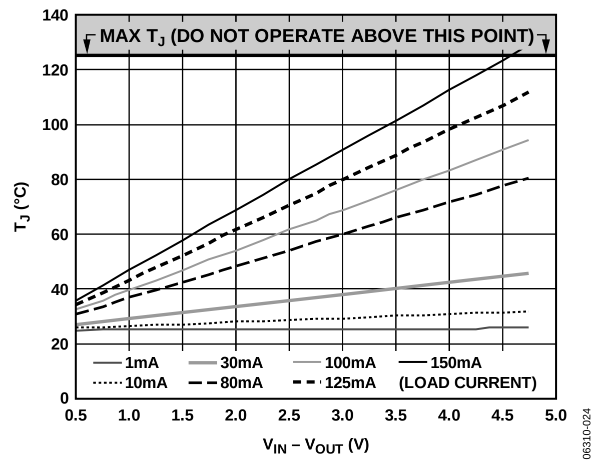


Figure 24. 100 mm² of PCB Copper, T_A = 25°C

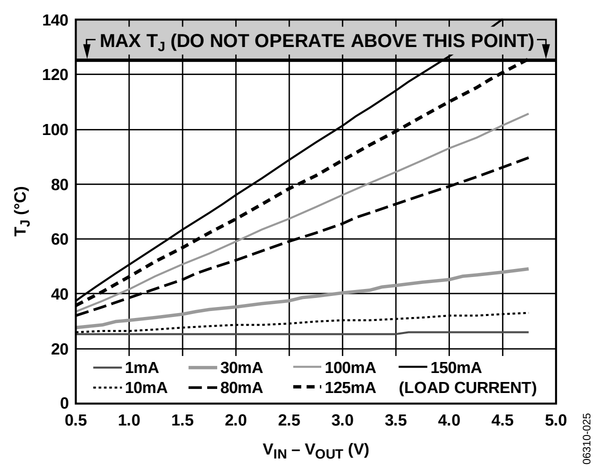


Figure 25. 0 mm² of PCB Copper, T_A = 25°C

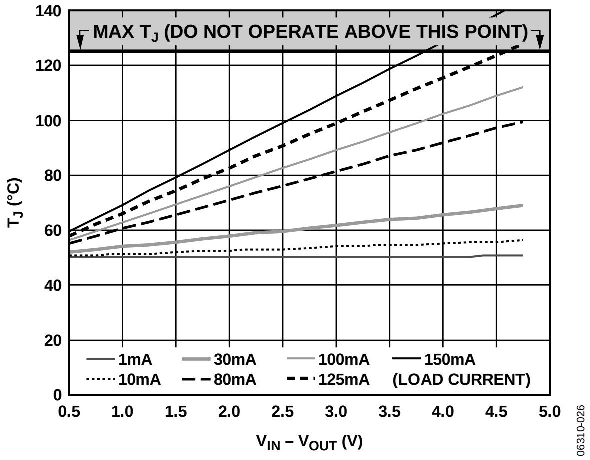


Figure 26. 500 mm² of PCB Copper, $T_A = 50°C$

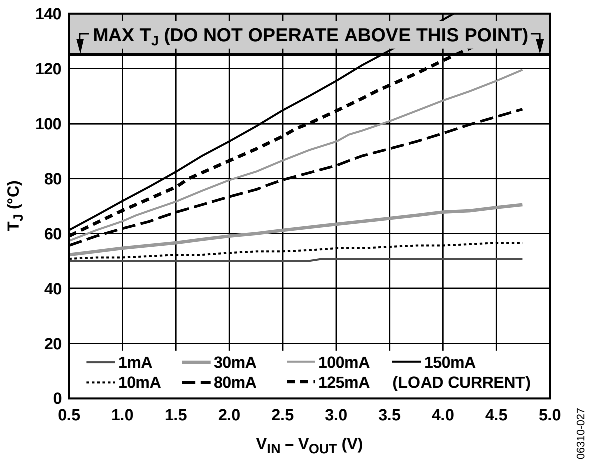


Figure 27. 100 mm² of PCB Copper, $T_A = 50°C$

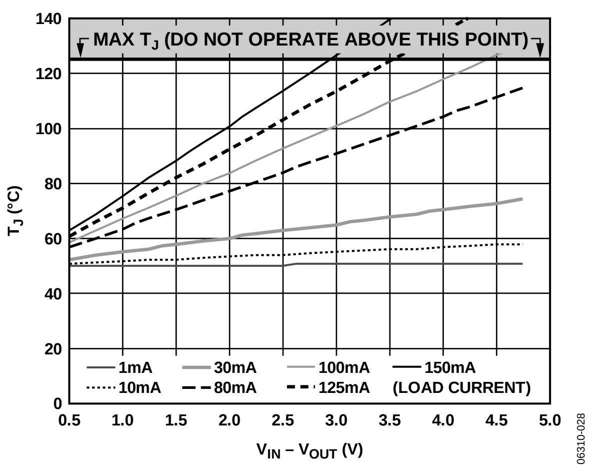


Figure 28. 0 mm² of PCB Copper, $T_A = 50°C$

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP1710/ ADP1711. However, as can be seen from Table 5, a point of diminishing returns eventually is reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the IN and GND pins. Place the output capacitor as close as possible to the OUT and GND pins. For ADP1711, place the internal reference bypass capacitor as close as possible to the BYP pin. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

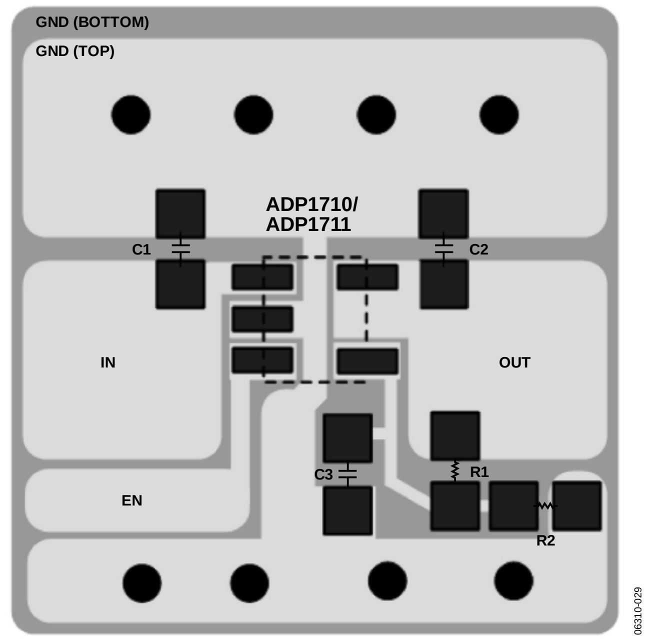


Figure 29. Example PCB Layout

OUTLINE DIMENSIONS

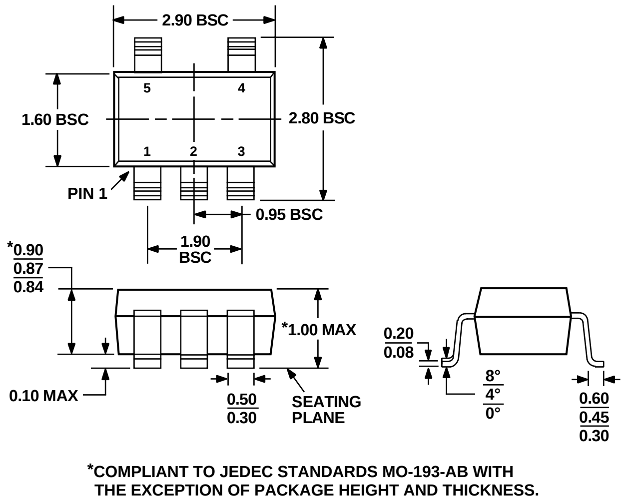


Figure 30. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions show in millimeters

ORDERING GUIDE

Model	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP1710AUJZ-0.75R7[1]	–40°C to +125°C	0.75	5-Lead TSOT	UJ-5	L4S
ADP1710AUJZ-0.8-R7[1]	–40°C to +125°C	0.80	5-Lead TSOT	UJ-5	L0D
ADP1710AUJZ-0.85R7[1]	–40°C to +125°C	0.85	5-Lead TSOT	UJ-5	L40
ADP1710AUJZ-0.9-R7[1]	–40°C to +125°C	0.90	5-Lead TSOT	UJ-5	L41
ADP1710AUJZ-0.95R7[1]	–40°C to +125°C	0.95	5-Lead TSOT	UJ-5	L42
ADP1710AUJZ-1.0-R7[1]	–40°C to +125°C	1.00	5-Lead TSOT	UJ-5	L0E
ADP1710AUJZ-1.05R7[1]	–40°C to +125°C	1.05	5-Lead TSOT	UJ-5	L43
ADP1710AUJZ-1.10R7[1]	–40°C to +125°C	1.10	5-Lead TSOT	UJ-5	L47
ADP1710AUJZ-1.15R7[1]	–40°C to +125°C	1.15	5-Lead TSOT	UJ-5	L44
ADP1710AUJZ-1.2-R7[1]	–40°C to +125°C	1.20	5-Lead TSOT	UJ-5	L45
ADP1710AUJZ-1.3-R7[1]	–40°C to +125°C	1.30	5-Lead TSOT	UJ-5	L46
ADP1710AUJZ-1.5-R7[1]	–40°C to +125°C	1.50	5-Lead TSOT	UJ-5	L0F
ADP1710AUJZ-1.8-R7[1]	–40°C to +125°C	1.80	5-Lead TSOT	UJ-5	L0G
ADP1710AUJZ-2.5-R7[1]	–40°C to +125°C	2.50	5-Lead TSOT	UJ-5	L0H
ADP1710AUJZ-3.0-R7[1]	–40°C to +125°C	3.00	5-Lead TSOT	UJ-5	L0J
ADP1710AUJZ-3.3-R7[1]	–40°C to +125°C	3.30	5-Lead TSOT	UJ-5	L0K
ADP1710AUJZ-R7[1]	–40°C to +125°C	0.8 to 5.0	5-Lead TSOT	UJ-5	L0L
ADP1711AUJZ-0.75R7[1]	–40°C to +125°C	0.75	5-Lead TSOT	UJ-5	L4T
ADP1711AUJZ-0.8-R7[1]	–40°C to +125°C	0.80	5-Lead TSOT	UJ-5	L0M
ADP1711AUJZ-0.85R7[1]	–40°C to +125°C	0.85	5-Lead TSOT	UJ-5	L48
ADP1711AUJZ-0.9-R7[1]	–40°C to +125°C	0.90	5-Lead TSOT	UJ-5	L49
ADP1711AUJZ-0.95R7[1]	–40°C to +125°C	0.95	5-Lead TSOT	UJ-5	L4A
ADP1711AUJZ-1.0-R7[1]	–40°C to +125°C	1.00	5-Lead TSOT	UJ-5	L0N
ADP1711AUJZ-1.05R7[1]	–40°C to +125°C	1.05	5-Lead TSOT	UJ-5	L4C
ADP1711AUJZ-1.10R7[1]	–40°C to +125°C	1.10	5-Lead TSOT	UJ-5	L4G
ADP1711AUJZ-1.15R7[1]	–40°C to +125°C	1.15	5-Lead TSOT	UJ-5	L4D
ADP1711AUJZ-1.2-R7[1]	–40°C to +125°C	1.20	5-Lead TSOT	UJ-5	L4E
ADP1711AUJZ-1.3-R7[1]	–40°C to +125°C	1.30	5-Lead TSOT	UJ-5	L4F
ADP1711AUJZ-1.5-R7[1]	–40°C to +125°C	1.50	5-Lead TSOT	UJ-5	L0P
ADP1711AUJZ-1.8-R7[1]	–40°C to +125°C	1.80	5-Lead TSOT	UJ-5	L0Q
ADP1711AUJZ-2.5-R7[1]	–40°C to +125°C	2.50	5-Lead TSOT	UJ-5	L0R
ADP1711AUJZ-3.0-R7[1]	–40°C to +125°C	3.00	5-Lead TSOT	UJ-5	L0S
ADP1711AUJZ-3.3-R7[1]	–40°C to +125°C	3.30	5-Lead TSOT	UJ-5	L0U

[1] Z = Pb-free part.

NOTES

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