THE DATASHEET OF

ADP1821ARQZ-R7

Step-Down DC-to-DC Controller

ADP1821

FEATURES

Wide power-input voltage range: 1 V to 24 V
Chip supply voltage range: 3.7 V to 5.5 V
Wide output voltage range: 0.6 V to 85% of input voltage
1% accuracy, 0.6 V reference voltage
All N-channel MOSFET design for low cost
Fixed-frequency operation 300 kHz, 600 kHz, or synchronized operation up to 1.2 MHz
No current sense resistor required
Power-good output
Programmable soft start with reverse current protection
Soft start, thermal overload, current-limit protection
Undervoltage lockout
10 µA shutdown supply current
Small, 16-lead QSOP

APPLICATIONS

Telecommunications and networking systems
Set-top boxes
Printers
Servers
Medical imaging systems
Microprocessor and DSP core power supplies
Mobile communication base stations

GENERAL DESCRIPTION

The ADP1821 is a versatile and inexpensive, synchronous, pulse-width-modulated (PWM), voltage-mode, step-down controller. It drives an all N-channel power stage to regulate an output voltage as low as 0.6 V. The ADP1821 can be configured to provide output voltages from 0.6 V to 85% of the input voltage and is sized to handle large MOSFETs for point-of-load regulators.

The ADP1821 is well suited for a wide range of high power applications, such as DSP and processor core power in telecommunications, medical imaging, high performance servers, and industrial applications. It operates from a 3.7 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a pin-selectable, fixed switching frequency of either 300 kHz or 600 kHz, minimizing external component size and cost. For noise sensitive applications, it can be synchronized to an external clock to achieve switching frequencies between 300 kHz and 1.2 MHz. The ADP1821 includes soft start protection to limit the inrush current from the input supply during startup, reverse current protection during soft start for precharged outputs, as well as a unique adjustable lossless current-limit scheme utilizing external MOSFET sensing.

The ADP1821 operates over the –40°C to +125°C junction temperature range and is available in a 16-lead QSOP.

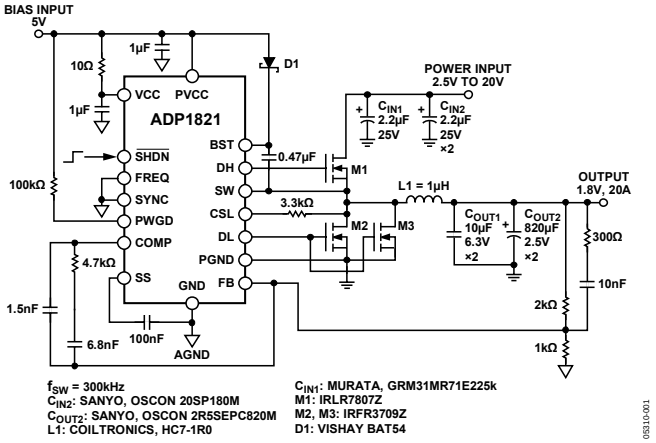

Figure 1. Typical Operating Circuit

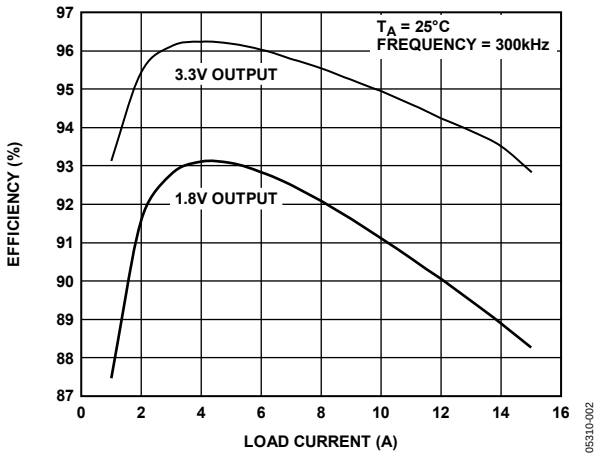

Figure 2. Efficiency vs. Load Current, 5 V Input

Rev. C

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7/05—Revision 0: Initial Version

SPECIFICATIONS

$V_{VCC} = V_{PVCC} = V_{\overline{SHDN}} = V_{FREQ}$ = 5 V, SYNC = GND. All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). T_J = −40°C to +125°C, unless otherwise specified. Typical values are at T_A=25°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Input Voltage		3.7		5.5	V
Undervoltage Lockout Threshold	V_{VCC} rising, T_J = −40°C to +125°C	2.4	2.7	3.0	V
Undervoltage Lockout Threshold	V_{VCC} rising, T_A = 25°C	2.5	2.7	2.9	V
Undervoltage Lockout Hysteresis	V_{VCC}		0.1		V
Quiescent Current	I_{VCC} + I_{VCC}, not switching		1	2	mA
Shutdown Current	$\overline{SHDN}$ = GND			10	µA
Power Stage Supply Voltage		1.0		24	V
ERROR AMPLIFIER					
FB Regulation Voltage	T_J = −40°C to +85°C	594	600	606	mV
FB Regulation Voltage	T_J = −40°C to +125°C	588	600	606	mV
FB Input Bias Current		−100	+1	+100	nA
Error Amplifier Open-Loop Voltage Gain			70		dB
COMP Output Sink Current			600		µA
COMP Output Source Current			110		µA
COMP Clamp High Voltage			2.4		V
COMP Clamp Low Voltage			0.75		V
PWM CONTROLLER					
PWM Peak Ramp Voltage			1.25		V
DL Minimum On Time	FREQ = VCC (300 kHz)	120	170	220	ns
DL Minimum On-Time	FREQ = VCC (300 kHz), T_A = 25°C	140	170	200	ns
DH Maximum Duty Cycle	FREQ = GND (300 kHz)	85	90		%
DH Minimum Duty Cycle	FREQ = GND (300 kHz)		1	3	%
SOFT START					
SS Pull-Up Resistance	SS = GND		95		kΩ
SS Pull-Down Resistance	V_{SS} = 0.6 V	1.65	2.5	4.2	kΩ
OSCILLATOR					
Oscillator Frequency	FREQ = GND	250	310	375	kHz
	FREQ = VCC	470	570	720	kHz
Synchronization Range	FREQ = GND	300		600	kHz
	FREQ = VCC	600		1200	kHz
SYNC Minimum Pulse Width				80	ns
CURRENT SENSE					
CSL Threshold Voltage	Relative to PGND	−30	0	+30	mV
CSL Output Current	V_{CSL} = 0 V	42	50	54	µA
Current Sense Blanking Period			160		ns
GATE DRIVERS					
DH Rise Time	C_{GATE} = 3 nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW}$ = 5 V		16		ns
DH Fall Time	C_{GATE} = 3 nF, $V_{DH} = V_{IN}$, $V_{BST} - V_{SW}$ = 5 V		12		ns
DL Rise Time	C_{GATE} = 3 nF, $V_{DL} = V_{IN}$		19		ns
DL Fall Time	C_{GATE} = 3 nF, V_{DL} = 0 V		13		ns
DL Low to DH High Dead Time			33		ns
DH Low to DL High Dead Time			42		ns

Parameter	Conditions	Min	Typ	Max	Unit
LOGIC THRESHOLDS ($\overline{SHDN}$, SYNC, FREQ)					
$\overline{SHDN}$, SYNC, FREQ Input High Voltage	V_{VCC} = 3.7 V to 5.5 V	2.0			V
$\overline{SHDN}$, SYNC, FREQ Input Low Voltage	V_{VCC} = 3.7 V to 5.5 V			0.8	V
SYNC, FREQ Input Leakage Current	SYNC = FREQ = GND		0.1	1	µA
$\overline{SHDN}$ Pull-Down Resistance			100		kΩ
THERMAL SHUTDOWN					
Thermal Shutdown Threshold			145		°C
Thermal Shutdown Hysteresis			10		°C
PWGD OUTPUT					
FB Overvoltage Threshold	V_{FB} rising		750		mV
FB Overvoltage Hysteresis			35		mV
FB Undervoltage Threshold	V_{FB} rising		550		mV
FB Undervoltage Hysteresis			35		mV
PWGD Off Current	V_{PWGD} = 5 V			1	µA
PWGD Low Voltage	I_{PWGD} = 10 mA		150	500	mV

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC, $\overline{\text{SHDN}}$, SYNC, FREQ, COMP, SS, FB to GND, PVCC to PGND, BST to SW	−0.3 V to +6 V
BST to GND	−0.3 V to +30 V
CSL to GND	−1 V to +30 V
DH to GND	(V_{SW} − 0.3 V) to (V_{BST} + 0.3 V)
DL to PGND	−0.3 V to (V_{PVCC} + 0.3 V)
SW to GND	−2 V to +30 V
PGND to GND	±2 V
θ_{JA}, 2-Layer (SEMI Standard Board)	150°C/W
θ_{JA}, 4-Layer (JEDEC Standard Board)	105°C/W
Operating Ambient Temperature Range	−40°C to +85°C
Operating Junction Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Soldering Lead Temperature	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to GND.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

SIMPLIFIED BLOCK DIAGRAM

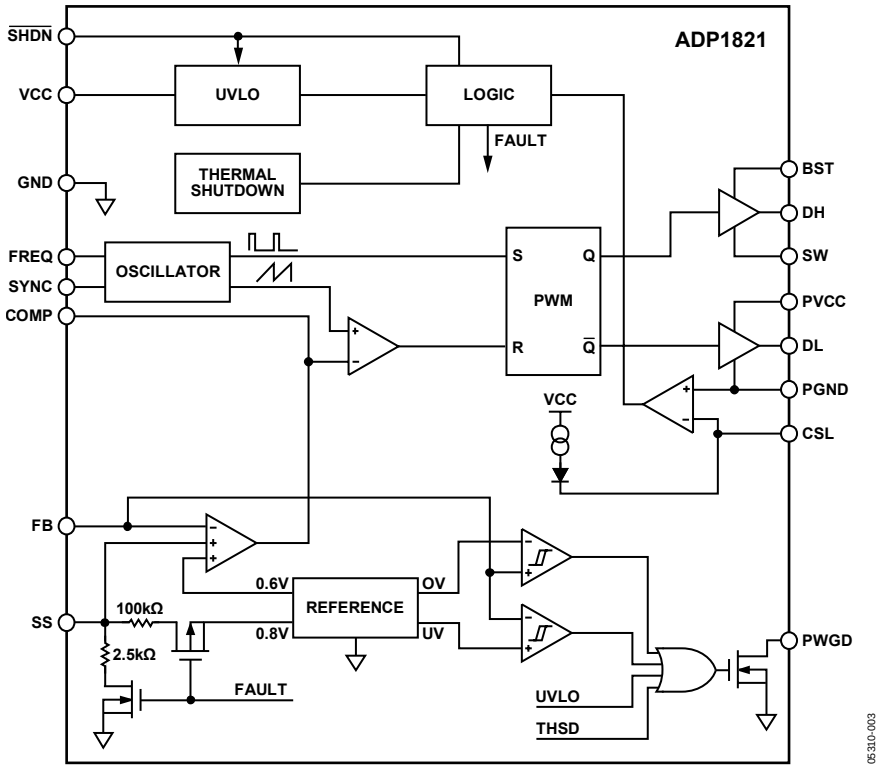

Figure 3. Simplified Block Diagram

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

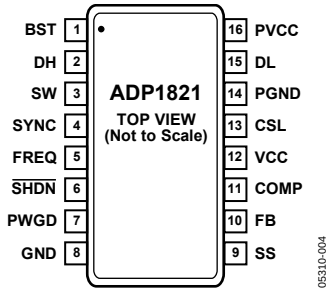

Figure 4. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	BST	High-Side Gate Driver Boost Capacitor Input. A capacitor between SW and BST powers the high-side gate driver, DH. The capacitor is charged through a diode from PVCC when the low-side MOSFET is on. Connect a 0.1 µF or greater ceramic capacitor from BST to SW and a Schottky diode from PVCC to BST to power the high-side gate driver.
2	DH	High-Side Gate Driver Output. Connect DH to the gate of the external high-side, N-channel MOSFET switch. DH is powered from the capacitor between SW and BST, and its voltage swings between V_{SW} and V_{BST}.
3	SW	Power Switch Node. Connect the source of the high-side, N-channel MOSFET switch and the drain of the low-side, N-channel MOSFET synchronous rectifier to SW. SW powers the output through the output LC filter.
4	SYNC	Frequency Synchronization Input. Drive SYNC with an external 300 kHz to 1.2 MHz signal to synchronize the converter switching frequency to the applied signal. The maximum SYNC frequency is limited to 2 times the nominal internal frequency selected by FREQ. Do not leave SYNC unconnected; when not used, connect SYNC to GND.
5	FREQ	Frequency Select Input. FREQ selects the converter switching frequency. Drive FREQ low to select 300 kHz, or high to select 600 kHz. Do not leave FREQ unconnected.
6	$\overline{\text{SHDN}}$	Active Low, DC-to-DC Shutdown Input. Drive $\overline{\text{SHDN}}$ high to turn on the converter and low to turn it off. Connect $\overline{\text{SHDN}}$ to VCC for automatic startup.
7	PWGD	Open-Drain, Power-Good Output. PWGD sinks current to GND when the output voltage is above or below the regulation voltage. Connect a pull-up resistor from PWGD to VDD for a logical power-good indicator.
8	GND	Analog Ground. Connect GND to PGND at a single point as close as possible to the internal circuitry (IC).
9	SS	Soft Start Control Input. A capacitor from SS to GND controls the soft start period. When the output is overloaded, SS is discharged to prevent excessive input current while the output recovers. Connect a 1 nF capacitor to a 1 µF capacitor from SS to GND to set the soft start period. See the Soft Start section.
10	FB	Voltage Feedback Input. Connect to a resistive voltage divider from the output to FB to set the output voltage. See the Setting the Output Voltage section.
11	COMP	Compensation Node. Connect a resistor-capacitor network from COMP to FB to compensate the regulation control system. See the Compensation section.
12	VCC	Internal Power Supply Input. VCC powers the internal circuitry. Bypass VCC to GND with a 0.1 µF or greater capacitor connected as close as possible to the IC.
13	CSL	Low-Side Current Sense Input. Connect CSL to SW through a resistor to set the current limit. See the Setting the Current Limit section.
14	PGND	Power Ground. Connect GND to PGND at a single point as close as possible to the IC.
15	DL	Low-Side Gate Driver Output. Connect DL to the gate of the low-side, N-channel MOSFET synchronous rectifier. The DL voltage swings between PGND and PVCC.
16	PVCC	Internal Gate Driver Power Supply Input. PVCC powers the low-side gate driver, DL. Bypass PVCC to PGND with a 1 µF or greater capacitor connected as close as possible to the IC.

TYPICAL PERFORMANCE CHARACTERISTICS

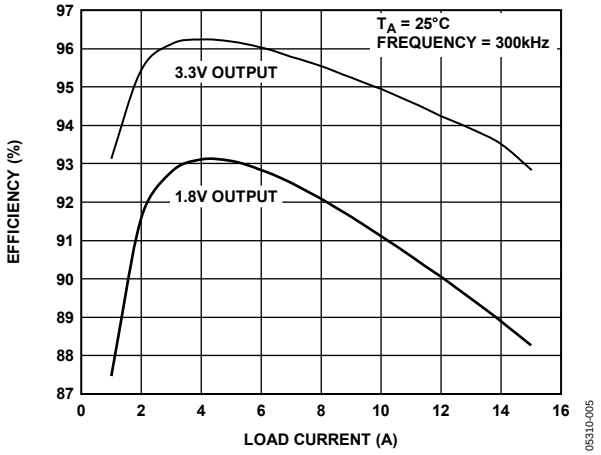

Figure 5. Efficiency vs. Load Current, V_{IN} = 5 V, V_{OUT} = 3.3 V, 1.8 V

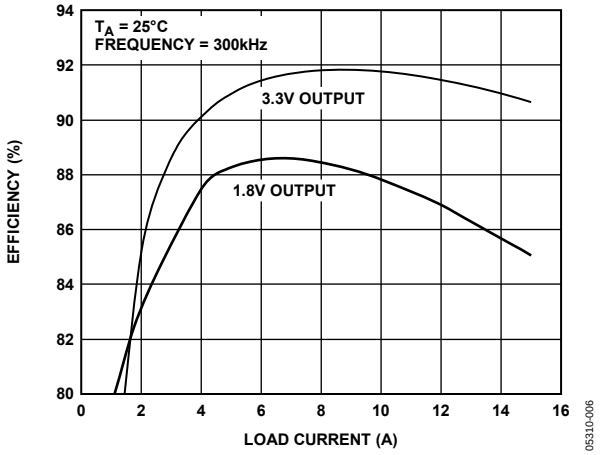

Figure 6. Efficiency vs. Load Current, V_{IN} = 12 V, V_{OUT} = 3.3 V, 1.8 V

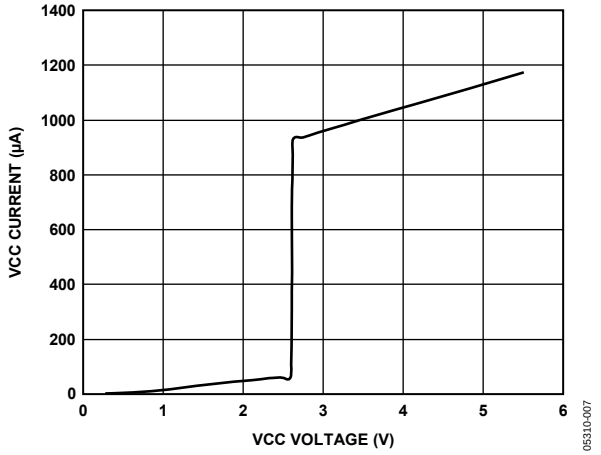

Figure 7. VCC Supply Current vs. VCC Voltage

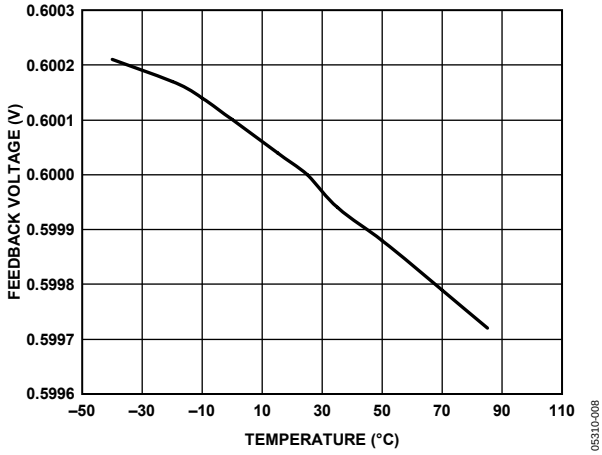

Figure 8. FB Regulation Voltage vs. Temperature

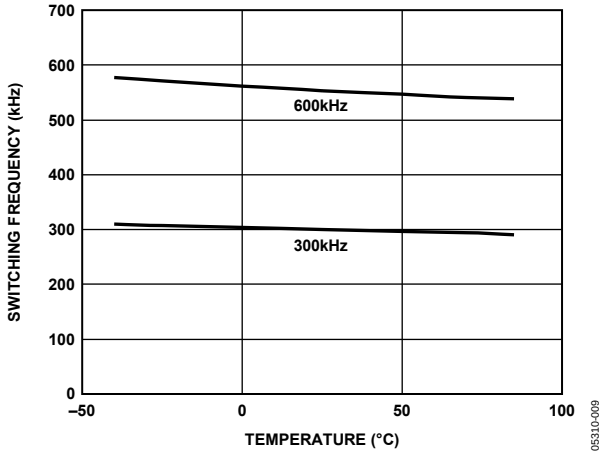

Figure 9. Switching Frequency vs. Temperature

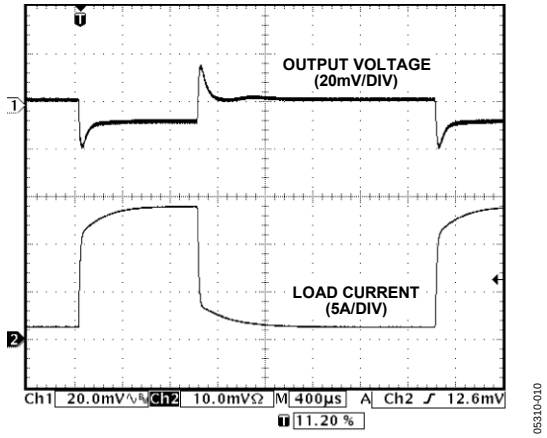

Figure 10. Load Transient Response, 1.5 A to 15 A

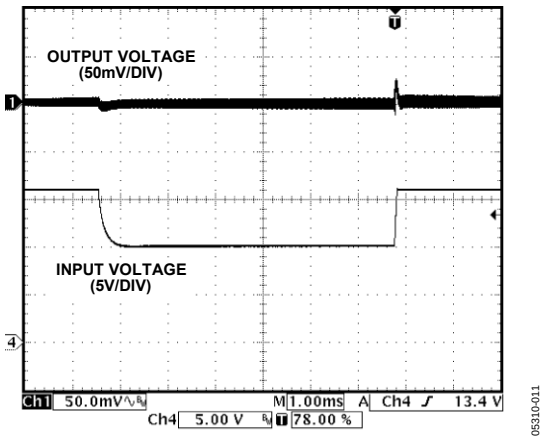

Figure 11. Line Transient Response, 10 V to 16 V

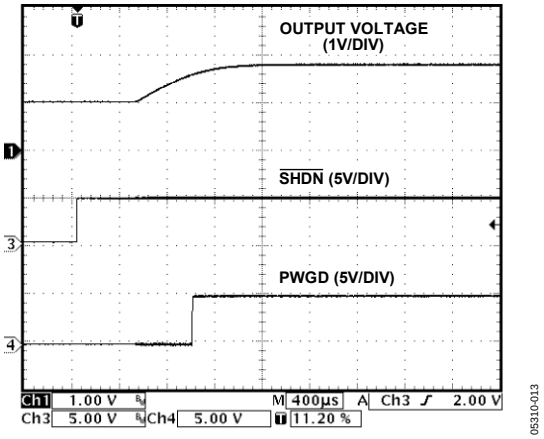

Figure 13. Power-On Response, Prebiased Output

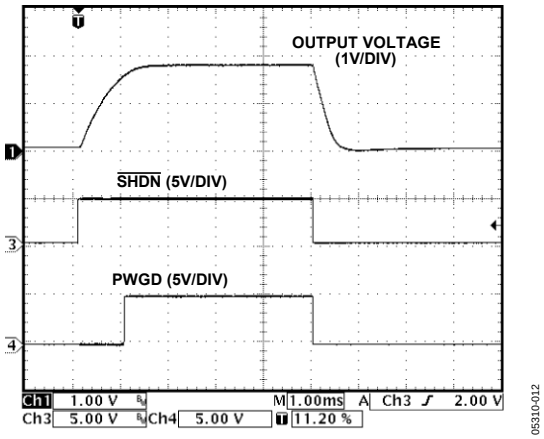

Figure 12. Power-On Response

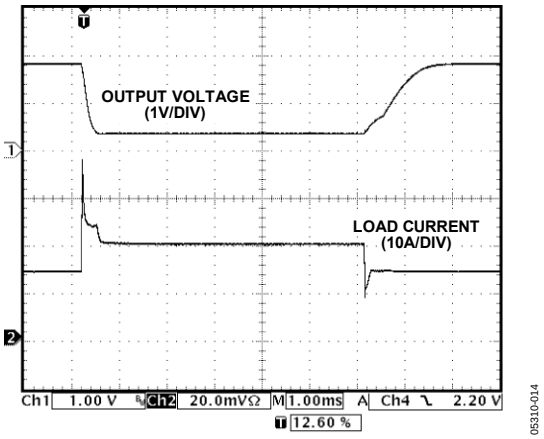

Figure 14. Output Short-Circuit Response and Recovery

THEORY OF OPERATION

The ADP1821 is a versatile, economical, synchronous-rectified, fixed-frequency, PWM, voltage mode step-down controller capable of generating an output voltage as low as 0.6 V. It is ideal for a wide range of high power applications, such as DSP power and processor core power in telecommunications, medical imaging, and industrial applications. The ADP1821 controller operates from a 3.7 V to 5.5 V supply with a power input voltage ranging from 1.0 V to 24 V.

The ADP1821 operates at a fixed, internally set 300 kHz or 600 kHz switching frequency that is controlled by the state of the FREQ input. The high frequency reduces external component size and cost while maintaining high efficiency. For noise sensitive applications where the switching frequency needs to be more tightly controlled, synchronize the ADP1821 to an external signal whose frequency is between 300 kHz and 1.2 MHz.

The ADP1821 includes adjustable soft start with output reverse-current protection, and a unique adjustable, lossless current limit. It operates over the −40°C to +125°C temperature range and is available in a space-saving, 16-lead QSOP.

SOFT START

When powering up or resuming operation after shutdown, overload, or short-circuit conditions, the ADP1821 employs an adjustable soft start feature that reduces input current transients and prevents output voltage overshoot at start-up and overload conditions. The soft start period is set by the value of the soft start capacitor, C_{SS}, between SS and GND.

When starting the ADP1821, C_{SS} is initially discharged. It is enabled when $\overline{SHDN}$ is high and VCC is above the undervoltage lockout threshold. C_{SS} begins charging to 0.8 V through an internal 100 kΩ resistor. As C_{SS} charges, the regulation voltage at FB is limited to the lesser of either the voltage at SS or the internal 0.6 V reference voltage. As the voltage at SS rises, the output voltage rises proportionally until the voltage at SS exceeds 0.6 V. At this time, the output voltage is regulated to the desired voltage.

If the output voltage is precharged prior to turn-on, the ADP1821 limits reverse inductor current, which would discharge the output voltage. Once the voltage at SS exceeds the 0.6 V regulation voltage, the reverse current is re-enabled to allow the output voltage regulation to be independent of load current.

ERROR AMPLIFIER

The ADP1821 error amplifier is an operational amplifier. The ADP1821 senses the output voltages through an external resistor divider at the FB pin. The FB pin is the inverting input to the error amplifier. The error amplifier compares this feedback voltage to the internal 0.6 V reference, and the output of the error amplifier appears at the COMP pin. The COMP pin voltage then directly controls the duty cycle of the switching converter.

A series/parallel RC network is tied between the FB pin and the COMP pin to provide the compensation for the buck converter control loop. A detailed design procedure for compensating the system is provided in the Compensating the Voltage Mode Buck Regulator section.

The error amplifier output is clamped between a lower limit of about 0.7 V and a higher limit of about 2.4 V. When the COMP pin is low, the switching duty cycle goes to 0%, and when the COMP pin is high, the switching duty cycle goes to the maximum.

The SS pin is an auxiliary positive input to the error amplifier. Whichever voltage is lowest, SS or the internal 0.6 V reference, controls the FB pin voltage and thus the output. As a consequence, if two of these inputs are close to each other, a small offset is imposed on the error amplifier.

CURRENT-LIMIT SCHEME

The ADP1821 employs a unique, programmable, cycle-by-cycle, lossless current-limit circuit that uses an ordinary, inexpensive resistor to set the threshold. Every switching cycle, the synchronous rectifier turns on for a minimum time and the voltage drop across the MOSFET R_{DSON} is measured to determine if the current is too high.

This measurement is done by an internal current limit comparator and an external current-limit set resistor. The resistor is connected between the switch node (that is the drain of the rectifier MOSFET) and the CSL pin. The CSL pin, which is the inverting input of the comparator, forces 50 μA through the resistor to create an offset voltage drop across it.

When the inductor current is flowing in the MOSFET rectifier, its drain is forced below PGND by the voltage drop across its R_{DSON}. If the R_{DSON} voltage drop exceeds the preset drop on the current-limit set resistor, the inverting comparator input is similarly forced below PGND and an overcurrent fault is flagged.

The normal transient ringing on the switch node is ignored for 100 ns after the synchronous rectifier turns on, therefore, the over current condition must also persist for 100 ns for a fault to be flagged.

When the ADP1821 senses an overcurrent condition, the next switching cycle is suppressed, the soft start capacitor is discharged through an internal 2.5 kΩ resistor, and the error amplifier output voltage is pulled down. The output behaves like a constant current source around the preset current limit when the overcurrent condition exists. The ADP1821 remains in this mode for as long as the overcurrent condition persists. In the event of a short circuit, the short-circuit output current is the current limit set by the R_{CL} resistor and is monitored cycle by cycle. When the overcurrent condition is removed, operation resumes in soft start mode.

The ADP1821 also offers a technique for implementing a current-limit foldback in the event of a short circuit with the use of an additional resistor. See the Setting the Current Limit section for more information.

MOSFET DRIVERS

The DH pin drives the high-side switch MOSFET. This is a boosted 5 V gate driver that is powered by a bootstrap capacitor circuit. This configuration allows the high-side, N-channel MOSFET gate to be driven above the input voltage, allowing full enhancement and a low voltage drop across the MOSFET. The bootstrap capacitor is connected from the SW pin to the BST pin. A bootstrap Schottky diode connected from the PVCC pin to the BST pin recharges the bootstrap capacitor every time the SW node goes low. Use a bootstrap capacitor value greater than 100× the high-side MOSFET input capacitance.

In practice, the switch node can run up to 24 V of input voltage, and the boost nodes can operate more than 5 V above this to allow full gate drive. The power input voltage can be run from 1 V to 24 V.

The switching cycle is initiated by the internal clock signal. The high-side MOSFET is turned on by the DH driver, and the SW node goes high, pulling up on the inductor. When the internally generated ramp signal crosses the COMP pin voltage, the switch MOSFET is turned off and the low-side synchronous rectifier MOSFET is turned on by the DL driver. Active break-before-make circuitry as well as a supplemental fixed dead time are used to prevent cross-conduction in the switches.

The DL pin provides the gate drive for the low-side MOSFET synchronous rectifier. Internal circuitry monitors the external MOSFETs to ensure break-before-make switching to prevent cross-conduction. An active dead-time reduction circuit reduces the break-before-make time of the switching to limit the losses due to current flowing through the synchronous rectifier body diode.

The PVCC pin provides power to the low-side drivers. It is limited to 5.5 V maximum input and should have a local decoupling capacitor to PGND.

The synchronous rectifier is turned on for a minimum time of about 200 ns on every switching cycle in order to sense the current. This and the nonoverlap dead time put a limit on the maximum high-side switch duty cycle based on the selected switching frequency. Typically, this is about 90% at 300 kHz switching, and at 1 MHz switching, it reduces to about 70% maximum duty cycle.

INPUT VOLTAGE RANGE

The ADP1821 takes its internal power from the VCC and PVCC inputs. PVCC powers the low-side MOSFET gate drive (DL), and VCC powers the internal control circuitry. Both of these inputs are limited to between 3.7 V and 5.5 V. Bypass PVCC to PGND with a 1 µF or greater capacitor. Bypass VCC to GND with a 0.1 µF or greater capacitor.

The power input to the dc-to-dc converter can range between 1.2× the output voltage and 24 V. Bypass the power input to PGND with a suitably large capacitor. See the Selecting the Input Capacitor section.

SETTING THE OUTPUT VOLTAGE

The output voltage is set using a resistive voltage divider from the output to FB. The voltage divider drops the output voltage to the 0.6 V FB regulation voltage to set the regulation output voltage. The output voltage is set to voltages as low as 0.6 V and as high as 85% of the minimum power input voltage (see the Feedback Voltage Divider section).

SWITCHING FREQUENCY CONTROL AND SYNCHRONIZATION

The ADP1821 has a logic-controlled frequency select input (FREQ) which sets the switching frequency to 300 kHz or 600 kHz. Drive FREQ low for 300 kHz and high for 600 kHz.

The SYNC input is used to synchronize the converter switching frequency to an external signal. The converter switching can be synchronized to an external signal. This allows multiple ADP1821 converters to be operated at the same frequency to prevent frequency beating or other interactions.

To synchronize the ADP1821 switching to an external signal, drive the SYNC input with a synchronizing signal. The ADP1821 can only synchronize up to 2× the nominal oscillator frequency. If the frequency is set to 300 kHz (FREQ connected to GND), then the synchronization frequency needs to be in between 300 kHz and 600 kHz. Since the 300 kHz setting has a minimum specification (see Table 1) of 250 kHz and a maximum of 375 kHz over the specified temperature range, the recommended synchronization frequency range is between 375 kHz and 500 kHz to cover the whole range of part-to-part variation and over the operating temperature range. If the frequency is set to 600 kHz (FREQ connected to VCC), then the synchronization frequency needs to be in between 600 kHz and 1.2 MHz. Since the 600 kHz setting has a minimum specification (see Table 1) of 470 kHz and a maximum of 720 kHz over the specified temperature range, the recommended synchronization frequency range is between 720 kHz and 940 kHz to cover the whole range of part-to-part variation and over the operating temperature range. Driving SYNC faster than recommended for the FREQ setting results in a small ramp signal, which could affect the signal-to-noise ratio and the modulator gain and stability.

When an external clock is detected at the first SYNC edge, the internal oscillator is reset and clock control shifts to SYNC. The SYNC edges then trigger subsequent clocking of the PWM outputs. The DH rising edges appear about 320 ns after the corresponding SYNC edge, and the frequency is locked to the external signal. If the external SYNC signal disappears during operation, the ADP1821 reverts to its internal oscillator and experiences a delay of no more than a single cycle of the internal oscillator.

COMPENSATION

The control loop is compensated by an external series RC network from COMP to FB and sometimes requires a series RC in parallel with the top voltage divider resistor. COMP is the output of the internal error amplifier.

The internal error amplifier compares the voltage at FB to the internal 0.6 V reference voltage. The difference between the two (the feedback voltage error) is amplified by the error amplifier. To optimize the ADP1821 for stability and transient response for a given set of external components and input/output voltage conditions, choose the compensation components carefully. For more information on choosing the compensation components, see the Compensating the Voltage Mode Buck Regulator section.

POWER-GOOD INDICATOR

The ADP1821 features an open-drain, power-good output (PWGD) that sinks current when the output voltage drops 8.3% below or 25% above the nominal regulation voltage. Two comparators measure the voltage at FB to set these thresholds. The PWGD comparator directly monitors FB, and the threshold is fixed at 0.55 V for undervoltage and 0.75 V for overvoltage. The PWGD output also sinks current if an overtemperature or input undervoltage condition is detected and is operational with VCC voltage as low as 1 V.

Use this output as a logical power-good signal by connecting a pull-up resistor from PWGD to an appropriate supply voltage.

THERMAL SHUTDOWN

The ADP1821 controller does not generate much heat under normal conditions, even when driving a relatively large MOSFET. However, the surrounding power components or other circuits on the same PCB could heat up the PCB to an unsafe operating temperature. The ADP1821 controller goes into shutdown and shuts off the gate drivers when its junction temperature reaches about 145°C. When the junction temperature drops below about 135°C, the ADP1821 resumes normal operation in a soft start mode.

SHUTDOWN CONTROL

The ADP1821 dc-to-dc converter features a low power shutdown mode that reduces quiescent supply current to 1 µA. To shut down the ADP1821, drive $\overline{\text{SHDN}}$ low. To turn it on, drive $\overline{\text{SHDN}}$ high. For automatic startup, connect $\overline{\text{SHDN}}$ to VCC.

APPLICATION INFORMATION

SELECTING THE INPUT CAPACITOR

The input current to a buck converter is a pulsed waveform. It is zero when the high-side switch is off and approximately equal to the load current when it is on. The input capacitor carries the input ripple current, allowing the input power source to supply only the dc current. The input capacitor needs sufficient ripple current rating to handle the input ripple and the equivalent series resistance (ESR) that is low enough to mitigate input voltage ripple. For the usual current ranges for these converters, good practice is to use two parallel capacitors placed close to the drains of the high-side switch MOSFETs, one bulk capacitor of sufficiently high current rating as calculated in Equation 1, along with 10 µF of ceramic capacitor.

Select an input bulk capacitor based on its ripple current rating. First, determine the duty cycle of the output with the larger load current by

$$D = \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Second, determine the input capacitor ripple current, which is approximately

$$I_{RIPPLE} \approx I_L \sqrt{D(1-D)} \quad (2)$$

where:
I_L is the maximum inductor or load current for the channel.
D is the duty cycle.

Use this method to determine the input capacitor ripple current rating for duty cycles between 20% and 80%.

For duty cycles less than 20% or greater than 80%, use an input capacitor with a ripple current rating of

$$I_{RIPPLE} > 0.4\ I_L \quad (3)$$

OUTPUT LC FILTER

The output LC filter smoothes the switched voltage at SW, making the output voltage an almost dc voltage. Choose the output LC filter to achieve the desired output ripple voltage. Because the output LC filter is part of the regulator negative-feedback control loop, the choice of the output LC filter components affects the regulation control loop stability.

Choose an inductor value such that the inductor ripple current is approximately 1/3 of the maximum dc output load current. Using a larger value inductor results in a physical size larger than required and using a smaller value results in increased losses in the inductor and/or MOSFET switches.

Use the following equation to choose the inductor value:

$$L = \frac{1}{f_{SW} \times \Delta I_L} V_{OUT}\left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (4)$$

where:
L is the inductor value.
f_{SW} is the switching frequency.
V_{OUT} is the output voltage.
V_{IN} is the input voltage.
ΔI_L is the inductor ripple current, typically 1/3 of the maximum dc load current.

Choose the output bulk capacitor to set the desired output voltage ripple. The impedance of the output capacitor at the switching frequency multiplied by the ripple current gives the output voltage ripple. The impedance is made up of the capacitive impedance plus the nonideal parasitic characteristics, the ESR and the equivalent series inductance (ESL). The output voltage ripple can be approximated with

$$\Delta V_{OUT} = \Delta I_L \sqrt{ESR^2 + \left(\frac{1}{8 f_{SW} C_{OUT}}\right)^2 + (4 f_{SW} ESL)^2} \quad (5)$$

where:
ΔV_{OUT} is the output ripple voltage.
ΔI_L is the inductor ripple current.
ESR is the equivalent series resistance of the output capacitor (or the parallel combination of ESR of all output capacitors).
ESL is the equivalent series inductance of the output capacitor (or the parallel combination of ESL of all capacitors).

Note that the factors of 8 and 4 in Equation 5 would normally be 2π for sinusoidal waveforms, but the ripple current waveform in this application is triangular. Parallel combinations of different types of capacitors, for example, a large aluminum electrolytic in parallel with MLCCs, may give different results.

Usually the impedance is dominated by ESR at the switching frequency so this equation reduces to

$$\Delta V_{OUT} \cong \Delta I_L ESR \quad (6)$$

Electrolytic capacitors have significant ESL also, on the order of 5 nH to 20 nH, depending on type, size, and geometry; and PCB traces contribute some ESR and ESL as well. However, using the maximum ESR rating from a capacitor data sheet usually provides some margin such that measuring the ESL is not usually required.

In the case of output capacitors where the impedance of the ESR and ESL are small at the switching frequency, for instance, where the output capacitor is a bank of parallel MLCC capacitors, the capacitive impedance dominates and the ripple equation reduces to

$$\Delta V_{OUT} \cong \frac{\Delta I_L}{8\, C_{OUT} f_{SW}} \quad (7)$$

Make sure that the ripple current rating of the output capacitors is greater than the maximum inductor ripple current.

During a load step transient on the output, the output capacitor supplies the load until the control loop has a chance to ramp the inductor current. This initial output voltage deviation due to a change in load is dependent on the output capacitor characteristics. Again, usually the capacitor ESR dominates this response, and the ΔV_{OUT} in Equation 6 can be used with the load step current value for ΔI_L.

SELECTING THE MOSFETS

The choice of MOSFET directly affects the dc-to-dc converter performance. The MOSFET must have low on resistance to reduce I^2R losses and low gate charge to reduce transition losses. In addition, the MOSFET must have low thermal resistance to ensure that the power dissipated in the MOSFET does not result in excessive MOSFET die temperature.

The high-side MOSFET carries the load current during on time and carries all the transition losses of the converter. Typically, the lower the MOSFET on resistance, the higher the gate charge and vice versa. Therefore, it is important to choose a high-side MOSFET that balances the two losses. The conduction loss of the high-side MOSFET is determined by the equation

$$P_C \cong \left(I_{LOAD}\right)^2 R_{DSON} \left(\frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

where:
P_C is the conduction power loss.
R_{DSON} is the MOSFET on resistance.

The gate charging loss is approximated by the equation

$$P_G \cong V_{PVCC} Q_G f_{SW} \quad (9)$$

where:
P_G is the gate charging loss power.
V_{PVCC} is the gate driver supply voltage.
Q_G is the MOSFET total gate charge.
f_{SW} is the converter switching frequency.

The high-side MOSFET transition loss is approximated by the equation

$$P_T = \frac{V_{IN} I_{LOAD} \left(t_R + t_F\right) f_{SW}}{2} \quad (10)$$

where:
P_T is the high-side MOSFET switching loss power.
t_R is the MOSFET rise time.
t_F is the MOSFET fall time.

The total power dissipation of the high-side MOSFET is the sum of all the previous losses, or

$$P_D \cong P_C + P_G + P_T \quad (11)$$

where P_D is the total high-side MOSFET power loss.

The conduction losses may need an adjustment to account for the MOSFET R_{DSON} variation with temperature. Note that MOSFET R_{DSON} increases with increasing temperature. A MOSFET data sheet should list the thermal resistance of the package, θ_{JA}, along with a normalized curve of the temperature coefficient of the R_{DSON}. For the power dissipation estimated above, calculate the MOSFET junction temperature rise over the ambient temperature of interest.

$$T_J = T_A + \theta_{JA} P_D \quad (12)$$

Then calculate the new R_{DSON} from the temperature coefficient curve and the R_{DSON} spec at 25°C. A typical value of the temperature coefficient (TC) of the R_{DSON} is 0.004/°C, thus, an alternate method to calculate the MOSFET R_{DSON} at a second temperature, T_J, is

$$R_{DSON} @ T_J = R_{DSON} @ 25°C(1 + TC(T_J - 25°C)) \quad (13)$$

Next, the conduction losses can be recalculated and the procedure iterated once or twice until the junction temperature calculations are relatively consistent.

The synchronous rectifier, or low-side MOSFET, carries the inductor current when the high-side MOSFET is off. The low-side MOSFET transition loss is small and can be neglected in the calculation. For high input voltage and low output voltage, the low-side MOSFET carries the current most of the time. Therefore, to achieve high efficiency, it is critical to optimize the low-side MOSFET for low on resistance. In cases where the power loss exceeds the MOSFET rating or lower resistance is required than is available in a single MOSFET, connect multiple low-side MOSFETs in parallel. The equation for low-side MOSFET power loss is

$$P_{LS} \cong \left(I_{LOAD}\right)^2 R_{DSON} \left[1 - \frac{V_{OUT}}{V_{IN}}\right] \quad (14)$$

where:
P_{LS} is the low-side MOSFET on resistance.
R_{DSON} is the total on resistance of the low-side MOSFET(s).

Check the gate charge losses of the synchronous rectifier using the P_G equation (Equation 9) to be sure it is reasonable. If multiple low-side MOSFETs are used in parallel, then use the parallel combination of the on resistances for determining R_{DSON} to solve this equation.

SETTING THE CURRENT LIMIT

The current-limit comparator measures the voltage across the low-side MOSFET to determine the load current.

The current limit is set through the current-limit resistor, R_{CL}. CSL, the current sense pin, sources 50 µA through R_{CL}. This creates an offset voltage of R_{CL} multiplied by the 50 µA CSL current. When the drop across the low-side MOSFET R_{DSON} is equal to or greater than this offset voltage, the ADP1821 flags a current-limit event.

Because the CSL current and the MOSFET R_{DSON} vary over process and temperature, the minimum current limit should be set to ensure that the system can handle the maximum desired load current. To do this, use the peak current in the inductor, which is the desired current-limit level plus the ripple current, the maximum R_{DSON} of the MOSFET at its highest expected temperature, and the minimum CSL current.

$$R_{CL} = \frac{I_{LPK}\ R_{DSON(MAX)}}{42\,\mu A} \quad (15)$$

where I_{LPK} is the peak inductor current.

When an overcurrent event occurs, the overcurrent comparator prevents switching cycles until the rectifier current has decayed below the threshold. The overcurrent comparator is blanked for the first 100 ns of the synchronous rectifier cycle to prevent switch node ringing from falsely tripping the current limit. The ADP1821 senses the current limit during the off cycle. When the current-limit condition occurs, the output behaves like a constant current source around the preset current limit. When the overload condition is removed, the output recovers with the normal soft start slope and does not overshoot.

In the event of a short circuit, the ADP1821 offers a technique for implementing a current-limit foldback with the use of an additional resistor, as shown in Figure 15. Resistor R_{LO} is largely responsible for setting the foldback current limit during a short circuit, and Resistor R_{HI} is mainly responsible for setting up the normal current limit. R_{LO} is lower than R_{HI}. These current-limit sense resistors can be calculated as

$$R_{LO} = \frac{I_{PKFOLDBACK} R_{DSON(MAX)}}{42\mu A} \quad (16)$$

$$R_{HI} = \frac{V_{OUT}}{I_{LPK}\frac{R_{DSON(MAX)}}{R_{LO}} - 42\mu A} \quad (17)$$

where:

$I_{PKFOLDBACK}$ is the desired short circuit peak inductor current limit.
I_{LPK} is the peak inductor current limit during normal operation and is also used in Equation 15.

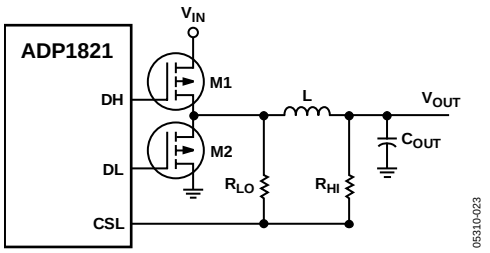

Figure 15. Short-Circuit Current Foldback Scheme

Because the buck converter is usually running at a fairly high current, PCB layout and component placement may affect the current-limit setting. An iteration of the R_{CL} or R_{LO} and R_{HI} values may be required for a particular board layout and MOSFET selection. If alternate MOSFETs are substituted at some point in production, these resistor values may also need an iteration.

FEEDBACK VOLTAGE DIVIDER

The output regulation voltage is set through the feedback voltage divider. The output voltage is reduced through the voltage divider and drives the FB feedback input. The regulation threshold at FB is 0.6 V. The maximum input bias current into FB is 100 nA. For a 0.15% degradation in regulation voltage and with 100 nA bias current, the low-side resistor, R_{BOT}, needs to be less than 9 kΩ, which results in 67 µA of divider current. For R_{BOT}, use 1 kΩ to 10 kΩ. A larger value resistor can be used, but results in a reduction in output voltage accuracy due to the input bias current at the FB pin, whereas lower values cause increased quiescent current consumption. Choose R_{TOP} to set the output voltage by using the following equation:

$$R_{TOP} = R_{BOT}\left(\frac{V_{OUT} - V_{FB}}{V_{FB}}\right) \quad (18)$$

where:

R_{TOP} is the high-side voltage divider resistance.
R_{BOT} is the low-side voltage divider resistance.
V_{OUT} is the regulated output voltage.
V_{FB} is the feedback regulation threshold, 0.6 V.

COMPENSATING THE VOLTAGE MODE BUCK REGULATOR

Assuming the LC filter design is complete, the feedback control system can be compensated. Good compensation is critical to proper operation of the regulator. Calculate the quantities in Equation 19 through Equation 47 to derive the compensation values.

The goal is to guarantee that the voltage gain of the buck converter crosses unity at a slope that provides adequate phase margin for stable operation. Additionally, at frequencies above the crossover frequency, f_{CO}, guaranteeing sufficient gain margin and attenuation of switching noise are important secondary goals.

For initial practical designs, a good choice for the crossover frequency is 1/10 of the switching frequency; first calculate

$$f_{CO} = \frac{f_{SW}}{10} \quad (19)$$

This gives sufficient frequency range to design a compensation that attenuates switching artifacts, yet also gives sufficient control loop bandwidth to provide good transient response.

The output LC filter is a resonant network that inflicts two poles upon the response at a Frequency f_{LC}, so next calculate

$$f_{LC} = \frac{1}{2\pi\sqrt{LC}} \quad (20)$$

The LC corner frequency is about two orders of magnitude below the switching frequency, and therefore about one order of magnitude below crossover. To achieve sufficient phase margin at crossover to guarantee stability, the design must compensate for the two poles at the LC corner frequency with two zeros to boost the system phase prior to crossover. The two zeros require an additional pole or two above the crossover frequency to guarantee adequate gain margin and attenuation of switching noise at high frequencies.

Depending on component selection, one zero might already be generated by the ESR of the output capacitor. Calculate this zero corner frequency, f_{ESR}, as

$$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}} \quad (21)$$

This zero is often near or below crossover and is useful in bringing back some of the phase lost at the LC corner.

Figure 16 shows a typical bode plot of the LC filter by itself.

The gain of the LC filter at crossover can be linearly approximated from Figure 16 as

$$A_{FILTER} = A_{LC} + A_{ESR}$$

$$A_{FILTER} = -40\ \text{dB} \times \log\left(\frac{f_{ESR}}{f_{LC}}\right) - 20\ \text{dB} \times \log\left(\frac{f_{CO}}{f_{ESR}}\right) \quad (22)$$

If $f_{ESR} \approx f_{CO}$, then add another 3 dB to account for the local difference between the exact solution and the preceding linear approximation.

To compensate the control loop, the gain of the system must be brought back up so that it is 0 dB at the desired crossover frequency. Some gain is provided by the PWM modulation itself, and it is given by

$$A_{MOD} = 20\log\left(\frac{V_{IN}}{V_{RAMP}}\right) \quad (23)$$

For systems using the internal oscillator, this becomes

$$A_{MOD} = 20\log\left(\frac{V_{IN}}{1.25\ \text{V}}\right) \quad (24)$$

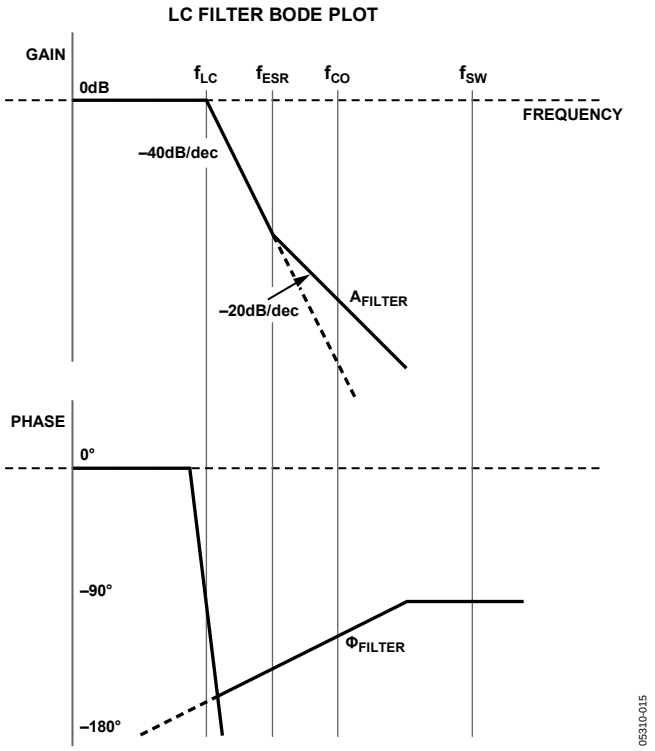

Figure 16. LC Filter Bode Plot

Note that if the converter is being synchronized, the ramp voltage, V_{RAMP}, is lower than 1.25 V by the percentage of frequency increase over the nominal setting of the FREQ pin

$$V_{RAMP} = 1.25\ \text{V}\left(\frac{f_{FREQ}}{f_{SYNC}}\right) \quad (25)$$

The rest of the system gain is needed to reach 0 dB at crossover. The total gain of the system therefore, is given by

$$A_T = A_{MOD} + A_{FILTER} + A_{COMP} \quad (26)$$

where:

A_{MOD} is the gain of the PWM modulator.

A_{FILTER} is the gain of the LC filter including the effects of the ESR zero.

A_{COMP} is the gain of the compensated error amplifier.

Additionally, the phase of the system must be brought back up to guarantee stability. Note from the bode plot of the filter that the LC contributes −180° of phase shift. Additionally, because the error amplifier is an integrator at low frequency, it contributes an initial −90°. Therefore, before adding compensation or accounting for the ESR zero, the system is already down −270°. To avoid loop inversion at crossover, or −180° phase shift, a good initial practical design is to require a phase margin of 60°, which gives an overall phase loss of −120° from the initial low frequency dc phase. The goal of the compensation is to boost the phase back up from −270° to −120° at crossover.

Two common compensation schemes are used, which are sometimes referred to as Type II or Type III compensation, depending on whether the compensation design includes two or three poles. (Dominant pole compensations, or single pole compensation, is referred to as Type I compensation, but it is not very useful for dealing successfully with switching regulators.)

If the zero produced by the ESR of the output capacitor provides sufficient phase boost at crossover, Type II compensation is adequate. If the phase boost produced by the ESR of the output capacitor is not sufficient, another zero is added to the compensation network, and thus Type III is used.

In Figure 17, the location of the ESR zero corner frequency gives significantly different net phase at the crossover frequency.

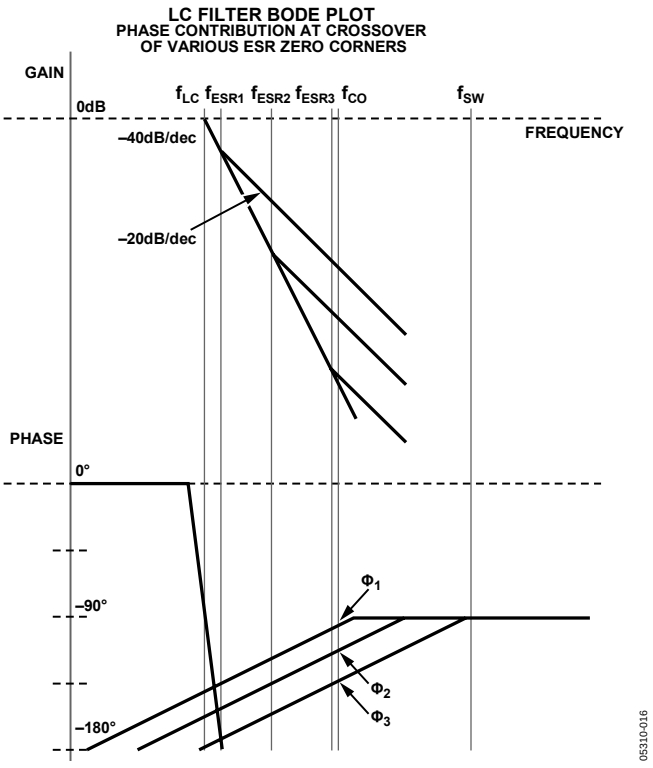

Figure 17. LC Filter Bode Plot

Use the following guidelines for selecting between Type II and Type III compensators.

If $f_{ESRZ} \le \frac{f_{CO}}{2}$, use Type II compensation.

If $f_{ESRZ} > \frac{f_{CO}}{2}$, use Type III compensation.

The following equations were used for the calculation of the compensation components as shown in Figure 18 and Figure 19:

$$f_{Z1} = \frac{1}{2\pi R_Z C_I} \quad (27)$$

$$f_{Z2} = \frac{1}{2\pi C_{FF}(R_{TOP} + R_{FF})} \quad (28)$$

$$f_{P1} = \frac{1}{2\pi R_Z \frac{C_I C_{HF}}{C_I + C_{HF}}} \quad (29)$$

$$f_{P2} = \frac{1}{2\pi R_{FF} C_{FF}} \quad (30)$$

where:

f_{Z1} is the zero produced in the Type II compensation.
f_{Z2} is the zero produced in the Type III compensation.
f_{P1} is the pole produced in the Type II compensation.
f_{P2} in the pole produced in the Type III compensation.

Type II Compensator

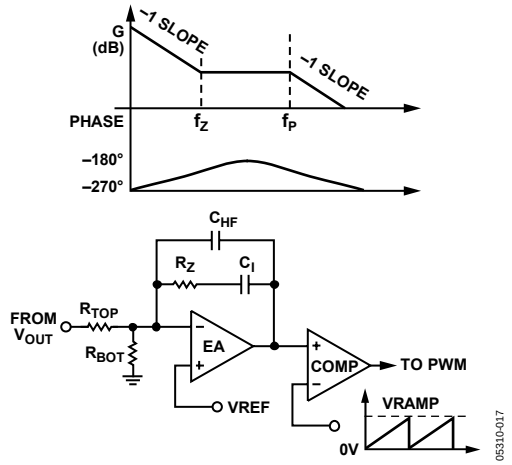

Figure 18. Type II Compensation

If the output capacitor ESR zero frequency is sufficiently low (≤ ½ of the crossover frequency), use the ESR to stabilize the regulator. In this case, use the circuit shown in Figure 18. Calculate the compensation resistor, Rz, with the following equation:

$$R_Z = \frac{R_{TOP} V_{RAMP} f_{ESR} f_{CO}}{V_{IN} f_{LC}^2} \quad (31)$$

where:

f_{CO} is chosen to be 1/10 of $f_{SW.}$
V_{RAMP} is 1.25 V.

Next, choose the compensation capacitor to set the compensation zero, f_{Z1}, to the lesser of ¼ of the crossover frequency or ½ of the LC resonant frequency

$$f_{Z1} = \frac{f_{CO}}{4} = \frac{f_{SW}}{40} = \frac{1}{2\pi R_Z C_I} \quad (32)$$

or

$$f_{Z1} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \quad (33)$$

Solving for C_I in Equation 32 yields

$$C_I = \frac{20}{\pi R_Z f_{SW}} \quad (34)$$

Solving for C_I in Equation 33 yields

$$C_I = \frac{1}{\pi R_Z f_{LC}} \quad (35)$$

Use the larger value of C_I from Equation 34 or Equation 35. Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Next, choose the high frequency pole f_{P1} to be ½ of f_{SW}.

$$f_{P1} = \frac{1}{2} f_{SW} \quad (36)$$

Since $C_{HF} << C_I$, Equation 29 is simplified to

$$f_{P1} = \frac{1}{2\pi R_Z C_{HF}} \quad (37)$$

Solving for C_{HF} in Equation 36 and Equation 37 yields

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \quad (38)$$

Type III Compensator

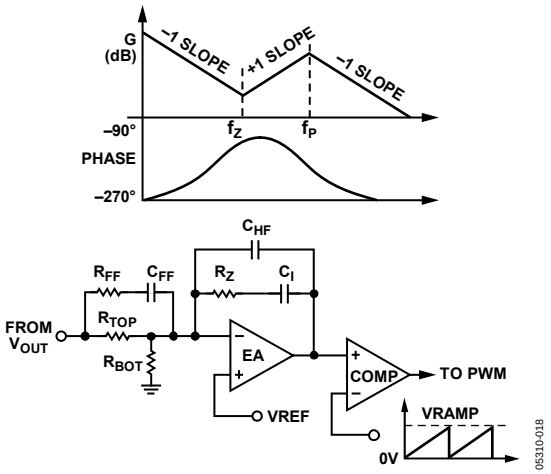

Figure 19. Type III Compensation

If the output capacitor ESR zero frequency is greater than ½ of the crossover frequency, use Type III compensator as shown in Figure 19. Set the poles and zeros as follows:

$$f_{P1} = f_{P2} = \frac{1}{2} f_{SW} \quad (39)$$

$$f_{Z1} = f_{Z2} = \frac{f_{CO}}{4} = \frac{f_{SW}}{40} = \frac{1}{2\pi R_Z C_I} \quad (40)$$

or

$$f_{Z1} = f_{Z2} = \frac{f_{LC}}{2} = \frac{1}{2\pi R_Z C_I} \quad (41)$$

Use the lower zero frequency from Equation 40 or Equation 41. Calculate the compensator resistor, R_Z, by

$$R_Z = \frac{R_{TOP} V_{RAMP} f_{Z1} f_{CO}}{V_{IN} f_{LC}^2} \quad (42)$$

Next calculate C_I

$$C_I = \frac{1}{2\pi R_Z f_{Z1}} \quad (43)$$

Because of the finite output current drive of the error amplifier, C_I needs to be less than 10 nF. If it is larger than 10 nF, choose a larger R_{TOP} and recalculate R_Z and C_I until C_I is less than 10 nF.

Since $C_{HF} << C_I$, combining Equation 29 and Equation 39 yields

$$C_{HF} = \frac{1}{\pi f_{SW} R_Z} \quad (44)$$

Next calculate the feedforward capacitor C_{FF}. Assume $R_{FF} << R_{TOP}$, then Equation 28 is simplified to

$$f_{Z2} = \frac{1}{2\pi C_{FF} R_{TOP}} \quad (45)$$

Solving C_{FF} in Equation 45 yields

$$C_{FF} = \frac{1}{2\pi R_{TOP} f_{Z2}} \quad (46)$$

where f_{Z2} is obtained from Equation 40 or Equation 41.

The feedforward resistor, R_{FF}, can be calculated by combining Equation 30 and Equation 39

$$R_{FF} = \frac{1}{\pi C_{FF} f_{SW}} \quad (47)$$

Check that the calculated component values are reasonable. For instance, capacitors smaller than about 10 pF should be avoided. In addition, the ADP1821 error amplifier has finite output current drive, so R_Z values less than 3 kΩ and C_I values greater than 10 nF should be avoided. If necessary, recalculate the compensation network with a different starting value of R_{TOP}. If C_{HF} is too small, start with a smaller value of R_{TOP}. If R_Z is too small and C_I is too big, start with a larger value of R_{TOP}.

In general, aluminum electrolytic capacitors have high ESR, therefore, a Type II compensation is adequate. However, if several aluminum electrolytic capacitors are connected in parallel, producing a low effective ESR, then Type III compensation is needed. In addition, ceramic capacitors have very low ESR, on the order of a few milliohms, requiring Type III compensation for ceramic output capacitors. Type III compensation offers better performance than Type II in terms of more low frequency gain, more phase margin, and less high frequency gain at the crossover frequency.

SETTING THE SOFT START PERIOD

The ADP1821 uses an adjustable soft start to limit the output voltage ramp-up period, limiting the input inrush current. The soft start is set by selecting the capacitor, C_{SS}, from SS to GND. The ADP1821 charges C_{SS} to 0.8 V through an internal 100 kΩ resistor. The voltage on C_{SS} while it is charging is

$$V_{CSS} = 0.8\ \text{V}\left(1 - e^{\frac{t}{RC_{SS}}}\right) \quad (48)$$

where R is the internal 100 kΩ resistor.

The soft start period, t_{SS}, is achieved when V_{CSS} = 0.6 V or

$$0.6\ \text{V} = 0.8\ \text{V}\left(1 - e^{\frac{t_{SS}}{100\ \text{k}\Omega(C_{SS})}}\right) \quad (49)$$

or

$$\frac{t_{SS}}{100\ \text{k}\Omega(C_{SS})} = -1\text{n}\left(1 - \frac{0.6\ \text{V}}{0.8\ \text{V}}\right) = 1.386 \quad (50)$$

Solve for C_{SS} by

$$C_{SS} = t_{SS} \times 7.21\ \mu\text{F/sec} \quad (51)$$

PCB LAYOUT GUIDELINE

In any switching converter, there are some circuit paths that carry high dI/dt, which can create spikes and noise. Other circuit paths are sensitive to noise and still others carry high dc current and can produce significant IR voltage drops. The key to proper PCB layout of a switching converter is to identify these critical paths and arrange the components and copper area accordingly. When designing PCB layouts, be sure to keep high current loops small. In addition, keep compensation and feedback components away from the switch nodes and their associated components.

The following is a list of recommended layout practices for ADP1821, arranged in approximately decreasing order of importance. A PCB layout example of the circuit shown in Figure 23 is shown in Figure 20 and Figure 21.

- The current waveform in the top and bottom FETs is a pulse with very high dI/dt, so the path to, through, and from each individual FET should be as short as possible and the two paths should be as similar as possible. In designs that use a pair of D-Paks or SO-8 FETs on one side of the PCB, it is best to counter-rotate the two so that the switch node is on one side of the pair and the high side drain can be bypassed to the low side source with a suitable ceramic bypass capacitor, placed as close as possible to the FETs to minimize inductance around this loop through the FETs and capacitor. The recommended bypass ceramic capacitor values range from 1 μF to 22 μF depending upon the output current. This bypass capacitor is usually connected to a larger value bulk filter capacitor and should be grounded to the PGND plane.
- GND, VCC bypass, soft start capacitor, and the bottom end of the output feedback divider resistors should be tied to an almost isolated, small AGND plane. All of these connections to the AGND plane should be kept as short as possible. No high current or high dI/dt signals should be connected to this AGND plane. The AGND area should be connected through one wide trace to the negative terminal of the output filter capacitors.
- The PGND pin handles high dI/dt gate drive current returning from the source of the low side MOSFET. The voltage at this pin also establishes the 0 V reference for the overcurrent limit protection (OCP) function and the CSL pin. A small PGND plane should connect the PGND pin and the PVCC bypass capacitor through a wide and direct path to the source of the low side MOSFET. The placement of C_{IN} is critical for controlling ground bounce. The negative terminal of C_{IN} needs to be placed very close to the source of the low-side MOSFET.
- Avoid long traces or large copper areas at the FB and CSL pins, which are low signal level inputs that are sensitive to capacitive and inductive noise pickup. It is best to position any series resistors and capacitors as closely as possible to these pins. Avoid running these traces close and parallel to high dI/dt traces.
- The switch node is the noisiest place in the switcher circuit with large ac and dc voltage and current. This node should be wide to minimize resistive voltage drop. But to minimize the generation of capacitively coupled noise, the total area should be small. Place the FETs and inductor close together on a small copper plane in order to minimize series resistance and keep the copper area small.
- Gate drive traces (DH and DL) handle high dI/dt and tend to produce noise and ringing. They should be as short and direct as possible. If possible, avoid using feed-through vias in the gate drive traces. If vias are needed, it is best to use two relatively large ones in parallel to reduce the peak current density and the current in each via. If the overall PCB layout is less than optimal, slowing down the gate drive slightly can be very helpful to reduce noise and ringing. It is occasionally helpful to place small value resistors (such as 5 Ω or 10 Ω) in series with the gate leads, mainly DH traces to the high side FET gates. These can be populated with 0 Ω resistors if resistance is not needed. Note that the added gate resistance increases the switching rise and fall times, and that also increases the switching power loss in the MOSFET.
- The negative terminal of output filter capacitors should be tied closely to the source of the low side FET. Doing this helps to minimize voltage difference between GND and PGND at the ADP1821.
- Generally, be sure that all traces are sized according to the current being handled as well as their sensitivity in the circuit. Standard PCB layout guidelines mainly address heating effects of current in a copper conductor. Although these are completely valid, they do not fully cover other concerns, such as stray inductance or dc voltage drop. Any dc voltage differential in connections between ADP1821 GND and the converter power output ground can cause a significant output voltage error, as it affects converter output voltage according to the ratio with the 600 mV feedback reference. For example, a 6 mV offset between ground on the ADP1821 and the converter power output causes a 1% error in the converter output voltage.

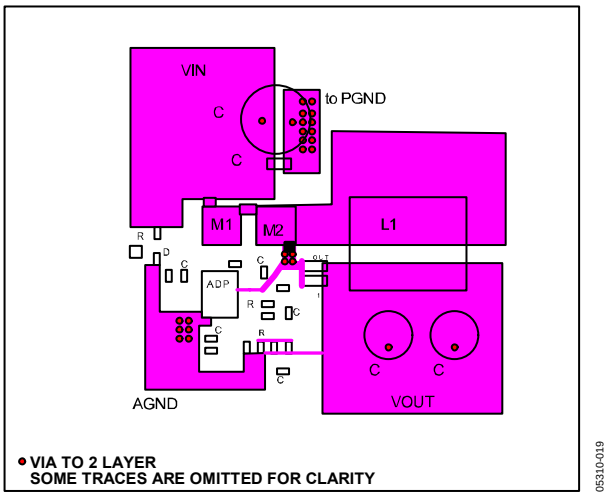

Figure 20. Top Layer Layout Example of Circuit (See Figure 23)

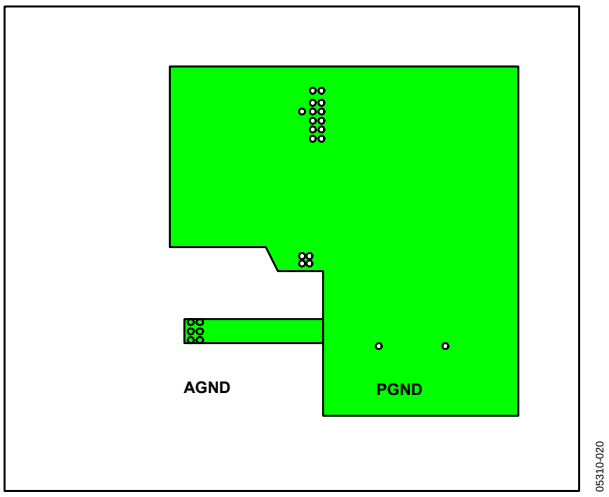

Figure 21. Bottom Layer Layout Example of Circuit (See Figure 23)

RECOMMENDED COMPONENT MANUFACTURERS

Table 4.

Vendor	Components
AVX Corporation	Capacitors
Central Semiconductor Corp.	Diodes
Coilcraft®, Inc.	Inductors
Diodes, Inc.	Diodes
International Rectifier	Diodes, MOSFETs
Murata Manufacturing Co., Ltd.	Capacitors, inductors
ON Semiconductor®	Diodes, MOSFETs
Rubycon Corporation	Capacitors
Sanyo	Capacitors
Sumida Corporation	Inductors
Taiyo Yuden, Inc.	Capacitors, inductors
Toko America, Inc.	Inductors
United Chemi-Con, Inc.	Capacitors
Vishay Siliconix	Diodes, MOSFETs, resistors, capacitors

APPLICATION CIRCUITS

The ADP1821 controller can be configured to regulate an output with a load of more than 20 A if the power components, such as the inductor, MOSFETs, and the bulk capacitors are chosen carefully to meet the power requirement. The maximum load and power dissipation are limited by the power-train components. Figure 1 shows a typical application circuit that can drive an output load of 20 A. Note that two low-side MOSFETs are needed to deliver the 20 A load. In this example, two power rails are needed: a 5 V bias supply, which needs to supply about 30 mA to power the ADP1821 at full load, and a power input rail, which ranges from 2.5 V to 20 V. The bulk input and output capacitors used in this example are Sanyo OSCON™ capacitors, which have low ESR and high current ripple rating. An alternative to the OSCON capacitors are the polymer aluminum capacitors that are available from other manufacturers such as United Chemi-Con. Aluminum electrolytic capacitors, such as the Rubycon ZLG low-ESR series, can also be paralleled up at the input or output to meet the current ripple requirement. Because the aluminum electrolytic capacitors have higher ESR and much larger variation in capacitance over the operating temperature range, a larger bulk input and output capacitance is needed to reduce the effective ESR and suppress the current ripple.

The ADP1821 can be configured to drive an output load of less than 1 A. Figure 22 shows a typical application circuit that drives a 3 A load in an all multilayer ceramic capacitor (MLCC) solution. Notice that the two MOSFETs used in this example are dual-channel MOSFETs in a PowerPAK® SO-8 package, which reduces cost and saves layout space.

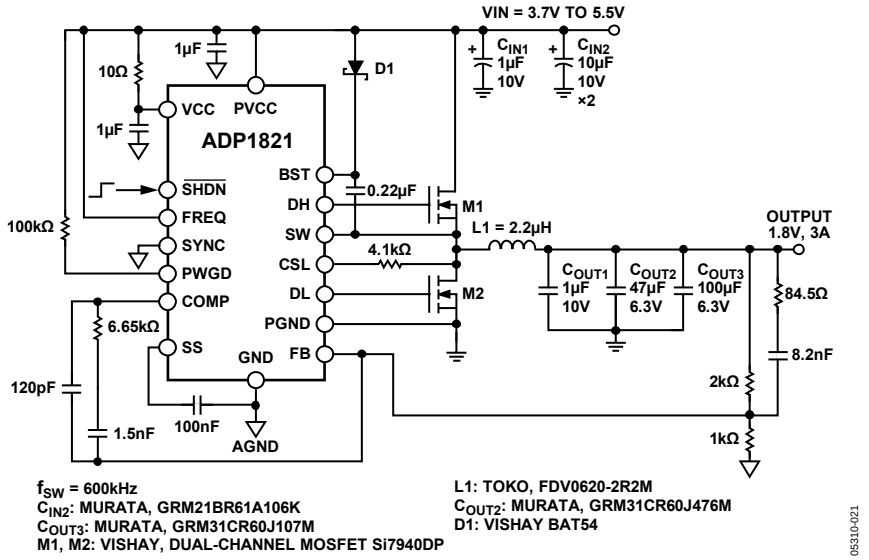

Figure 22. Typical Application Circuit with all Multilayer Ceramic Capacitors (MLCC), 3.3 V to 5 V Input

The ADP1821 can also be configured to run with an input voltage higher than 5.5 V. Figure 23 shows a typical application circuit that operates from a 12 V input. An external LDO is built, with an NPN, a 5.6 V Zener diode, and a resistor to step down the input voltage from 12 V to 5 V to power the ADP1821. These external signal components are cheap and small in size. Alternatively, LDOs such as the ADP3300 or the ADP3330 in a small SOT-23 package can be used for input voltages up to 12 V.

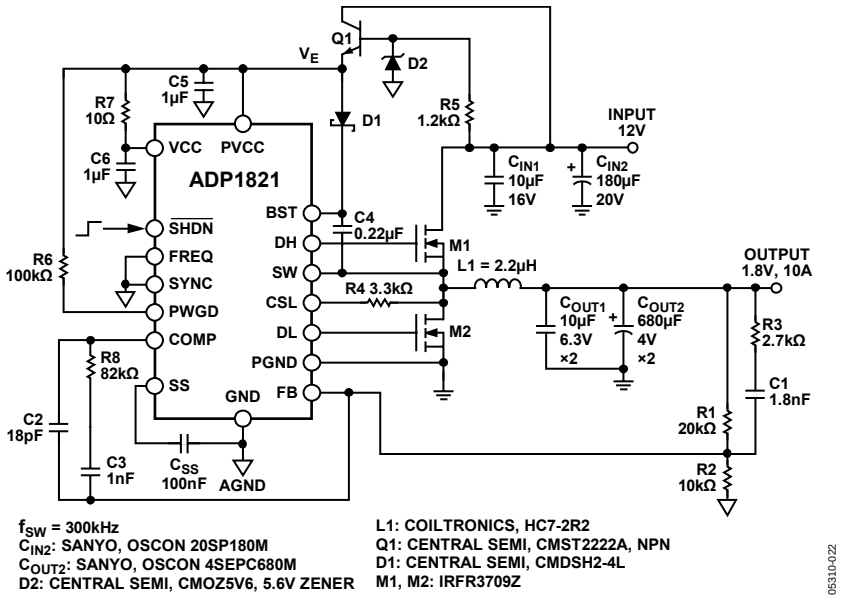

Figure 23. Typical Application Circuit, 12 V Input

OUTLINE DIMENSIONS

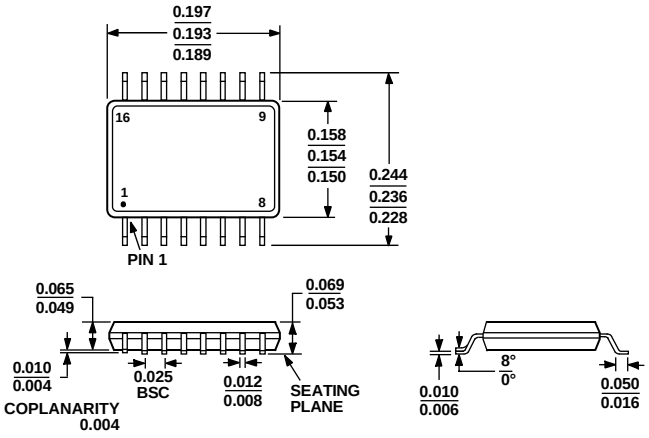

Figure 24. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches

ORDERING GUIDE

Model	Temperature Range[1]	Package Description	Package Option	Quantity
ADP1821ARQZ-R7[2]	–40°C to +85°C	16-Lead Shrink Small Outline Package [QSOP]	RQ-16	1,000
ADP1821-EVAL		Evaluation Board		

[1] Operating junction temperature is –40°C to +125°C.
[2] Z = RoHS Compliant Part.

NOTES

D05310-0-4/07(C)

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