



**THE DATASHEET OF  
ADP197ACBZ-01-R7**



## FEATURES

- Low  $R_{DS(on)}$  of 12 m $\Omega$
- Low input voltage range: 1.8 V to 5.5 V
- Quick output discharge (QOD) circuit ([ADP197-02](#))
- 3 A continuous operating current at 70°C
- 1.2 V logic-compatible enable input
- Low 18  $\mu$ A quiescent current,  $V_{IN} < 3$  V
- Low 31  $\mu$ A quiescent current,  $V_{IN} = 4.2$  V
- Overtemperature protection
- Ultralow shutdown current:  $< 1$   $\mu$ A
- Ultrasmall 1.0 mm  $\times$  1.5 mm, 0.5 mm pitch, 6-ball WLCSP
- Tiny 2.0 mm  $\times$  2.0 mm  $\times$  0.55 mm, 0.65 mm pitch, 6-lead LFCSP

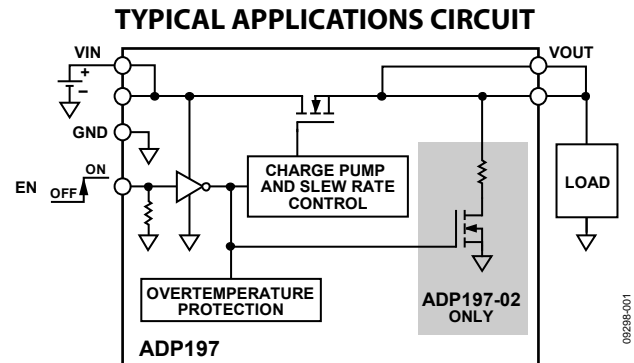
## APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- Portable and battery-powered equipment

## GENERAL DESCRIPTION

The [ADP197](#) is a high-side load switch designed for operation between 1.8 V and 5.5 V. This load switch provides power domain isolation, which helps extend battery operation. The device contains a low on-resistance, N-channel MOSFET that supports more than 3 A of continuous current and minimizes power loss. The low 18  $\mu$ A quiescent current and ultralow shutdown current make the [ADP197](#) ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the [ADP197](#) compatible with many processors and GPIO controllers.

Overtemperature protection circuitry activates if the junction temperature exceeds 125°C, thereby protecting itself and downstream circuits from potential damage.



The [ADP197-02](#) incorporates an internal quick output discharge (QOD) circuit to discharge the output capacitance when the [ADP197-02](#) output is disabled

In addition to operating performance, the [ADP197](#) WLCSP package occupies minimal printed circuit board (PCB) space with an area of less than 1.5 mm<sup>2</sup> and a height of 0.60 mm.

The [ADP197](#) is available in an ultrasmall 1.0 mm  $\times$  1.5 mm, 0.5 mm pitch, 6-ball WLCSP and a 2.0 mm  $\times$  2.0 mm  $\times$  0.55 mm, 0.65 mm pitch, 6-lead LFCSP.

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## REVISION HISTORY

### 10/14—Rev. B to Rev. C

Added 6-lead LFCSP .....	Universal
Changes to Features Section, General Description Section, and Figure 1 .....	1
Changes to Table 1.....	3
Changes to Table 3.....	4
Added Figure 4 and Table 5; Renumbered Sequentially .....	5
Added Figure 7.....	6
Changes to Figure 9.....	6
Changes to Figure 13.....	7
Changes to Theory of Operation Section.....	10
Changes to Figure 26 Caption.....	11
Changes to Figure 29 to Figure 33 and Timing Section .....	12
Added Figure 35, Outline Dimensions .....	13
Updated Outline Dimensions .....	13
Changes to Ordering Guide .....	13

### 5/12—Rev. A to Rev. B

Changes to Ordering Guide .....	13
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### 11/11—Rev. 0 to Rev. A

Changed EN to GND Rating, Table 2 .....	4
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### 4/11—Revision 0: Initial Version

## SPECIFICATIONS

$V_{IN} = 1.8\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $I_{OUT} = 1\text{ A}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	$V_{IN}$	$T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$	1.8		5.5	V
EN INPUT						
EN Input	$V_{IH}$	$V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$	1.2			V
	$V_{IL}$	$V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$ , $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$			0.4	V
		$V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$ , $T_J = -40^\circ\text{C}$ to $+110^\circ\text{C}$			0.35	V
EN Input Pull-Down Current	$I_{EN}$	$V_{IN} = 1.8\text{ V}$		500		nA
CURRENT						
Ground Current	$I_{GND}$	$V_{IN} = 1.8\text{ V}$		18		$\mu\text{A}$
		$V_{IN} = 3.4\text{ V}$		14		$\mu\text{A}$
		$V_{IN} = 4.2\text{ V}$ , $T_J = -40^\circ\text{C}$ to $+110^\circ\text{C}$		18	31	$\mu\text{A}$
		$V_{IN} = 5.5\text{ V}$		28		$\mu\text{A}$
Off State Current	$I_{OFF}$	$V_{EN} = \text{GND}$ , $V_{OUT} = 0\text{ V}$ , $V_{IN} = 4.2\text{ V}$		0.1		$\mu\text{A}$
		$V_{EN} = \text{GND}$ , $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$ , $V_{OUT} = 0\text{ V}$ , $V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$			20	$\mu\text{A}$
		$V_{EN} = \text{GND}$ , $T_J = -40^\circ\text{C}$ to $+110^\circ\text{C}$ , $V_{OUT} = 0\text{ V}$ , $V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$			75	$\mu\text{A}$
Continuous Operating Current <sup>1</sup>	$I_{OUT}$	$V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$		3		A
VIN TO VOUT RESISTANCE	$R_{DS(ON)}$					
WLCSP		$V_{IN} = 5.5\text{ V}$		0.012		$\Omega$
		$V_{IN} = 4.2\text{ V}$		0.012		$\Omega$
		$V_{IN} = 1.8\text{ V}$		0.012		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$		0.012	0.017	$\Omega$
LFCSP		$V_{IN} = 5.5\text{ V}$		0.027		$\Omega$
		$V_{IN} = 4.2\text{ V}$		0.027		$\Omega$
		$V_{IN} = 1.8\text{ V}$		0.027		$\Omega$
		$V_{IN} = 1.8\text{ V}$ , $T_J = -40^\circ\text{C}$ to $+85^\circ\text{C}$		0.027	0.036	$\Omega$
VOUT TURN-ON DELAY TIME		See Figure 2				
Turn-On Delay Time	$t_{ON\_DLY}$	$V_{IN} = 1.8\text{ V}$ to $5.5\text{ V}$ , $C_{LOAD} = 1\ \mu\text{F}$		1		ms
ACTIVE PULL-DOWN RESISTANCE (ADP197-02 OPTION ONLY)	$R_{PULLDOWN}$	$V_{IN} = 3.2\text{ V}$		380		$\Omega$
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	$T_{SD}$	$T_J$ rising		125		$^\circ\text{C}$
Thermal Shutdown Hysteresis	$T_{SD-HYS}$			15		$^\circ\text{C}$

<sup>1</sup> At an ambient temperature of  $85^\circ\text{C}$ , the device can withstand a continuous current of 2.22 A. At a load current of 3 A, the operational lifetime derates to 2190 hours.

## TIMING DIAGRAM

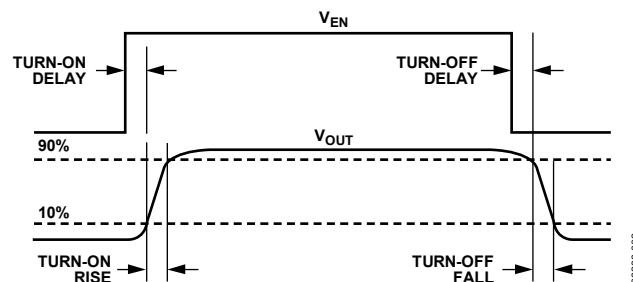


Figure 2. Timing Diagram

## ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V <sub>IN</sub> to GND	–0.3 V to +6.5 V
V <sub>OUT</sub> to GND	–0.3 V to V <sub>IN</sub>
EN to GND	–0.3 V to +6.5 V
Continuous Drain Current	
T <sub>A</sub> = 25°C	±4 A
T <sub>A</sub> = 85°C	±2.22 A
Continuous Diode Current	–50 mA
Storage Temperature Range	–65°C to +150°C
Operating Junction Temperature Range	–40°C to +105°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Typical  $\theta_{JA}$  and  $\Psi_{JB}$  Values

Package Type	$\theta_{JA}$	$\Psi_{JB}$	Unit
6-Ball, 0.5 mm Pitch WLCSP	260	58	°C/W
6-Lead, 0.65 mm Pitch LFCSP	68.9	44.1	°C/W

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

### PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

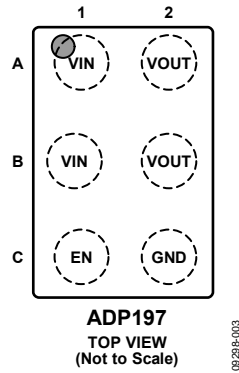
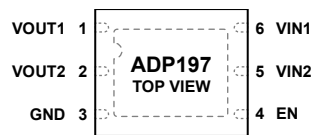


Figure 3. 6-Ball WLCSP Pin Configuration

Table 4. 6-Ball WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, B1	VIN	Input Voltage.
A2, B2	VOUT	Output Voltage.
C1	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
C2	GND	Ground.



**NOTES**  
1. EXPOSED PAD MUST BE CONNECTED TO GROUND.

Figure 4. 6-Lead LFCSP Pin Configuration

Table 5. 6-Lead LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VOUT1	Output Voltage. Connect VOUT1 and VOUT2 together.
2	VOUT2	Output Voltage. Connect VOUT1 and VOUT2 together.
3	GND	Ground.
4	EN	Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.
5	VIN2	Input Voltage. Connect VIN1 and VIN2 together.
6	VIN1	Input Voltage. Connect VIN1 and VIN2 together.
	EP	Exposed Pad. The exposed pad must be connected to ground.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 1.8\text{ V}$ ,  $V_{EN} = V_{IN}$ ,  $C_{IN} = C_{OUT} = 1\ \mu\text{F}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

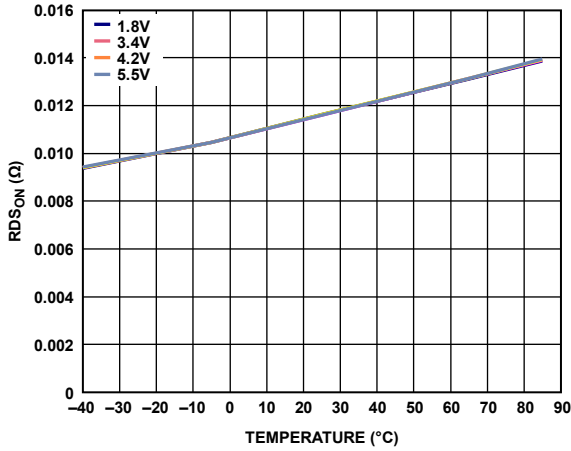


Figure 5.  $R_{DS(on)}$  vs. Temperature, 500 mA

09298-004

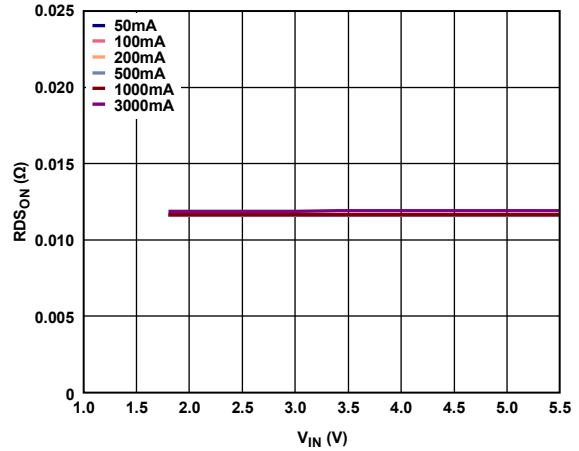


Figure 8.  $R_{DS(on)}$  vs. Input Voltage ( $V_{IN}$ ), Different Load Currents

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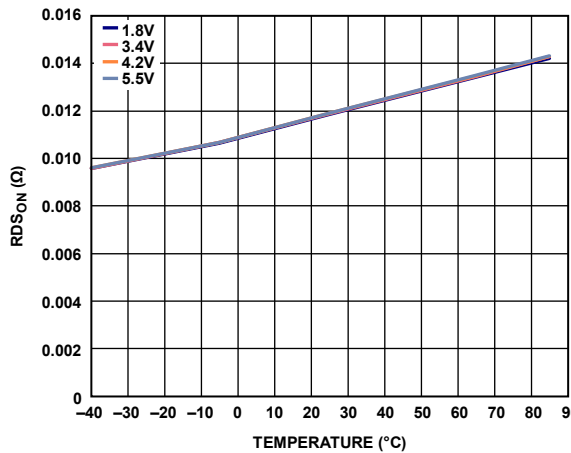


Figure 6.  $R_{DS(on)}$  vs. Temperature, 3 A, Different Input Voltages ( $V_{IN}$ )

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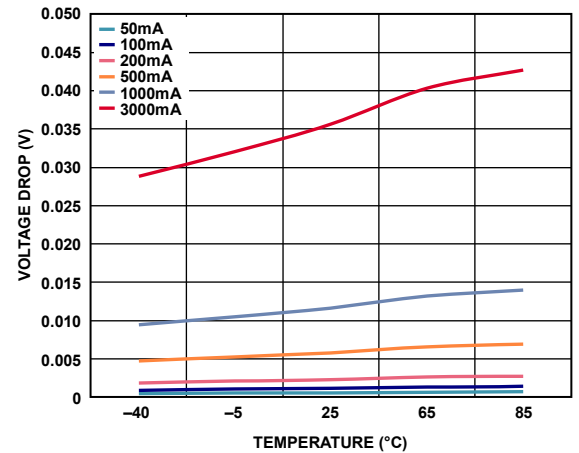


Figure 9. Voltage Drop vs. Temperature, Different Load Currents

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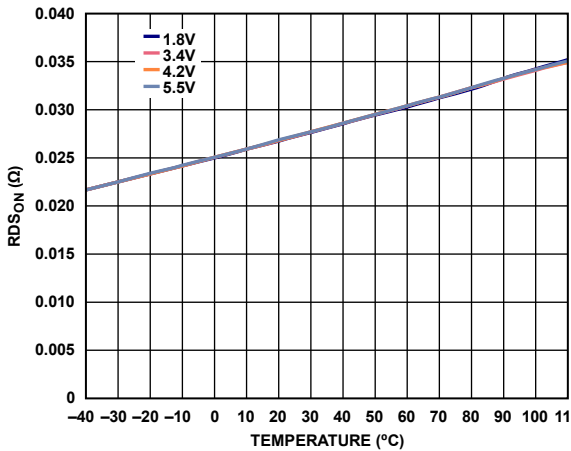


Figure 7.  $R_{DS(on)}$  (LFCSP) vs. Temperature, 500 mA, Different Input Voltages ( $V_{IN}$ )

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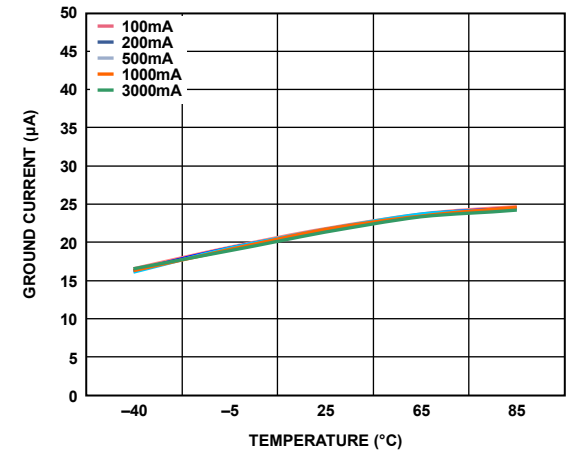


Figure 10. Ground Current vs. Temperature, Different Load Currents,  $V_{IN} = 1.8\text{ V}$

09298-016

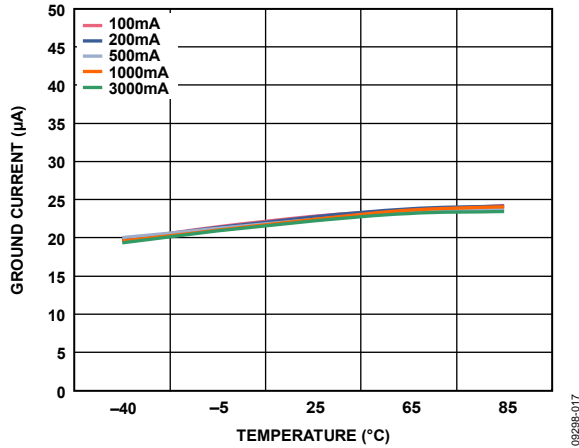


Figure 11. Ground Current vs. Temperature, Different Load Currents,  $V_{IN} = 4.2 V$

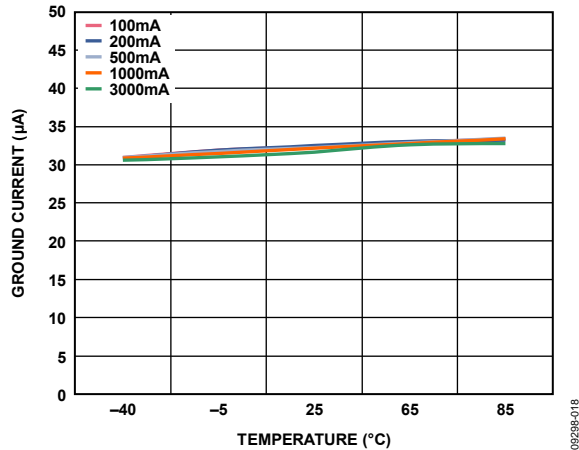


Figure 12. Ground Current vs. Temperature, Different Load Currents,  $V_{IN} = 5.5 V$

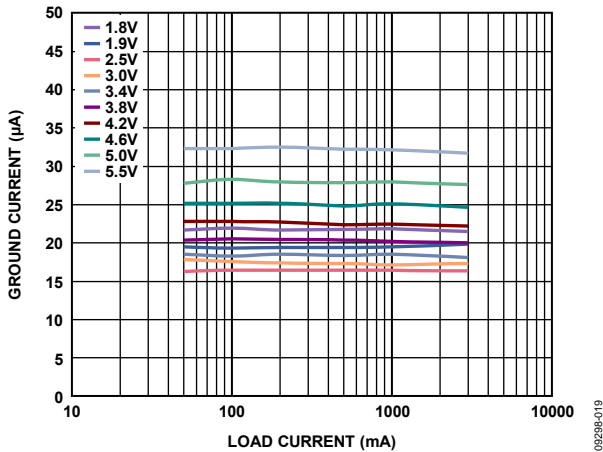


Figure 13. Ground Current vs. Load Current, Different Input Voltages ( $V_{IN}$ )

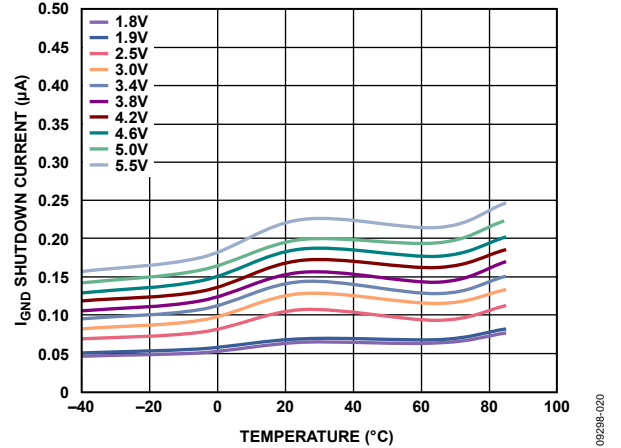


Figure 14.  $I_{GND}$  Shutdown Current vs. Temperature, Output Open, Different Input Voltages ( $V_{IN}$ )

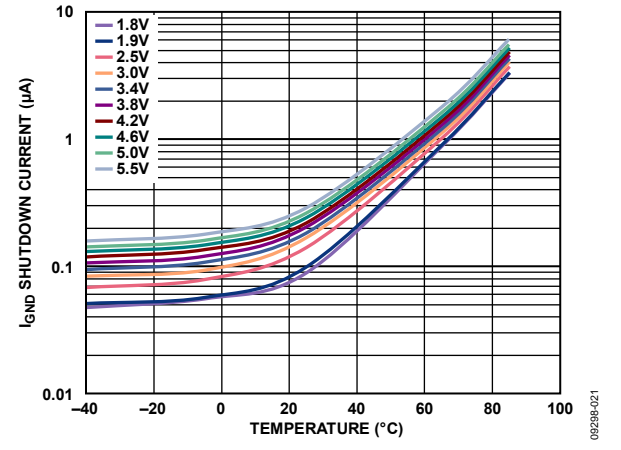


Figure 15.  $I_{GND}$  Shutdown Current vs. Temperature,  $V_{OUT} = 0 V$ , Different Input Voltages ( $V_{IN}$ )

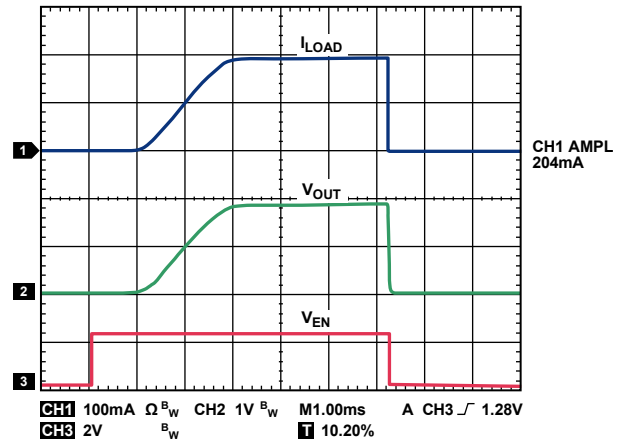


Figure 16. Typical Turn-On Time and Inrush Current,  $V_{IN} = 1.9 V$ , 200 mA Load

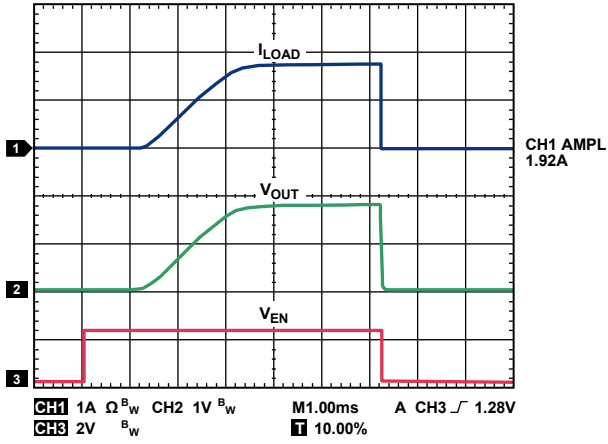


Figure 17. Typical Turn-On Time and Inrush Current,  $V_{IN} = 1.9V$ , 2A Load

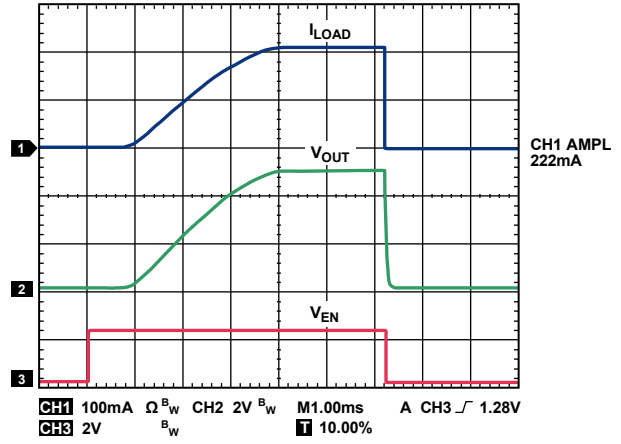


Figure 20. Typical Turn-On Time and Inrush Current,  $V_{IN} = 5.5V$ , 200mA Load

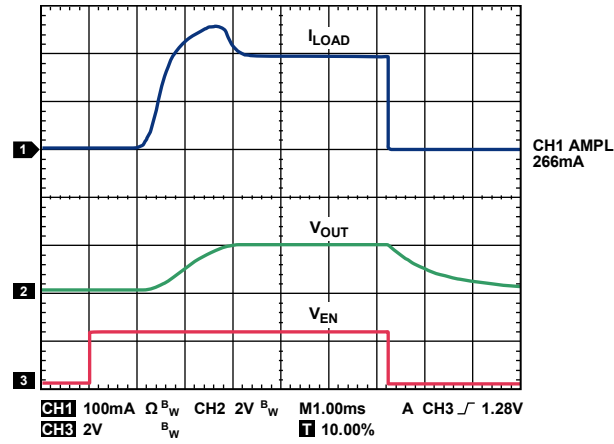


Figure 18. Typical Turn-On Time and Inrush Current,  $V_{IN} = 1.9V$ , 200mA Load,  $C_{OUT} = 100\mu F$

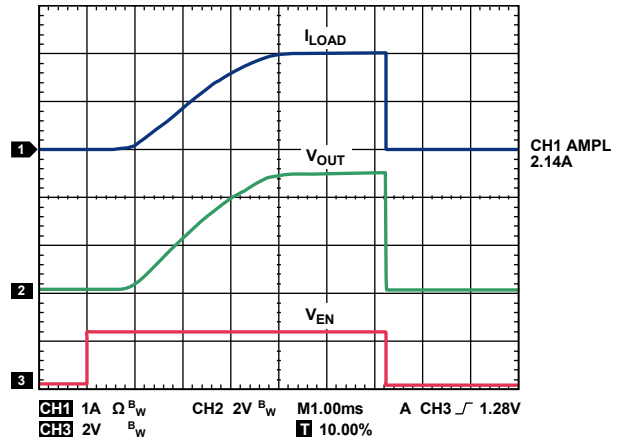


Figure 21. Typical Turn-On Time and Inrush Current,  $V_{IN} = 5.5V$ , 2A Load

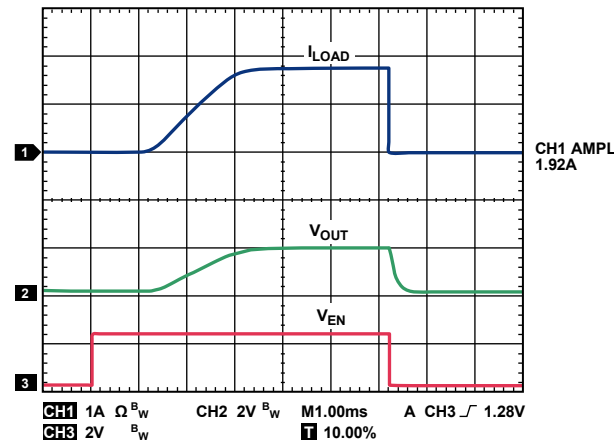


Figure 19. Typical Turn-On Time and Inrush Current,  $V_{IN} = 1.9V$ , 2A Load,  $C_{OUT} = 100\mu F$

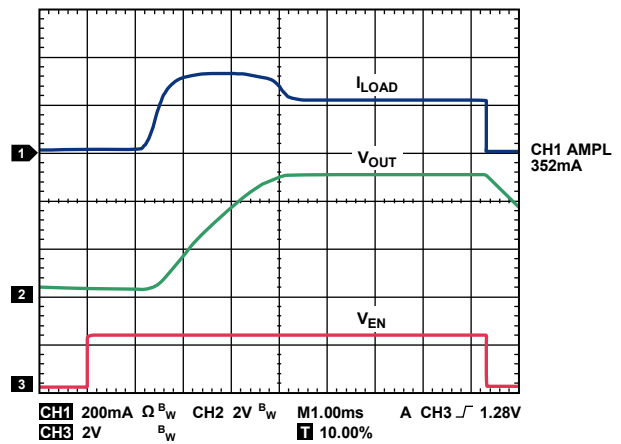


Figure 22. Typical Turn-On Time and Inrush Current,  $V_{IN} = 5.5V$ , 200mA Load,  $C_{OUT} = 100\mu F$

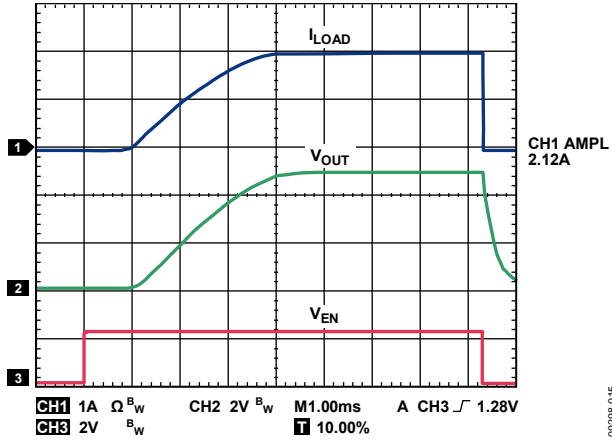


Figure 23. Typical Turn-On Time and Inrush Current,  $V_{IN} = 5.5V$ , 2 A Load,  $C_{OUT} = 100\mu F$

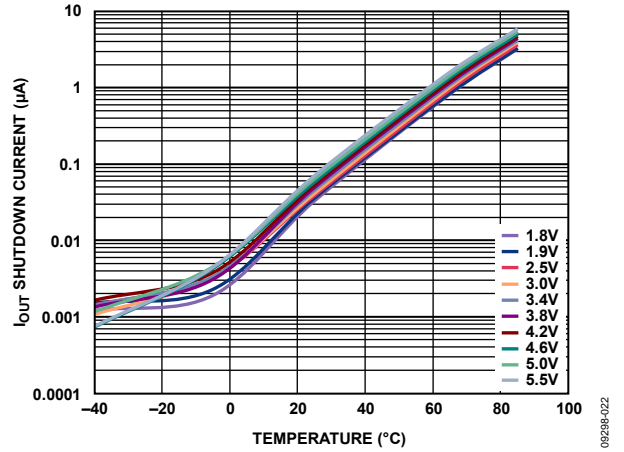


Figure 24.  $I_{OUT}$  Shutdown Current vs. Temperature,  $V_{OUT} = 0V$ , Different Input Voltages ( $V_{IN}$ )

## THEORY OF OPERATION

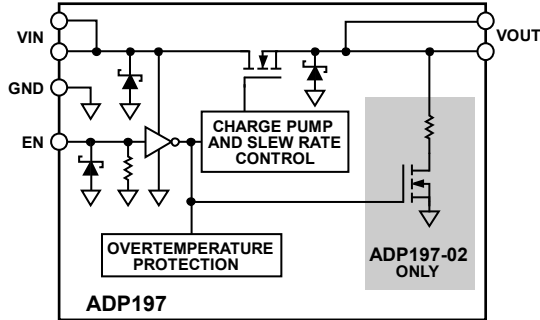


Figure 25. Functional Block Diagram

The **ADP197** is a high-side NMOS load switch, controlled by an internal charge pump. The **ADP197** is designed to operate with power supply voltages between 1.8 V and 5.5 V.

An internal charge pump biases the NMOS switch to achieve a relatively constant, ultralow on resistance of 12 m $\Omega$  across the entire input voltage range. The use of the internal charge pump also allows for controlled turn-on times. Turning the NMOS switch on and off is controlled by the enable input pin (EN), which is capable of interfacing directly with 1.8 V logic signals.

The **ADP197** is capable of 3 A of continuous operating current as long as  $T_j$  is less than 70°C. At 85°C, the rated current drops to 2.22 A.

The overtemperature protection circuit activates if the load current causes the junction temperature to exceed 125°C. When this occurs, the overtemperature protection circuitry disables the output until the junction temperature falls below approximately 110°C, at which point the output is reenabled. If the fault condition persists, the output cycles off and on until the fault is removed.

The **ADP197-02** incorporates a QOD circuit to discharge the output capacitance when the **ADP197-02** output is disabled.

ESD protection structures are shown in the block diagram as Zener diodes.

The **ADP197** is a low quiescent current device with a nominal 4 M $\Omega$  pull-down resistor on its EN pin. The package is a space-saving 1.0 mm  $\times$  1.5 mm, 0.5 mm pitch, 6-ball WLCSP and a tiny 2.0 mm  $\times$  2.0 mm  $\times$  0.55 mm, 0.65 mm pitch, 6-lead LFCSP.

## APPLICATIONS INFORMATION

### CAPACITOR SELECTION

#### Output Capacitor

The ADP197 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors when the effective series resistance (ESR) value is carefully considered. The ESR of the output capacitor affects the response to load transients. A typical 1  $\mu\text{F}$  capacitor with an ESR of 0.1  $\Omega$  or less is recommended for good transient response. Using a larger value of output capacitance improves the transient response to large changes in load current.

#### Input Bypass Capacitor

Connecting at least 1  $\mu\text{F}$  of capacitance from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when high source impedance or long input traces are encountered. When greater than 1  $\mu\text{F}$  of output capacitance is required, increase the input capacitor to match it.

### GROUND CURRENT

The major source for ground current in the ADP197 is the internal charge pump for the FET drive circuitry. Figure 26 shows the typical ground current when  $V_{\text{EN}} = V_{\text{IN}}$ , and varies from 1.8 V to 5.5 V.

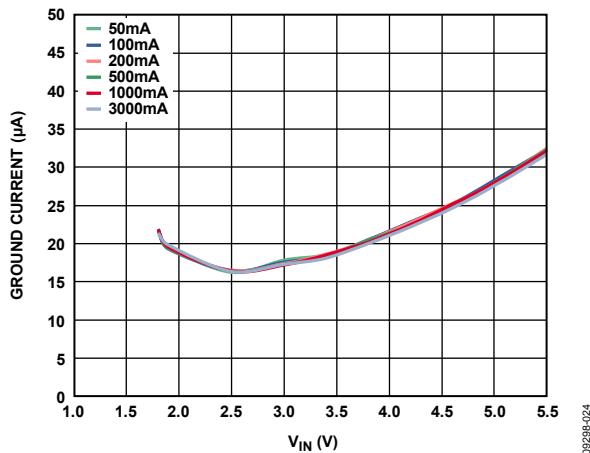


Figure 26. Ground Current vs. Input Voltage ( $V_{\text{IN}}$ ), Different Load Currents

### ENABLE FEATURE

The ADP197 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 27, when a rising voltage ( $V_{\text{EN}}$ ) on the EN pin crosses the active threshold, VOUT turns on. When a falling voltage ( $V_{\text{EN}}$ ) on the EN pin crosses the inactive threshold, VOUT turns off.

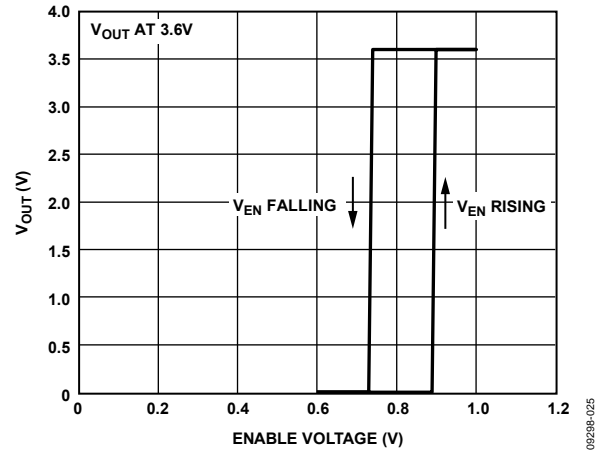


Figure 27. Typical EN Operation

As shown in Figure 27, the EN pin has hysteresis built into it. This built-in hysteresis prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active and inactive thresholds derive from the  $V_{\text{IN}}$  voltage; therefore, these thresholds vary with the changing input voltage. Figure 28 shows the typical EN active and inactive thresholds when the input voltage varies from 1.8 V to 5.5 V.

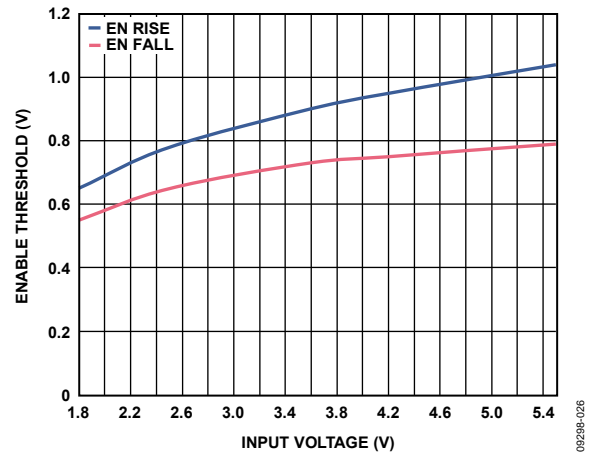


Figure 28. Typical EN Threshold vs. Input Voltage ( $V_{\text{IN}}$ )

**TIMING**

Turn-on delay is defined as the interval between the time that  $V_{EN}$  exceeds the rising threshold voltage and when  $V_{OUT}$  rises to  $\sim 10\%$  of its final value. The ADP197 includes circuitry that has a typical 1 ms turn-on delay and a controlled rise time to limit the  $V_{IN}$  inrush current. As shown in Figure 29 and Figure 30, the turn-on delay is nearly independent of the input voltage.

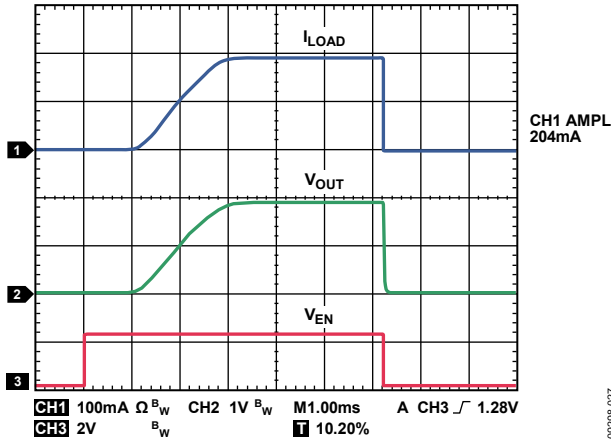


Figure 29. Typical Turn-On Delay Time with  $V_{IN} = 1.9\text{ V}$ ,  $I_{LOAD} = 200\text{ mA}$

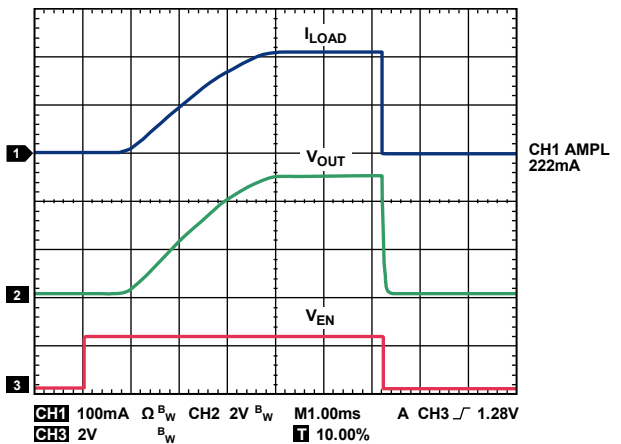


Figure 30. Typical Turn-On Delay Time with  $V_{IN} = 5.5\text{ V}$ ,  $I_{LOAD} = 220\text{ mA}$

The rise time is defined as the time it takes the output voltage to rise from 10% to 90% of  $V_{OUT}$  reaching its final value. It is dependent on the rise time of the internal charge pump.

For very large values of output capacitance, the RC time constant (where C is the load capacitance ( $C_{LOAD}$ ) and R is the  $R_{DS(ON)} || R_{LOAD}$ ) can become a factor in the rise time of the output voltage. Because  $R_{DS(ON)}$  is much smaller than  $R_{LOAD}$ , an adequate approximation for RC is  $R_{DS(ON)} \times C_{LOAD}$ . An input or load capacitor is not required for the ADP197 although capacitors can be used to suppress noise on the board. Figure 31 and Figure 32 show the inrush current when  $C_{LOAD}$  is 100  $\mu\text{F}$ .

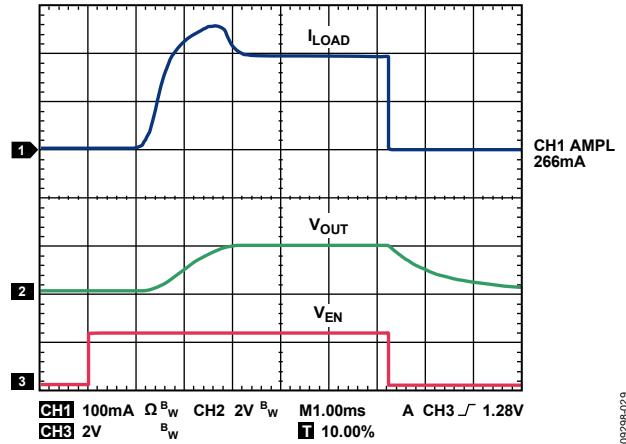


Figure 31. Typical Rise Time and Inrush Current,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $V_{IN} = 1.9\text{ V}$ ,  $I_{LOAD} = 270\text{ mA}$

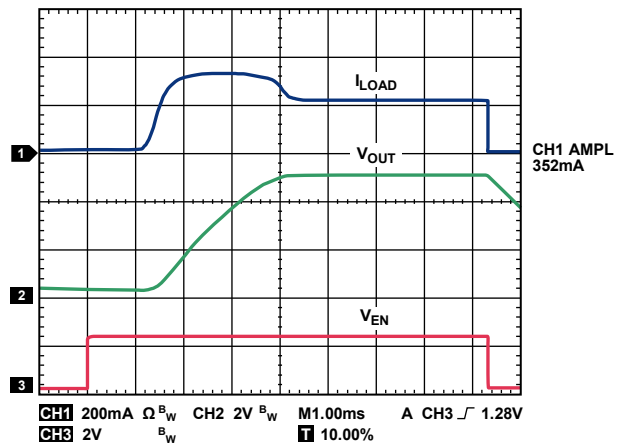


Figure 32. Typical Rise Time and Inrush Current,  $C_{LOAD} = 100\ \mu\text{F}$ ,  $V_{IN} = 5.5\text{ V}$ ,  $I_{LOAD} = 350\text{ mA}$

The turn-off time is defined as the time it takes for the output voltage to fall from 90% to 10% of  $V_{OUT}$  reaching its final value. It is also dependent on the RC time constant of the output capacitance and load resistance. Figure 33 shows the typical turn-off time with  $V_{IN} = 3.6\text{ V}$ ,  $C_{OUT} = 1\ \mu\text{F}$ , and  $R_{LOAD} = 18\ \Omega$ .

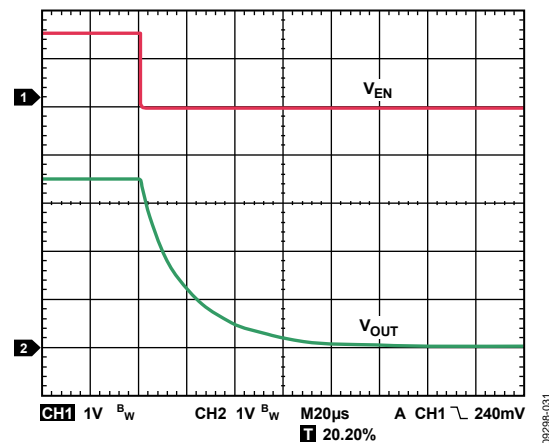


Figure 33. Typical Turn-Off Time

OUTLINE DIMENSIONS

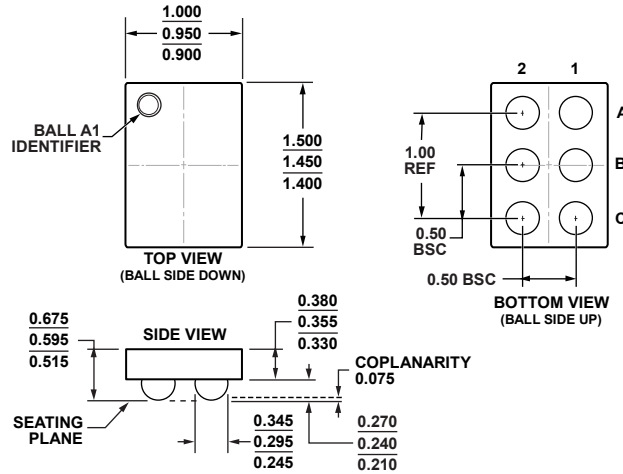


Figure 34. 6-Ball Wafer Level Chip Scale Package [WLCSP] (CB-6-2)  
Dimensions shown in millimeters

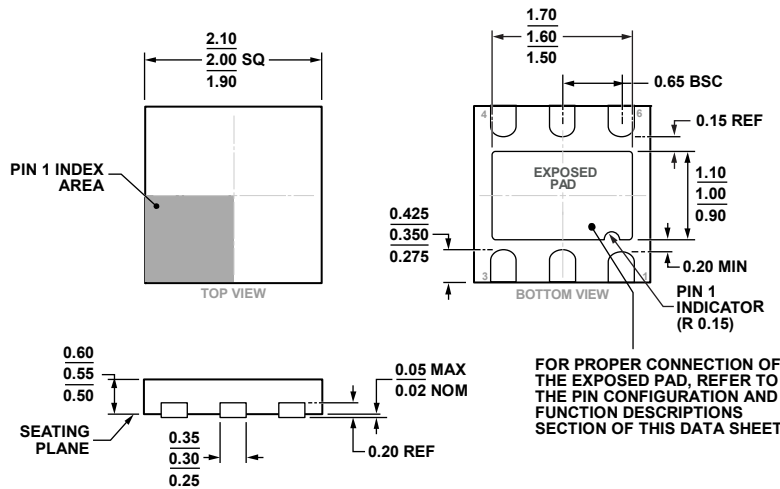


Figure 35. 6-Lead Lead Frame Chip Scale Package [LFCSP\_UD] 2.00 mm x 2.00 mm Body, Ultra Thin, Dual Lead (CP-6-3)  
Dimensions shown in millimeters

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding	On/Off Time (μs)
ADP197ACBZ-R7	-40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	87	300
ADP197ACBZ-01-R7	-40°C to +85°C	6-Ball Wafer Level Chip Scale Package [WLCSP]	CB-6-2	AP	20
ADP197ACPZN-01-R7	-40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-3	AP	20
ADP197ACPZN-02-R7	-40°C to +85°C	6-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-6-3	D8	20
ADP197CB-EVALZ		Evaluation Board			
ADP197CP-EVALZ		Evaluation Board			

<sup>1</sup> Z = RoHS Compliant Part.

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